Compal Confidential

Schematic Document

Crestline + ICH8M

2008 / 02 / 18 Rev:0.3

Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

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Title: *Cover Sheet*

Size: Custom | Document Number: *LA-4131P* | Rev: 0.2

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Project Code: ANRJAL6000 (JAL60)

File Name : LA-4131P

JAL60 UMA / Discrete

ZZZ1
PCB

Thermal Sensor
ADM1032ARMZ
P4

Fan conn
P4

Mobile Merom
uFCPGA-478 CPU
P4, 5, 6

CK505 TSSOP-64
Clock Generator
ICS 9LPRS365
P16

CRT
P15

LVDS Panel Interface
P15

GDDR3 x 4
P39 , 40

nVidia
NB8P-SE
P34 ~ 38

PCI-E x16

H_A#(3..35)
H_D#(0..63)

FSB
667/800MHz 1.05V

Intel Crestline MCH
FCBGA 1299
P7, 8, 9, 10, 11, 12

DDR2 667MHz 1.8V

Dual Channel

DDR2-SO-DIMM X2
BANK 0, 1, 2, 3
P13, 14

CardBus Controller
O2 OZ129
P25

PCI

DMI x4

C-Link

Media Card

1394

Express Card
P26

PCIE2

PCI-E x1

Intel ICH8M
mBGA-676
P17, 18, 19, 20

USB2.0
Azalia
SATA0
SATA1
PATA

USB0 Finger Printer P31
USB1 Blue Tooth P31
USB2,3 JUSBP5 Conn. P30
USB4 JUSBP1 Conn. P30
USB5 USB Hub P31
USB6 JUSBP4 Conn. P30
USB7 Express Card P26
USB8 JUSBP3 Conn. P30
USB9 JUSBP2 Conn. P30

Camera P31
Felica P31

PCIE5 10/100/1000 LAN
REALTEK
RTL8111C-GR
P22

RJ45 CONN
P22

PCIE4 Mini Card-1
(WLAN)
P27

PCIE3 Mini Card-2
(Robson)
P27

LPC BUS

Option
TPM1.2
P28

ENE KB926
P28

Touch Pad Conn
P29

Int.KBD
P29

BIOS (System/EC)
P28

Audio CKT
ALC268
P23

AMP & Audio Jack
P24

SATA HDD1 Conn.
P21

SATA HDD2 Conn.
P21

ODD Conn.
P21

Power On/Off CKT.
P29

DC/DC Interface CKT.
P32

RTC CKT.
P18

Power Circuit DC/DC
P41~48

Power OK CKT.
P29

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Title: **Block Diagram**

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Voltage Rails

O MEANS ON X MEANS OFF

State \ Power plane	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.8VS +1.5VS +1.25VS +1.2VS +0.9VS +CPU_CORE +VGA_CORE +VCCP	CLOCK
S0	O	O	O	O	O
S3	O	O	O	X	O
S5 S4/AC	O	O	X	X	O
S5 S4/ Battery only	O	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra / Rc	100K +/- 5%

Board ID	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

O MEANS ON
X MEANS OFF

S3 : STR
S4 : STD
S5 : SOFT OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD21	0	PIRQG

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b?
EEPROM(24C16/02)	1010 000X b?
(24C04)	1011 000Xb?

EC SM Bus2 address

Device	Address	
EMC1402-1-ACZL-TR_MSOP8	4C	for CPU Thermal Sensor

ICH8 SM Bus address

Device	Address
Clock Generator (ICS ICS9LPR365)	1101 001Xb?
DDRII DIMM1	1001 000Xb?
DDRII DIMM2	1001 010Xb?

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Title: Notes

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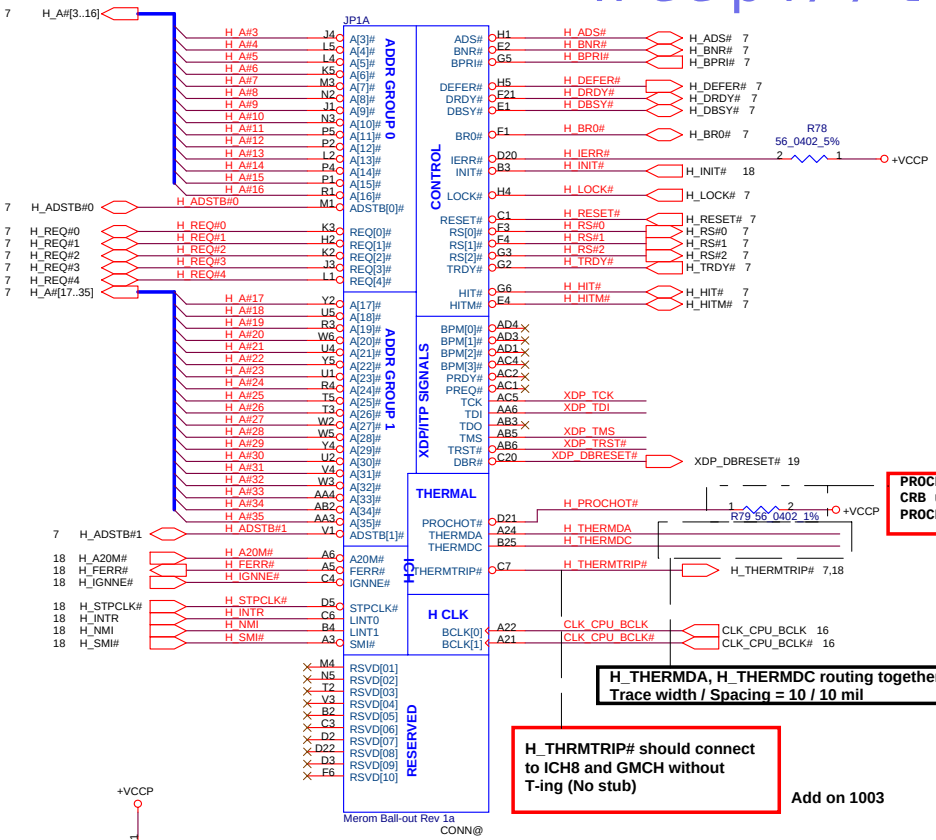
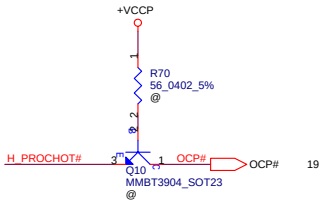
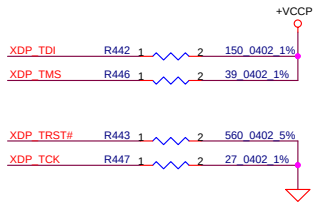
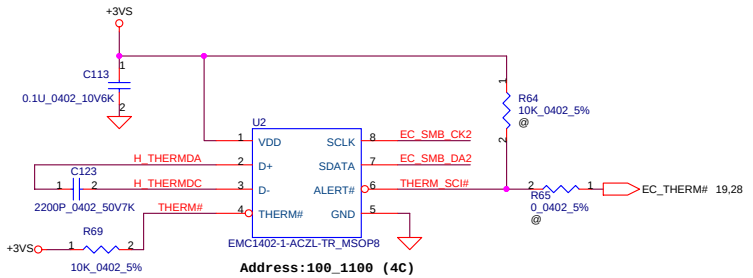




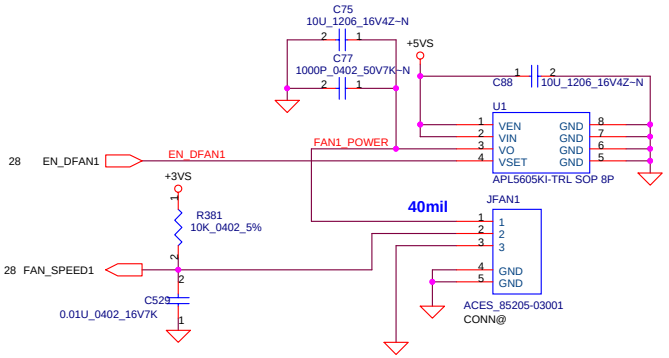
XDP Reserve



Thermal Sensor ADM1032ARMZ



Fan Control and Tachometer



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Compal Electronics, Inc.			
Title: Merom(1/3)_AGTL+ / XDP			
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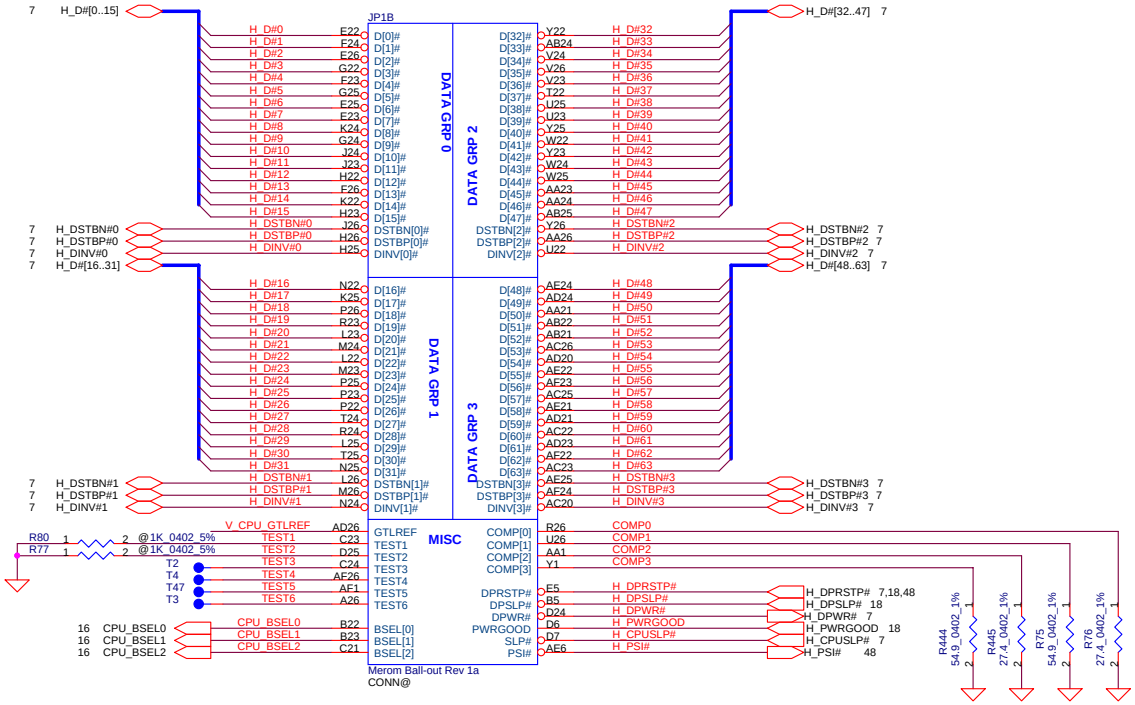
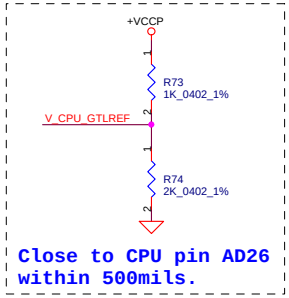


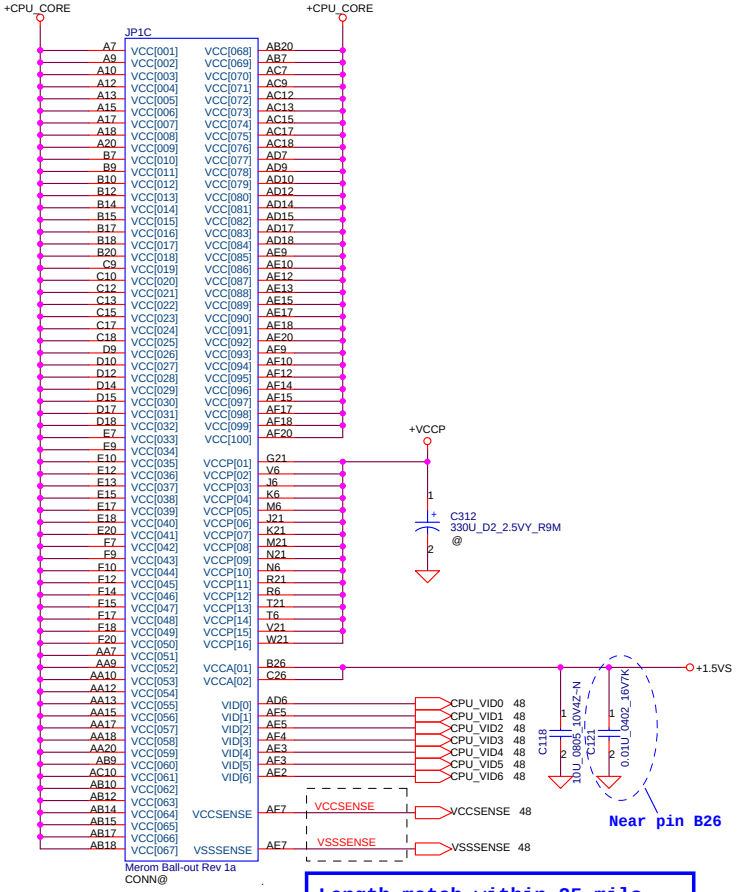
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

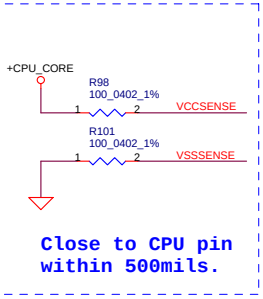
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Close to CPU pin AD26 within 500mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin within 500mils.

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Compal Electronics, Inc.

Title: Merom(2/3)_AGTL+ / PWR

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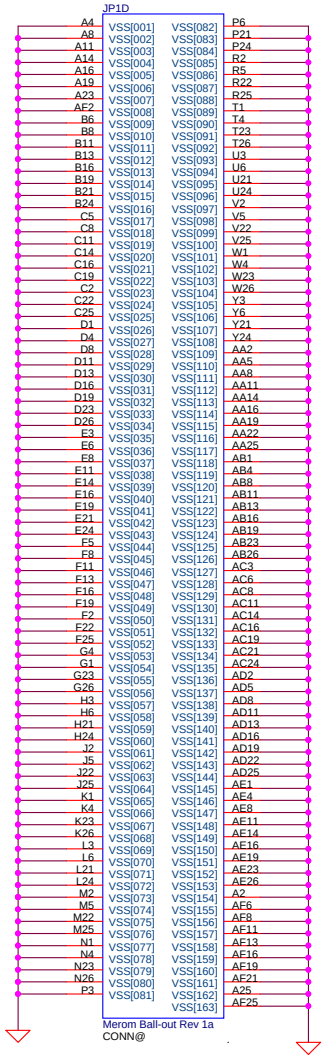
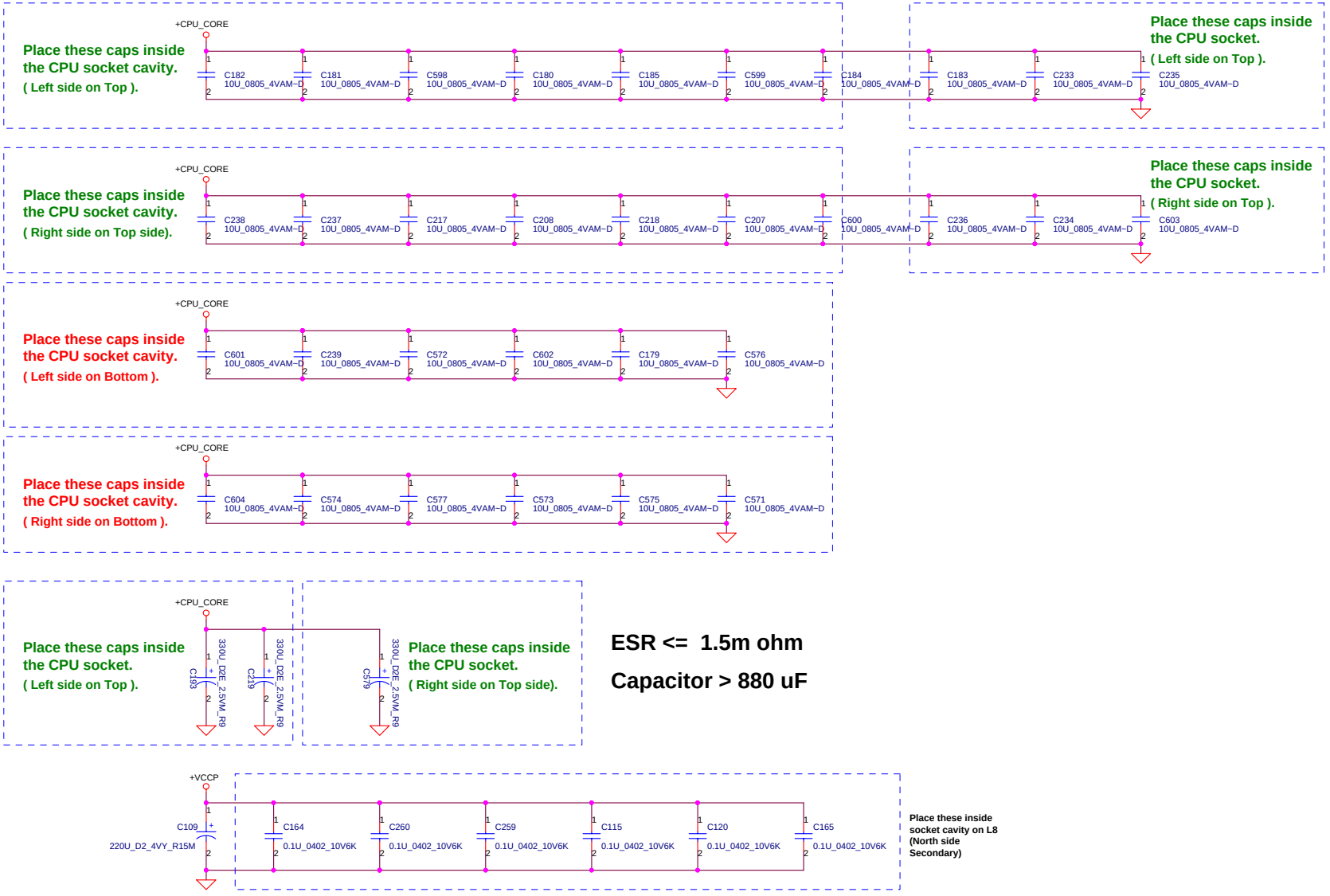
High Frequence Decoupling

10uF 0805 X5R -> 85 degree.





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Compal Electronics, Inc.

Title: **Merom(3/3)_GND / Bypass**

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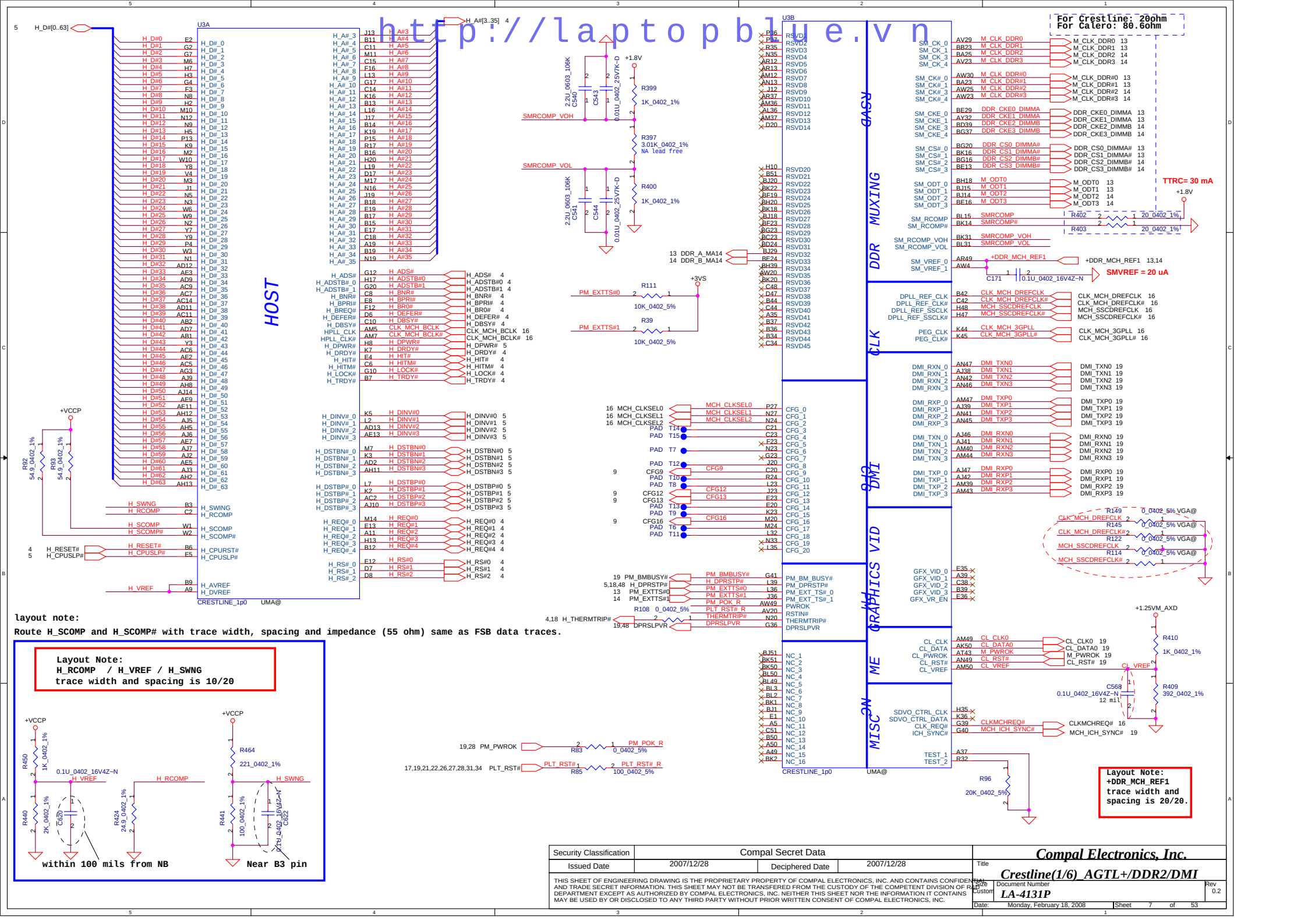

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Compal Electronics, Inc.			
Title: Crestline(1/6)_AGTL+/DDR2/DMI			
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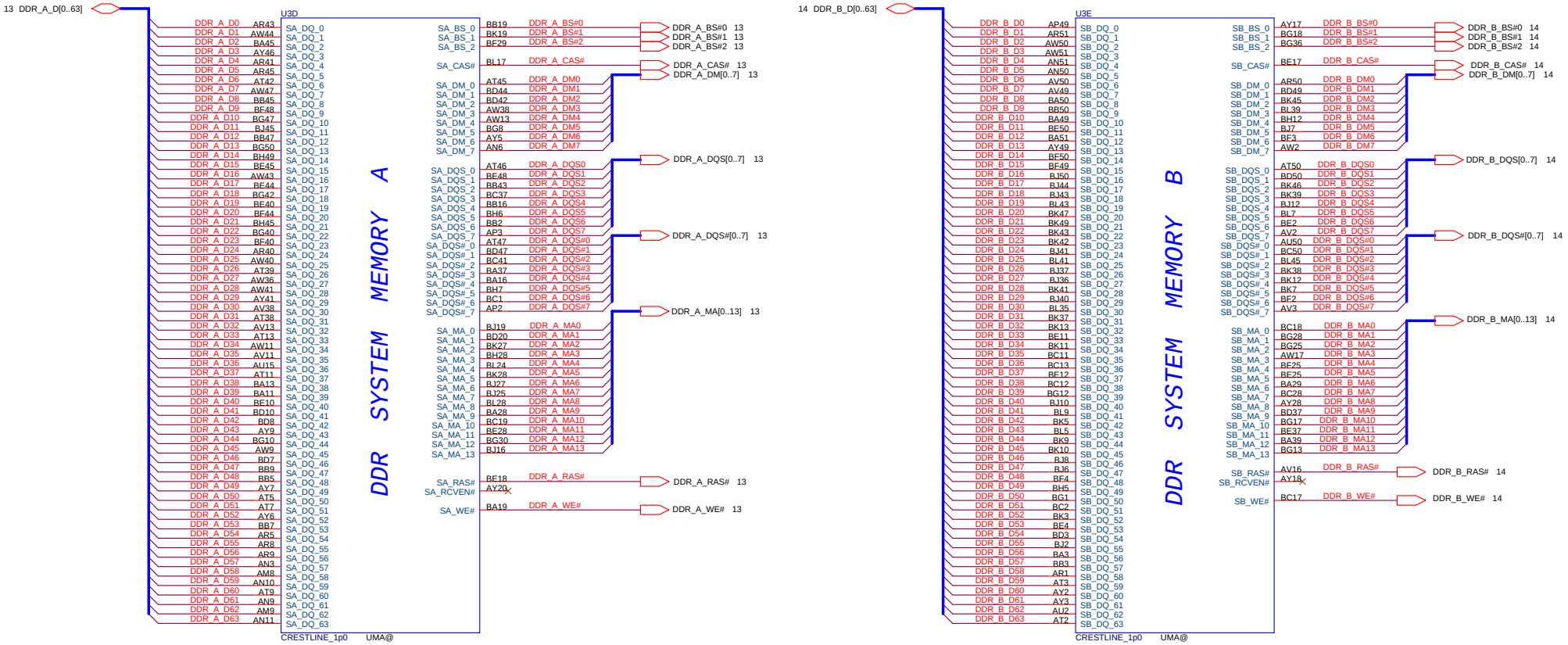

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Compal Electronics, Inc.

Title: Crestline(2/6)_DDR2 Channel A/B

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For Crestline:2.4kohm
For Calero: 1.5Kohm

PEGCOMP trace width and spacing is 20/25 mils.

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

For Crestline:1.3kohm
For Calero: 255ohm

Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

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Title: Crestline(3/6)_LVDS / CRT/ PCIE

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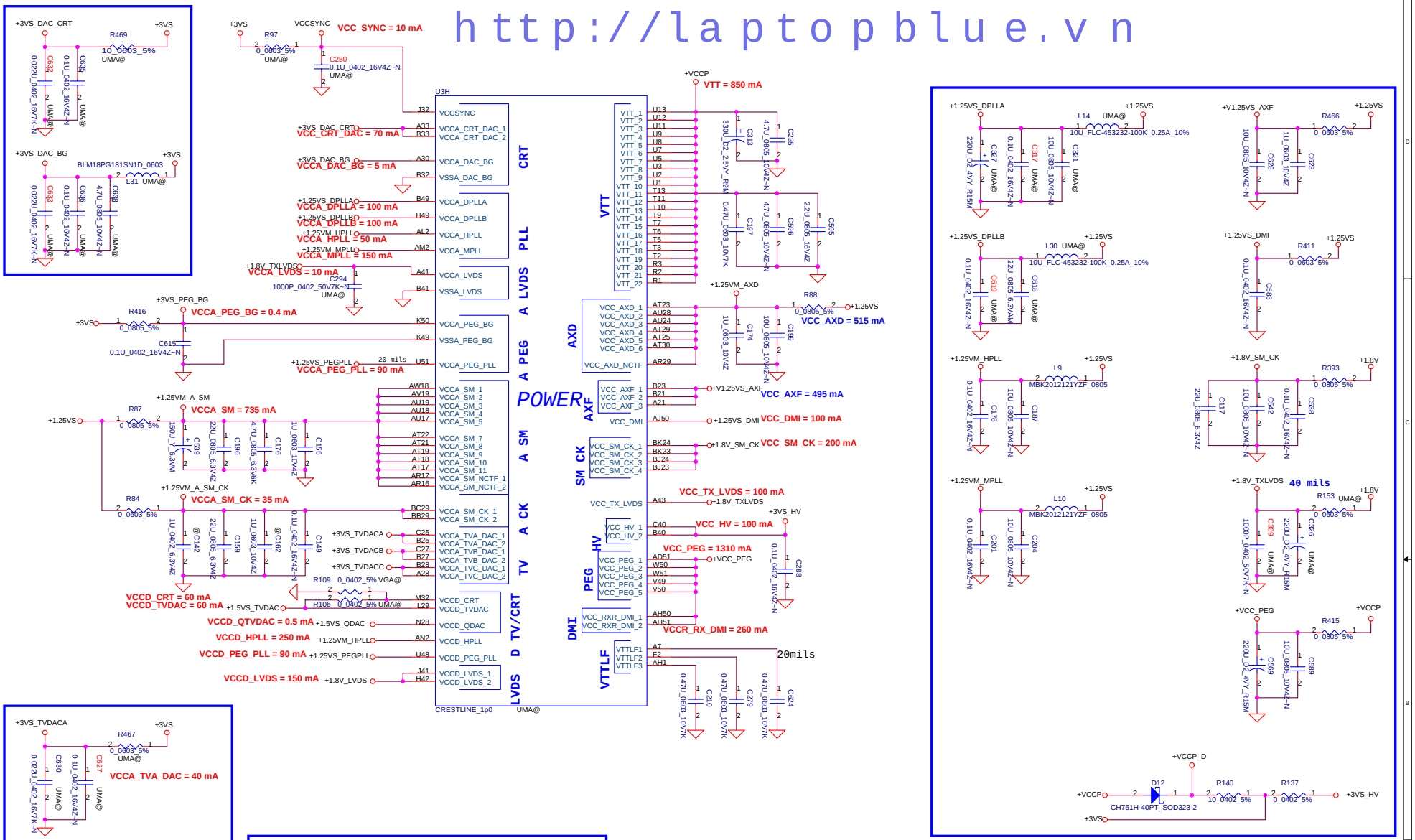

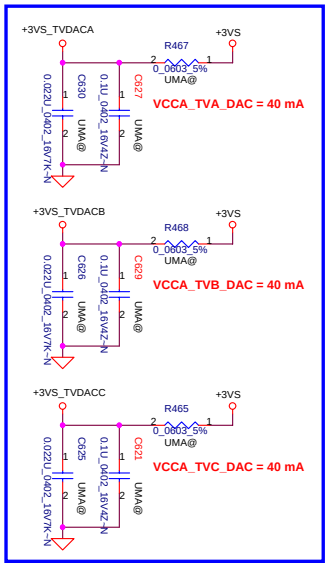

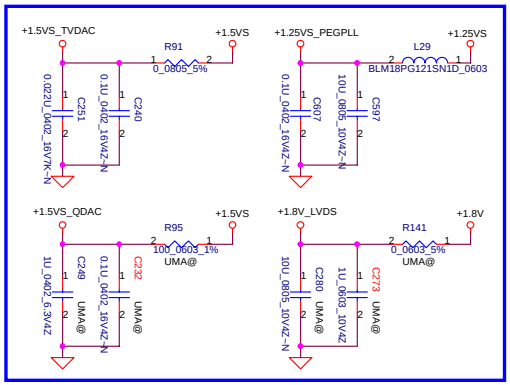

For Discrete BOM

C633	C627	C621	C273	C619	U3
0_0402_5% VGA@	0_0402_5% VGA@	0_0402_5% VGA@	0_0603_5% VGA@	0_0402_5% VGA@	PM965_C0 VGA@
C632	**C629**	**C232**	**C309**	**C250**	**C317**
0_0402_5% VGA@	0_0402_5% VGA@	0_0402_5% VGA@	0_0402_5% VGA@	0_0402_5% VGA@	0_0402_5% VGA@

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Compal Electronics, Inc.

Title: *Crestline(4/6)_PWR*

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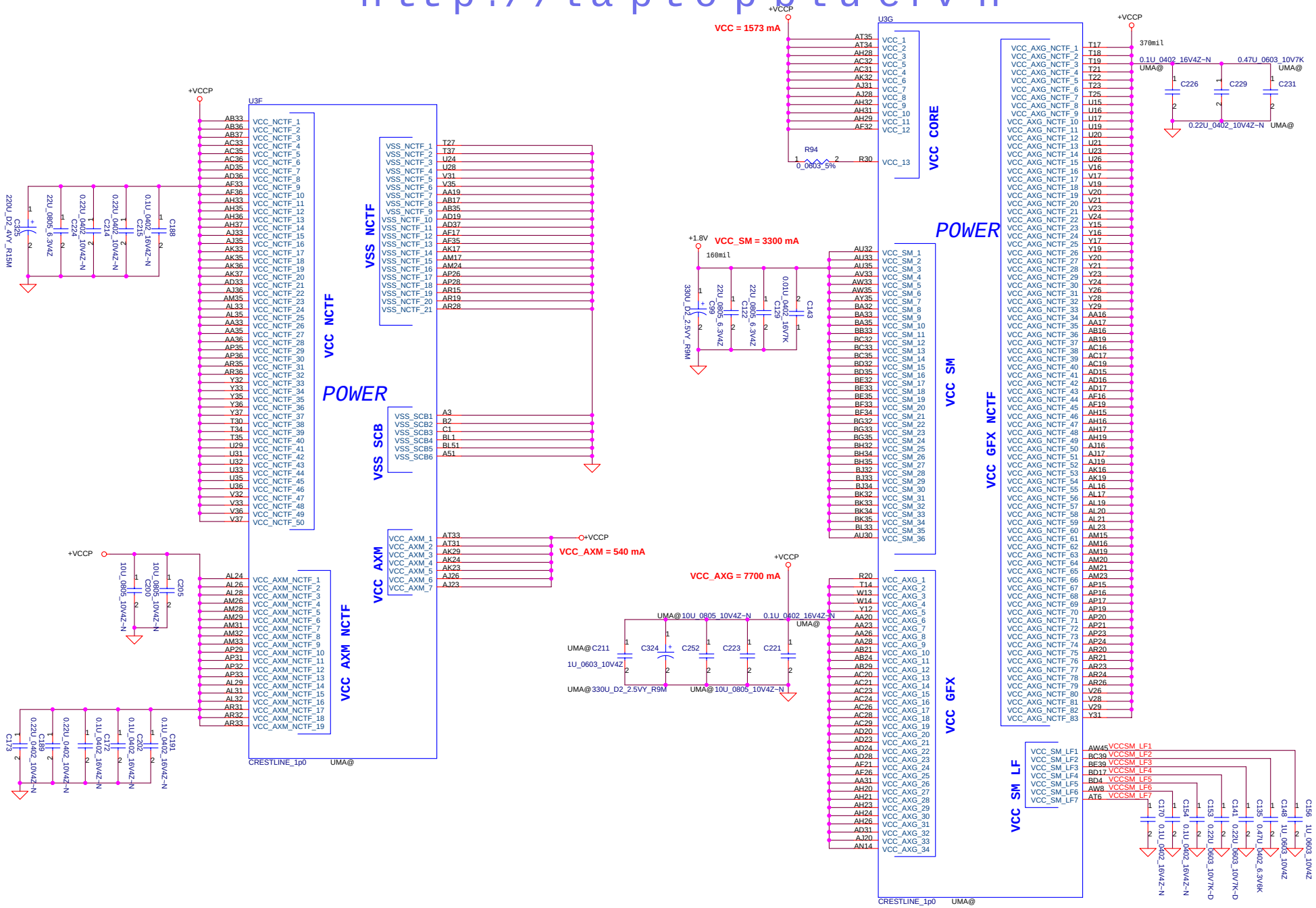

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Title: Crestline(5/6)_PWR / GND

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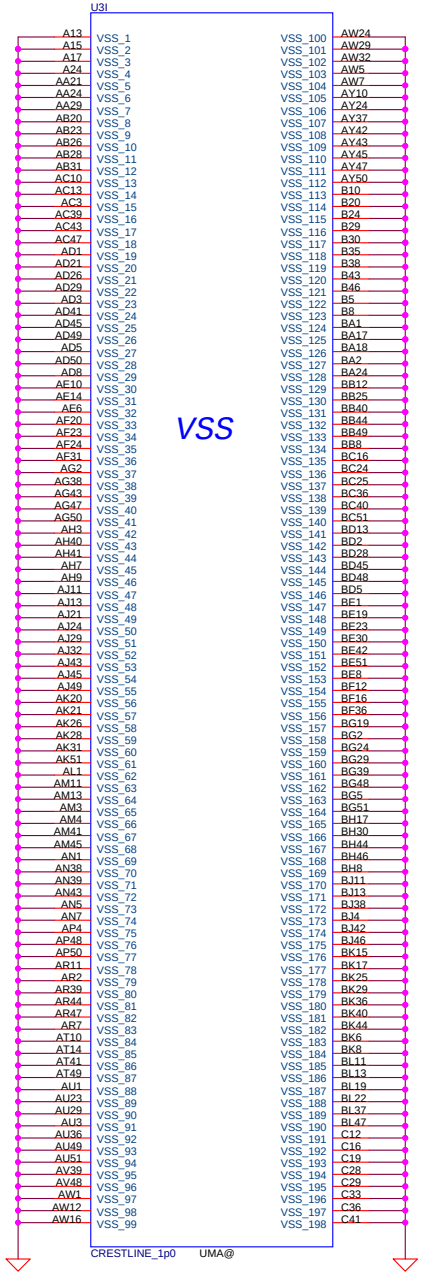

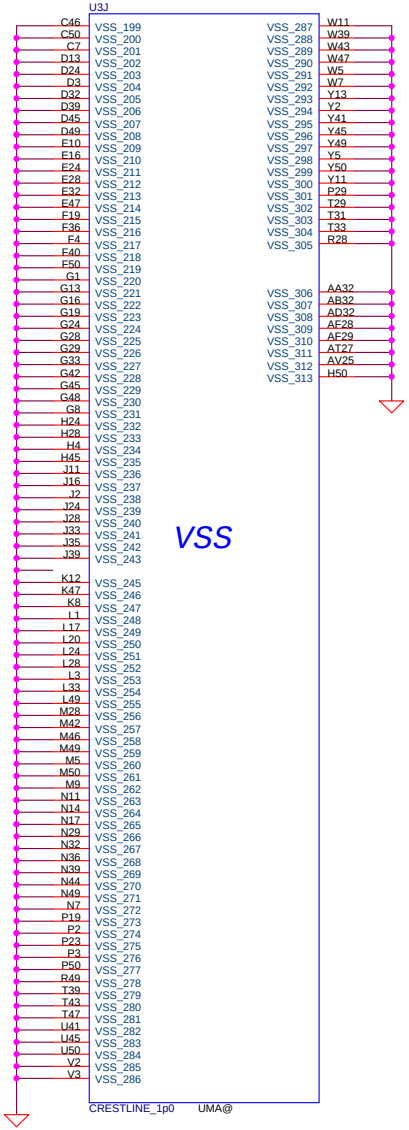

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Compal Electronics, Inc.

Title: Crestline(6/6)_GND

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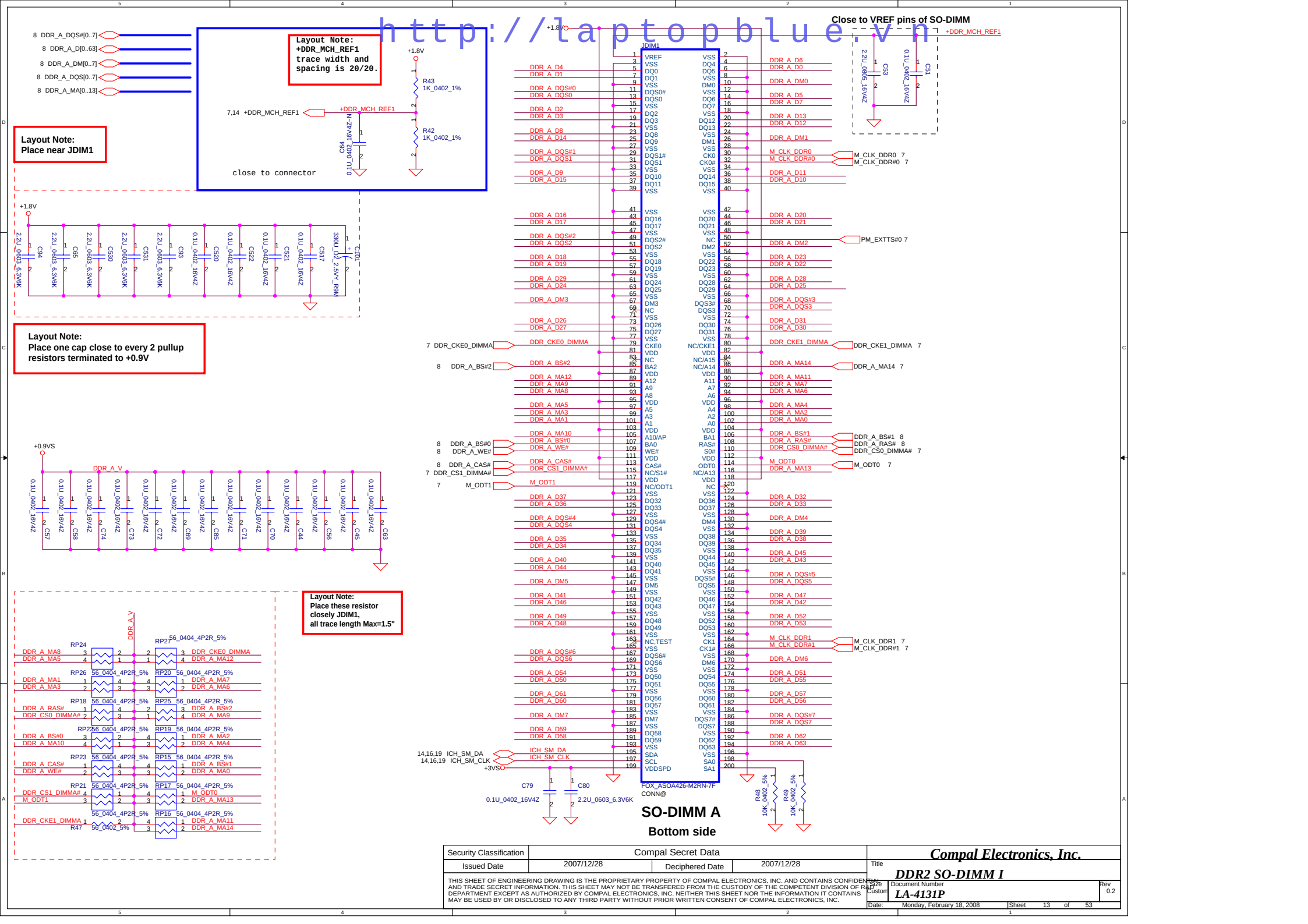

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Compal Electronics, Inc.			
Title: DDR2 SO-DIMM I			
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8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..13]

Layout Note:
Place near JDIM2

+1.8V
2.2U_0603_6.3V6K C49, C67, C66, C76, C78
0.1U_0402_16V4Z C523, C518, C519, C68
330U_D2_2.5V-Y_R9M C100@

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

+0.9VS
DDR_B_V
0.1U_0402_16V4Z C83, C81, C62, C82, C84, C86, C87, C59, C61, C60, C47, C48, C46

Layout Note:
Place these resistor closely JDIM2, all trace length Max=1.5"

DDR_B_V
RP14 56_0404_4P2R_5%: DDR_CKE2_DIMMB, DDR_B_BS#2 / DDR_B_MA7, DDR_B_MA6
RP10 56_0404_4P2R_5%: DDR_B_MA8, DDR_B_MA5 / DDR_B_MA4, DDR_B_MA2
RP6 56_0404_4P2R_5%: DDR_CS2_DIMMB#, DDR_B_BS#1 / DDR_B_MA12, DDR_B_MA9
RP12 56_0404_4P2R_5%: DDR_B_WE#, DDR_B_CAS# / DDR_B_MA0, DDR_B_RAS#
RP9 56_0404_4P2R_5%: DDR_B_MA10, DDR_B_BS#0 / DDR_B_MA3, DDR_B_MA1
RP8 56_0404_4P2R_5%: M_ODT3, DDR_CS3_DIMMB# / DDR_B_MA13, M_ODT2
RP4 56_0404_4P2R_5%
RP3 56_0404_4P2R_5%
RP11 56_0404_4P2R_5%
RP7 56_0404_4P2R_5%
RP13 56_0404_4P2R_5%
RP2 56_0404_4P2R_5%
RP5 56_0404_4P2R_5%: DDR_B_MA14, DDR_B_MA11
DDR_CKE3_DIMMB — R36 56_0402_5% — RP5

+1.8V
DDR_MCH_REF1
Close to VREF pins of SO-DIMM
2.2U_0805_16V4Z C52, 0.1U_0402_16V4Z C50
+DDR_MCH_REF1 7,13

JDIM2
FOX_AS0A426-NARN-7F-N
CONN@

1 VREF	2 VSS		
3 VSS	4 DQ4	DDR_B_D0	DDR_B_D5
5 DQ0	6 DQ5	DDR_B_D1	DDR_B_D4
7 DQ1	8 VSS		
9 VSS	10 DM0		DDR_B_DM0
11 DQS0#	12 VSS	DDR_B_DQS#0	
13 DQS0	14 DQ6	DDR_B_DQS0	DDR_B_D6
15 VSS	16 DQ7		DDR_B_D7
17 DQ2	18 VSS	DDR_B_D2	
19 DQ3	20 DQ12	DDR_B_D3	DDR_B_D12
21 VSS	22 DQ13		DDR_B_D13
23 DQ8	24 VSS	DDR_B_D8	
25 DQ9	26 DM1	DDR_B_D9	DDR_B_DM1
27 VSS	28 VSS		
29 DQS1#	30 CK0	DDR_B_DQS#1	M_CLK_DDR2 — M_CLK_DDR2 7
31 DQS1	32 CK0#	DDR_B_DQS1	M_CLK_DDR#2 — M_CLK_DDR#2 7
33 VSS	34 VSS		
35 DQ10	36 DQ14	DDR_B_D10	DDR_B_D14
37 DQ11	38 DQ15	DDR_B_D11	DDR_B_D15
39 VSS	40 VSS		
41 VSS	42 VSS		
43 DQ16	44 DQ20	DDR_B_D17	DDR_B_D21
45 DQ17	46 DQ21	DDR_B_D20	DDR_B_D16
47 VSS	48 VSS		
49 DQS2#	50 NC	DDR_B_DQS#2	PM_EXTTS#1 7
51 DQS2	52 DM2	DDR_B_DQS2	DDR_B_DM2
53 VSS	54 VSS		
55 DQ18	56 DQ22	DDR_B_D18	DDR_B_D22
57 DQ19	58 DQ23	DDR_B_D19	DDR_B_D23
59 VSS	60 VSS		
61 DQ24	62 DQ28	DDR_B_D28	DDR_B_D26
63 DQ25	64 DQ29	DDR_B_D25	DDR_B_D24
65 VSS	66 VSS		
67 DM3	68 DQS3#	DDR_B_DM3	DDR_B_DQS#3
69 NC	70 DQS3		DDR_B_DQS3
71 VSS	72 VSS		
73 DQ26	74 DQ30	DDR_B_D30	DDR_B_D29
75 DQ27	76 DQ31	DDR_B_D31	DDR_B_D27
77 VSS	78 VSS		
79 CKE0	80 NC/CKE1	7 DDR_CKE2_DIMMB — DDR_CKE2_DIMMB	DDR_CKE3_DIMMB — DDR_CKE3_DIMMB 7
81 VDD	82 VDD		
83 NC	84 NC/A15		
85 BA2	86 NC/A14	8 DDR_B_BS#2 — DDR_B_BS#2	DDR_B_MA14 — DDR_B_MA14 7
87 VDD	88 VDD		
89 A12	90 A11	DDR_B_MA12	DDR_B_MA11
91 A9	92 A7	DDR_B_MA9	DDR_B_MA7
93 A8	94 A6	DDR_B_MA8	DDR_B_MA6
95 VDD	96 VDD		
97 A5	98 A4	DDR_B_MA5	DDR_B_MA4
99 A3	100 A2	DDR_B_MA3	DDR_B_MA2
101 A1	102 A0	DDR_B_MA1	DDR_B_MA0
103 VDD	104 VDD		
105 A10/AP	106 BA1	DDR_B_MA10	DDR_B_BS#1 — DDR_B_BS#1 8
107 BA0	108 RAS#	8 DDR_B_BS#0 — DDR_B_BS#0	DDR_B_RAS# — DDR_B_RAS# 8
109 WE#	110 S0#	8 DDR_B_WE# — DDR_B_WE#	DDR_CS2_DIMMB# — DDR_CS2_DIMMB# 7
111 VDD	112 VDD		
113 CAS#	114 ODT0	8 DDR_B_CAS# — DDR_B_CAS#	M_ODT2 — M_ODT2 7
115 NC/S1#	116 NC/A13	7 DDR_CS3_DIMMB# — DDR_CS3_DIMMB#	DDR_B_MA13 — DDR_B_MA13
117 VDD	118 VDD		
119 NC/ODT1	120 NC	7 M_ODT3 — M_ODT3	
121 VSS	122 VSS		
123 DQ32	124 DQ36	DDR_B_D32	DDR_B_D36
125 DQ33	126 DQ37	DDR_B_D33	DDR_B_D37
127 VSS	128 VSS		
129 DQS4#	130 DM4	DDR_B_DQS#4	DDR_B_DM4
131 DQS4	132 VSS	DDR_B_DQS4	
133 VSS	134 DQ38		DDR_B_D39
135 DQ34	136 DQ39	DDR_B_D34	DDR_B_D38
137 DQ35	138 VSS	DDR_B_D35	
139 VSS	140 DQ44		DDR_B_D44
141 DQ40	142 DQ45	DDR_B_D40	DDR_B_D45
143 DQ41	144 VSS	DDR_B_D41	
145 VSS	146 DQS5#		DDR_B_DQS#5
147 DM5	148 DQS5	DDR_B_DM5	DDR_B_DQS5
149 VSS	150 VSS		
151 DQ42	152 DQ46	DDR_B_D42	DDR_B_D46
153 DQ43	154 DQ47	DDR_B_D43	DDR_B_D47
155 VSS	156 VSS		
157 DQ48	158 DQ52	DDR_B_D48	DDR_B_D52
159 DQ49	160 DQ53	DDR_B_D49	DDR_B_D53
161 VSS	162 VSS		
163 NC,TEST	164 CK1		M_CLK_DDR3 — M_CLK_DDR3 7
165 VSS	166 CK1#		M_CLK_DDR#3 — M_CLK_DDR#3 7
167 DQS6#	168 VSS	DDR_B_DQS#6	
169 DQS6	170 DM6	DDR_B_DQS6	DDR_B_DM6
171 VSS	172 VSS		
173 DQ50	174 DQ54	DDR_B_D51	DDR_B_D54
175 DQ51	176 DQ55	DDR_B_D50	DDR_B_D55
177 VSS	178 VSS		
179 DQ56	180 DQ60	DDR_B_D56	DDR_B_D60
181 DQ57	182 DQ61	DDR_B_D61	DDR_B_D57
183 VSS	184 VSS		
185 DM7	186 DQS7#	DDR_B_DM7	DDR_B_DQS#7
187 VSS	188 DQS7		DDR_B_DQS7
189 DQ58	190 VSS	DDR_B_D59	
191 DQ59	192 DQ62	DDR_B_D58	DDR_B_D62
193 VSS	194 DQ63		DDR_B_D63
195 SDA	196 VSS	13,16,19 ICH_SM_DA — ICH_SM_DA	
197 SCL	198 SAO	13,16,19 ICH_SM_CLK — ICH_SM_CLK	
199 VDDSPD	200 SA1	+3VS	R37 1 — 2 +3VS, 10K_0402_5%

C54 0.1U_0402_16V4Z, C55 2.2U_0603_6.3V6K
R38 10K_0402_5%

SO-DIMM B
Bottom side

Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.
Title: DDR2 SO-DIMM II
Size: Custom
Document Number: LA-4131P
Rev: 0.2
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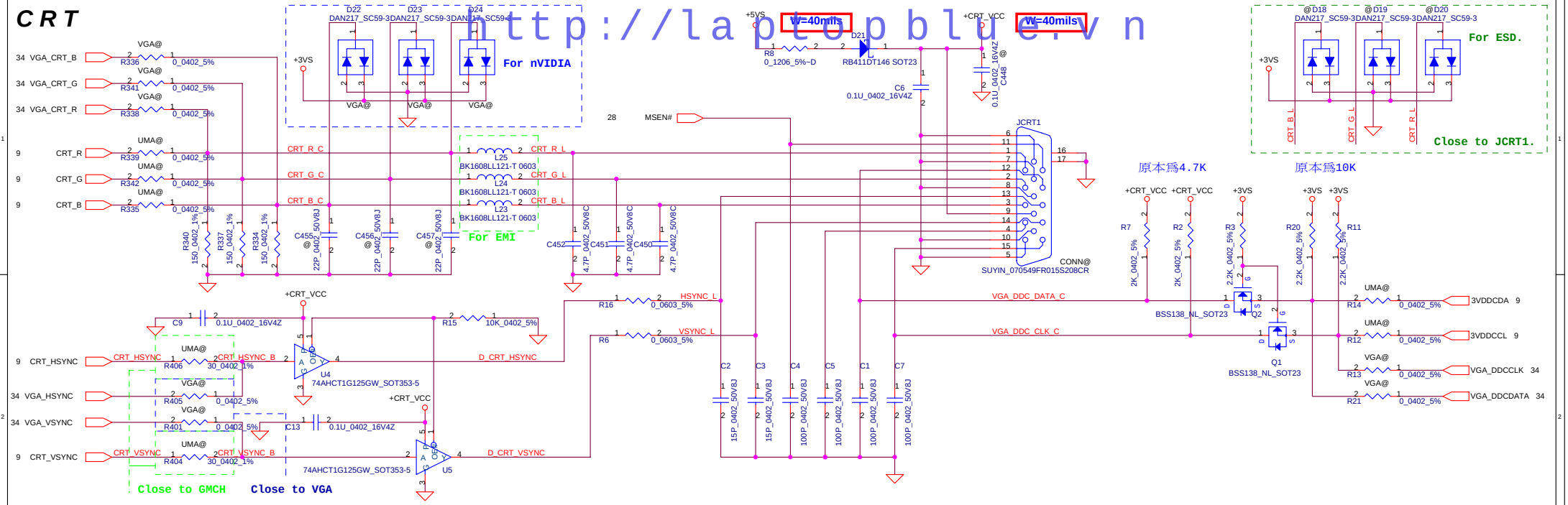
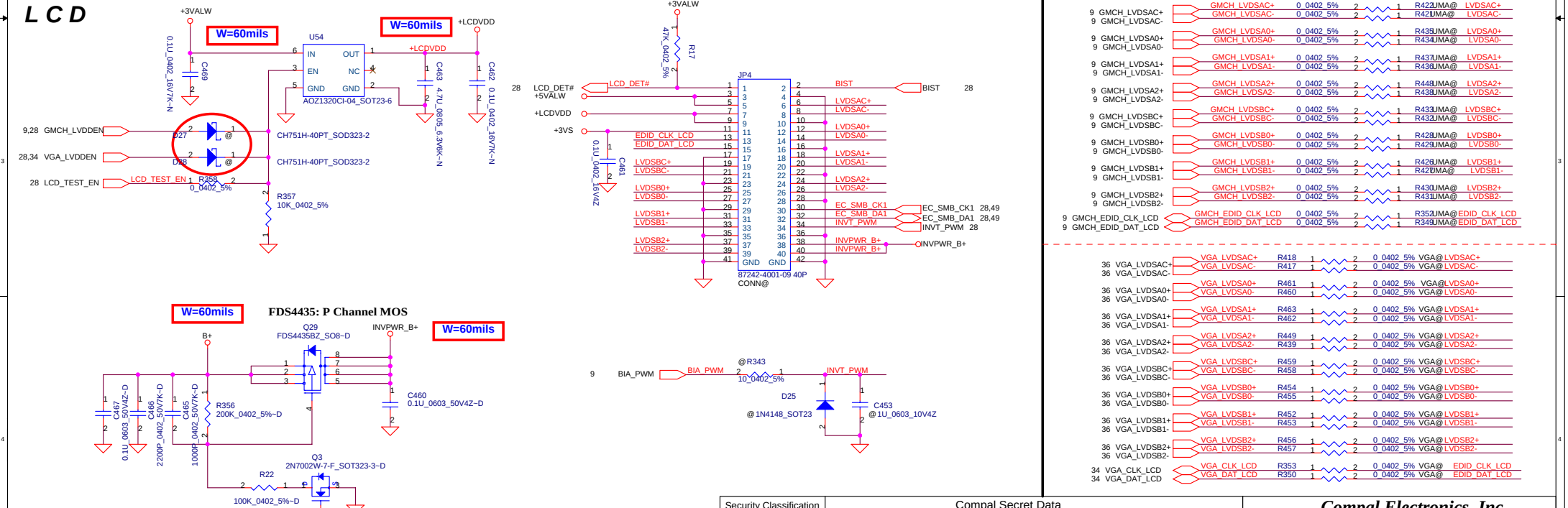
CRT



LCD



Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: **CRT Conn / LCD Conn**

Size	Document Number	Rev
Custom	LA-4131P	0.2

Date: Monday, February 18, 2008 Sheet 15 of 53

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff	R1107	R1135	R1083			
*(Default)	No Stuff	R1074	R1086	R1098	R1113	R1128	R1139
667MHz	Stuff	R1086	R1139	R1135	R1074	R1139	R1135
	No Stuff	R1083 R1113	R1107 R1098	R1128			
800MHz	Stuff	R1135	R1139				
	No Stuff	R1083 R1074	R1086 R1107	R1098 R1113	R1128		

Place these caps close to U6

+3VM_CK505 = 250 mA

+3VS — R521 0_0805_5% — +3VM_CK505

C684 10U_0805_10V4Z~N | C687 0.1U_0402_16V4Z~N | C678 0.1U_0402_16V4Z~N | C685 0.1U_0402_16V4Z~N | C677 0.1U_0402_16V4Z~N | C683 0.1U_0402_16V4Z~N | C676 0.1U_0402_16V4Z~N

+1.25VM_CK505 = 80 mA

+1.25VS — R520 0_0805_5% — +1.25VM_CK505

C682 22U_0805_6.3V4Z | C686 0.1U_0402_16V4Z~N | C688 0.1U_0402_16V4Z~N | C681 22U_0805_6.3V4Z | C689 0.1U_0402_16V4Z~N | C680 0.1U_0402_16V4Z~N | C679 0.1U_0402_16V4Z~N

U6 — ICS9LPRS365BGLFT_TSSOP64

+3VM_CK505: VDDPCI(2), VDD48(9), VDDPLL3(16), VDDREF(61), VDDSRC(39), VDDCPU(55)

+1.25VM_CK505: VDD96_IO(12), VDDPLL3_IO(20), VDDSRC_IO(26), VDDSRC_IO(36), VDDCPU_IO(49)

NC(48)

SCLK(64) — ICH_SM_CLK 13,14,19

SDATA(63) — ICH_SM_DA 13,14,19

PCI_STOP#(38) — H_STP_PCI# 19

CPU_STOP#(37) — H_STP_CPU# 19

CPU0(54) R_CPU_BCLK — CLK_CPU_BCLK 4

CPU0#(53) R_CPU_BCLK# — CLK_CPU_BCLK# 4

CPU1_F(51) R_MCH_BCLK — CLK_MCH_BCLK 7

CPU1#_F(50) R_MCH_BCLK# — CLK_MCH_BCLK# 7

SRC8/CPU2_ITP(47) R_PCIE_LAN — CLK_PCIE_LAN 22

SRC8#/CPU2_ITP#(46) R_PCIE_LAN# — CLK_PCIE_LAN# 22

SRC10(34) R_PCIE_EXPR — CLK_PCIE_EXPR 26

SRC10#(35) R_PCIE_EXPR# — CLK_PCIE_EXPR# 26

SRC11/CR#_H(33) R_CLKREQ#_H — EXPR_CARD_REQ# 26

SRC11#/CR#_G(32) R_CLKREQ#_G — MCARD_REQ# 27

SRC9(30) R_CLK_PCIE_MCard — CLK_PCIE_MCARD 27

SRC9#(31) R_CLK_PCIE_MCard# — CLK_PCIE_MCARD# 27

SRC7/CR#_F(44) R_PCIE_LAN_REQ# — PCIE_LAN_REQ# 22

SRC7#/CR#_E(43) R_ROBSON_REQ# — ROBSON_REQ# 27

SRC6(41) R_CLK_ROB — CLK_PCIE_ROB 27

SRC6#(40) R_CLK_ROB# — CLK_PCIE_ROB# 27

SRC4(27) R_MCH_3GPLL — CLK_MCH_3GPLL 7

SRC4#(28) R_MCH_3GPLL# — CLK_MCH_3GPLL# 7

SRC3/CR#_C(24) R_PCIE_ICH — CLK_PCIE_ICH 19

SRC3#/CR#_D(25) R_PCIE_ICH# — CLK_PCIE_ICH# 19

SRC2/SATA(21) R_PCIE_SATA — CLK_PCIE_SATA 18

SRC2#/SATA#(22) R_PCIE_SATA# — CLK_PCIE_SATA# 18

SRC1/SE1/27MHz_NonSS(17) R_SSCDREFCLK — MCH_SSCDREFCLK 7

SRC1#/SE2/27MHz_SS(18) R_SSCDREFCLK# — MCH_SSCDREFCLK# 7

SRC0/DOT96(13) R_MCH_DREFCLK — CLK_MCH_DREFCLK 7

SRC0#/DOT96#(14) R_MCH_DREFCLK# — CLK_MCH_DREFCLK# 7

R553 — CLK_PCIE_VGA 34

R554 — CLK_PCIE_VGA# 34

CK_PWRGD/PD#(56) — CK_PWRGD 19

@R507 — CLK_EN# 48

PCI0/CR#_A(1) ← SATA_REQ ← R525 475_0402_1% ← CLKSATAREQ# 19

PCI1/CR#_B(3) ← MCH_REQ ← R529 475_0402_1% ← CLKMCHREQ# 7

PCI2/TME(4) ← PCI2_TME ← R527 33_0402_5% ← CLK_PCI_CB 25,28

PCI3 ← R528 33_0402_5% ← CLK_PCI_TPM 28

PCI4/27_Select(6) ← 27_SEL ← R536 33_0402_5% ← CLK_PCI_EC 28

PCI_F5/ITP_EN(7) ← ITP_EN ← R526 33_0402_5% ← CLK_PCI_ICH 17

PCI_CLK3(5) ← R532 33_0402_5% ← CLK_DEBUG_PORT 27

+3VS — R524 10K_0402_5% — R530 10K_0402_5%

CLK_XTAL_IN(60) — CLK_XTAL_OUT(59) — X1, X2

USB_48MHZ/FSLA(10) ← FSLA ← R533 33_0402_5% ← CLK_48M_ICH 19

FSLB/TEST_MODE(57) ← FSB

REF0/FSLC/TEST_SEL(62) ← FSC ← R515 33_0402_5% ← CLK_14M_ICH 19; R509 33_0402_5% ← CLK_14M_SIO

VDDSRC_IO(45) ← +1.25VM_CK505

GNDSRC(42), GNDPCI(8), GND48(11), GND(15), GND(19), GNDCPU(52), GNDSRC(23), GNDSRC(29), GNDREF(58)

R548 2.2K_0402_5% — FSA — MCH_CLKSEL0 7

CPU_BSEL0 5 — R550 0_0402_5% — R556 1K_0402_5%

+VCCP — R502 @ 1K_0402_5%

FSB — MCH_CLKSEL1 7

CPU_BSEL1 5 — R501 0_0402_5% — R499 1K_0402_5%

R516 10K_0402_5% — FSC — MCH_CLKSEL2 7

CPU_BSEL2 5 — @R519 0_0402_5% — R517 1K_0402_5%

R514 0_0402_5%

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

For 27_SEL, 0 = Enable DOT96 & SRC1,

1 = Enable SRC0 & 27MHz

For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed

1 = Overclocking of CPU and SRC NOT allowed

CLK_XTAL_OUT — CLK_XTAL_IN — Y4 14.31818MHz_20P_1BX14318BE1A — C667 18P_0402_50V8J~N — C666 18P_0402_50V8J~N

Placed within 500 mils of CK505M

Routing the trace at least 10mil

+3VM_CK505 — R549 10K_0402_5% VGA@ — 27_SEL

+3VM_CK505 — R535 10K_0402_5% — PCI2_TME

ITP_EN — R534 10K_0402_5% — R545 10K_0402_5% UMA@ — R531 10K_0402_5% @

Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: Clock Generator

Size: Custom | Document Number: LA-4131P | Rev: 0.2

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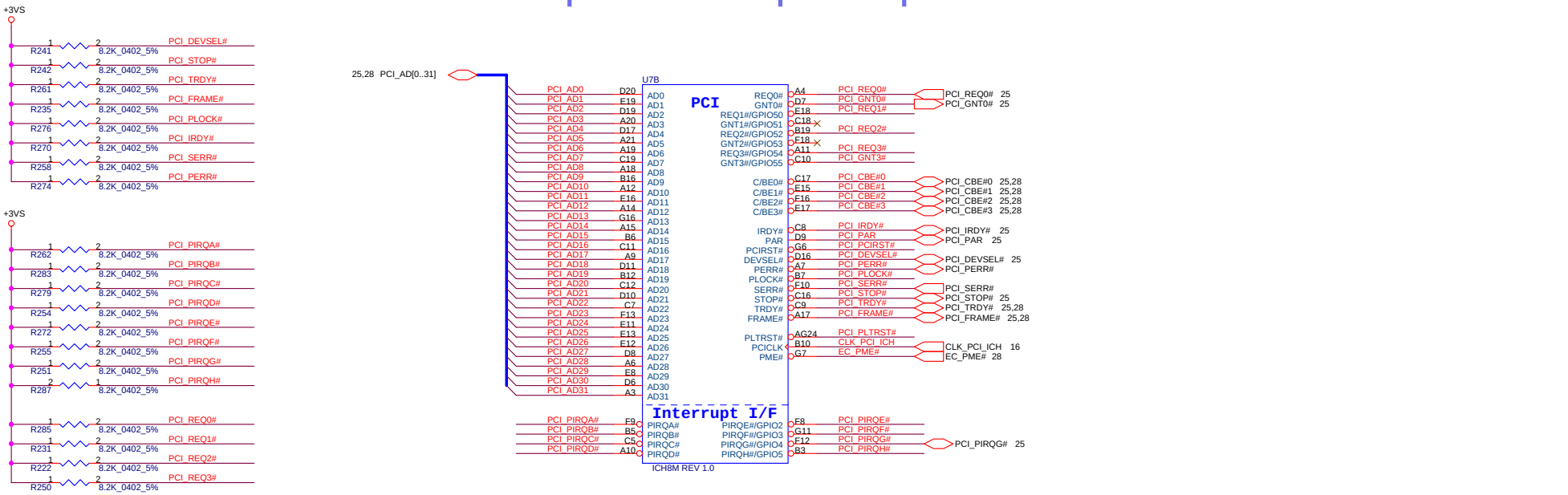
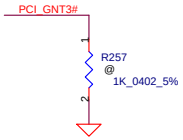
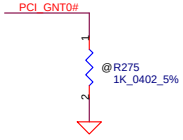


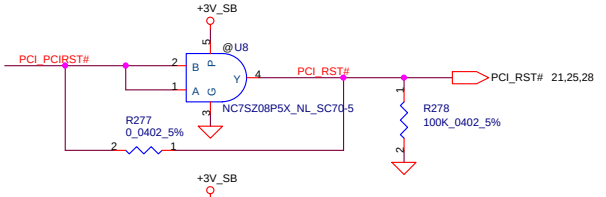


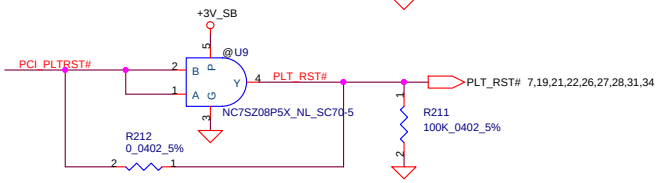
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*

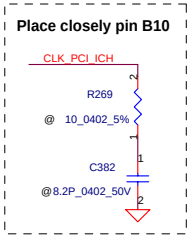
Check if use LPC

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *









Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: ICH8M(1/4)_PCI / INT

Size	Document Number	Rev
Custom	LA-4131P	0.2

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+RTC_CELL
R204 330K_0402_1% LAN100_SLP
R201 1M_0402_5% SM_INTRUDER#
R160 330K_0402_1% ICH_INTVRMEN

ICH_RTCX1
R200 10M_0402_5%
ICH_RTCX2
C351 15P_0402_50V8J
C355 15P_0402_50V8J
Y1 32.768KHZ QTFM28-32768K125P10L

+3VS
R260 10K_0402_5% SATA_LED#

+RTC_CELL
R173 20K_0402_5%
C343 1U_0603_10V6K
JCMOS1 @
NO SHORT PAD

U7A
ICH_RTCX1 AG25 RTCX1
ICH_RTCX2 AF24 RTCX2
ICH_RTCRST# AF23 RTCRST#
SM_INTRUDER# AD22 INTRUDER#
ICH_INTVRMEN AF25 INTVRMEN
LAN100_SLP AD21 LAN100_SLP
RTC
B24 GLAN_CLK
D22 LAN_RSTSYNC
C21 LAN_RXD0
B21 LAN_RXD1
C22 LAN_RXD2
D21 LAN_TXD0
E20 LAN_TXD1
C20 LAN_TXD2
AH21 GLAN_DOCK#/GPIO13
D25 GLAN_COMPI
C25 GLAN_COMPO
LAN / GLAN
+1.5VS R189 24.9_0402_1% GLAN_COMP
23 ACZ_BITCLK R273 33_0402_5% HDA_BITCLK_R AJ16 HDA_BIT_CLK
23 ACZ_SYNC R268 33_0402_5% HDA_SYNC_R AJ15 HDA_SYNC
23 ACZ_RST# R244 33_0402_5% HDA_RST_R# AE14 HDA_RST#
23 ADC_ACZ_SDIN0 ADC_ACZ_SDIN0 AJ17 HDA_SDIN0
AH17 HDA_SDIN1
AH15 HDA_SDIN2
AD13 HDA_SDIN3
23 ACZ_SDOUT R224 33_0402_5% HDA_SDOUT_R AE13 HDA_SDOUT
AE10 HDA_DOCK_EN#/GPIO33
AG14 HDA_DOCK_RST#/GPIO34
IHDA
29 SATA_LED# SATA_LED# AE10 SATALED#
21 SATA_IRX_DTX_N0_C SATA_IRX_DTX_N0_C AF6 SATA0RXN
21 SATA_IRX_DTX_P0_C SATA_IRX_DTX_P0_C AF5 SATA0RXP
SATA_ITX_DRX_N0_C AH5 SATA0TXN
SATA_ITX_DRX_P0_C AH6 SATA0TXP
21 SATA_IRX_DTX_N1_C SATA_IRX_DTX_N1_C AG3 SATA1RXN
21 SATA_IRX_DTX_P1_C SATA_IRX_DTX_P1_C AG4 SATA1RXP
SATA_ITX_DRX_N1_C AJ4 SATA1TXN
SATA_ITX_DRX_P1_C AJ3 SATA1TXP
SATA_IRX_DTX_N2_C AF2 SATA2RXN
SATA_IRX_DTX_P2_C AF1 SATA2RXP
SATA_ITX_DRX_N2_C AE4 SATA2TXN
SATA_ITX_DRX_P2_C AE3 SATA2TXP
16 CLK_PCIE_SATA# CLK_PCIE_SATA# AB7 SATA_CLKN
16 CLK_PCIE_SATA CLK_PCIE_SATA AC6 SATA_CLKP
SATA
IDE
R290 24.9_0402_1% Within 500 mils
AG1 SATARBIAS#
AG2 SATARBIAS
ICH8M REV 1.0

FWH0/LAD0 E5 LPC_AD0
FWH1/LAD1 F5 LPC_AD1
FWH2/LAD2 G8 LPC_AD2
FWH3/LAD3 F6 LPC_AD3
LPC_AD[0..3] 27,28
FWH4/LFRAME# C4 LPC_FRAME#
LPC_FRAME# 27,28
LDRQ0# G9 LPC_DRQ0#
LDRQ1#/GPIO23 E6 LPC_DRQ1#
LPC_DRQ0#
T39 PAD
A20GATE AF13 GATEA20
A20M# AG26 H_A20M#
GATEA20 28
H_A20M# 4
DPRSTP# AF26 H_DPRSTP_R#
DPSLP# AE26
R175 2 1 H_DPRSTP# 0_0402_5%
H_DPRSTP# 5,7,48
H_DPSLP# 5
FERR# AD24 H_FERR#
H_FERR# 4
CPUPWRGD/GPIO49 AG29 H_PWRGOOD
H_PWRGOOD 5
IGNNE# AF27 H_IGNNE#
H_IGNNE# 4
INIT# AF24 H_INIT#
INTR AC20 H_INTR
RCIN# AH14 KB_RST#
H_INIT# 4
H_INTR 4
KB_RST# 28
NMI AD23 H_NMI
SMI# AG28 H_SMI#
H_NMI 4
H_SMI# 4
STPCLK# AA24 H_STPCLK#
H_STPCLK# 4
THRMTRIP# AE27 THRMTRIP_ICH#
R185 24.0_0402_1%
H_THERMTRIP# 4,7
TP8 AA23
IDE_DD[0..15] 21
DD0 V1 IDE_DD0
DD1 U2 IDE_DD1
DD2 V3 IDE_DD2
DD3 T1 IDE_DD3
DD4 V4 IDE_DD4
DD5 T5 IDE_DD5
DD6 AB2 IDE_DD6
DD7 T6 IDE_DD7
DD8 T3 IDE_DD8
DD9 R2 IDE_DD9
DD10 T4 IDE_DD10
DD11 V6 IDE_DD11
DD12 V5 IDE_DD12
DD13 U1 IDE_DD13
DD14 V2 IDE_DD14
DD15 U6 IDE_DD15
DA0 AA4 IDE_DA0
DA1 AA1 IDE_DA1
DA2 AB3 IDE_DA2
IDE_DA0 21
IDE_DA1 21
IDE_DA2 21
DCS1# Y6 IDE_DCS1#
DCS3# Y5 IDE_DCS3#
IDE_DCS1# 21
IDE_DCS3# 21
DIOR# W4 IDE_DIOR#
DIOW# W3 IDE_DIOW#
DDACK# V2 IDE_DDACK#
IDEIRQ Y3 IDE_IRQ
IORDY Y1 IDE_DIORDY
DDREQ W5 IDE_DDREQ
IDE_DIOR# 21
IDE_DIOW# 21
IDE_DDACK# 21
IDE_IRQ 21
IDE_DIORDY 21
IDE_DDREQ 21

+3VS
GATEA20 R227 10K_0402_5%
KB_RST# R248 10K_0402_5%
+VCCP
H_FERR# R203 56_0402_5%

within 2" from R1557
+VCCP
R172 56_0402_5%
placed within 2" from ICH8M

+3VS
IDE_DIORDY R292 4.7K_0402_5%
IDE_IRQ R288 8.2K_0402_5%

21 SATA_ITX_DRX_N0 SATA_ITX_DRX_N0 C403 3900P_0402_50V7K SATA_ITX_DRX_N0_C
21 SATA_ITX_DRX_P0 SATA_ITX_DRX_P0 C400 3900P_0402_50V7K SATA_ITX_DRX_P0_C
Close ICH8

SATA_IRX_DTX_N1_C
SATA_IRX_DTX_P1_C
21 SATA_ITX_DRX_N1 SATA_ITX_DRX_N1 C692 3900P_0402_50V7K SATA_ITX_DRX_N1_C
21 SATA_ITX_DRX_P1 SATA_ITX_DRX_P1 C697 3900P_0402_50V7K SATA_ITX_DRX_P1_C
Close ICH8
R284 0_0402_5% @
R282 0_0402_5% @

PAD T42 SATA_IRX_DTX_N2_C
PAD T43 SATA_IRX_DTX_P2_C
PAD T45 SATA_ITX_DRX_N2 C415 3900P_0402_50V7K SATA_ITX_DRX_N2_C @
PAD T44 SATA_ITX_DRX_P2 C414 3900P_0402_50V7K SATA_ITX_DRX_P2_C @
Close ICH8
R286 0_0402_5%
R285 0_0402_5%

+3VS
@R223 1K_0402_5% ACZ_SDOUT
@R218 1K_0402_5% ICH_RSVD
ICH_RSVD 19

XOR CHAIN ENTRANCE STRAP:RSVD

XOR Chain Entrance Strap		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.
Title: ICH8M(2/4)_LAN / HD / IDE / LPC
Size: Custom
Document Number: LA-4131P
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Low--> Default
High --> No Reboot Mode

Place closely pin G5
Place closely pin AG9

RSMRST# -> CLPWROK -> PWROK

Modify follow intel check list-1003

Reserve

Express Card

Robson

WLAN

GLAN

Finger Printer
Blue Tooth
JUSBP5
JUSBP5
JUSBP1
USB Hub
JUSBP4
Express Card
JUSBP3
JUSBP2

Within 500 mils
Within 500 mils

RSMRST circuit

For(DDR/CLKGEN/G-sensor/WWAN)
For(WLAN/EXP-Card/LAN)

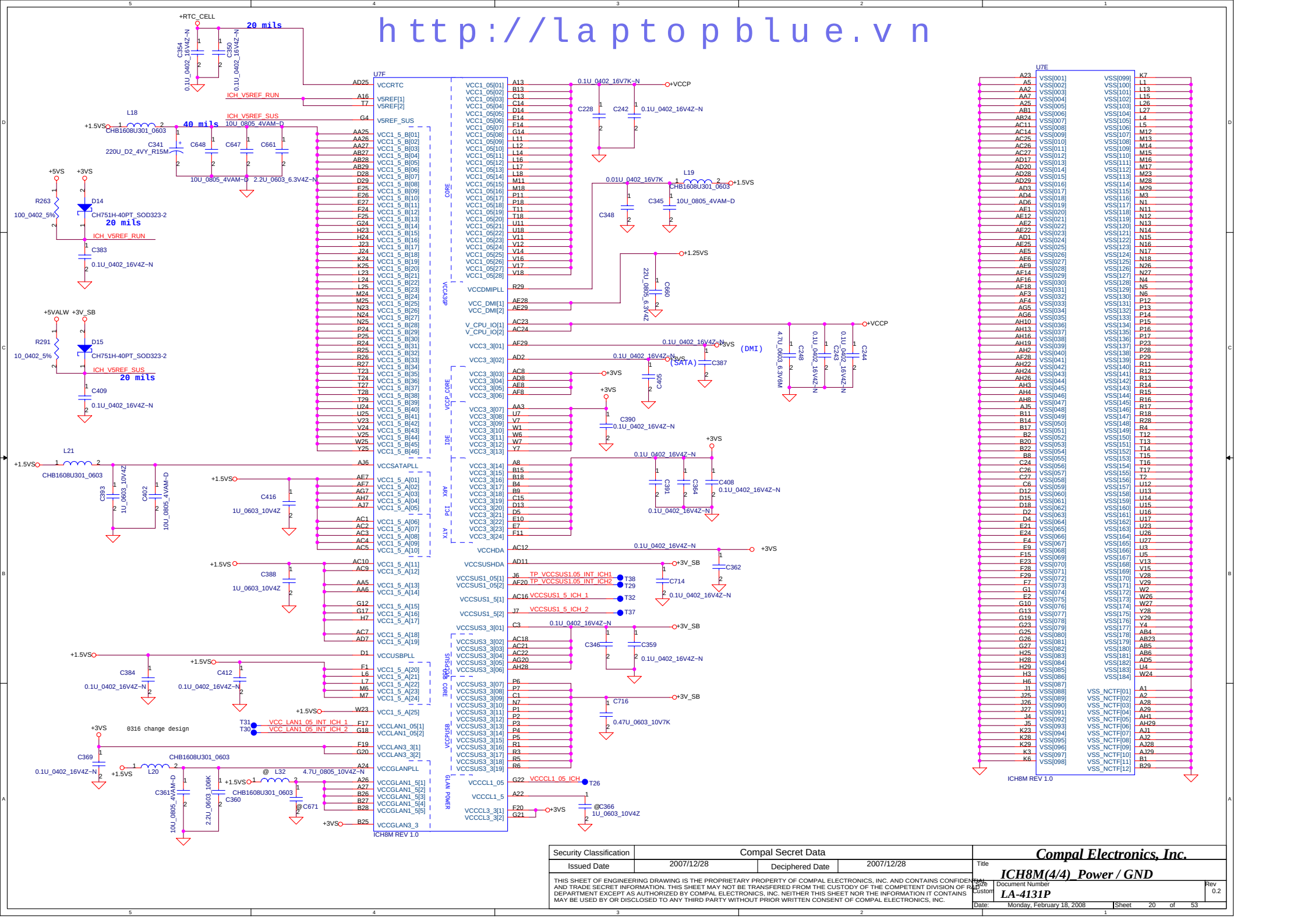
Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: ICH8M(3/4)_PM/USB/GPIO

Size: Custom | Document Number: LA-4131P | Rev: 0.2

Date: Monday, February 18, 2008 | Sheet 19 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

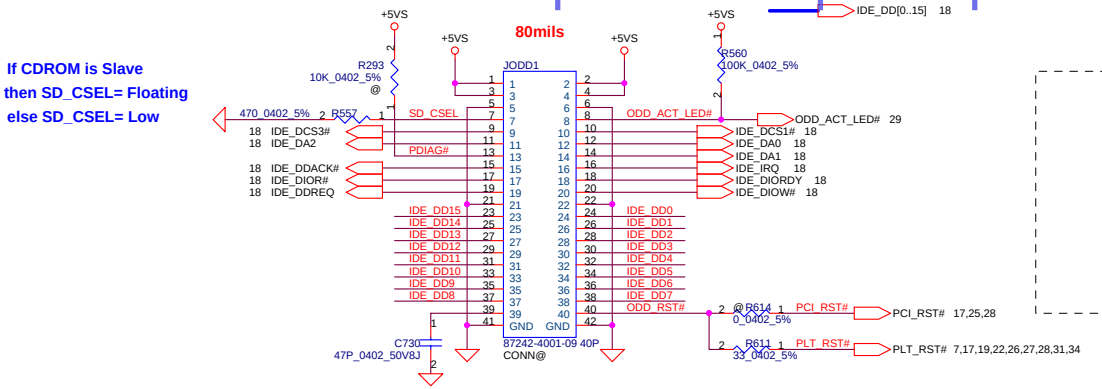
Compal Electronics, Inc.

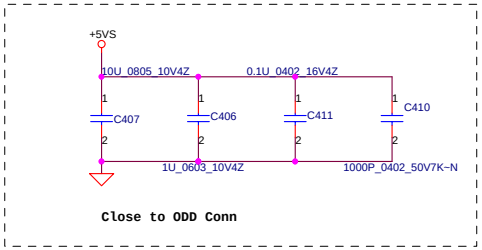
Title: ICH8M(4/4)_Power / GND

Size: Custom | Document Number: LA-4131P | Rev: 0.2

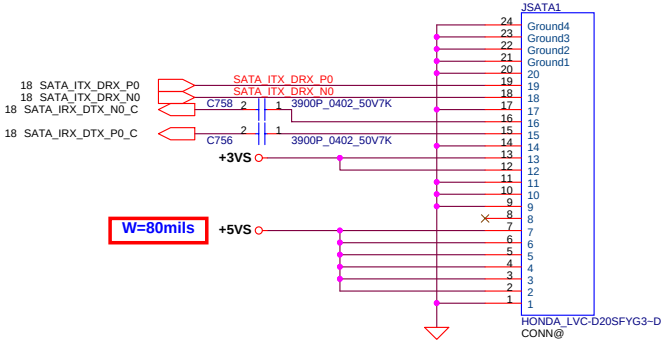
Date: Monday, February 18, 2008 | Sheet 20 of 53

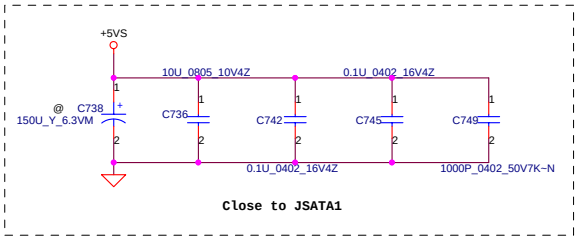
ODD Conn



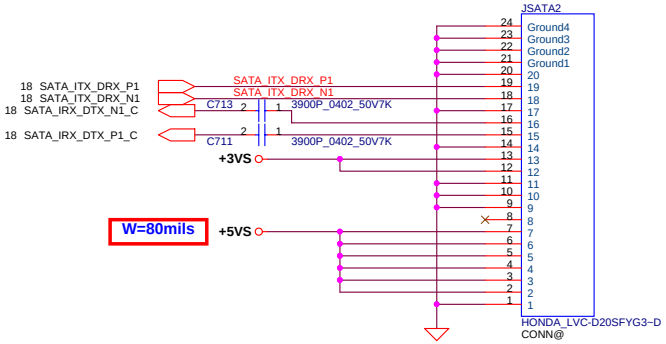


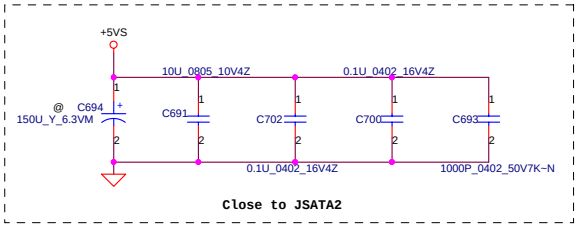
SATA HDD1 Conn





SATA HDD2 Conn





Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: **HDD / ODD**

Size: Custom | Document Number: **LA-4131P** | Rev: 0.2

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W=60mils +3VALW
W=60mils +LAN_IO
1.5A
Q30 AO6402A 1N TSOP-6
L26 FBMA-L11-322513-201LMA40T_1210
C473 1U_0603_10V6K
B+_BIAS
R359 470K_0402_5%
EN_WOL
28 EN_WOL#
Q31 SSM3K7002FU_SC70-3
R364 1.5M_0402_5%
C29 C482 C33 C31 C26 C35 C17
These caps close to U30: Pin 16, 37, 46, 53
+LAN_VDD R19 0_0603_5% LAN_DVDD12
C479 C481 C477 C32 C34 C471 C25 C478 C480 C475
These caps close to U30: Pin 21, 32, 38, 43, 49, 52
U30 RTL8111C-GR_QFN64_9X9
R361 3.6K_0402_5% +LAN_IO
U43 @ AT93C46-10SU-2.7 SO 8P
R360@ 0_0402_5% C483@ 0.1U_0402_16V7K-N
C36 C464
These caps close to U30: Pin 63
(Should be place within 200 mils)
W=60mils +LAN_VDD
L2 4.7UH_1008HC-472EJFS-A_5%_1008
C19 C16
These components close to U30: Pin 1
(Should be place within 200 mils)
W=60mils
R355 2.49K_0402_1%
R362 1K_0402_5%
R363 15K_0402_5%
W=30mils L1 FBML10160808121LMT_0603 W=30mils +LAN_VDD
C27 C30
These caps close to U30: Pin 22, 28
L3 FBML10160808121LMT_0603 +LAN_IO
C28 C18
These caps close to U30: Pin 2, 59
R18 0_0603_5% LAN_AVDD12
C21 C472 C20 C22
These caps close to U30: Pin 8, 11, 14, 58
Y2 25MHZ_20P_1BX25000CK1A C470 C468
C459 C458 R354 R351 R346 R344 R333 R332 R330 R329
C454 C449
These components close to T47.
for EMI
T46 BOTH_GST5009-LF
RP1 75_1206_8P4R_5%
C8 1000P_1206_2KV7K
R331 R1 @R4 @R328
D4 D3 D2 D1 CH751H-40PT_SOD323-2
JLAN1 C-1775553 CONN@
R5 R10 R9 220_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.
Title: Realtek RTL8111C-GR
Size: Custom
Document Number: LA-4131P
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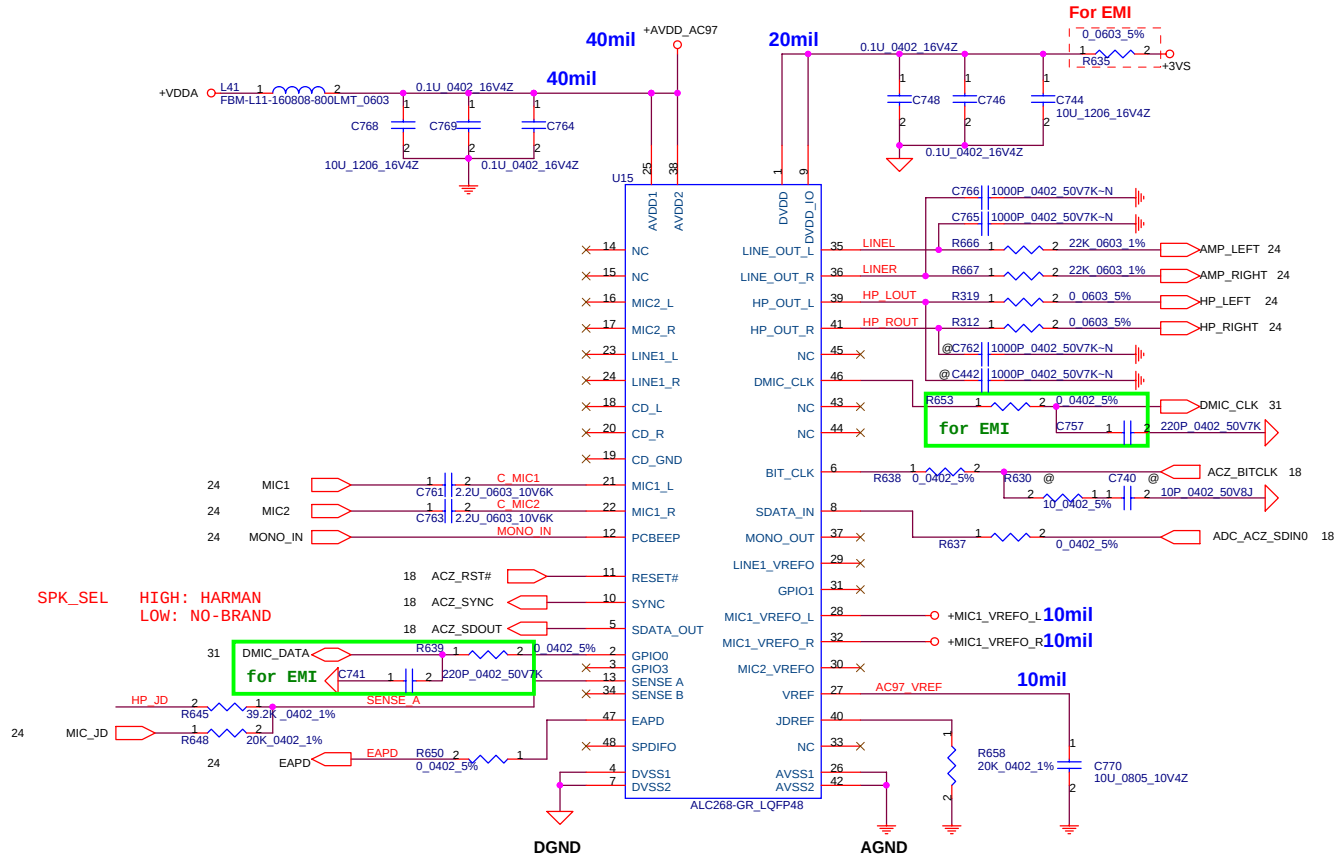
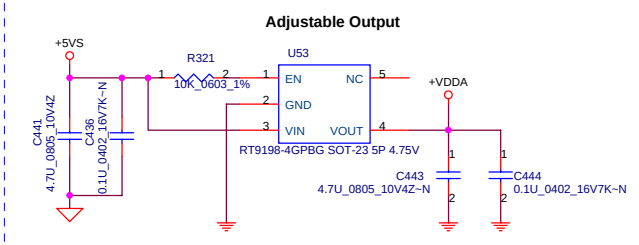
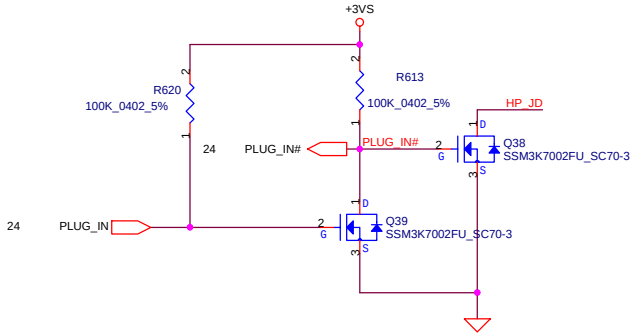
HD Audio Codec



SPK_SEL HIGH: HARMAN
LOW: NO-BRAND

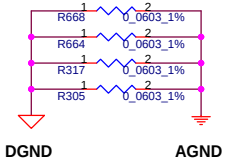
Regulator for Codec





Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Moat Bridge



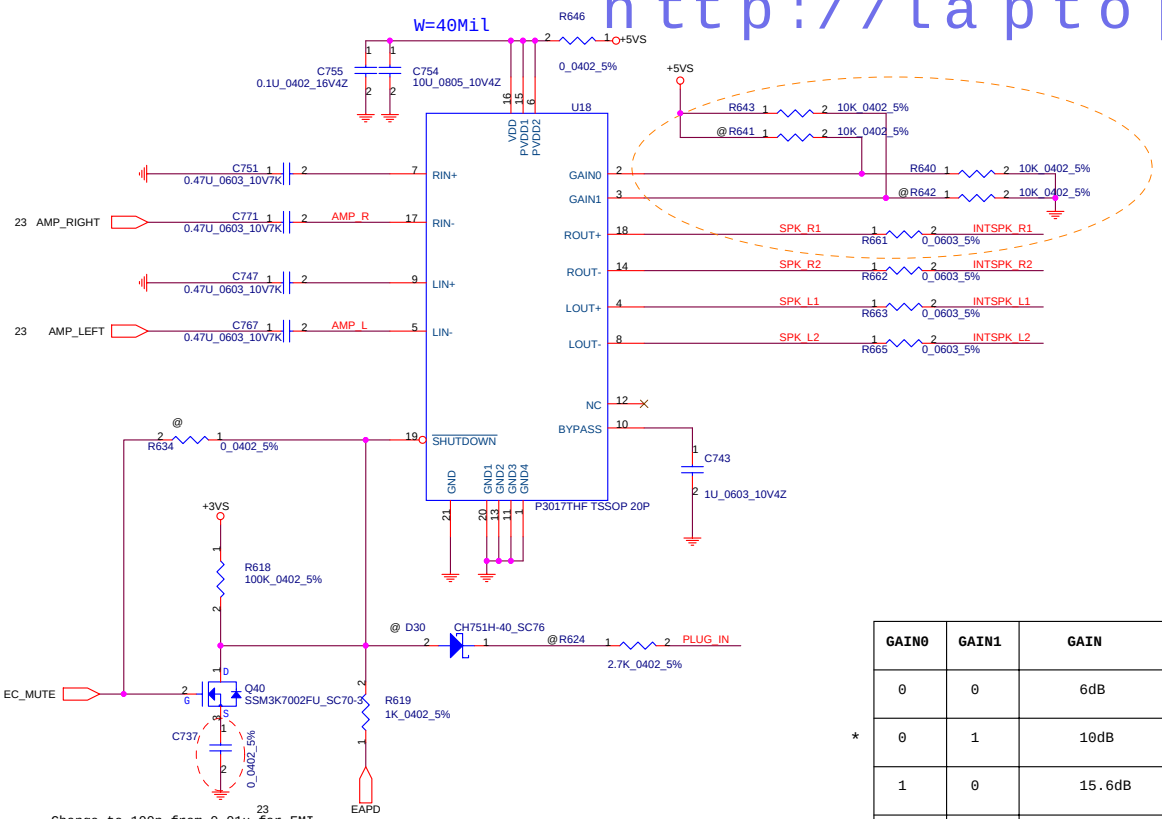
Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: **Audio Codec_ALC268**

Size: Custom | Document Number: **LA-4131P** | Rev: 0.2

Date: Monday, February 18, 2008 | Sheet 23 of 53

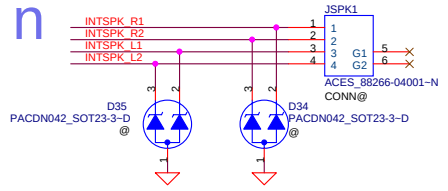


Change to 100p from 0.01u for EMI
-1012

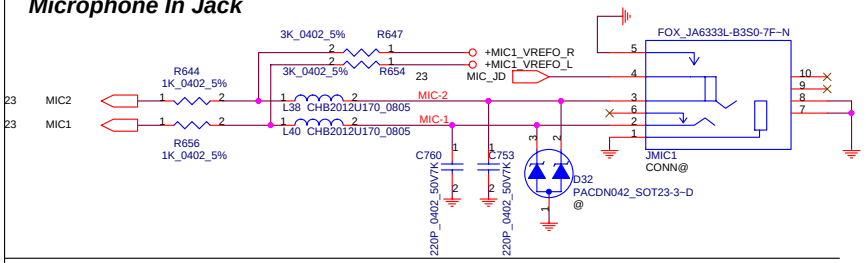
Buzzer need to support ICH/PCM_SPK/Battery_low and WL_on/off

	GAIN0	GAIN1	GAIN
	0	0	6dB
*	0	1	10dB
	1	0	15.6dB
	1	1	21.6dB

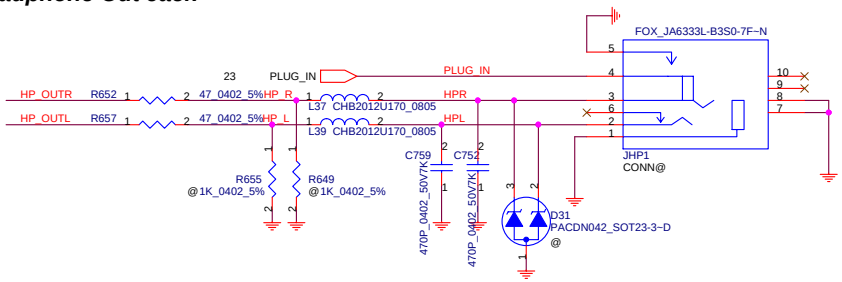
Speaker Connector

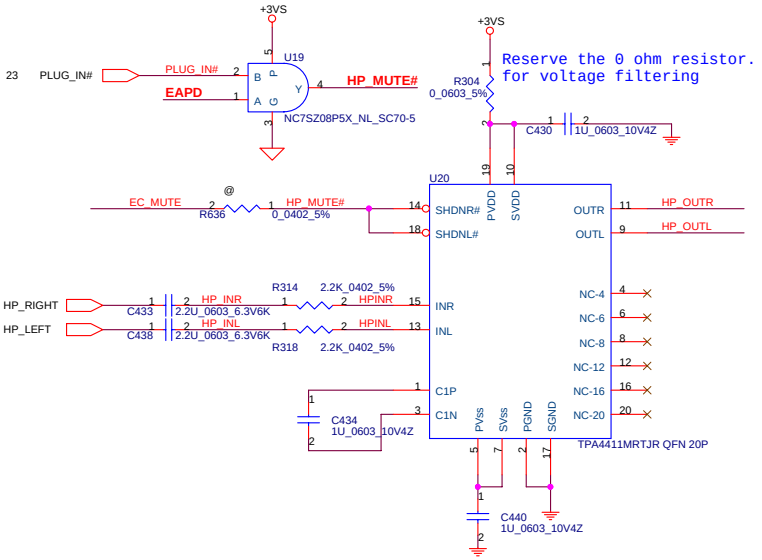


Microphone In Jack



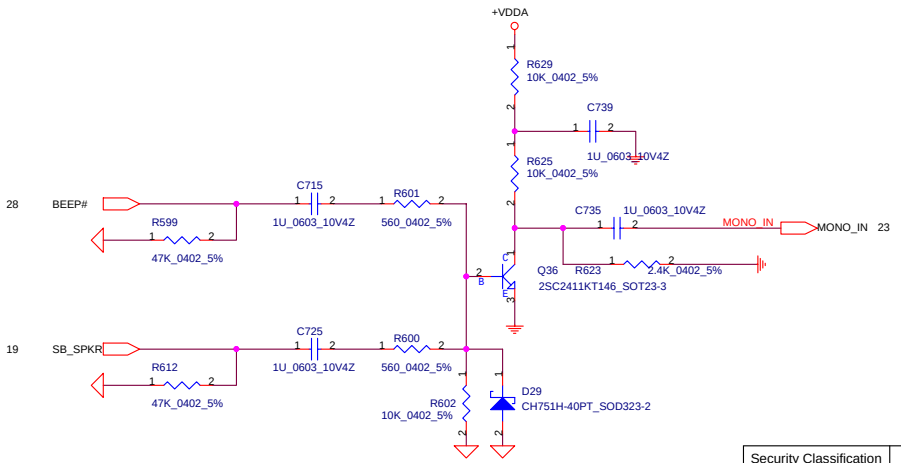
Headphone Out Jack





EC Beep

ICH Beep



Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: **AMP / Audio Jack**

Size	Document Number	Rev
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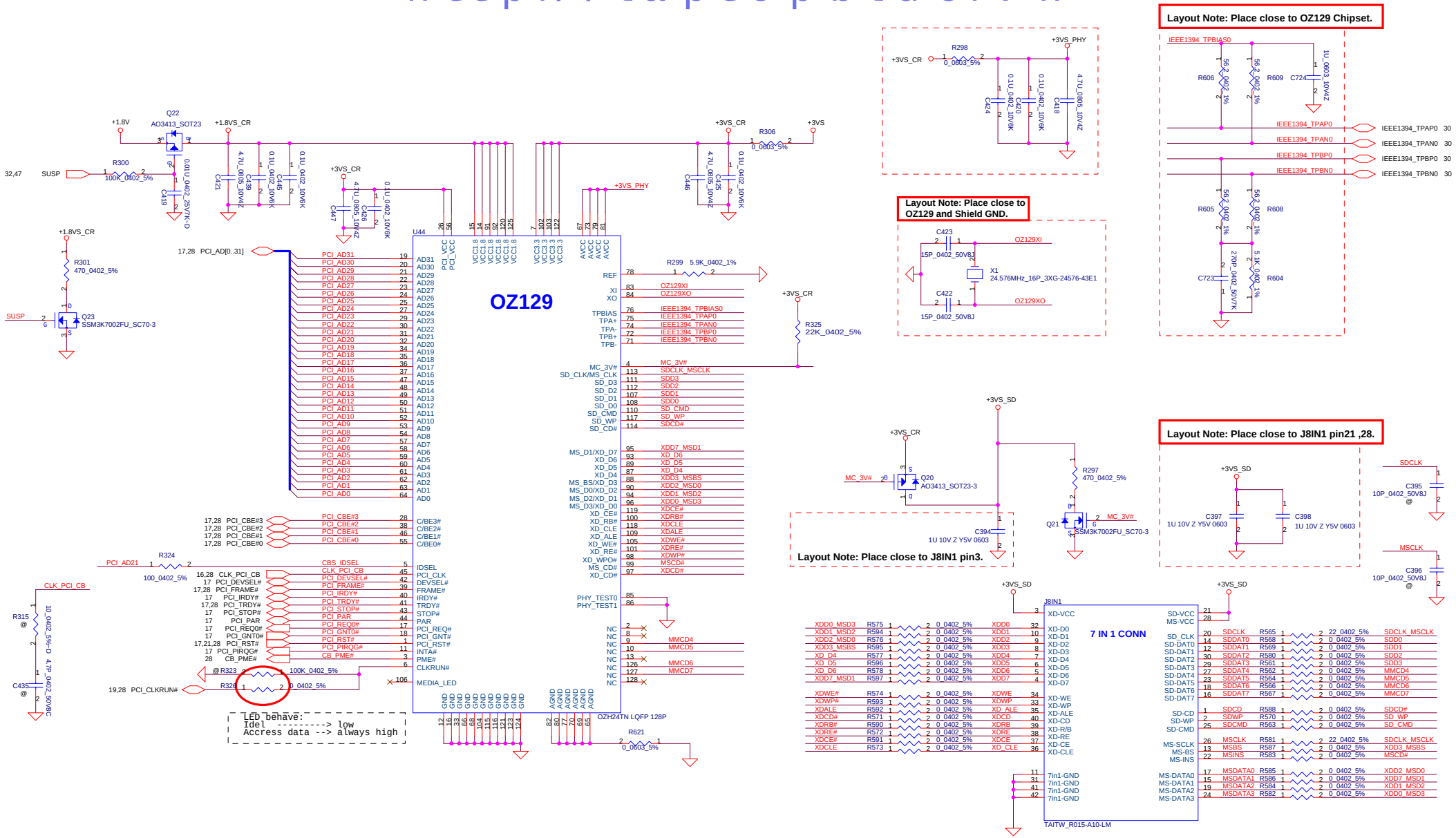

Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: *OZH24_Card Reader / 1394*

Size	Document Number	Rev
Custom	LA-4131P	0.2

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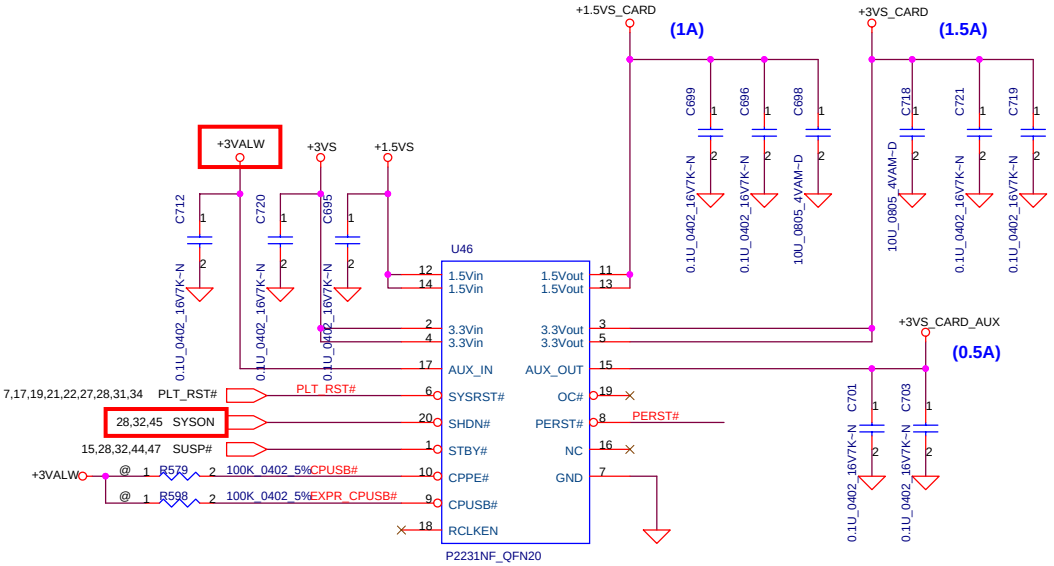
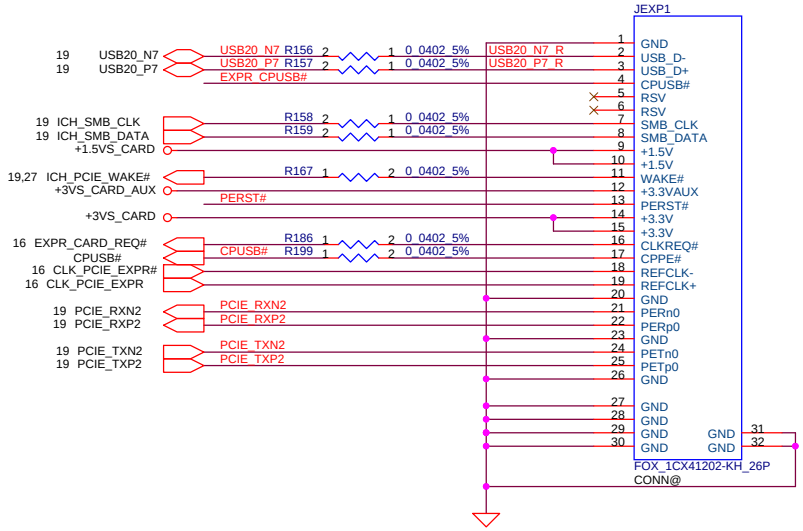
Express Card Power Switch



Express Card



Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: **Express Card**

Size	Document Number	Rev
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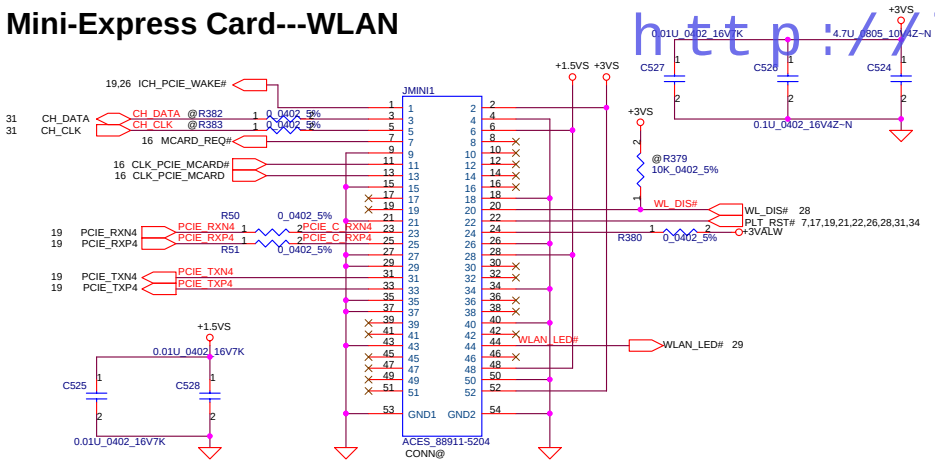
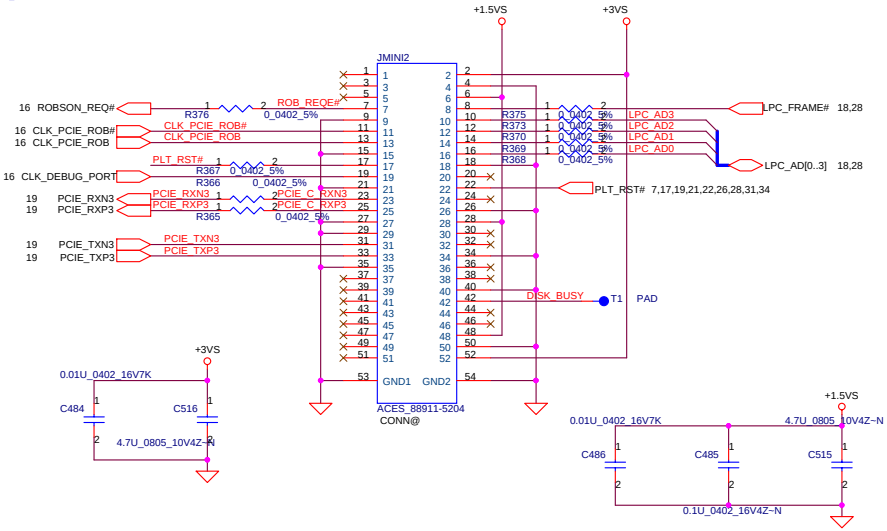
Mini-Express Card---WLAN



Mini-Express Card---Robson



Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: **Mini Card**

Size: Custom | Document Number: **LA-4131P** | Rev: 0.2

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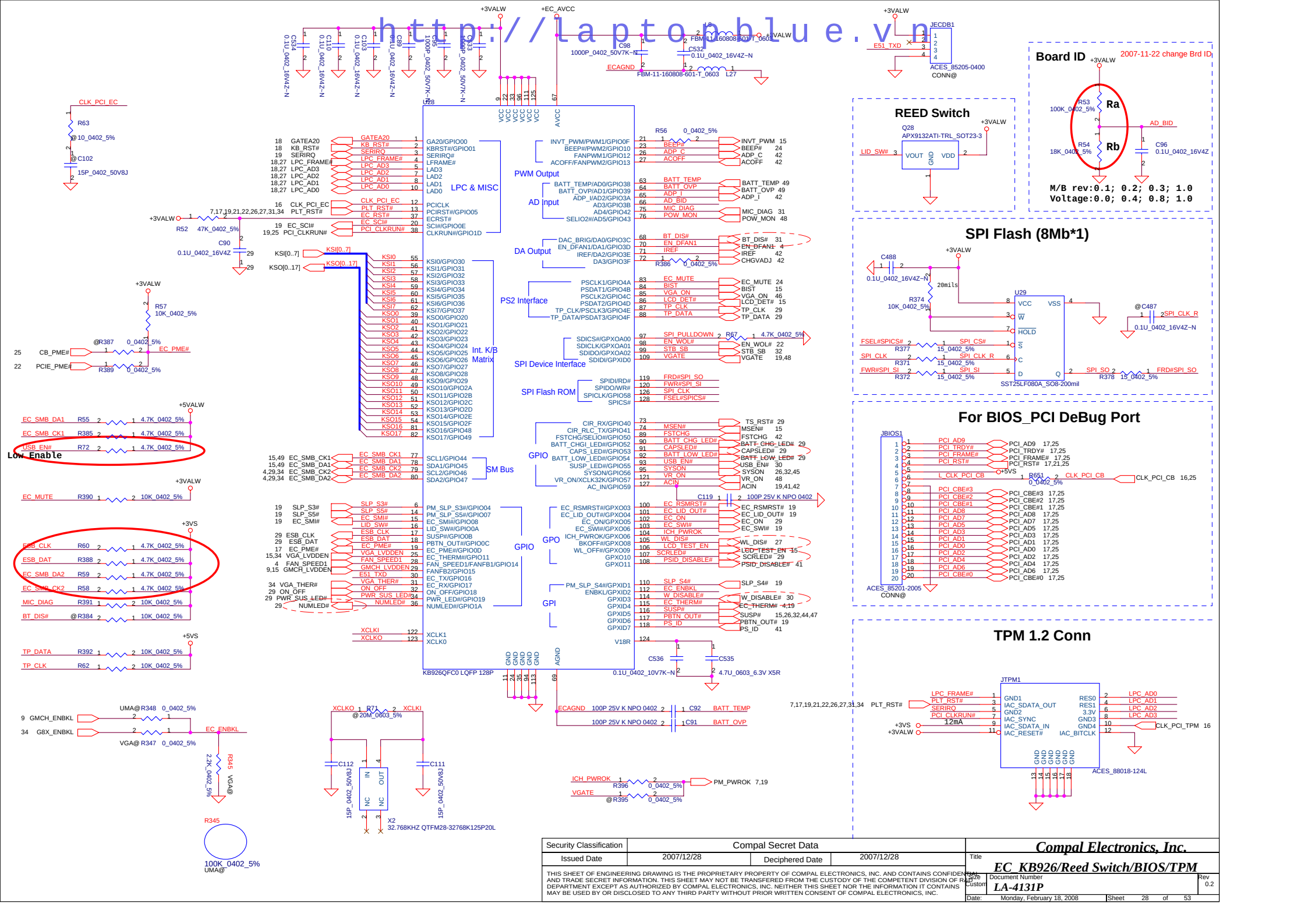

Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.			
Title: EC_KB926/Reed Switch/BIOS/TPM			
Size: Custom	Document Number: LA-4131P		Rev: 0.2
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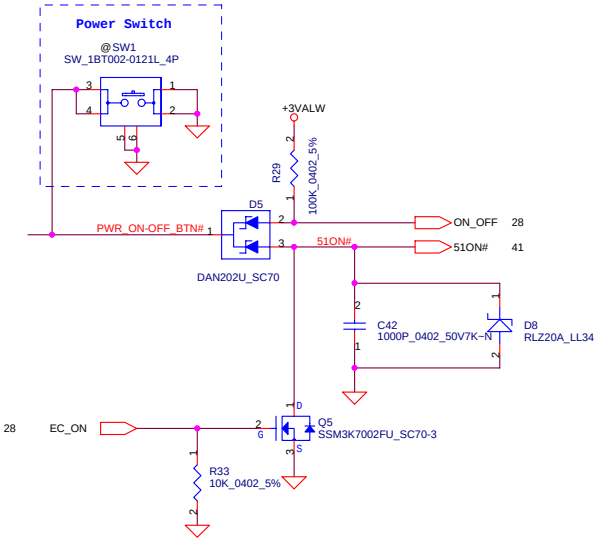
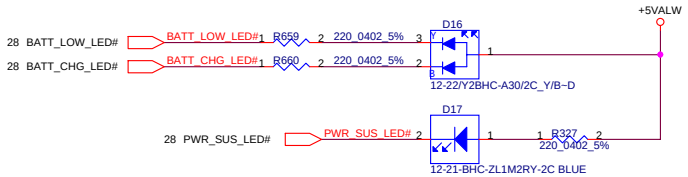
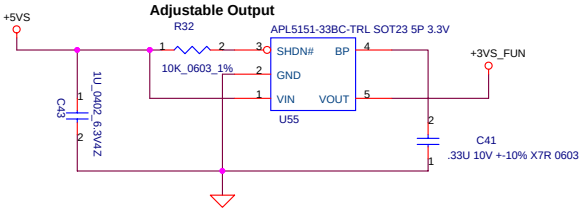
Power Button

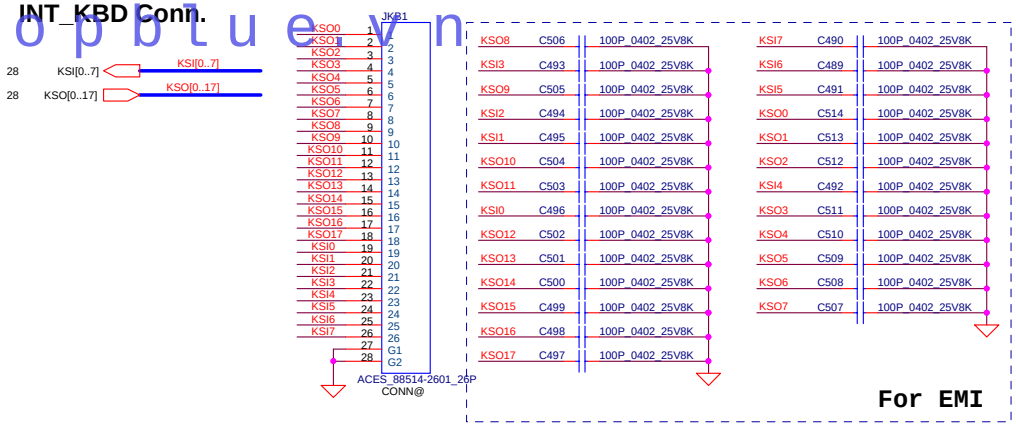




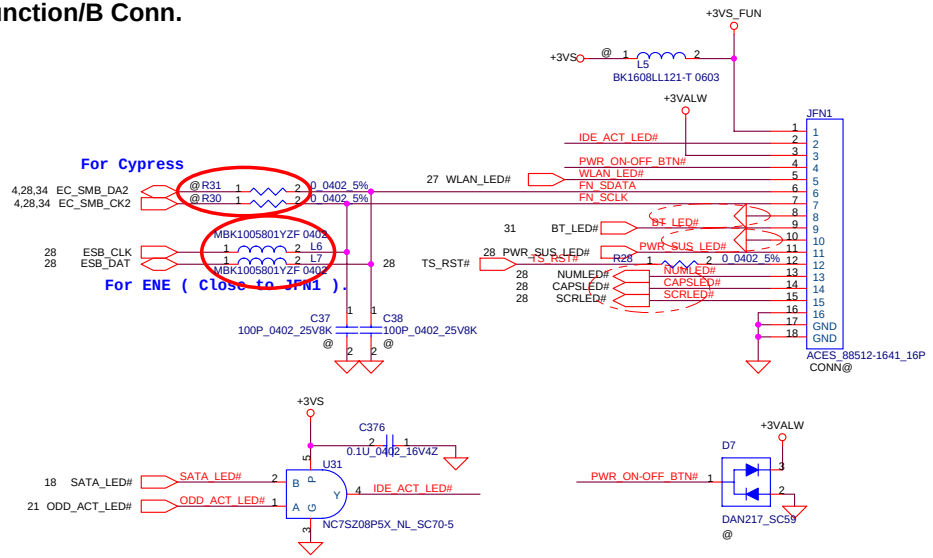
Regulator for ENE sensor



INT_KBD Conn.

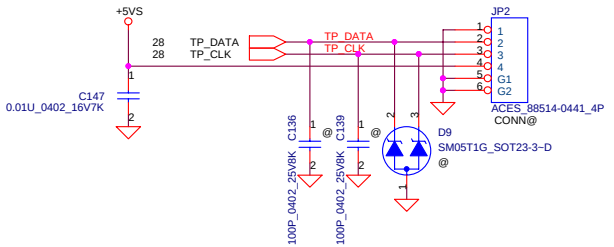


Function/B Conn.



Touch Pad/B Conn.

TP/B to M/B



Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: PWR_OK / BTN / KB / TP

Size	Document Number	Rev
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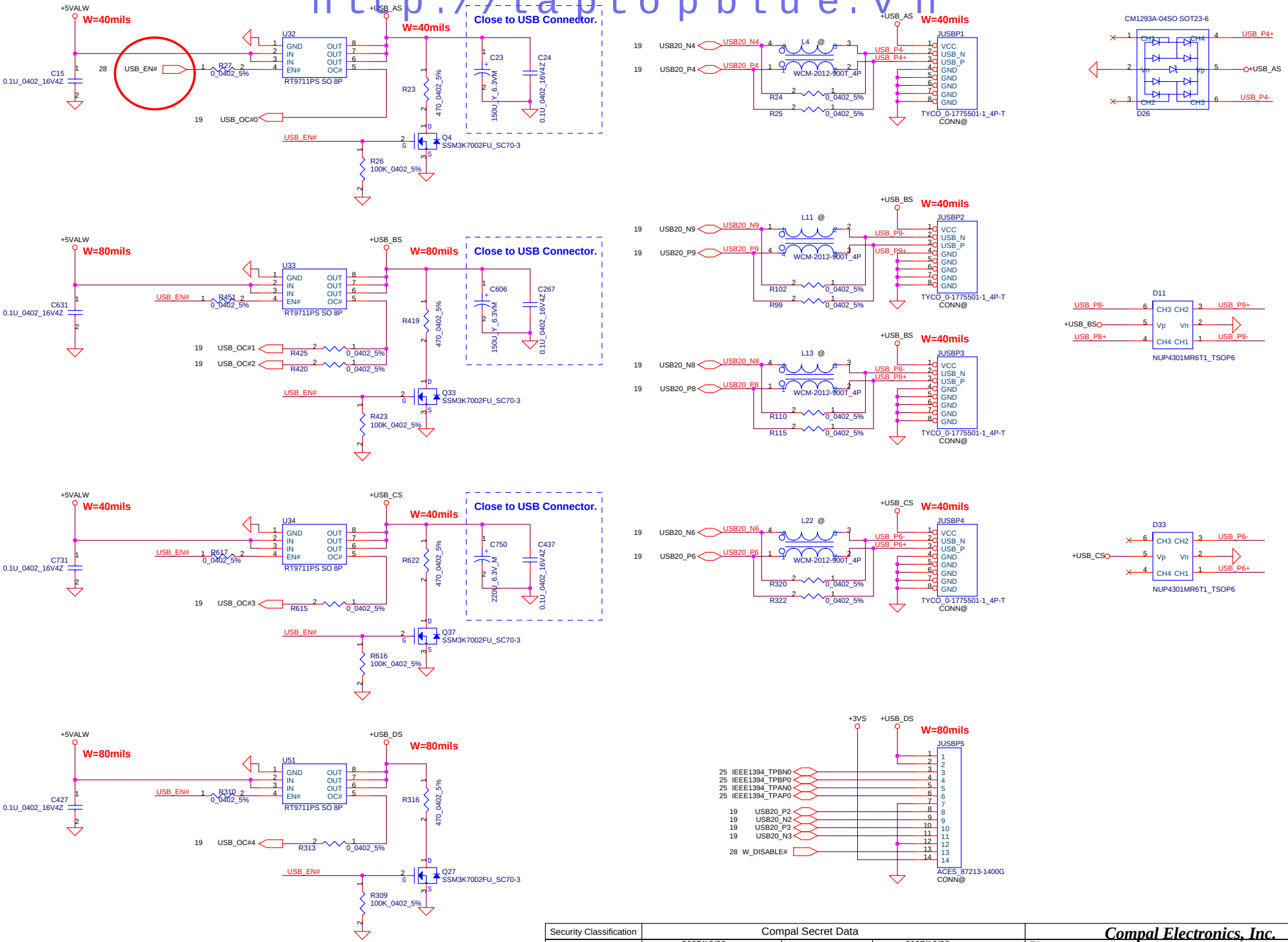

Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: **USB / 1394 Conn**

Size	Document Number	Rev
Custom	LA-4131P	0.2

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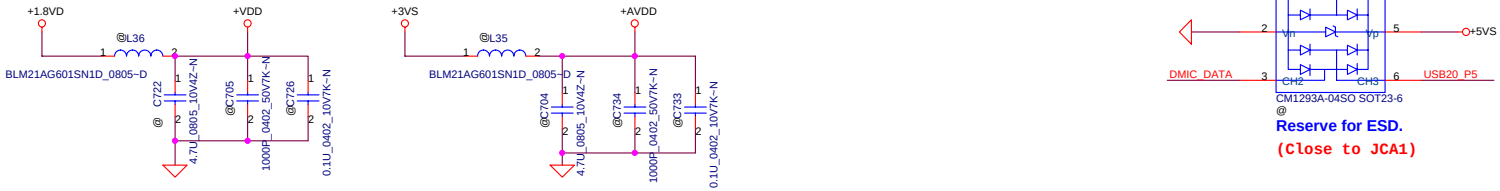
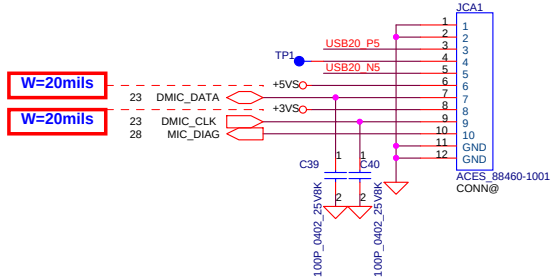
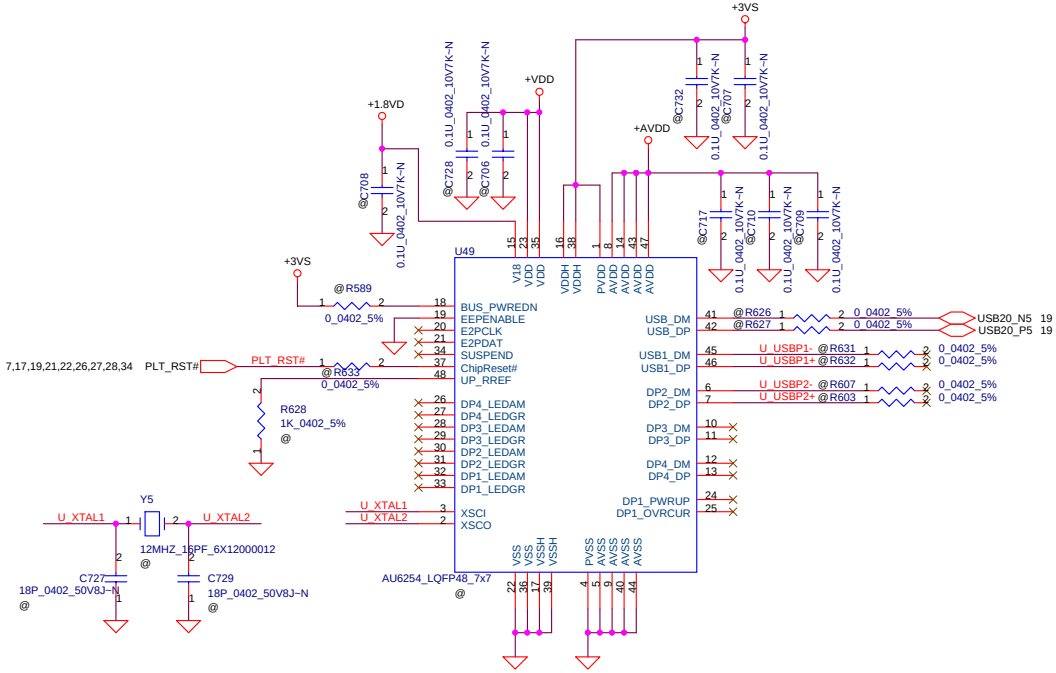
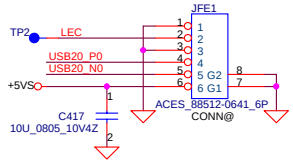


Camera Conn

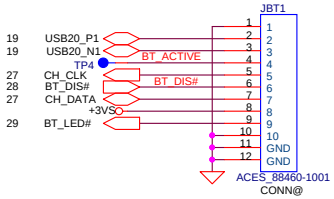


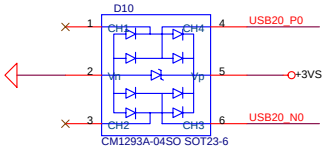


Felica Conn

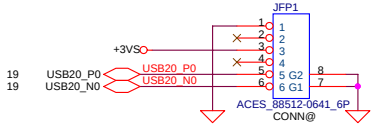


Blue Tooth





Finger Printer



Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: USB Hub / Camera / Felcia / FP/ BT

Size: Custom | Document Number: LA-4131P | Rev: 0.2

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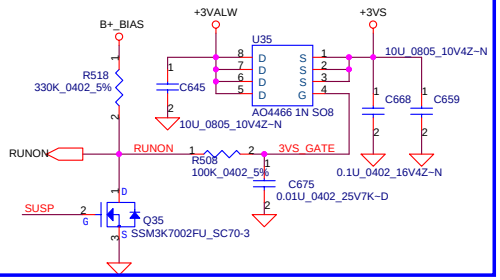
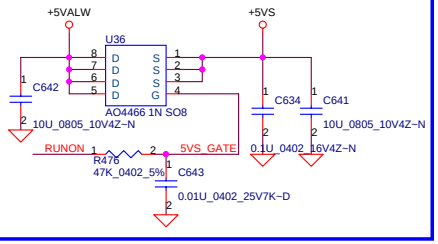
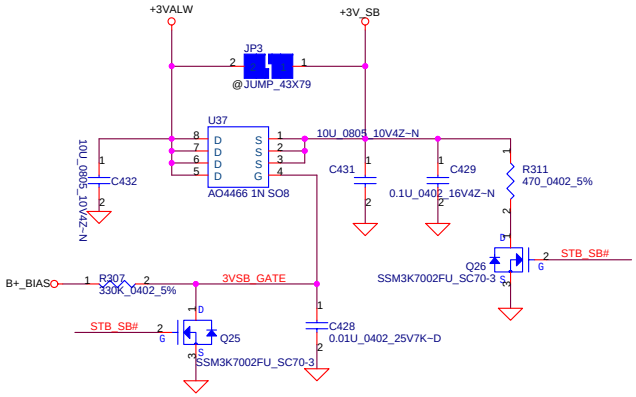
+3VALW to +3VS Transfer 4.5A

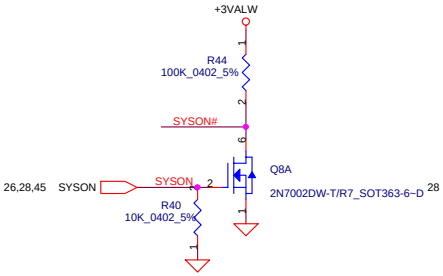


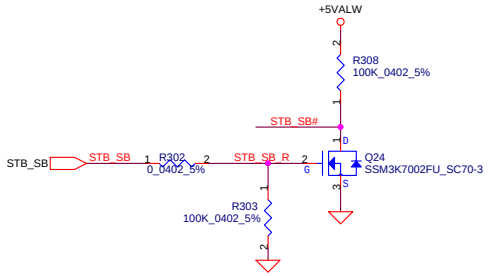
+5VALW to +5VS Transfer 6.5A

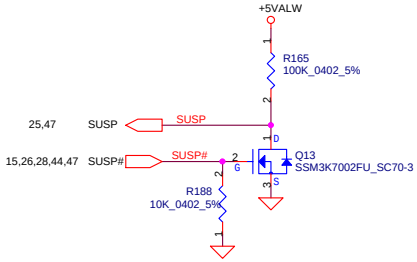


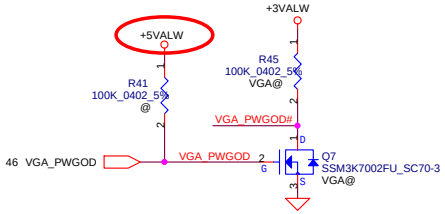
+3VALW to +3V_SB



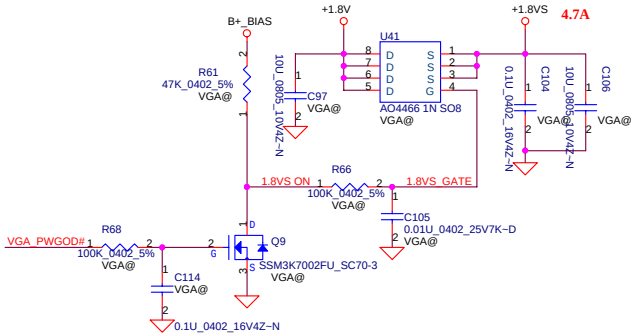




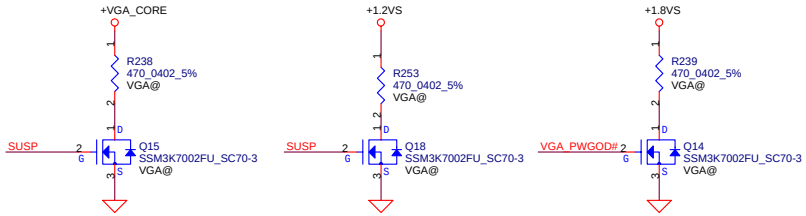




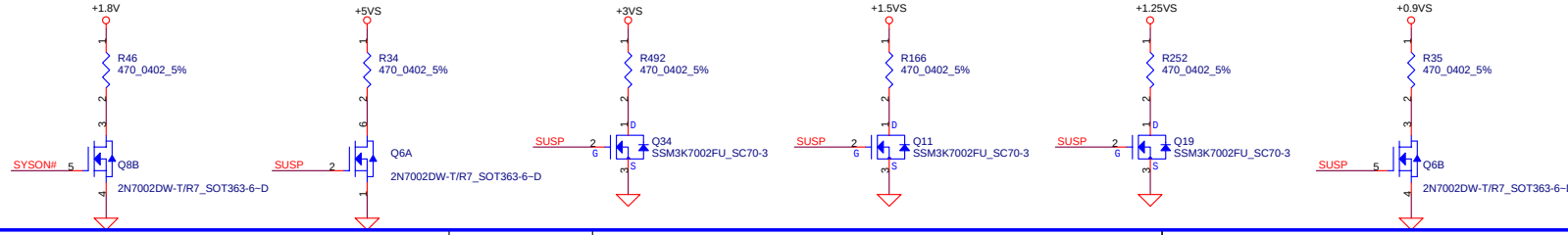
+1.8V to +1.8VS Transfer (For Discrete)



VGA Discharge Circuit



Discharge Circuit



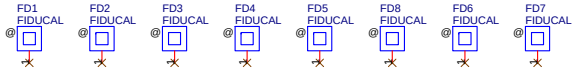
Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

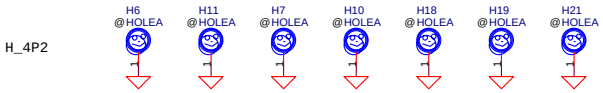
Compal Electronics, Inc.

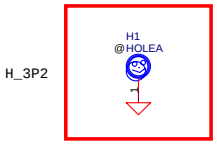
Title: DC/DC Interface

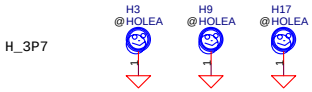
Size: Custom | Document Number: LA-4131P | Rev: 0.2

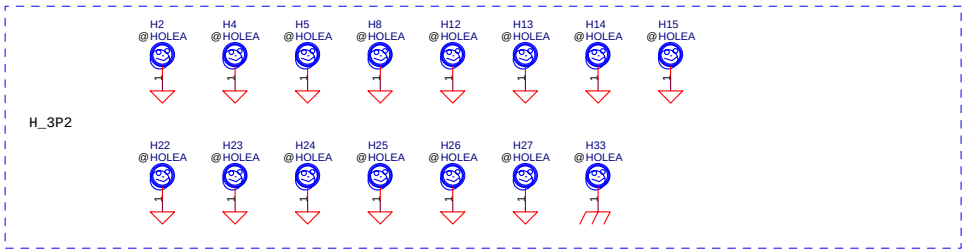
Date: Monday, February 18, 2008 | Sheet 32 of 53

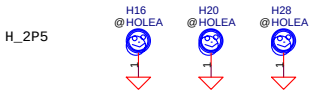


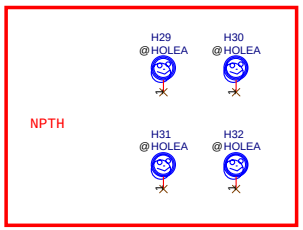












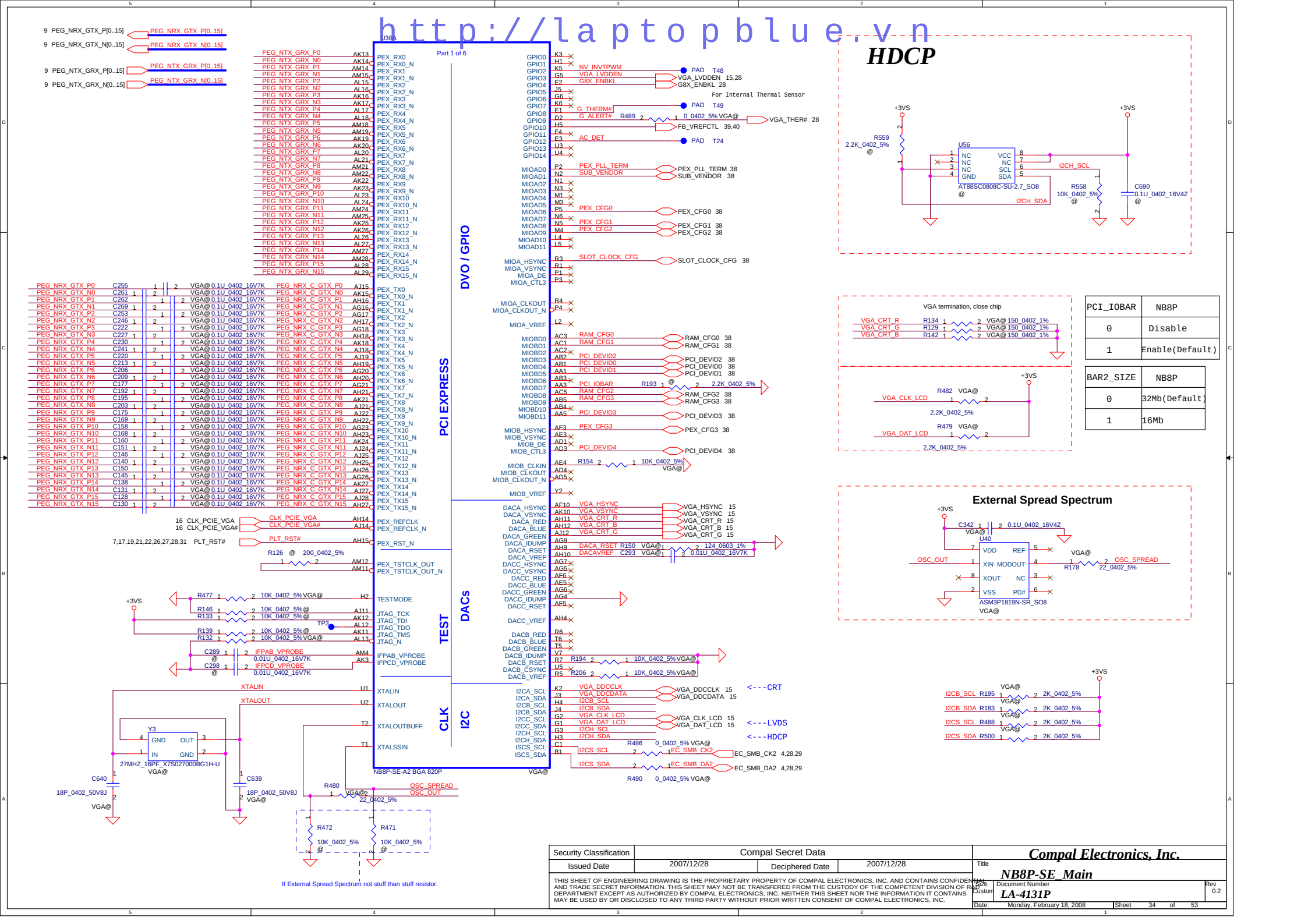
Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: **Screws**

Size	Document Number	Rev
Custom	LA-4131P	0.2

Date: Monday, February 18, 2008 Sheet 33 of 53



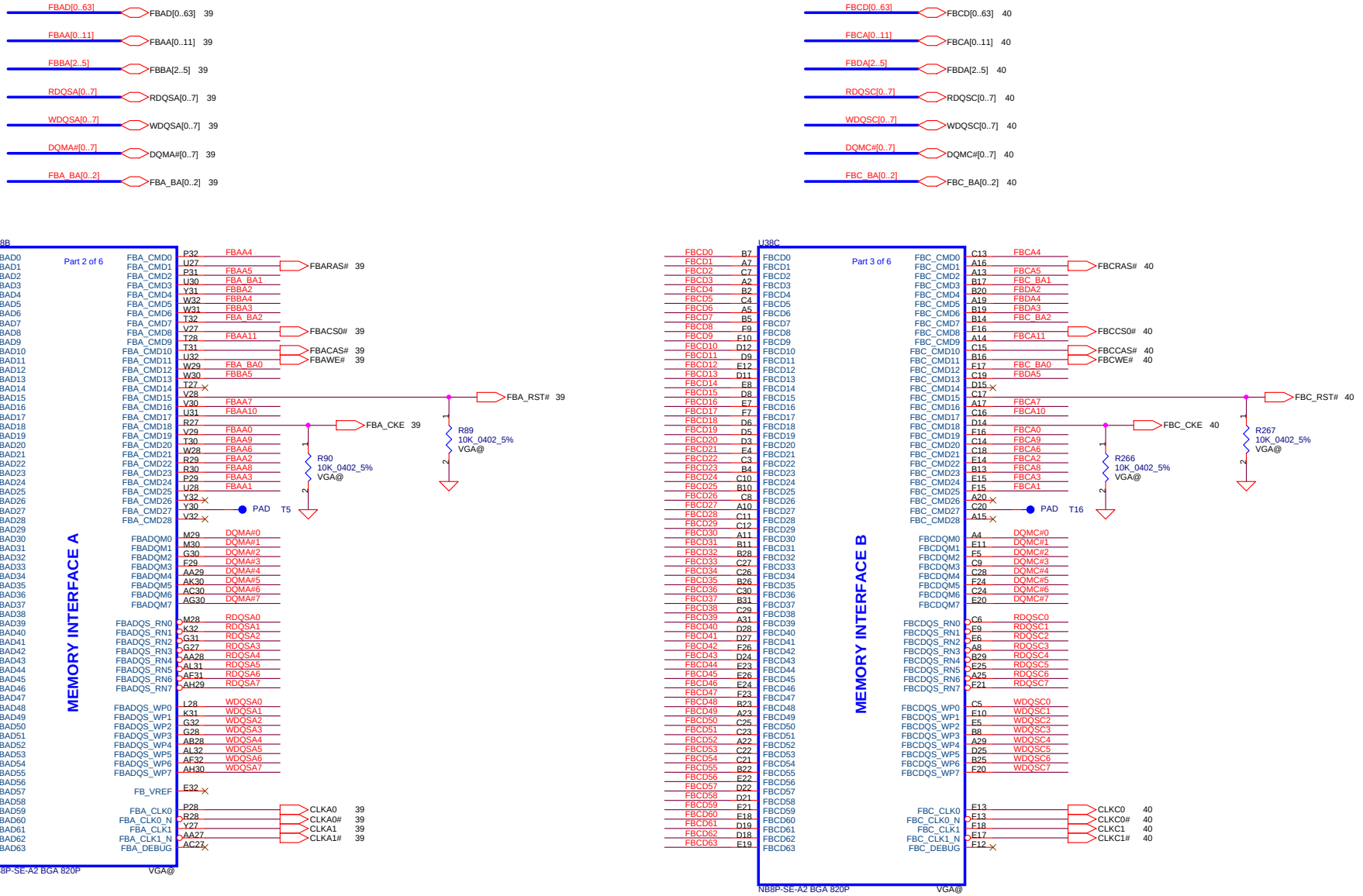
Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: NB8P-SE_Main

Size: Custom | Document Number: LA-4131P | Rev: 0.2

Date: Monday, February 18, 2008 | Sheet 34 of 53



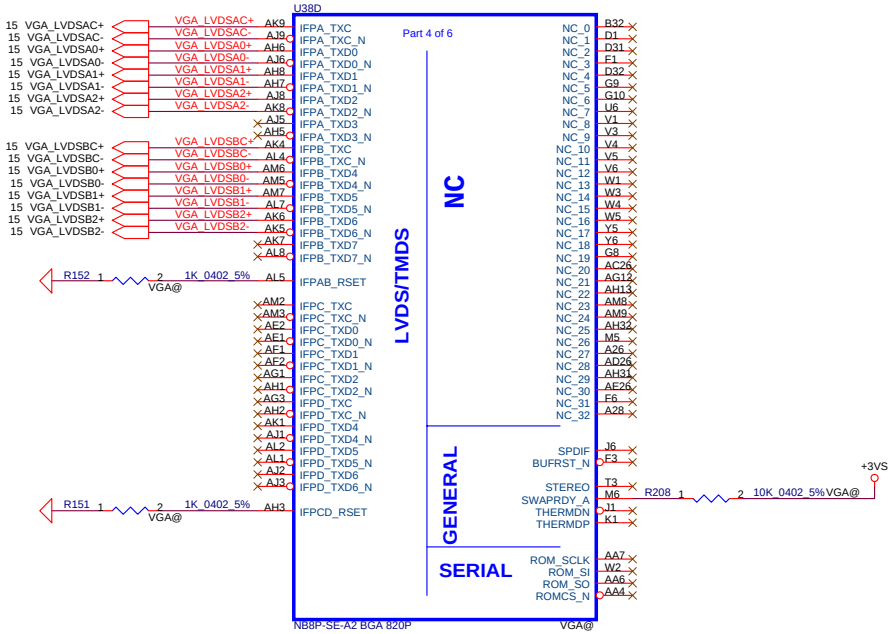
Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

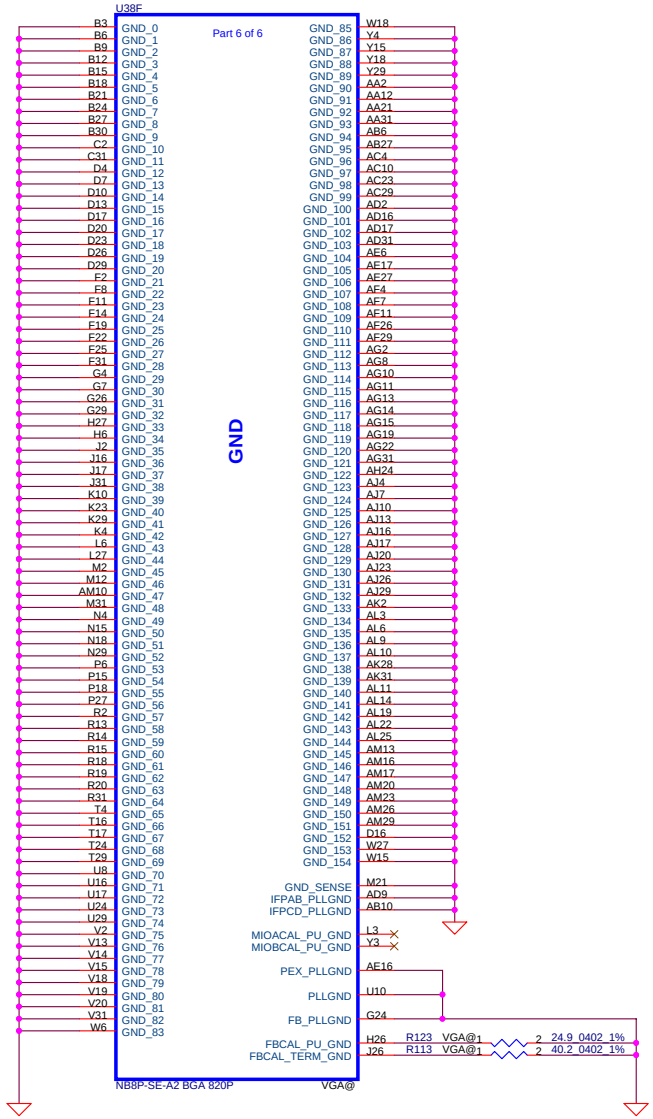
Compal Electronics, Inc.

Title: **NB8P-SE_Memory Interface**

Size	Document Number	Rev
Custom	LA-4131P	0.2

Date: Monday, February 18, 2008 Sheet 35 of 53





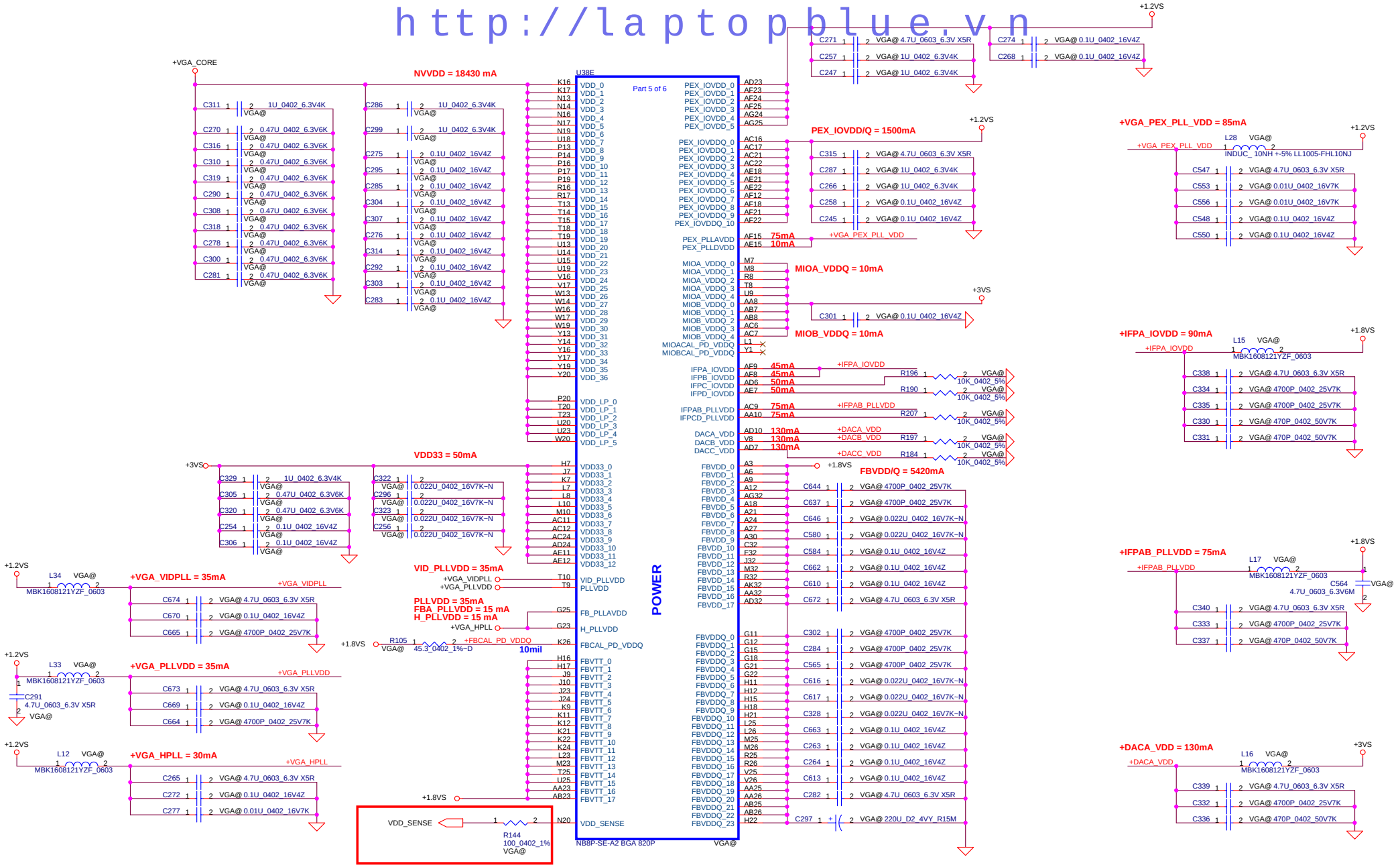
Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: NB8P-SE_LVDS / TMDS / GND

Size: Custom | Document Number: LA-4131P | Rev: 0.2

Date: Monday, February 18, 2008 | Sheet 36 of 53



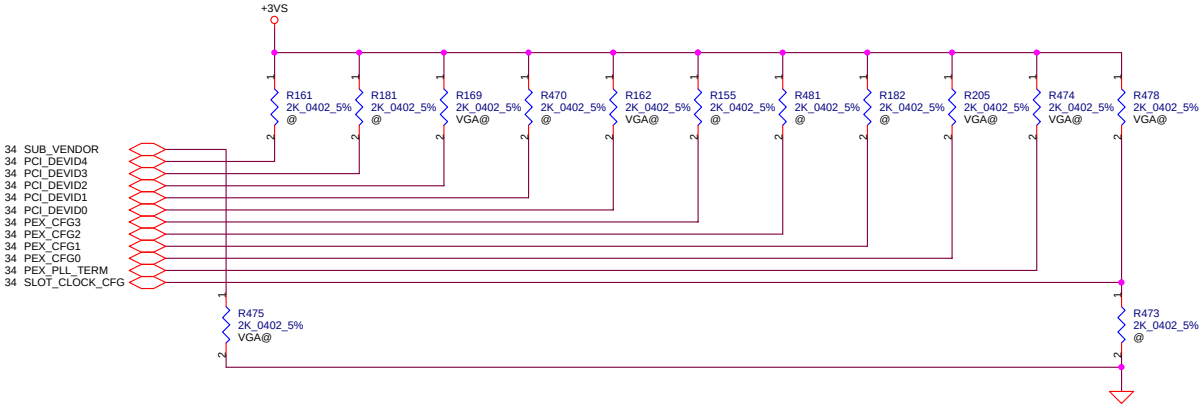
Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: NB8P-SE_Power

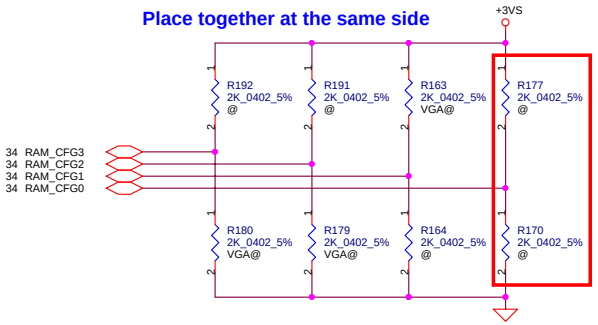
Size: | Document Number: LA-4131P | Rev: 0.2

Date: Monday, February 18, 2008 | Sheet 37 of 53



Straps	SUB_VENDOR	PCI_DEVID [4:0]	PEX_CFG[3:0]	PEX_PLL_TERM	SLOT_CLK_CFG
Description	0: BIOS not present 1: BIOS present	NB8P-GS: 0x0407 NB8P-GT: 0x0408 NB8P-SE: 0x0425	0X1	0: Enable 1: Disable	0: GPU&MCH do not share a common ref. CLK. 1: GPU&MCH share a common ref. CLK.
Setting	0: BIOS not present	NB8P-SE: 0x0425 (00101) Internal Pull down	0001: 0X1 (0001) Internal Pull down	1: Disable	1: GPU & MCH share a common ref. CLK.

Place together at the same side



RAM_CFG[3:0]

RAM_CFG3 0 = Single Rank 1 = Dual Rank	RAM_CFG2 RAM Size 0=16Mx32 1= 8Mx32	RAM_CFG[1:0] Vendor 10 = Hynix 11 = Samsung		Description NB8P-GS
0	0	0	0	
0	0	0	1	
0	0	1	0	Hynix (16M*32 4pcs = 256MB)
0	0	1	1	Samsung (16M*32 4pcs = 256MB)
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

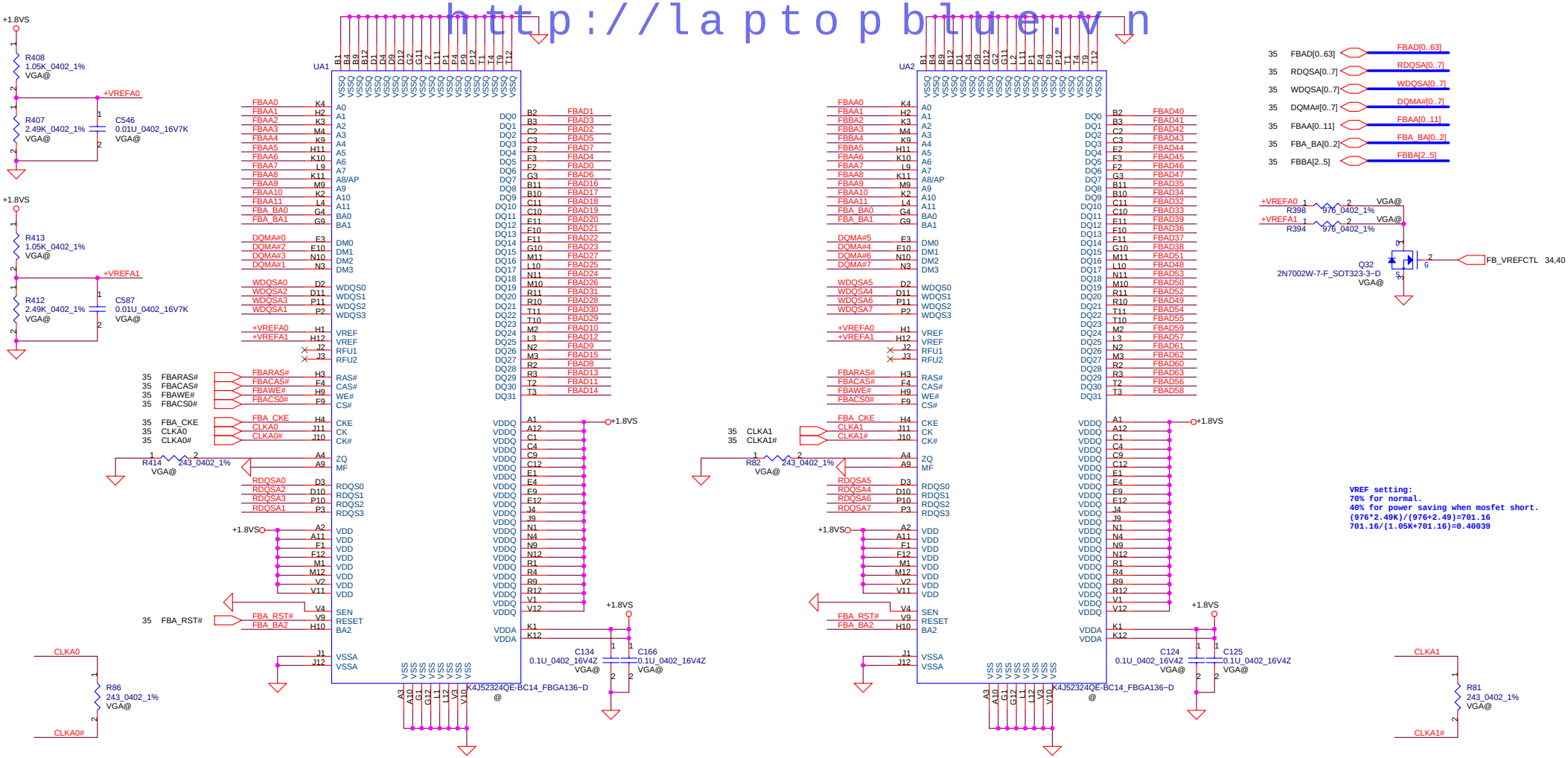
Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

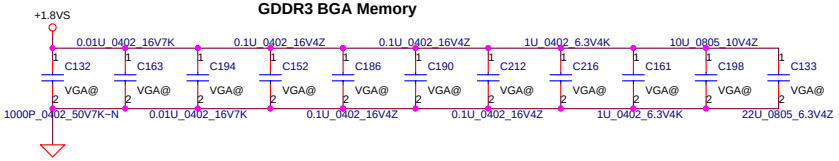
Title: NB8P-SE_Straps

Size: Custom | Document Number: LA-4131P | Rev: 0.2

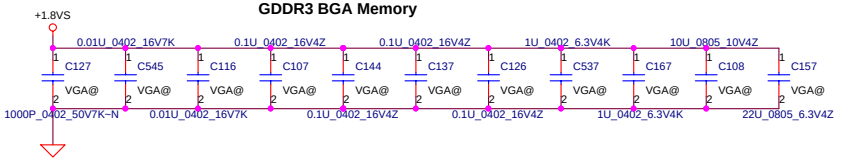
Date: Monday, February 18, 2008 | Sheet 38 of 53



GDDR3 BGA Memory



GDDR3 BGA Memory



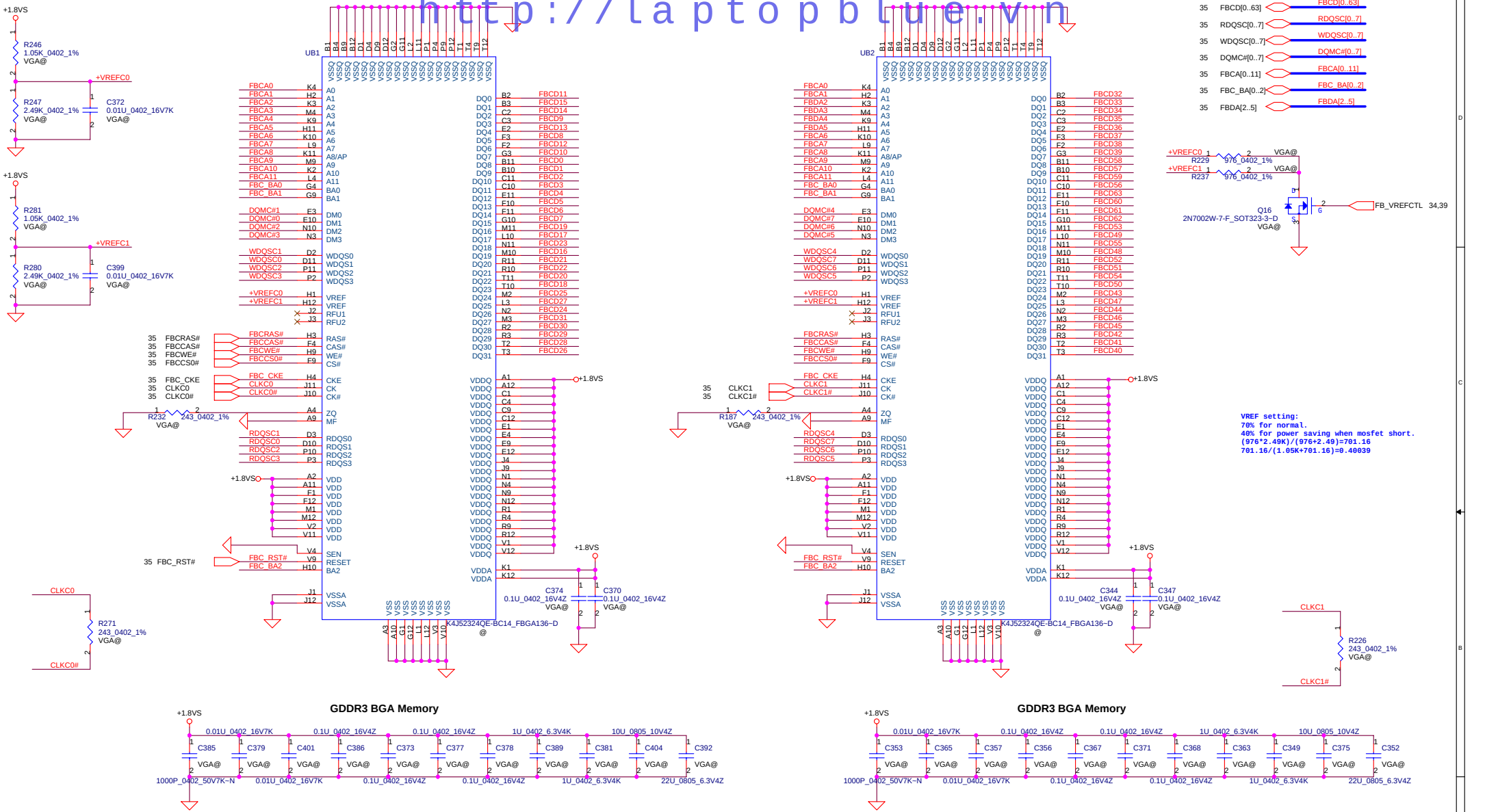
Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

Compal Electronics, Inc.

Title: GDDR3_A

Size: Custom | Document Number: LA-4131P | Rev: 0.2

Date: Monday, February 18, 2008 | Sheet 39 of 53



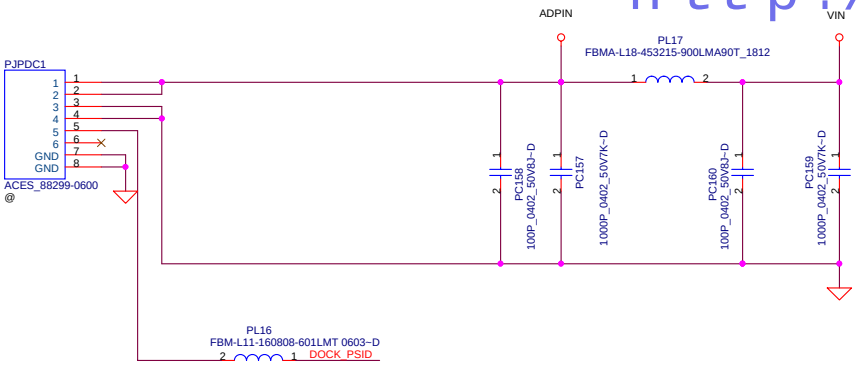
Security Classification	Compal Secret Data		
Issued Date	2007/12/28	Deciphered Date	2007/12/28

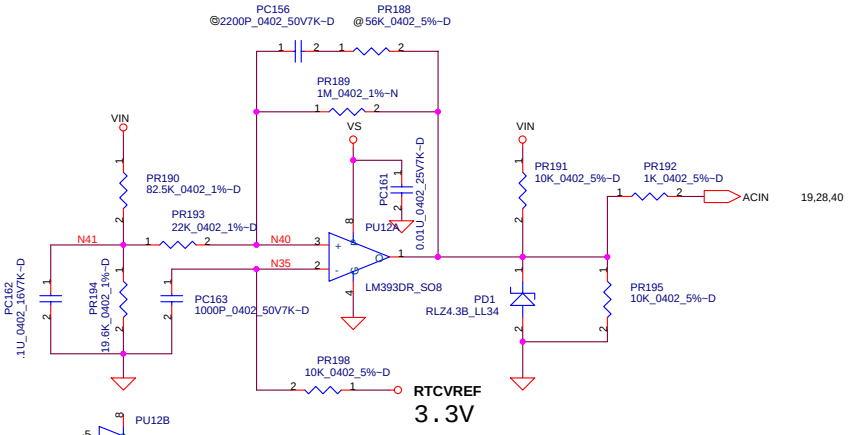
Compal Electronics, Inc.

Title: **GRRD3_B**

Size	Document Number	Rev
Custom	LA-4131P	0.2

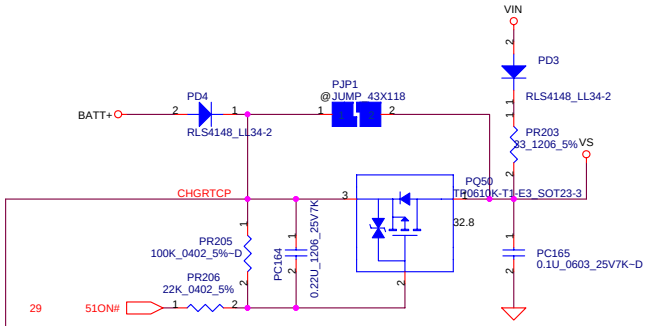
Date: Monday, February 18, 2008 Sheet 40 of 53

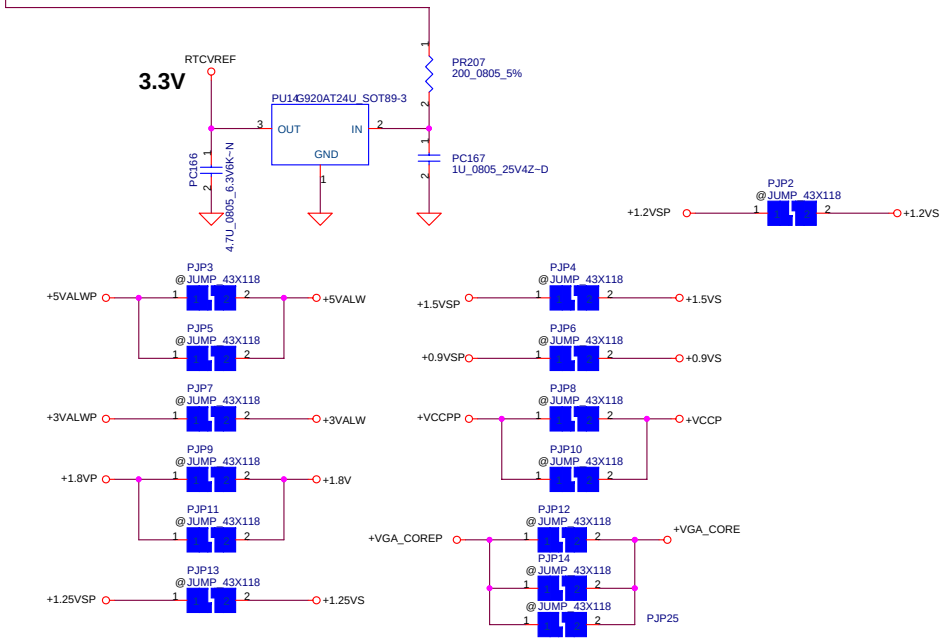


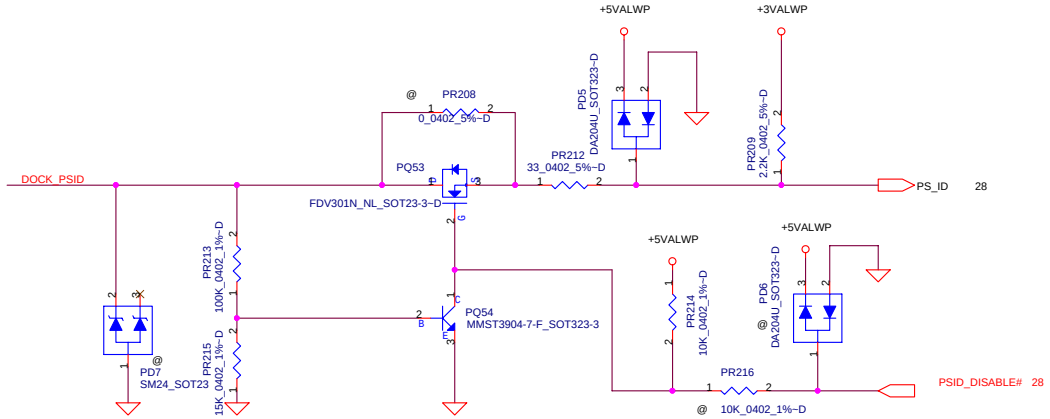


Vin Detector

	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813







Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/5/01

Title: **DCIN / Precharge**

Size	Document Number	Rev
Custom	JAL60	0.2

Date: Monday, February 18, 2008 Sheet 41 of 50

90W adapter
Icharge=(Vsrset/Vvdac)*(0.1/PR34)=3A
Iadapter=(Vacset/Vvdac)*(0.1/PR23)=3.65A
Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz

CP setting

ICHG setting

Cells selector

CELLS	GND	3 Cell
	VREF	4 Cell

COIN RTC Battery

IREF	Current
3.265V	3.3A
0.49V	0.5A

Move to power schematic

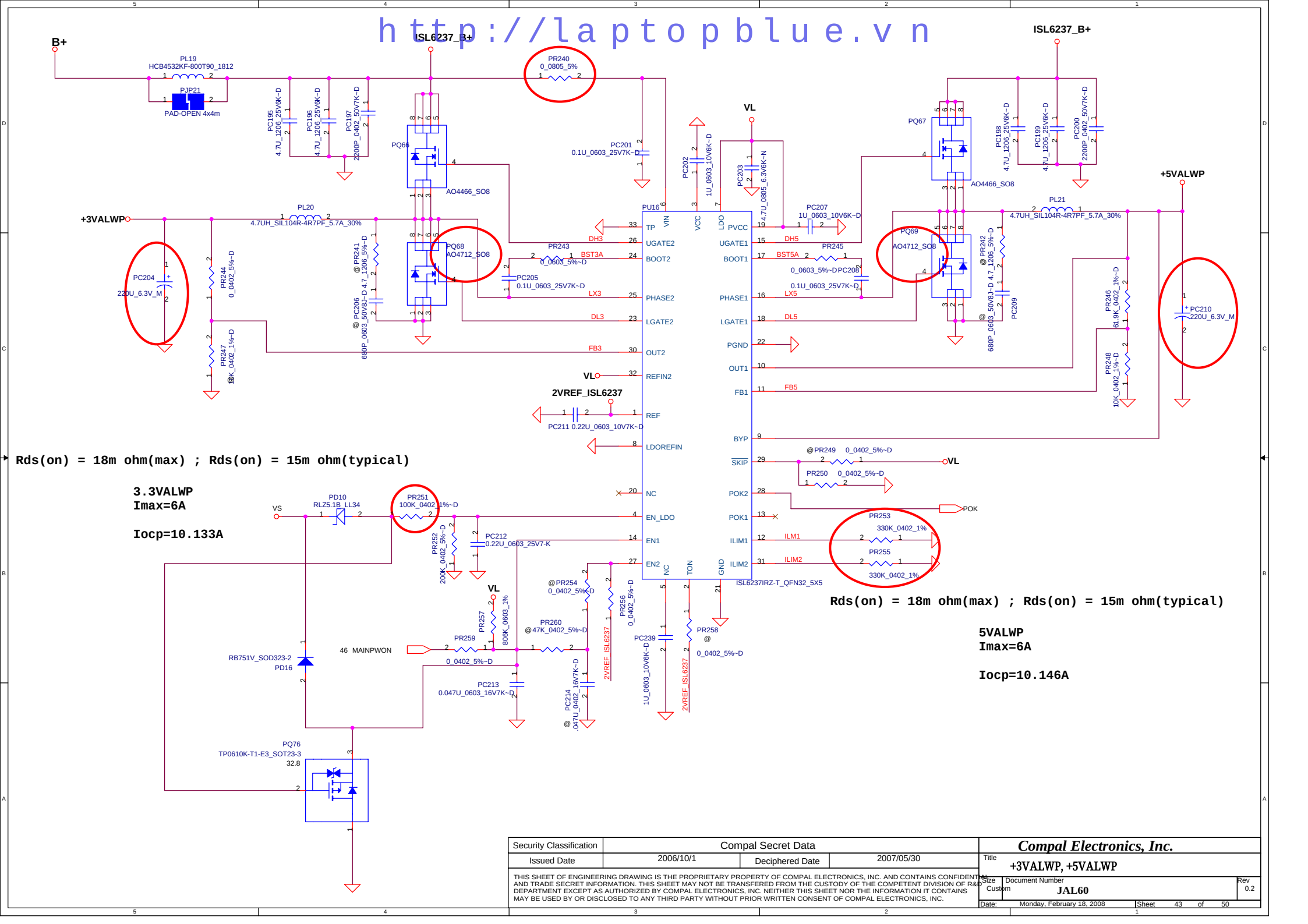
Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/5/01

Compal Electronics, Inc.

Title: Charger

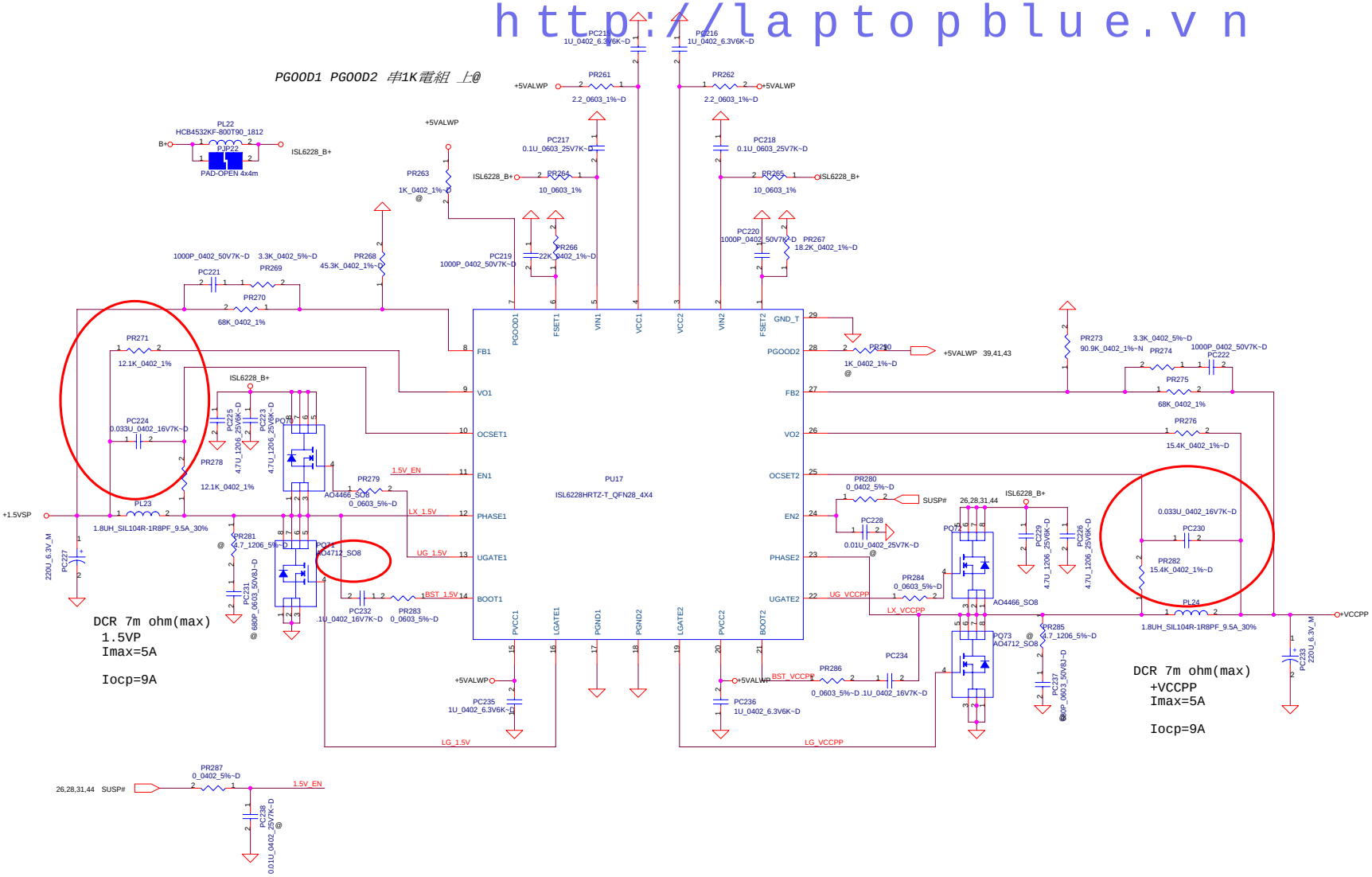
Size: B | Document Number: JAL60 **** | Rev: 0.2

Date: Monday, February 18, 2008 | Sheet 42 of 50



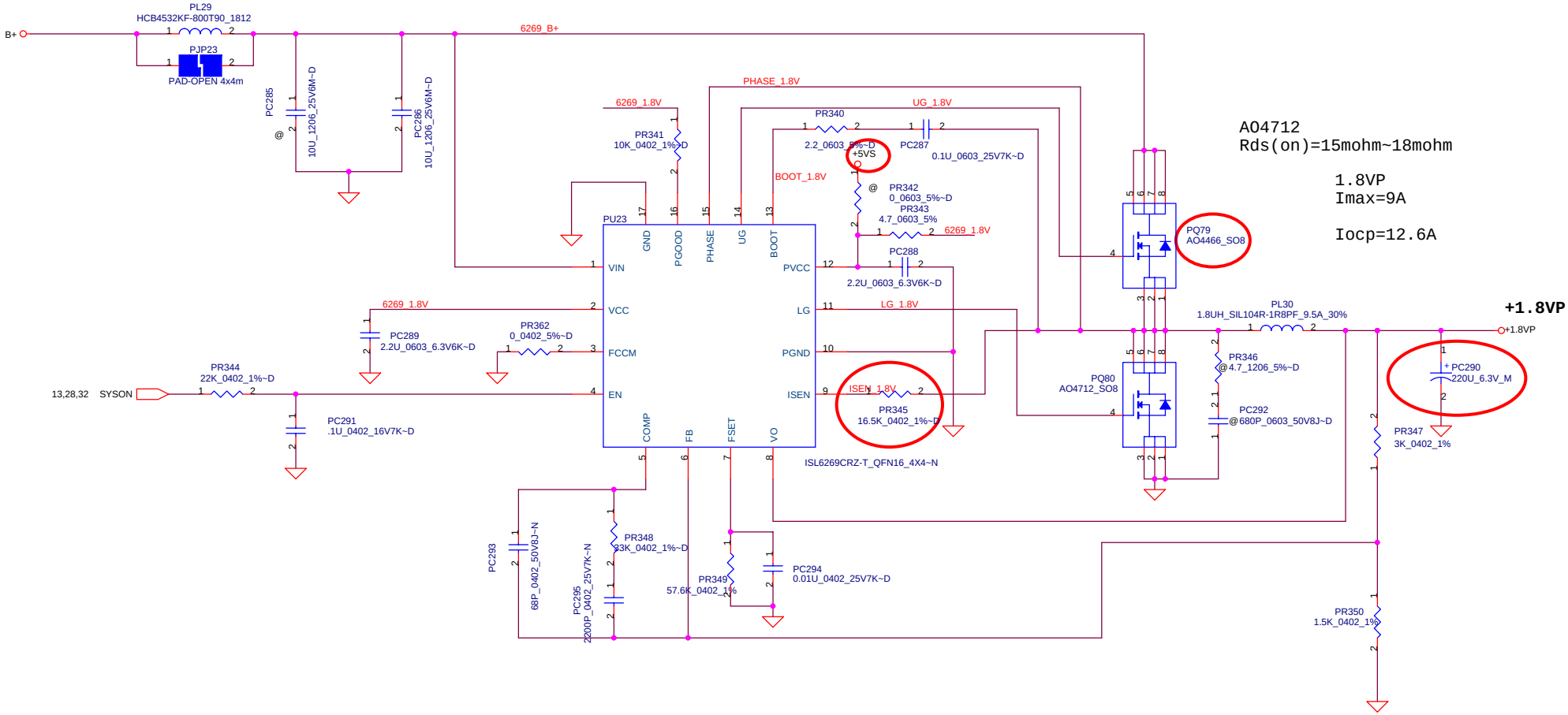
Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/05/30

Compal Electronics, Inc.			
Title: +3VALWP, +5VALWP			
Size: Custom	Document Number: JAL60		Rev: 0.2
Date: Monday, February 18, 2008	Sheet 43 of 50		



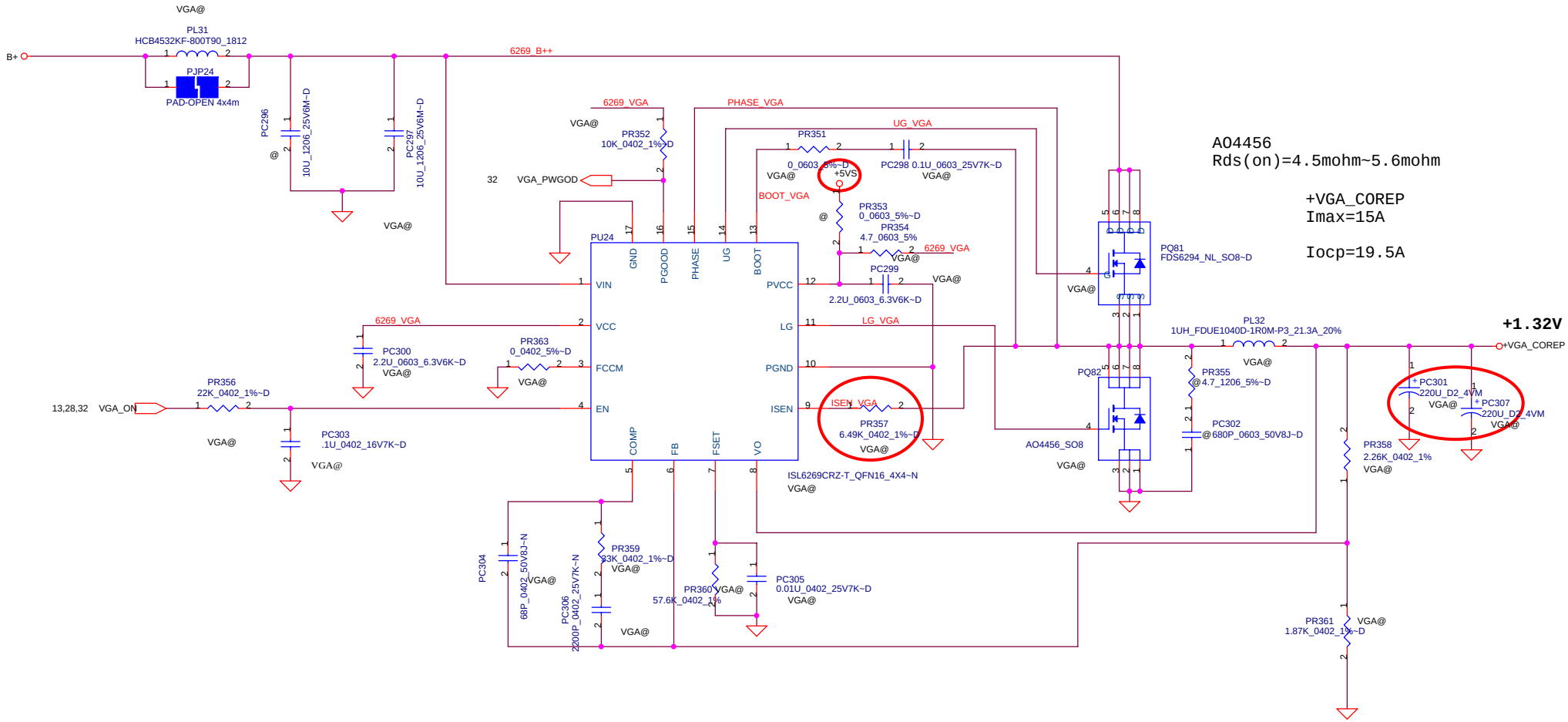
Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/5/01

Title	+1.5VP/VCCPP		
Size	Document Number	JAL60	Rev 0.2
Date:	Monday, February 18, 2008	Sheet 44 of 50	

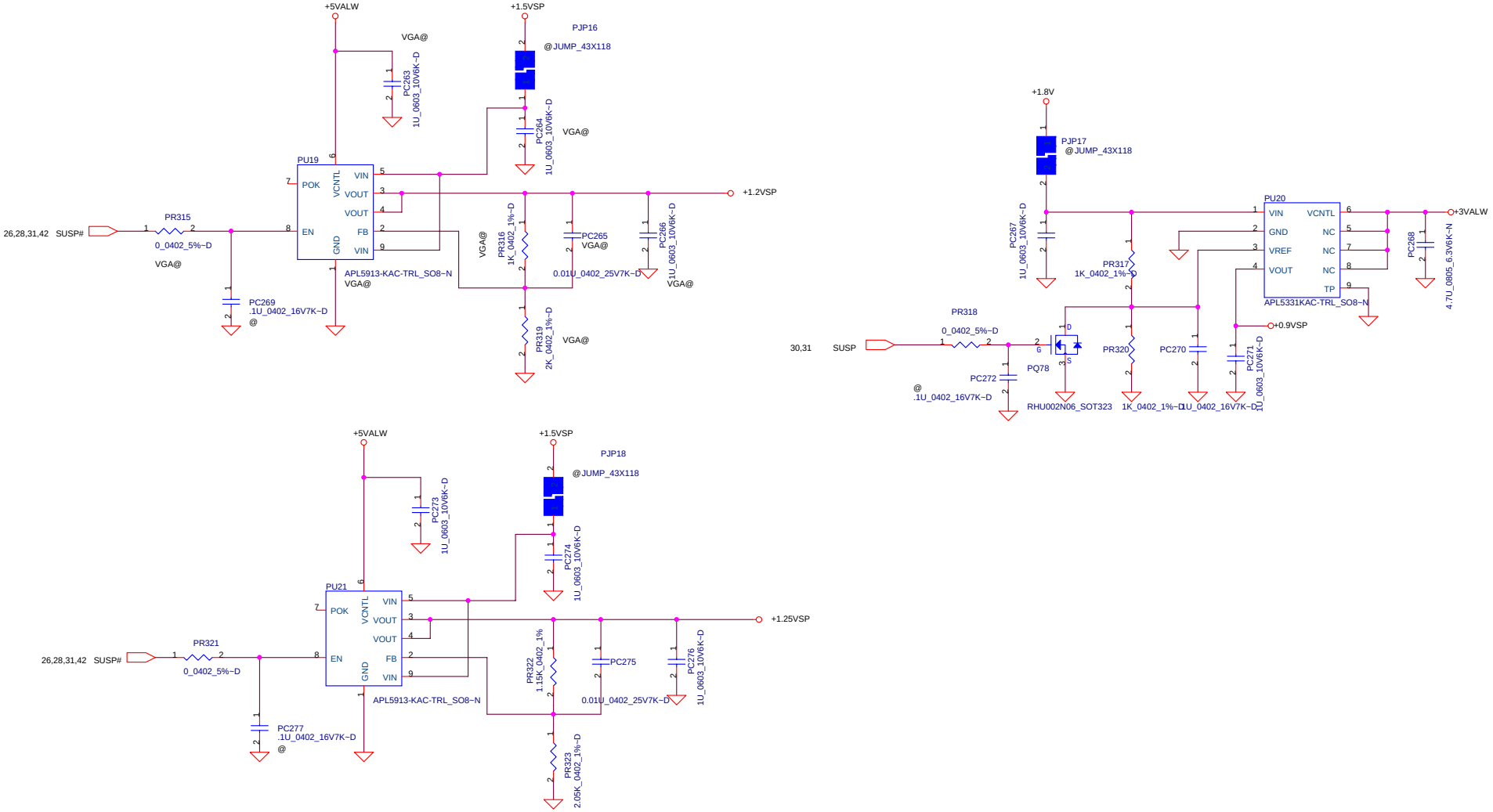


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2006/10/1	Deciphered Date	2007/05/30

Title	NB_CORE		
Size	Document Number		Rev
	JAL70		0.11
Date:	Monday, February 18, 2008	Sheet	45 of 10



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2006/10/1	Deciphered Date	2007/05/30
Title	+VGA_COREP		
Size	Document Number	JAL60	Rev 0.11
Date:	Monday, February 18, 2008	Sheet 46 of 10	



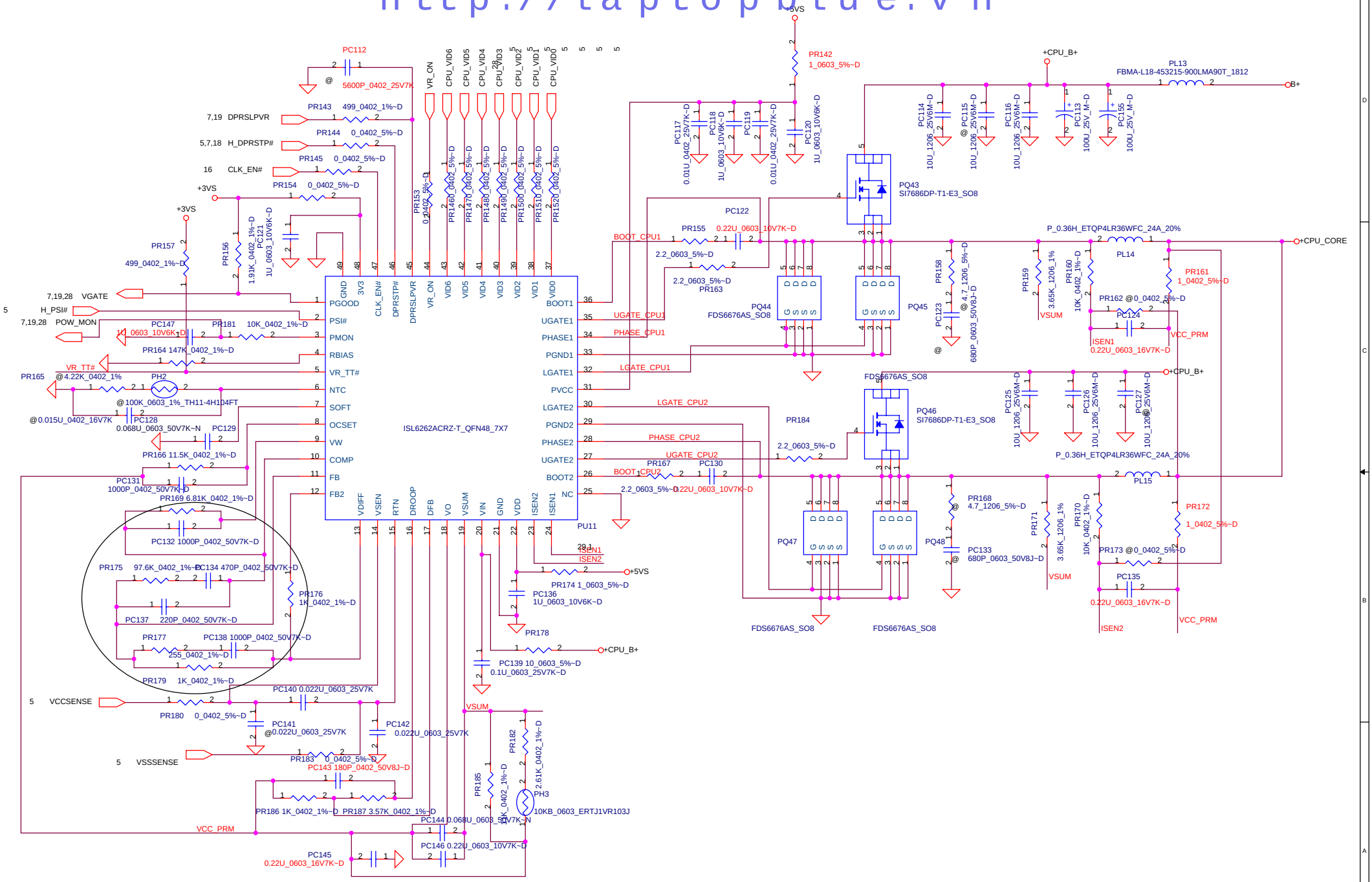
Security Classification	Compal Secret Data		
Issued Date	2005/10/1	Deciphered Date	2007/05/30

Compal Electronics, Inc.

Title: **+1.25VSP / +0.9VSP/ +1.2VSP**

Size	Document Number	Rev
Custom	JAL60	0.2

Date: Monday, February 18, 2008 Sheet 47 of 50



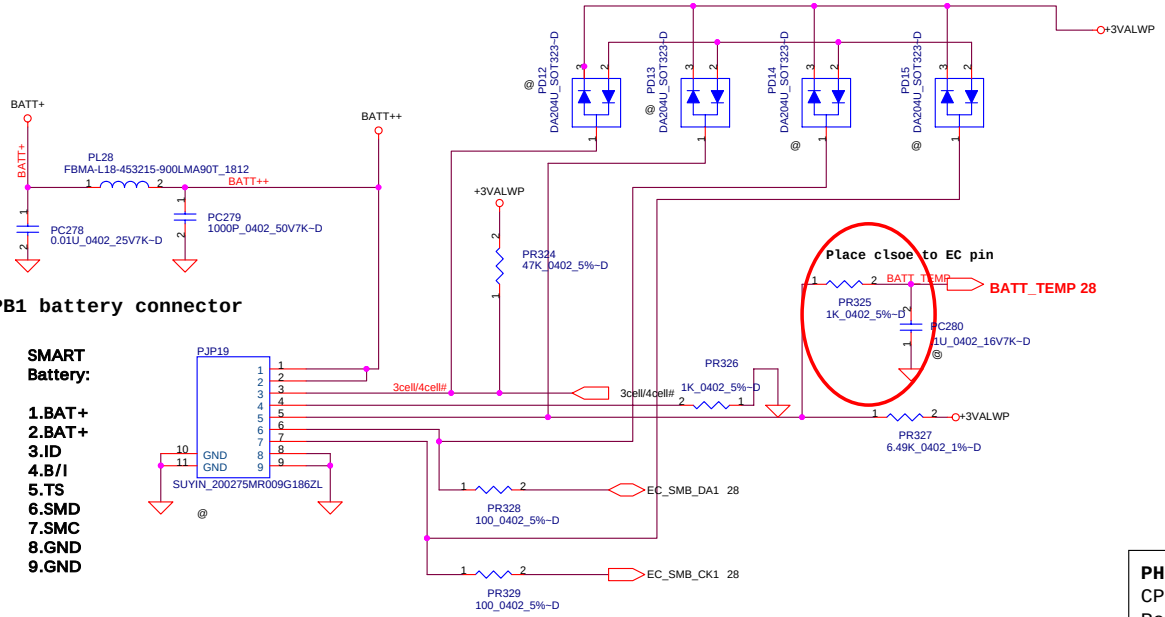
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
Custom	JAL60	0.1

Date: Monday, February 18, 2008 Sheet 48 of 50



PJPB1 battery connector

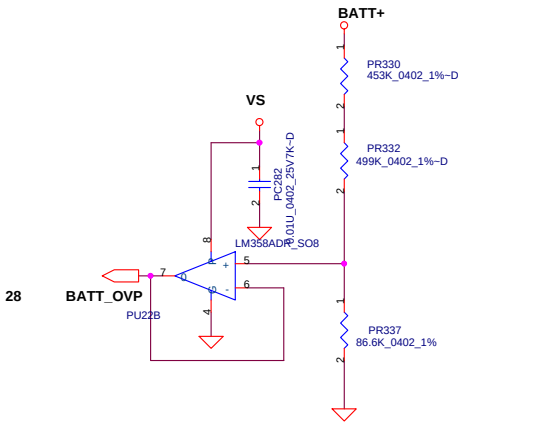
SMART Battery:

1.BAT+
2.BAT+
3.ID
4.B/I
5.TS
6.SMD
7.SMC
8.GND
9.GND

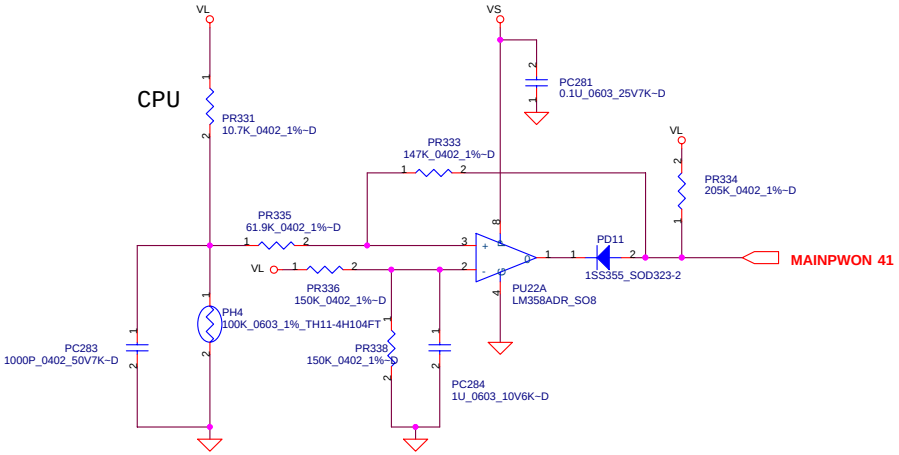
Battery Connect/OTP

CPU

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C



LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.111*BATT+



Security Classification	Compal Secret Data		
Issued Date	2005/10/1	Deciphered Date	2007/05/30

Compal Electronics, Inc.

Title: **BATTERY CONN**

Size: Custom | Document Number: **JAL60** | Rev: 0.2

Date: Monday, February 18, 2008 | Sheet 49 of 50

Version Change List (P. I. R. List) Page 1/1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	ALL	ALL Page	07/11/30	DELL	base on customer request change SD SE to *L part	ALL SD* SE*	
2	P40	CHARGER	07/12/11	COMPAL	in order to meet the JETA rule,the charge voltage will be auto adjust by EC	ADD PR53(4.3K) PR54 PR51	
3	P41	+3VALWP/+5VALWP	07/12/11	COMPAL	When battery only and 4s shut down the system can not turn off the 3valwp and 5valwp	ADD PD16 (RB751V),PQ76(TP0610K)	
4	P41	+3VALWP/+5VALWP	07/12/11	COMPAL	in order to trial run ISL6237 2'nd source,reserve PC239 in ISL6237 PIN5.	ADD PC239 (1U 0603 10V)	
5	P44	+VGA_CORE	07/12/11	COMPAL	Base on HW power budger,change the VGA_CORE high low side MOS and choke.	change PQ81 from AO4466 to FDS6294,PQ82 from AO4712 to AO4456,PL32 from 1.8uH 9.5A to 1uH 21.3A	
6	P39	DC-IN / Precharge	07/12/11	COMPAL	base on customer spec no need CHARGE RTC, delete CHARGE RTC limit resister	Del PR210,PR211	
7	P46	CPU_CORE	07/12/14	COMPAL	EMI request to increase resister in CPU_CORE low side mos gate pin	ADD PR163(2.2 ohm),PR184(2.2ohm)	
8	P43	1.8VP	07/12/14	COMPAL	EMI request to increase resister in 1.8VP BOOT pin	Change PR340 from 0 ohm to 2.2 ohm	
9	P40	CHARGER	08/01/04	COMPAL	disable BQ24751 VIN detecte function	CHANGE PQ62 to @ and PR232 to @	
10	P40	CHARGER	08/02/12	COMPAL	EC have drop volotage in CHGVADJ,it will make the charge voltage not correct	CHANGE PR53 from 4.3k to 210k and PR54 from 10k to 499k	
11	P44	+VGA_CORE	08/02/12	COMPAL	Base on HW power budger,change the VGA_CORE output capacity	change PC301,PC307 from SF22001M300 S ELE CAP 220U 6.3V M F60(6.3X5.7) PXC to SGA20221150 S POLY C 220U 4V M D2 PSL LESR15M H1.9	
12							

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Title	PW PIR-1		
Size: Custom	Document Number: JAL60		Rev: 0.1
Date: Monday, February 18, 2008	Sheet 50 of 50		

Version Change List (P. I. R. List) Page 1/1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	28	EC_KB926/Reed Switch/BIOS/TPM	2007/11/14	Compal_HW	Change Board ID.	Change R459 to 8.2K ohm.	0.2
2	38	NB8P-SE_Straps	2007/11/14	Compal_HW	There is display issue on Discrete platform.	Not stuff R784.	0.2
3	32	DC/DC Interface	2007/11/19	Compal_HW	Sometime system can't detect USB device.	Change R522 pull high to +5VALW. (for SUSP)	0.2
4	15	CRT Conn/LCD Conn	2007/12/03	Compal_HW	Support BIST and LCD detect function for LCD panel.	Add nets: LCD_DET# , BIST and Modify the pin definition of JP4.	0.2
5	23	Audio Codec_ALC268	2007/12/03	Compal_EMI	There are EMI issue on DMIC_DATA and DMIC_CLK.	Add R933, R934, C1189, C1190 for EMI.	0.2
6	25	OZ129_Card Reader/1394	2007/12/03	Compal_HW	OZ129 has power sequence and leakage issue.	Update the circuit of OZ129 on Page 25.	0.2
7	28	EC_KB926/Reed Switch/BIOS/TPM	2007/12/03	Compal_HW	Can't Wake up on LAN.	Change R464 pull high to +3VALW for WOL.	0.2
8	28	EC_KB926/Reed Switch/BIOS/TPM	2007/12/03	Compal_HW	Support Wake up from USB Port and replace USB HUB port arrangement.	Add USB_EN# to enable USB power swith.	0.2
9	29	PWR_OK/BTN/KB/TP	2007/12/13	Compal_HW	51ON# shout down issue.	Change R493 pull down to GND and del R494.	0.2
10	29	PWR_OK/BTN/KB/TP	2007/12/03	Compal_HW	Int. Keyboard can't work.	Modify the pin definition of JKB1.	0.2
11	30	USB/1394 Conn	2007/12/03	Compal_HW	Support Wake up from USB Port.	1.U32, U33, U34, U51 change input voltage to +5VALW. 2.JUSBP1~5 change USB differential pair from ICH8M.	0.2
12	32	DC/DC Interface	2007/12/03	Compal_HW	VGA_PWGOD sequence issue.	1.Change R551 pull high to +5VALW and don't stuff R551. 2.Change VGA_PWGOD to PR352 pin2.	0.2
13	15	CRT Conn/LCD Conn	2007/12/13	Compal_HW	Dell 17" LCD Panel gray color issue.	Add Q83, Q84, R942, R943, C1191~C1194 for Dell 17" panel.	0.2
14	22	Realtek RTL8111C-GR	2007/12/13	Compal_EMI	These is EMI issue on Transformer.	Add R945~R952 and C1195~C1198 for EMI.	0.2
15	22	Realtek RTL8111C-GR	2007/12/18	Compal_HW	RJ-45: LED support "link" and "activity" status.	1.Change the connector of JLAN1. 2.Add D41, D42, D43, D44, R953, R954, R955.	0.2
16	15	CRT Conn/LCD Conn	2007/12/19	Compal_EMI	EMI' request.	Del CRT_GND, R105, R107 for EMI.	0.2
17	31	USB Hub/Camera/Felcia/FP/BT	2007/12/24	Compal_HW	Finfer Print assermble FFC.	Modify the definition of JFP1.	
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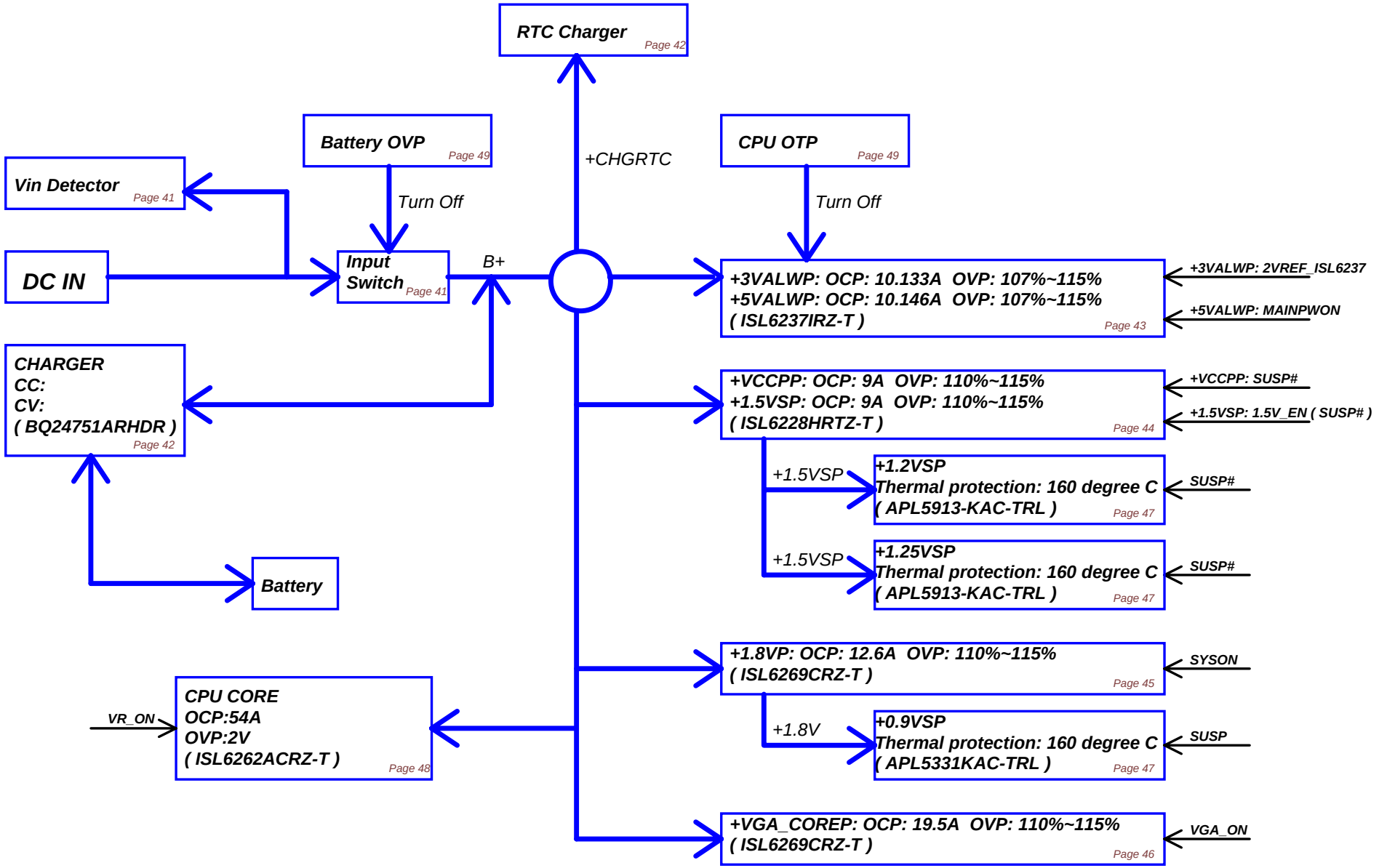
JAL60 Power Block



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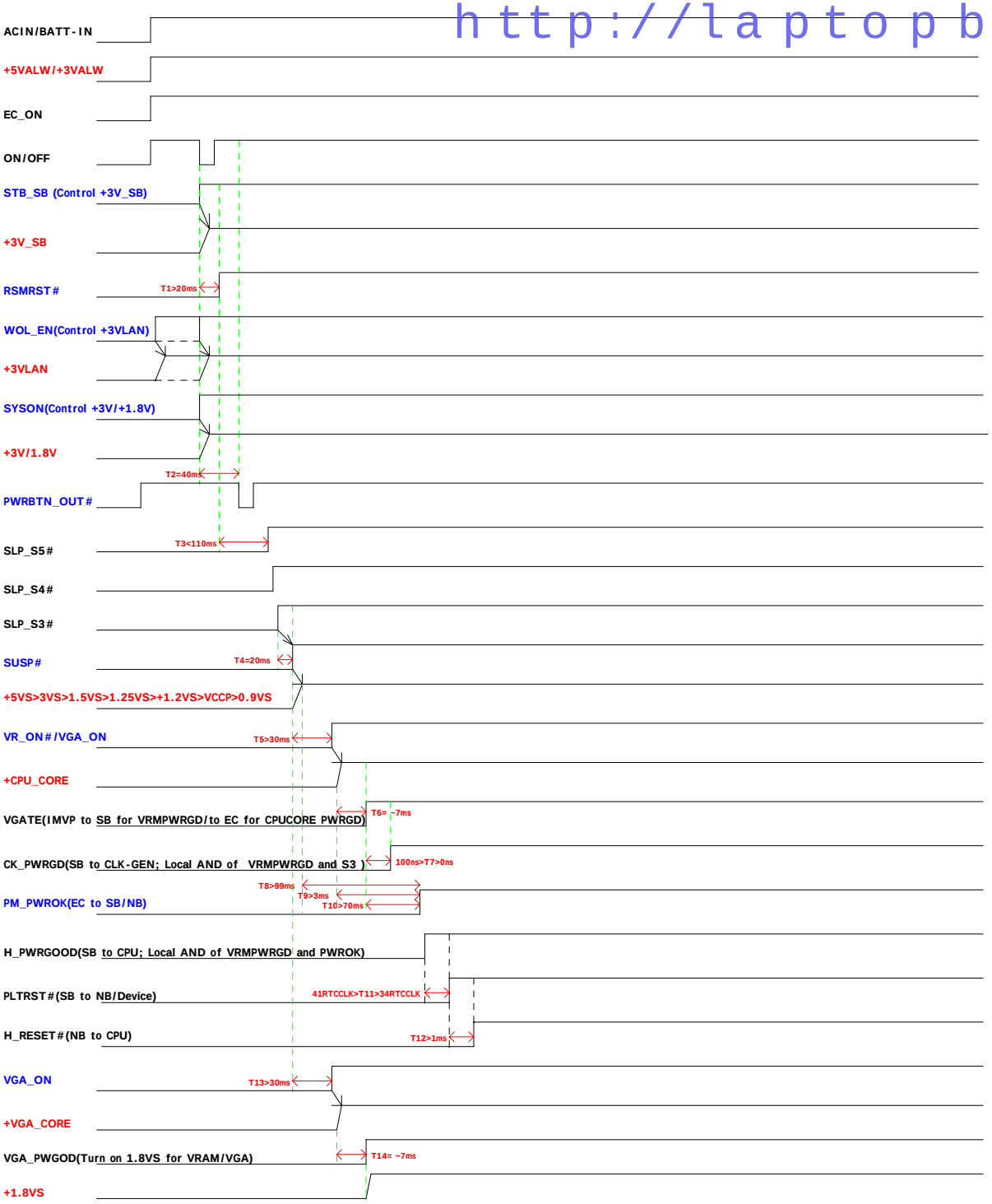

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