1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2010-07-23

SCHEM,MLB,K16

07/23/2010

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8467	1	SCHEM,MLB,K16	SCH	CRITICAL	
820-2838	1	PCBF,MLB,K16	PCB	CRITICAL	

DRAWING TITLE: SCHEM,MLB,K16

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

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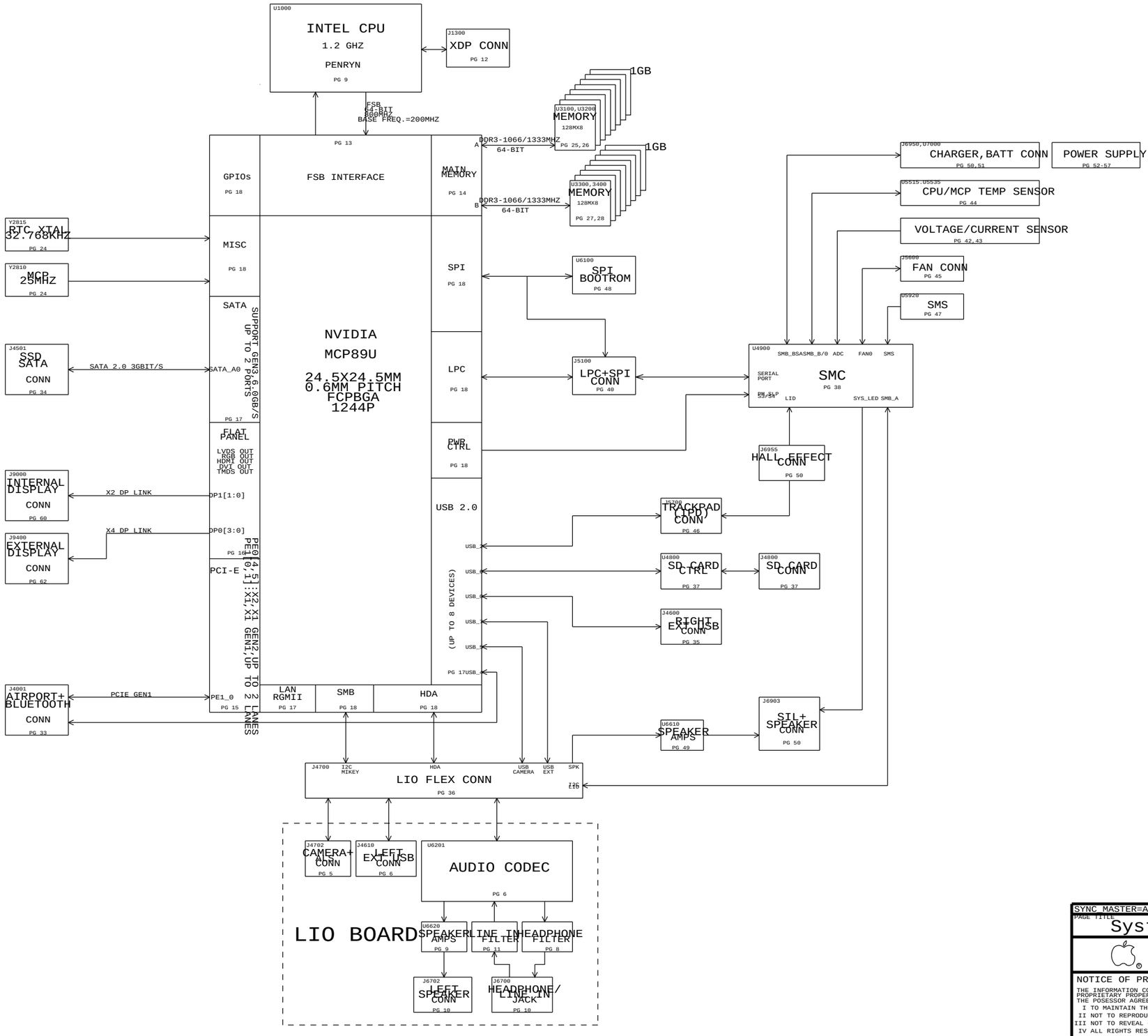

SYNC_MASTER=ALAN.DAI SYNC_DATE=02/26/2010

PAGE TITLE
System Block Diagram

Apple Inc.

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K16 POWER SYSTEM ARCHITECTURE

PP18V5_DCIN_CONN
Q7080
Q7085
PPDCIN_G3H_OR_PBUS
PBUS_VSENSE
ENABLE
3.425V G3HOT
LT3470
U6990
VOUT
PP3V42_G3H_REG
(60MA MAX CURRENT)
SMC PWRGD
RN5VD30A-F
U5010
8A FUSE
F7040
PPVBAT_G3H_CHGR_REG
PPBUS_G3H
Q5315
PBUS_G3H_VSENSE
AC ADAPTER IN
DCIN(16.5V)
F6905
6A FUSE
CHGR_EN (S5)
ENABLES
VIN
VOUT
R7020
SMC_DCIN_ISENSE
PBUS SUPPLY/ BATTERY CHARGER
ISL6259
U7000
R7050
SMC_BATT_ISENSE
CPUVTTS0_EN (S0)
CPUVTT
(1.05V)
ISL95870
U7600
EN_PSV
PGOOD
PP1V05_S0
(11.5A MAX CURRENT)
CPUVTTS0_PGOOD
J6950
3S2P
(9 TO 12.6V)
PPVBAT_G3H_CONN
Q7055
CHGR_BGATE
PPVBAT_G3H_CHGR_R
CPU VCORE
TPS51982
IMVP_VR_ON_R
VR_ON
PGOOD
SMC_CPU_VSENSE
SMC_CPU_ISENSE
PPVCORE_S0_CPU
(28A MAX CURRENT)
VR_PWRGOOD_DELAY
MCP89
PWRBTN*
PLTRST*
RSMRST*
CPUPWRGD(GPIO49)
CPU_RESET#
U1400
MCP_PS_PWRGD
U2850
LPC_RESET_L
CPU_PWRGD
FSB_CPURST_L
CPU
PWRGOOD
RESET*
U1000
4.5V AUDIO
MAX8840
U6200
PP4V5_AUDIO_ANALOG
PPBUS_G3H
MCP89
PM_SLP_S4_L
PM_SLP_S3_L
U1400
P3V3S3_EN
DDRREG_EN
P5VS3_EN_L
RC DELAY
SMC
U4900
P16
P60
SMC_PM_G2_EN (S5)
P5VS3_EN_L
U7840
LP8545
U9701
BKLT_EN
ENA
PPVOUT_SW_LCDBKLT
5V (RT)
3.3V
TPS51980
U7201
PGOOD1,2
VREG3
PP5V_S3_REG
(5.6A MAX CURRENT)
PP3V3_S5_REG
(5.3A MAX CURRENT)
P3V3S3_EN
P5V3V3_PGOOD
Q7910
PP3V3_S3_FET
Q4050
P3V3_S3_WLAN
PM_WLAN_EN_L
Q7940
PP5V_S0_FET
P5VS0_EN
Q7930
ISL8009B
U7750
PP0V9_S5_REG
P3V3S0_EN
PP3V3_S0_FET
1.5V
ISL8009B
U7710
PP1V5_S0_REG
1.05V
TPS74701
U7740
PP1V05_S0_MCP_PLL_REG
S0PGOOD_RST_L
P1V5S0_PGOOD
P5V3V3_PGOOD
MCPCORES0_PGOOD
CPUVTTS0_PGOOD
MCPPLLDO_PGOOD
SMC
RSMRST_OUT(P15)
PWRGD(P12)
IMVP_VR_ON(P16)
RSMRST_IN(P13)
PLT_RST*
PWR_BUTTON(P90)
P17(BTN_OUT)
RST*
99ms DLY
PM_RSMRST_L
IMVP_VR_ON_R
PM_PWRBTN_L
SMC_RESET_L
ALL_SYS_PWRGD
RSMRST_PWRGD
SMC_ONOFF_L
SLP_S5_L
SLP_S4_L
SLP_S3_L
SLP_S5_L(P95)
SLP_S4_L(P94)
SLP_S3_L(P93)
U4900
Q7890
AP_PWR_EN
PM_WLAN_EN_L
Q7890,Q7891
PM_SLP_S3_L
SMC_ADAPTER_EN
Q2300
PP1V5R1V35_SW_MCP
=DDRREG_EN
=DDTVTT_EN
1.5V
0.75V
TPS51116
U7300
MCPMEM_GATE
PP1V5_S3_REG
(13A MAX CURRENT)
PP0V75_S0_REG
(1A MAX CURRENT)
P1V5S0_EN
PBUSVSENSE_EN (S0)
P5VS0_EN (S0)
CPUVTTS0_EN
DDRVTT_EN
MCPCORES0_EN
P3V3S0_EN
MCP_CORE
ISL9563B
U7500
PPMCPCORE_S0_R
(25A MAX CURRENT)
R7525 PPMCPCORE_S0_REG
ISL88042
U7870
PP3V3_S0
PP1V5_S0
PP1V05_S0
V1
V2
V3
RST*

SYNC_MASTER=MARTIN.YEH	SYNC_DATE=2/25/2010
PAGE TITLE	Power Block Diagram
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K16 BOM Variants on following page

DRAM CFG CHART

VENDOR	CFG 0	CFG 1
HYNIX	0	0
SAMSUNG	0	1
MICRON	1	0
ELPIDA	1	1

SIZE	CFG 2
2GB	0
4GB	1

DIE REV	CFG 3
A	0
B	1

BOM Groups

BOM GROUP	BOM OPTIONS
K16_COMMON	COMMON,ALTERNATE,PROJ:K16,K16_MISC,MCP89U:A03,K16_DEBUG:ENG,K16_PROGPARTS,SPI:41MHZ,LVDDR3:YES,WLAN_PCTL:HW,IPD_5V:S5_INT,IPD_3V3:S5
K16_MISC	DP_ESD,DP_PWR:SMC,VFRQ:SLPS3,HVDDLDO:FIXED,MCPHVDD:P2V5,MCPPLL_R:REG,S0PGOOD_BJT,ISL6259_SCREENED:YES,DPI2C:SMC
K16_PROGPARTS	BOOTROM:UNLOCKED,SMC:PROG
K16_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,LPCPLUS,VREFMRGN:YES,EFI_DEBUG,S0PGOOD_ISL,MCPPLL_LDO,S3_S0_LED
K16_DEVEL:PVT	LPCPLUS
K16_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG:YES,XDP
K16_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
K16_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
DDR3:HYNIX_2GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:HYNIX_2GB
DDR3:SAMSUNG_2GB	DRAM_CFG0:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_2GB
DDR3:MICRON_2GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:MICRON_2GB
DDR3:ELPIDA_2GB	DRAM_CFG0:H,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_2GB
DDR3:ELPIDA_4GB	DRAM_CFG0:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_4GB
DDR3:HYNIX_4GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:SAMSUNG_4GB	DRAM_CFG0:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:MICRON_4GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:MICRON_4GB
CAPS:SS	SS_CAP_2_2UF,SS_CAP_10UF,SS_CAP_1UF,SS_CAP_22UF
CAPS:MU	MU_CAP_2_2UF,MU_CAP_10UF,MU_CAP_1UF,MU_CAP_22UF
CAPS:TY	TY_CAP_2_2UF,TY_CAP_10UF,TY_CAP_1UF,TY_CAP_22UF

Programmable Parts

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC:BLANK
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM:BLANK

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0681	138S0638		ALL	TAIYO YUDEN AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
353S2987	353S2988	HVDDLDO:FIXED	ALL	TPS71725 ALTERNATE FOR U2590
104S0023	104S0018		ALL	CYNTEC/DALE AS ALTERNATES
107S0139	107S0075		ALL	CYNTEC AS ALTERNATE
138S0671	138S0673		ALL	TAIYO AS ALTERNATE
155S0578	155S0367		ALL	TAIYO AS ALTERNATE
376S0926	376S0610		ALL	FAIRCHILD AS ALTERNATE
155S0457	155S0329		ALL	MAGLAYERS AS ALTERNATE
377S0107	377S0066		ALL	ON SEMI AS ALTERNATE

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3820	1	IC,MCP89U-A01,24.5MMX24.5MM,1244FCBGA	U1400	CRITICAL	MCP89U:A01
337S3868	1	IC,MCP89U-A02,24.5MMX24.5MM,1244FCBGA	U1400	CRITICAL	MCP89U:A02
337S3938	1	IC,MCP89U-A03,24.5MMX24.5MM,1244FCBGA	U1400	CRITICAL	MCP89U:A03
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0566	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,7.5X10.6	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,7.5X10.6	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,7.5X10.6	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:MICRON_4GB
353S2392	1	IC,ISL6259,BATCHARGER,4X4MM,QFN28	U7000	CRITICAL	ISL6259_SCREENED:NO
353S2929	1	IC,ISL6259,BATCHARGER,3%,4C4MM,QFN28	U7000	CRITICAL	ISL6259_SCREENED:YES

SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1070	PCBA,MLB,1.86GHZ HY 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWQ,CAPS:MU,DDR3:HYNIX_2GB
639-0837	PCBA,MLB,1.86GHZ,HY 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXW,CAPS:SS,DDR3:HYNIX_2GB
639-1096	PCBA,MLB,1.86GHZ HY 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXN,CAPS:TY,DDR3:HYNIX_2GB
639-1101	PCBA,MLB,1.86GHZ HY 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXV,CAPS:MU,DDR3:HYNIX_4GB
639-1098	PCBA,MLB,1.86GHZ HY 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXQ,CAPS:SS,DDR3:HYNIX_4GB
639-1068	PCBA,MLB,1.86GHZ HY 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWN,CAPS:TY,DDR3:HYNIX_4GB
639-1083	PCBA,MLB,1.86GHZ MI 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX6,CAPS:MU,DDR3:MICRON_2GB
639-1078	PCBA,MLB,1.86GHZ MI 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX1,CAPS:SS,DDR3:MICRON_2GB
639-1090	PCBA,MLB,1.86GHZ MI 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXG,CAPS:TY,DDR3:MICRON_2GB
639-1088	PCBA,MLB,1.86GHZ MI 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXD,CAPS:MU,DDR3:MICRON_4GB
639-1067	PCBA,MLB,1.86GHZ MI 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWM,CAPS:SS,DDR3:MICRON_4GB
639-1077	PCBA,MLB,1.86GHZ MI 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX0,CAPS:TY,DDR3:MICRON_4GB
639-1080	PCBA,MLB,1.86GHZ SA 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX3,CAPS:MU,DDR3:SAMSUNG_2GB
639-1095	PCBA,MLB,1.86GHZ SA 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXM,CAPS:SS,DDR3:SAMSUNG_2GB
639-1071	PCBA,MLB,1.86GHZ SA 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWR,CAPS:TY,DDR3:SAMSUNG_2GB
639-1097	PCBA,MLB,1.86GHZ SA 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXP,CAPS:MU,DDR3:SAMSUNG_4GB
639-1084	PCBA,MLB,1.86GHZ SA 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX7,CAPS:SS,DDR3:SAMSUNG_4GB
639-1091	PCBA,MLB,1.86GHZ SA 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXH,CAPS:TY,DDR3:SAMSUNG_4GB
639-1092	PCBA,MLB,2.13GHZ HY 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXJ,CAPS:MU,DDR3:HYNIX_2GB
639-1082	PCBA,MLB,2.13GHZ,HY 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX5,CAPS:SS,DDR3:HYNIX_2GB
639-1085	PCBA,MLB,2.13GHZ HY 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX8,CAPS:TY,DDR3:HYNIX_2GB
639-1089	PCBA,MLB,2.13GHZ HY 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXF,CAPS:MU,DDR3:HYNIX_4GB
639-1075	PCBA,MLB,2.13GHZ HY 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWX,CAPS:SS,DDR3:HYNIX_4GB
639-1079	PCBA,MLB,2.13GHZ HY 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX2,CAPS:TY,DDR3:HYNIX_4GB
639-1099	PCBA,MLB,2.13GHZ MI 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXR,CAPS:MU,DDR3:MICRON_2GB
639-1087	PCBA,MLB,2.13GHZ MI 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXC,CAPS:SS,DDR3:MICRON_2GB
639-1069	PCBA,MLB,2.13GHZ MI 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWP,CAPS:TY,DDR3:MICRON_2GB
639-1100	PCBA,MLB,2.13GHZ MI 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXT,CAPS:MU,DDR3:MICRON_4GB
639-1093	PCBA,MLB,2.13GHZ MI 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXK,CAPS:SS,DDR3:MICRON_4GB
639-1076	PCBA,MLB,2.13GHZ MI 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWY,CAPS:TY,DDR3:MICRON_4GB
639-1074	PCBA,MLB,2.13GHZ SA 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWW,CAPS:MU,DDR3:SAMSUNG_2GB
639-1072	PCBA,MLB,2.13GHZ SA 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWT,CAPS:SS,DDR3:SAMSUNG_2GB
639-1086	PCBA,MLB,2.13GHZ SA 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX9,CAPS:TY,DDR3:SAMSUNG_2GB
639-1073	PCBA,MLB,2.13GHZ SA 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWV,CAPS:MU,DDR3:SAMSUNG_4GB
639-1081	PCBA,MLB,2.13GHZ SA 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX4,CAPS:SS,DDR3:SAMSUNG_4GB
639-1094	PCBA,MLB,2.13GHZ SA 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXL,CAPS:TY,DDR3:SAMSUNG_4GB
639-1450	PCBA,MLB,1.86GHZ EL 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG4W,CAPS:MU,DDR3:ELPIDA_2GB
639-1451	PCBA,MLB,1.86GHZ EL 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG4Y,CAPS:SS,DDR3:ELPIDA_2GB
639-1455	PCBA,MLB,1.86GHZ EL 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG53,CAPS:TY,DDR3:ELPIDA_2GB
639-1453	PCBA,MLB,2.13GHZ EL 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG51,CAPS:MU,DDR3:ELPIDA_2GB
639-1454	PCBA,MLB,2.13GHZ EL 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG52,CAPS:SS,DDR3:ELPIDA_2GB
639-1452	PCBA,MLB,2.13GHZ EL 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG50,CAPS:TY,DDR3:ELPIDA_2GB
639-1458	PCBA,MLB,1.86GHZ EL 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG5P,CAPS:MU,DDR3:ELPIDA_4GB
639-1463	PCBA,MLB,1.86GHZ EL 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG5W,CAPS:SS,DDR3:ELPIDA_4GB
639-1460	PCBA,MLB,1.86GHZ EL 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG5T,CAPS:TY,DDR3:ELPIDA_4GB
639-1462	PCBA,MLB,2.13GHZ EL 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG5Q,CAPS:MU,DDR3:ELPIDA_4GB
639-1459	PCBA,MLB,2.13GHZ EL 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG5V,CAPS:SS,DDR3:ELPIDA_4GB
639-1461	PCBA,MLB,2.13GHZ EL 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG5R,CAPS:TY,DDR3:ELPIDA_4GB
607-6915	CMN PTS,PCBA,MLB,K16	K16_COMMON
085-1327	K16 MLB DEVELOPMENT BOM	K16_DEVEL:ENG

Bar Code Labels / EEE #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWM]	CRITICAL	EEEE:DCWM
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWN]	CRITICAL	EEEE:DCWN
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWP]	CRITICAL	EEEE:DCWP
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWQ]	CRITICAL	EEEE:DCWQ
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWR]	CRITICAL	EEEE:DCWR
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWT]	CRITICAL	EEEE:DCWT
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWV]	CRITICAL	EEEE:DCWV
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWW]	CRITICAL	EEEE:DCWW
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWX]	CRITICAL	EEEE:DCWX
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWY]	CRITICAL	EEEE:DCWY
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX0]	CRITICAL	EEEE:DCX0
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX1]	CRITICAL	EEEE:DCX1
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX2]	CRITICAL	EEEE:DCX2
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX3]	CRITICAL	EEEE:DCX3
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX4]	CRITICAL	EEEE:DCX4
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX5]	CRITICAL	EEEE:DCX5
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX6]	CRITICAL	EEEE:DCX6
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX7]	CRITICAL	EEEE:DCX7
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX8]	CRITICAL	EEEE:DCX8
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX9]	CRITICAL	EEEE:DCX9
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXC]	CRITICAL	EEEE:DCXC
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXD]	CRITICAL	EEEE:DCXD
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXF]	CRITICAL	EEEE:DCXF
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXG]	CRITICAL	EEEE:DCXG
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXH]	CRITICAL	EEEE:DCXH
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXJ]	CRITICAL	EEEE:DCXJ
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXK]	CRITICAL	EEEE:DCXK
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXL]	CRITICAL	EEEE:DCXL
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXM]	CRITICAL	EEEE:DCXM
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXN]	CRITICAL	EEEE:DCXN
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXP]	CRITICAL	EEEE:DCXP
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXQ]	CRITICAL	EEEE:DCXQ
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXR]	CRITICAL	EEEE:DCXR
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXT]	CRITICAL	EEEE:DCXT
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXV]	CRITICAL	EEEE:DCXV
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXW]	CRITICAL	EEEE:DCXW
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG4W]	CRITICAL	EEEE:DG4W
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG4Y]	CRITICAL	EEEE:DG4Y
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG53]	CRITICAL	EEEE:DG53
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG51]	CRITICAL	EEEE:DG51
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG52]	CRITICAL	EEEE:DG52
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG50]	CRITICAL	EEEE:DG50
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5P]	CRITICAL	EEEE:DG5P
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5W]	CRITICAL	EEEE:DG5W
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5T]	CRITICAL	EEEE:DG5T
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5Q]	CRITICAL	EEEE:DG5Q
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5V]	CRITICAL	EEEE:DG5V
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5R]	CRITICAL	EEEE:DG5R

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	1	CAP, 2.2UF, 6.3V, 20%, 0402	C4807	CRITICAL	SS_CAP_2_2UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0633	1	CAP, 2.2UF, 6.3V, 20%, 0402	C4807	CRITICAL	MU_CAP_2_2UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0634	1	CAP, 2.2UF, 6.3V, 20%, 0402	C4807	CRITICAL	TY_CAP_2_2UF

K16-Specific BOM Tables

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3751	1	PDC,SLGAB,PRQ,1.86,17W,1066,ED,6M,BGA	U1000	CRITICAL	CPU:1.86GHZ
337S3758	1	PDC,SLGEQ,PRQ,2.13,17W,1066,ED,6M,BGA	U1000	CRITICAL	CPU:2.13GHZ
341T0276	1	IC ASSY,SMC EXTERNAL,K16	U4900	CRITICAL	SMC:PROG
341T0275	1	IC ASSY,EFI UNLOCKED,K16	U6100	CRITICAL	BOOTROM:UNLOCKED
341S2785	1	IC EFI ROM,PVT,LOCKED,K16	U6100	CRITICAL	BOOTROM:LOCKED

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1327	1	K16 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-6915	1	CMN PTS,PCBA,MLB,K16	CMNPTS	CRITICAL	K16_CMNPTS

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: K16 BOM Variants

Apple Inc.

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REVISION: 3.3.0

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Revision History

Proto 0 (ECO #0000876215, v1.0.0, P4 change #210266, 03/16/2010)

v1.1.0 (P4 change #211399, 03/24/2010)

MCP:
7742015 - Added RC to DDC pass FETs to avoid glitch (pp. 7, 93).
7788138 - Added feedback divider and BOM tables for more HVDD LDOs (pp. 4, 25).
SMC:
7761747 - Added resistors to connect TCON to SMC or MCP SMBus (pp. 4, 52, 90).
7787883 - Added support for DP HPD wake / S4 state (pp. 4, 7, 8, 19, 49, 50, 78, 94).
SMS:
7765466 - Added S3 pull-up to SMS_INT_L to prevent leakage path (pp. 50, 59).
7769139 - Unstuffed SMS circuit (pg. 4).
General:
7787897 - Property/page fixes to reduce CheckPlus warnings/errors (pp. 7, 8, 12, 17, 74, 93, 108).

v1.2.0 (P4 change #211839, 03/26/2010)

USB:
7796626 - Changed port switch from TPS2052B to TPS2069 (pg. 46).
SMC:
7787883 - Added PLACE_NEAR property on R5022 to avoid stub (pg. 50).
SMBus:
7761747 - Added TCON I2C nets to FUNC_TEST list for J9000 (pg. 7).
Power:
7796648 - Changed DP and LCD power from PP3V3_S3 to PP3V3_S5 (pp. 8, 90).
7796658 - Changed backlight driver to E00 version (pg. 97).
BOM:
7796661 - Set up primary & alternate for power supply FET (pp. 4, 72).
7796654 - Consolidated SSM6N15FE to SSM6N37FE (pg. 48).
7796658 - Changed RCs on some SMC analog inputs (pg. 54).
7796683 - Stuffed RC on backlight driver PWM input (pg. 97).
General:
7796631 - Sorted BOM variants for easier verification (pg. 5).
7796631 - Cosmetic clean-up (pg. 76).

v1.3.0 (P4 change #212050, 03/26/2010)

SMBus:
7761747 - Added isolation FET and unstuffed series R's on TCON I2C for now (pp. 4, 90, 108).
Power Supply:
7796661 - Removed alternate FET, made some FETs primary to other APN (pp. 4, 72, 73, 76).
7798425 - R/C value changes for 3.42V G3Hot power supply (pg. 69).
7798399 - R/C value changes for 5V/3.3V power supply (pg. 72).
7800179 - R value changes for CPU VCore power supply (pg. 74).
7798445 - R value changes for 0.9V S5 power supply (pg. 77).
7796658 - Changed backlight driver back to non-E00 version (pp. 4, 97).
BOM:
7796658 - Added alternates for two caps per GSM and removed unused alternates (pg. 4).
7798399 - Consolidated 100pF caps (pp. 74, 75).

v1.4.0 (P4 change #212757, 03/31/2010)

MCP SPI:
7809733 - Changed strapping to select 62.5MHz SPI bus frequency (pg. 4).
SMBus:
7796631 - Added XDP connection to SMBus aliases page (pp. 13, 52).
7808530 - Changed SMC 'MGMT' SMBus pull-ups from 4.7K to 2K (pg. 52).
7761747 - Documented SMBus addresses for panel (pg. 52).
SD Card:
7800415 - Changed SD Card discharge R to more standard value (pg. 48).
Power Supplies:
7803283 - Changed 5V S3 regulator output from 5.02V to 5.12V nominal (pg. 72).
7809760 - Stuffed C9799 and clarified tables/BOMOPTIONs around these parts (pg. 97).

Proto 1 (ECO #0000884508, v2.0.0, P4 change #212783, 03/31/2010)

v2.1.0 (P4 change #??????, ??/??/2010)

BOM:
7796658 - Changed OMITs to OMIT_TABLEs (pp. 10-11, 14-20, 26, 31-36, 49, 61).

NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: Revision History

Apple Inc.

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Functional Test Points

J4001: AirPort / BT Connector

FUNC_TEST			
TRUE	PP3V3_WLAN_F	7 34 40	(Need 5 TPs)
TRUE	WIFI_EVENT_L	34 39 40	
TRUE	PCIE_AP_R2D_N	34 68	
TRUE	PCIE_AP_R2D_P	34 68	
TRUE	PCIE_CLK100M_AP_N	16 34 68	
TRUE	PCIE_CLK100M_AP_P	16 34 68	
TRUE	USB_BT_P	18 34 69	
TRUE	USB_BT_N	18 34 69	
TRUE	PCIE_AP_D2R_P	16 34 68	
TRUE	PCIE_AP_D2R_N	16 34 68	
TRUE	PCIE_WAKE_L	16 34	
TRUE	AP_RESET_CONN_L	34	
TRUE	AP_CLKREQ_Q_L	34	
TRUE	=PP3V3_S3_BT	8 34	

(Need to add 6 GND TPs)

J4501: SATA SSD Connector

FUNC_TEST			
TRUE	PP3V3_S0_HDD_R	7 35	(Need 5 TPs)
TRUE	SATA_HDD_D2R_C_P	35 68	
TRUE	SATA_HDD_D2R_C_N	35 68	
TRUE	SATA_HDD_R2D_N	35 68	
TRUE	SATA_HDD_R2D_P	35 68	
TRUE	SMC_HDD_OOB_TEMP	35 39	
TRUE	SMC_HDD_TEMP_CTL	35 39	

(Need to add 6 GND TPs)

J4700: LIO Connector

FUNC_TEST			
TRUE	=PP3V42_G3H_ONEWIRE	8 37	
TRUE	=PP3V3_S0_AUDIO	8 37	(Need 2 TPs)
TRUE	=PP1V8R1V5_S0_AUDIO	8 37	
TRUE	SYS_ONEWIRE	37 39	
TRUE	SMC_BC_ACOK	9 37 39 40	
TRUE	=USB_PWR_EN	36 37 58	
TRUE	SMC_LID	7 37 39 40 47	
TRUE	=I2C_LIO_SDA	37 42	
TRUE	=I2C_LIO_SCL	37 42	
TRUE	=I2C_MIKEY_SCL	37 42	
TRUE	=I2C_MIKEY_SDA	37 42	
TRUE	AUD_IPHS_SWITCH_EN	19 37	
TRUE	AUD_IP_PERIPHERAL_DET	17 37	
TRUE	AUD_I2C_INT_L	19 37	
TRUE	AUD_GPIO_3	37 49	
TRUE	SPKRAMP_INR_N	37 49 72	
TRUE	SPKRAMP_INR_P	37 49 72	
TRUE	USB_EXTD_N	18 37 69	
TRUE	USB_EXTD_P	18 37 69	
TRUE	USB_CAMERA_N	18 37 69	
TRUE	USB_CAMERA_P	18 37 69	
TRUE	HDA_SDOUT	19 37 69	
TRUE	HDA_BIT_CLK	19 37 69	
TRUE	HDA_SDIN0	19 37 69	
TRUE	USB_EXTD_OC_L	18 37	
TRUE	HDA_RST_L	19 37 69	
TRUE	HDA_SYNC	19 37 69	

(Need to add 5 GND TPs)

J4800: SD Card Connector

FUNC_TEST		
TRUE	PP3V3_SW_SD_PWR	38
TRUE	SD_CLK	38 70
TRUE	SD_CMD	38 70
TRUE	SD_D<7..0>	38 70
TRUE	SD_CD_L	38
TRUE	SD_WP	38

(Need to add 2 GND TPs)

J5100: LPC+SPI Connector

FUNC_TEST		
TRUE	=PP3V3_S5_LPCPLUS	8 41
TRUE	=PP5V_S0_LPCPLUS	8 41
TRUE	LPC_AD<3..0>	19 39 41 69
TRUE	SPI_ALT_MOSI	41 69
TRUE	SPI_ALT_MISO	41 69
TRUE	LPC_FRAME_L	19 39 41 69
TRUE	PM_CLKRUN_L	19 39 41
TRUE	SMC_TMS	39 40 41
TRUE	LPCPLUS_RESET_L	25 41
TRUE	SMC_TDO	39 40 41
TRUE	SMC_TRST_L	39 41
TRUE	SMC_MD1	39 41
TRUE	SMC_TX_L	36 39 40 41
TRUE	LPC_CLK33M_LPCPLUS	25 41 69
TRUE	SPIROM_USE_MLB	19 41 48
TRUE	SPI_ALT_CLK	41 69
TRUE	SPI_ALT_CS_L	41 69
TRUE	LPC_SERIRQ	19 39 41
TRUE	LPC_PWRDWN_L	19 39 41
TRUE	SMC_TDI	39 40 41
TRUE	SMC_TCK	39 40 41
TRUE	SMC_RESET_L	39 40 41 51
TRUE	SMC_NMI	39 41
TRUE	SMC_RX_L	36 39 40 41
TRUE	LPCPLUS_GPIO	19 41

(Need to add 6 GND TPs)

J5600: Fan Connector

FUNC_TEST		
TRUE	PP5V_S0	7 8 58
TRUE	FAN_RT_TACH	46
TRUE	FAN_RT_PWM	46

(Need to add 1 GND TP)

J5700: IPD Flex Connector

FUNC_TEST		
TRUE	=PP5V_S3_TPAD	8 57
TRUE	=PP3V42_G3H_TPAD	8 47
TRUE	=PP3V3_S3_TPAD	8 47
TRUE	USB_TPAD_CONN_P	47 72
TRUE	USB_TPAD_CONN_N	47 72
TRUE	=I2C_TPAD_SDA	42 47
TRUE	=I2C_TPAD_SCL	42 47
TRUE	SMC_ONOFF_L	39 40 47
TRUE	SMC_LID	7 37 39 40 47
TRUE	SMC_TPAD_RST_L	40 47

(Need to add 5 GND TPs)

J6900: DC-In Connector

FUNC_TEST			
TRUE	=PP18V5_DCIN_CONN	8 50	(Need 6 TPs)
TRUE	=PP5V_S3_LIO_CONN	8 50	

(Need to add 6 GND TPs)

J6903: Speaker Connector

FUNC_TEST		
TRUE	SPKRAMP_R_P_OUT	49 50
TRUE	SPKRAMP_R_N_OUT	49 50

J6950: Battery Connector

FUNC_TEST			
TRUE	PPVBAT_G3H_CONN	50 51	(Need 4 TPs)
TRUE	SMBUS_SMC_BSA_SCL	42 71	
TRUE	SMBUS_SMC_BSA_SDA	42 71	
TRUE	SYS_DETECT_L	50	

(Need to add 4 GND TPs near J6950 and 1 for shield)

J9000: Internal DP Connector

FUNC_TEST			
TRUE	PPVOUT_SW_LCDBKLT	7 43 60 63	(Need 2 TPs)
TRUE	PP3V3_SW_LCD	60	(Need 2 TPs)
TRUE	=I2C_TCON_SDA	42 60	
TRUE	LED_RETURN_6	60 63	
TRUE	LED_RETURN_5	60 63	
TRUE	LED_RETURN_4	60 63	
TRUE	LED_RETURN_3	60 63	
TRUE	LED_RETURN_2	60 63	
TRUE	LED_RETURN_1	60 63	
TRUE	DP_INT_HPD_CONN	60	
TRUE	DP_INT_AUX_CH_C_N	60 72	
TRUE	DP_INT_AUX_CH_C_P	60 72	
TRUE	DP_INT_ML_F_P<0>	60 72	
TRUE	DP_INT_ML_F_N<0>	60 72	
TRUE	DP_INT_ML_F_P<1>	60 72	
TRUE	DP_INT_ML_F_N<1>	60 72	
TRUE	=I2C_TCON_SCL	42 60	

(Need to add 5 GND TPs)

Misc Voltages & Control Signals

FUNC_TEST		
TRUE	PPVOUT_SW_LCDBKLT	7 43 60 63
TRUE	PPDCIN_S5_S5	8
TRUE	PPBUS_G3H	8 43 50
TRUE	PPBUS_G3H_ISNS	8
TRUE	PP5V_S3	8
TRUE	PP5V_S3_RTUSB_A_F	36
TRUE	PP5V_S0	7 8 58
TRUE	PP3V42_G3H	8
TRUE	PP3V3_S5	8 58 72
TRUE	PP3V3_SW_DPPWR	62
TRUE	PP3V3_S3	8
TRUE	PP3V3_WLAN_F	7 34 40
TRUE	PP3V3_S0	8 58 72
TRUE	PP3V3_S0_HDD_R	7 35
TRUE	PP3V3_ENET	8
TRUE	PP1V5R1V35_S3	8 72
TRUE	PP1V5_S0	8 58 72
TRUE	PP1V05_S0	8 58
TRUE	PP1V05_S0_MCP_PLL_UF	8
TRUE	PP0V9_S5	8
TRUE	PP0V9_ENET	8
TRUE	PPVCORE_S0_CPU	8 43
TRUE	PPVCORE_S0_MCP	8 43

(Need to add 27 GND TPs)

TRUE	SMC_PM_G2_EN	39 58
TRUE	PM_SLP_S4_L	19 39 58
TRUE	PM_SLP_S3_L	19 39 40 58

NO_TEST Nets

FSB Signals (Covered via CPU/MCP JTAG)

NO_TEST		
TRUE	FSB_A_L<35..3>	10 14 66
TRUE	FSB_ADS_L	10 14 66
TRUE	FSB_ADSTB_L<1..0>	10 14 66
TRUE	FSB_D_L<63..0>	10 14 66
TRUE	FSB_DINV_L<3..0>	10 14 66
TRUE	FSB_DSTB_L_N<3..0>	10 14 66
TRUE	FSB_DSTB_L_P<3..0>	10 14 66
TRUE	FSB_HIT_L	10 14 66
TRUE	FSB_HITM_L	10 14 66
TRUE	FSB_LOCK_L	10 14 66
TRUE	FSB_REQ_L<4..0>	10 14 66

SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/16/2010)

PAGE TITLE: Functional Test / No Test

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

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"G3Hot" (Always-Present) Rails

=PP18V5_DCIN_CONN → PPDCIN_S5_S5 (MIN_LINE_WIDTH=1mm, MIN_NECK_WIDTH=0.20mm, VOLTAGE=18.5V, MAKE_BASE=TRUE)
- =PPDCIN_S5_CHGR

=PPBUS_G3H → PPBUS_G3H (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0.4V, MAKE_BASE=TRUE)
- =PPBUS_G3H_R_IN
- =PPBUS_S0_LCDBKLT
- =PPVIN_S5_P5VP3V3
- =PPBUS_5V_S5

=PPBUS_G3H_R_OUT → PPBUS_G3H_ISNS (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=0.4V, MAKE_BASE=TRUE)
- =PPVIN_S5_CPU_IMVP
- =PPVIN_S3_DDRREG
- =PPVIN_S0_MCPCORE
- =PPVIN_S0_CPUVTTS0

=PP3V42_G3H_REG, 0.064 → PP3V42_G3H (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.42V, MAKE_BASE=TRUE)
- PP3V3_G3_RTC
- =PP3V42_G3H_SMCUSBMUX
- =PP3V42_G3H_ONEWIRE
- =PP3V42_G3H_SMBUS_SMC_BSA
- =PP3V42_G3H_BMON_ISNS
- =PP3V42_G3H_TPAD
- =PP3V42_G3H_CHGR
- =PP3V42_G3H_PWRCTL
- =PP3V3_S5_SMC
- =PP3V3_S5_LPCPLUS
- =PPVIN_S5_SMCVREF

"S5" Rails

=PP3V3_S5_REG, 1.07 A + S3 + S0 → PP3V3_S5 (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V, MAKE_BASE=TRUE)
- =PP3V3_S5_MCP_GPIO
- =PP3V3_S5_MCP
- =PP3V3_S5_MCPPWRGD
- =PP3V3_S5_SMBUS_SMC_MGMT
- =PP3V3_S5_ROM
- =PP3V3_S5_P0V9S5
- =PP3V3_S5_VMON
- =PP3V3_S5_P3V3S3FET
- =PP3V3_S5_P3V3ENETFET
- =PP3V3_S5_P3V3S0FET
- =PP3V3_S5_P0V9ENETFET
- =PP3V3_S5_DP_PORT_PWR
- =PP3V3_S0_LCD
- =PP3V3_S5_TPAD
- =PP3V3_SMC_PME

=PP0V9_S5_REG, 0.290 A → PP0V9_S5 (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0.9V, MAKE_BASE=TRUE)
- 105 mA/241 mA: =PP0V9_S5_MCP_VDD_AUXC
- =PP0V9_ENET_P0V9ENETFET

"S3" Rails

=PP3V3_S3_FET, 1.274 A → PP3V3_S3 (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=3.3V, MAKE_BASE=TRUE)
- =PP3V3_S3_MCP_GPIO
- =PP3V3_S3_VREFMRGN
- =PP3V3_S3_BT
- =PP3V3_S3_WLAN
- =PP3V3_S3_CARDREADER
- =PP3V3_S3_SMBUS_SMC_A_S3
- =PP3V3_S3_1V5S3ISNS
- =PP3V3_S3_WLANISNS
- =PP3V3_S3_TPAD
- =PP3V3_S3_SMS
- =PP3V3_S3_DBGLEDS
- =PP3V3_S3_PDCISENS

=PP5V_S3_REG, 5.40 A → PP5V_S3 (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V, MAKE_BASE=TRUE)
- =PP5V_S3_MCPDDRFET
- =PP5V_S3_RTUSB
- =PP5V_S3_SYSLED
- =PP5V_S3_TPAD
- =PP5V_S3_AUDIO_AMP
- =PP5V_S3_LIO_CONN
- =PP5V_S3_DDRREG
- =PP5V_S3_P5VS0FET

=PPDDR_S3_REG, 11.30 A → PP1V5R1V35_S3 (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.5V, MAKE_BASE=TRUE (OR 1.35V))
- =PP1V5R1V35_S3_MCP_MEM
- =PP1V5R1V35_S0_MCPDDRFET
- 0 mA: =PPLVDDR_S3_MEM_A
- 4250 mA: =PPLVDDR_S3_MEM_B
- =PPVIN_S0_DDRREG_LDO

=PPVTT_S3_DDR_BUF → PPDDRVREF_S3 (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0.75V, MAKE_BASE=TRUE (OR 0.675V))

"ENET" Rails

=PP3V3_ENET_FET_R, 300mA → PP3V3_ENET (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V, MAKE_BASE=TRUE)
- 300mA: =PP3V3_ENET_MCP_RMGT
- =PP3V3_ENET_MCP_PLL_MAC

=PP0V9_ENET_FET → PP0V9_ENET (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0.9V, MAKE_BASE=TRUE)
- =PP0V9_ENET_MCP_RMGT

"S0" Rails

=PP5V_S0_FET, 0.100 A → PP5V_S0 (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=5V, MAKE_BASE=TRUE)
- =PP5V_S0_MCPFSBFET
- =PP5V_S0_LPCPLUS
- =PP5V_S0_FAN
- =PP5V_S0_CPU_IMVP
- =PP5V_S0_MCPREG
- =PP5V_S0_CPUVTTS0
- =PP5V_S0_BKL
- =PP5VR3V3_S0_DPCADET

=PP3V3_S0_FET, 3.30 A → PP3V3_S0 (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V, MAKE_BASE=TRUE)
- =PP3V3_S0_XDP
- =PP3V3_S0_MCP_GPIO
- =PP3V3_S0_MCP_HVDD
- =PP3V3_S0_MCP
- =PP3V3_S0_MCP_PLL_UF
- =PP3V3_S0_HDD
- =PP3V3_S0_AUDIO
- =PP3V3_S0_SMC
- =PP3V3_S0_DEBUGROM
- =PP3V3_S0_SMBUS_MCP_0
- =PP3V3_S0_SMBUS_MCP_1
- =PP3V3_S0_SMBUS_SMC_B_S0
- =PP3V3_S0_SMBUS_SMC_0_S0
- =PP3V3_S0_BKLTISNS
- =PP3V3_S0_HDDISNS
- =PP3V3_S0_CSREGISNS
- =PP3V3_S0_MCPCOREISNS
- =PP3V3_S0_MCPDDRISNS
- =PP3V3_S0_CPUTHMSNS
- =PP3V3_S0_MCPTHMSNS
- =PP3V3_S0_FAN
- =PP3V3_S0_IMVP
- =PP3V3_S0_MCP_PLL_VLDO
- =PP3V3_S0_P1V5S0
- =PP3V3_S0_PWRCTL
- =PP3V3_S0_DPCONN
- =PP3V3_S0_BKL_VDDIO

=PP1V5_S0_REG, 0.210 A → PP1V5_S0 (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE)
- =PP1V5_S0_CPU
- =PP1V5_S0_MCP_PLL_VLDO
- =PP3V3R1V5_S0_MCP_HDA
- =PP1V8R1V5_S0_AUDIO

=PPCPUVTT_S0_REG, 9.40 A → PP1V05_S0 (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.05V, MAKE_BASE=TRUE)
- =PP1V05_S0_CPU
- =PP1V05_S0_XDP
- =PP1V05_S0_MCP_FSB
- =PP1V05_S0_MCP_M2CLK_DLL
- =PP1V05_S0_MCP_DP0_VDD
- =PP1V05_S0_MCP_PE_DVDD
- =PP1V05_S0_MCP_SATA_DVDD
- =PP1V05_S0_MCP_AVDD_UF
- =PP1V05_S0_MCP_PLL_UF_R
- =PP1V05_SW_MCP_FSB

=PP1V05_S0_MCP_PLL_OR → PP1V05_S0_MCP_PLL_UF (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.05V, MAKE_BASE=TRUE)
- =PP1V05_S0_MCP_PLL_UF

=PPVCORE_S0_CPU_REG, 18 A → PPVCORE_S0_CPU (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=1.65V, MAKE_BASE=TRUE)
- =PPVCORE_S0_CPU

=PPMCPCORE_S0_REG, 23.8 A → PPVCORE_S0_MCP (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE)
- =PPVCORE_S0_MCP
- =PPVCORE_S0_MCPGFXFET

=PPVTT_S0_DDR_LDO, 1.20 A → PPDDRVTT_S0 (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0.75V, MAKE_BASE=TRUE (OR 0.675V))
- =PPDDRVTT_S0_MEM_A
- =PPDDRVTT_S0_MEM_B

SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/11/2010)

PAGE TITLE: Power Aliases

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Plated Board Slot

SL0900
TH-NSP
SL-2.3X3.9-2.9X4.5

CPU Heat Sink Mounting Bosses

Z0913 STDOFF-4.5OD1.8H-SM
Z0910 STDOFF-4.5OD1.8H-SM
Z0911 STDOFF-4.5OD1.8H-SM
Z0912 STDOFF-4.5OD1.8H-SM
4x 860-1327

MCP Heat Sink Mounting Bosses

Z0906 STDOFF-4.5OD1.8H-SM
Z0909 STDOFF-4.5OD1.8H-SM
Z0908 STDOFF-4.5OD1.8H-SM
Z0907 STDOFF-4.5OD1.8H-SM
4x 860-1327

Fan Boss

Z0905
STDOFF-4.5OD1.8H-SM
860-1327

X21 Boss

Z0914
STDOFF-4.5OD1.9H-SM
860-1327

SSD Boss

Z0915
STDOFF-4.5OD1.9H-SM
860-1327

EMI I/O Pogo Pins

DisplayPort Pogo

CRITICAL
ZS0905
POGO-2.0OD-3.6H-K86-K87
SM
870-1938

USB/SD Card Pogo

CRITICAL
ZS0906
POGO-2.0OD-3.6H-K86-K87
SM
870-1938

DisplayPort PCB Stiffener

(Provides PCB support for small finger above J9400)

NO STUFF
MT0900
STIFFENER-K16-K99
SM-SP
806-1176

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.1 mm
MIN_LINE_WIDTH=0.5 mm

CPU Aliases

66 10 IN CPU_BSEL<0:2> = =MCP_BSEL<0:2> OUT 14
MAKE_BASE=TRUE
14 BI CPU_PECI_MCP = TP_CPU_PECI_MCP
MAKE_BASE=TRUE

DisplayPort Aliases

External DisplayPort Signals

68 17 IN DP_IG_ML0_P<0..3> = DP_EXT_ML_P<0..3> OUT 62 72
68 17 IN DP_IG_ML0_N<0..3> = DP_EXT_ML_N<0..3> OUT 62 72
MAKE_BASE=TRUE
68 17 BI DP_IG_AUX_CH0_P = DP_EXT_AUX_CH_P BI 61
68 17 BI DP_IG_AUX_CH0_N = DP_EXT_AUX_CH_N BI 61
17 OUT DP_IG_HPD0 = DP_EXT_HPD IN 62
61 OUT DP_CA_DET = DP_EXT_CA_DET IN 62
61 BI DP_AUX_CH_C_N = DP_EXT_AUX_CH_C_N BI 62 72
61 BI DP_AUX_CH_C_P = DP_EXT_AUX_CH_C_P BI 62 72

Internal DisplayPort Signals

68 17 IN DP_IG_ML1_P<0..1> = DP_INT_ML_P<0..1> OUT 60 72
68 17 IN DP_IG_ML1_N<0..1> = DP_INT_ML_N<0..1> OUT 60 72
68 17 BI DP_IG_AUX_CH1_P = DP_INT_AUX_CH_P BI 60 72
68 17 BI DP_IG_AUX_CH1_N = DP_INT_AUX_CH_N BI 60 72
17 OUT DP_IG_HPD1 = DP_INT_HPD IN 60
17 IN DP_IG_ML1_P<2..3> = TP_DP_INT_MLP<2..3>
17 IN DP_IG_ML1_N<2..3> = TP_DP_INT_MLN<2..3>
MAKE_BASE=TRUE
17 IN LCD_IG_BKLT_PWM = LCD_BKLT_PWM OUT 63
60 17 9 IN LCD_IG_PWR_EN = LCD_IG_PWR_EN OUT 9 17 60
17 IN LCD_IG_BKLT_EN = LCD_BKLT_EN OUT 64

Ethernet Aliases

16 OUT ENET_CLKREQ_L = NC_ENET_CLKREQ_L
MAKE_BASE=TRUE NO_TEST=TRUE

R0911
0
PP3V3_ENET_FET = 1 2 =PP3V3_ENET_FET_R OUT 8
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
59 =PP3V3_ENET_FET
5% 1/16W MF 402

ENET_RXD_PD
MAKE_BASE=TRUE
ENET_RXD<0> OUT 18 70
ENET_RXD<1> OUT 18 70
ENET_RXD<2> OUT 18 70
ENET_RXD<3> OUT 18 70
ENET_RXCLK_PD
MAKE_BASE=TRUE
ENET_CLK125M_RXCLK OUT 18 70
ENET_RX_CTRL OUT 18 70
ENET_MDIO BI 18 70
MCP_RGMII_VREF OUT 18
ENET_ENERGY_DET OUT 18

R0980 10K 5% 1/20W MF 201
R0981 10K 5% 1/20W MF 201
R0982 10K 5% 1/20W MF 201
R0983 10K 5% 1/20W MF 201
R0984 10K 5% 1/20W MF 201
R0985 10K 5% 1/20W MF 201

Charger Signal

51 IN =CHGR_ACOK = SMC_BC_ACOK OUT 7 37 39 40
MAKE_BASE=TRUE

MCPCOREISNS Signals

55 IN MCPCORES0_VO = =MCPCOREISNS_N OUT 44
MAKE_BASE=TRUE
55 IN MCPCORES0_ISP_R = =MCPCOREISNS_P OUT 44
MAKE_BASE=TRUE

LVDS Aliases

17 IN =MCP_IFPA_TXC_P = NC_LVDS_IG_A_CLKP
17 IN =MCP_IFPA_TXC_N = NC_LVDS_IG_A_CLKN
17 IN =MCP_IFPA_TXD_P<0..3> = NC_LVDS_IG_A_DATAP<0..3>
17 IN =MCP_IFPA_TXD_N<0..3> = NC_LVDS_IG_A_DATAN<0..3>
17 IN =MCP_IFPB_TXC_P = NC_LVDS_IG_B_CLKP
17 IN =MCP_IFPB_TXC_N = NC_LVDS_IG_B_CLKN
17 IN =MCP_IFPB_TXD_P<0..3> = NC_LVDS_IG_B_DATAP<0..3>
17 IN =MCP_IFPB_TXD_N<0..3> = NC_LVDS_IG_B_DATAN<0..3>
MAKE_BASE=TRUE NO_TEST=TRUE
17 IN =MCP_IFPAB_DDC_CLK = TP_LVDS_DDC_CLK
17 BI =MCP_IFPAB_DDC_DATA = TP_LVDS_DDC_DATA
MAKE_BASE=TRUE

PCI-E Aliases

Unused PCI-E Lanes

16 IN =PEG_R2D_C_N<5:4> = NC_PEG_R2DCN<5:4>
16 IN =PEG_R2D_C_P<5:4> = NC_PEG_R2DCP<5:4>
16 OUT =PEG_D2R_N<5:4> = NC_PEG_D2RN<5:4>
16 OUT =PEG_D2R_P<5:4> = NC_PEG_D2RP<5:4>
MAKE_BASE=TRUE NO_TEST=TRUE
68 16 IN PEG_CLK100M_P = NC_PEG_CLK100MP
68 16 IN PEG_CLK100M_N = NC_PEG_CLK100MN
MAKE_BASE=TRUE NO_TEST=TRUE
16 OUT PEG_CLKREQ_L = NC_PEG_CLKREQ_L
MAKE_BASE=TRUE NO_TEST=TRUE

SATA Aliases

Unused SATA ODD Signals

68 18 IN SATA_ODD_R2D_C_P = NC_SATA_ODD_R2DCP
68 18 IN SATA_ODD_R2D_C_N = NC_SATA_ODD_R2DCN
68 18 OUT SATA_ODD_D2R_P = NC_SATA_ODD_D2RP
68 18 OUT SATA_ODD_D2R_N = NC_SATA_ODD_D2RN
MAKE_BASE=TRUE NO_TEST=TRUE

USB Aliases

Unused USB Ports

69 18 BI USB_MINI_P = NC_USB_MINIP
69 18 BI USB_MINI_N = NC_USB_MININ
69 18 BI USB_EXTC_P = NC_USB_EXTCP
69 18 BI USB_EXTC_N = NC_USB_EXTCN
MAKE_BASE=TRUE NO_TEST=TRUE

Misc MCP89 Aliases

17 TP_MCP_RGB_DAC_VREF = NC_MCP_RGB_DAC_VREF
MAKE_BASE=TRUE NO_TEST=TRUE
67 15 IN MEM_A_CLK_P<1> = TP_MEM_A_CLKP<1>
67 15 IN MEM_A_CLK_N<1> = TP_MEM_A_CLKN<1>
67 15 IN MEM_B_CLK_P<1> = TP_MEM_B_CLKP<1>
67 15 IN MEM_B_CLK_N<1> = TP_MEM_B_CLKN<1>
MAKE_BASE=TRUE
67 15 IN MEM_A_A<15> = TP_MEM_A_A<15>
67 15 IN MEM_B_A<15> = TP_MEM_B_A<15>
MAKE_BASE=TRUE
10 IN MCP_MEM_VDD_SEL_1V5 = TP_MEM_VDD_SEL_1V5
MAKE_BASE=TRUE

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
PAGE TITLE
Signal Aliases

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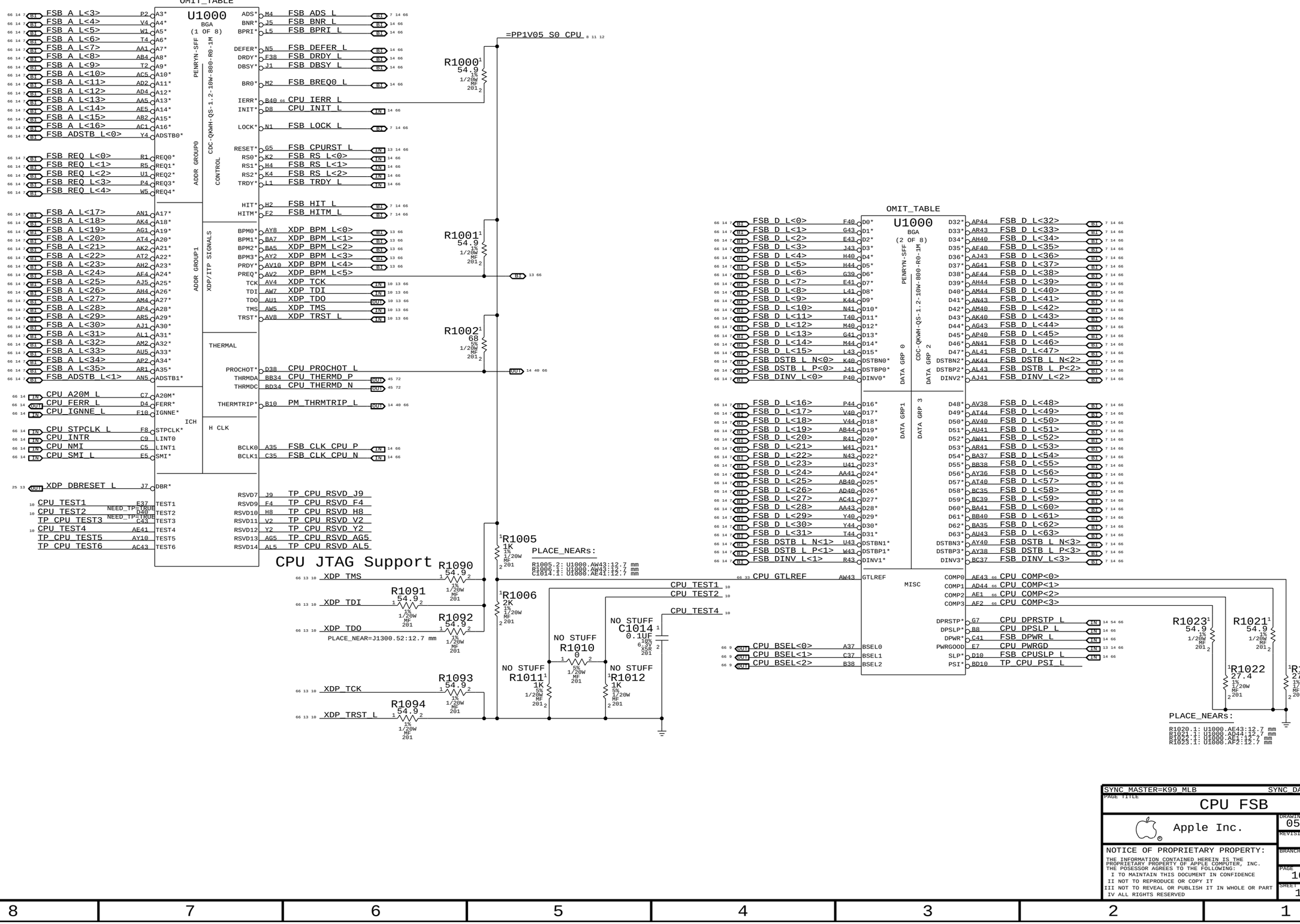

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: CPU FSB

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(CPU CORE POWER)
=PPVCORE_S0_CPU 8 11 12 65

18 A (CULV Design Target)
17.6 A (CULV ICC_Max)

OMIT_TABLE

U1000
BGA
(7 OF 8)
PENRYN-SFF
CDC-QKWH-QS-1.2-10W-800-R0-1M

BD30	K20	H32	AD28
BB28	M16	G33	AD30
BB30	M18	F32	AB28
B24	K16	N33	AB30
B22	K18	M32	Y28
H22	V20	L33	Y30
H24	T20	K32	AK26
F22	P20	J33	AH26
F24	V16	W33	AF26
D24	V18	V32	AK28
D22	T16	U33	AK30
M22	T18	T32	AH28
M24	P16	R33	AH30
K22	P18	P32	AF28
K24	AD20	AD32	AF30
V22	AB20	AC33	AP26
V24	Y20	AB32	AM26
T22	AD16	AA33	AP28
T24	AD18	Y32	AP30
P22	AB16	AK32	AM28
P24	AB18	AJ33	AM30
AD22	Y16	AH32	AY26
AD24	Y18	AG33	AV26
AB22	AK20	AF32	AT26
AB24	AK16	AE33	AY28
Y22	AK18	AR33	AY30
Y24	AH20	AP32	AV28
AK22	AF20	AN33	AV30
AK24	AH16	AM32	AT28
AH22	AH18	AL33	AT30
AH24	AF16	AY32	BD26
AF22	AF18	AV32	BB26
AF24	AP20	AU33	BD28
AP22	AM20	AT32	
AP24	AP16	AT34	
AM22	AP18	BD32	
AM24	AM16	BB32	
AY22	AM18	B26	
AY24	AY20	B30	
AV22	AV20	B28	
AV24	AT20	H26	
AT22	AY16	F26	
AT24	AY18	D26	
BD22	AV16	H28	
BD24	AV18	H30	
BB22	AT16	F28	
BB24	AT18	F30	
B20	BD20	D30	
B18	BB20	D28	
B16	BD16	M26	
H20	BD18	K26	
F20	BB16	M28	
D20	BB18	M30	
H16	AP14	K28	
H18	AM14	K30	
F16	AY14	V26	
F18	AV14	T26	
D18	AT14	P26	
D16	BD14	V28	
M20	BB14	V30	
		T28	
		T30	
		P28	
		P30	
		AD26	
		AB26	
		Y26	

VCC

(CPU IO POWER 1.05V)
=PP1V05_S0_CPU 8 10 11 12

4500 mA (before VCC stable)
2500 mA (after VCC stable)

N37	
L37	
K38	
J37	
W37	
V38	
U37	
R37	
P38	
AC37	
AB38	
AA37	
AK38	
AJ37	
AG37	
AE38	

VCCP

(CPU INTERNAL PLL POWER 1.5V)
=PP1V5_S0_CPU 8 12

130 mA

B34	
D34	

VCCA

BD8	CPU_VID<0>	OUT 12 54 66
BC7	CPU_VID<1>	OUT 12 54 66
BB10	CPU_VID<2>	OUT 12 54 66
BB8	CPU_VID<3>	OUT 12 54 66
BC5	CPU_VID<4>	OUT 12 54 66
BB4	CPU_VID<5>	OUT 12 54 66
AY4	CPU_VID<6>	OUT 12 54 66

VID

=PPVCORE_S0_CPU 8 11 12 65

R1100
100
1%
1/20W
MF
201
2
PLACE_NEAR=U1000.BD12:25.4 mm

BD12	CPU_VCCSENSE_P	OUT 54 66
BC13	CPU_VCCSENSE_N	OUT 54 66

VCCSENSE
VSSSENSE

PLACE_NEAR=U1000.BC13:25.4 mm

R1101
100
1%
1/20W
MF
201
2

=PP1V05_S0_CPU 8 10 11 12

OMIT_TABLE

U1000
BGA
(8 OF 8)
PENRYN-SFF
CDC-QKWH-QS-1.2-10W-800-R0-1M

AE37	R13
AP38	P12
AN37	P14
AL37	AB10
C33	AD14
B32	AC11
H36	AC13
F36	AB12
G35	AB14
F34	AA11
E33	AA13
E35	Y14
D32	AK10
K36	AF10
N35	AK12
L35	AK14
J35	AJ11
W35	AJ13
V36	AH14
P36	AG11
U35	AG13
R35	AF12
AB36	AF14
AC35	AE11
AA35	AE13
AK36	AP10
AF36	AR11
AJ35	AR13
AG35	AP12
AE35	AN11
AP36	AN13
AN35	AL11
AL35	AL13
C13	AU11
B14	AU13
B12	N7
H12	N9
H14	L7
G11	L9
G13	W7
F12	W9
F14	U7
E11	U9
E13	R7
D14	R9
D12	AC7
K10	AC9
N11	AA7
N13	AA9
M14	AJ7
L11	AJ9
L13	AG7
K12	AG9
K14	AE7
J11	AE9
J13	AR7
V10	AR9
P10	AN7
W11	AN9
W13	AL7
V12	AL9
V14	A33
U11	A13
U13	
T14	
R11	

VCCP

OMIT_TABLE

U1000
BGA
(4 OF 8)
PENRYN-SFF
CDC-QKWH-QS-1.2-10W-800-R0-1M

B42	AP34
H42	AM34
F42	AV36
D42	AT36
D44	AY34
F44	AW33
M42	AW35
K42	AV34
V42	AU35
T42	BD36
P42	BB36
AD42	BC33
AB42	BA33
Y42	C31
AK42	C29
AH42	C27
AF42	G31
AP42	E31
AM42	G27
AY42	G29
AV42	E27
AT42	E29
AV44	N31
AY44	L31
BB42	J31
BA43	N27
C39	N29
H38	L27
G37	L29
E39	J27
N39	J29
M38	W31
L39	W27
J39	W29
W39	U31
U39	R31
T38	U27
R39	U29
AD38	R27
AC39	R29
AA39	AC31
Y38	AA31
AJ39	AC27
AH38	AC29
AG39	AA27
AE39	AA29
AR37	AJ31
AR39	AG31
AN39	AE31
AM38	AJ27
AL39	AJ29
AW37	AG27
AW39	AG29
AU37	AE27
AU39	AE29
AT38	AR31
BD38	AR27
BD40	AR29
BC41	AN31
BA39	AL31
B36	AN27
D36	AN29
H34	AL27
M36	AL29
M34	AW31
K34	AU31
T36	AW27
V34	AW29
T34	AU27
P34	AU29
AD36	BC31
Y36	BA31
AD34	BC27
AB34	BC29
Y34	BA27
AK34	BA29
AH36	C25
AH34	C23
AF34	C21
AR35	G21
AM36	G23
	G25

VSS

OMIT_TABLE

U1000
BGA
(5 OF 8)
PENRYN-SFF
CDC-QKWH-QS-1.2-10W-800-R0-1M

E21	AE17
E23	AE19
E25	AR17
N21	AR19
N23	AN17
N25	AN19
L21	AL17
L23	AL19
L25	AW17
J21	AW19
J23	AU17
J25	AU19
W21	BC17
W23	BC19
W25	BA17
U21	BA19
U23	C15
U25	C11
R21	H10
R23	G15
R25	E15
AC21	M10
AC23	N15
AC25	L15
AA21	J15
AA23	M12
AA25	T10
AJ21	W15
AJ23	U15
AJ25	R15
AG21	T12
AG23	AD10
AG25	Y10
AE21	AC15
AE23	AA15
AE25	AD12
AR21	Y12
AR23	AH10
AR25	AJ15
AN21	AG15
AN23	AE15
AN25	AH12
AL21	AM10
AL23	AR15
AL25	AN15
AW21	AL15
AW23	AM12
AW25	AT10
AU21	AW15
AU23	AU15
AU25	AY12
BC21	AW11
BC23	AW13
BC25	AV12
BA21	AT12
BA23	BC15
BA25	BA15
C19	BC11
C17	
G17	BB12
G19	BA11
E17	BA13
E19	B6
N17	H6
N19	G9
L17	F6
L19	E9
J17	D6
J19	M6
W17	M8
W19	K6
U17	K8
U19	U5
R17	V6
R19	V8
AC17	T6
AC19	T8
AA17	P6
AA19	P8
AJ17	AD6
AJ19	AD8
AG17	AB6
AG19	AB8

VSS

OMIT_TABLE

U1000
BGA
(6 OF 8)
PENRYN-SFF
CDC-QKWH-QS-1.2-10W-800-R0-1M

Y6	AJ3
Y8	AG3
AK6	AE3
AK8	AR3
AH6	AN3
AH8	AL3
AF6	AW3
AF8	AU3
AP6	BD4
AP8	BC3
AM6	BB2
AM8	BA3
AY6	G1
AW9	E1
AU7	AW1
AV6	BA1
AU9	A39
AT6	A41
AT8	A31
BD6	A27
BC9	A29
BB6	A21
BA9	A23
C3	A25
B4	A17
G3	A19
E3	A15
D2	A11
N3	A9
L3	A5
J3	A7
W3	
U3	
R3	
AC3	
AA3	

VSS

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
CPU Power & Ground

Apple Inc.

DRAWING NUMBER 051-8467
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CPU VCORE HF AND BULK DECOUPLING

4x 270uF. 32x 10uF 0603, 28x 2.2uF 0402 + 40x 2.2uF 0402

65 11 8 =PPVCORE_S0_CPU

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL NO STUFF C1200 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1201 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1202 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1203 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1204 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1205 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1206 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1207 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1208 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1209 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1210 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1211 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1212 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1213 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1214 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1215 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1216 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1217 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1218 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1219 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL NO STUFF C1220 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1221 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1222 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1223 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1224 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1225 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1226 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1227 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1228 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1229 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1230 10UF 20% 6.3V X5R 603
CRITICAL NO STUFF C1231 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1240 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1241 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1242 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1243 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1244 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1245 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1246 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1247 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1248 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1249 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1250 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1251 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1252 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1253 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1254 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1255 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1256 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1257 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1258 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1259 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1260 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1261 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1262 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1263 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1264 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1265 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1266 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1267 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU

CRITICAL C1270 270UF 20% 2V TANT CASE-B4-SM
CRITICAL C1271 270UF 20% 2V TANT CASE-B4-SM
CRITICAL C1272 270UF 20% 2V TANT CASE-B4-SM
CRITICAL C1273 270UF 20% 2V TANT CASE-B4-SM

CPU VCORE VID CONNECTIONS

66 54 11 IN CPU_VID<0..6> = IMVP6_VID<0..6> OUT 66
MAKE_BASE=TRUE

VCCA (CPU AVdd) DECOUPLING

11 8 =PP1V5_S0_CPU 1x 10uF, 1x 0.01uF

OMIT_TABLE C1280 10UF 20% 6.3V X5R 603
C1281 0.01UF 10% 16V X5R 201

LAYOUT NOTE:
PLACE C1281 NEAR PIN B34 OF U1000

VCCP (CPU I/O) DECOUPLING

11 10 8 =PP1V05_S0_CPU 1x 270uF, 12x 2.2uF

OMIT_TABLE C1283 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1284 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1285 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1286 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1287 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1288 2.2UF 20% 6.3V CERM 402-LF

CRITICAL C1290 270UF 20% 2V TANT CASE-B4-SM
OMIT_TABLE C1291 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1292 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1293 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1294 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1295 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1296 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE C1290 CLOSE TO CPU
PLACE C1283-C1288 CLOSE TO FSB ADDRESS PINS
PLACE C1291-C1296 CLOSE TO FSB DATA PINS

SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/11/2010)

PAGE TITLE
CPU Decoupling & VID

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
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BRANCH
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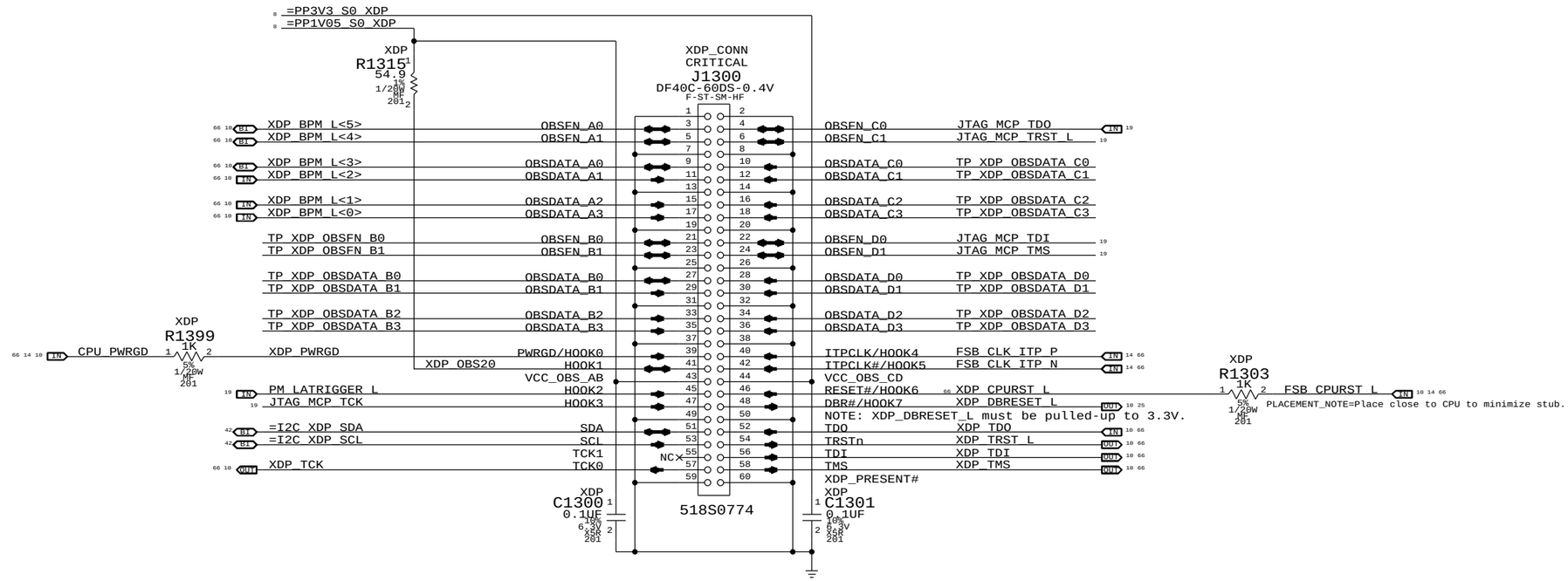
Micro2-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0782 Adapter Flex to support chipset debug.



Direction of XDP adapter flex

Please place J1300 within 1" of
board edge with odd-numbered pins
facing edge. Avoid any tall
components between J1300 and edge.

SYNC_MASTER=K99_MLB SYNC_DATE=03/01/2010

PAGE TITLE
eXtended Debug Port (Micro-XDP)

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
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OMIT_TABLE

U1400
MCP89U-A01
BGA
SYMBOL 1 OF 11

FSB

FSB_DSTB_L_P<0>	J38	CPU_DSTBP0*	CPU_D0*	M37	FSB_D_L<0>	
FSB_DSTB_L_N<0>	J39	CPU_DSTBN0*	CPU_D1*	M39	FSB_D_L<1>	
FSB_DINV_L<0>	F39	CPU_DBI0*	CPU_D2*	P39	FSB_D_L<2>	
			CPU_D3*	L38	FSB_D_L<3>	
FSB_DSTB_L_P<1>	R34	CPU_DSTBP1*	CPU_D4*	L39	FSB_D_L<4>	
FSB_DSTB_L_N<1>	R35	CPU_DSTBN1*	CPU_D5*	L40	FSB_D_L<5>	
FSB_DINV_L<1>	U36	CPU_DBI1*	CPU_D6*	M40	FSB_D_L<6>	
			CPU_D7*	P40	FSB_D_L<7>	
FSB_DSTB_L_P<2>	J37	CPU_DSTBP2*	CPU_D8*	H40	FSB_D_L<8>	
FSB_DSTB_L_N<2>	J36	CPU_DSTBN2*	CPU_D9*	L37	FSB_D_L<9>	
FSB_DINV_L<2>	L35	CPU_DBI2*	CPU_D10*	F38	FSB_D_L<10>	
			CPU_D11*	F40	FSB_D_L<11>	
FSB_DSTB_L_P<3>	C37	CPU_DSTBP3*	CPU_D12*	H38	FSB_D_L<12>	
FSB_DSTB_L_N<3>	C38	CPU_DSTBN3*	CPU_D13*	M38	FSB_D_L<13>	
FSB_DINV_L<3>	B35	CPU_DBI3*	CPU_D14*	H39	FSB_D_L<14>	
			CPU_D15*	J40	FSB_D_L<15>	
FSB_A_L<3>	U38	CPU_A3*	CPU_D16*	U35	FSB_D_L<16>	
FSB_A_L<4>	V37	CPU_A4*	CPU_D17*	R36	FSB_D_L<17>	
FSB_A_L<5>	Y36	CPU_A5*	CPU_D18*	R37	FSB_D_L<18>	
FSB_A_L<6>	V40	CPU_A6*	CPU_D19*	P35	FSB_D_L<19>	
FSB_A_L<7>	Y39	CPU_A7*	CPU_D20*	R38	FSB_D_L<20>	
FSB_A_L<8>	Y40	CPU_A8*	CPU_D21*	R33	FSB_D_L<21>	
FSB_A_L<9>	V39	CPU_A9*	CPU_D22*	U34	FSB_D_L<22>	
FSB_A_L<10>	AA39	CPU_A10*	CPU_D23*	R40	FSB_D_L<23>	
FSB_A_L<11>	AA36	CPU_A11*	CPU_D24*	P34	FSB_D_L<24>	
FSB_A_L<12>	AA37	CPU_A12*	CPU_D25*	P37	FSB_D_L<25>	
FSB_A_L<13>	Y38	CPU_A13*	CPU_D26*	P38	FSB_D_L<26>	
FSB_A_L<14>	AC36	CPU_A14*	CPU_D27*	P36	FSB_D_L<27>	
FSB_A_L<15>	AA40	CPU_A15*	CPU_D28*	P33	FSB_D_L<28>	
FSB_A_L<16>	AA38	CPU_A16*	CPU_D29*	P32	FSB_D_L<29>	
FSB_A_L<17>	AF39	CPU_A17*	CPU_D30*	R32	FSB_D_L<30>	
FSB_A_L<18>	AD38	CPU_A18*	CPU_D31*	R39	FSB_D_L<31>	
FSB_A_L<19>	AC38	CPU_A19*	CPU_D32*	H36	FSB_D_L<32>	
FSB_A_L<20>	AJ38	CPU_A20*	CPU_D33*	F36	FSB_D_L<33>	
FSB_A_L<21>	AD37	CPU_A21*	CPU_D34*	L33	FSB_D_L<34>	
FSB_A_L<22>	AJ39	CPU_A22*	CPU_D35*	M35	FSB_D_L<35>	
FSB_A_L<23>	AC40	CPU_A23*	CPU_D36*	L34	FSB_D_L<36>	
FSB_A_L<24>	AC37	CPU_A24*	CPU_D37*	M33	FSB_D_L<37>	
FSB_A_L<25>	AD40	CPU_A25*	CPU_D38*	M36	FSB_D_L<38>	
FSB_A_L<26>	AC39	CPU_A26*	CPU_D39*	M32	FSB_D_L<39>	
FSB_A_L<27>	AF36	CPU_A27*	CPU_D40*	J34	FSB_D_L<40>	
FSB_A_L<28>	AF40	CPU_A28*	CPU_D41*	H35	FSB_D_L<41>	
FSB_A_L<29>	AG39	CPU_A29*	CPU_D42*	H34	FSB_D_L<42>	
FSB_A_L<30>	AD39	CPU_A30*	CPU_D43*	L36	FSB_D_L<43>	
FSB_A_L<31>	AD36	CPU_A31*	CPU_D44*	M34	FSB_D_L<44>	
FSB_A_L<32>	AF37	CPU_A32*	CPU_D45*	F37	FSB_D_L<45>	
FSB_A_L<33>	AJ40	CPU_A33*	CPU_D46*	H37	FSB_D_L<46>	
FSB_A_L<34>	AG40	CPU_A34*	CPU_D47*	J35	FSB_D_L<47>	
FSB_A_L<35>	AG38	CPU_A35*	CPU_D48*	D39	FSB_D_L<48>	
			CPU_D49*	E36	FSB_D_L<49>	
FSB_ADSTB_L<0>	Y37	CPU_ADSTB0*	CPU_D50*	D40	FSB_D_L<50>	
FSB_ADSTB_L<1>	AF38	CPU_ADSTB1*	CPU_D51*	E40	FSB_D_L<51>	
			CPU_D52*	C39	FSB_D_L<52>	
FSB_REQ_L<0>	U40	CPU_REQ0*	CPU_D53*	E38	FSB_D_L<53>	
FSB_REQ_L<1>	U39	CPU_REQ1*	CPU_D54*	A37	FSB_D_L<54>	
FSB_REQ_L<2>	V38	CPU_REQ2*	CPU_D55*	C36	FSB_D_L<55>	
FSB_REQ_L<3>	U37	CPU_REQ3*	CPU_D56*	B38	FSB_D_L<56>	
FSB_REQ_L<4>	V36	CPU_REQ4*	CPU_D57*	E37	FSB_D_L<57>	
			CPU_D58*	C35	FSB_D_L<58>	
FSB_ADS_L	AG33	CPU_ADS*	CPU_D59*	A35	FSB_D_L<59>	
FSB_BNR_L	AD35	CPU_BNR*	CPU_D60*	B37	FSB_D_L<60>	
FSB_BREQ0_L	AG34	CPU_BR0*	CPU_D61*	D36	FSB_D_L<61>	
FSB_DBSY_L	AF35	CPU_DBSY*	CPU_D62*	A36	FSB_D_L<62>	
FSB_DRDY_L	U32	CPU_DRDY*	CPU_D63*	D38	FSB_D_L<63>	
FSB_HIT_L	AD34	CPU_HIT*				
FSB_HITM_L	AD32	CPU_HITM*				
FSB_LOCK_L	AG37	CPU_LOCK*				
FSB_TRDY_L	AG32	CPU_TRDY*				
			CPU_BPRI*	AF32	FSB_BPRI_L	
CPU_PECI_MCP	AG36	CPU_PECI	CPU_DEFER*	AG35	FSB_DEFER_L	
CPU_PROCHOT_L	V32	CPU_PROCHOT*				
	V35	CPU_THERMTRIP*	BCLK_OUT_CPU_P	AJ37	FSB_CLK_CPU_P	
	AC33	CPU_FERR*	BCLK_OUT_CPU_N	AJ36	FSB_CLK_CPU_N	
			BCLK_OUT_ITP_P	AK32	FSB_CLK_ITP_P	
=MCP_BSEL<2>	D35	CPU_BSEL2	BCLK_OUT_ITP_N	AK33	FSB_CLK_ITP_N	
=MCP_BSEL<1>	E35	CPU_BSEL1	BCLK_OUT_NB_P	AJ35	FSB_CLK_MCP_P	
=MCP_BSEL<0>	F35	CPU_BSEL0	BCLK_OUT_NB_N	AJ34	FSB_CLK_MCP_N	
FSB_RS_L<0>	AF33	CPU_RS0*	BCLK_IN_N	AJ32		
FSB_RS_L<1>	AD33	CPU_RS1*	BCLK_IN_P	AJ33		
FSB_RS_L<2>	AF34	CPU_RS2*				
			CPU_A20M*	AA33	CPU_A20M_L	
MCP_BCLK_VML_COMP_VDD	AK39	BCLK_VML_COMP_VDD	CPU_IGNNE*	V33	CPU_IGNNE_L	
MCP_BCLK_VML_COMP_GND	AK40	BCLK_VML_COMP_GND	CPU_INIT*	Y33	CPU_INIT_L	
			CPU_INTR	Y35	CPU_INTR	
MCP_CPU_COMP_VCC	AK38	CPU_COMP_VCC	CPU_NMI	AA35	CPU_NMI	
MCP_CPU_COMP_GND	AK37	CPU_COMP_GND	CPU_SMI*	AC35	CPU_SMI_L	
			CPU_PWRGD	AA32	CPU_PWRGD	
			CPU_RESET*	AC34	FSB_CPURST_L	
			CPU_DPRSLPVR	D2	PM_DPRSLPVR	
			CPU_SLP*	V34	FSB_CPUSLP_L	
			CPU_DPSLP*	Y32	CPU_DPSLP_L	
			CPU_DPWR*	U33	FSB_DPWR_L	
			CPU_STPCLK*	Y34	CPU_STPCLK_L	
			CPU_DPRSTP*	AA34	CPU_DPRSTP_L	

=PP1V05_S0_MCP_FSB

R1410 54.9 1% 1/20W MF 201

R1415 62 5% 1/20W MF 201

PM_THRMTRIP_L
CPU_FERR_L

R1430 49.9 1% 1/20W MF 201

R1435 49.9 1% 1/20W MF 201

R1431 49.9 1% 1/20W MF 201

R1436 49.9 1% 1/20W MF 201

Loop-back clock for delay matching.

=PP1V05_S0_MCP_FSB
NO STUFF
R1440 150 5% 1/20W MF 201

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
MCP CPU Interface

Apple Inc.

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MEMORY PARTITION 0

MEM_A_DQ<63>	AN6	MDQ0_63	MDQS0_7_P	AR4	MEM_A_DQS_P<7>
MEM_A_DQ<62>	AN4	MDQ0_62	MDQS0_7_N	AR5	MEM_A_DQS_N<7>
MEM_A_DQ<61>	AT4	MDQ0_61	MDQS0_6_P	AT6	MEM_A_DQS_P<6>
MEM_A_DQ<60>	AU3	MDQ0_60	MDQS0_6_N	AU6	MEM_A_DQS_N<6>
MEM_A_DQ<59>	AM7	MDQ0_59	MDQS0_5_P	AN11	MEM_A_DQS_P<5>
MEM_A_DQ<58>	AN7	MDQ0_58	MDQS0_5_N	AM11	MEM_A_DQS_N<5>
MEM_A_DQ<57>	AT5	MDQ0_57	MDQS0_4_P	AT12	MEM_A_DQS_P<4>
MEM_A_DQ<56>	AT3	MDQ0_56	MDQS0_4_N	AR12	MEM_A_DQS_N<4>
MEM_A_DQ<55>	AU5	MDQ0_55	MDQS0_3_P	AR29	MEM_A_DQS_P<3>
MEM_A_DQ<54>	AV5	MDQ0_54	MDQS0_3_N	AP29	MEM_A_DQS_N<3>
MEM_A_DQ<53>	AR6	MDQ0_53	MDQS0_2_P	AR32	MEM_A_DQS_P<2>
MEM_A_DQ<52>	AN9	MDQ0_52	MDQS0_2_N	AP32	MEM_A_DQS_N<2>
MEM_A_DQ<51>	AV3	MDQ0_51	MDQS0_1_P	AV36	MEM_A_DQS_P<1>
MEM_A_DQ<50>	AV4	MDQ0_50	MDQS0_1_N	AU36	MEM_A_DQS_N<1>
MEM_A_DQ<49>	AM8	MDQ0_49	MDQS0_0_P	AN35	MEM_A_DQS_P<0>
MEM_A_DQ<48>	AN8	MDQ0_48	MDQS0_0_N	AN34	MEM_A_DQS_N<0>
MEM_A_DQ<47>	AP8	MDQ0_47			
MEM_A_DQ<46>	AP9	MDQ0_46			
MEM_A_DQ<45>	AN12	MDQ0_45			
MEM_A_DQ<44>	AT11	MDQ0_44			
MEM_A_DQ<43>	AT8	MDQ0_43			
MEM_A_DQ<42>	AR8	MDQ0_42			
MEM_A_DQ<41>	AT9	MDQ0_41			
MEM_A_DQ<40>	AM12	MDQ0_40			
MEM_A_DQ<39>	AP12	MDQ0_39			
MEM_A_DQ<38>	AN14	MDQ0_38			
MEM_A_DQ<37>	AT14	MDQ0_37			
MEM_A_DQ<36>	AR14	MDQ0_36			
MEM_A_DQ<35>	AR11	MDQ0_35			
MEM_A_DQ<34>	AP11	MDQ0_34			
MEM_A_DQ<33>	AM15	MDQ0_33			
MEM_A_DQ<32>	AN15	MDQ0_32			
MEM_A_DQ<31>	AR27	MDQ0_31			
MEM_A_DQ<30>	AT27	MDQ0_30			
MEM_A_DQ<29>	AM30	MDQ0_29			
MEM_A_DQ<28>	AN30	MDQ0_28			
MEM_A_DQ<27>	AN27	MDQ0_27			
MEM_A_DQ<26>	AP27	MDQ0_26			
MEM_A_DQ<25>	AN29	MDQ0_25			
MEM_A_DQ<24>	AM29	MDQ0_24			
MEM_A_DQ<23>	AT30	MDQ0_23			
MEM_A_DQ<22>	AT32	MDQ0_22			
MEM_A_DQ<21>	AP33	MDQ0_21			
MEM_A_DQ<20>	AR33	MDQ0_20			
MEM_A_DQ<19>	AP30	MDQ0_19			
MEM_A_DQ<18>	AR30	MDQ0_18			
MEM_A_DQ<17>	AM33	MDQ0_17			
MEM_A_DQ<16>	AN33	MDQ0_16			
MEM_A_DQ<15>	AU35	MDQ0_15			
MEM_A_DQ<14>	AV35	MDQ0_14			
MEM_A_DQ<13>	AT37	MDQ0_13			
MEM_A_DQ<12>	AT38	MDQ0_12			
MEM_A_DQ<11>	AT33	MDQ0_11			
MEM_A_DQ<10>	AT35	MDQ0_10			
MEM_A_DQ<9>	AV37	MDQ0_9			
MEM_A_DQ<8>	AU38	MDQ0_8			
MEM_A_DQ<7>	AR35	MDQ0_7			
MEM_A_DQ<6>	AN36	MDQ0_6			
MEM_A_DQ<5>	AM35	MDQ0_5			
MEM_A_DQ<4>	AM34	MDQ0_4			
MEM_A_DQ<3>	AR36	MDQ0_3			
MEM_A_DQ<2>	AR37	MDQ0_2			
MEM_A_DQ<1>	AM36	MDQ0_1			
MEM_A_DQ<0>	AM37	MDQ0_0			
MEM_A_DM<7>	AN5	MDQM0_7			
MEM_A_DM<6>	AM9	MDQM0_6			
MEM_A_DM<5>	AR9	MDQM0_5			
MEM_A_DM<4>	AM14	MDQM0_4			
MEM_A_DM<3>	AT29	MDQM0_3			
MEM_A_DM<2>	AN32	MDQM0_2			
MEM_A_DM<1>	AT36	MDQM0_1			
MEM_A_DM<0>	AN37	MDQM0_0			

MRAS0*	AR17	MEM_A_RAS_L	26 27 32 67
MCAS0*	AM17	MEM_A_CAS_L	26 27 32 67
MWE0*	AM18	MEM_A_WE_L	26 27 32 67
MBA0_2	AR26	MEM_A_BA<2>	26 27 32 67
MBA0_1	AR18	MEM_A_BA<1>	26 27 32 67
MBA0_0	AP17	MEM_A_BA<0>	26 27 32 67
MA0_15	AN26	MEM_A_A<15>	9 67
MA0_14	AP26	MEM_A_A<14>	26 27 32 67
MA0_13	AR15	MEM_A_A<13>	26 27 32 67
MA0_12	AR24	MEM_A_A<12>	26 27 32 67
MA0_11	AP23	MEM_A_A<11>	26 27 32 67
MA0_10	AP18	MEM_A_A<10>	26 27 32 67
MA0_9	AP24	MEM_A_A<9>	26 27 32 67
MA0_8	AN24	MEM_A_A<8>	26 27 32 67
MA0_7	AR23	MEM_A_A<7>	26 27 32 67
MA0_6	AM23	MEM_A_A<6>	26 27 32 67
MA0_5	AM24	MEM_A_A<5>	26 27 32 67
MA0_4	AN23	MEM_A_A<4>	26 27 32 67
MA0_3	AR21	MEM_A_A<3>	26 27 32 67
MA0_2	AP20	MEM_A_A<2>	26 27 32 67
MA0_1	AP21	MEM_A_A<1>	26 27 32 67
MA0_0	AR20	MEM_A_A<0>	26 27 32 67

=PP1V05_S0_MCP_M2CLK_DLL 8 23

+VIO_M2CLK_DLL	AJ30	550 mA
+VIO_M2CLK_DLL	AK30	
+VIO_M2CLK_DLL	AK31	

PP1V05_S0_MCP_PLL_FSBMEM 23

+VIO_PLL_MEM	AH29	20 mA
+VIO_PLL_MEM	AH30	
+VIO_PLL_MEM	AJ31	25 mA
+VIO_PLL_FSB	AF29	
+VIO_PLL_FSB	AF30	
+VIO_PLL_FSB	AF31	25 mA
+VIO_PLL_CPU	AG29	
+VIO_PLL_CPU	AG30	
+VIO_PLL_CPU	AG31	

MCLK0A_1_P	AM21	MEM_A_CLK_P<1>	9 67
MCLK0A_1_N	AN21	MEM_A_CLK_N<1>	9 67
MCLK0A_0_P	AM20	MEM_A_CLK_P<0>	26 27 32 67
MCLK0A_0_N	AN20	MEM_A_CLK_N<0>	26 27 32 67
MCS0A_1*	AP15	MEM_A_CS_L<1>	26 27 32 67
MCS0A_0*	AN18	MEM_A_CS_L<0>	26 27 32 67
MODT0A_1	AP14	MEM_A_ODT<1>	26 27 32 67
MODT0A_0	AN17	MEM_A_ODT<0>	26 27 32 67
MCKE0A_1	AM27	MEM_A_CKE<1>	21 26 27 32 67
MCKE0A_0	AM26	MEM_A_CKE<0>	21 26 27 32 67

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MEMORY PARTITION 1

MEM_B_DQ<63>	AM1	MDQ1_63	MDQS1_7_P	AN2	MEM_B_DQS_P<7>
MEM_B_DQ<62>	AN1	MDQ1_62	MDQS1_7_N	AN3	MEM_B_DQS_N<7>
MEM_B_DQ<61>	AT1	MDQ1_61	MDQS1_6_P	AY5	MEM_B_DQS_P<6>
MEM_B_DQ<60>	AU1	MDQ1_60	MDQS1_6_N	AY4	MEM_B_DQS_N<6>
MEM_B_DQ<59>	AM3	MDQ1_59	MDQS1_5_P	AV11	MEM_B_DQS_P<5>
MEM_B_DQ<58>	AM2	MDQ1_58	MDQS1_5_N	AW11	MEM_B_DQS_N<5>
MEM_B_DQ<57>	AR2	MDQ1_57	MDQS1_4_P	AV14	MEM_B_DQS_P<4>
MEM_B_DQ<56>	AR1	MDQ1_56	MDQS1_4_N	AW14	MEM_B_DQS_N<4>
MEM_B_DQ<55>	AW3	MDQ1_55	MDQS1_3_P	AW27	MEM_B_DQS_P<3>
MEM_B_DQ<54>	AW4	MDQ1_54	MDQS1_3_N	AY27	MEM_B_DQS_N<3>
MEM_B_DQ<53>	AU8	MDQ1_53	MDQS1_2_P	AV32	MEM_B_DQS_P<2>
MEM_B_DQ<52>	AV8	MDQ1_52	MDQS1_2_N	AW32	MEM_B_DQS_N<2>
MEM_B_DQ<51>	AU2	MDQ1_51	MDQS1_1_P	AY31	MEM_B_DQS_P<1>
MEM_B_DQ<50>	AV2	MDQ1_50	MDQS1_1_N	AY36	MEM_B_DQS_N<1>
MEM_B_DQ<49>	AW6	MDQ1_49	MDQS1_0_P	AN38	MEM_B_DQS_P<0>
MEM_B_DQ<48>	AV6	MDQ1_48	MDQS1_0_N	AN39	MEM_B_DQS_N<0>
MEM_B_DQ<47>	AY9	MDQ1_47			
MEM_B_DQ<46>	AW9	MDQ1_46			
MEM_B_DQ<45>	AY11	MDQ1_45			
MEM_B_DQ<44>	AY12	MDQ1_44			
MEM_B_DQ<43>	AW8	MDQ1_43			
MEM_B_DQ<42>	AY8	MDQ1_42			
MEM_B_DQ<41>	AU9	MDQ1_41			
MEM_B_DQ<40>	AU11	MDQ1_40			
MEM_B_DQ<39>	AU12	MDQ1_39			
MEM_B_DQ<38>	AU14	MDQ1_38			
MEM_B_DQ<37>	AV15	MDQ1_37			
MEM_B_DQ<36>	AU15	MDQ1_36			
MEM_B_DQ<35>	AW12	MDQ1_35			
MEM_B_DQ<34>	AV12	MDQ1_34			
MEM_B_DQ<33>	AY15	MDQ1_33			
MEM_B_DQ<32>	AW15	MDQ1_32			
MEM_B_DQ<31>	AW26	MDQ1_31			
MEM_B_DQ<30>	AY26	MDQ1_30			
MEM_B_DQ<29>	AV29	MDQ1_29			
MEM_B_DQ<28>	AW29	MDQ1_28			
MEM_B_DQ<27>	AU26	MDQ1_27			
MEM_B_DQ<26>	AV26	MDQ1_26			
MEM_B_DQ<25>	AU27	MDQ1_25			
MEM_B_DQ<24>	AU29	MDQ1_24			
MEM_B_DQ<23>	AW30	MDQ1_23			
MEM_B_DQ<22>	AV30	MDQ1_22			
MEM_B_DQ<21>	AY33	MDQ1_21			
MEM_B_DQ<20>	AW33	MDQ1_20			
MEM_B_DQ<19>	AY29	MDQ1_19			
MEM_B_DQ<18>	AY30	MDQ1_18			
MEM_B_DQ<17>	AU32	MDQ1_17			
MEM_B_DQ<16>	AY32	MDQ1_16			
MEM_B_DQ<15>	AW35	MDQ1_15			
MEM_B_DQ<14>	AY35	MDQ1_14			
MEM_B_DQ<13>	AV39	MDQ1_13			
MEM_B_DQ<12>	AU39	MDQ1_12			
MEM_B_DQ<11>	AV33	MDQ1_11			
MEM_B_DQ<10>	AU33	MDQ1_10			
MEM_B_DQ<9>	AW38	MDQ1_9			
MEM_B_DQ<8>	AV38	MDQ1_8			
MEM_B_DQ<7>	AR40	MDQ1_7			
MEM_B_DQ<6>	AR39	MDQ1_6			
MEM_B_DQ<5>	AM39	MDQ1_5			
MEM_B_DQ<4>	AM38	MDQ1_4			
MEM_B_DQ<3>	AT40	MDQ1_3			
MEM_B_DQ<2>	AU40	MDQ1_2			
MEM_B_DQ<1>	AN40	MDQ1_1			
MEM_B_DQ<0>	AM40	MDQ1_0			
MEM_B_DM<7>	AR3	MDQM1_7			
MEM_B_DM<6>	AY6	MDQM1_6			
MEM_B_DM<5>	AV9	MDQM1_5			
MEM_B_DM<4>	AY14	MDQM1_4			
MEM_B_DM<3>	AV27	MDQM1_3			
MEM_B_DM<2>	AU30	MDQM1_2			
MEM_B_DM<1>	AW37	MDQM1_1			
MEM_B_DM<0>	AR38	MDQM1_0			

MRAS1*	AW18	MEM_B_RAS_L	28 29 32 67
MCAS1*	AV17	MEM_B_CAS_L	28 29 32 67
MWE1*	AY18	MEM_B_WE_L	28 29 32 67
MBA1_2	AW24	MEM_B_BA<2>	28 29 32 67
MBA1_1	AT18	MEM_B_BA<1>	28 29 32 67
MBA1_0	AV18	MEM_B_BA<0>	28 29 32 67
MA1_15	AU24	MEM_B_A<15>	9 67
MA1_14	AV24	MEM_B_A<14>	28 29 32 67
MA1_13	AU17	MEM_B_A<13>	28 29 32 67
MA1_12	AY24	MEM_B_A<12>	28 29 32 67
MA1_11	AW23	MEM_B_A<11>	28 29 32 67
MA1_10	AU18	MEM_B_A<10>	28 29 32 67
MA1_9	AY23	MEM_B_A<9>	28 29 32 67
MA1_8	AU23	MEM_B_A<8>	28 29 32 67
MA1_7	AV23	MEM_B_A<7>	28 29 32 67
MA1_6	AT21	MEM_B_A<6>	28 29 32 67
MA1_5	AT23	MEM_B_A<5>	28 29 32 67
MA1_4	AU21	MEM_B_A<4>	28 29 32 67
MA1_3	AV21	MEM_B_A<3>	28 29 32 67
MA1_2	AY21	MEM_B_A<2>	28 29 32 67
MA1_1	AW21	MEM_B_A<1>	28 29 32 67
MA1_0	AY20	MEM_B_A<0>	28 29 32 67

=PP1V5R1V35_S3_MCP_MEM 8

R1520
1K
5%
1/20W
MF
201
2 1

MRESET0*	AM6	MEM_RESET_L	26 27 28 29
MCLK1A_1_P	AV20	MEM_B_CLK_P<1>	9 67
MCLK1A_1_N	AW20	MEM_B_CLK_N<1>	9 67
MCLK1A_0_P	AT20	MEM_B_CLK_P<0>	28 29 32 67
MCLK1A_0_N	AU20	MEM_B_CLK_N<0>	28 29 32 67
MCS1A_1*	AT15	MEM_B_CS_L<1>	28 29 32 67
MCS1A_0*	AY17	MEM_B_CS_L<0>	28 29 32 67
MODT1A_1	AT17	MEM_B_ODT<1>	28 29 32 67
MODT1A_0	AW17	MEM_B_ODT<0>	28 29 32 67
MCKE1A_1	AT24	MEM_B_CKE<1>	21 28 29 32 67
MCKE1A_0	AT26	MEM_B_CKE<0>	21 28 29 32 67

23 21 20 =PP1V5R1V35_SW_MCP_MEM

R1510
40.2
1%
1/20W
MF
201
2 1

R1511
40.2
1%
1/20W
MF
201
2 1

67 MCP_MEM_COMP_GND	AL23	MEM_COMP_GND
67 MCP_MEM_COMP_VDD	AL24	MEM_COMP_VDD

Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

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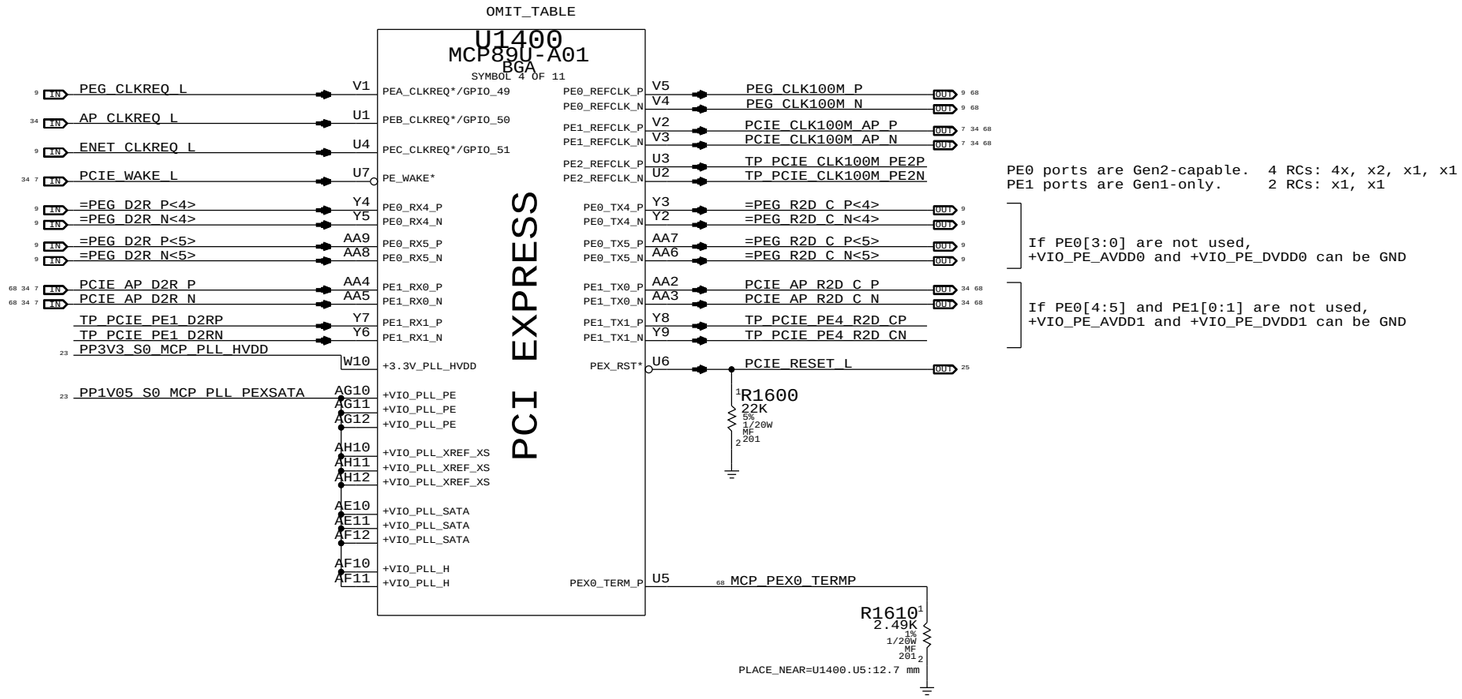

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

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RGB

24	PP3V3_S0_MCP_DAC 140 mA	K30	+3.3V_RGBDAC			
9	TP_MCP_RGB_DAC_VREF	J29	RGB_DAC_VREF			
				DDC_CLK0/GPIO_38	G30	AUD_IP_PERIPHERAL_DET (IN) 7 17 37
				DDC_DATA0/GPIO_39	F30	MIKEY_MIC_LOAD_DET (IN) 17

FLAT PANEL

68 9	OUT DP_IG_ML0_P<3>	H27	DP0_3_P/TMDS0_TXC_P	IFPA_TXC_P	K24	=MCP_IFPA_TXC_P (OUT) 9
68 9	OUT DP_IG_ML0_N<3>	J27	DP0_3_N/TMDS0_TXC_N	IFPA_TXC_N	K23	=MCP_IFPA_TXC_N (OUT) 9
68 9	OUT DP_IG_ML0_P<2>	D26	DP0_2_P/TMDS0_TX0_P	IFPA_TXD0_P	B23	=MCP_IFPA_TXD_P<0> (OUT) 9
68 9	OUT DP_IG_ML0_N<2>	C26	DP0_2_N/TMDS0_TX0_N	IFPA_TXD0_N	C23	=MCP_IFPA_TXD_N<0> (OUT) 9
68 9	OUT DP_IG_ML0_P<1>	F26	DP0_1_P/TMDS0_TX1_P	IFPA_TXD1_P	D23	=MCP_IFPA_TXD_P<1> (OUT) 9
68 9	OUT DP_IG_ML0_N<1>	E26	DP0_1_N/TMDS0_TX1_N	IFPA_TXD1_N	E23	=MCP_IFPA_TXD_N<1> (OUT) 9
68 9	OUT DP_IG_ML0_P<0>	H26	DP0_0_P/TMDS0_TX2_P	IFPA_TXD2_P	F23	=MCP_IFPA_TXD_P<2> (OUT) 9
68 9	OUT DP_IG_ML0_N<0>	G26	DP0_0_N/TMDS0_TX2_N	IFPA_TXD2_N	G23	=MCP_IFPA_TXD_N<2> (OUT) 9
9	OUT DP_IG_ML1_P<3>	F27	DP1_3_P/TMDS0B_TXC_P	IFPA_TXD3_P	H23	=MCP_IFPA_TXD_P<3> (OUT) 9
9	OUT DP_IG_ML1_N<3>	G27	DP1_3_N/TMDS0B_TXC_N	IFPA_TXD3_N	J23	=MCP_IFPA_TXD_N<3> (OUT) 9
9	OUT DP_IG_ML1_P<2>	E27	DP1_2_P/TMDS0_TX3_P	IFPB_TXC_P	J24	=MCP_IFPB_TXC_P (OUT) 9
9	OUT DP_IG_ML1_N<2>	D27	DP1_2_N/TMDS0_TX3_N	IFPB_TXC_N	H24	=MCP_IFPB_TXC_N (OUT) 9
68 9	OUT DP_IG_ML1_P<1>	C27	DP1_1_P/TMDS0_TX4_P	IFPB_TXD4_P	G24	=MCP_IFPB_TXD_P<0> (OUT) 9
68 9	OUT DP_IG_ML1_N<1>	B27	DP1_1_N/TMDS0_TX4_N	IFPB_TXD4_N	F24	=MCP_IFPB_TXD_N<0> (OUT) 9
68 9	OUT DP_IG_ML1_P<0>	A29	DP1_0_P/TMDS0_TX5_P	IFPB_TXD5_P	E24	=MCP_IFPB_TXD_P<1> (OUT) 9
68 9	OUT DP_IG_ML1_N<0>	B29	DP1_0_N/TMDS0_TX5_N	IFPB_TXD5_N	D24	=MCP_IFPB_TXD_N<1> (OUT) 9
				IFPB_TXD6_P	C24	=MCP_IFPB_TXD_P<2> (OUT) 9
				IFPB_TXD6_N	B24	=MCP_IFPB_TXD_N<2> (OUT) 9
9	IN DP_IG_HPD0	C29	HPLUG_DET0/GPIO_20	IFPB_TXD7_P	J26	=MCP_IFPB_TXD_P<3> (OUT) 9
9	IN DP_IG_HPD1	D30	HPLUG_DET1/GPIO_21	IFPB_TXD7_N	K26	=MCP_IFPB_TXD_N<3> (OUT) 9
17	OUT SATARDRVR_A_EN	E30	HPLUG_DET2/GPIO_22			
68 17 9	BI DP_IG_AUX_CH0_P	E29	DDC_CLK2/DP_AUX_CH0_P	DDC_CLK1/GPIO_40	J30	=MCP_IFPAB_DDC_CLK (OUT) 9
68 17 9	BI DP_IG_AUX_CH0_N	D29	DDC_DATA2/DP_AUX_CH0_N	DDC_DATA1/GPIO_41	H30	=MCP_IFPAB_DDC_DATA (BI) 9
68 17 9	BI DP_IG_AUX_CH1_P	G29	DDC_CLK3/DP_AUX_CH1_P			
68 17 9	BI DP_IG_AUX_CH1_N	F29	DDC_DATA3/DP_AUX_CH1_N			

(GMUX_INT)

23	PP3V3_S0_MCP_PLL_DP_USB 210 mA 180 mA	L23 M23	+3.3V_PLL_DP0 +3.3V_PLL_DP0	LCD_BKL_CTL/GPIO_57	B30	LCD_IG_BKLT_PWM (OUT) 9
				LCD_BKL_ON/GPIO_59	C30	LCD_IG_BKLT_EN (OUT) 9
	30 mA	L22 M22	+3.3V_PLL_USB +3.3V_PLL_USB	LCD_PANEL_PWR/GPIO_58	A30	LCD_IG_PWR_EN (OUT) 9 60
24	=PP1V05_S0_MCP_PLL_IFP 60 mA	L25 M25	+VIO_PLL_IFPAB +VIO_PLL_IFPAB			
23	PP1V05_S0_MCP_PLL_CORE 160 mA 40 mA	L26 M26	+VIO_PLL_CORE_LEG +VIO_PLL_CORE_LEG			
	60 mA	L27 M27	+VIO_PLL_SPPLL0 +VIO_PLL_SPPLL0			
	40 mA	L28 M28	+VIO_PLL_V +VIO_PLL_V	IFPAB_VPROBE	C21	MCP_IFPAB_VPROBE (OUT) 24 68
				IFPAB_RSET	B21	MCP_IFPAB_RSET (OUT) 24 68
	20 mA	L24 M24	+VIO_PLL_NV +VIO_PLL_NV			
24	=PP3V3R1V8_S0_MCP_IFP_VDD 180 mA CKPLUS_WAIVE=PwrTerm2Gnd CKPLUS_WAIVE=PwrTerm2Gnd	A23 A24	+VDD_IFPA +VDD_IFPB			
24 8	=PP1V05_S0_MCP_DP0_VDD 160 mA	B26 A27 A26	+VIO_DP0 +VIO_DP0 +VIO_DP0	TMDS0_VPROBE	H29	MCP_TMDS0_VPROBE (OUT) 24 68
				TMDS0_RSET	K27	MCP_TMDS0_RSET (OUT) 24 68

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required (or use as GPIOs).
Connect +3.3V_RGBDAC pin to GND.

NOTE: No Composite/S-Video/Component Video support on MCP89

Interface Mode

MCP Signal	TMDS/HDMI	LVDS
=MCP_IFPA_TXC_P/N	TMDS_IG_TXC_P/N	LVDS_IG_A_CLK_P/N
=MCP_IFPA_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	LVDS_IG_A_DATA_P/N<0>
=MCP_IFPA_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	LVDS_IG_A_DATA_P/N<1>
=MCP_IFPA_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	LVDS_IG_A_DATA_P/N<2>
=MCP_IFPA_TXD_P/N<3>	(UNUSED)	LVDS_IG_A_DATA_P/N<3>
=MCP_IFPB_TXC_P/N	(UNUSED)	LVDS_IG_B_CLK_P/N
=MCP_IFPB_TXD_P/N<0>	TMDS_IG_TXD_P/N<3>	LVDS_IG_B_DATA_P/N<0>
=MCP_IFPB_TXD_P/N<1>	TMDS_IG_TXD_P/N<4>	LVDS_IG_B_DATA_P/N<1>
=MCP_IFPB_TXD_P/N<2>	TMDS_IG_TXD_P/N<5>	LVDS_IG_B_DATA_P/N<2>
=MCP_IFPB_TXD_P/N<3>	(UNUSED)	LVDS_IG_B_DATA_P/N<3>
=MCP_IFPAB_DDC_CLK	TMDS_IG_DDC_CLK	LVDS_IG_DDC_CLK
=MCP_IFPAB_DDC_DATA	TMDS_IG_DDC_DATA	LVDS_IG_DDC_DATA

LVDS: Power +VDD_IFPx at 1.8V
TMDS: Power +VDD_IFPx at 3.3V

NOTE: 100K pull-downs required if HPLUG_DET0/HPLUG_DET1 are not used.

DDC Mode Pull-downs

NOTE: DP_AUX_CH1 also requires pull-downs if used for dual-mode DisplayPort (DP++). If unused no pulls are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.

R1710	100K 5% 1/20W MF 201	1 2	DP_IG_AUX_CH0_P	9 17 68
R1711	100K 5% 1/20W MF 201	1 2	DP_IG_AUX_CH0_N	9 17 68
R1712	100K 5% 1/20W MF 201	1 2	DP_IG_AUX_CH1_P	9 17 68
R1713	100K 5% 1/20W MF 201	1 2	DP_IG_AUX_CH1_N	9 17 68

GPIO Pull-Ups

=PP3V3_S0_MCP_GPIO 8 18 19

R1780	10K 5% 1/20W MF 201	1 2	SATARDRVR_A_EN	17
R1781	10K 5% 1/20W MF 201	1 2	AUD_IP_PERIPHERAL_DET	7 17 37
R1782	10K 5% 1/20W MF 201	1 2	MIKEY_MIC_LOAD_DET	17

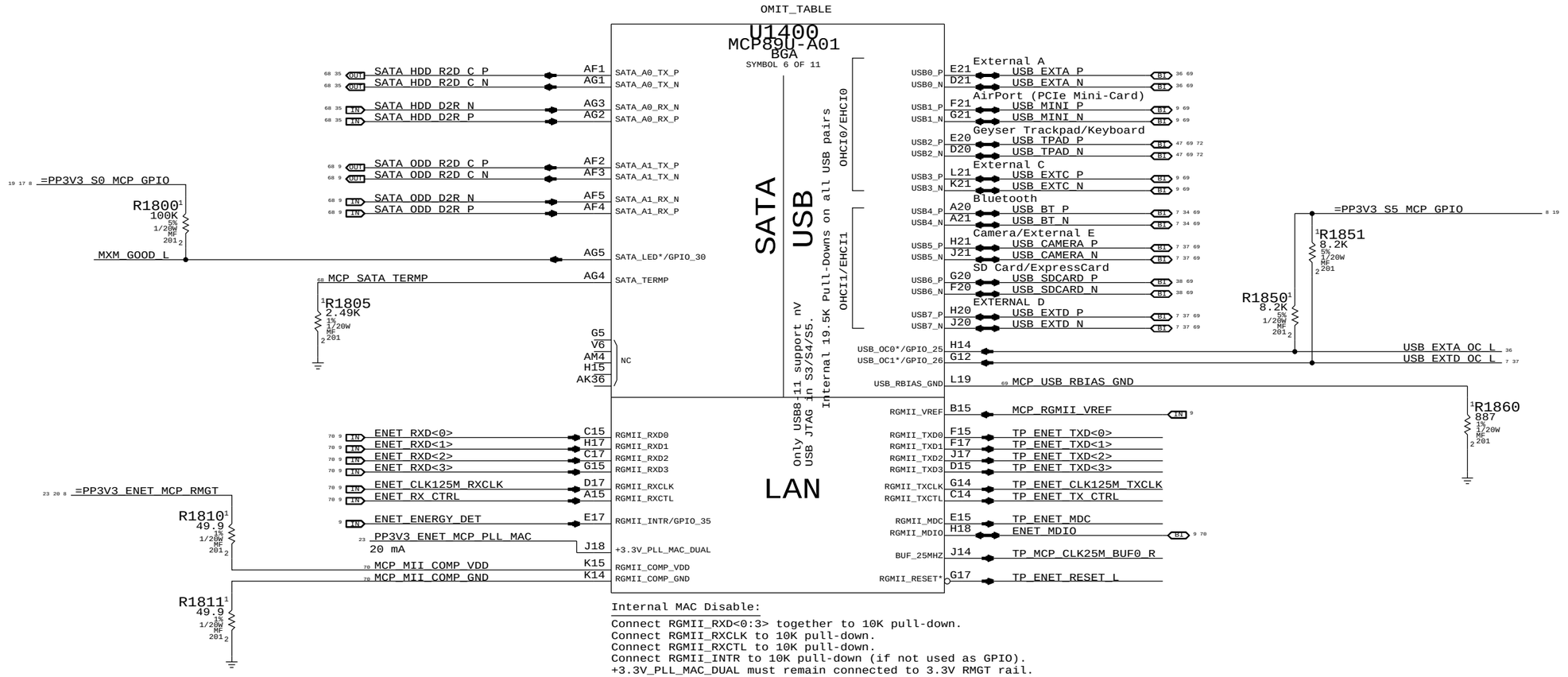
Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: MCP Graphics

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D
REVISION: 3.3.0
BRANCH:
PAGE: 17 OF 110
SHEET: 17 OF 74



Internal MAC Disable:

Connect RGMII_RXD<0:3> together to 10K pull-down.
Connect RGMII_RXCLK to 10K pull-down.
Connect RGMII_RXCTL to 10K pull-down.
Connect RGMII_INTR to 10K pull-down (if not used as GPIO).
+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.
RGMII_COMP_VDD/_GND must remain connected as shown.
Connect RGMII_VREF to 10K pull-down.
Connect RGMII_MDIO to 10K pull-down.
All other pins can be left TP or NC.

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: MCP SATA, USB & Ethernet

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

BRANCH:

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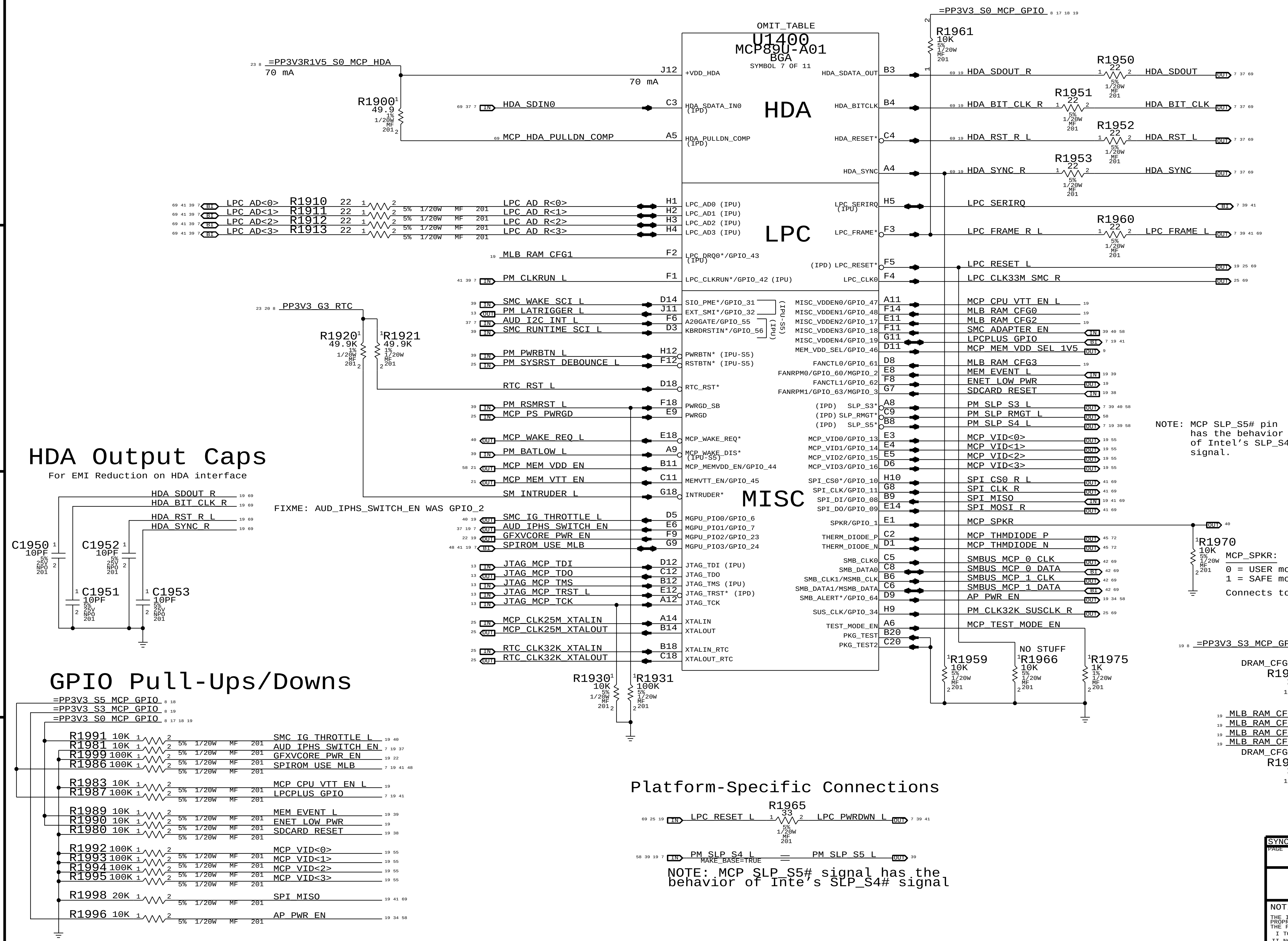

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

BIOS Boot Select

I/F	LPC_FRAME#
LPC	0
SPI	1

NOTE: MCP89 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
42.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command. Straps not provided on this page.

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: MCP HDA, LPC & MISC

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

NOTE: "SW" rails are dynamically switched in the S0 state as needed, controlled by MCP89 GPIOs.

=PP1V05_SW_MCP_FSB
2000 mA

OMIT_TABLE
U1400
MCP89U-A01
BGA
SYMBOL 8 OF 11
POWER I

C32	+VTT_CPU	+VDD_MEM	AK19
E33	+VTT_CPU	+VDD_MEM	AJ23
L29	+VTT_CPU	+VDD_MEM	AJ24
AA29	+VTT_CPU	+VDD_MEM	AK21
E32	+VTT_CPU	+VDD_MEM	AJ17
AA30	+VTT_CPU	+VDD_MEM	AK15
L31	+VTT_CPU	+VDD_MEM	AK5
T30	+VTT_CPU	+VDD_MEM	AJ26
N30	+VTT_CPU	+VDD_MEM	AK13
M31	+VTT_CPU	+VDD_MEM	AK16
F33	+VTT_CPU	+VDD_MEM	AJ19
H33	+VTT_CPU	+VDD_MEM	AK12
J32	+VTT_CPU	+VDD_MEM	AK4
B33	+VTT_CPU	+VDD_MEM	AK26
G33	+VTT_CPU	+VDD_MEM	AK20
B32	+VTT_CPU	+VDD_MEM	AJ27
J33	+VTT_CPU	+VDD_MEM	AJ10
F32	+VTT_CPU	+VDD_MEM	AJ12
H32	+VTT_CPU	+VDD_MEM	AK17
G32	+VTT_CPU	+VDD_MEM	AK23
A33	+VTT_CPU	+VDD_MEM	AJ2
D32	+VTT_CPU	+VDD_MEM	AK3
AB30	+VTT_CPU	+VDD_MEM	AJ22
AB29	+VTT_CPU	+VDD_MEM	AJ21
C33	+VTT_CPU	+VDD_MEM	AK14
D33	+VTT_CPU	+VDD_MEM	AK22
A32	+VTT_CPU	+VDD_MEM	AK8
M29	+VTT_CPU	+VDD_MEM	AK27
M30	+VTT_CPU	+VDD_MEM	AJ4
R30	+VTT_CPU	+VDD_MEM	AK29
P30	+VTT_CPU	+VDD_MEM	AK18
L32	+VTT_CPU	+VDD_MEM	AK24
T29	+VTT_CPU	+VDD_MEM	AJ9
L30	+VTT_CPU	+VDD_MEM	AK11
U30	+VTT_CPU	+VDD_MEM	AK6
P29	+VTT_CPU	+VDD_MEM	AK2
R29	+VTT_CPU	+VDD_MEM	AK25
V30	+VTT_CPU	+VDD_MEM	AJ28
U29	+VTT_CPU	+VDD_MEM	AK9
V29	+VTT_CPU	+VDD_MEM	AK28
Y30	+VTT_CPU	+VDD_MEM	AJ11
Y29	+VTT_CPU	+VDD_MEM	AJ5
W29	+VTT_CPU	+VDD_MEM	AJ29
W30	+VTT_CPU	+VDD_MEM	AJ3
N29	+VTT_CPU	+VDD_MEM	AJ20
K31	+VTT_CPU	+VDD_MEM	AK10
		+VDD_MEM	AJ18
=PP1V05_S0_MCP_FSB			
200 mA			
AC29	+VTT_CPU2	+VDD_MEM	AK1
AD29	+VTT_CPU2	+VDD_MEM	AJ1
AC30	+VTT_CPU2	+VDD_MEM	AJ7
AD30	+VTT_CPU2	+VDD_MEM	AJ8
AB31	+VTT_CPU2	+VDD_MEM	AJ25
AC31	+VTT_CPU2	+VDD_MEM	AJ16
AD31	+VTT_CPU2	+VDD_MEM	AJ15
AC32	+VTT_CPU2	+VDD_MEM	AK7
		+VDD_MEM	AJ6
=PP3V3_S0_MCP_HVDD			
30 mA	V9	+3.3V_HVDD	
	V10	+3.3V	
	H11	+3.3V	
=PP3V3_S0_MCP	K29	+3.3V	
250 mA			
=PP0V9_S5_MCP_VDD_AUXC	AU18	+VDD_DUAL_AUXC	
150 mA	K18	+VDD_DUAL_AUXC	
PP3V3_G3_RTC	A18	+3.3V_VBAT	
2? uA (G3)			
5 mA (S0)	L20	+3.3V_DUAL_USB	
200 mA	K20	+3.3V_DUAL_USB	
	J15	+3.3V_DUAL	
=PP3V3_S5_MCP			
240 mA 40 mA			

+VDD_DUAL_RMGT	K17	=PP0V9_ENET_MCP_RMGT	
+VDD_DUAL_RMGT	L17	140 mA	
+3.3V_DUAL_RMGT	A17	=PP3V3_ENET_MCP_RMGT	
+3.3V_DUAL_RMGT	B17	300 mA	

=PP1V5R1V35_SW_MCP_MEM
4300 mA

=PPVCORE_S0_MCP
8450 mA (0.85V)

NOTE: VDD_COREx_SENSE signals should NOT be used for remote sensing unless COREA/COREB are powered by separate regulators.
Instead connect regulator sense point as close to COREB FET as possible.

OMIT_TABLE
U1400
MCP89U-A01
BGA
SYMBOL 9 OF 11
POWER II

N7	+VDD_COREA	+VDD_COREB	M9
N2	+VDD_COREA	+VDD_COREB	K2
N11	+VDD_COREA	+VDD_COREB	L7
R12	+VDD_COREA	+VDD_COREB	M7
P9	+VDD_COREA	+VDD_COREB	Y23
R8	+VDD_COREA	+VDD_COREB	M2
N4	+VDD_COREA	+VDD_COREB	AB23
R5	+VDD_COREA	+VDD_COREB	M11
R3	+VDD_COREA	+VDD_COREB	M12
P3	+VDD_COREA	+VDD_COREB	L8
P4	+VDD_COREA	+VDD_COREB	M8
P8	+VDD_COREA	+VDD_COREB	M10
R2	+VDD_COREA	+VDD_COREB	L10
P1	+VDD_COREA	+VDD_COREB	M6
R9	+VDD_COREA	+VDD_COREB	L12
N5	+VDD_COREA	+VDD_COREB	K10
N10	+VDD_COREA	+VDD_COREB	K7
P10	+VDD_COREA	+VDD_COREB	M1
R1	+VDD_COREA	+VDD_COREB	K8
P2	+VDD_COREA	+VDD_COREB	K5
R4	+VDD_COREA	+VDD_COREB	L9
N8	+VDD_COREA	+VDD_COREB	M3
R10	+VDD_COREA	+VDD_COREB	J4
P5	+VDD_COREA	+VDD_COREB	M4
AD24	+VDD_COREA	+VDD_COREB	L11
R7	+VDD_COREA	+VDD_COREB	L5
P6	+VDD_COREA	+VDD_COREB	J2
R6	+VDD_COREA	+VDD_COREB	J1
AB24	+VDD_COREA	+VDD_COREB	J7
AC24	+VDD_COREA	+VDD_COREB	M5
P11	+VDD_COREA	+VDD_COREB	L4
P12	+VDD_COREA	+VDD_COREB	L3
P7	+VDD_COREA	+VDD_COREB	J3
R11	+VDD_COREA	+VDD_COREB	K11
AD23	+VDD_COREA	+VDD_COREB	J6
Y24	+VDD_COREA	+VDD_COREB	L2
AA24	+VDD_COREA	+VDD_COREB	L1
N12	+VDD_COREA	+VDD_COREB	J5
AD17	+VDD_COREA	+VDD_COREB	L6
AD18	+VDD_COREA	+VDD_COREB	K4
AD19	+VDD_COREA	+VDD_COREB	V23
AD20	+VDD_COREA	+VDD_COREB	V17
AD21	+VDD_COREA	+VDD_COREB	V19
AD22	+VDD_COREA	+VDD_COREB	V18
U24	+VDD_COREA	+VDD_COREB	V20
V24	+VDD_COREA	+VDD_COREB	V21
W24	+VDD_COREA	+VDD_COREB	V22
T11	+VDD_COREA	+VDD_COREB	AB21
T12	+VDD_COREA	+VDD_COREB	Y17
U11	+VDD_COREA	+VDD_COREB	Y18
V11	+VDD_COREA	+VDD_COREB	Y19
		+VDD_COREB	Y20
TP_MCP_VDDCOREA_SENSEP	U9	+VDD_COREA_SENSE	+VDD_COREB	Y21
TP_MCP_VDDCOREA_SENSEN	U8	GND_COREA_SENSE	+VDD_COREB	Y22
			+VDD_COREB	AB22
=PP1V05_S0_MCP_PE_DVDD			+VDD_COREB	AB17
400 MA	AD8	+VIO_PE_DVDD	+VDD_COREB	AB18
(PE0[5:0], PE1[1:0])	AD6	+VIO_PE_DVDD	+VDD_COREB	AB19
	AC8	+VIO_PE_DVDD	+VDD_COREB	AB20
	AC9	+VIO_PE_DVDD	+VDD_COREB	L13
	AD9	+VIO_PE_DVDD	+VDD_COREB	L14
	AC7	+VIO_PE_DVDD	+VDD_COREB	M13
	AC10	+VIO_PE_DVDD	+VDD_COREB	M14
	AD7	+VIO_PE_DVDD		
	AD11	+VIO_PE_DVDD		
	AD10	+VIO_PE_DVDD		
	AC11	+VIO_PE_DVDD		
	AC12	+VIO_PE_DVDD	+VDD_COREB_SENSE	J9	TP_MCP_VDDCOREB_SENSEP
	AD12	+VIO_PE_DVDD	GND_COREB_SENSE	J8	TP_MCP_VDDCOREB_SENSEN
	AE12	+VIO_PE_DVDD		
PP1V05_S0_MCP_PE_AVDD				
1000 MA	AA10	+VIO_PE_AVDD	+VIO_SATA_AVDD	AF6	PP1V05_S0_MCP_SATA_AVDD
(PE0[5:0], PE1[1:0])	U12	+VIO_PE_AVDD	+VIO_SATA_AVDD	AG8	300 mA
	AB10	+VIO_PE_AVDD	+VIO_SATA_AVDD	AF7	
	V12	+VIO_PE_AVDD	+VIO_SATA_AVDD	AF8	
	W11	+VIO_PE_AVDD	+VIO_SATA_AVDD	AG9	
	W12	+VIO_PE_AVDD	+VIO_SATA_AVDD	AG6	
	Y11	+VIO_PE_AVDD	+VIO_SATA_AVDD	AF9	
	Y12	+VIO_PE_AVDD	+VIO_SATA_AVDD	AG7	
	AA11	+VIO_PE_AVDD		
	AA12	+VIO_PE_AVDD		
	AB11	+VIO_PE_AVDD	+VIO_SATA_DVDD	AD1	=PP1V05_S0_MCP_SATA_DVDD
	AB12	+VIO_PE_AVDD	+VIO_SATA_DVDD	AD2	100 mA
			+VIO_SATA_DVDD	AD3	
			+VIO_SATA_DVDD	AD4	
			+VIO_SATA_DVDD	AC3	
			+VIO_SATA_DVDD	AC4	
			+VIO_SATA_DVDD	AC5	
			+VIO_SATA_DVDD	AD5	
			+VIO_SATA_DVDD	AC6	
			+VIO_SATA_DVDD	AC1	
			+VIO_SATA_DVDD	AC2	

=PPVCORE_SW_MCP_GFX
15350 mA (0.85V)

OMIT_TABLE
U1400
MCP89U-A01
BGA
SYMBOL 10 OF 11
GND

AL34	GND	GND	G13
AT10			E10
AE4			B10
K37			AM32
AL25			AU25
T36			AY38
T37			W4
AB2			AU10
AB4			D10
C40			H31
B5			AL31
G4			U31
AE8			AT31
AW34			AH31
AC20			AN25
AE5			AC21
W18			AA22
AT16			AN16
AB5			AE31
N34			AU34
AT2			AW19
W20			G10
AW16			B22
D7			B19
B2			B34
G37			E22
D16			AC18
K39			K34
G31			AL22
B7			AP36
L15			G34
W19			P31
Y10	GND	GND	U21
AW2			H25
AH7			B31
B13			AU4
AE37			AA19
AV1			W8
AN19			AT19
AP10			AT13
W33			AH2
AB36			AP19
K13			A38
AU13			AT34
AA23			AE39
AA31			AA18
Y31			AT25
AE33			AW31
AY3			U23
N33			D22
T2			W36
B39			W39
T4			W37
AH37			AC23
V31			AP22
AU37			AN13
AW5			AP31
AU7			AU31
AT7			AL19
AN28			AL2
D4			AA20
AU19			E28
AP25			AH34
AU22			B28
AW13			AV40
T33			D28
E7			H28
AW7			G36
H13			AE36

OMIT_TABLE
U1400
MCP89U-A01
BGA
SYMBOL 11 OF 11
GND

B16	GND	GND	B36
E16			AB37
AP16			AE2
AL36			AL7
G19			D13
AA21			T39
K16			AH4
K28			AB7
D25			AH36
AL16			AC17
AP4			AH5
G25			AL33
K25			AW10
E31			W17
G16			G39
AP13			AB39
U22			AH39
AP28			AL5
AT28			AW39
H16			AN10
AH33			AB8
AT22			N39
AL8			N36
AA1			N37
AP37			AE29
W22			AW28
H19			AU28
A3			E19
AH8	GND	GND	L16
G28			K22
R31			AW22
AW25			T34
AP39			AN22
AB33			D31
B25			AE30
U10			T8
W34			M16
U19			M15
K12			M17
E34			M18
AL28			M19
AE34			M20
AT39			M21
AP5			AE7
W21			W5
D34			W7
E25			AP2
K36			AL10
D19			AP34
Y1			U18
W23			T7
AC22			W31
H22			AL39
H8			T31
K19			N31
G2			AA17
E2			T10
T5			K33
AC19			E13
AN31			AL13
AL37			AP7
AU16			U17
AB34			W2
U20			AK34
G22			AK35
AW36			H6
AL4			H7
C1			V7
E39			V8
D37			AM5

Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: MCP Power & Ground

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D
REVISION: 3.3.0
BRANCH:
PAGE: 20 OF 110
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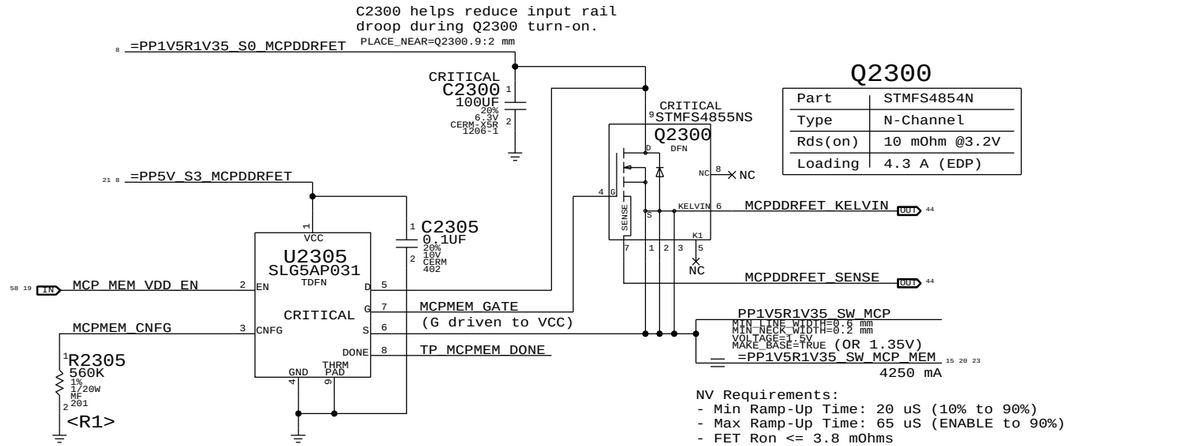
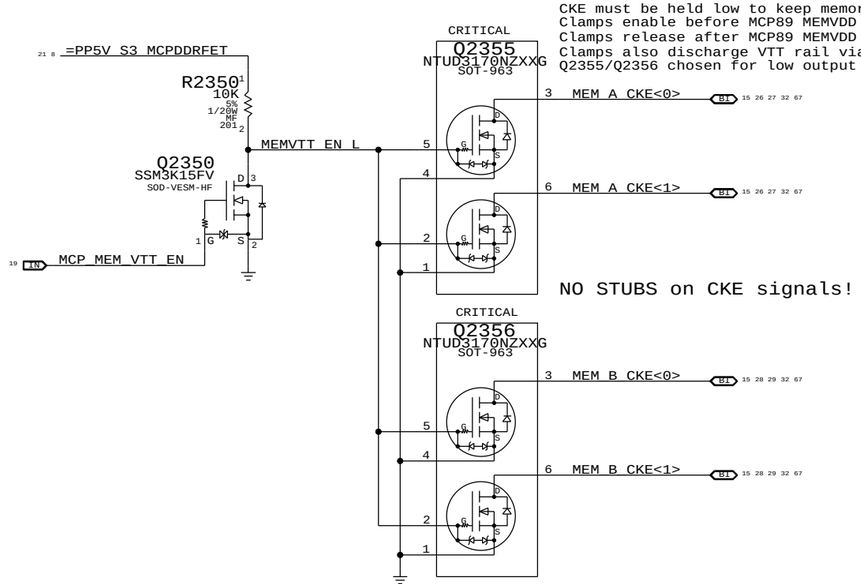


Q2300

Part	STMFS4854N
Type	N-Channel
Rds(on)	10 mOhm @3.2V
Loading	4.3 A (EDP)

DIMM CKE Clamps

CKE must be held low to keep memory in self-refresh.
Clamps enable before MCP89 MEMVDD rail switched off.
Clamps release after MCP89 MEMVDD is up and CKEs are driven by MCP89.
Clamps also discharge VTT rail via termination resistor on each CKE signal on DIMM.
Q2355/Q2356 chosen for low output capacitance.



SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2016

PAGE TITLE
MCP89 Memory Rail Gating

Apple Inc.

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REVISION 3.3.0
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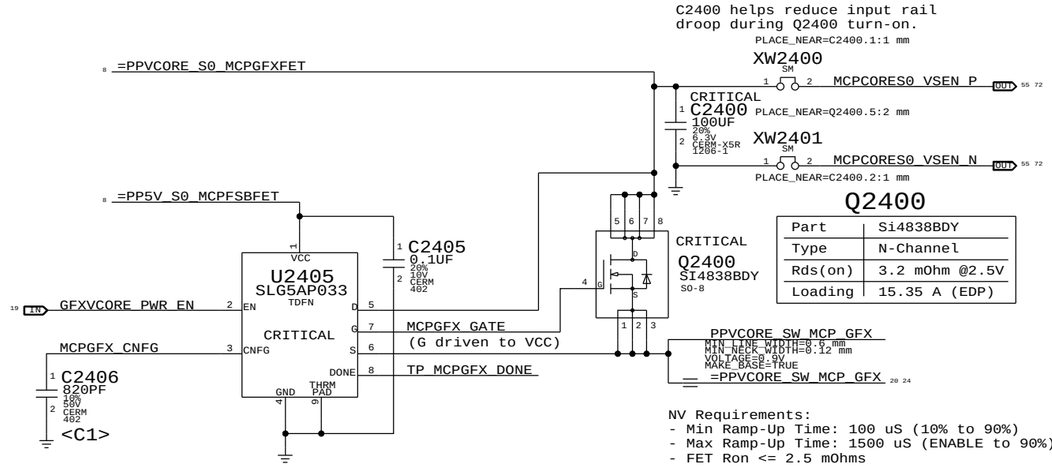

Q2400

Part	Si4838BDY
Type	N-Channel
Rds(on)	3.2 mOhm @2.5V
Loading	15.35 A (EDP)

Approx. Ramp Time (EN to 1V, uS): 43.9 + 0.6943 * C1(pF)

NV Requirements:
- Min Ramp-Up Time: 100 uS (10% to 90%)
- Max Ramp-Up Time: 1500 uS (ENABLE to 90%)
- FET Ron <= 2.5 mOhms

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.

Gated Rail Savings: 860mW

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
MCP89 GFX Core Rail Gating

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
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MCP Non-GFX Core Power
=PPVCORE_S0_MCP
8450 mA (0.85V)
OMIT_TABLE
C2500 10UF 20% 6.3V X5R 603-1
C2501 4.7UF 20% 4V X5R-1 402
C2502 1.0UF 20% 6.3V X5R 0201
C2503 0.22UF 20% 6.3V X5R 201
C2504 0.1UF 10% 6.3V X5R 201
C2505 0.1UF 10% 6.3V X5R 201
C2506 0.1UF 10% 6.3V X5R 201
C2507 0.1UF 10% 6.3V X5R 201
C2508 0.1UF 10% 6.3V X5R 201

MCP Memory Power
=PP1V5R1V35_SW_MCP_MEM
4300 mA (1.5V)
C2510 4.7UF 20% 4V X5R-1 402
C2511 0.1UF 10% 6.3V X5R 201
C2512 0.1UF 10% 6.3V X5R 201
C2513 0.1UF 10% 6.3V X5R 201
C2514 0.1UF 10% 6.3V X5R 201
C2515 0.1UF 10% 6.3V X5R 201
C2516 0.1UF 10% 6.3V X5R 201
C2517 0.1UF 10% 6.3V X5R 201
C2518 0.1UF 10% 6.3V X5R 201
C2519 0.1UF 10% 6.3V X5R 201

MCP CPU FSB (VTT) Power
=PP1V05_SW_MCP_FSB
2000 mA
OMIT_TABLE
C2520 10UF 20% 6.3V X5R 603-1
C2521 4.7UF 20% 4V X5R-1 402
C2522 1.0UF 20% 6.3V X5R 0201
C2523 1.0UF 20% 6.3V X5R 0201

MCP S0 FSB (VTT) Power
=PP1V05_S0_MCP_FSB
200 mA
C2524 4.7UF 20% 4V X5R-1 402
C2525 1.0UF 20% 6.3V X5R 0201

MCP 0.9V AUX Core Power
=PP0V9_S5_MCP_VDD_AUXC
150 mA
C2526 0.1UF 10% 6.3V X5R 201
C2527 0.1UF 10% 6.3V X5R 201

MCP 0.9V MAC/SMU Power
=PP0V9_ENET_MCP_RMGT
140 mA
C2528 4.7UF 20% 4V X5R-1 402
C2529 0.1UF 10% 6.3V X5R 201

MCP 1.05V PCIE Digital Power
=PP1V05_S0_MCP_PE_DVDD
200 mA
C2530 4.7UF 20% 4V X5R-1 402
C2538 4.7UF 20% 4V X5R-1 402
C2531 1.0UF 20% 6.3V X5R 0201
C2532 1.0UF 20% 6.3V X5R 0201
C2533 0.1UF 10% 6.3V X5R 201
C2534 0.1UF 10% 6.3V X5R 201
C2535 0.1UF 10% 6.3V X5R 201

MCP 1.05V SATA Digital Power
=PP1V05_S0_MCP_SATA_DVDD
100 mA
C2536 4.7UF 20% 4V X5R-1 402
C2537 0.1UF 10% 6.3V X5R 201

MCP 1.05V Memory DLL Power
=PP1V05_S0_MCP_M2CLK_DLL
550 mA
C2540 4.7UF 20% 4V X5R-1 402

MCP 3.3V PCIe/SATA I/O PLL Power
=PP3V3_S0_MCP_HVDD
30 mA
C2541 4.7UF 20% 6.3V CERM 603
C2542 0.1UF 20% 10V CERM 402

MCP 3.3V I/O Power
=PP3V3_S0_MCP
250 mA
C2543 4.7UF 20% 6.3V CERM 603
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402

MCP 3.3V/1.5V HDA Power
=PP3V3R1V5_S0_MCP_HDA
70 mA
C2548 4.7UF 20% 6.3V CERM 603
C2549 0.1UF 10% 6.3V X5R 201

MCP 3.3V AUX/USB Power
=PP3V3_S5_MCP
240 mA
C2550 4.7UF 20% 6.3V CERM 603
C2551 0.1UF 20% 10V CERM 402

MCP 2.0V-3.3V RTC Power
PP3V3_G3_RTC
? uA (G3)
5 mA (S0)
C2552 4.7UF 20% 6.3V CERM 603

MCP 3.3V MAC/SMU Power
=PP3V3_ENET_MCP_RMGT
300 mA
C2553 4.7UF 20% 6.3V CERM 603
C2554 0.1UF 20% 10V CERM 402

MCP 3.3V MAC PLL POWER
=PP3V3_ENET_MCP_PLL_MAC
20 mA
CRITICAL
L2555 FERR-240-OHM-200MA 0402
PP3V3_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
C2555 4.7UF 20% 6.3V CERM 603
C2556 0.1UF 20% 10V CERM 402

MCP 1.05V PCIe Analog Power
=PP1V05_S0_MCP_AVDD_UF
800 mA
L2560 30-OHM-5A 0603
PP1V05_S0_MCP_PE_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
500 mA
OMIT_TABLE
C2560 10UF 20% 6.3V X5R 603-1
C2561 4.7UF 20% 4V X5R-1 402
C2559 4.7UF 20% 4V X5R-1 402
C2562 1.0UF 20% 6.3V X5R 0201
C2563 1.0UF 20% 6.3V X5R 0201
C2564 0.1UF 10% 6.3V X5R 201
C2565 0.1UF 10% 6.3V X5R 201
C2566 0.1UF 10% 6.3V X5R 201

MCP 1.05V SATA Analog Power
L2567 30-OHM-5A 0603
PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
300 mA
OMIT_TABLE
C2567 10UF 20% 6.3V X5R 603-1
C2568 4.7UF 20% 4V X5R-1 402
C2569 0.1UF 10% 6.3V X5R 201

MCP 1.05V CPU/FSB/MEM PLL Power
=PP1V05_S0_MCP_PLL_UF
555 mA
CRITICAL
L2570 220-OHM-2.2A 0603
PP1V05_S0_MCP_PLL_FSBMEM
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
70 mA
C2570 4.7UF 20% 4V X5R-1 402
C2571 0.1UF 10% 6.3V X5R 201
C2572 0.1UF 10% 6.3V X5R 201
C2573 0.1UF 10% 6.3V X5R 201
R2570 0.33 5% 1/16W MF 0402
PLACE_NEAR=R2570.1:50 mil
GND_MCP_PLL_FSB
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=0V

MCP 1.05V PCIe/SATA PLL Power
CRITICAL
L2575 220-OHM-2.2A 0603
PP1V05_S0_MCP_PLL_PEXSATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
325 mA
C2575 4.7UF 20% 4V X5R-1 402
C2576 0.1UF 10% 6.3V X5R 201
C2577 0.1UF 10% 6.3V X5R 201
C2578 0.1UF 10% 6.3V X5R 201
C2579 0.1UF 10% 6.3V X5R 201

MCP 1.05V Core/Misc PLL Power
CRITICAL
L2580 220-OHM-2.2A 0603
PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
160 mA
C2580 4.7UF 20% 4V X5R-1 402
C2581 0.1UF 10% 6.3V X5R 201
C2582 0.1UF 10% 6.3V X5R 201
C2583 0.1UF 10% 6.3V X5R 201
C2584 0.1UF 10% 6.3V X5R 201

MCP 3.3V PLL Power
MCPHVDD:P3V3
CRITICAL
L2590 FERR-240-OHM-200MA 0402
=PP3V3_S0_MCP_PLL_UF
260 mA
PP3V3_S0_MCP_PLL_HVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
50 mA
MCPHVDD:P2V5
R2590 10K 5% 1/20W MF 201
MCPHVDD:P2V5
C2592 1.0UF 20% 6.3V X5R 0201
CRITICAL
OMIT_TABLE
U2590 MIC5365-2.5V SC70
VIN VOUT EN NC GND
P2V8HVDD_EN
HVDDLDO:ADJ
R2591 665K 1% 1/20W MF 201
<Ra>
P2V8HVDD_FB
HVDDLDO:ADJ
R2592 316K 1% 1/20W MF 201
<Rb>
C2590 4.7UF 20% 6.3V CERM 603
C2591 0.1UF 20% 10V CERM 402
Vout = 0.8V * (Ra + Rb) / Rb, Rb ~ 320kOhms

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2988	1	IC,MIC5366,LDO REG,2.5V,150MA,SC70	U2590	CRITICAL	HVDDLDO:FIXED
353S2979	1	IC,LDO,TPS717,ADJ,150MA,3%,SC70,HF	U2590	CRITICAL	HVDDLDO:ADJ

MCP 3.3V DP & USB PLL Power
CRITICAL
L2595 220-OHM-2.2A 0603
PP3V3_S0_MCP_PLL_DP_USB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
210 mA
C2595 4.7UF 20% 6.3V CERM 603
C2596 0.1UF 20% 10V CERM 402
C2597 0.1UF 20% 10V CERM 402
R2595 0.33 5% 1/16W MF 0402
PLACE_NEAR=R2595.1:50 mil
GND_MCP_PLL_DP_USB
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=0V

Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010
PAGE TITLE: MCP Standard Decoupling
Apple Inc.
DRAWING NUMBER: 051-8467 SIZE: D
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MCP GFX Core Power

=PPVCORE_SW_MCP_GFX
15350 mA (0.85V)
OMIT_TABLE

C2600 10UF 20% 6.3V X5R 603-1
C2601 4.7UF 20% 4V X5R-1 402
C2602 1.0UF 20% 6.3V X6R 0201
C2603 1.0UF 20% 6.3V X6R 0201
C2604 0.22UF 20% 6.3V X5R 201
C2605 0.22UF 20% 6.3V X5R 201
C2606 0.1UF 10% 6.3V X5R 201
C2607 0.1UF 10% 6.3V X5R 201
C2608 0.1UF 10% 6.3V X5R 201
C2609 0.1UF 10% 6.3V X5R 201
C2610 0.1UF 10% 6.3V X5R 201
C2611 0.1UF 10% 6.3V X5R 201
C2612 0.1UF 10% 6.3V X5R 201

MCP 3.3V RGBDAC Power

GND_MCP_DAC_P3V3
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
MAKE_BASE=TRUE

R2670 0 5% 1/20W MF 201

PP3V3_S0_MCP_DAC
140 mA

If RGBDAC is used, requires ferrite (155S0382) plus 1x 4.7uF 0603 & 1x 0.1uF 0402 cap.
If RGBDAC is not used, tie to GND.

=PP3V3R1V8_S0_MCP_IFP_VDD

=PP1V05_S0_MCP_PLL_IFP

MCP 1.05V DisplayPort Power

=PP1V05_S0_MCP_DP0_VDD
160 mA

C2640 4.7UF 20% 4V X5R-1 402
C2641 0.1UF 10% 6.3V X5R 201

MCP_TMDS0_RSET
MCP_TMDS0_VPROBE

NO STUFF
C2650 0.1UF 10% 6.3V X5R 201
R2650 1K 1% 1/20W MF 201

MCP_IFPAB_RSET
MCP_IFPAB_VPROBE

NO STUFF
C2655 0.1UF 10% 6.3V X5R 201
NO STUFF
R2655 1K 1% 1/20W MF 201

Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: MCP Graphics Support

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D
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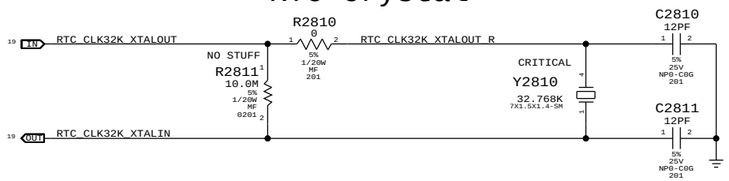
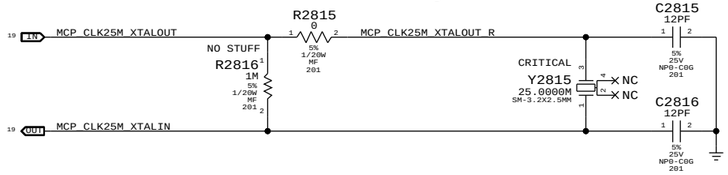
RTC Crystal

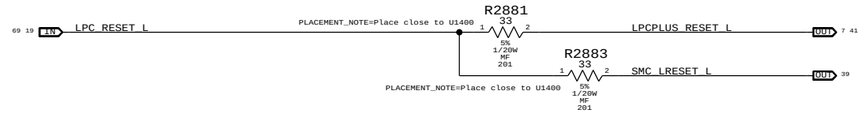


MCP 25MHz Crystal

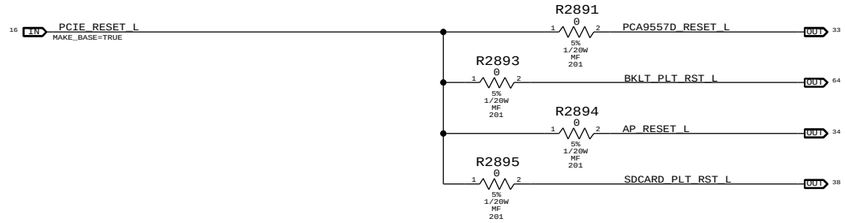


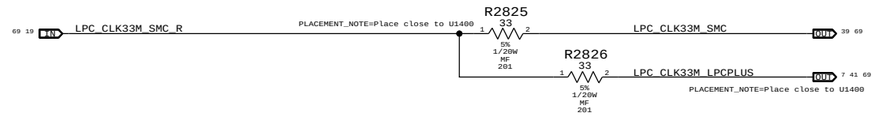
Platform Reset Connections

LPC Reset (Unbuffered)

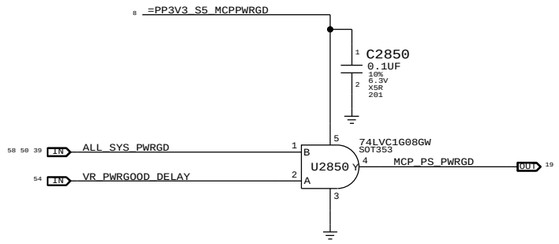


PCIE Reset (Unbuffered)

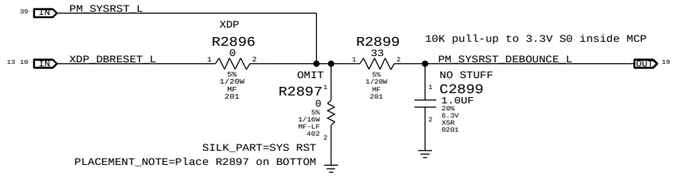




MCP S0 PWRGD & CPU_VLD



System Reset Circuit



SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/11/2010)

PAGE TITLE: SB Misc

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

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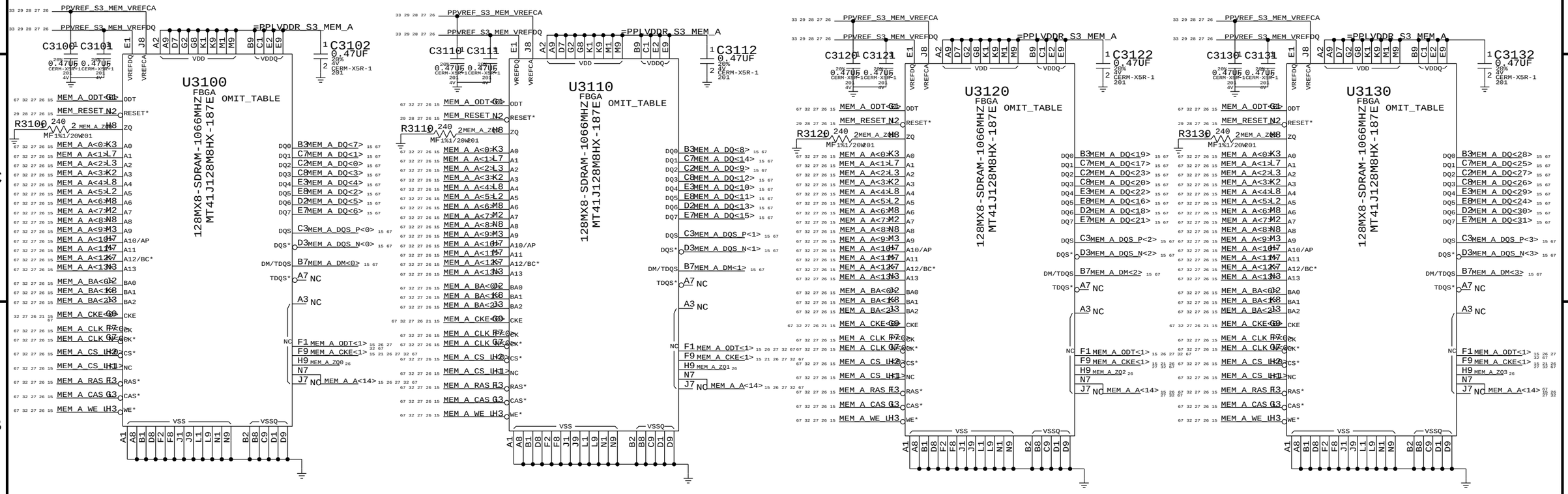

A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
DDR3 DRAM Channel A (0-31)

Apple Inc.

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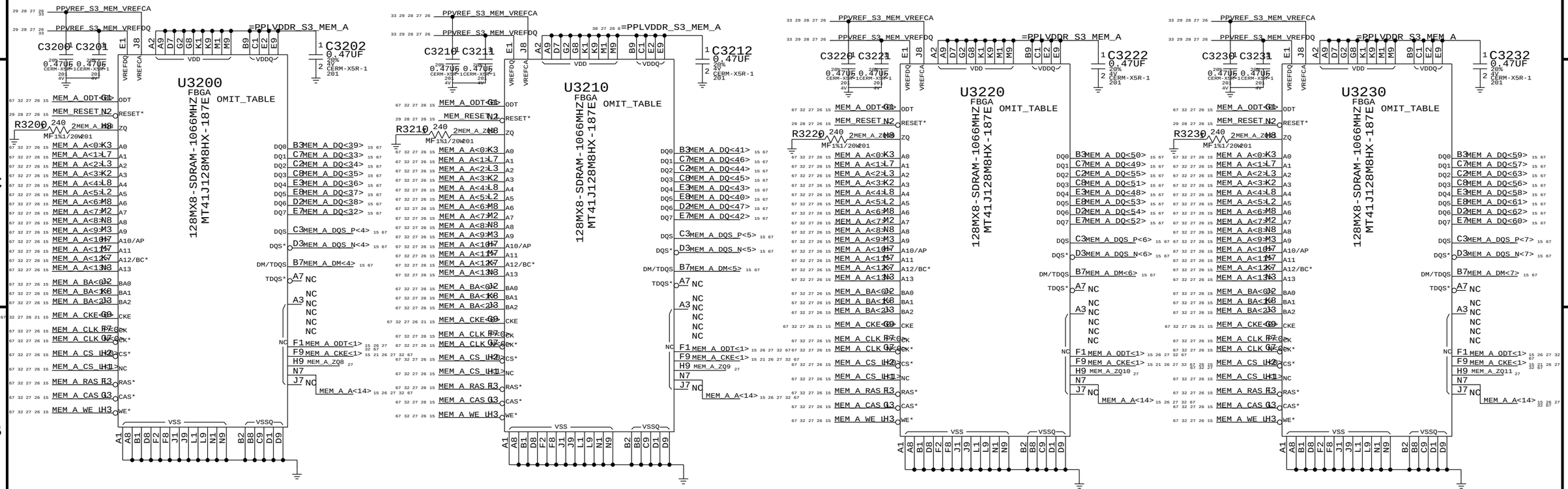

A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
DDR3 DRAM Channel A (32-63)

Apple Inc.

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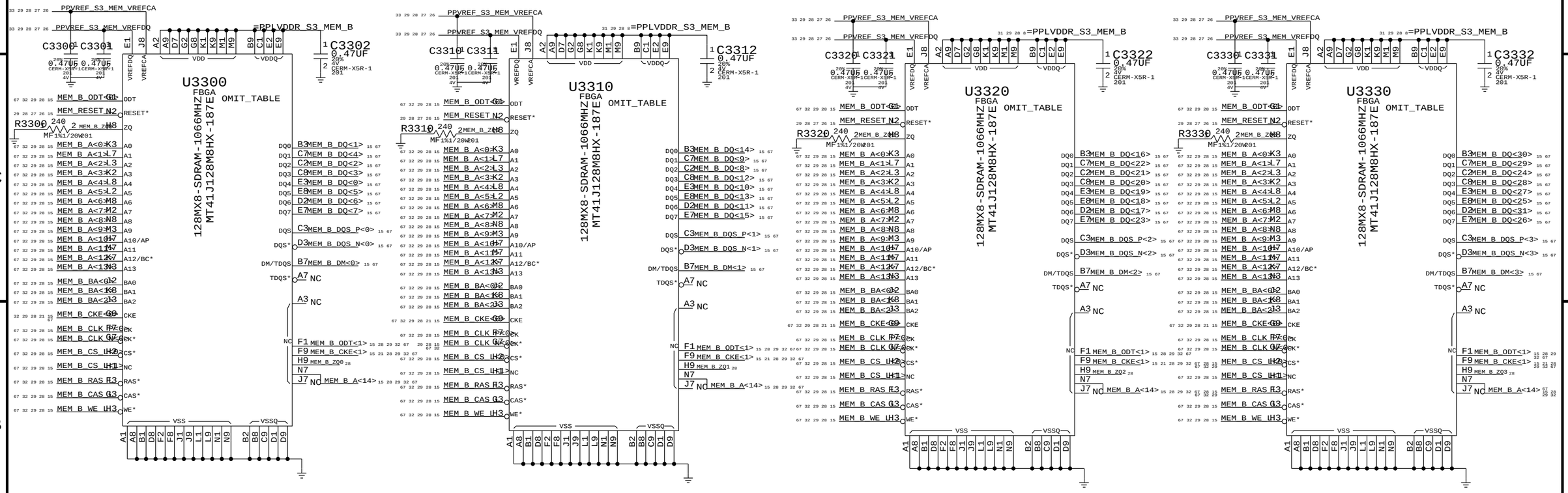

A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
DDR3 DRAM Channel B (0-31)

Apple Inc.

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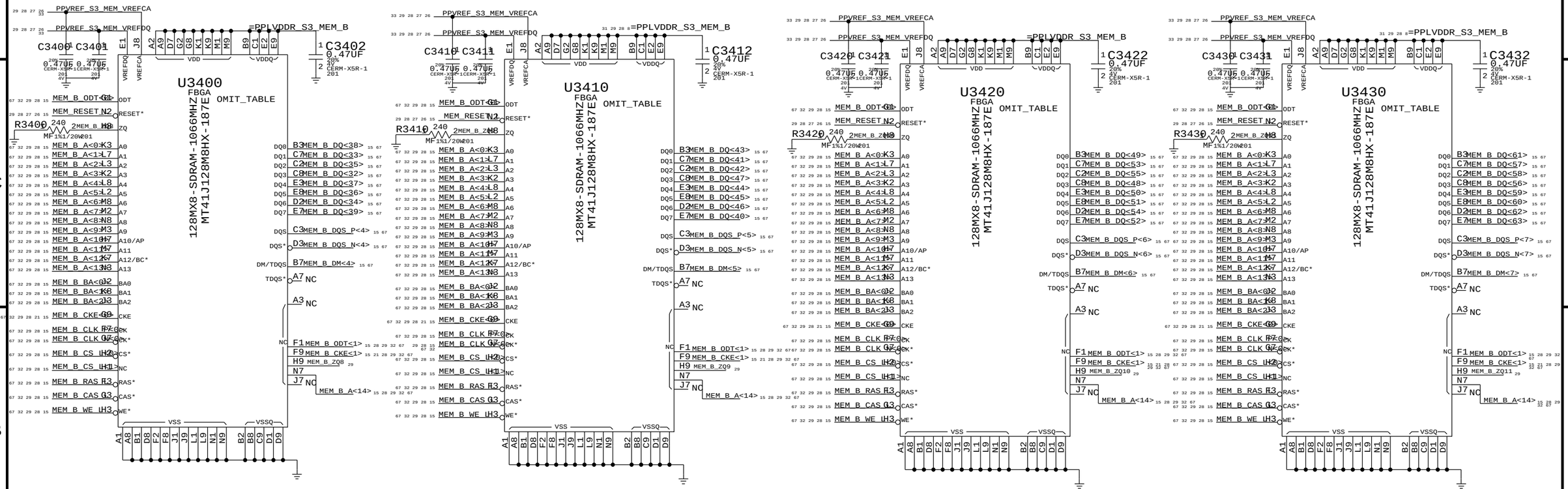

A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
DDR3 DRAM Channel B (32-63)

Apple Inc.

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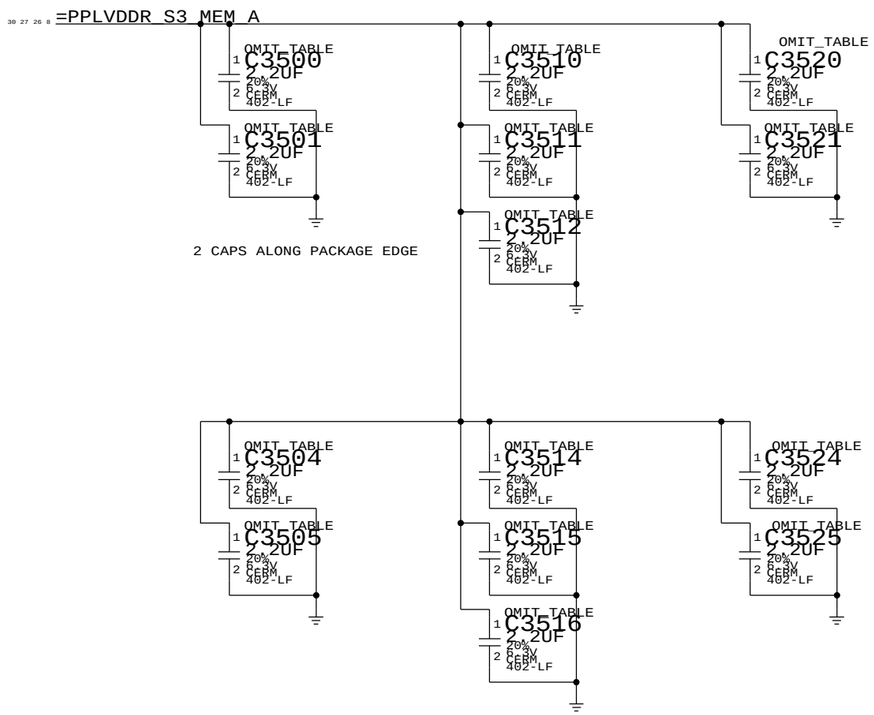

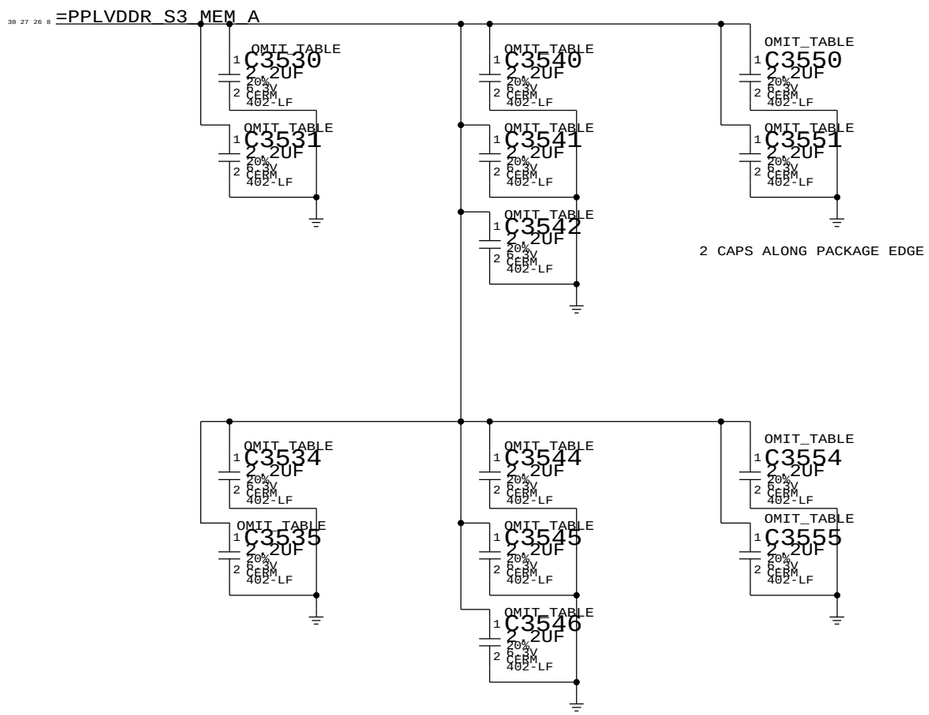

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
DDR BYPASSING 1

Apple Inc.

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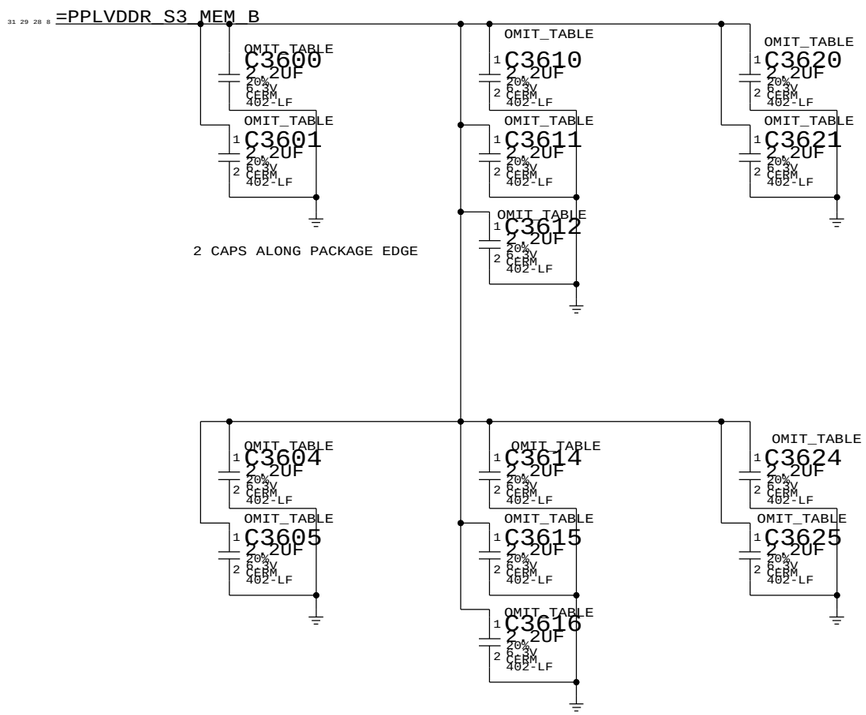

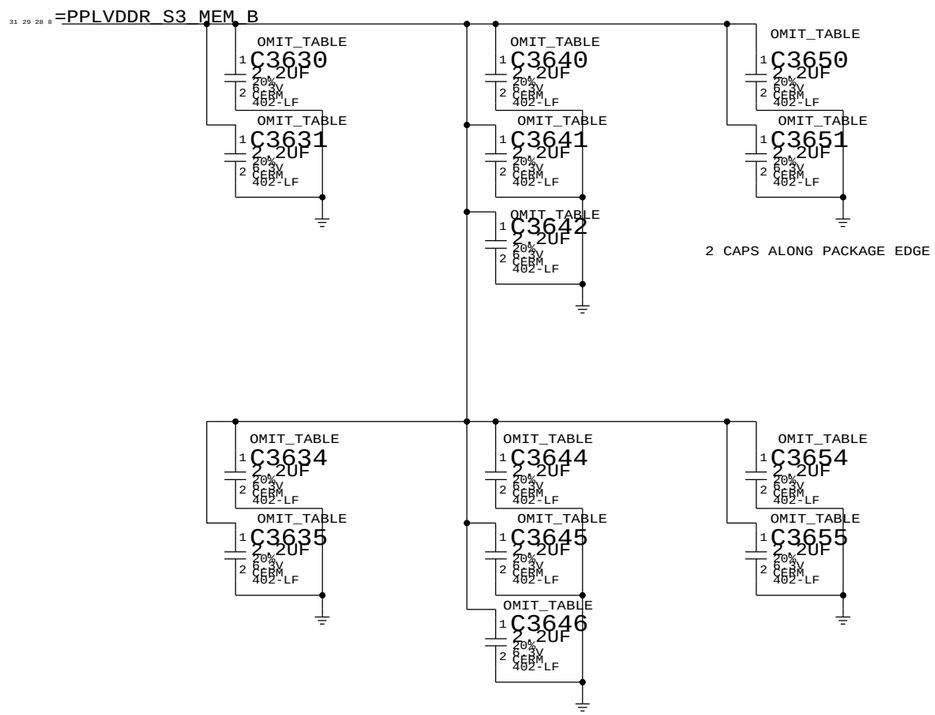

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
DDR BYPASSING 2

Apple Inc.

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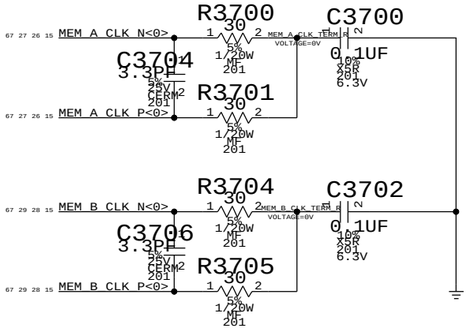
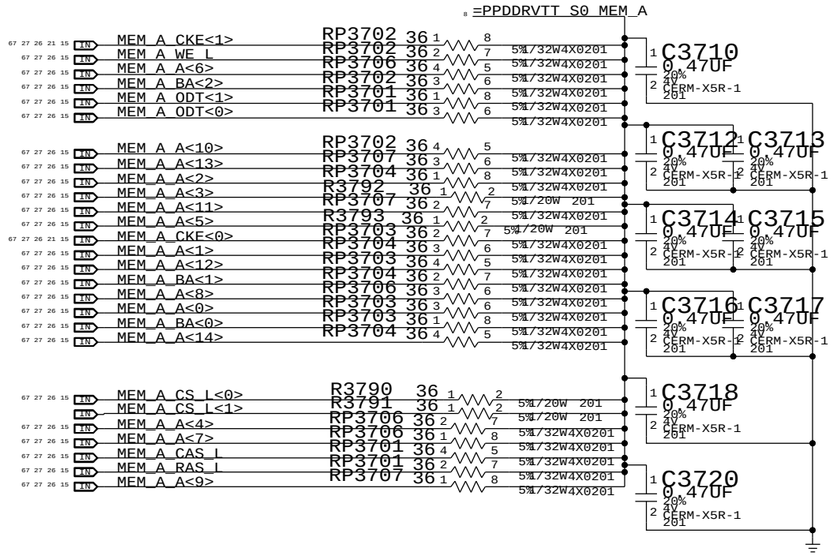
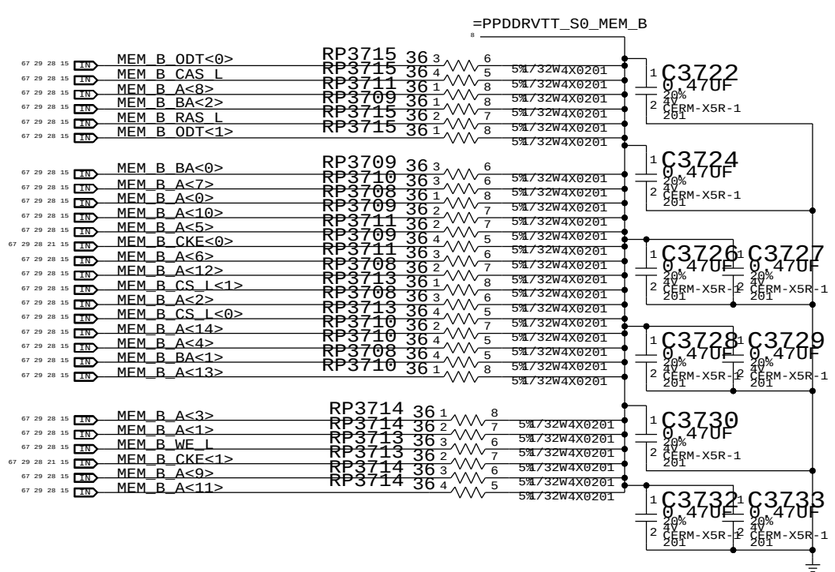
MEM CLOCK TERMINATION

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2016

PAGE TITLE
Memory Active Termination

Apple Inc.

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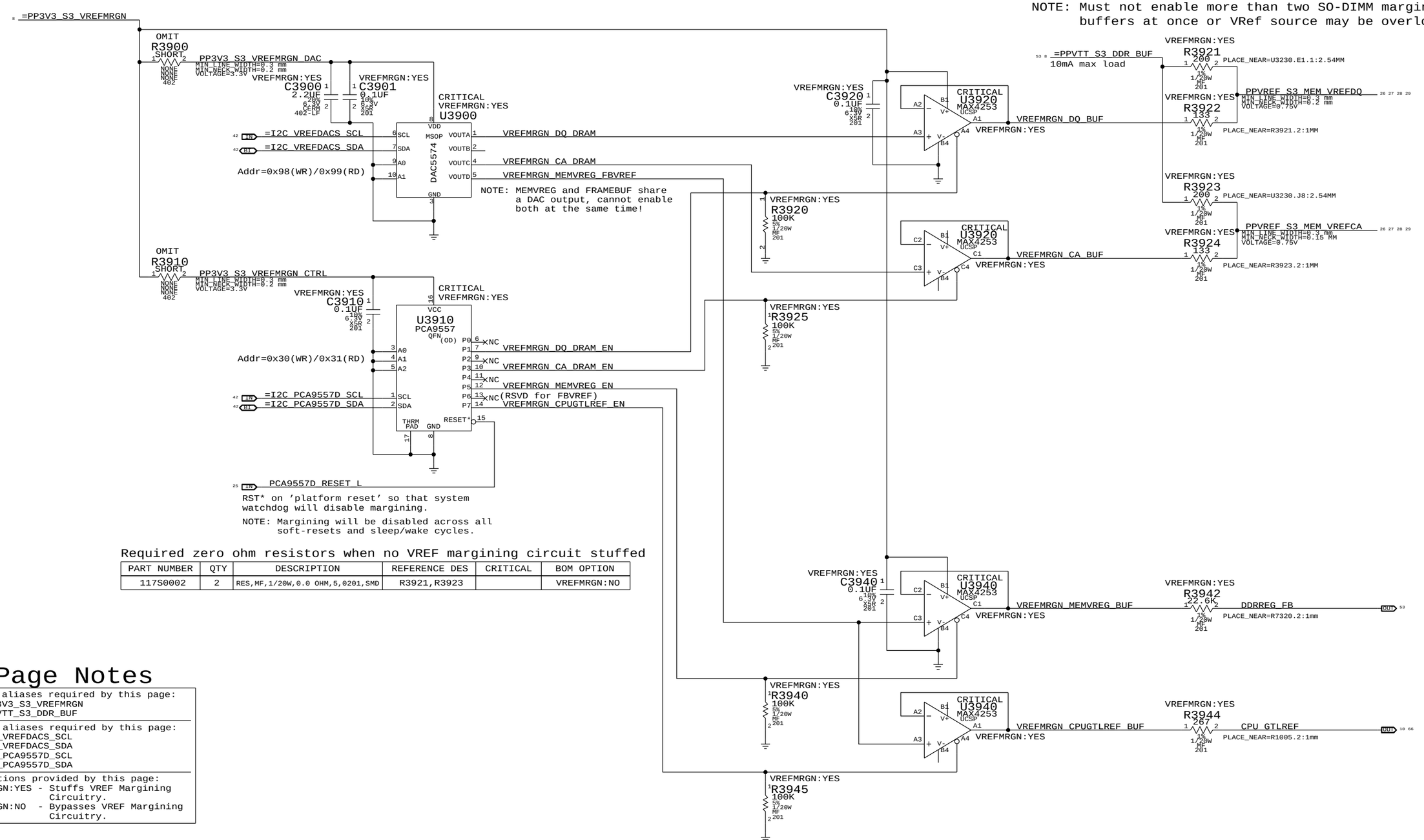

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	2	RES,MF,1/20W,0.0 OHM,5,0201,SMD	R3921,R3923		VREFMRGN:NO

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN:YES - Stuffs VREF Margining Circuitry.
VREFMRGN:NO - Bypasses VREF Margining Circuitry.

	MEM VREF DQ	MEM VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	C	D	D
PCA9557D Pin:	1	3	5	7
Nominal value		0.75V (DAC: 0x3A)	1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)	1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
VRef current:		+3.4mA - -3.4mA (- = sourced)	+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:		7.69mV / step @ output	8.59mV / step @ output	9.24mV / step @ output

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: FSB/DDR3 Vref Margining

Apple Inc.

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AIRPORT

CRITICAL
J4001
SSD-K99
F-RT-SM1

514S0335

WIFI_EVENT_L
PCIE_AP_R2D_N
PCIE_AP_R2D_C_N
PCIE_AP_R2D_P
PCIE_AP_R2D_C_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_AP_D2R_P
PCIE_AP_D2R_N
PCIE_WAKE_L

C4030 0.1UF 10% 6.3V 201X5R
PLACEMENT_NOTE=Place close to J4001.

C4031 0.1UF 10% 6.3V X5R 201
PLACEMENT_NOTE=Place close to J4001.

BLUETOOTH

USB_BT_N
USB_BT_P

=PP3V3_S3_BT

C4032 0.1UF 10% 6.3V X5R 201
PLACE_NEAR=J4001.27:1.5mm

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.750 A (EDP)

CRITICAL
R4052 0.020 1% 0.25W MF 805
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
=PP3V3_WLAN_F
=PP3V3_WLAN_R

CRITICAL
Q4050 TPCP8102 23V1K-SM

C4021 0.1UF 10% 6.3V X5R 201
C4020 10UF 20% 10V X5R 805
PLACEMENT_NOTE=Place close to Q4050.
PLACEMENT_NOTE=Place close to Q4050.

C4051 0.033UF 10% 16V X5R 402
C4050 0.1UF 10% 16V X5R 402
R4050 100K 5% 1/20W MF 201
P3V3WLAN_SS
R4051 10K 5% 1/20W MF 201
=PP3V3_S3_WLAN
PM_WLAN_EN_L

ISNS_AIRPORT_P
ISNS_AIRPORT_N

DLY = 60 MS +/- 20%

C4053 0.1UF 10% 6.3V X5R 201
=PP3V3_S3_WLAN

CRITICAL
U4002
SLG4AP016V
TDFN
VDD
SENSE 0.7V
DLY
RESET*
MR*
EN
IN
OUT (OD)
THRM PAD
GND

R4053 100K 5% 1/20W MF 201
R4054 232K 1% 1/20W MF 201
P3V3WLAN_VMON
AP_RESET_CONN_L
AP_CLKREQ_Q_L

R4055 100K 5% 1/20W MF 201

AP_RESET_L
AP_PWR_EN
AP_CLKREQ_L

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
X21 WIRELESS CONNECTOR

Apple Inc.

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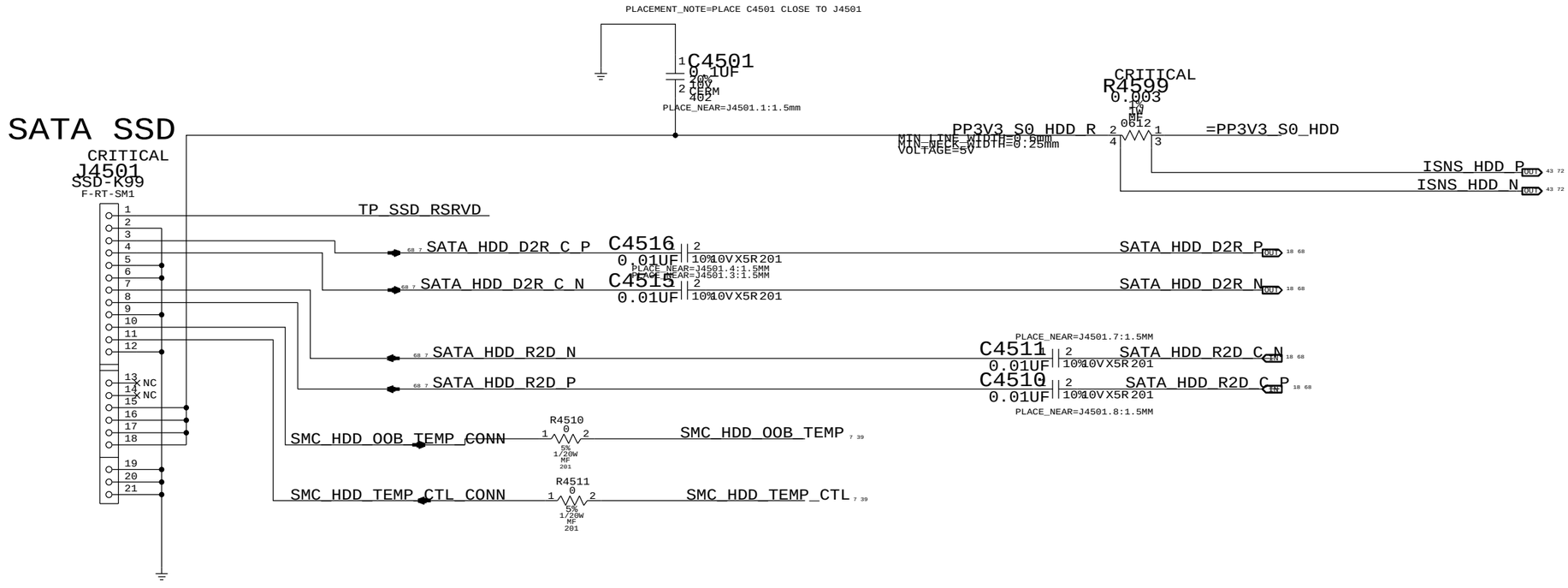

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE

SATA CONNECTOR

Apple Inc.

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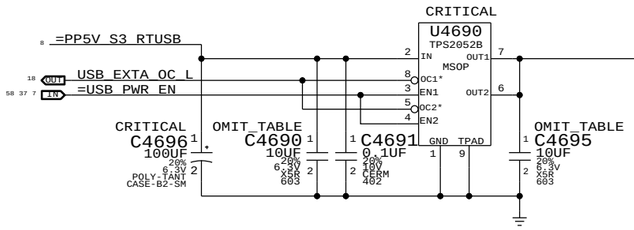
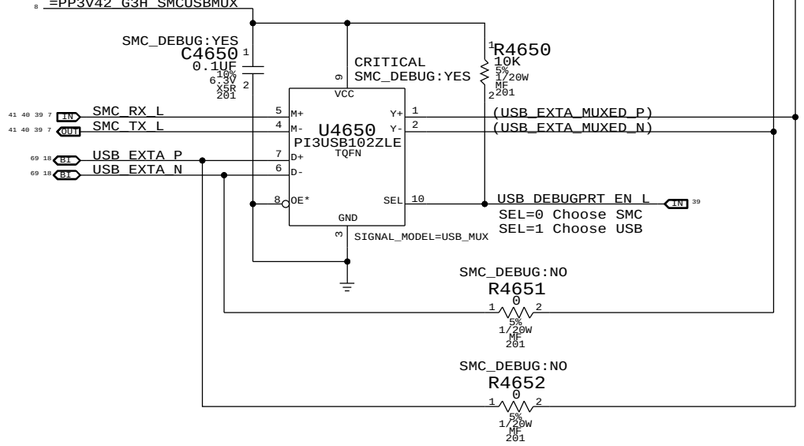
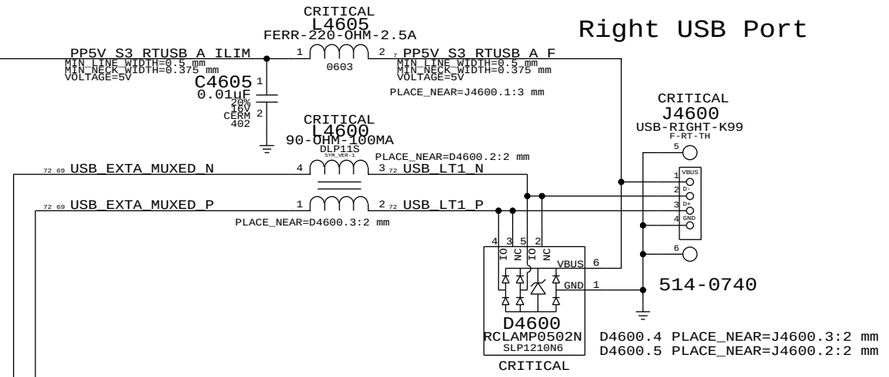
Port Power Switch



USB/SMC Debug Mux



Right USB Port



SYNC_MASTER=K99_MLB	SYNC_DATE=03/01/2010
PAGE TITLE	External USB Connectors
Apple Inc.	DRAWING NUMBER 051-8467 SIZE D
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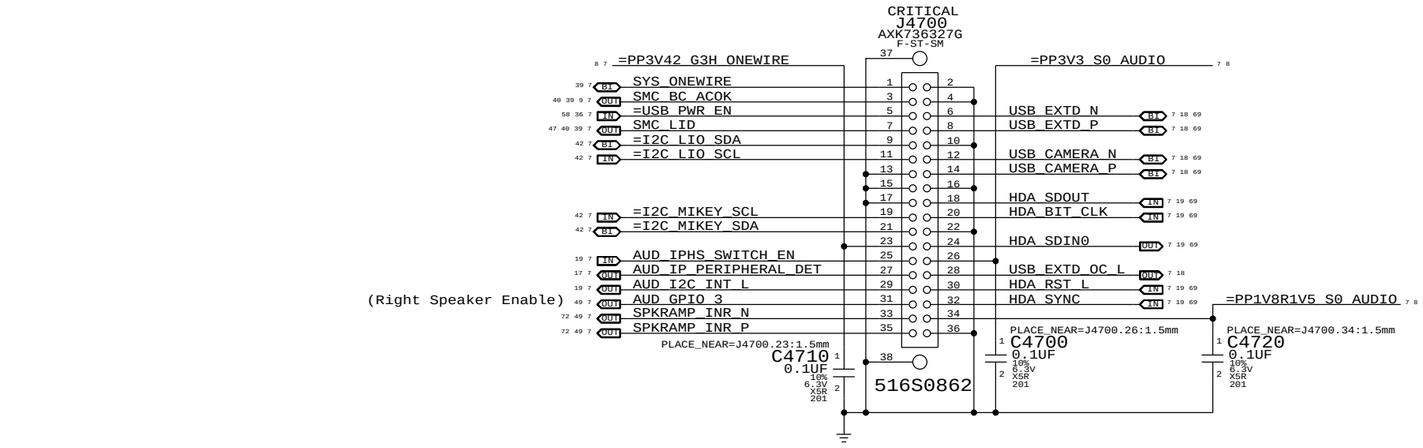

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

PAGE TITLE
Left I/O (LIO) Connector

Apple Inc.

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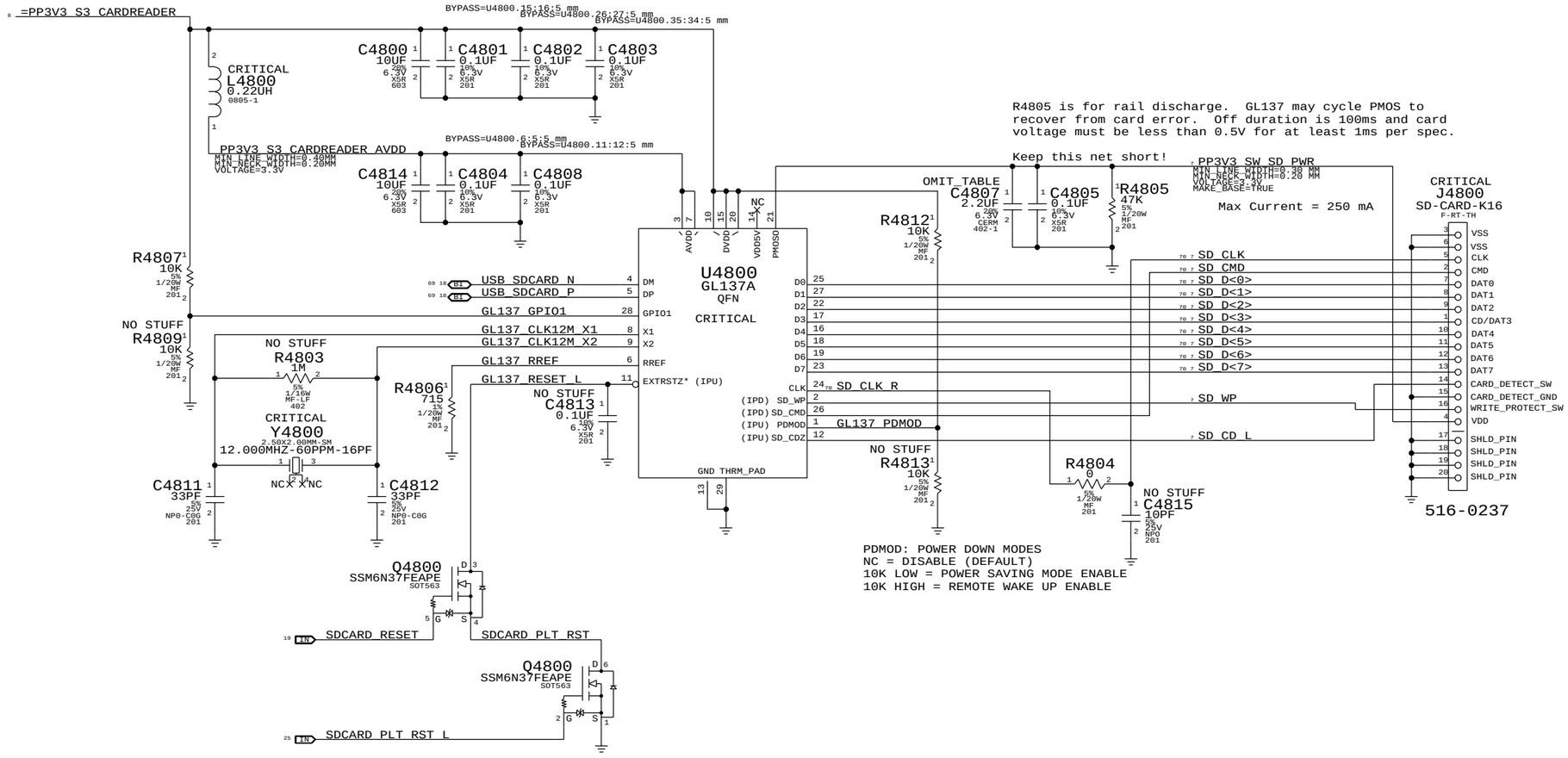

SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
PAGE TITLE	SecureDigital Card Reader
Apple Inc.	DRAWING NUMBER 051-8467 SIZE D
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	BRANCH
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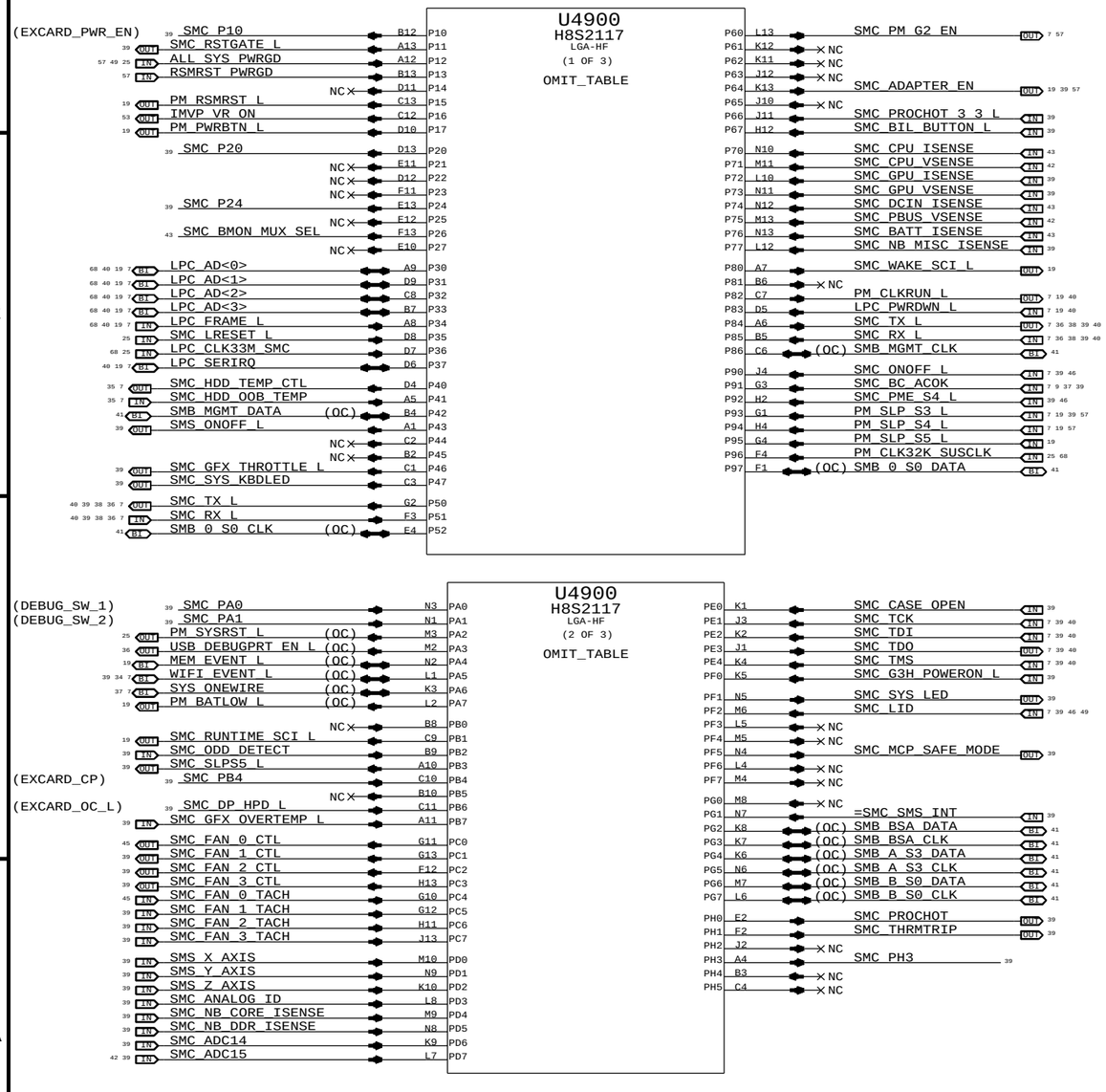
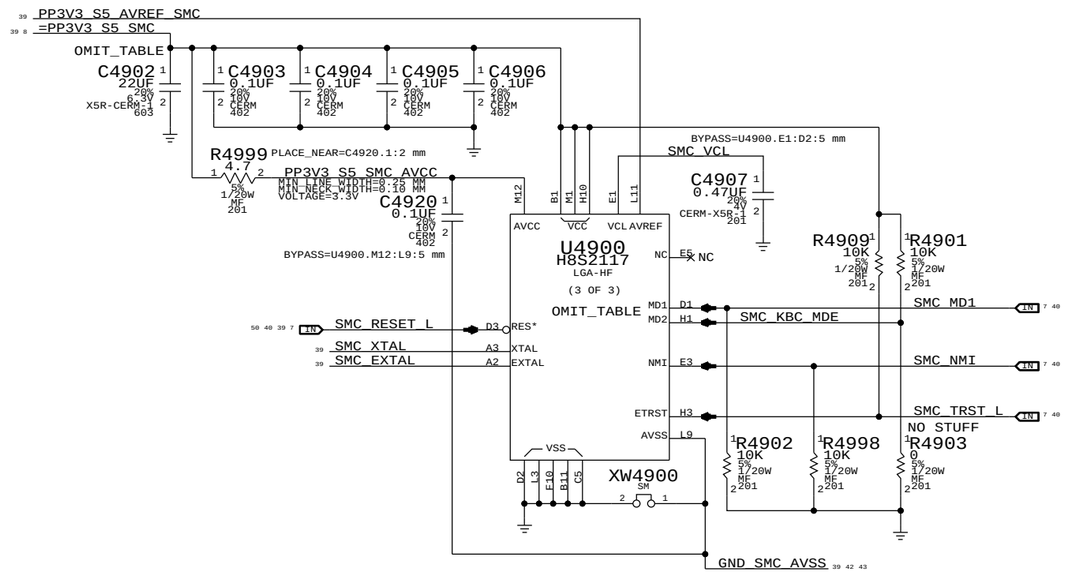
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

H8S2117-R:
(SMC_PECI)
(SMC_PECI_VREF)
(SMC_PECI_VSTP)

SYNC_MASTER=K16_MLB SYNC_DATE=06/01/2010

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D
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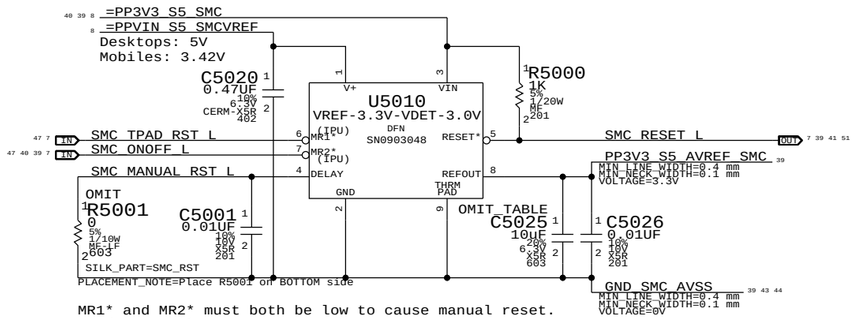
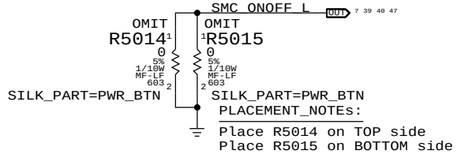
SMC Reset "Button", Supervisor & AVREF Supply



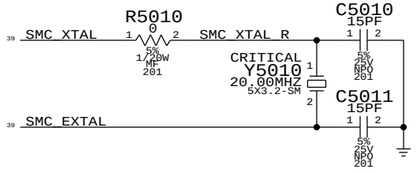
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

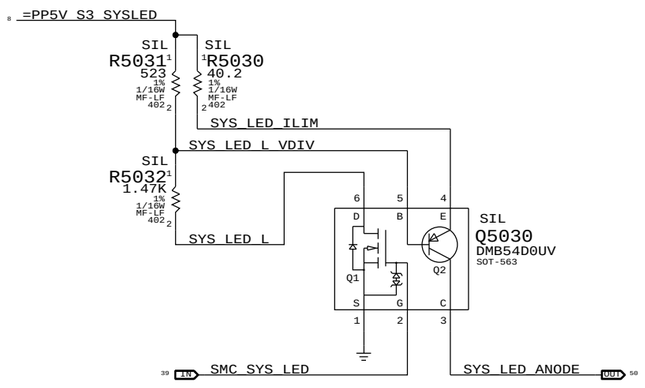
Debug Power "Buttons"



SMC Crystal Circuit



System (Sleep) LED Circuit



SMC Aliases

SMC_LCDBKLT_ISENSE (MAKE_BASE=TRUE)	=	SMS_X_AXIS
SMC_WLAN_ISENSE (MAKE_BASE=TRUE)	=	SMS_Y_AXIS
SMC_HDD_ISENSE (MAKE_BASE=TRUE)	=	SMS_Z_AXIS
SMC_CSREG_ISENSE (MAKE_BASE=TRUE)	=	SMC_ADC14
SMC_LCDBKLT_VSENSE (MAKE_BASE=TRUE)	=	SMC_ADC15
SMC_MCP_CORE_ISENSE (MAKE_BASE=TRUE)	=	SMC_NB_CORE_ISENSE
SMC_MCP_DDR_ISENSE (MAKE_BASE=TRUE)	=	SMC_NB_DDR_ISENSE
SMC_1V5S3_ISENSE (MAKE_BASE=TRUE)	=	SMC_NB_MISC_ISENSE
TP_SMC_ANALOG_ID (MAKE_BASE=TRUE)	=	SMC_ANALOG_ID
TP_SMC_GPU_ISENSE (MAKE_BASE=TRUE)	=	SMC_GPU_ISENSE
SMC_MCP_VSENSE (MAKE_BASE=TRUE)	=	SMC_GPU_VSENSE
SMC_GFX_THROTTLE_L	=	SMC_IG_THROTTLE_L (MAKE_BASE=TRUE)
SMS_INT_L (MAKE_BASE=TRUE)	=	=SMC_SMS_INT
MCP_WAKE_REQ_L	=	SMC_G3H_POWERON_L (MAKE_BASE=TRUE)

R5096 0 5% 1/20W MF 201: SMC_MCP_SAFE_MODE — MCP_SPKR

DP_PWR:S0 R5020 0 5% 1/20W MF 201: PM_SLP_S3_L — DP_PWR_EN (MAKE_BASE=TRUE) = =DP_PWR_EN

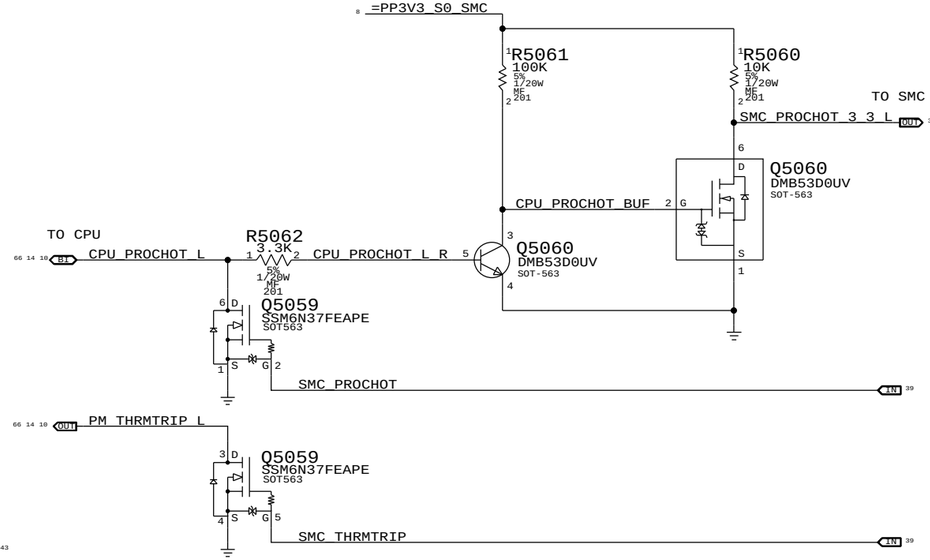
DP_PWR:SMC R5021 0 5% 1/20W MF 201: SMC_SLPS5_L

DP_PWR:SMC R5022 0 5% 1/20W MF 201: SMC_DP_HPD_L — DP_EXT_HPD_L (PLACE_NEAR=Q9441.2:5 mm)

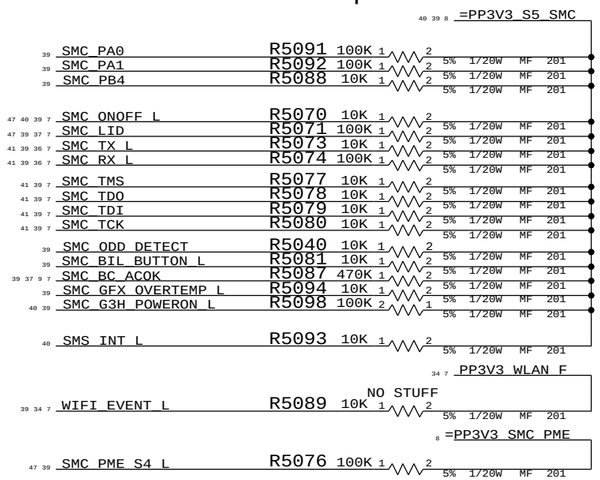
Unused Pins

SMS_ONOFF_L	=	TP_SMS_ONOFF_L (MAKE_BASE=TRUE)
SMC_SYS_KBDLED	=	TP_SMC_SYS_KBDLED (MAKE_BASE=TRUE)
SMC_FAN_1_CTL	=	TP_SMC_FAN_1_CTL (MAKE_BASE=TRUE)
TP_SMC_FAN_1_TACH (MAKE_BASE=TRUE)	=	SMC_FAN_1_TACH
SMC_FAN_2_CTL	=	NC_SMC_FAN_2_CTL (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_SMC_FAN_2_TACH (MAKE_BASE=TRUE, NO_TEST=TRUE)	=	SMC_FAN_2_TACH
SMC_FAN_3_CTL	=	NC_SMC_FAN_3_CTL (MAKE_BASE=TRUE, NO_TEST=TRUE)
NC_SMC_FAN_3_TACH (MAKE_BASE=TRUE, NO_TEST=TRUE)	=	SMC_FAN_3_TACH
SMC_RSTGATE_L	=	TP_SMC_RSTGATE_L (MAKE_BASE=TRUE)
SMC_P10	=	TP_SMC_P10 (MAKE_BASE=TRUE)
SMC_P20	=	TP_SMC_P20 (MAKE_BASE=TRUE)
SMC_P24	=	TP_SMC_P24 (MAKE_BASE=TRUE)
SMC_PH3	=	TP_SMC_PH3 (MAKE_BASE=TRUE)

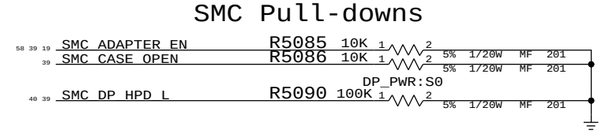
SMC FSB to 3.3V Level Shifting



SMC Pull-ups



SMC Pull-downs



SYNC_MASTER=(K99_MLB) SYNC_DATE=(03/01/2010)

PAGE TITLE: SMC Support

Apple Inc.

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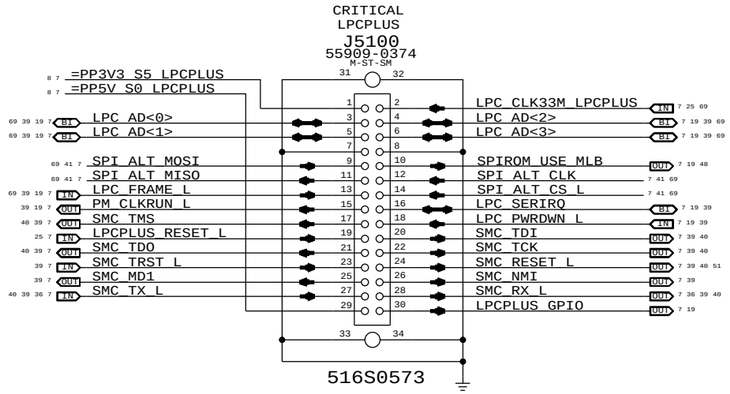
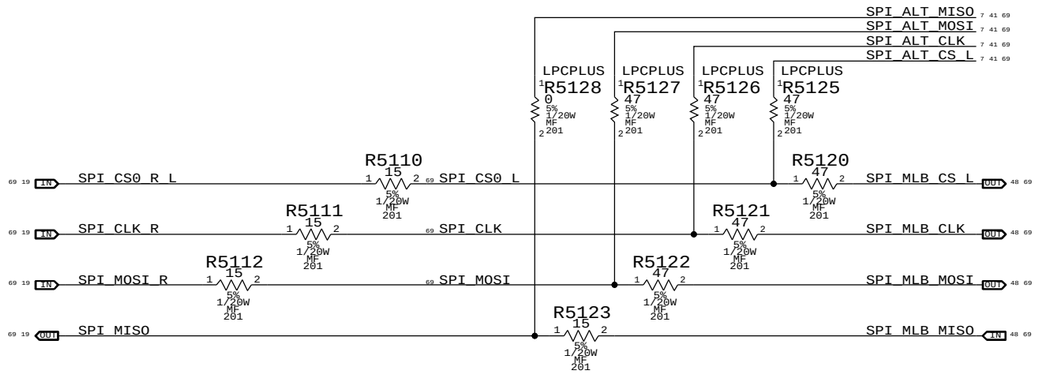
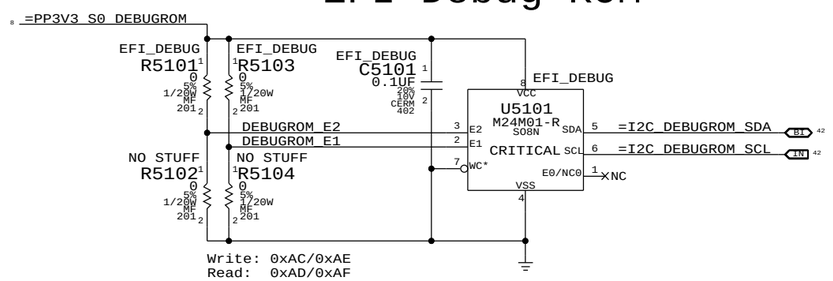
LPC+SPI Connector



SPI Bus Series Termination



EFI Debug ROM



SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

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MCP89 SMBus "0" Connections

=PP3V3_S0_SMBUS_MCP_0

MCP89
U1400
(MASTER)

- SMBUS_MCP_0_CLK (MAKE_BASE=TRUE)
- SMBUS_MCP_0_DATA (MAKE_BASE=TRUE)

R5200 1K 5% 1/20W MF 201
R5201 1K 5% 1/20W MF 201

LP8545 (Bklt)
U9701
(Write: 0x58 Read: 0x59)

- =I2C_BKL_1_SCL
- =I2C_BKL_1_SDA

XDP Connector
J1300
(MASTER)

- =I2C_XDP_SCL
- =I2C_XDP_SDA

DPI2C:MCP
R5241 0 5% 1/20W MF 201

DPI2C:MCP
R5240 0 5% 1/20W MF 201

Vref DACs
U3900
(Write: 0x98 Read: 0x99)

- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA

Margin Control
U3910
(Write: 0x30 Read: 0x31)

- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

EFI Debug Serial
U5101
(Write: 0xAC/0xAE
Read: 0xAD/0xAF)

- =I2C_DEBUGROM_SCL
- =I2C_DEBUGROM_SDA

Mikey
J4700 (LIO Connector)
(Write: 0x72 Read: 0x73)

- =I2C_MIKEY_SCL
- =I2C_MIKEY_SDA

SMC "0" SMBus Connections

=PP3V3_S0_SMBUS_SMC_0_S0

SMC
U4900
(MASTER)

- SMB_0_S0_CLK
- SMB_0_S0_DATA

NO STUFF
R5250 2.0K 5% 1/20W MF 201

NO STUFF
R5251 2.0K 5% 1/20W MF 201

- SMBUS_SMC_0_S0_SCL (MAKE_BASE=TRUE)
- SMBUS_SMC_0_S0_SDA (MAKE_BASE=TRUE)

DPI2C:SMC
R5242 0 5% 1/20W MF 201

DPI2C:SMC
R5243 0 5% 1/20W MF 201

- I2C_TCON_SCL (MAKE_BASE=TRUE)
- I2C_TCON_SDA (MAKE_BASE=TRUE)

Internal DP
J9000
(See Table)

- =I2C_TCON_SCL
- =I2C_TCON_SDA

Internal DP

Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)
Parade T-con - (0x10-0x1F or 0x30-0x3F)
DVR - (Write: 0x4E Read: 0x4F)

(* = Multiple options)

K16		K99		
Samsung	LGD	Samsung	LGD	AUO
N	Y	*	Y	*
Y	N	*	N	*
Y	Y	Y	Y	N

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

=PP3V3_S3_SMBUS_SMC_A_S3

SMC
U4900
(MASTER)

- SMB_A_S3_CLK
- SMB_A_S3_DATA

R5270 1K 5% 1/20W MF 201
R5271 1K 5% 1/20W MF 201

- SMBUS_SMC_A_S3_SCL (MAKE_BASE=TRUE)
- SMBUS_SMC_A_S3_SDA (MAKE_BASE=TRUE)

Left I/O Board
J4700
(See Table)

- =I2C_LIO_SCL
- =I2C_LIO_SDA

Left I/O Board

ALS - N/A (Feature Removed)
Finstack Temp - (Write: 0x98 Read: 0x99)

SMC "Battery A" SMBus Connections

=PP3V42_G3H_SMBUS_SMC_BSA

SMC
U4900
(MASTER)

- SMB_BSA_CLK
- SMB_BSA_DATA

R5280 2.61K 1% 1/20W MF 201
R5281 2.61K 1% 1/20W MF 201

- SMBUS_SMC_BSA_SCL (MAKE_BASE=TRUE)
- SMBUS_SMC_BSA_SDA (MAKE_BASE=TRUE)

Battery Charger
ISL6259 - U7000
(Write: 0x12 Read: 0x13)

- =SMBUS_CHGR_SCL
- =SMBUS_CHGR_SDA

Battery
J6950
(See Table)

- =SMBUS_BATT_SCL
- =SMBUS_BATT_SDA

Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

=PP3V3_S5_SMBUS_SMC_MGMT

SMC
U4900
(MASTER)

- SMB_MGMT_CLK
- SMB_MGMT_DATA

R5290 2.0K 5% 1/20W MF 201
R5291 2.0K 5% 1/20W MF 201

- SMBUS_SMC_MGMT_SCL (MAKE_BASE=TRUE)
- SMBUS_SMC_MGMT_SDA (MAKE_BASE=TRUE)

Trackpad
J5700
(Write: 0x90 Read: 0x91)

- =I2C_TPAD_SCL
- =I2C_TPAD_SDA

MCP89 SMBus "1" Connections

=PP3V3_S0_SMBUS_MCP_1

MCP89
U1400
(Write: 0xE0 Read: 0xE1)

- SMBUS_MCP_1_CLK (MAKE_BASE=TRUE)
- SMBUS_MCP_1_DATA (MAKE_BASE=TRUE)

NO STUFF
R5230 2.0K 5% 1/20W MF 201

NO STUFF
R5231 2.0K 5% 1/20W MF 201

R5235 0 5% 1/20W MF 201

R5236 0 5% 1/20W MF 201

MCP89 SMBus 1 is slave port to access internal thermal diodes.

Another slave port is available at 0x10/0x11, probably not used.

SMC "B" SMBus Connections

=PP3V3_S0_SMBUS_SMC_B_S0

SMC
U4900
(MASTER)

- SMB_B_S0_CLK
- SMB_B_S0_DATA

R5260 4.7K 5% 1/20W MF 201
R5261 4.7K 5% 1/20W MF 201

- SMBUS_SMC_B_S0_SCL (MAKE_BASE=TRUE)
- SMBUS_SMC_B_S0_SDA (MAKE_BASE=TRUE)

CPU Temp
EMC1413: U5515
(Write: 0x98 Read: 0x99)

- =I2C_CPUTHMSNS_SCL
- =I2C_CPUTHMSNS_SDA

MCP Temp
EMC1413: U5535
(Write: 0xD8 Read: 0xD9)

- =I2C_MCPTHMSNS_SCL
- =I2C_MCPTHMSNS_SDA

SYNC_MASTER=K99_MLB SYNC_DATE=07/23/2010

PAGE TITLE
K16/K99 SMus Connections

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DRAWING NUMBER 051-8467 SIZE D
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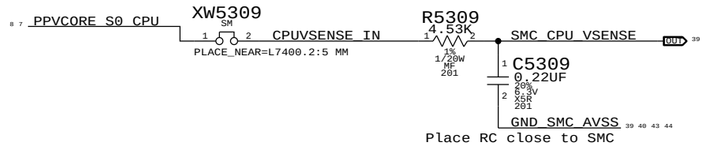
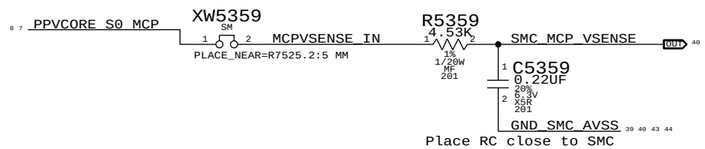
CPU Voltage Sense / Filter



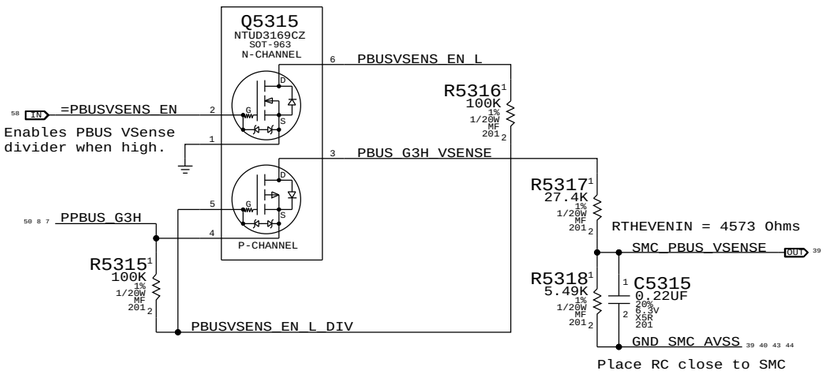
Place RC close to SMC

MCP Voltage Sense / Filter

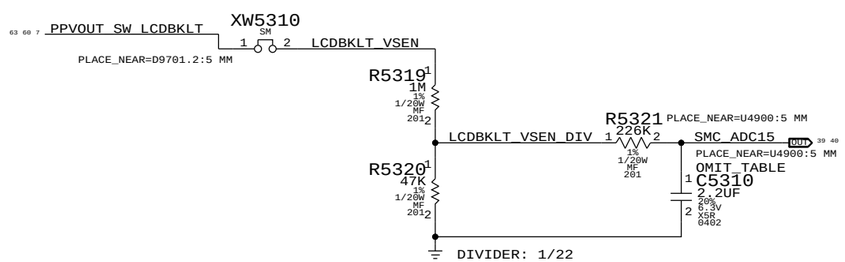


Place RC close to SMC

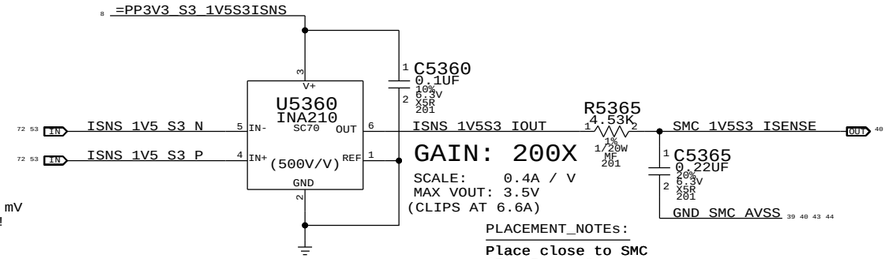
PBUS Voltage Sense Enable & Filter



Place RC close to SMC

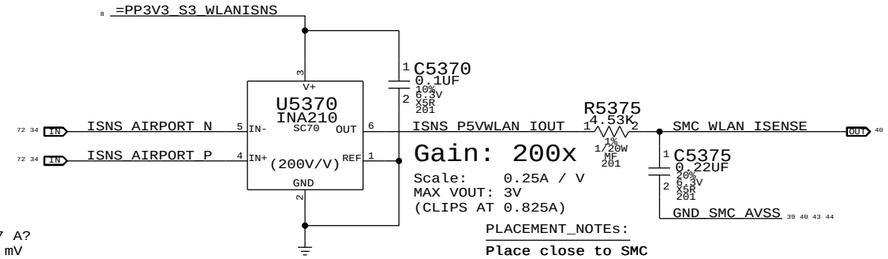


DDR3 1V5R1V35 Current Sense / Filter



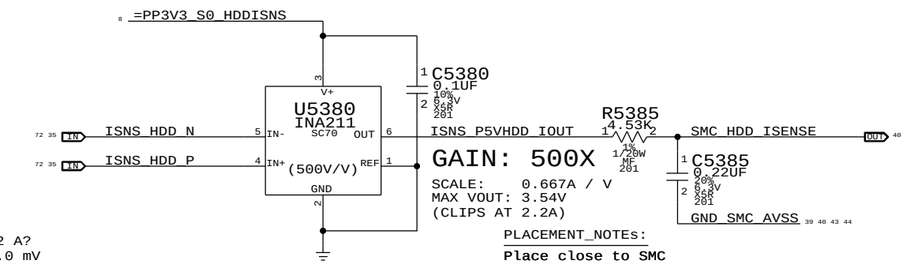
EDP Current: 7 A
Max Vdiff: 13.0 mV
WF: Verify SO-DIMM current!

AirPort Current Sense / Filter



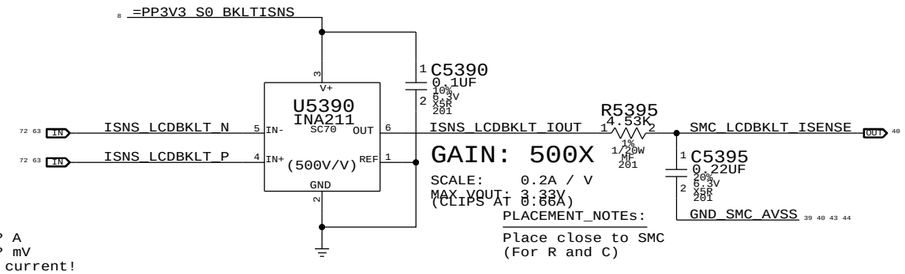
EDP Current: 0.727 A?
Max Vdiff: 14.6 mV
WF: Verify Airport current!

HDD Current Sense / Filter



EDP Current: 1.2 A?
Max Vdiff: 24.0 mV
WF: Verify SSD current!

LCD Backlight Driver Input Current Sense / Filter



EDP Current: ??? A
Max Vdiff: ??? mV
WF: Verify LCD backlight current!

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
Voltage & Current Sensing

Apple Inc.

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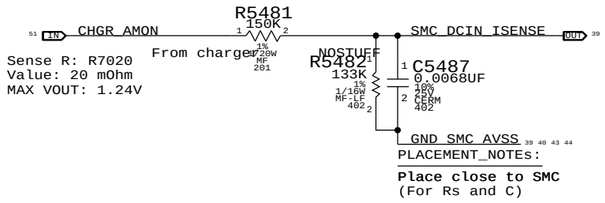
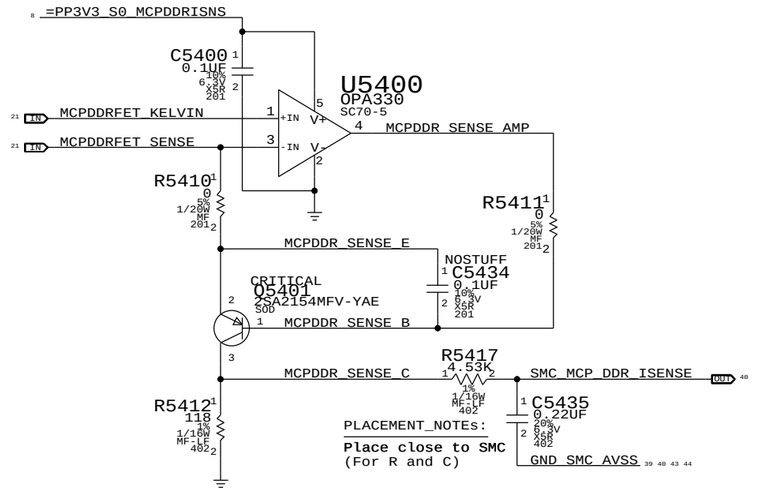
DCIN (AMON) Current Sense, RMUX & Filter

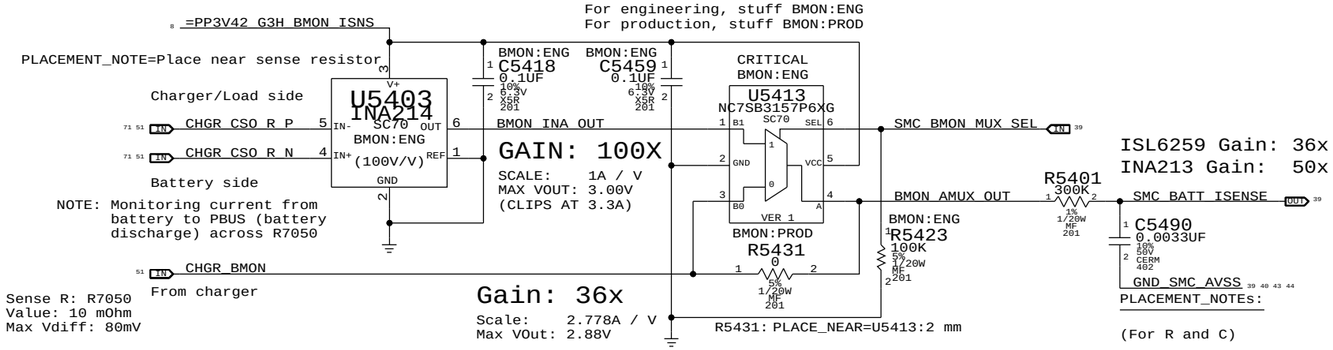
ISL6259 Gain: 20x



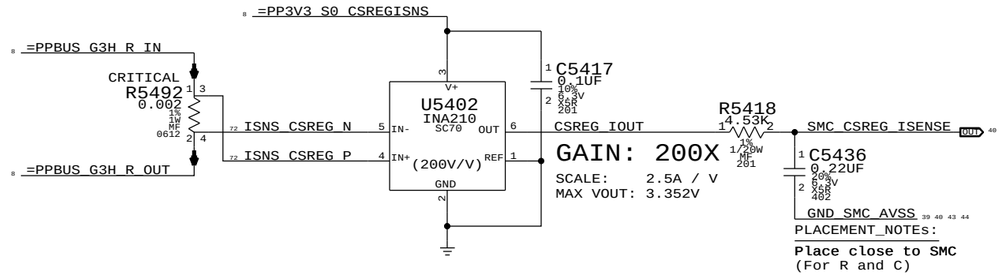
MCP MEM VDD Current Sense / Filter



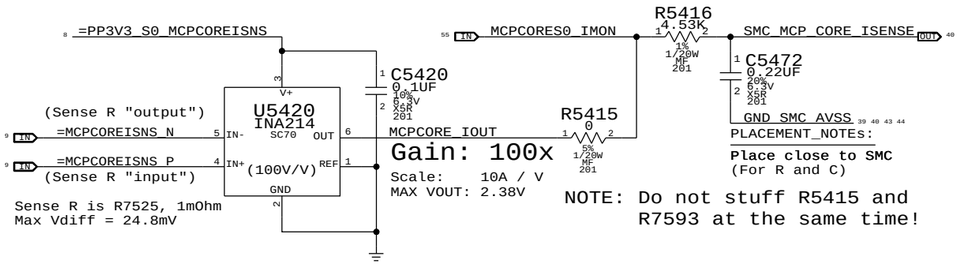
Battery (BMON) Current Sense, MUX & Filter



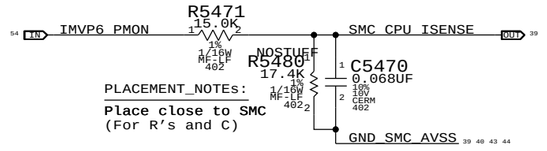
Chipset Regulators High-Side Current Sense / Filter



MCP VCore Current Sense Filter



CPU VCore Load Side Current Sense / Filter



VERIFY ALL RESISTOR AND GAINS

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: Current Sensing

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

BRANCH:

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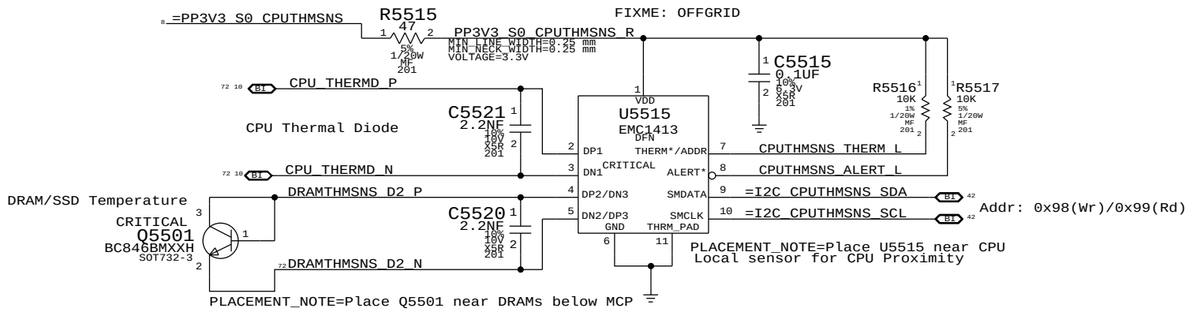
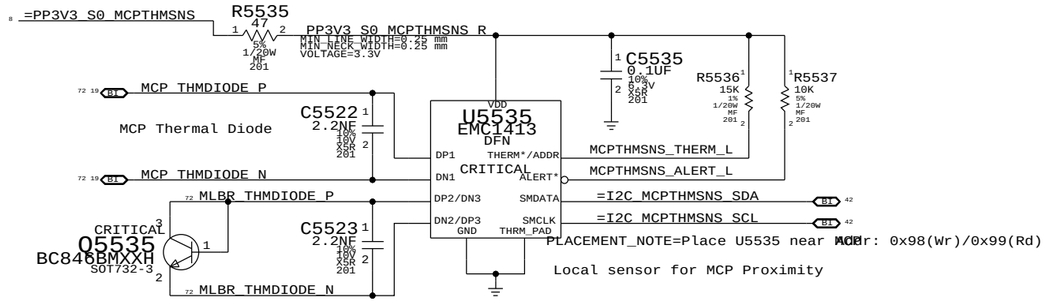
CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

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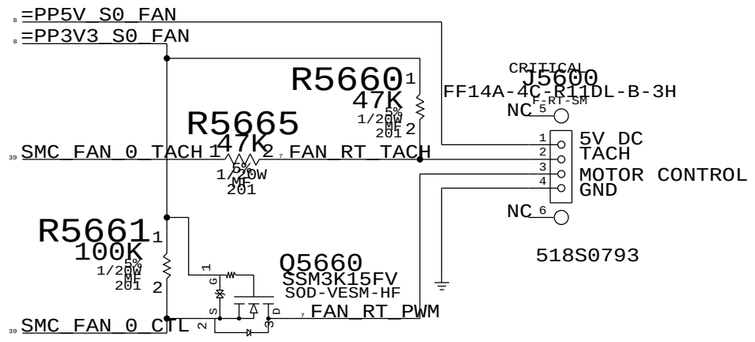
FAN CONNECTOR



SYNC_MASTER=K99_MLB	SYNC_DATE=04/08/2010
PAGE TITLE: Fan	
Apple Inc.	DRAWING NUMBER: 051-8467 SIZE: D
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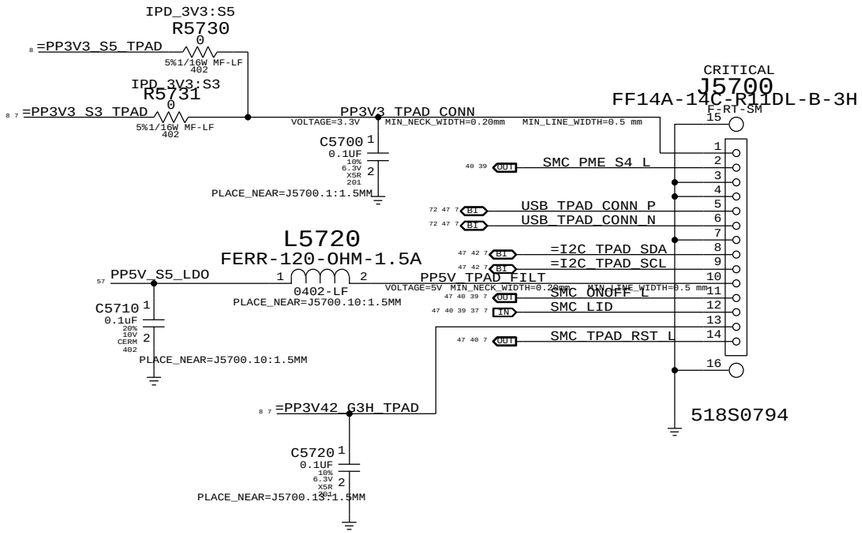
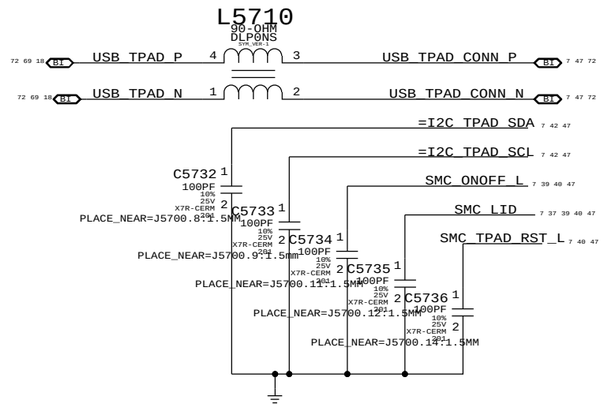
IPD Flex Connector





SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: WELLSPRING 1

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

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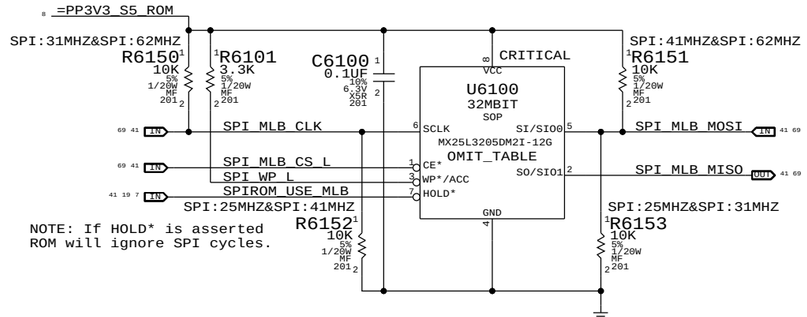

MCP89 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command.

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: SPI ROM

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

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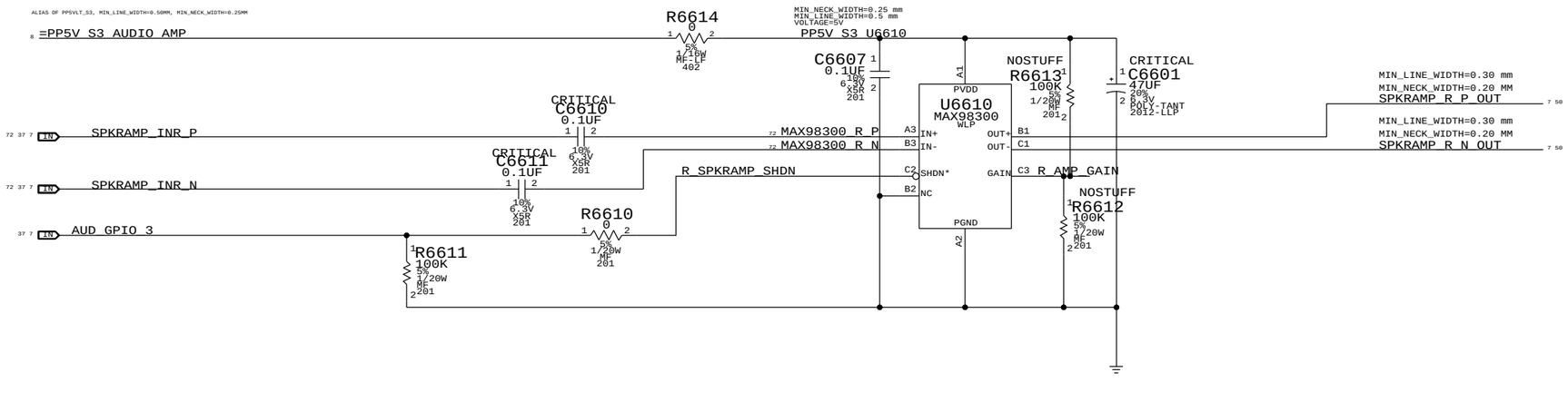
SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ

GAIN 6DB



SYNC_MASTER=K99_MLB	SYNC_DATE=04/08/2010
PAGE TITLE: AUDI0: SPEAKER AMP	
Apple Inc.	DRAWING NUMBER: 051-8467 SIZE: D
	REVISION: 3.3.0
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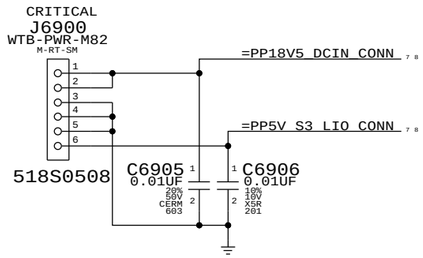
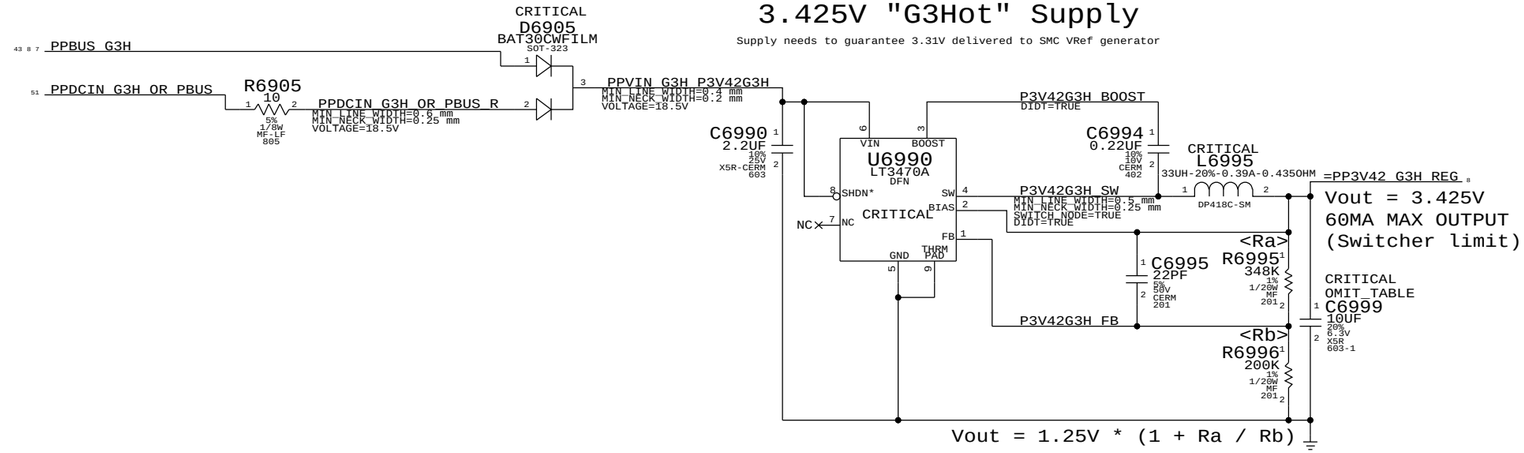
MLB to LIO Power Cable Connector



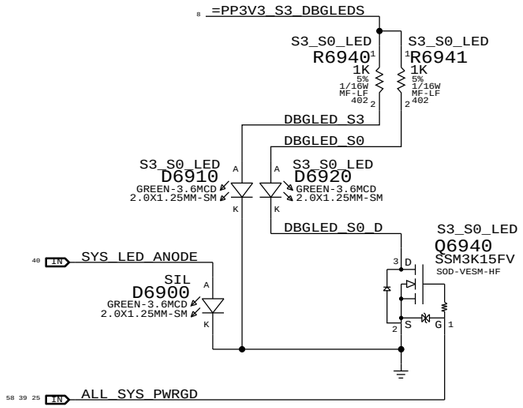
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

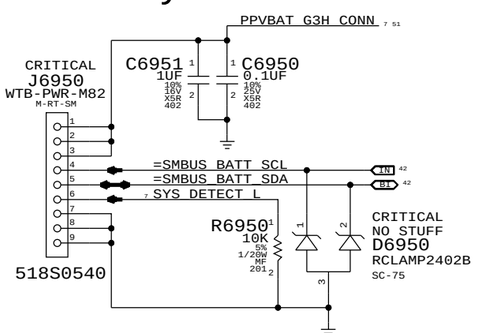


Debug LEDs

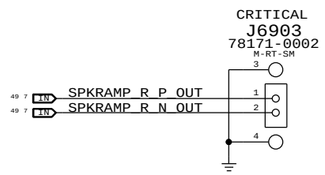
(For development only)



K16-Specific Battery Connector



Right Speaker Connector



SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

PAGE TITLE: DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

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Reverse-Current Protection

This node is powered through body diodes:
* DCIN through Q7080.
* PBUS through Q7085, Charger TOP FETs and Q7055.

Inrush Limiter

FROM ADAPTER
=PPDCIN_S5_CHGR

CRITICAL Q7080 SI5419DU POWERPAK

R7080 100K 5% 1/20W MF 201

PPDCIN_G3H_OR_PBUS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V

C7085 0.1UF 10% 25V X5R 402

R7085 470K 1% 1/20W MF 201

CRITICAL Q7085 SI5419DU POWERPAK

PPDCIN_G3H_INRUSH
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

CHGR_SGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.25 mm

R7081 62K 5% 1/20W MF 201

CHGR_AGATE_DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.25 mm

R7086 332K 1% 1/20W MF 201

CRITICAL D7005 BAT30CWFILM SOT-323

R7005 20 5% 1/20W MF 201

CHGR_DCIN_D_R

(CHGR_SGATE)
(CHGR_AGATE)
(CHGR_DCIN)

ACIN pin threshold is 3.2V, +/- 50mV
DIVIDER SETS ACIN THRESHOLD AT 12.18V
Input impedance of ~40K meets sparkitecture requirements

30mA max load

PP5V1_CHGR_VDD
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=5.1V

R7001 4.7 5% 1/16W MF-LF 402

PP5V1_CHGR_VDDP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V

=PP3V42_G3H_CHGR

C7001 1UF 10% 10V X5R 402

R7010 30.1K 1% 1/20W MF 201

NO STUFF
R7002 100K 5% 1/20W MF 201

CRITICAL OMIT_TABLE

R7000 0 5% 1/20W MF 201

SMC_RESET_L
CHGR_RST_L
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA
CHGR_VFRQ
CHGR_CELL

Float CELL for 1S

CHGR_ACIN
CHGR_ICOMP
CHGR_VCOMP
CHGR_VNEG
CHGR_CSO_P
CHGR_CSO_N

U7000 ISL6259HRTZ TQFN

12	VHST	DCIN	2 CHGR_DCIN
13	SMB_RST_N	SGATE	26 CHGR_SGATE
11	SCL	AGATE	1 CHGR_AGATE
10	SDA	CSIP	28 CHGR_CSI_P
4	VFRQ	CSIN	27 CHGR_CSI_N
6	CELL	BOOT	25 CHGR_BOOT
3	ACIN	UGATE	24 CHGR_UGATE
5	ICOMP	PHASE	23 CHGR_PHASE
7	VCOMP	LGATE	21 CHGR_LGATE
8	VNEG	BGATE	16 CHGR_BGATE
18	CSOP	20V/V AMON	9 CHGR_AMON
17	CSON	36V/V BMON	15 CHGR_BMON
		(0D) ACOK	14 =CHGR_ACOK
	(AGND) THRM_PAD		29
	PGND		22

R7013 100 1% 1/20W MF 201

R7015 220K 5% 1/20W MF 201

R7011 10.5K 1% 1/20W MF 201

CHGR_VCOMP_R

C7050 0.47UF 10% 10V X5R 402

C7015 470PF 10% 10V X5R-X7R 201

R7016 3.01K 1% 1/20W MF 201

CHGR_VNEG_R

C7016 470PF 10% 10V X5R-X7R 201

C7002 1UF 10% 10V X5R 402

XW7000 SM

(GND)

PLACE_NEAR=U7000.29:1mm
PLACE_NEAR=U7000.22:1mm

C7042 0.1UF 10% 6.3V X5R 201

C7011 0.01UF 10% 10V X5R 201

C7000 1UF 10% 10V X5R 402-1

C7005 0.22UF 20% 25V X5R 603

C7026 1000PF 10% 16V X7R 201

GND_CHGR_AGND
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V

R7021 10 5% 1/20W MF 201

C7020 0.047UF 10% 16V X7R 402

R7022 10 5% 1/20W MF 201

C7022 0.1UF 10% 25V X5R 402

C7021 0.1UF 10% 25V X5R 402

CHGR_CSI_R_P
CHGR_CSI_R_N

CRITICAL R7020 0.020 9.5% 1W MF-LF 0612

PPDCIN_G3H_CHGR
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=18.5V

CRITICAL C7030 33UF-0.060HM 20% 25V POLY-TANT CASE-D3L

CRITICAL C7031 33UF-0.060HM 20% 25V POLY-TANT CASE-D3L

C7035 1UF 10% 25V X5R 603-1

C7036 1UF 10% 25V X5R 603-1

C7037 0.001UF 10% 50V X7R 402

PLACE_NEAR=Q7030.5:1.5mm

CRITICAL Q7030 RJK0332DPB-01 LFPAK-SM

C7025 0.22UF 10% 16V CERM 402

Max Current = 8A

f = 400 kHz

CRITICAL L7030 4.7UH-7.5A IHLP4040CZ-SM

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL F7040 7AMP-24V 1206-1

TO SYSTEM
=PPBUS_G3H

CRITICAL Q7035 RJK0305DPB LFPAK-HF

PPVBAT_G3H_CHGR_REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=8.4V

CRITICAL C7040 62UF 20% 11V ELEC CASE-B2

CRITICAL C7041 62UF 20% 11V ELEC CASE-B2

CRITICAL C7043 62UF 20% 11V ELEC CASE-B2

C7045 1000PF 10% 16V X7R 201

PLACE_NEAR=L7030.2:1.5mm

R7050 0.01 0.5% 1W MF 0612-3

R7051 2.2 5% 1/20W MF 201

R7052 0 5% 1/20W MF 201

CHGR_CSO_R_P
CHGR_CSO_R_N

PPVBAT_G3H_CHGR_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=8.4V

CRITICAL Q7055 SI7615DN PWRPK-1212-8

TO/FROM BATTERY
PPVBAT_G3H_CONN
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=8.4V

(PPVBAT_G3H_CHGR_R)
(CHGR_BGATE)

C7017 10UF 10% 25V X5R 805

C7014 1UF 10% 25V X5R 603-1

C7013 0.1UF 10% 25V X5R 402

C7012 0.01UF 10% 25V X7R 402

* R7051 HAS 2.2OHM TO COMPENSATE UNVALANCED VOLTAGE DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)

SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/16/2010)

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

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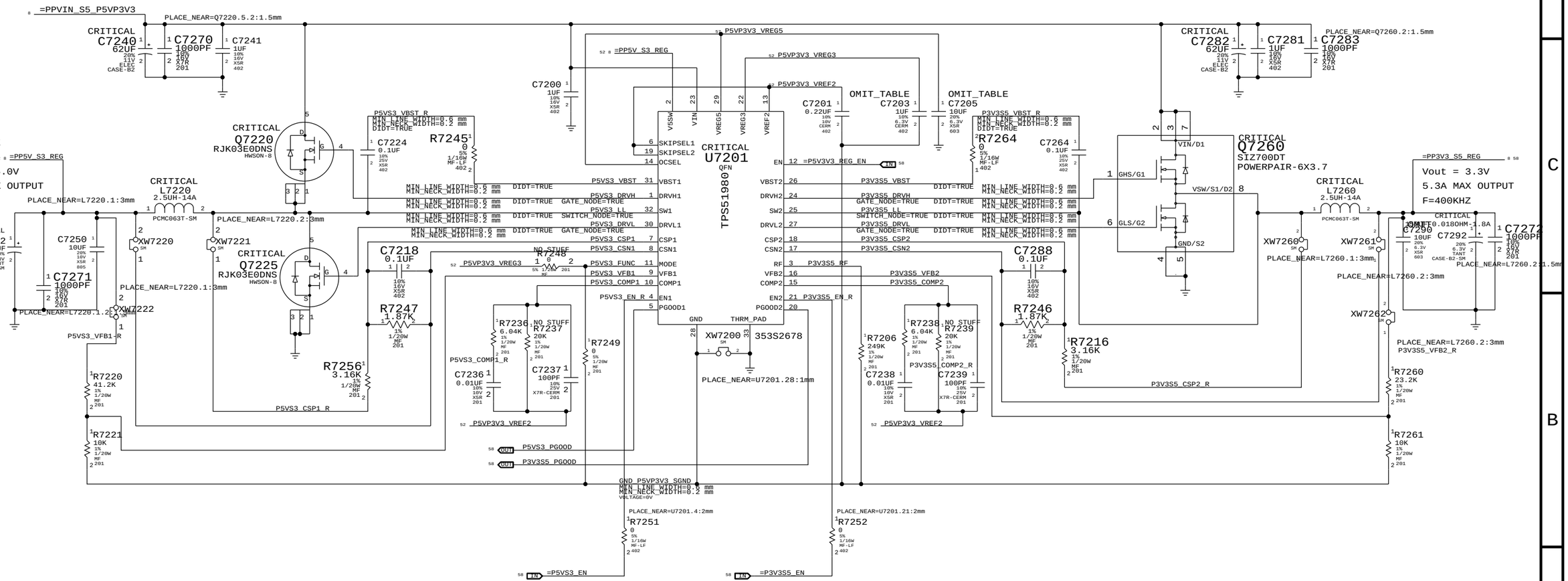

SYNC_MASTER=K99_MLB	SYNC_DATE=04/08/2016
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER 051-8467 · SIZE D
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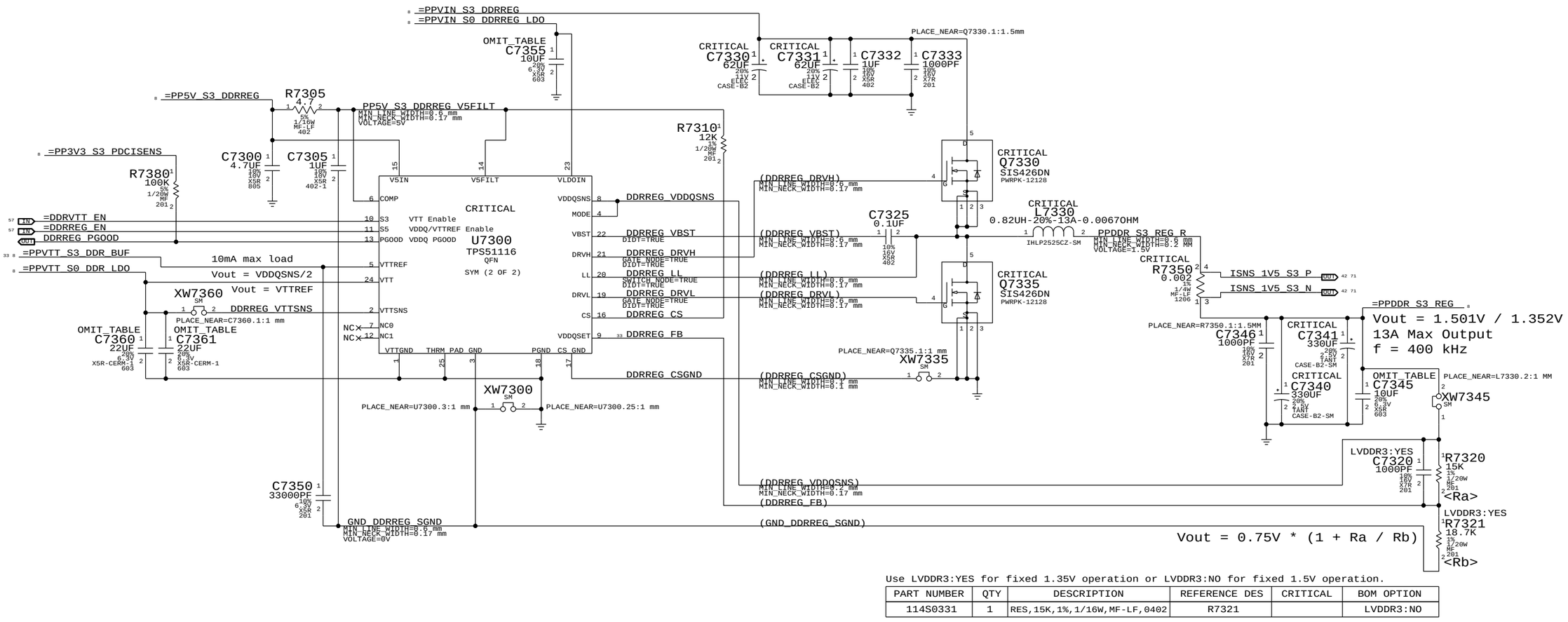

Use LVDDR3:YES for fixed 1.35V operation or LVDDR3:NO for fixed 1.5V operation.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0331	1	RES,15K,1%,1/16W,MF-LF,0402	R7321		LVDDR3:NO

SYNC_MASTER=K16_MLB SYNC_DATE=06/01/2010

PAGE TITLE: 1.5V/1.35V LVDDR3 Supply

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

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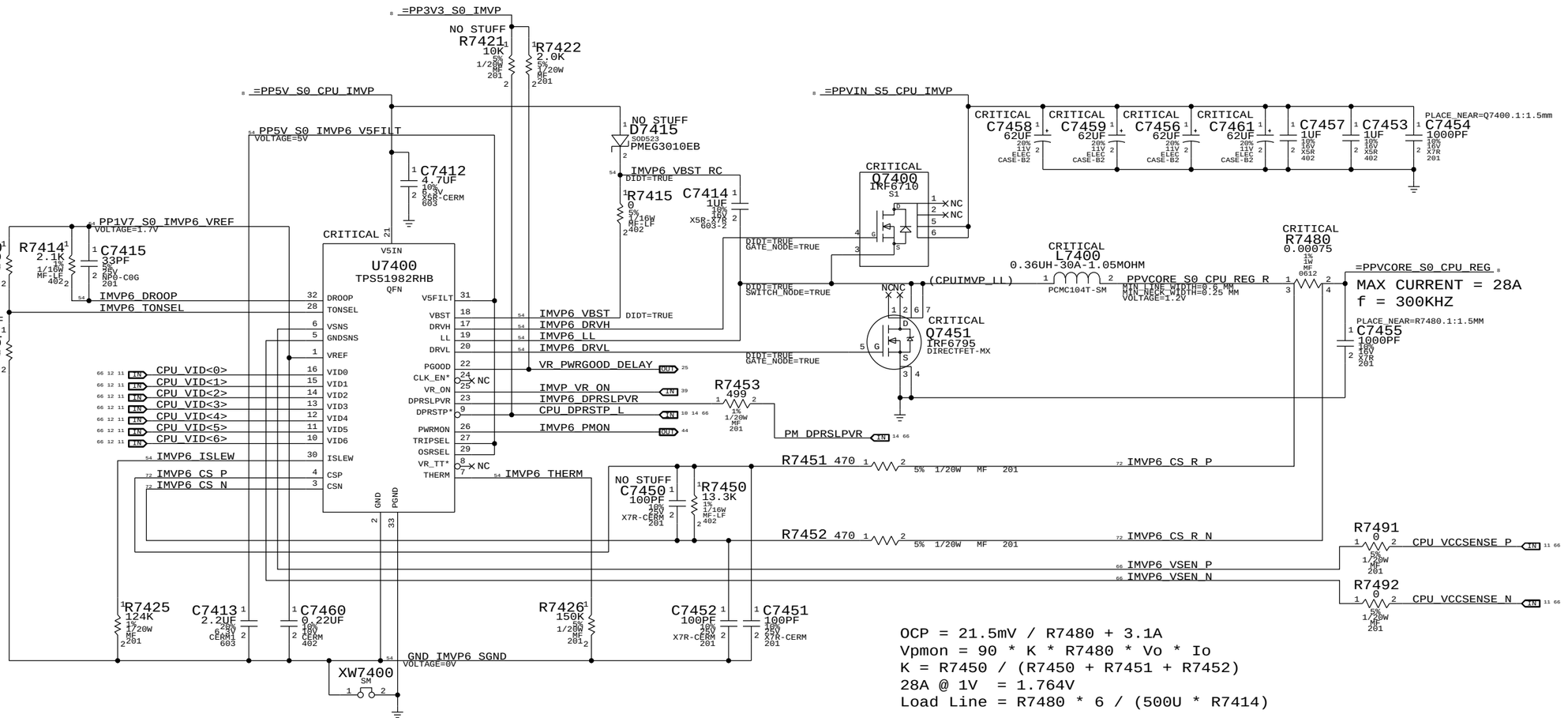

OCP = 21.5mV / R7480 + 3.1A
Vpmon = 90 * K * R7480 * Vo * Io
K = R7450 / (R7450 + R7451 + R7452)
28A @ 1V = 1.764V
Load Line = R7480 * 6 / (500U * R7414)

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_THERM	0.25 MM	0.20 MM
IMVP6_ISLEW	0.25 MM	0.20 MM
PP1V7_S0_IMVP6_VREF	0.25 MM	0.20 MM
PP5V_S0_IMVP6_V5FILT	0.25 MM	0.20 MM
IMVP6_LL	1.5 MM	0.20 MM
IMVP6_VBST	0.25 MM	0.20 MM
IMVP6_DRVH	1.5 MM	0.20 MM
IMVP6_DRVL	1.5 MM	0.20 MM
IMVP6_VBST_RC	1.5 MM	0.20 MM

SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/16/2010)

PAGE TITLE: IMVP6 CPU VCore Regulator

Apple Inc.

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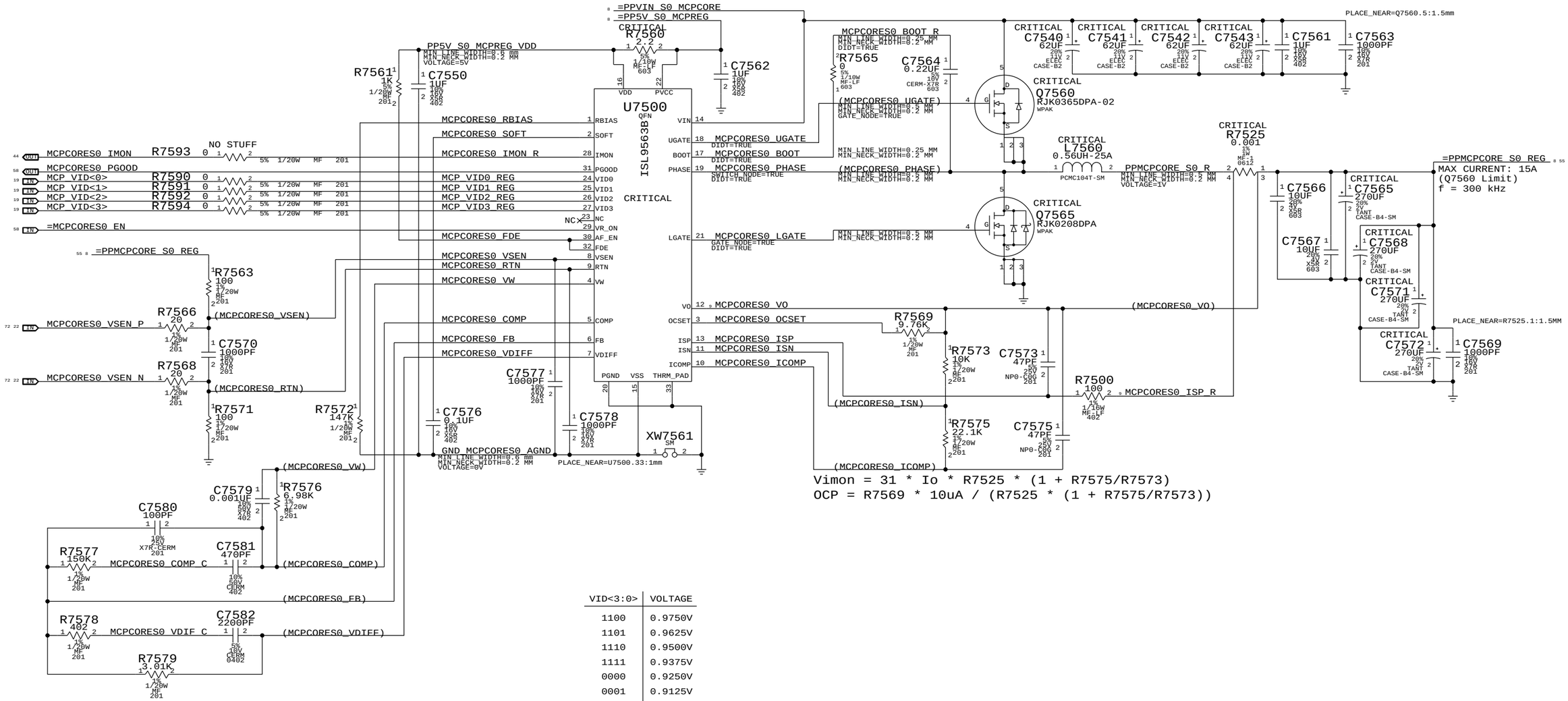


VID<3:0>	VOLTAGE
1100	0.9750V
1101	0.9625V
1110	0.9500V
1111	0.9375V
0000	0.9250V
0001	0.9125V
0010	0.9000V
0011	0.8875V
0100	0.8750V
0101	0.8625V
0110	0.8500V
0111	0.8375V
1000	0.8250V
1001	0.8125V
1010	0.8000V
1011	0.7875V

K6 NOTES : XOR AND INVERTER IS REMOVED, CANNOT SYNC THIS PAGE FROM T27

SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/11/2010)

PAGE TITLE: MCP VCore Regulator

Apple Inc.

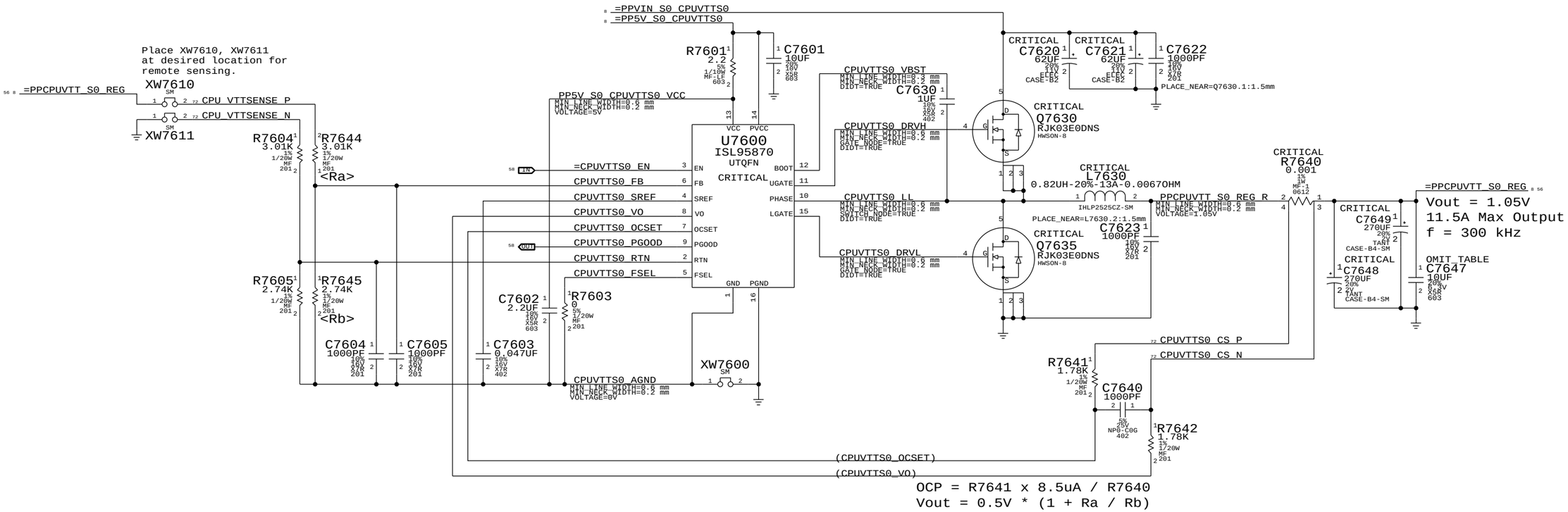
DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

BRANCH:

PAGE: 75 OF 110

SHEET: 55 OF 74



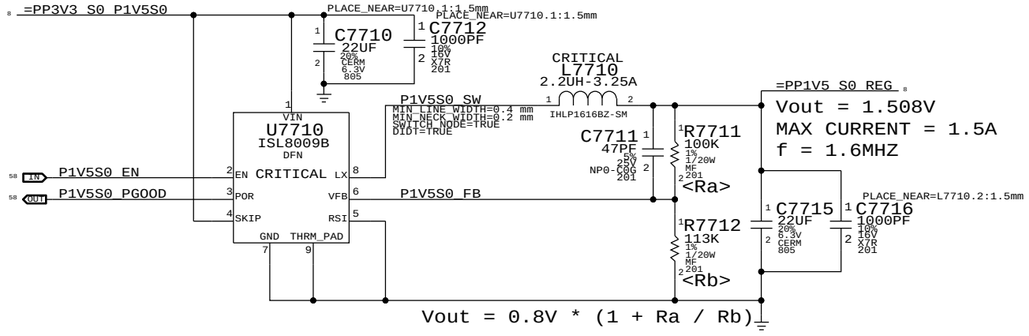
SYNC_MASTER=(K99_MLB) SYNC_DATE=(03/01/2010)

PAGE TITLE
CPUVTT (1.05V) Power Supply

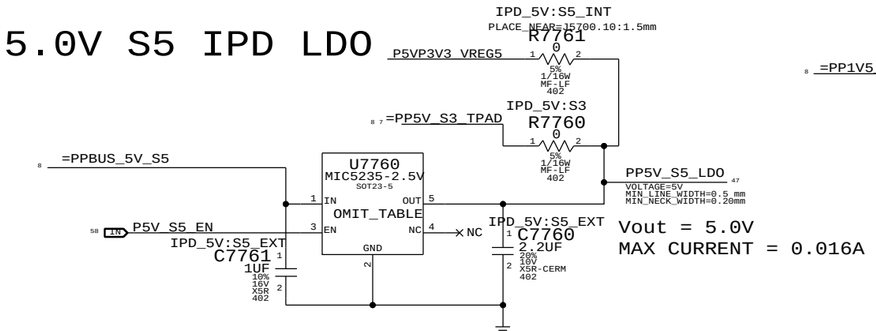
Apple Inc.

DRAWING NUMBER 051-8467 | SIZE D
REVISION 3.3.0
BRANCH
PAGE 76 OF 110
SHEET 56 OF 74

1.5V S0 Regulator

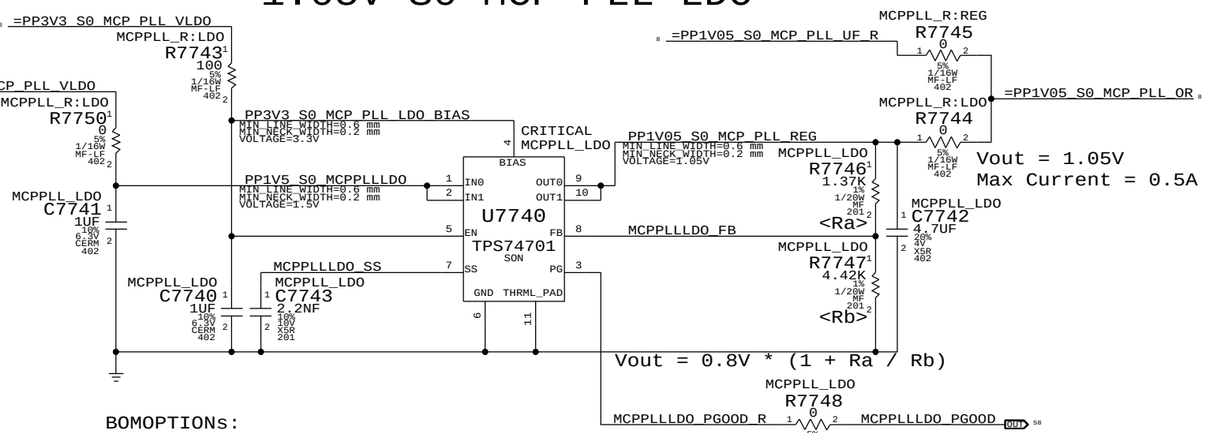


5.0V S5 IPD LDO



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3034	1	IC,LDO,MIC5235,5V,1%,150MA,SOT23-5	U7760		IPD_5V:S5_EXT

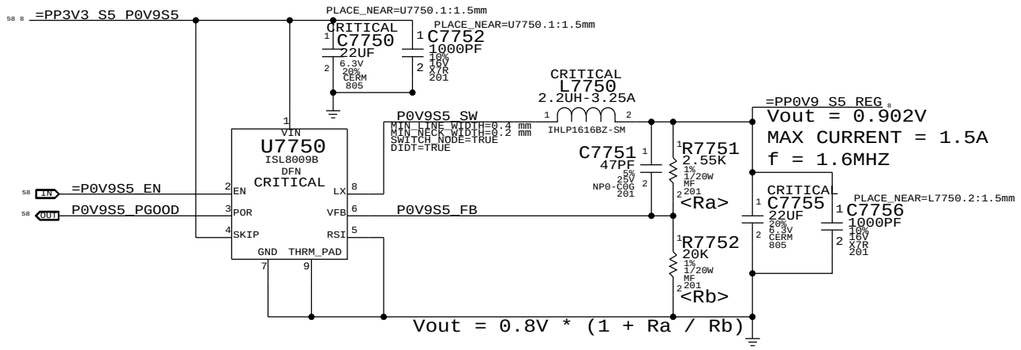
1.05V S0 MCP PLL LDO



BOMOPTIONs:

MCPPLL_R:LDO - 1.05V S0 USED FOR MCP PLL LDO POWER.
MCPPLL_LDO - STUFFS U7740 AND RELATED CIRCUITRY.
TO USE U7740, MCPPLL_R:LDO AND MCPPLL_LDO MUST BE ACTIVE.
TO USE 1.05V S0, MCPPLL_R:REG MUST BE ACTIVE, MCPPLL_LDO CAN BE ACTIVE, MCPPLL_R:LDO MUST BE INACTIVE.

MCP 0.9V S5 (AUXC) Switcher



SYNC_MASTER=K99_MLB	SYNC_DATE=04/08/2010
PAGE TITLE: Misc Power Supplies	
Apple Inc.	DRAWING NUMBER: 051-8467 SIZE: D
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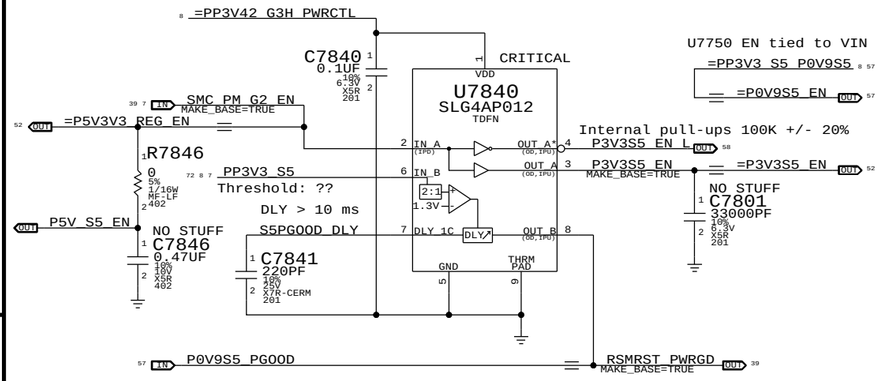
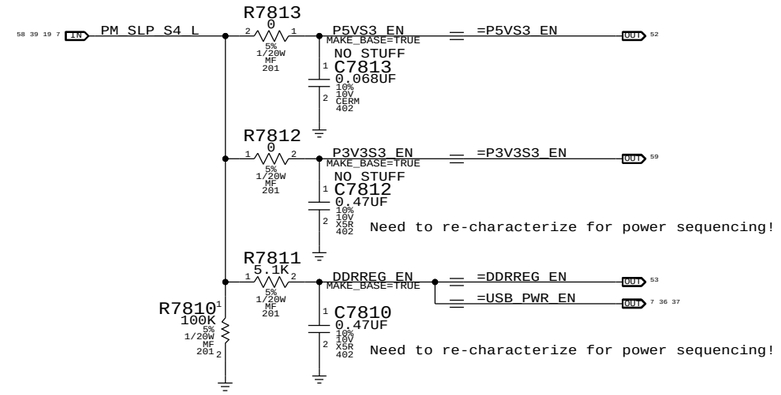
S5 Rail Enables & PGOOD

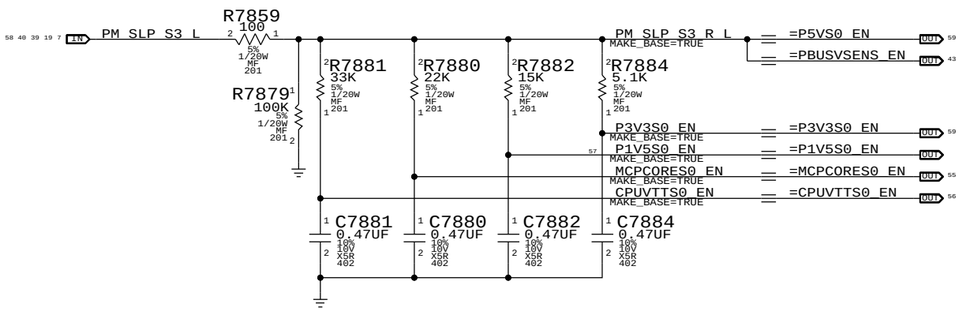


S3 Rail Enables



ENET Rail Enables

S0 Rail Enables

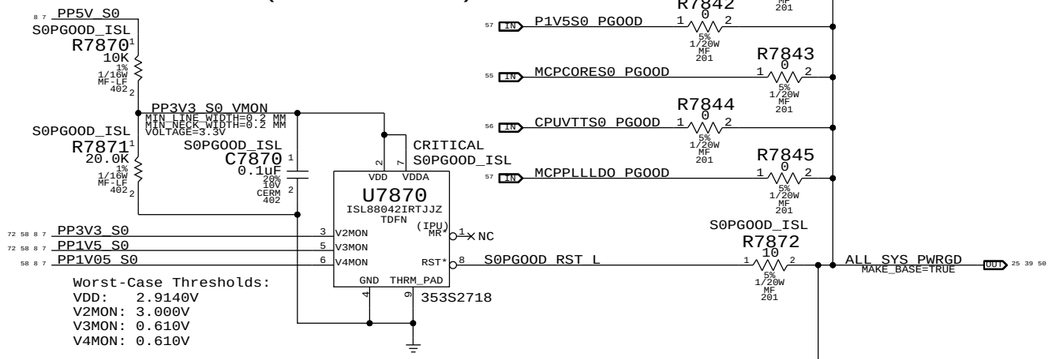


VTT Rail Enable

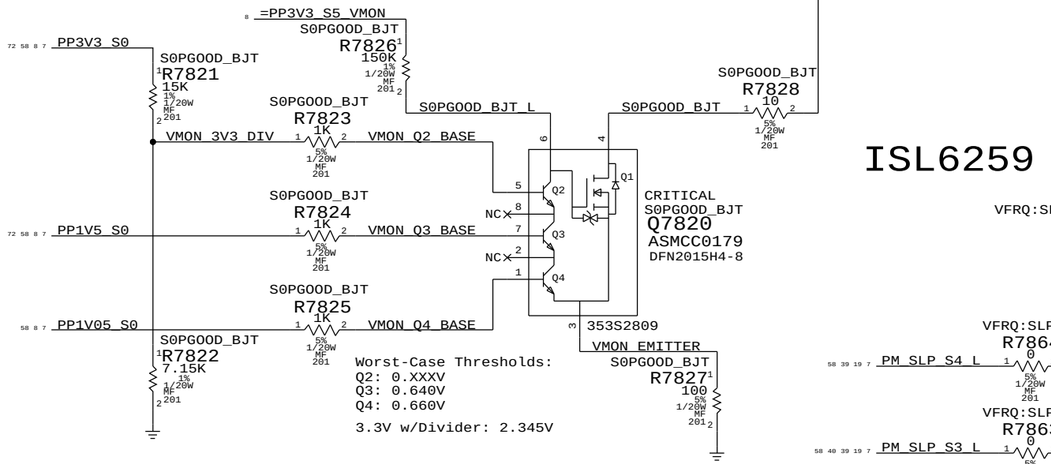
VTT rail must ramp up in about the same time as MEMVDD rail (Q2300).

S0 Rail PGOOD Circuitry

S0 Rail PGOOD (ISL Version)



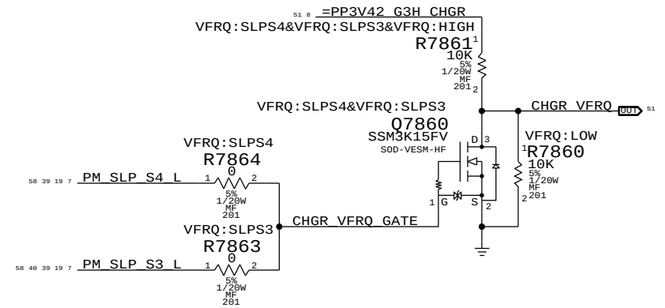
S0 Rail PGOOD (BJT Version)



Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

ISL6259 Frequency Select

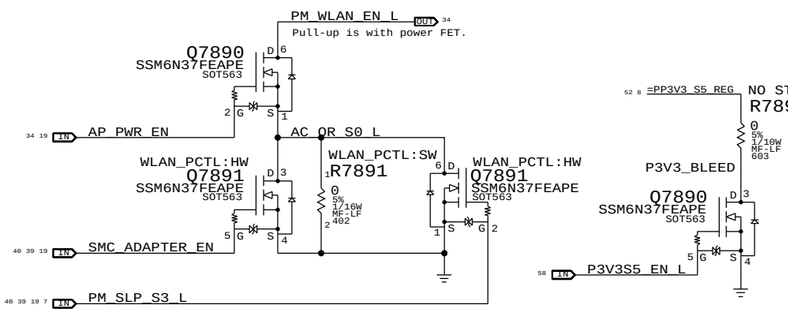


WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

NOTE: "AC" term valid only when Q7891 is stuffed



SYNC_MASTER=K99_MLB	SYNC_DATE=04/08/2010
PAGE TITLE: Power Sequencing	
Apple Inc.	DRAWING NUMBER: 051-8467 SIZE: D
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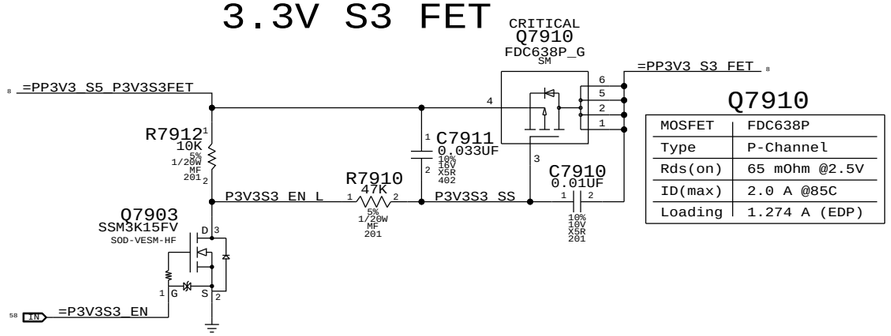
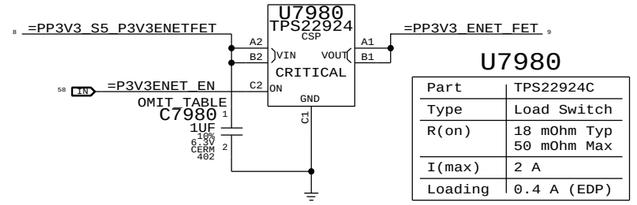
3.3V S3 FET



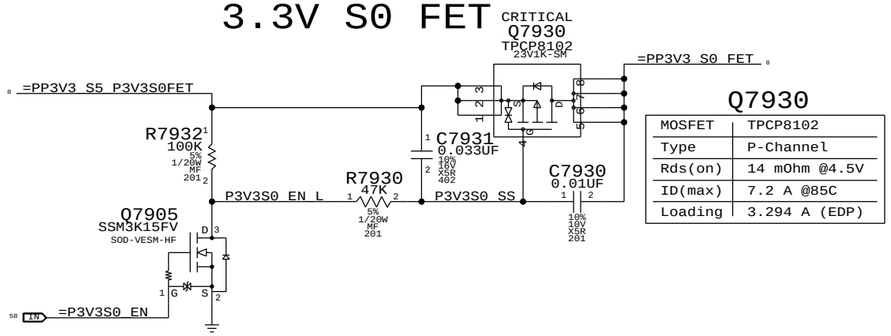
Q7910	
MOSFET	FDC638P
Type	P-Channel
Rds(on)	65 mOhm @2.5V
ID(max)	2.0 A @85C
Loading	1.274 A (EDP)

3.3V ENET Switch



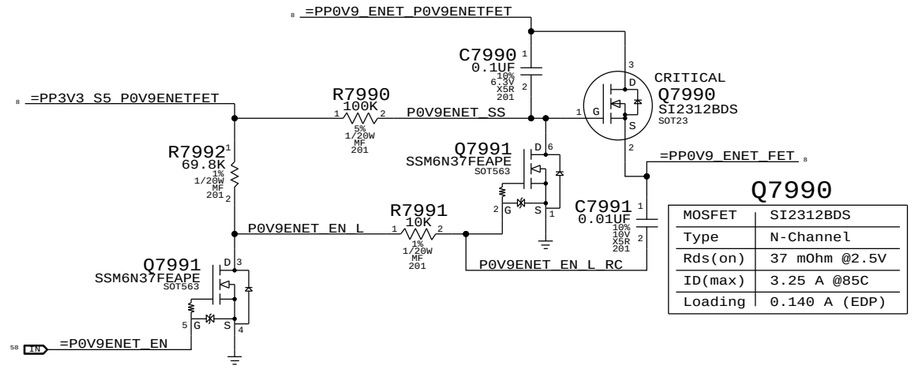
U7980	
Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max
I(max)	2 A
Loading	0.4 A (EDP)

3.3V S0 FET



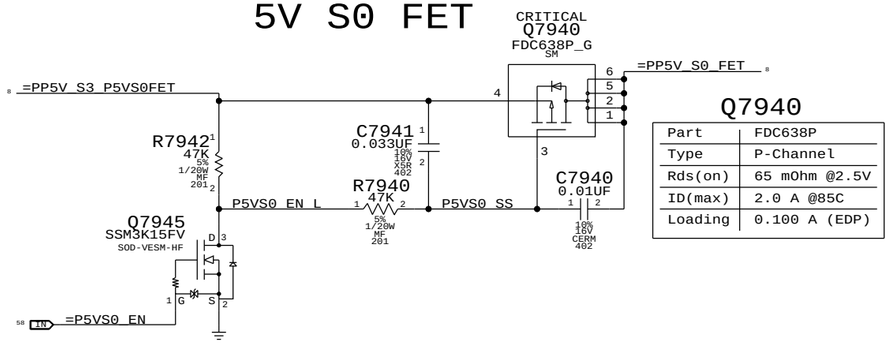
Q7930	
MOSFET	TPCP8102
Type	P-Channel
Rds(on)	14 mOhm @4.5V
ID(max)	7.2 A @85C
Loading	3.294 A (EDP)

0.9V ENET FET



Q7990	
MOSFET	SI2312BDS
Type	N-Channel
Rds(on)	37 mOhm @2.5V
ID(max)	3.25 A @85C
Loading	0.140 A (EDP)

5V S0 FET



Q7940	
Part	FDC638P
Type	P-Channel
Rds(on)	65 mOhm @2.5V
ID(max)	2.0 A @85C
Loading	0.100 A (EDP)

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

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LCD Connector

Internal DP Connector: 518S0787

CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP

=PP3V3_S0_LCD

LCD_IG_PWR_EN

CRITICAL
U9000
FPF1009
MFET-2X2

PP3V3_SW_LCD_UF
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

R9014 1K 5% 1/20W MF 201

C9009 0.1UF 10% 6.3V X5R 201

C9011 0.1UF 10% 6.3V X5R 201

OMIT_TABLE
C9012 10UF 20% 6.3V X5R 603

Pull-ups on panel side,
4.7 kOhm to 3.3V

=I2C_TCON_SDA

=I2C_TCON_SCL

DP_INT_HPD

R9060 0 5% 1/20W MF 201

DP_INT_HPD_CONN

L9004
FERR-120-OHM-1.5A
0402-LF

PP3V3_SW_LCD
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

C9015 1000PF 10% 16V X7R 201

R9070 100K 5% 1/20W MF 201

C9024 0.1uF 10% 16V X5R 402

C9025 0.1uF 10% 16V X5R 402

DP_INT_AUX_CH_N — (DP_INT_AUX_CH_C_N)

DP_INT_AUX_CH_P — (DP_INT_AUX_CH_C_P)

C9020 0.1uF 10% 16V X5R 402

C9021 0.1uF 10% 16V X5R 402

DP_INT_ML_P<0> — DP_INT_ML_C_P<0>

DP_INT_ML_N<0> — DP_INT_ML_C_N<0>

C9022 0.1uF 10% 16V X5R 402

C9023 0.1uF 10% 16V X5R 402

DP_INT_ML_P<1> — DP_INT_ML_C_P<1>

DP_INT_ML_N<1> — DP_INT_ML_C_N<1>

CRITICAL
FL9000
12-OHM-100MA
TCM1210-4SM

CRITICAL
FL9001
12-OHM-100MA
TCM1210-4SM

R9050 100K 5% 1/20W MF 201

R9080 100K 5% 1/20W MF 201

PLACEMENT_NOTE=PLACE CLOSE TO J9000

C9017 1000PF 5% 50V C0G-CERM 603

PPVOUT_SW_LCDBKLT

LED_RETURN_6
LED_RETURN_5
LED_RETURN_4
LED_RETURN_3
LED_RETURN_2
LED_RETURN_1

CRITICAL
J9000
CABLINE-CA
F-RT-SM

NC
NC
NC

LED Backlight I/F

DisplayPort I/F

DP_INT_AUX_CH_C_N
DP_INT_AUX_CH_C_P
DP_INT_ML_F_P<0>
DP_INT_ML_F_N<0>
DP_INT_ML_F_P<1>
DP_INT_ML_F_N<1>

SYNC_MASTER=K99_MLB SYNC_DATE=07/23/2010

PAGE TITLE
Internal DisplayPort Connector

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
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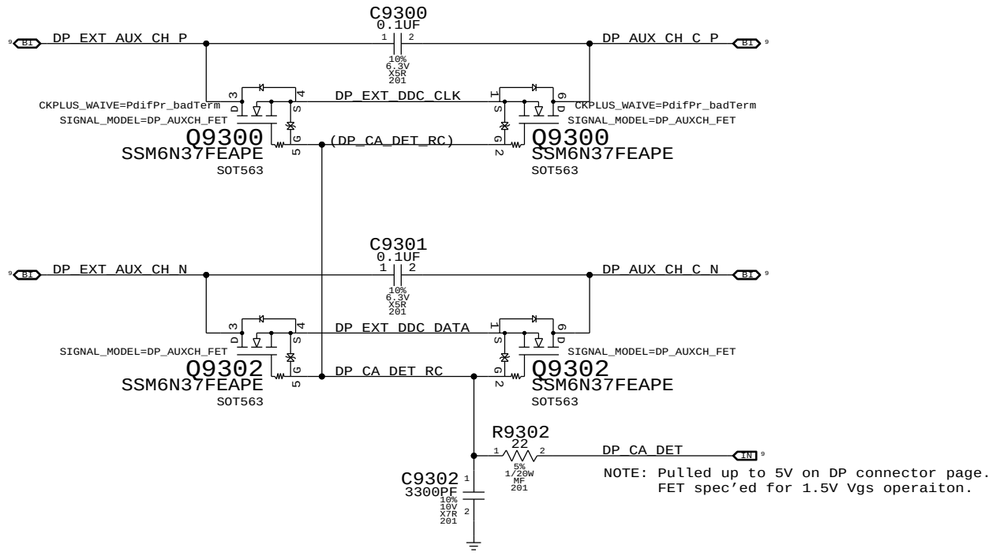

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
External DisplayPort Support

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

BRANCH

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Port Power Switch

=PP3V3_S5_DP_PORT_PWR
=DP_PWR_EN
CRITICAL
U9480
TPS2051B
SOT23
PP3V3_SW_DPILIM
MIN_LINE_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
TP_DPPWR_OC_L
L9400
FERR-120-OHM-3A
0603
PP3V3_SW_DPPWR
C9400 0.01UF
C9487 100UF
C9480 22UF
C9481 0.1UF
C9485 0.1UF
C9486 10UF
OMIT_TABLE

CRITICAL
DP_ESD
D9410
RCLAMP0524P
SLP2510P8

CRITICAL
J9400
MINIDSPLYPRT-K99
F-RT-TH
HOT_PLUG_DETECT
CONFIG1
CONFIG2
GND
ML_LANE3P
ML_LANE3N
AUX_CHP
AUX_CHN
DP_PWR
ML_LANE0P
ML_LANE0N
ML_LANE1P
ML_LANE1N
ML_LANE2P
ML_LANE2N
RETURN
SHIELD PINS

HDMI CEC
R9425 1M 5% 1/20W MF 201

CRITICAL
FL9403
12-OHM-100MA
TCM1210-4SM

R9420 100K 5% 1/20W MF 201

DP_EXT_ML_P<3> C9414 0.1UF
DP_EXT_ML_N<3> C9415 0.1UF
DP_EXT_AUX_CH_C_P
DP_EXT_AUX_CH_C_N
DP_EXT_ML_C_P<3>
DP_EXT_ML_C_N<3>
DP_EXT_ML_F_P<3>
DP_EXT_ML_F_N<3>

=PP3V3_S0_DPCONN
=PP5VR3V3_S0_DPCADET

R9443 100K 5% 1/20W MF 201
R9442 100K 5% 1/20W MF 201
DP_EXT_CA_DET
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q_L

NOTE: Q9440 must have Drain to Gate leakage of < 500 nA and gate to Source resistance of > 5 MOhm.

Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q
R9422 1M 5% 1/20W MF 201
DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.

R9421 100K 5% 1/20W MF 201

CRITICAL
DP_ESD
D9411
RCLAMP0524P
SLP2510P8

CRITICAL
DP_ESD
D9400
RCLAMP0504F
SC70-6-1

=PP3V3_S0_DPCONN
R9445 10K 5% 1/20W MF 201
DP_EXT_HPD
PP3V3_SW_DPILIM
R9444 10K 5% 1/20W MF 201
Q9441 2N7002DW-X-G SOT-363
DP_EXT_HPD_L
Q9441 2N7002DW-X-G SOT-363
DP_HPD_Q
R9423 100K 5% 1/20W MF 201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

CRITICAL
FL9400
12-OHM-100MA
TCM1210-4SM
DP_EXT_ML_C_P<0> C9410 0.1UF
DP_EXT_ML_C_N<0> C9411 0.1UF
DP_EXT_ML_F_P<0>
DP_EXT_ML_F_N<0>

CRITICAL
FL9401
12-OHM-100MA
TCM1210-4SM
DP_EXT_ML_C_P<1> C9412 0.1UF
DP_EXT_ML_C_N<1> C9413 0.1UF
DP_EXT_ML_F_P<1>
DP_EXT_ML_F_N<1>

CRITICAL
FL9402
12-OHM-100MA
TCM1210-4SM
DP_EXT_ML_C_P<2> C9416 0.1UF
DP_EXT_ML_C_N<2> C9417 0.1UF
DP_EXT_ML_F_P<2>
DP_EXT_ML_F_N<2>

CRITICAL
DP_ESD
D9411
RCLAMP0524P
SLP2510P8

SYNC_MASTER=K16_MLB	SYNC_DATE=06/01/2010
PAGE TITLE	DisplayPort Connector
Apple Inc.	DRAWING NUMBER 051-8467 SIZE D
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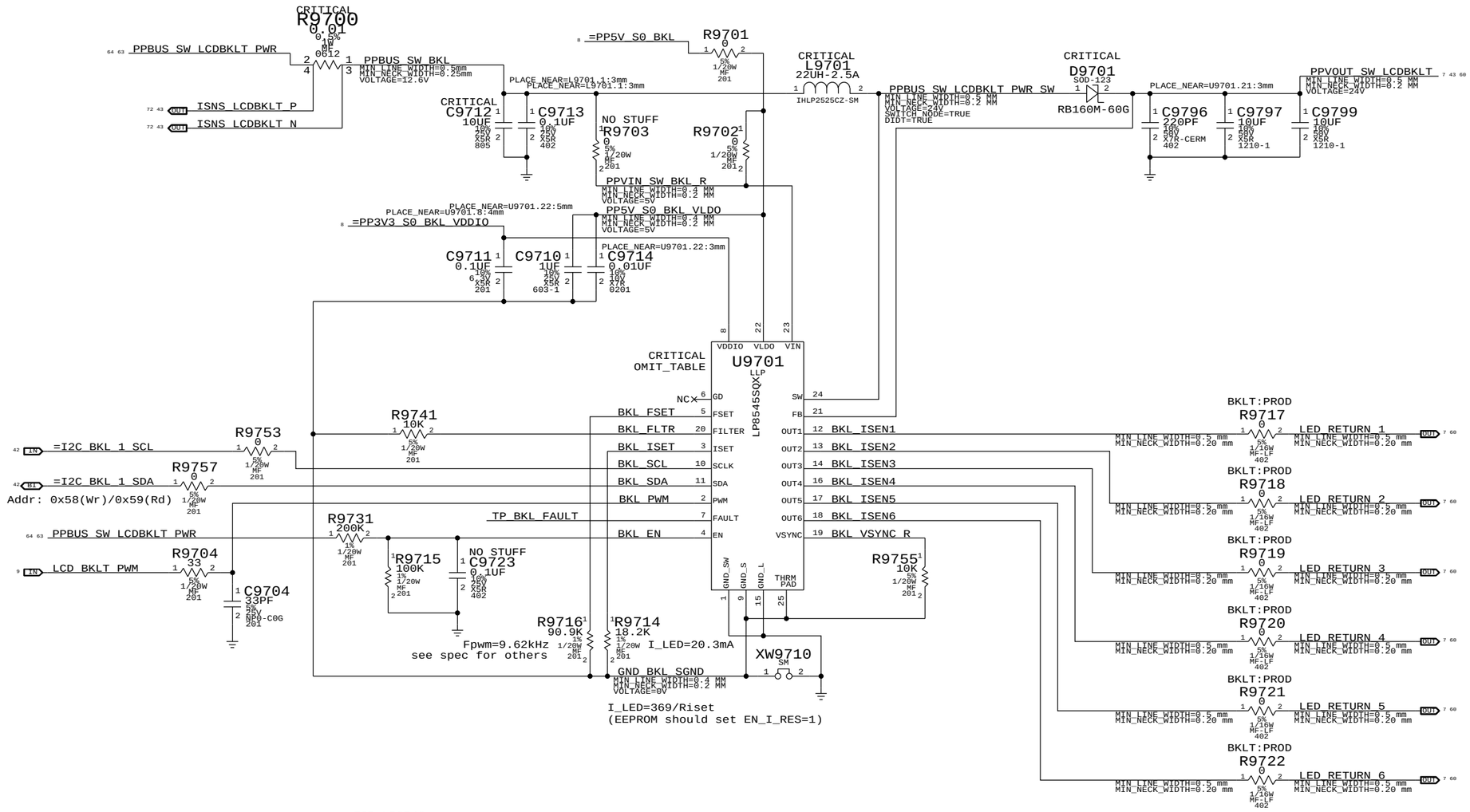
*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT



FOR LP8543:
STUFF R9741
NO STUFF R9740, C9740, C9741, R9754

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG
353S2896	1	IC,LP8545,LED BKLT CTRLR,PRODUCTIO,LLP24	U9701	CRITICAL	PROJ:K16
353S2967	1	IC,LP8545,LED BKLT CTRLR,LLP24,K99 VER	U9701	CRITICAL	PROJ:K99

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=(K99_MLB) SYNC_DATE=(03/01/2010)

PAGE TITLE
LCD Backlight Driver

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
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BRANCH
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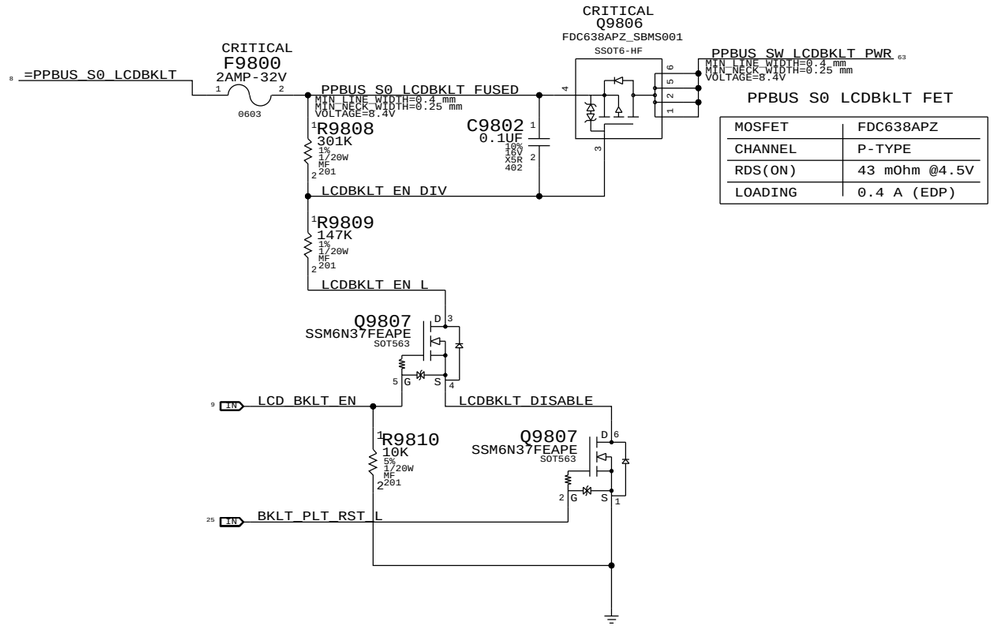

PPBUS S0 LCDBkLT FET	
MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
LCD Backlight Support

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
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ADDITIONAL CPU VCORE HF DECOUPLING

40x 1uF 0402

12 11 8 =PPVCORE_S0_CPU

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT_TABLE CRITICAL C9900 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9901 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9902 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9903 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9904 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9905 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9906 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9907 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9908 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C9909 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT_TABLE CRITICAL C9910 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9911 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9912 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9913 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9914 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9915 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9916 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9917 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9918 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C9919 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT_TABLE CRITICAL C9920 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9921 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9922 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9923 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9924 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9925 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9926 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9927 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9928 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C9929 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT_TABLE CRITICAL C9930 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9931 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9932 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9933 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9934 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9935 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9936 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9937 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE CRITICAL C9938 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C9939 2.2UF 20% 6.3V CERM 402-LF

SYNC_MASTER=K99_MLB SYNC_DATE=05/18/2010

PAGE TITLE
Additional CPU/GPU Decoupling

Apple Inc.

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
FSB 4X Signal Groups			
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0> 7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0> 7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0> 7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0> 7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16> 7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1> 7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1> 7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1> 7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32> 7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2> 7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2> 7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2> 7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48> 7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3> 7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3> 7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3> 7 10 14
FSB 2X Signals			
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3> 7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0> 7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0> 7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17> 7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1> 7 10 14
FSB 1X Signals			
FSB_1X	FSB_55S	FSB_1X	FSB_ADS_L 7 10 14
FSB_BREQ0_L	FSB_55S	FSB_1X	FSB_BREQ0_L 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_BNR_L 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_BPRI_L 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_DBSY_L 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_DEFER_L 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_DRDY_L 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_HIT_L 7 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_HITM_L 7 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_LOCK_L 7 10 14
FSB_CPURST_L	FSB_55S	FSB_1X	FSB_CPURST_L 10 13 14
FSB_1X	FSB_55S	FSB_1X	FSB_RS_L<2..0> 10 14
FSB_1X	FSB_55S	FSB_1X	FSB_TRDY_L 10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_A20M_L 10 14
CPU_BSEL	CPU_55S	CPU_AGTL	CPU_BSEL<2..0> 9 10
CPU_FERR_L	CPU_55S	CPU_8MIL	CPU_FERR_L 10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_IGNNE_L 10 14
CPU_INIT_L	CPU_55S	CPU_AGTL	CPU_INIT_L 10 14
CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU_INTR 10 14
CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU_NMI 10 14
CPU_PROCHOT_L	CPU_55S	CPU_AGTL	CPU_PROCHOT_L 10 14 40
CPU_PWRGD	CPU_55S	CPU_AGTL	CPU_PWRGD 10 13 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_SMI_L 10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_STPCLK_L 10 14
PM_THRMTRIP_L	CPU_55S	CPU_8MIL	PM_THRMTRIP_L 10 14 40
FSB_CPUSLP_L	CPU_55S	CPU_AGTL	FSB_CPUSLP_L 10 14
CPU_FROM_SB	CPU_55S	CPU_AGTL	CPU_DPSLP_L 10 14
CPU_DPRSTP_L	CPU_55S	CPU_AGTL	CPU_DPRSTP_L 10 14 54
CPU_ASYNC	CPU_55S	CPU_AGTL	FSB_DPWR_L 10 14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P 10 14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N 10 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P 13 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N 13 14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P 14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N 14
CPU_IERR_L	CPU_55S		CPU_IERR_L 10
PM_DPRSLPVR	CPU_55S	CPU_AGTL	PM_DPRSLPVR 14 54
(See above)	CPU_55S	CPU_AGTL	IMVP_DPRSLPVR
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD 14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND 14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC 14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND 14
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF 10 33
CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3> 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2> 10
CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1> 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0> 10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI 10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO 10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS 10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK 10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L 10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0> 10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5> 10 13
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L 13
	CPU_55S	CPU_8MIL	CPU_VID<6..0> 11 12 54
	CPU_55S	CPU_8MIL	IMVP6_VID<6..0> 12
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P 11 54
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N 11 54
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P 54
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N 54

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: CPU/FSB Constraints

Apple Inc.

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
MEM_CLK2MEM	*	=4:1_SPACING	?	NV DG says 3x inner, 4x outer
MEM_CTRL2CTRL	*	=2:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CTRL2MEM	*	=2.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CMD2CMD	*	=1.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CMD2MEM	*	=3:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DATA2DATA	*	=1.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DATA2MEM	*	=3:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DQS2MEM	*	=3:1_SPACING	?	NV DG says 4x inner, 5x outer
MEM_2OTHER	*	25 MIL	?	

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 360 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
CMD/CTRL signals should be matched within 150 ps.
All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2

MEM_A/B_CKE EC SET NAME IS CHANGED ON K6, CANNOT SYNC THIS PAGE FROM T27

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_A_CLK_P<5..0>	9 15 26 27 32
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_A_CLK_N<5..0>	9 15 26 27 32
MEM_A_CKE	MEM_50S	MEM_CTRL	MEM_A_CKE<3..0>	15 21 26 27 32
MEM_A_CNTL	MEM_50S	MEM_CTRL	MEM_A_CS_L<3..0>	15 26 27 32
MEM_A_CNTL	MEM_50S	MEM_CTRL	MEM_A_ODT<3..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_A<15..0>	9 15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_BA<2..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_RAS_L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_CAS_L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_WE_L	15 26 27 32
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56>	15 27
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DM<0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DM<1>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DM<2>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DM<3>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DM<7>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 26
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 26
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 26
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 26
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 26
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 26
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 26
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 26
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 27
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_B_CLK_P<5..0>	9 15 28 29 32
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_B_CLK_N<5..0>	9 15 28 29 32
MEM_B_CKE	MEM_50S	MEM_CTRL	MEM_B_CKE<3..0>	15 21 28 29 32
MEM_B_CNTL	MEM_50S	MEM_CTRL	MEM_B_CS_L<3..0>	15 28 29 32
MEM_B_CNTL	MEM_50S	MEM_CTRL	MEM_B_ODT<3..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_A<15..0>	9 15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_BA<2..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_RAS_L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_CAS_L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_WE_L	15 28 29 32
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	15
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	15

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PAGE TITLE: Memory Constraints

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	20 MIL	?
CRT_2CRT	*	15 MIL	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	=4x_DIELECTRIC	?
MCP_DAC_COMP	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max trace length: LVDS 10 inches, DP 8.5 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=4x_DIELECTRIC	?

SATA intra-pair matching should be 1 ps.
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	
	PCIE_90D	PCIE	PCIE_AP_R2D_P	7 34
	PCIE_90D	PCIE	PCIE_AP_R2D_N	7 34
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE_AP_R2D_C_P	16 34
	PCIE_90D	PCIE	PCIE_AP_R2D_C_N	16 34
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE_AP_D2R_P	7 16 34
	PCIE_90D	PCIE	PCIE_AP_D2R_N	7 16 34
	PCIE_90D	PCIE	PCIE_ENET_R2D_P	
	PCIE_90D	PCIE	PCIE_ENET_R2D_N	
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE_ENET_R2D_C_P	
	PCIE_90D	PCIE	PCIE_ENET_R2D_C_N	
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE_ENET_D2R_P	
	PCIE_90D	PCIE	PCIE_ENET_D2R_N	
	PCIE_90D	PCIE	PCIE_ENET_D2R_C_P	
	PCIE_90D	PCIE	PCIE_ENET_D2R_C_N	
	PCIE_90D	PCIE	PCIE_FW_R2D_P	
	PCIE_90D	PCIE	PCIE_FW_R2D_N	
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	
	PCIE_90D	PCIE	PCIE_FW_D2R_N	
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	9 16
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	9 16
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_P	7 16 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_N	7 16 34
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX0_TERMP	16
CRT_RED	CRT_50S	CRT	CRT_IG_R_C_PR	
CRT_GREEN	CRT_50S	CRT	CRT_IG_G_Y_Y	
CRT_BLUE	CRT_50S	CRT	CRT_IG_B_COMP_PB	
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC	
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC	
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET	
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF	
DP_INT_ML	DP_90D	DISPLAYPORT	DP_IG_ML1_P<1..0>	9 17
DP_INT_ML	DP_90D	DISPLAYPORT	DP_IG_ML1_N<1..0>	9 17
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH1_P	9 17
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH1_N	9 17
DP_EXT_ML	DP_90D	DISPLAYPORT	DP_IG_ML0_P<3..0>	9 17
DP_EXT_ML	DP_90D	DISPLAYPORT	DP_IG_ML0_N<3..0>	9 17
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH0_P	9 17
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH0_N	9 17
MCP_TMDS0_RSET	MCP_DV_COMP		MCP_TMDS0_RSET	17 24
MCP_TMDS0_VPROBE			MCP_TMDS0_VPROBE	17 24
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>	
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>	
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>	
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>	
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	17 24
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	17 24
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	18 35
	SATA_90D	SATA	SATA_HDD_R2D_C_N	18 35
	SATA_90D	SATA	SATA_HDD_R2D_P	7 35
	SATA_90D	SATA	SATA_HDD_R2D_N	7 35
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	18 35
	SATA_90D	SATA	SATA_HDD_D2R_N	18 35
	SATA_90D	SATA	SATA_HDD_D2R_C_P	7 35
	SATA_90D	SATA	SATA_HDD_D2R_C_N	7 35
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	9 18
	SATA_90D	SATA	SATA_ODD_R2D_C_N	9 18
	SATA_90D	SATA	SATA_ODD_R2D_P	
	SATA_90D	SATA	SATA_ODD_R2D_N	
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	9 18
	SATA_90D	SATA	SATA_ODD_D2R_N	9 18
	SATA_90D	SATA	SATA_ODD_D2R_C_P	
	SATA_90D	SATA	SATA_ODD_D2R_C_N	
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	18

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.7

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.8

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.10

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.11

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.12

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_55S	LPC	LPC AD<3..0>	7 19 39 41
LPC_FRAME_L	LPC_55S	LPC	LPC FRAME L	7 19 39 41
LPC_RESET_L	LPC_55S	LPC	LPC RESET L	19 25
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC R	19 25
	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC	25 39
	CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS	7 25 41
USB_EXTA	USB_90D	USB	USB EXTA P	18 36
	USB_90D	USB	USB EXTA N	18 36
	USB_90D	USB	USB EXTA MUXED P	36 72
	USB_90D	USB	USB EXTA MUXED N	36 72
USB_MINI	USB_90D	USB	USB MINI P	9 18
	USB_90D	USB	USB MINI N	9 18
USB_EXTD	USB_90D	USB	USB EXTD P	7 18 37
	USB_90D	USB	USB EXTD N	7 18 37
USB_CAMERA	USB_90D	USB	USB CAMERA P	7 18 37
	USB_90D	USB	USB CAMERA N	7 18 37
USB_BT	USB_90D	USB	USB BT P	7 18 34
	USB_90D	USB	USB BT N	7 18 34
USB_TPAD	USB_90D	USB	USB TPAD P	18 47 72
	USB_90D	USB	USB TPAD N	18 47 72
USB_IR	USB_90D	USB	USB IR P	
	USB_90D	USB	USB IR N	
USB_EXTB	USB_90D	USB	USB EXTB P	
	USB_90D	USB	USB EXTB N	
USB_T57	USB_90D	USB	USB T57 P	
	USB_90D	USB	USB T57 N	
USB_EXTC	USB_90D	USB	USB EXTC P	9 18
	USB_90D	USB	USB EXTC N	9 18
USB_SDCARD	USB_90D	USB	USB SDCARD P	18 38
	USB_90D	USB	USB SDCARD N	18 38
USB_WM	USB_90D	USB	USB WM P	
	USB_90D	USB	USB WM N	
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP USB RBIAS GND	18
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS MCP 0 CLK	19 42
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS MCP 0 DATA	19 42
(SMBUS_SMC_MGMT_SCL)	SMB_55S	SMB	SMBUS MCP 1 CLK	19 42
(SMBUS_SMC_MGMT_SDA)	SMB_55S	SMB	SMBUS MCP 1 DATA	19 42
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT CLK	7 19 37
	HDA_55S	HDA	HDA BIT CLK R	19
HDA_SYNC	HDA_55S	HDA	HDA SYNC	7 19 37
	HDA_55S	HDA	HDA SYNC R	19
HDA_RST_L	HDA_55S	HDA	HDA RST R L	19
	HDA_55S	HDA	HDA RST L	7 19 37
HDA_SDIN0	HDA_55S	HDA	HDA SDIN0	7 19 37
	HDA_55S	HDA	HDA SDIN CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA SDOUT	7 19 37
	HDA_55S	HDA	HDA SDOUT R	19
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP HDA PULLDN COMP	19
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK R	19 25
	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK	25 39
SPI_CLK	SPI_55S	SPI	SPI CLK R	19 41
	SPI_55S	SPI	SPI CLK	41
SPI_MOSI	SPI_55S	SPI	SPI MOSI R	19 41
	SPI_55S	SPI	SPI MOSI	41
SPI_MISO	SPI_55S	SPI	SPI MISO	19 41
SPI_CS0	SPI_55S	SPI	SPI CS0 R L	19 41
	SPI_55S	SPI	SPI CS0 L	41
	SPI_55S	SPI	SPI MLB CLK	41 48
	SPI_55S	SPI	SPI MLB MOSI	41 48
	SPI_55S	SPI	SPI MLB MISO	41 48
	SPI_55S	SPI	SPI MLB CS L	41 48
	SPI_55S	SPI	SPI ALT CLK	7 41
	SPI_55S	SPI	SPI ALT MOSI	7 41
	SPI_55S	SPI	SPI ALT MISO	7 41
	SPI_55S	SPI	SPI ALT CS L	7 41

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

SD Card Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

RGMII Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	9 18
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	9 18
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<0>	9 18
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	9 18
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	9 18
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<0>	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	
	ENET_MII_55S	ENET_MII	ENET_RESET_L	

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>

SD Card Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SD_DATA	SD_55S	SD_INTERFACE	SD_D<4..0>	7 38
	SD_55S	SD_INTERFACE	SDCONN_DATA<4..0>	
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<4>	
SD_DATA_R	SD_55S	SD_INTERFACE	SD_D<7..5>	7 38
	SD_55S	SD_INTERFACE	SDCONN_DATA<7..5>	
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<7..5>	
SD_CLK	SD_55S	SD_INTERFACE	SD_CLK	7 38
	SD_55S	SD_INTERFACE	SD_CLK_R	38
	SD_55S	SD_INTERFACE	SDCONN_CLK	
SD_CMD	SD_55S	SD_INTERFACE	SD_CMD	7 38
	SD_55S	SD_INTERFACE	SDCONN_CMD	
	SD_55S	SD_INTERFACE	BCM57765_CR_CMD	

NOTE: SD_D<7..5> are different to support BCM5764M/BCM57765 co-layout.

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5S	SMB	SMBUS_SMC_A_S3_SCL	42
SMBUS_SMC_A_S3_SDA	SMB_5S	SMB	SMBUS_SMC_A_S3_SDA	42
SMBUS_SMC_B_S0_SCL	SMB_5S	SMB	SMBUS_SMC_B_S0_SCL	42
SMBUS_SMC_B_S0_SDA	SMB_5S	SMB	SMBUS_SMC_B_S0_SDA	42
SMBUS_SMC_0_S0_SCL	SMB_5S	SMB	SMBUS_SMC_0_S0_SCL	42
SMBUS_SMC_0_S0_SDA	SMB_5S	SMB	SMBUS_SMC_0_S0_SDA	42
SMBUS_SMC_BSA_SCL	SMB_5S	SMB	SMBUS_SMC_BSA_SCL	7 42
SMBUS_SMC_BSA_SDA	SMB_5S	SMB	SMBUS_SMC_BSA_SDA	7 42
SMBUS_SMC_MGMT_SCL	SMB_5S	SMB	SMBUS_SMC_MGMT_SCL	42
SMBUS_SMC_MGMT_SDA	SMB_5S	SMB	SMBUS_SMC_MGMT_SDA	42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	51
	1TO1_DIFFPAIR		CHGR_CSI_N	51
	1TO1_DIFFPAIR		CHGR_CSI_R_P	51
	1TO1_DIFFPAIR		CHGR_CSI_R_N	51
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	51
	1TO1_DIFFPAIR		CHGR_CSO_N	51
	1TO1_DIFFPAIR		CHGR_CSO_R_P	44 51
	1TO1_DIFFPAIR		CHGR_CSO_R_N	44 51

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=1:1_SPACING	?
THERM	*	=1:1_SPACING	?
AUDIO	*	=1:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SD CARD READER LAYOUT RELAXATIONS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*		=STANDARD				
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	5.8 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	*			0.25 MM	250 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
(USB_EXTA)	USB_90D	USB	USB_EXTA_MUXED_P	36 69
(USB_EXTA)	USB_90D	USB	USB_EXTA_MUXED_N	36 69
(USB_EXTA)	USB_90D	USB	USB_LT1_P	36
(USB_EXTA)	USB_90D	USB	USB_LT1_N	36
(USB_TPAD)	USB_90D	USB	USB_TPAD_P	18 47 69
(USB_TPAD)	USB_90D	USB	USB_TPAD_N	18 47 69
(USB_TPAD)	USB_90D	USB	USB_TPAD_CONN_P	7 47
(USB_TPAD)	USB_90D	USB	USB_TPAD_CONN_N	7 47
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	I2C_SMC_SMS_SDA_R	
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	I2C_SMC_SMS_SCL_R	
	SMB_55S	SMB	I2C_TCON_SCL	42
	SMB_55S	SMB	I2C_TCON_SDA	42
	SMB_55S	SMB	I2C_TCON_SCL_CONN	60
	SMB_55S	SMB	I2C_TCON_SDA_CONN	60

Graphics Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_90D	DISPLAYPORT	DP_INT_ML_P<1..0>	9 60
	DP_90D	DISPLAYPORT	DP_INT_ML_N<1..0>	9 60
	DP_90D	DISPLAYPORT	DP_INT_ML_C_P<1..0>	60
	DP_90D	DISPLAYPORT	DP_INT_ML_C_N<1..0>	60
	DP_90D	DISPLAYPORT	DP_INT_ML_F_P<1..0>	7 60
	DP_90D	DISPLAYPORT	DP_INT_ML_F_N<1..0>	7 60
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_C_P	7 60
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_C_N	7 60
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_P	9 60
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_N	9 60
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP_EXT_ML_P<3..0>	9 62
	DP_90D	DISPLAYPORT	DP_EXT_ML_N<3..0>	9 62
	DP_90D	DISPLAYPORT	DP_EXT_ML_C_P<3..0>	62
	DP_90D	DISPLAYPORT	DP_EXT_ML_C_N<3..0>	62
	DP_90D	DISPLAYPORT	DP_EXT_ML_F_P<3..0>	62
	DP_90D	DISPLAYPORT	DP_EXT_ML_F_N<3..0>	62
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP_EXT_AUX_CH_C_P	9 62
	DP_90D	DISPLAYPORT	DP_EXT_AUX_CH_C_N	9 62

Power Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CPUTHMSNS_D2	THERM_1TO1_55S	THERM	DRAMTHMSNS_D2_P	45
	THERM_1TO1_55S	THERM	DRAMTHMSNS_D2_N	45
CPU_THERMD	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 45
	THERM_1TO1_55S	THERM	CPU_THERMD_N	10 45
MCPTHMSNS_D2	THERM_1TO1_55S	THERM	MLBR_THMDIODE_P	45
	THERM_1TO1_55S	THERM	MLBR_THMDIODE_N	45
MCP_THMDIODE	THERM_1TO1_55S	THERM	MCP_THMDIODE_P	19 45
	THERM_1TO1_55S	THERM	MCP_THMDIODE_N	19 45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	43 53
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	43 53
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	34 43
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	34 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CSREG_P	44
	SENSE_1TO1_55S	SENSE	ISNS_CSREG_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	35 43
	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	35 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	43 63
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	43 63
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_P	56
	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_N	56
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	IMVP6_CS_P	54
	SENSE_1TO1_55S	SENSE	IMVP6_CS_N	54
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	IMVP6_CS_R_P	54
	SENSE_1TO1_55S	SENSE	IMVP6_CS_R_N	54
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VTTSENSE_P	56
	SENSE_1TO1_55S	SENSE	CPU_VTTSENSE_N	56
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	MCPCORES0_VSEN_P	22 55
	SENSE_1TO1_55S	SENSE	MCPCORES0_VSEN_N	22 55
		MEM_POWER	PP1V5R1V35_S3	7 8
		SB_POWER	PP3V3_S5	7 8 58
		SB_POWER	PP3V3_S0	7 8 58
		SB_POWER	PP1V5_S0	7 8 58
		GND	GND	

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_P	7 37 49
	DIFFPAIR	AUDIO	SPKRAMP_INR_N	7 37 49
MAX98300_R	DIFFPAIR	AUDIO	MAX98300_R_P	49
	DIFFPAIR	AUDIO	MAX98300_R_N	49

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K99 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL3,ISL10	Y	0.250 MM	0.250 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.250 MM	0.250 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.140 MM	0.140 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.090 MM	0.090 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.076 MM	0.076 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL3,ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL4,ISL9	Y	0.155 MM	0.155 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.109 MM	0.109 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.125 MM	0.125 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
75_OHM_DIFF	TOP,BOTTOM	Y	0.160 MM	0.160 MM		0.160 MM	0.160 MM
75_OHM_DIFF	ISL3,ISL10	Y	0.120 MM	0.120 MM		0.140 MM	0.140 MM
75_OHM_DIFF	ISL4,ISL9	Y	0.140 MM	0.140 MM		0.140 MM	0.140 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
95_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
95_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL3,ISL10	Y	0.075 MM	0.075 MM		0.300 MM	0.300 MM
100_OHM_DIFF	ISL4,ISL9	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.28:1_SPACING	*	0.228 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V5_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NB_STATIC	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
1.5X_DIELECTRIC	*	0.105 MM	?
5X_DIELECTRIC	*	0.350 MM	?

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1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7980	CRITICAL	SS_CAP_1UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0628	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7980	CRITICAL	MU_CAP_1UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0630	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7980	CRITICAL	TY_CAP_1UF

2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	SS_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1284,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3536,C3537	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3600,C3601,C3604,C3605,C3610,C3611,C3612,C3614,C3615,C3616	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3620,C3621,C3624,C3625,C3630,C3631,C3634,C3635,C3636,C3637	CRITICAL	SS_CAP_2_2UF
138S0632	9	CAP, 2.2UF, 6.3V, 20%, 0402	C3642,C3644,C3645,C3646,C3650,C3651,C3654,C3655,C3656	CRITICAL	SS_CAP_2_2UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	MU_CAP_2_2UF
138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1284,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3536,C3537	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3600,C3601,C3604,C3605,C3610,C3611,C3612,C3614,C3615,C3616	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3620,C3621,C3624,C3625,C3630,C3631,C3634,C3635,C3636,C3637	CRITICAL	MU_CAP_2_2UF
138S0633	9	CAP, 2.2UF, 6.3V, 20%, 0402	C3642,C3644,C3645,C3646,C3650,C3651,C3654,C3655,C3656	CRITICAL	MU_CAP_2_2UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	TY_CAP_2_2UF
138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1284,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3536,C3537	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3600,C3601,C3604,C3605,C3610,C3611,C3612,C3614,C3615,C3616	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3620,C3621,C3624,C3625,C3630,C3631,C3634,C3635,C3636,C3637	CRITICAL	TY_CAP_2_2UF
138S0634	9	CAP, 2.2UF, 6.3V, 20%, 0402	C3642,C3644,C3645,C3646,C3650,C3651,C3654,C3655,C3656	CRITICAL	TY_CAP_2_2UF

10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C4690,C4695,C5025,C7205,C7290,C7345,C7355,C7360	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C4912,C9486,C2500,C2520,C2560,C2567,C2600,C2601	CRITICAL	SS_CAP_10UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0625	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C4690,C4695,C5025,C7205,C7290,C7345,C7355,C7360	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C4912,C9486,C2500,C2520,C2560,C2567,C2600,C2601	CRITICAL	MU_CAP_10UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0627	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C4690,C4695,C5025,C7205,C7290,C7345,C7355,C7360	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C4912,C9486,C2500,C2520,C2560,C2567,C2600,C2601	CRITICAL	TY_CAP_10UF

22UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0635	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	SS_CAP_22UF
138S0635	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	SS_CAP_22UF
138S0635	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	SS_CAP_22UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0676	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	MU_CAP_22UF
138S0676	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	MU_CAP_22UF
138S0676	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	MU_CAP_22UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0688	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	TY_CAP_22UF
138S0688	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	TY_CAP_22UF
138S0688	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	TY_CAP_22UF

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