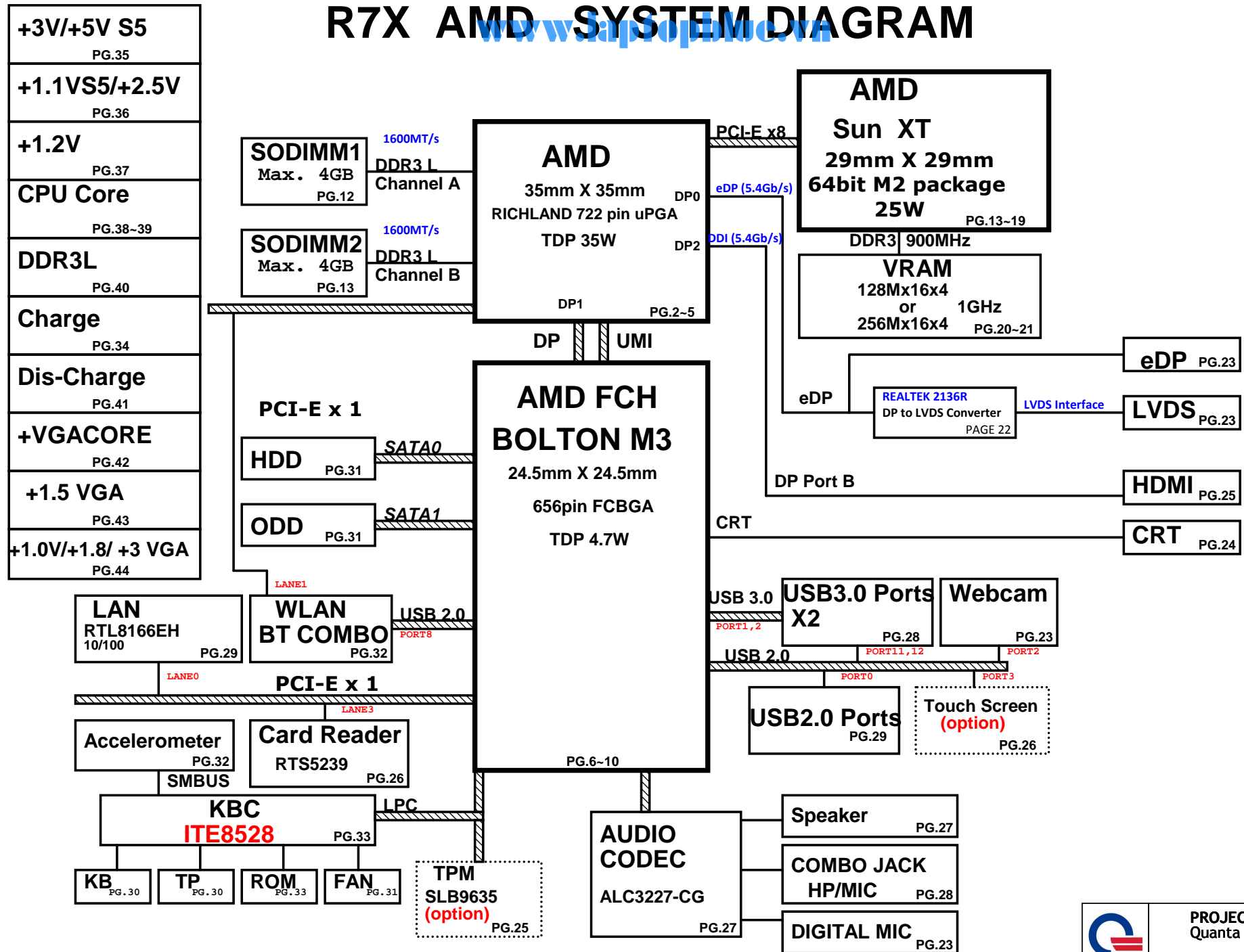


R7X AMD SYSTEM DIAGRAM

01





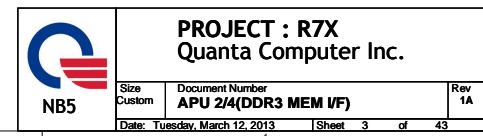
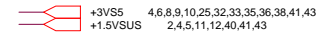
8



8V

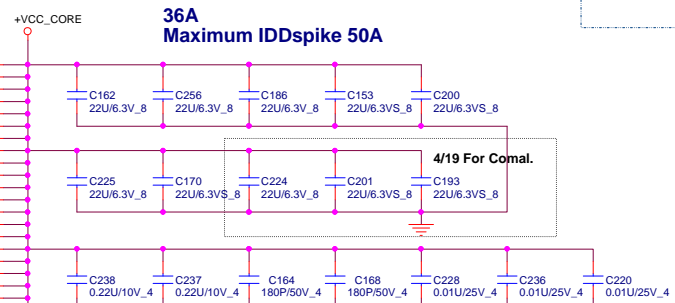
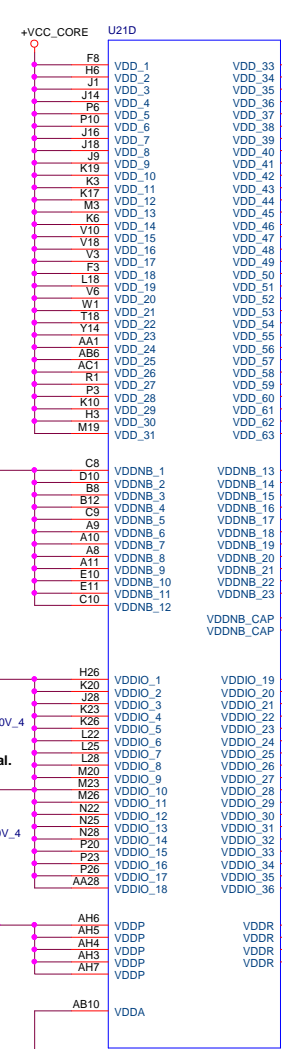
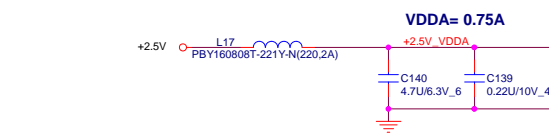
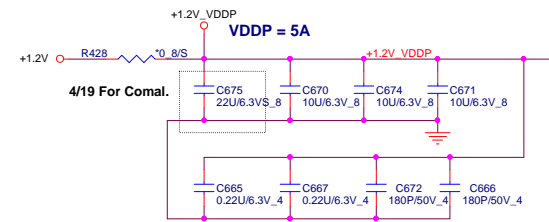
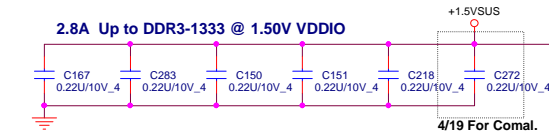
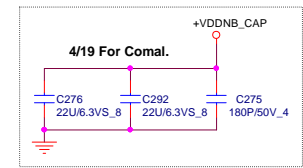
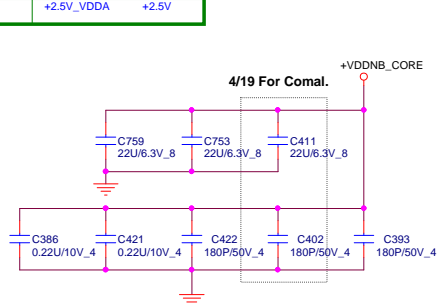
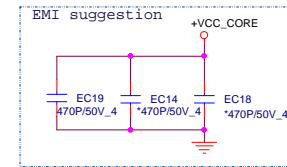
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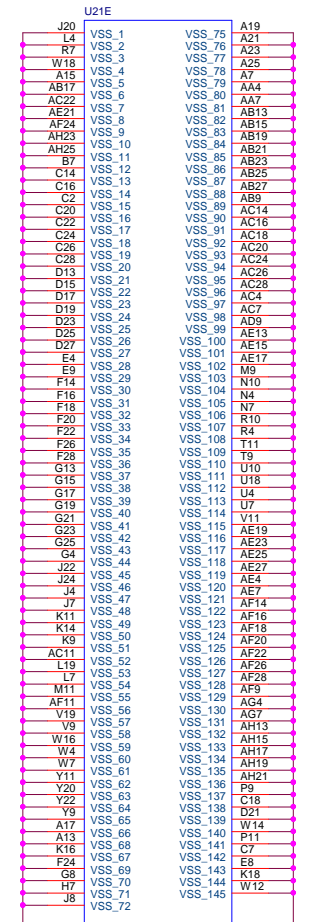
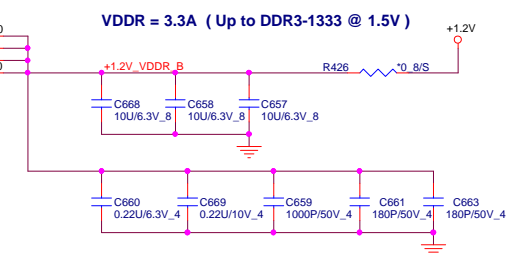
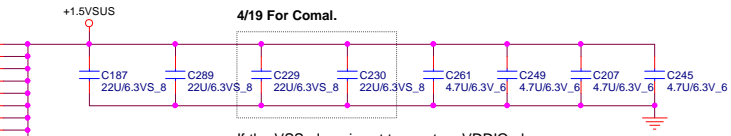
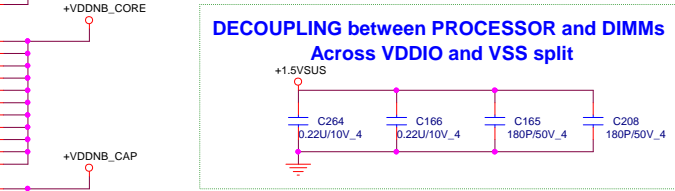


APU POWER TABLE

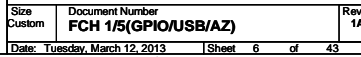
PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

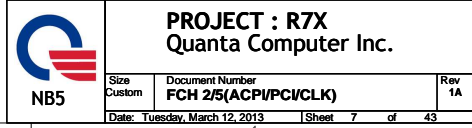


25A Maximum IDDNBSpike 33A



Richland APU

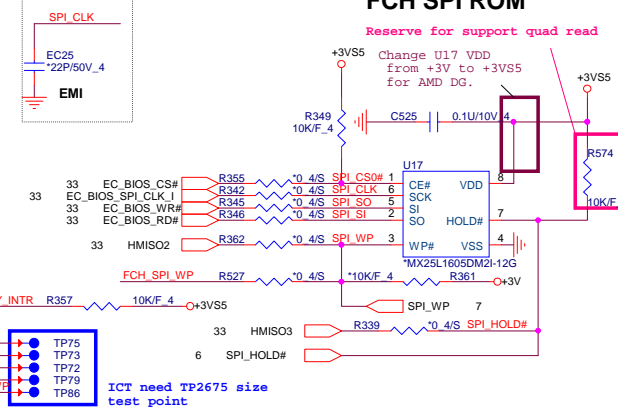




Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08F5023

FCH SPI ROM

Reserve for support quad read



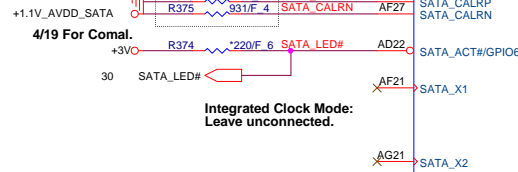
PLACE SATA AC COUPLING CAPS CLOSE TO HUDSON-M2/M3

SATA HDD

SATA ODD

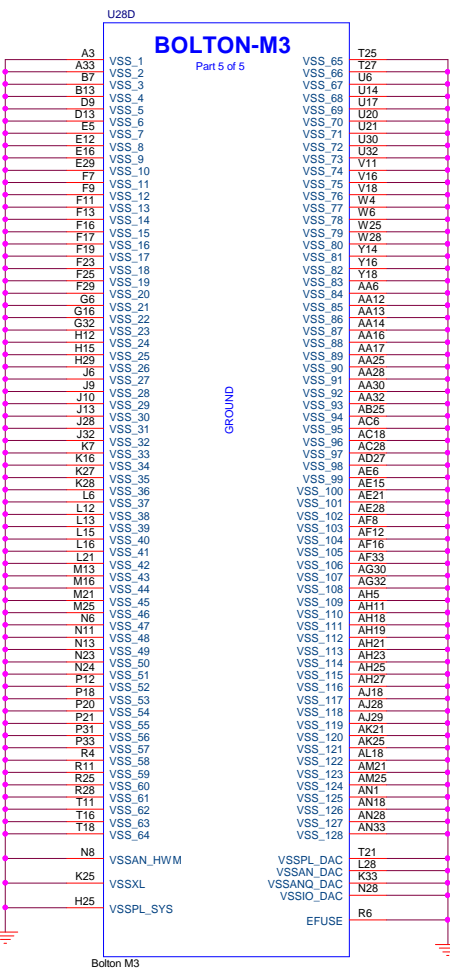
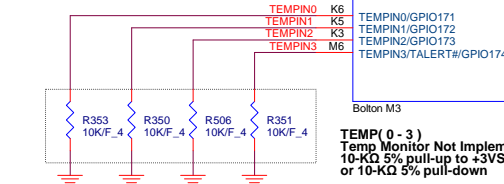


PLACE SATA CAL RES VERY CLOSE TO BALL OF HUDSON-M2/M3



Add GPIO for G-sensor LED control

GPIO52 internal pull Hi 8.2K to +3V
GPIO53 internal pull Hi 8.2K to +3V
GPIO54 internal pull Hi 8.2K to +3V
GPIO57 internal pull Hi 8.2K to +3V
GPIO58 internal pull Hi 8.2K to +3V

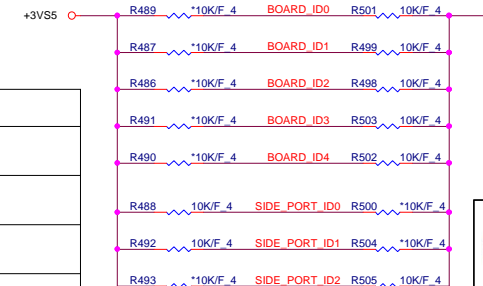


ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	DIS		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12

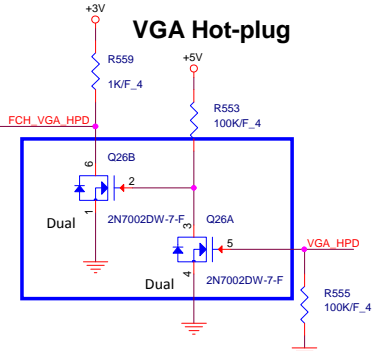
SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port

HW MONITOR

VIN (0-7)
Voltage Monitor Not Implemented
10-K 5% pull-up to +3V5
or 10-K 5% pull-down



VGA Hot-plug

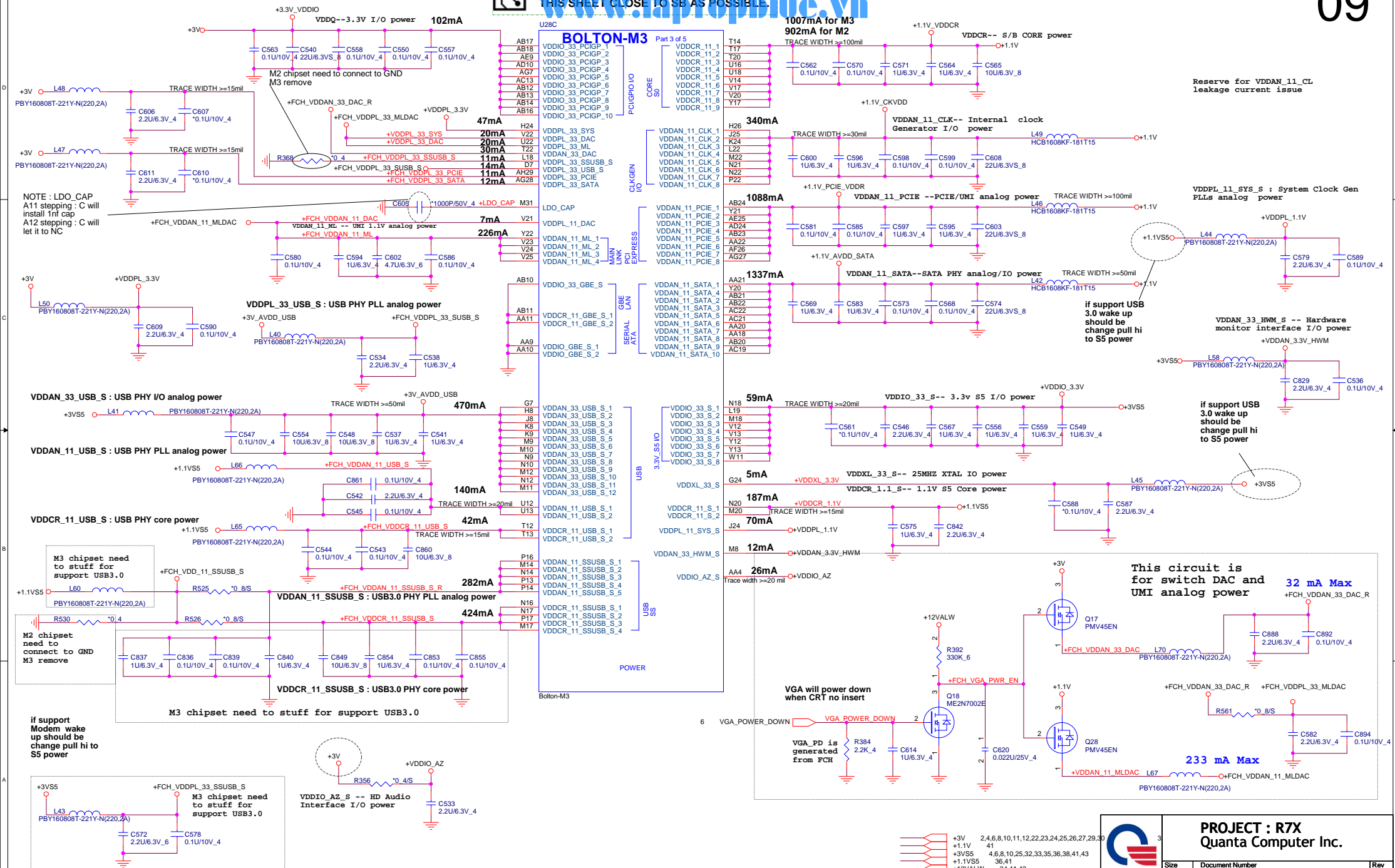
PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	FCH 3/5(SATA/VGA/GND/SPI)	1A
Date: Tuesday, March 12, 2013	Sheet 8	of 43



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

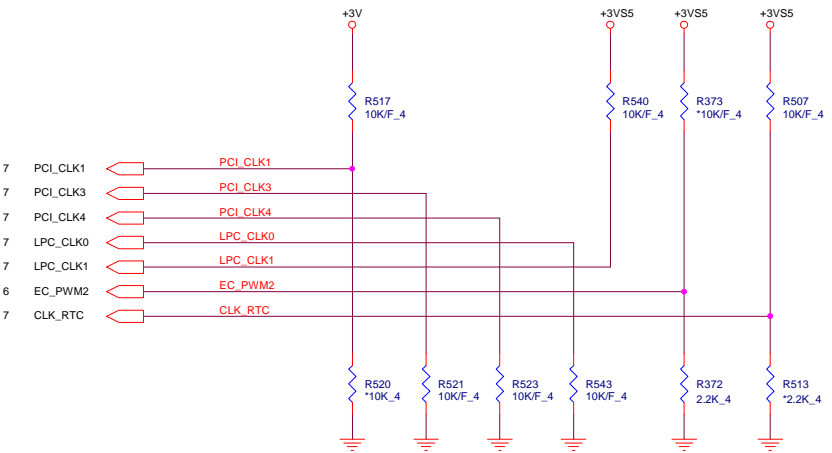
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

DEBUG STRAPS



REQUIRED STRAPS

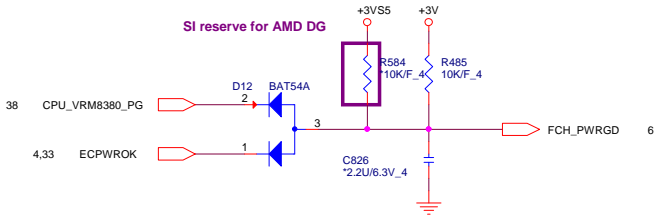
	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

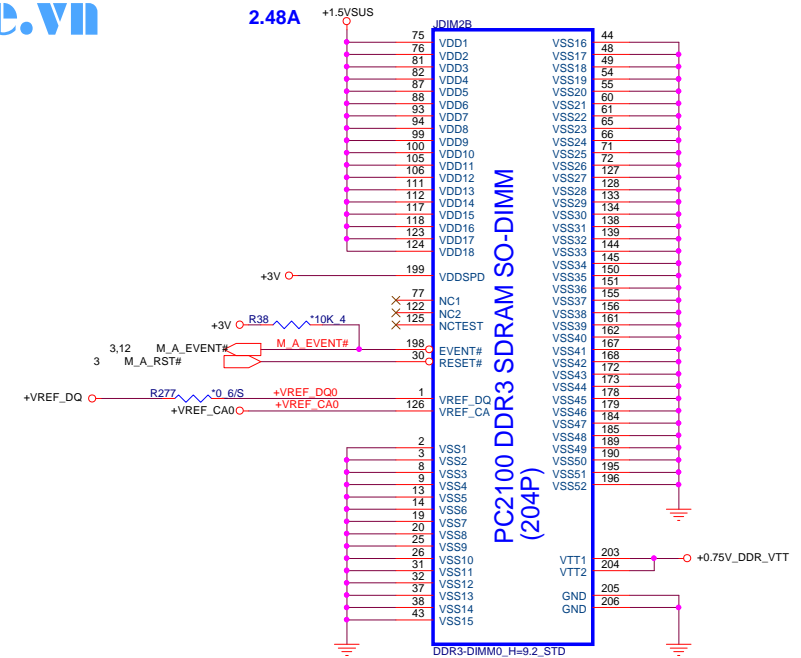
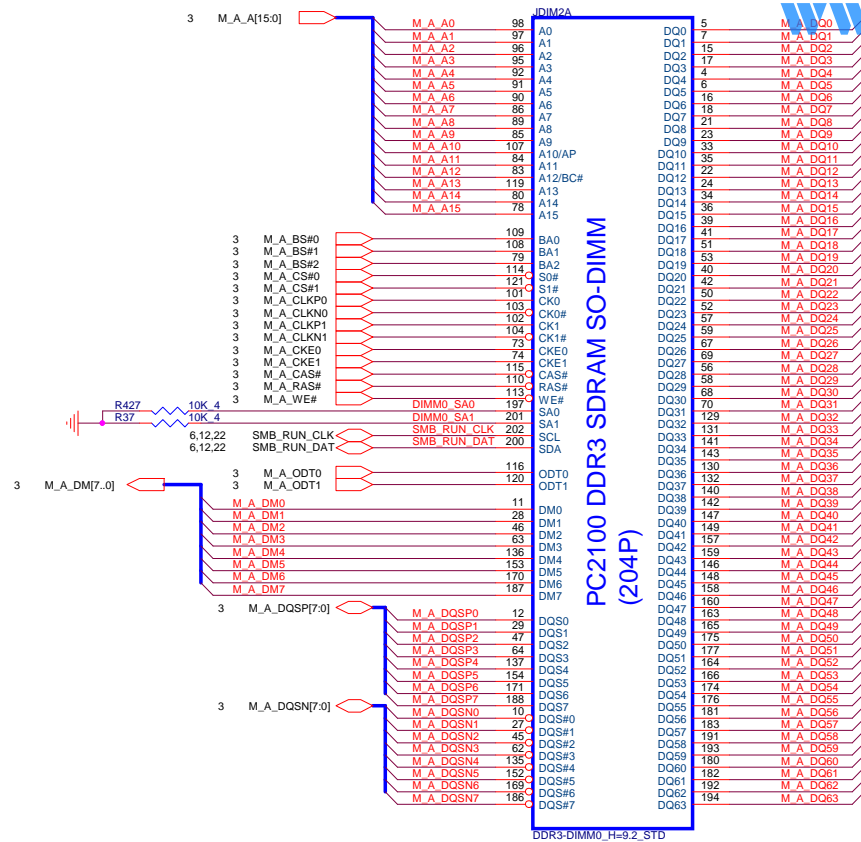
FCH has 15K Internal Pull Up for PCI_AD[27:23]



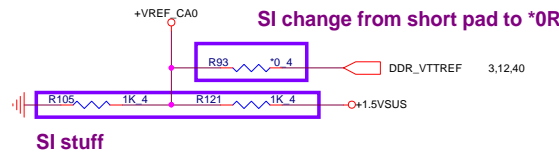
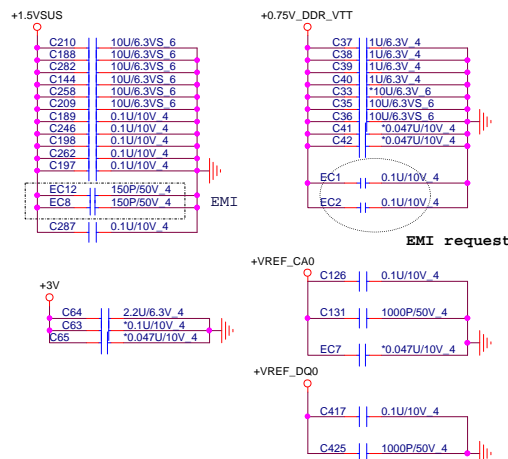
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH_PWRGD

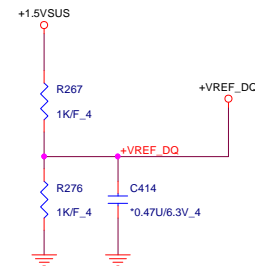
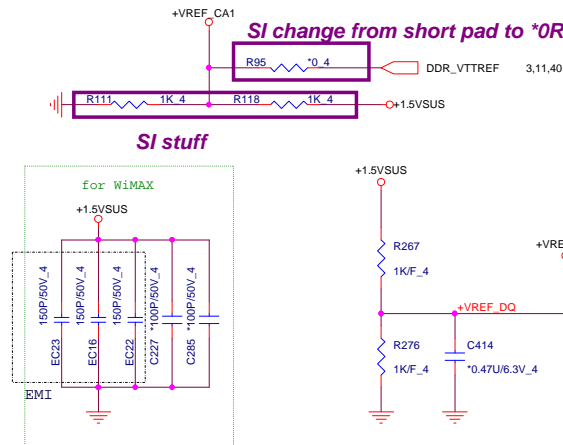
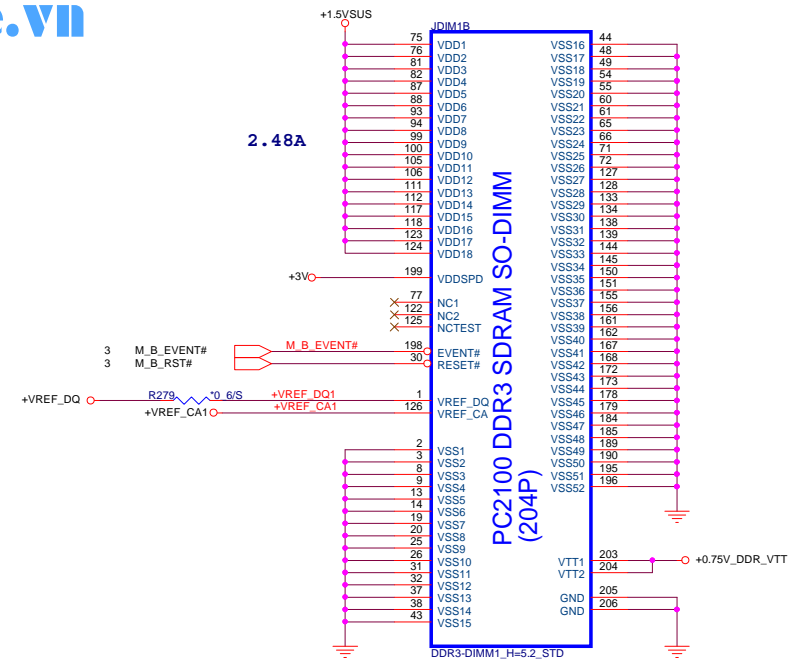




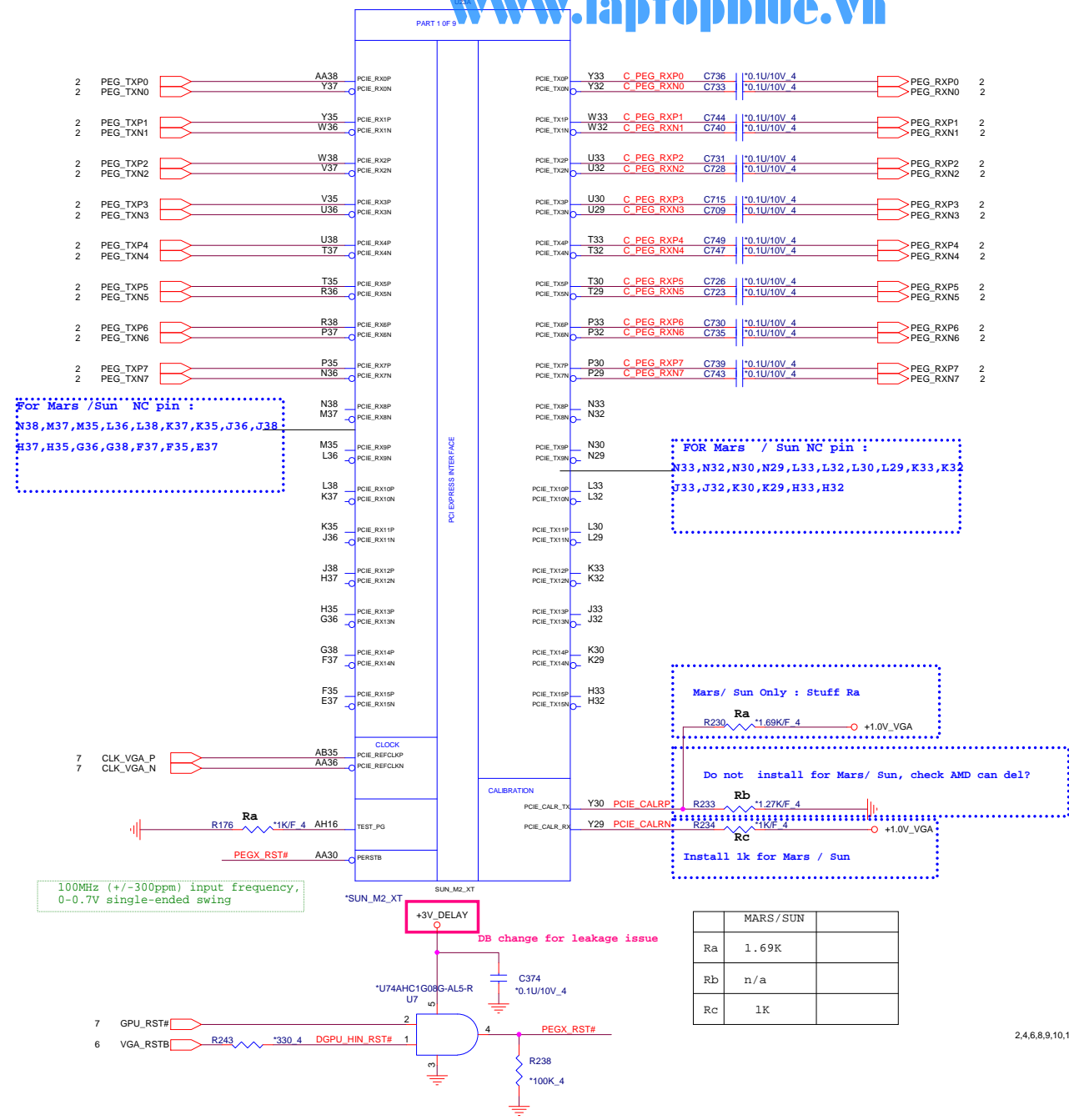
Place these Caps near So-Dimm0.



- +3V 2,4,6,8,9,10,12,22,23,24,25,26,27,29,30,31,32,33,41,42,43
- +1.5V 2,4,22,23,27,32,38,41
- +3VPCU 7,25,30,32,33,34,35
- +1.5VSUS 2,3,4,5,12,40,41,43
- +0.75V_DDR_VTT 12,40



+0.75V_DDR_VTT	11,40
+1.5VSUS	2,3,4,5,11,40,41,43
+3VPCU	7,25,30,32,33,34,35
+3V	2,4,6,8,9,10,11,22,23,24,25,26,27,29,30,31,32,33,41,42,43



2,4,6,8,9,10,11,12,22,23,24,25,26,27,29,30,31,32,33,41,42,43
15,17,18,43 +3V +1.0V_VGA

PROJECT : R7X
Quanta Computer Inc.

Size Custom	Document Number SUN_PCIE_Interface	Rev 1A
Date: Tuesday, March 12, 2013 Sheet 13 of 43		

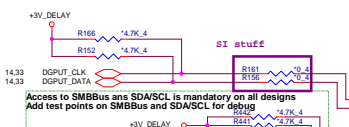
PS3 BIT3=>BIT1 [3:0]	Vendor	QBCW	Vendor P/N	QCI P/N (TOP B/S)
011	Hynix	128Mx16 *4	H5TC2G63PFR-11C	AKD5N2P7W02
100	Micron	128Mx16 *4	MT41J128M16JT-093G:K	AKD5M8TLL16
101	Samsung	128Mx16 *4	K4W2G1646E-BC1A	AKD5MGT534

Only for Test

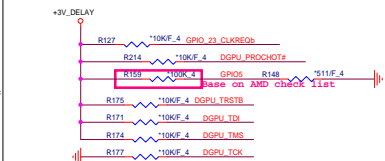
PS3 BIT3=>BIT1 [3:0]	Vendor	QBCW	Vendor P/N	QCI P/N
000	Hynix	256Mx16 *4	H5TC4G63APR-11C	AKD5P0WTW07
001	Micron	256Mx16 *4	MT41J256M16HA-093G:E	AKD5P2ZTL00
010	Samsung	256Mx16 *4	K4W4G1646E-BC1A	AKD5P2DT500

Vendor	QBCW	Vendor P/N
Samsung 2GB VRAM	AKD5MGT535	K4W2G1646E-BC1A
Samsung 4GB VRAM	AKD5PZDT501	K4W4G1646E-BC1A
Hynix 2GB VRAM	AKD5M2DTW03	H5TC2G63PFR-11C
Hynix 4GB VRAM	AKD5P0WTW08	H5TC4G63APR-11C
Micron 2G VRAM	AKD5MGTLL17	MT41J128M16JT-093G:K
Micron 4G VRAM	AKD5PZTL01	MT41J256M16HA-093G:E

For Sun only :
AP10 / AV11 / AT11 / AR12 / AM12 / AU12 / AP12 : NC pin



Access to SMBus and SDA/SCL is mandatory on all designs
Add test points on SMBus and SDA/SCL for debug

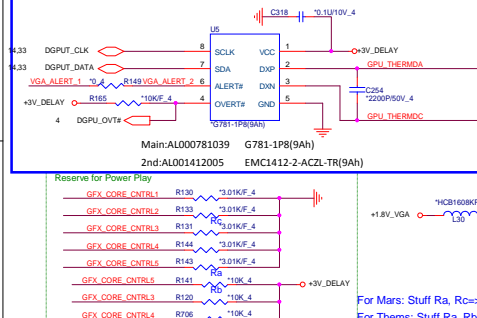


SI add TEMP FAIL circuit for SUN XT

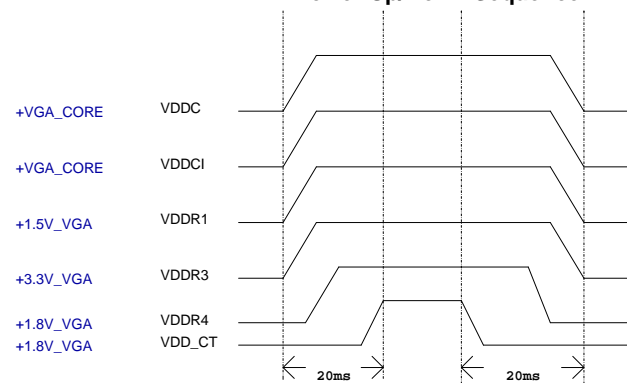
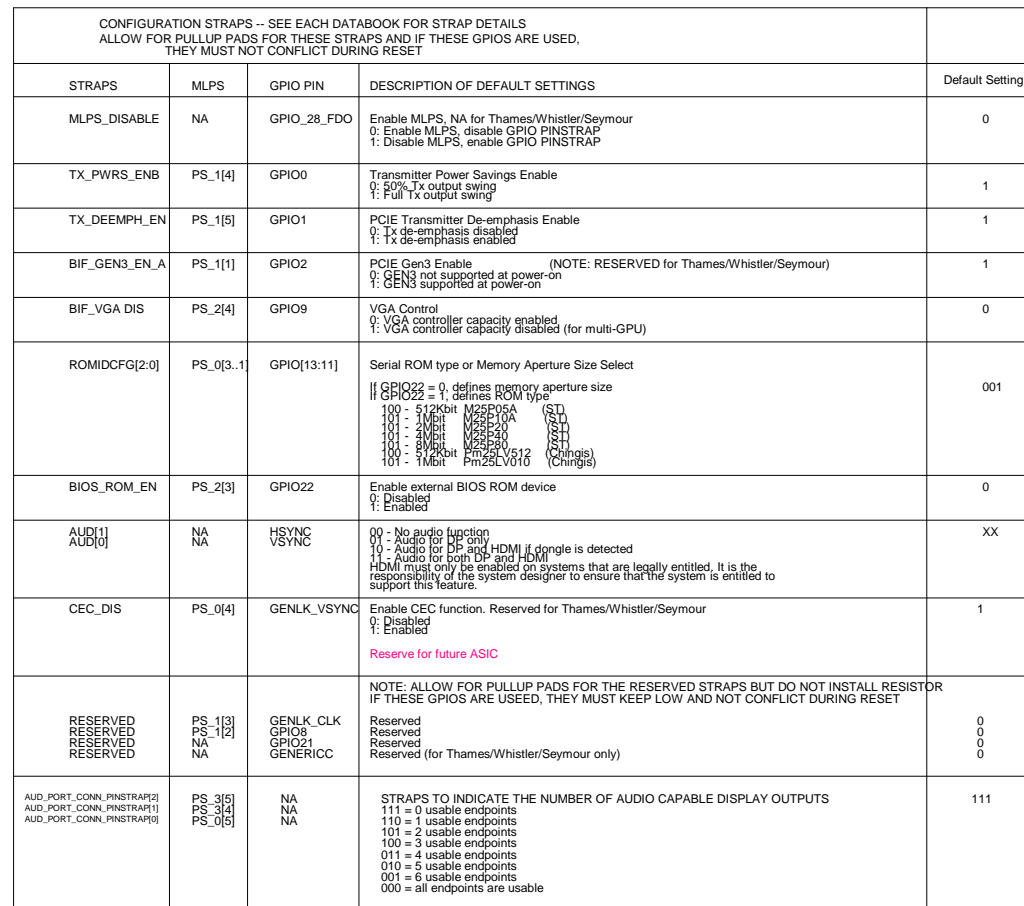
For SUN GPIO NC PIN : AJ19 / AK19 / AR24 / AK14 / AM14 / AJ24 / AR26 / AR24 / AJ20
AK20 / AR18 / AR16 / AK17 / AK16 / AL16 / AM16

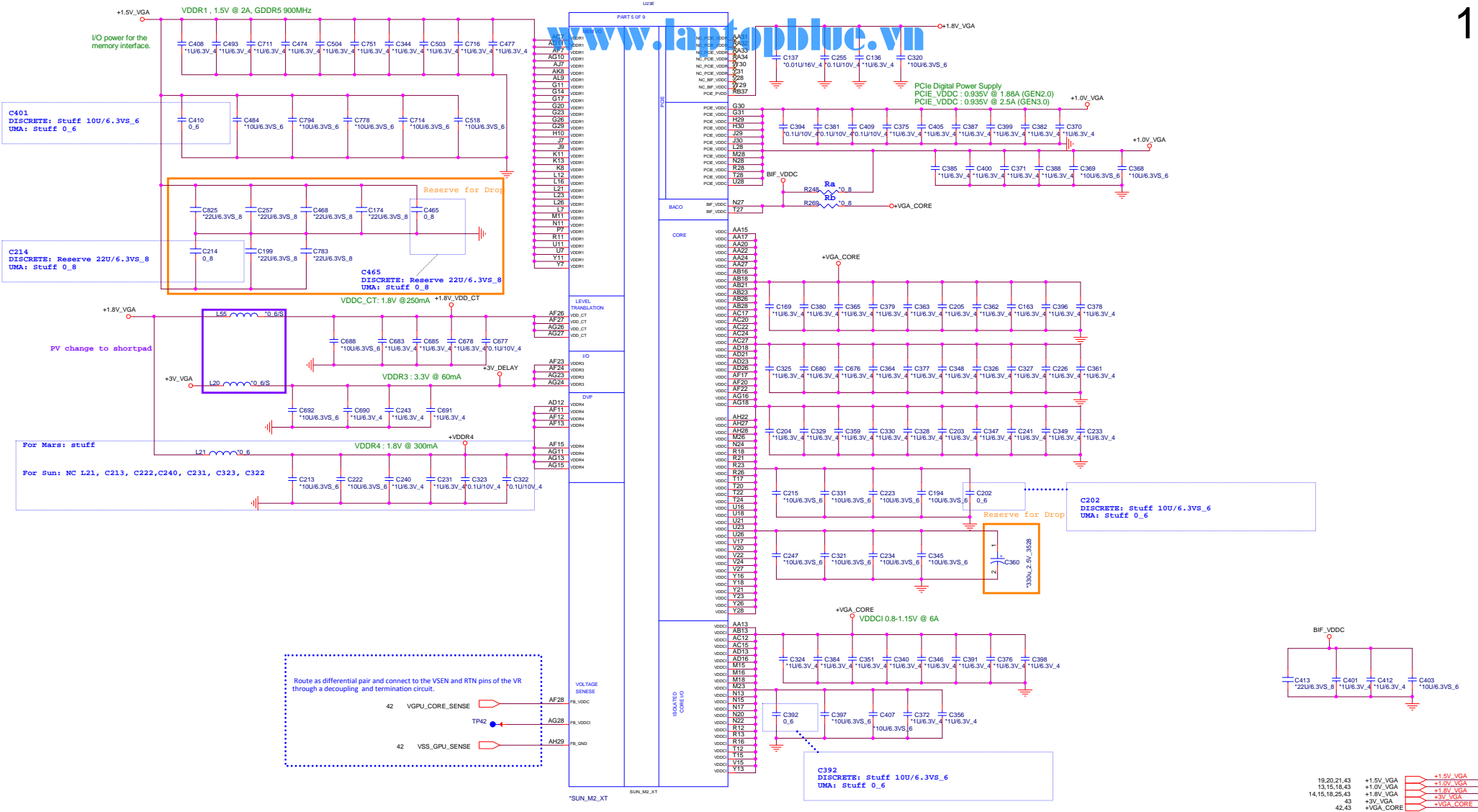
Mars: stuff
For Sun R140, R124, C148

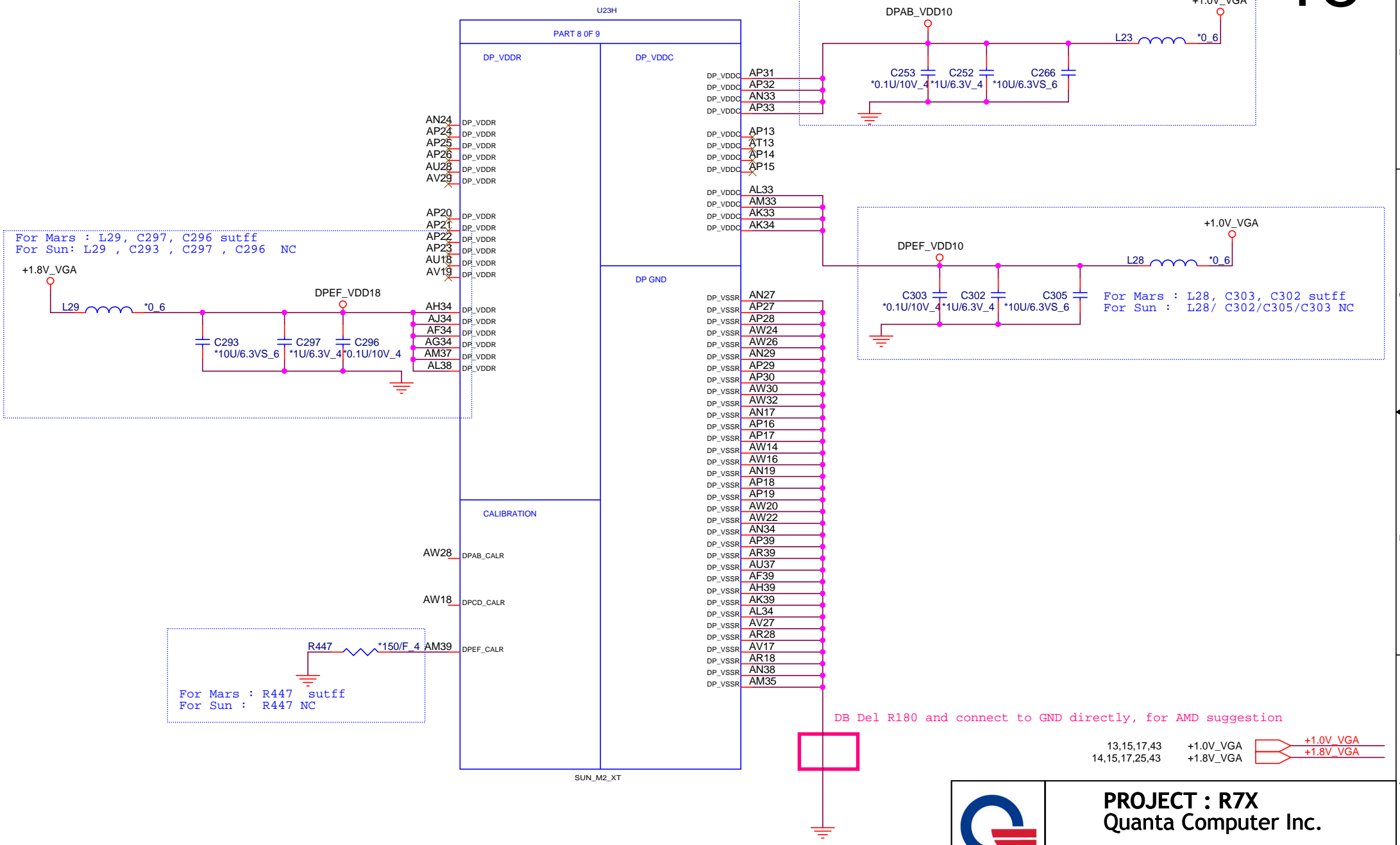
Thermal Solution(Close to GPU)





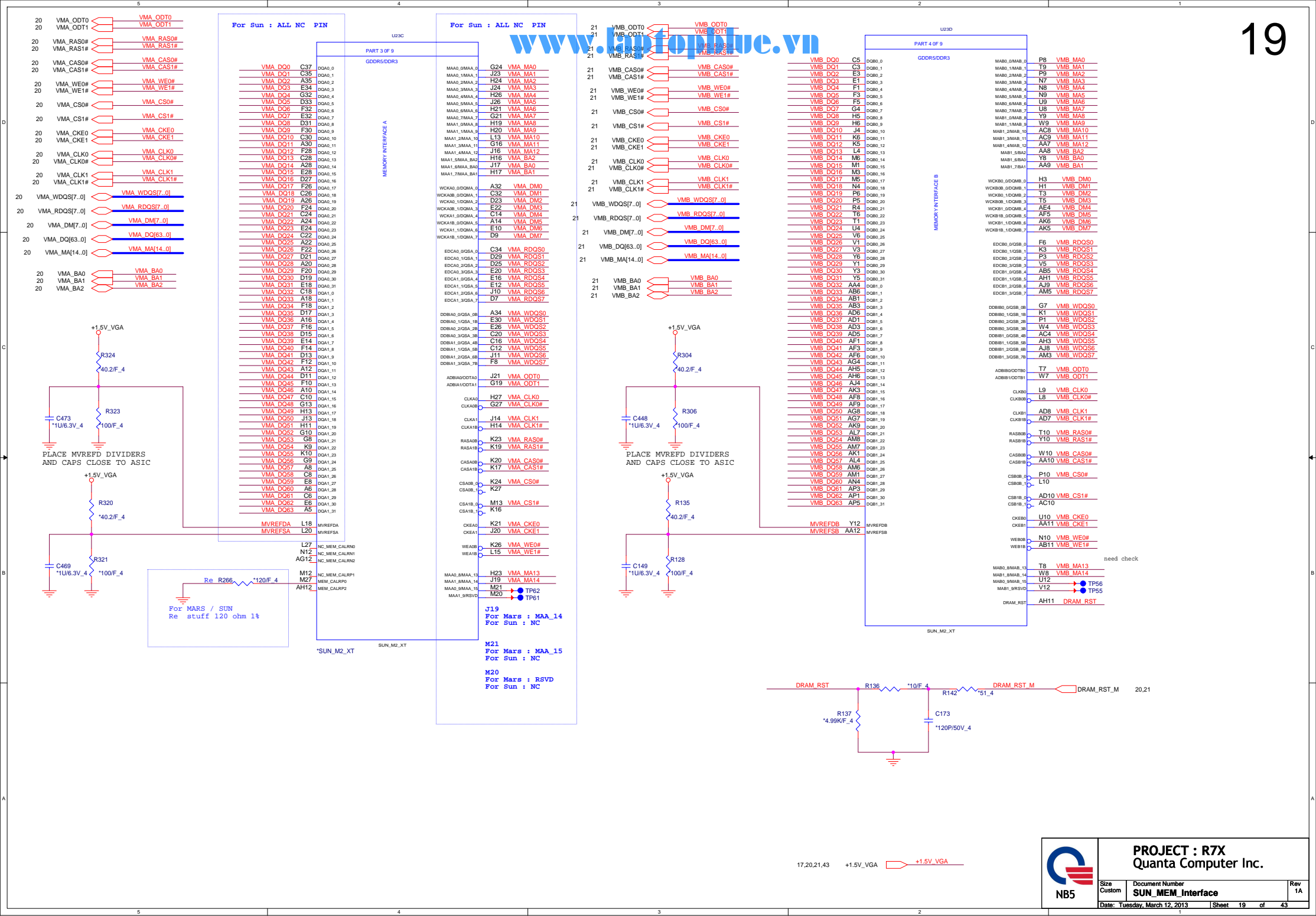


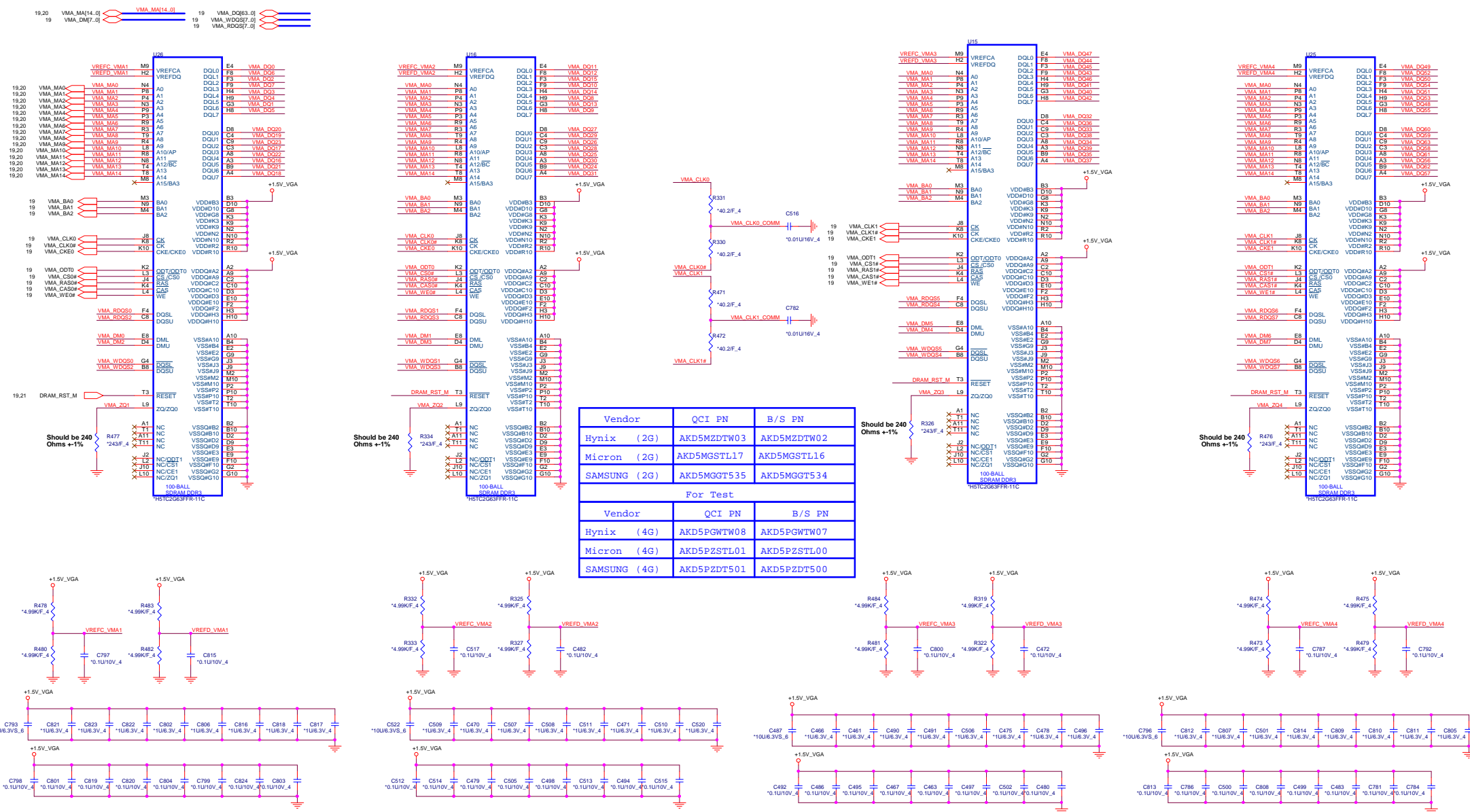




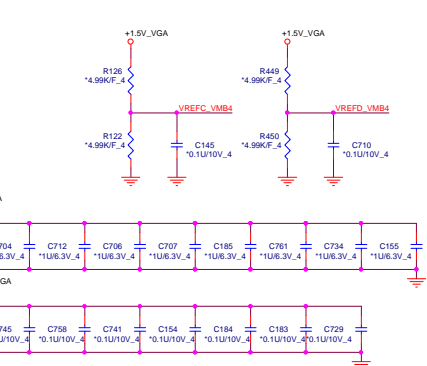
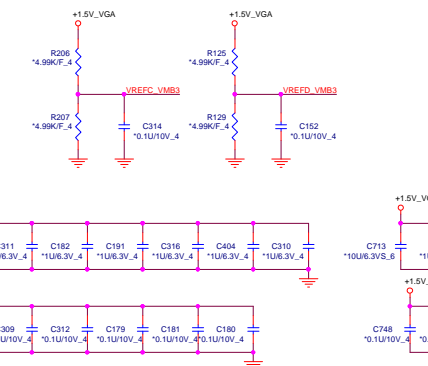
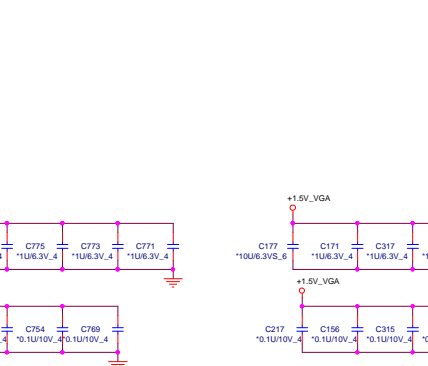
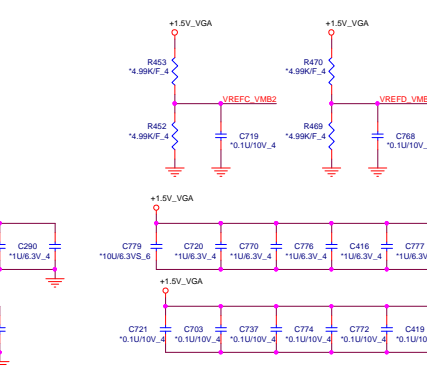
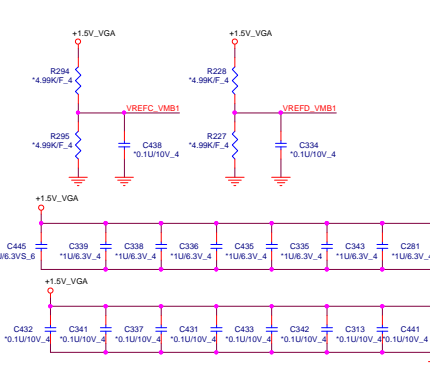
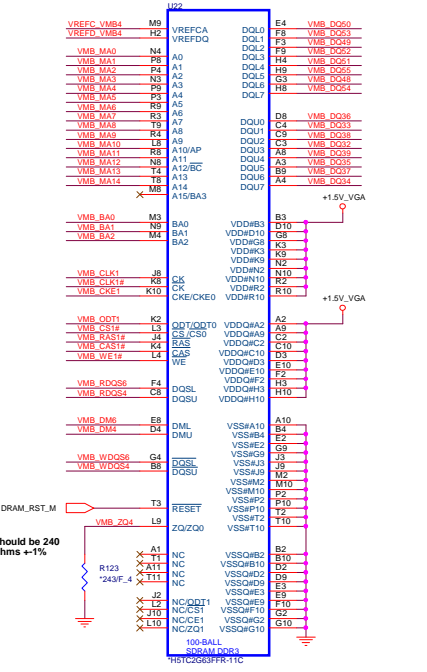
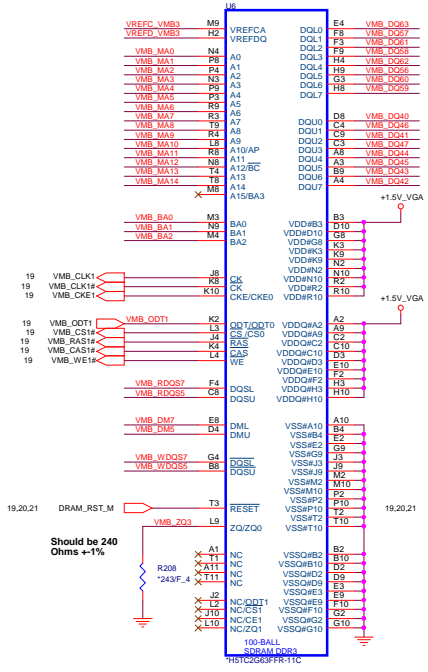
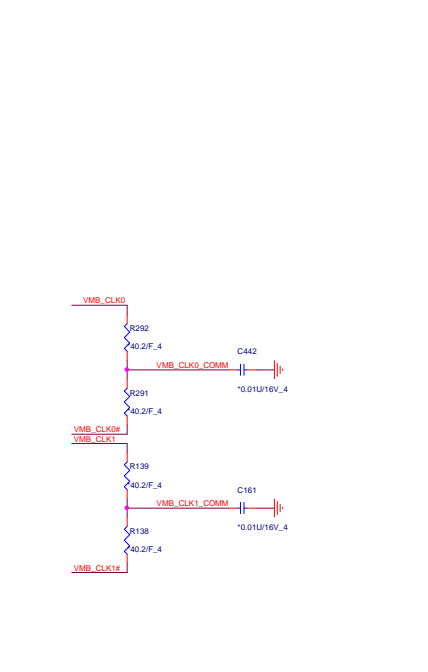
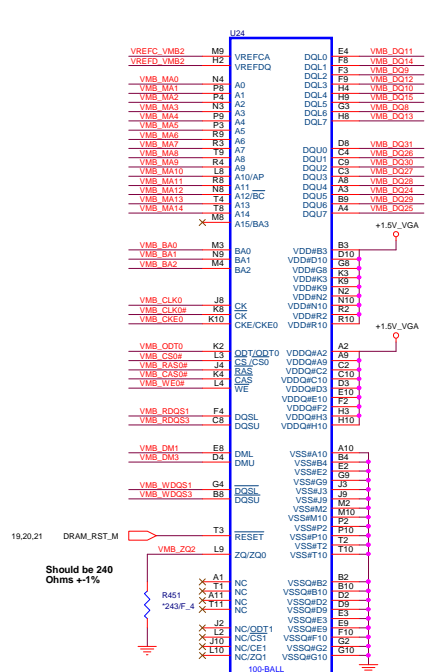
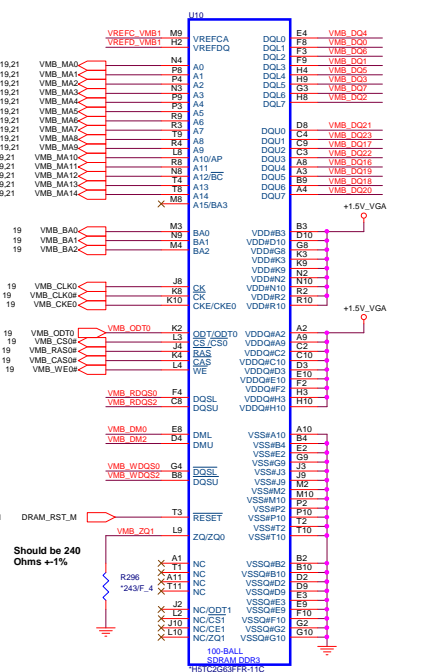
PROJECT : R7X
Quanta Computer Inc.

Size Custom	Document Number SUN_DP Powers	Rev 1A
Date: Tuesday, March 12, 2013	Sheet 18 of 43	

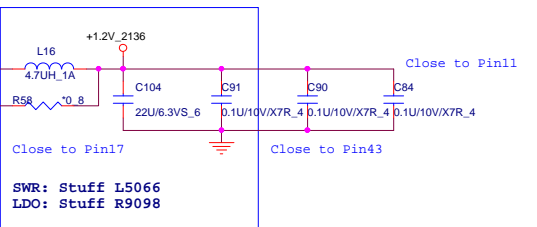
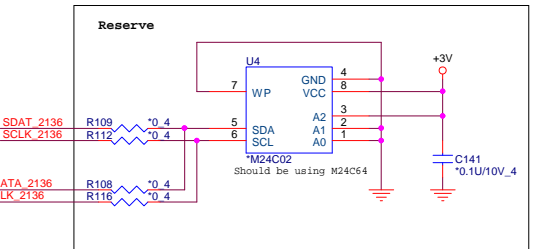
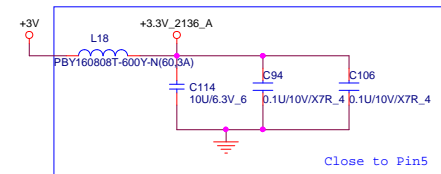
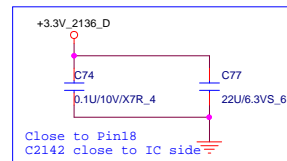
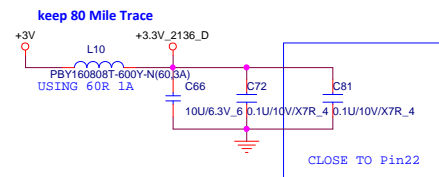
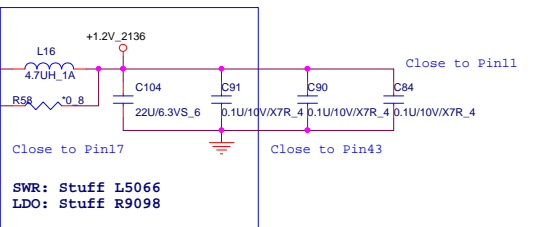
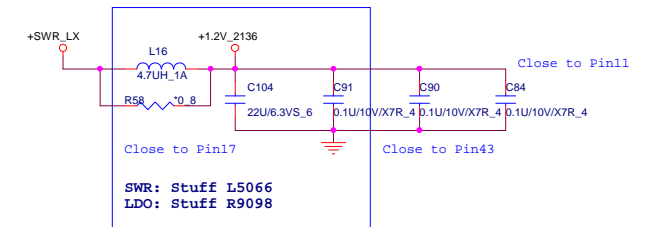




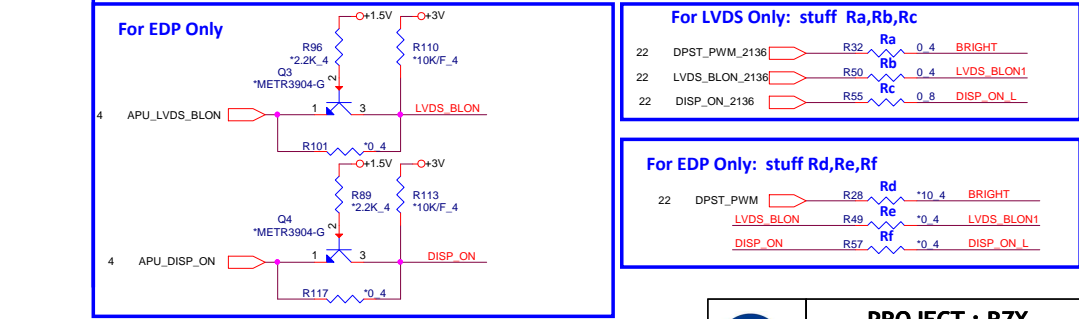
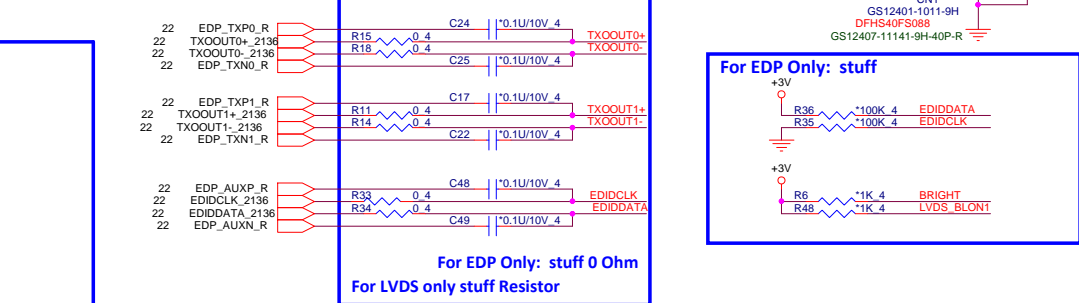
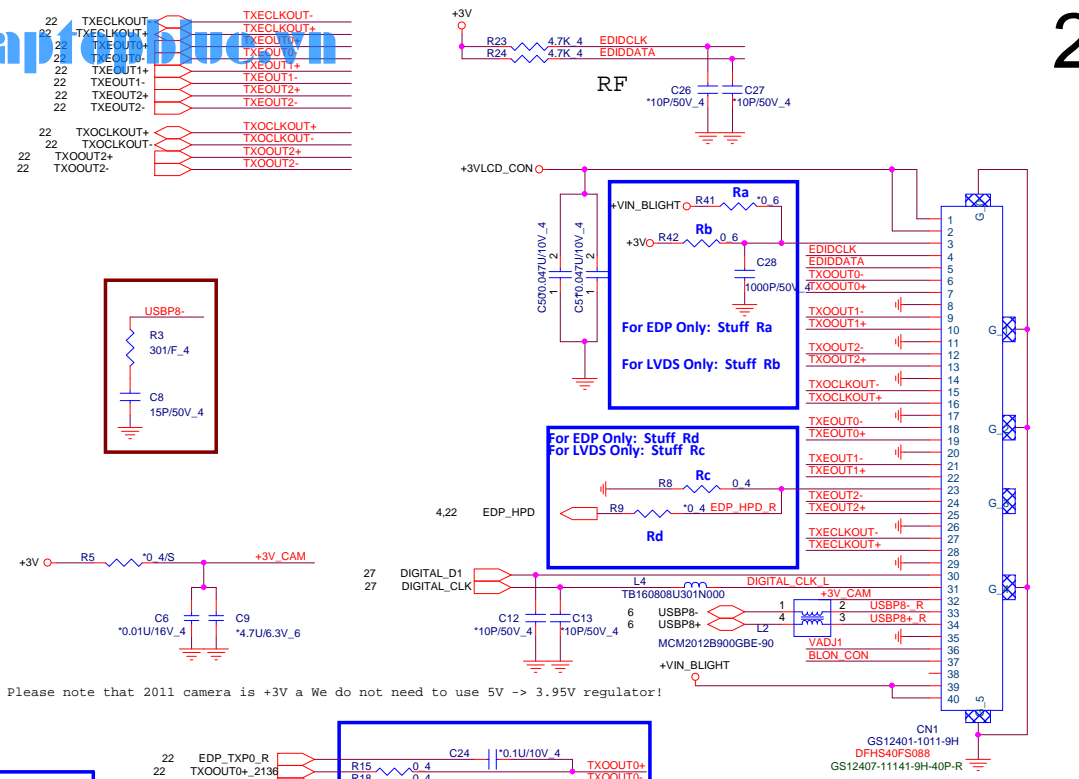
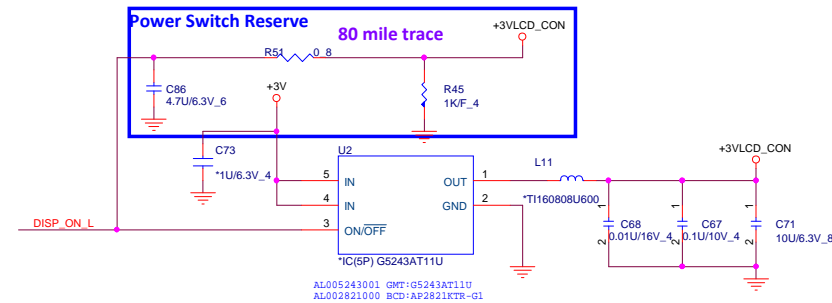
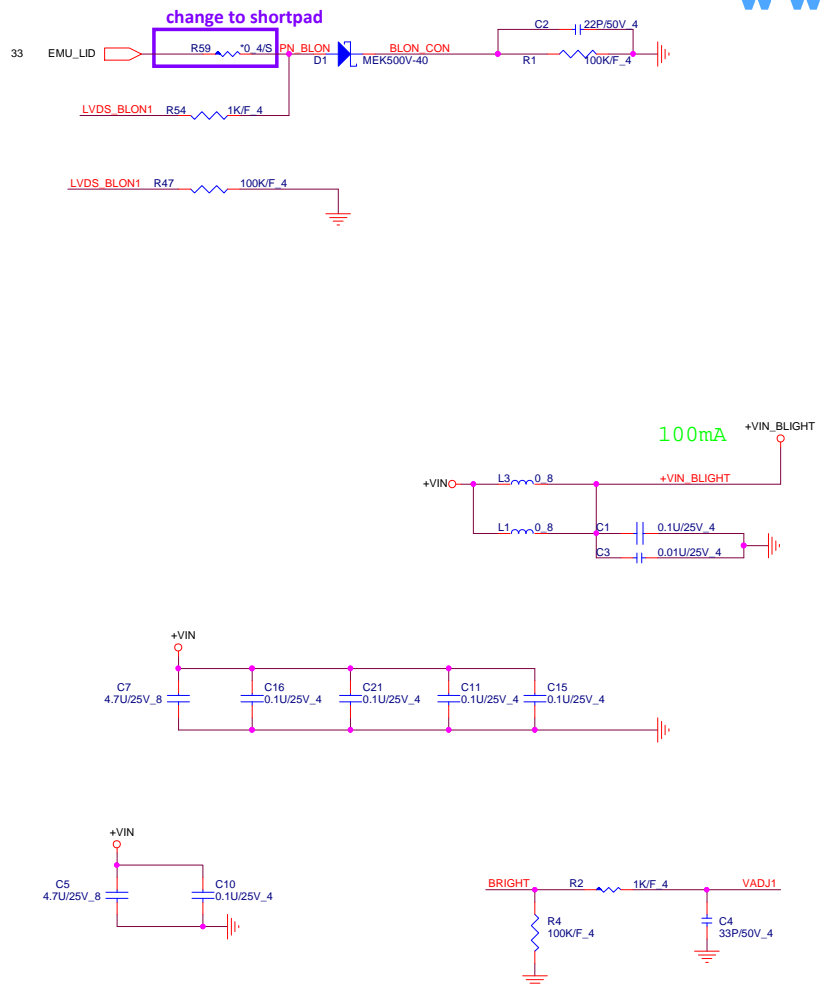
CHANNEL B: 256MB/512MB DDR3



17,19,20,21,43 +1.5V_VGA
17,19,20,21,43 +1.5V_VGA

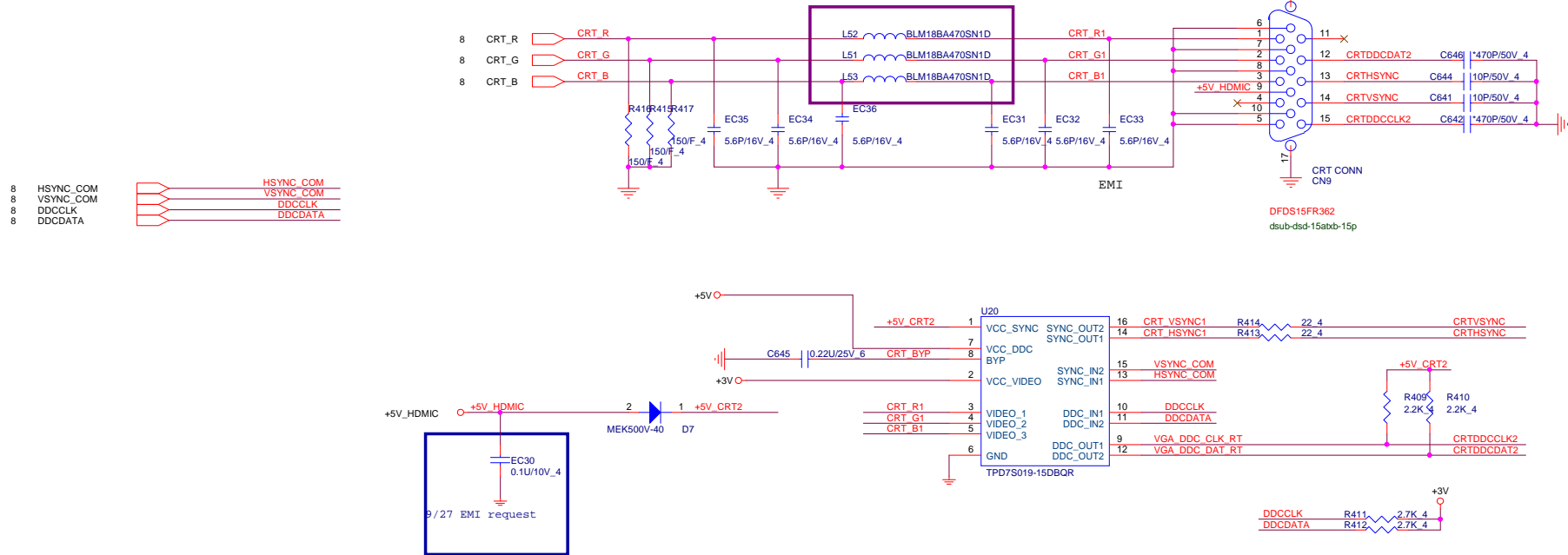


LID Switch



CRT PORT

SI change to 47Ω bead, BLM18BA470SN1D for solve CRT rise/fall time issue



HOLE

HOLE

FAN hole

PCH BKT

CPU BKT

VGA BKT

Nut PN:MBBU2005010

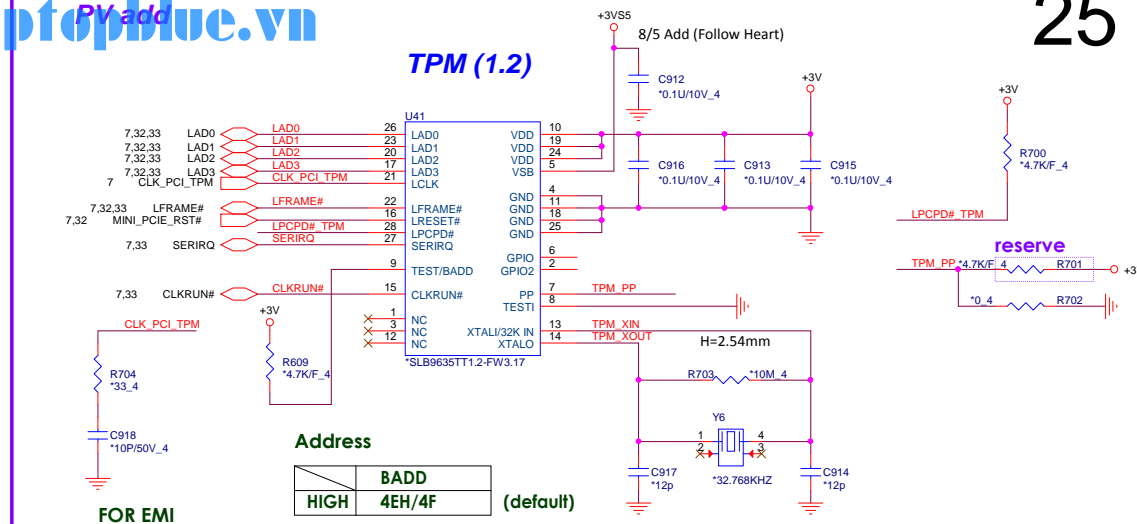
THERMAL BKT

KB lock

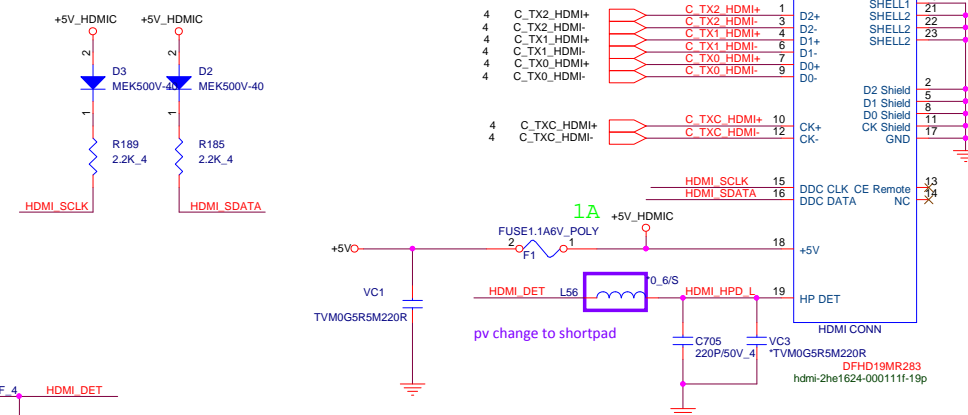
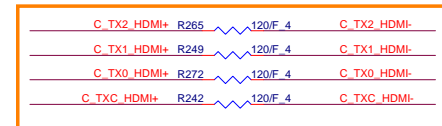
SI add

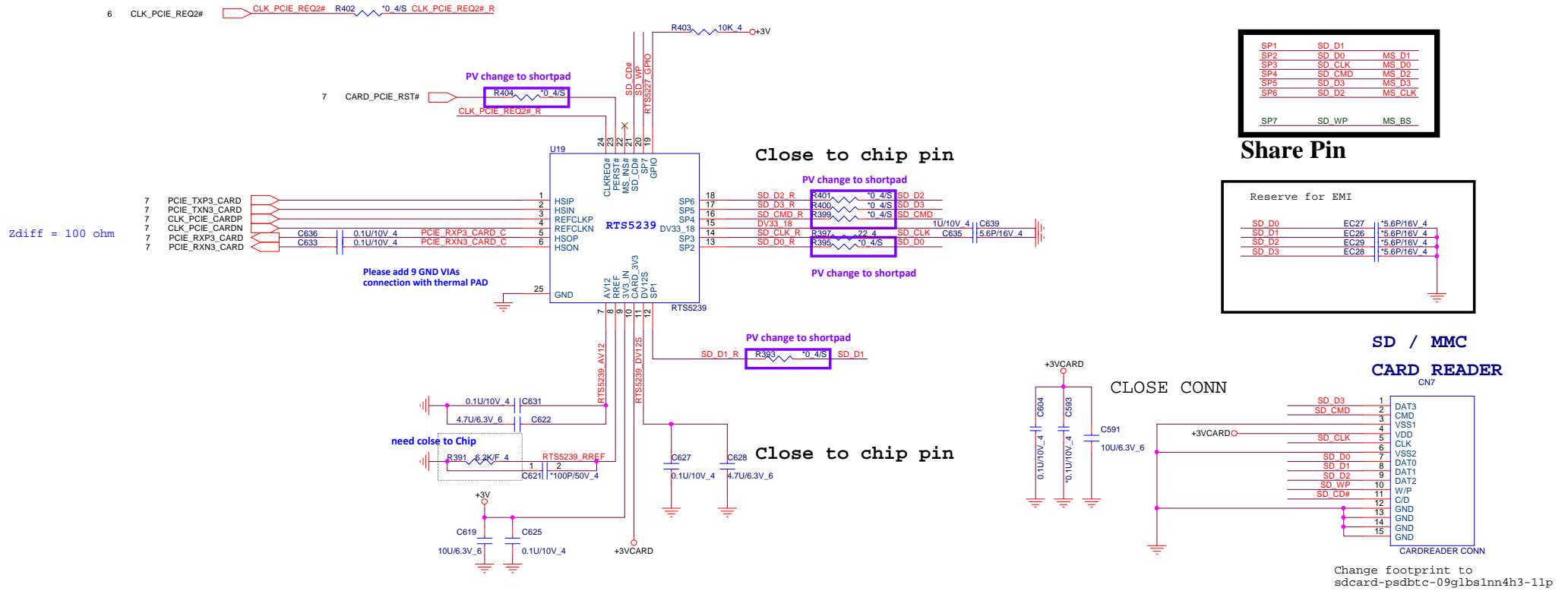
MV add

	PROJECT : R7X Quanta Computer Inc.		
	Size Custom	Document Number CRT,Hole	Rev 1A
	Date: Tuesday, March 12, 2013	Sheet 24	of 43

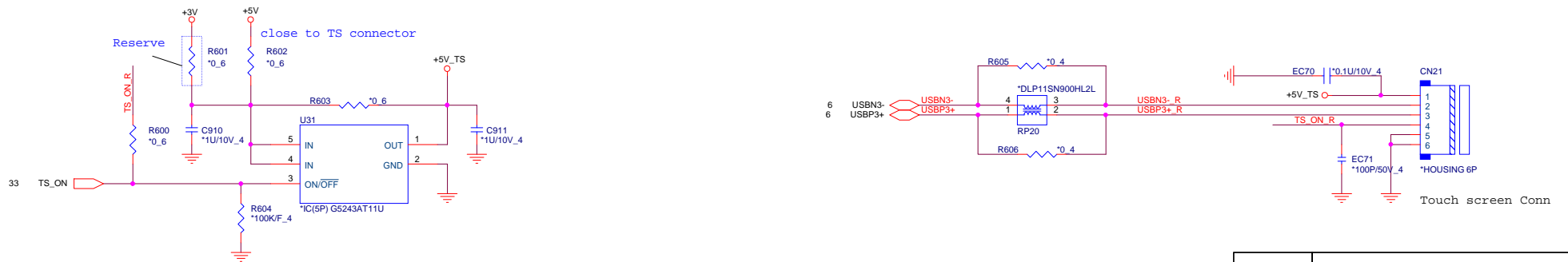


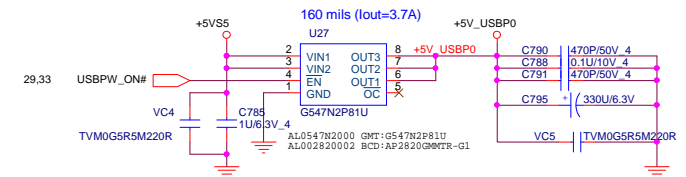
EMI request



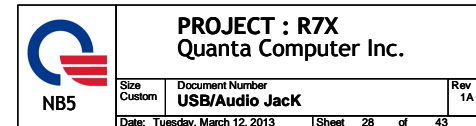


Touch Screen Connector

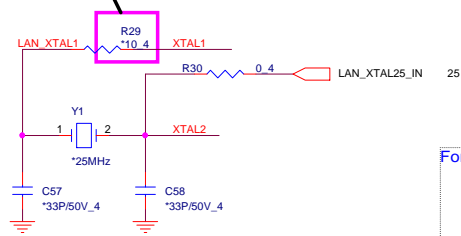




PCB layout for the audio section of the AJAK0017-P001A module. The layout shows the connection of external microphone (EXT_MIC_R, EXT_MIC_1) and headset (HPOUT_L, HPOUT_R) signals to the module's internal components. Key components include resistors R534, R536, R518, R535, R537, capacitors C841, C530, C526, C835, C863, and a clamp diode C909. The layout also shows the connection to the module's internal components via the CN16 connector. The layout is labeled "SI reserve for ESD".

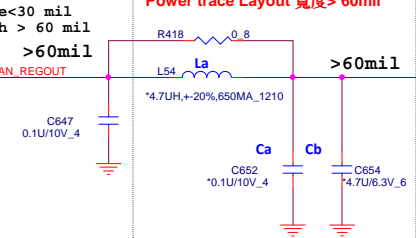


For EMI 0 ~ 22 ohm



For GbE
* Place Cc,Cd,Ce,Cf
close to each VDD10 pin-- 3, 8, 22, 30

For 10/100 NA Ce,Cf
* Place Cc, Cd
close to each VDD10 pin-- 8, 30 only,



For GbE
Stuff La, Ca, Cb

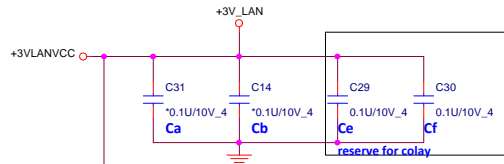
For 10/100
NA: La, Ca, Cb

For GbE
* Place Cg close to each VDD10 pin-- 22 (reserve)

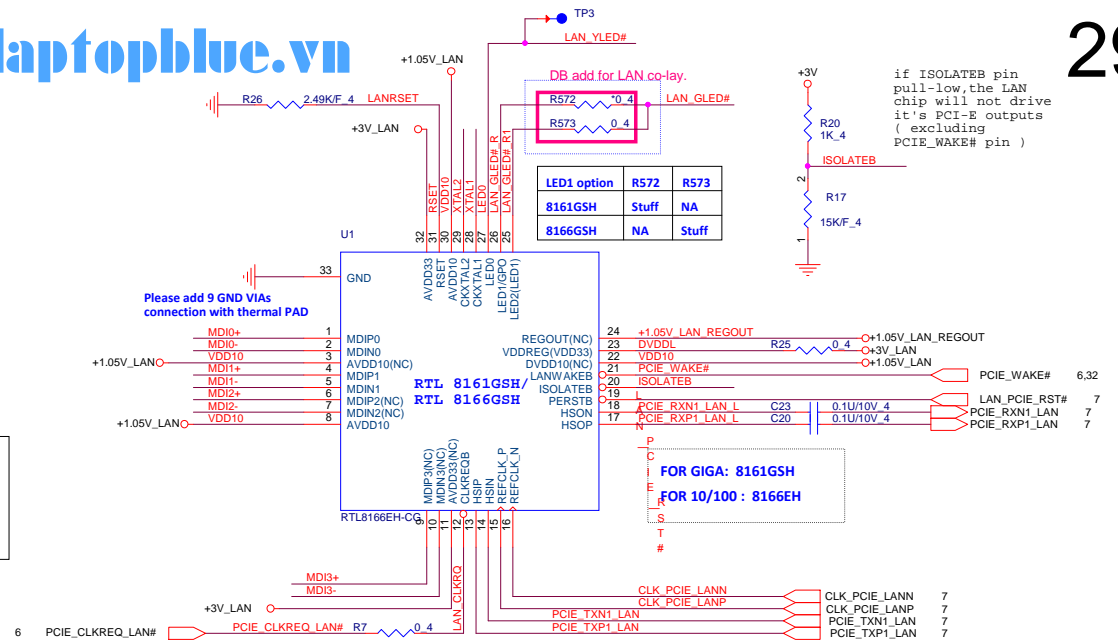
For 10/100
* Place Cf close to each VDD10 pin-- 30 (reserve)

For 10/100
* Stuff Ce and Cf only, close to each VDD33 pin-- 23, 32

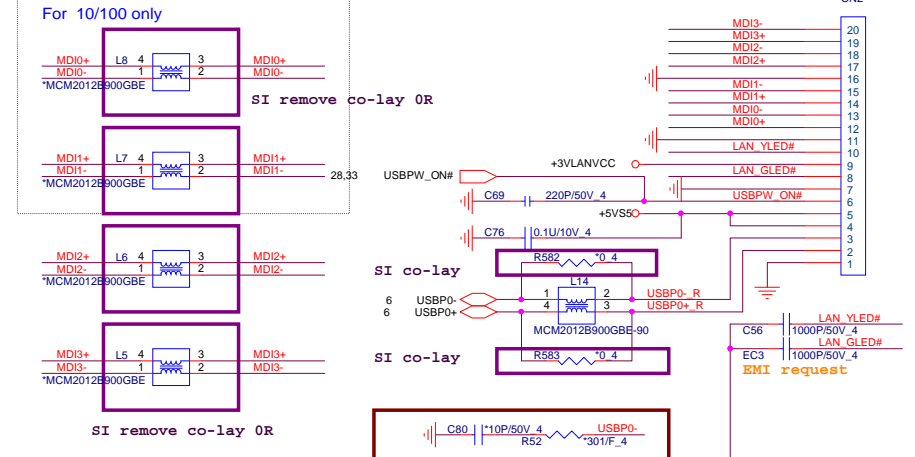
For GIGA
* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32



* Place Cc and Cd close to each VDD33 pin-- 23, 32
For GIGA
Stuff Cc, Cd
For 10/100
NA: Cc, Cd
Remove For Not Using SWR mode



LAN conn & Right SIDE USBX1

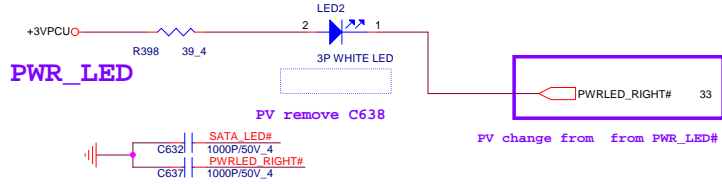
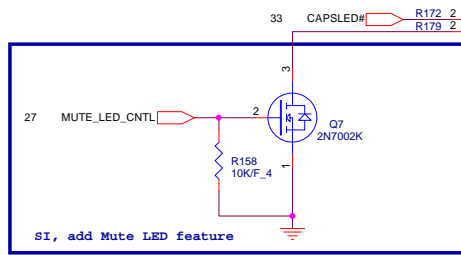
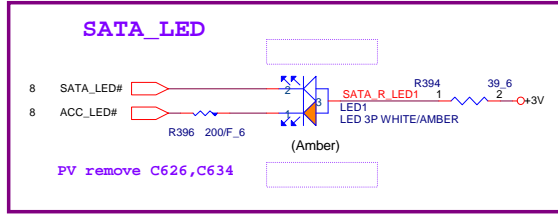


2,4,6,8,9,10,11,12,22,23,24,25,26,27,30,31,32,33,41,42,43
25,41

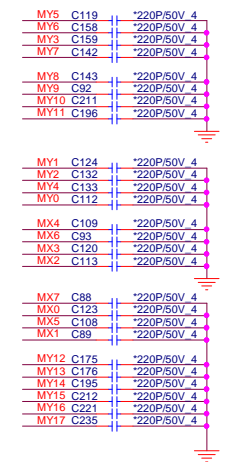
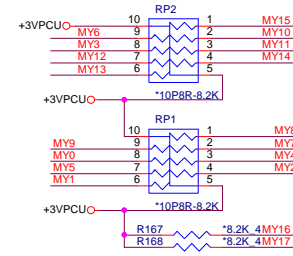
+3V
+3VLANVCC

KEYBOARD Con.

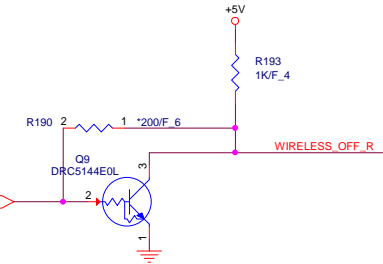
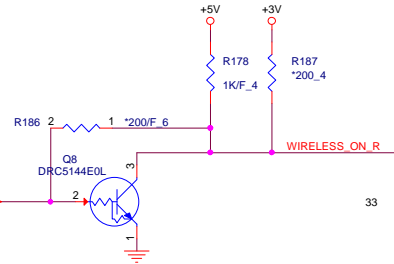
CNS



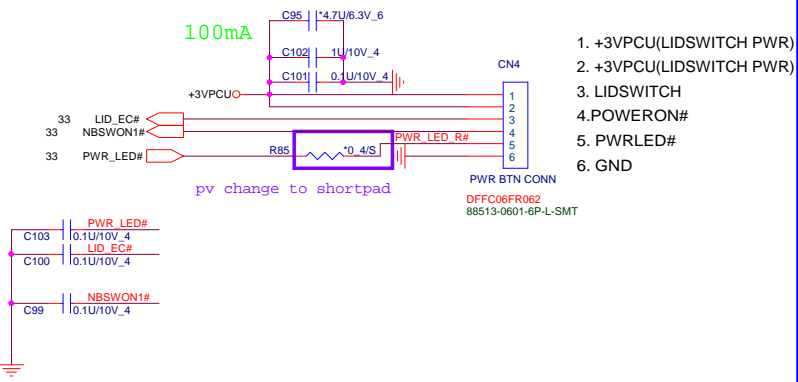
KEYBOARD PULL-UP



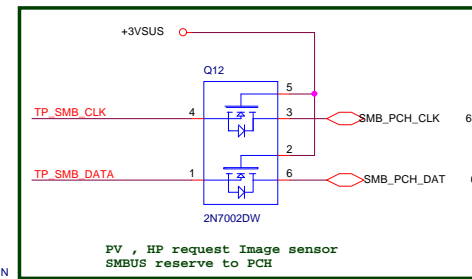
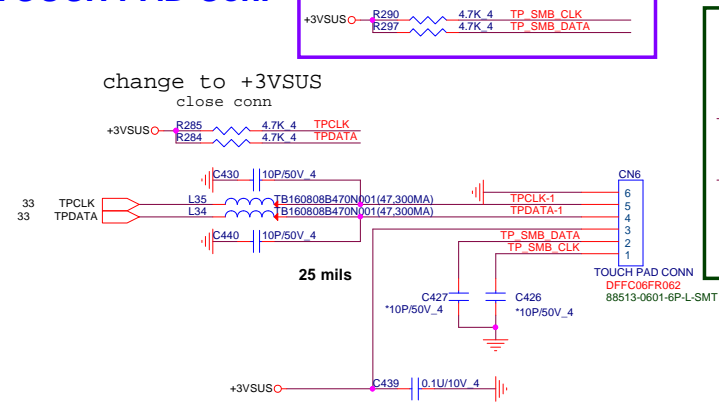
KB CONN
DFFC32FR038
50698-03201-001-32p4



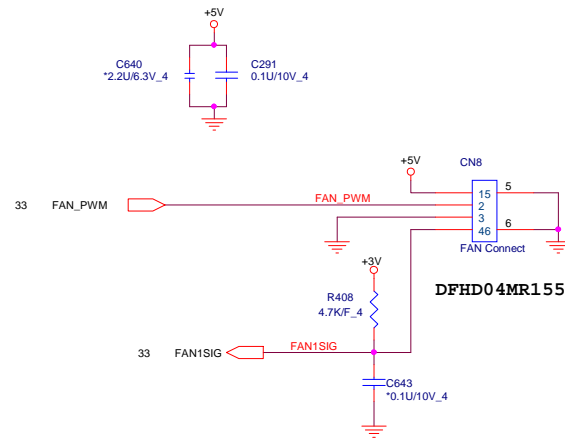
POWER BOTTON CONNECT



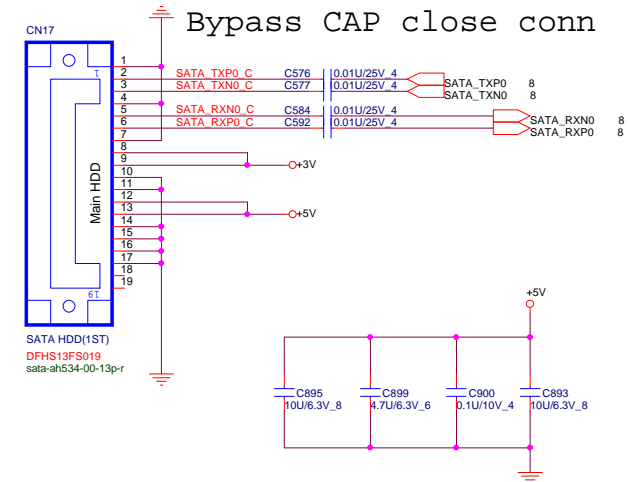
TOUCH PAD Con.



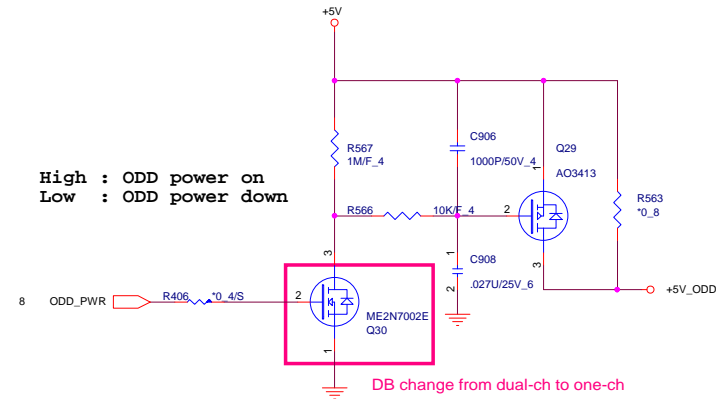
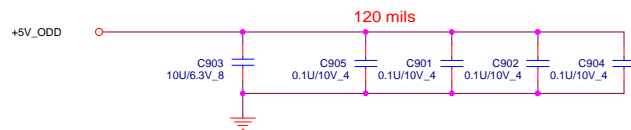
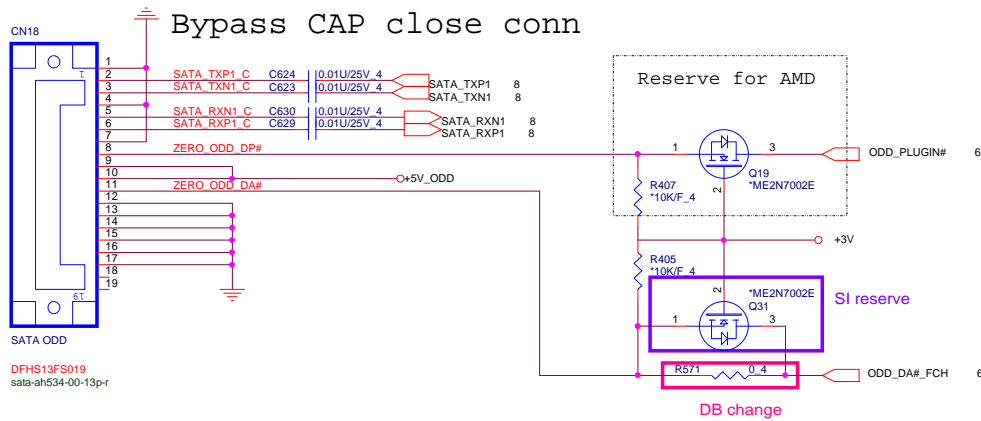
CPU FAN

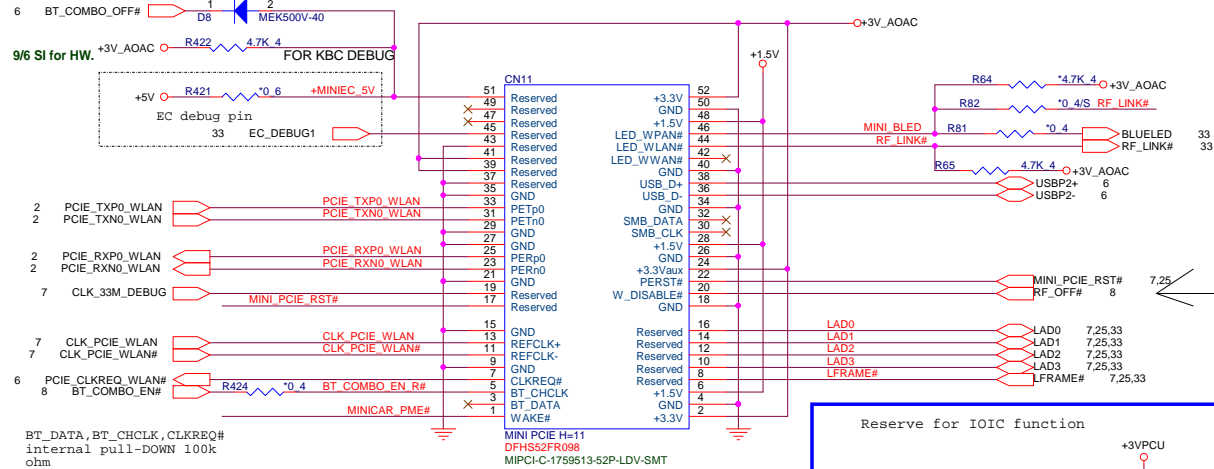


SATA HDD CONNECTOR



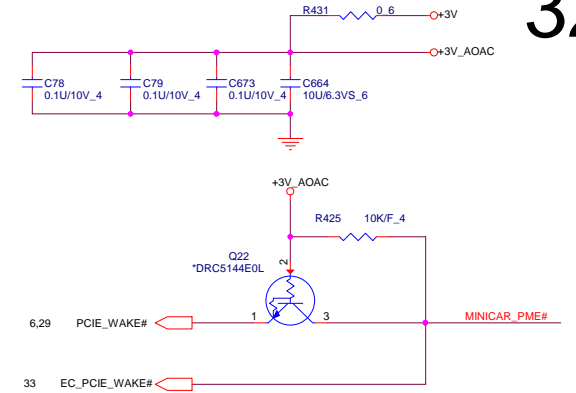
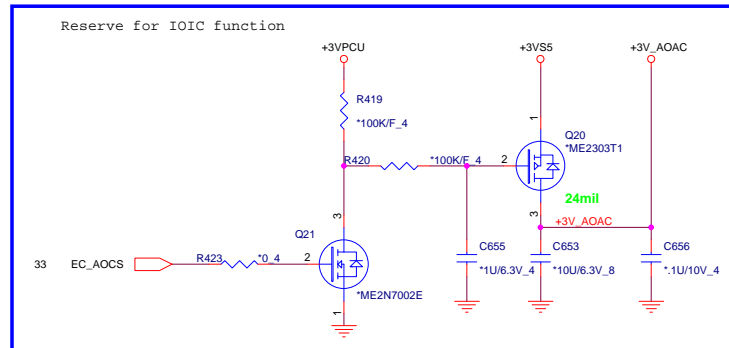
SATA ODD CONNECTOR



Mini PCI-E Card 1
WLAN

CLK_33M_DEBUG R53 *0.4 EC4 *33P/50V_4

for EMI request



2,4,6,8,9,10,11,12,22,23,24,25,26,27,29,30,31,33,41,42,43

2,4,22,23,27,38,41

+1.5V

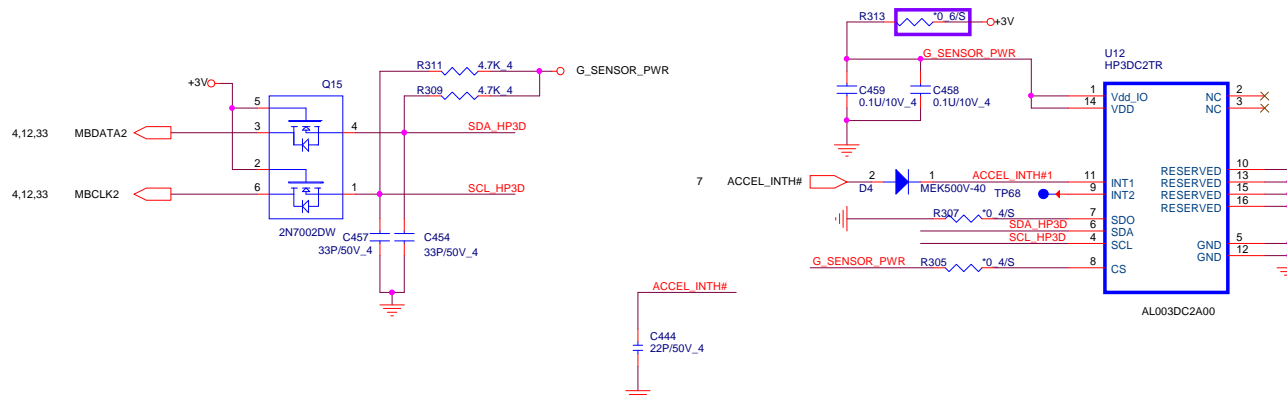
+3V

+3VPCU

+5V

Accelerometer Sensor

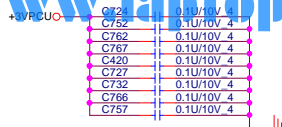
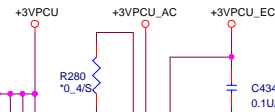
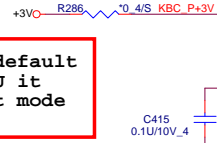
PV change to shortpad



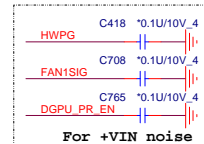
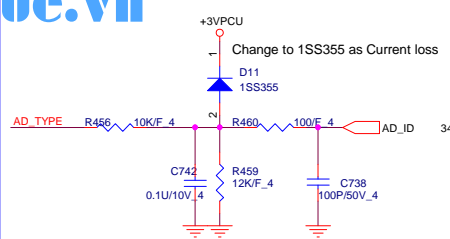
2,4,6,8,9,10,11,12,22,23,24,25,26,27,29,30,31,32,41,42,43
7,25,30,32,34,35
34,35,36



ITE pin 100 , 104 , 106 default
can not pull up to +3VPCU it
will cause chip into test mode

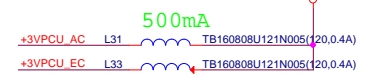


+3VPCU CAP close to EC pin

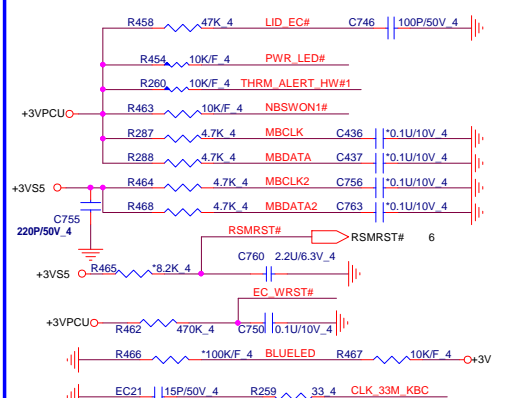
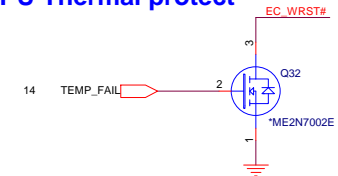


For +VIN nois

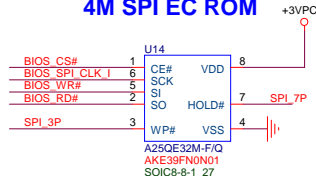
Vender	Size	P/N
AMIC	4M	AKE39ZN0800
EON	4M	AKE39ZN0Q03
WINBOND	4M	AKE39FN0N01
Socket		DFHS08FS023



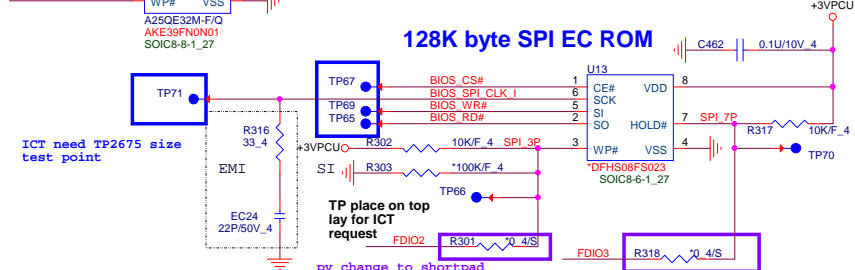
DGPU Thermal protect



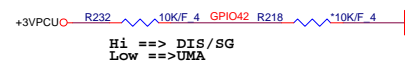
4M SPI EC ROM



128K byte SPI EC ROM



Adapter select

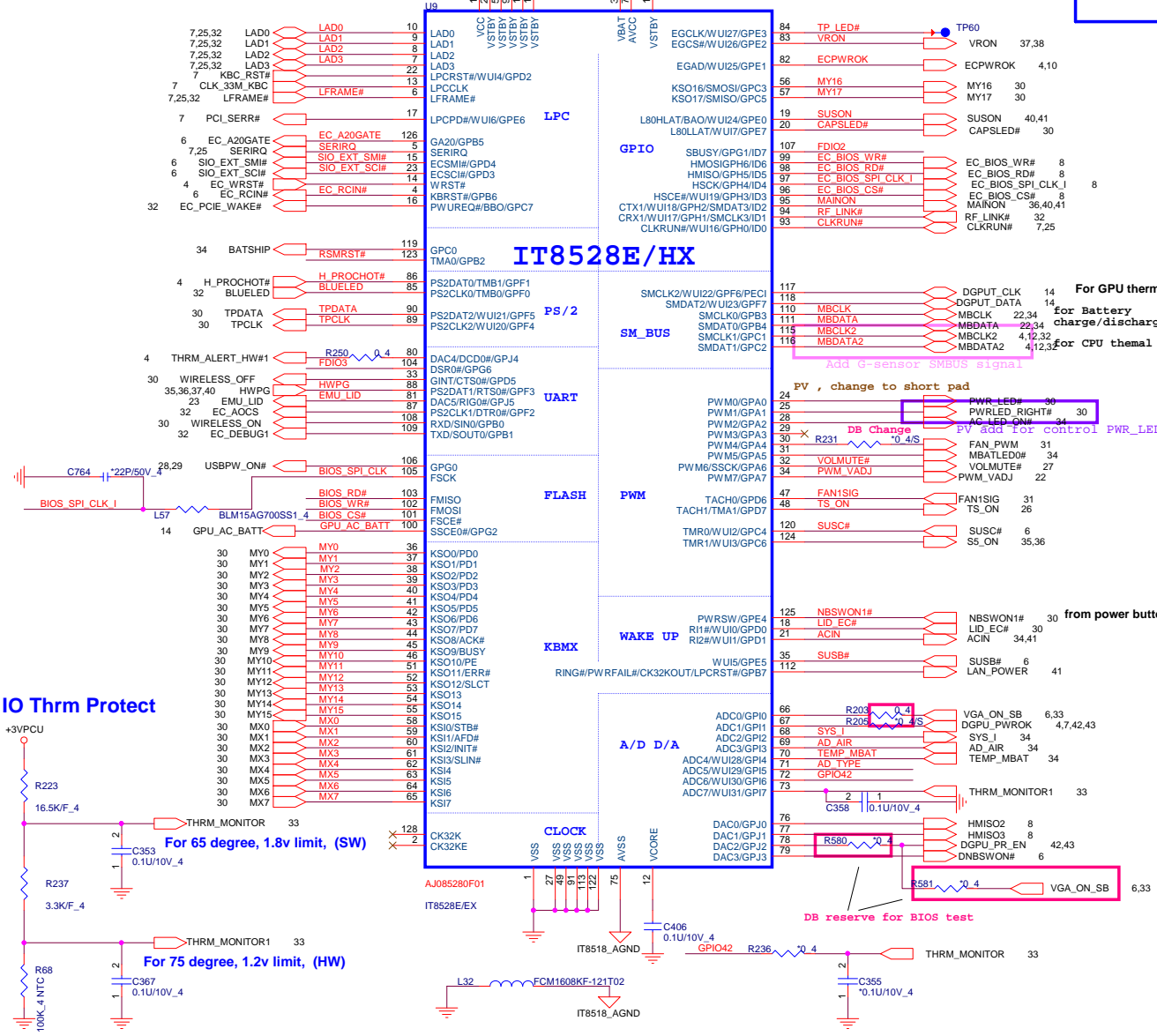


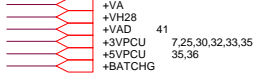
Platform model	GPI042	adapter
SG/DIS	High	90W
UMA	Low	65W

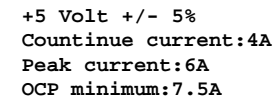


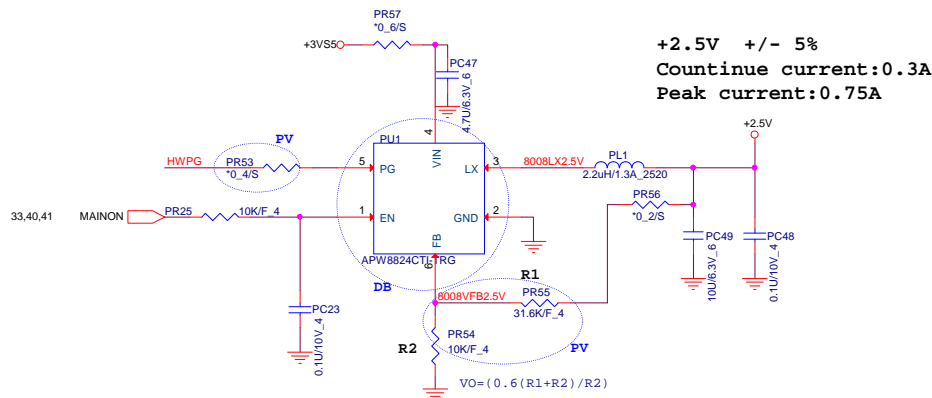
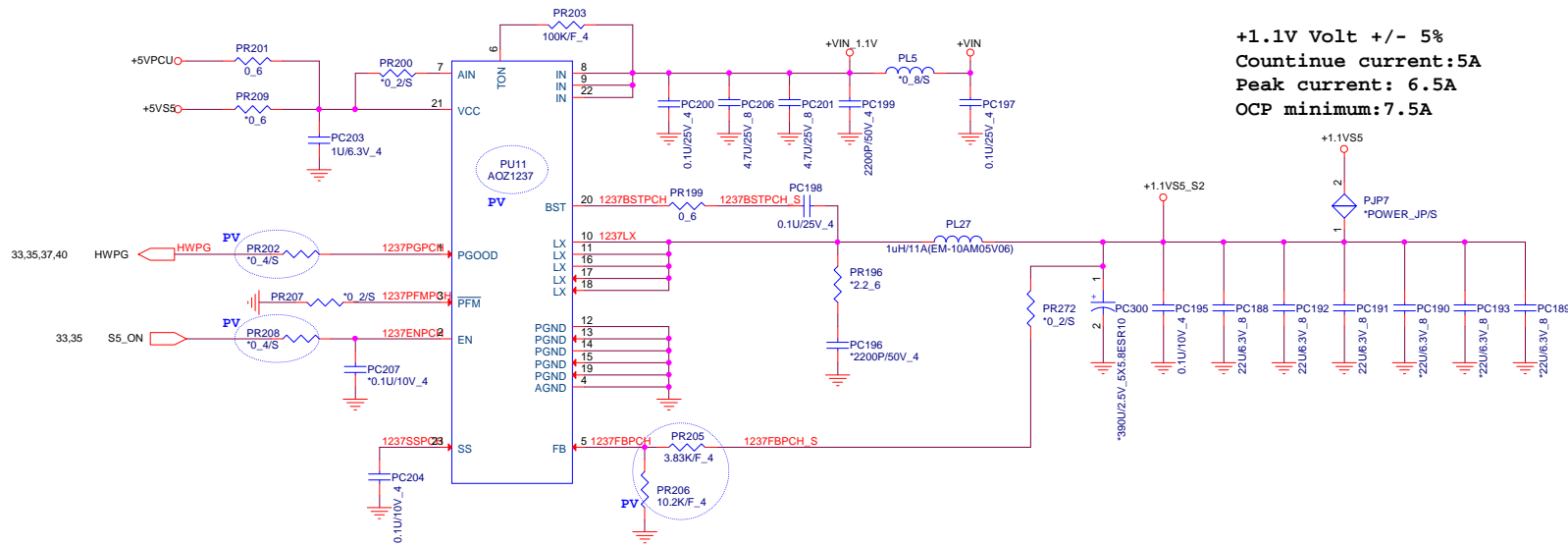
PROJECT : R7X
Quanta Computer Inc.

Size Custom	Document Number EC (IT8518E/HX)/ROM	Revision 1A
Date: Tuesday, March 12, 2013		Sheet 33 of 43

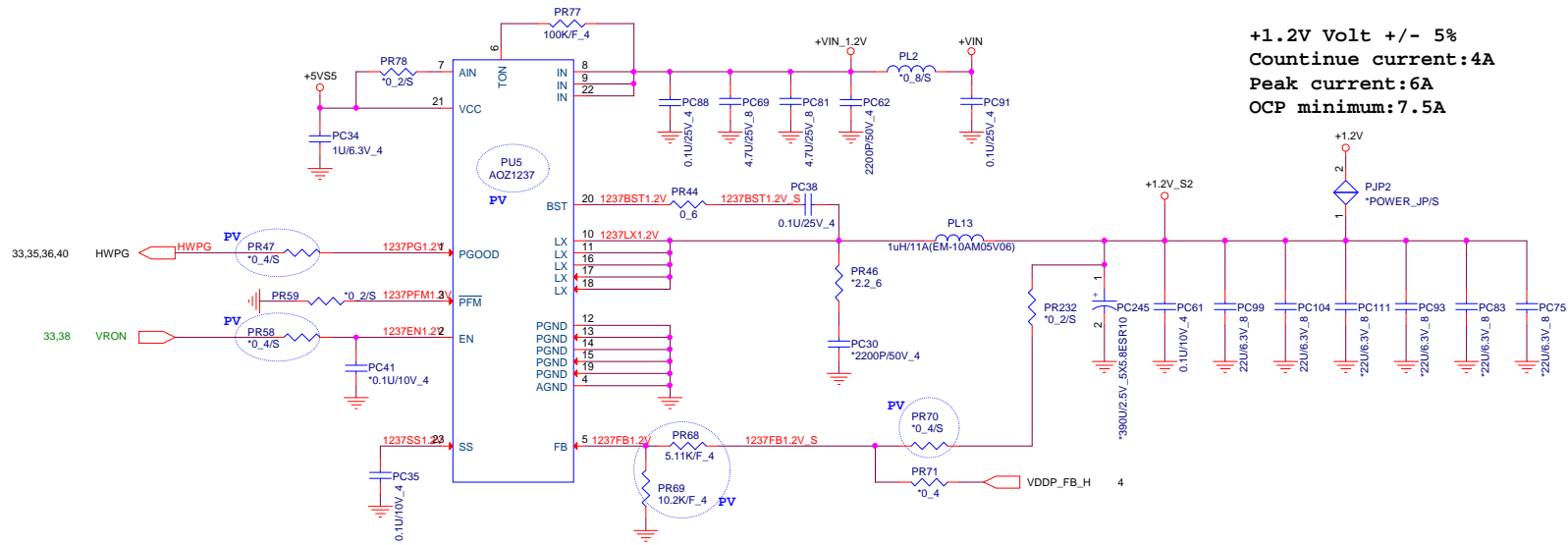


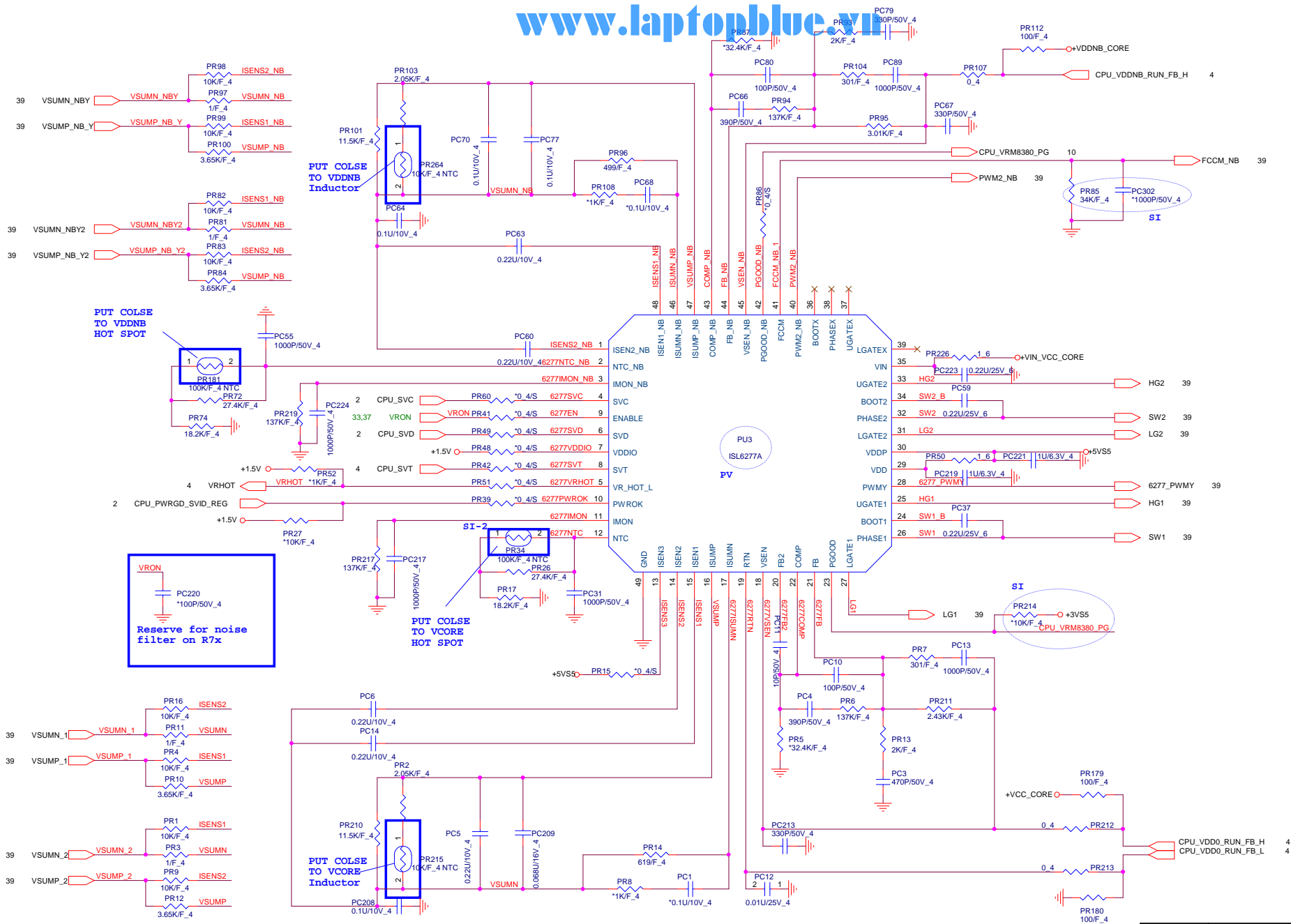


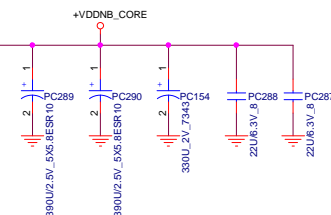
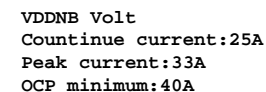
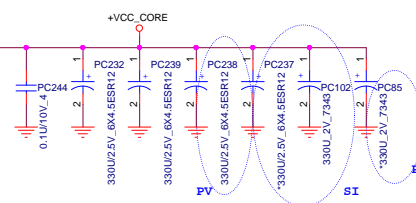
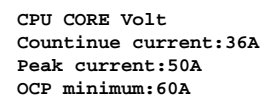


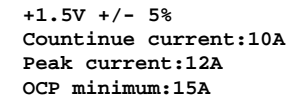


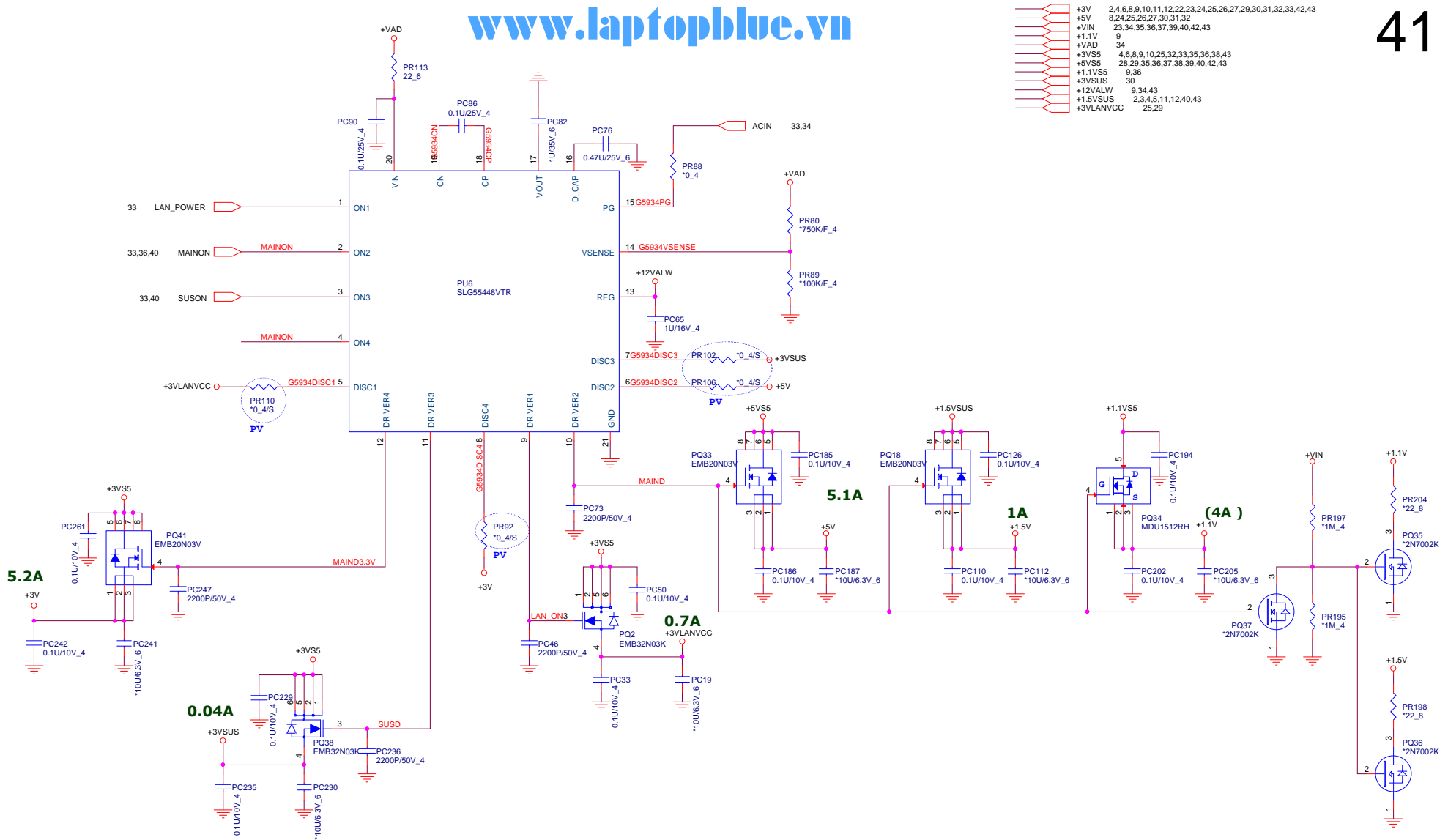
+VIN	23,34,35,37,39,40,41,42,43
+2.5V	5
+3VSS	4,6,8,9,10,25,32,33,35,38,41,43
+5VSS	28,29,35,37,38,39,40,41,42,43
+1.1VSS	9,41
+5VPCU	34,35









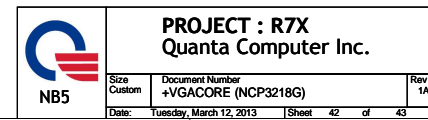


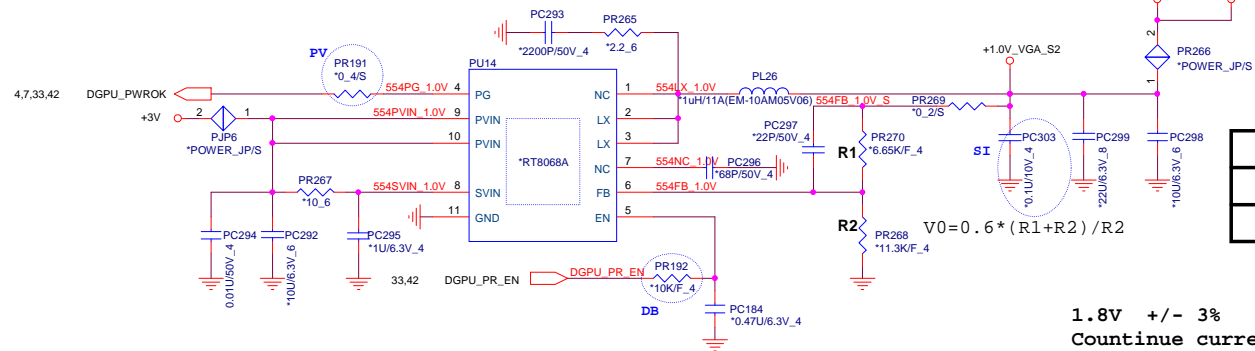
+3V	2,4,6,8,9,10,11,12,22,23,24,25,26,27,29,30,31,32,33,42,43
+5V	8,24,25,26,27,30,31,32
+VIN	23,34,35,36,37,39,40,42,43
+1.1V	9
+VAD	34
+3VS5	4,6,8,9,10,25,32,33,35,36,38,43
+5VS5	28,29,35,36,37,38,39,40,42,43
+1.1VS5	9,36
+3VSUS	30
+12VALW	9,34,43
+1.5VSUS	2,3,4,5,11,12,40,43
+3VLAVCC	25,29

Default

Default

+VGA_CORE
Continue current: 25A
Peak current: 30A
OCp minimum: 33A
L-L: 0mV/A





R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V

