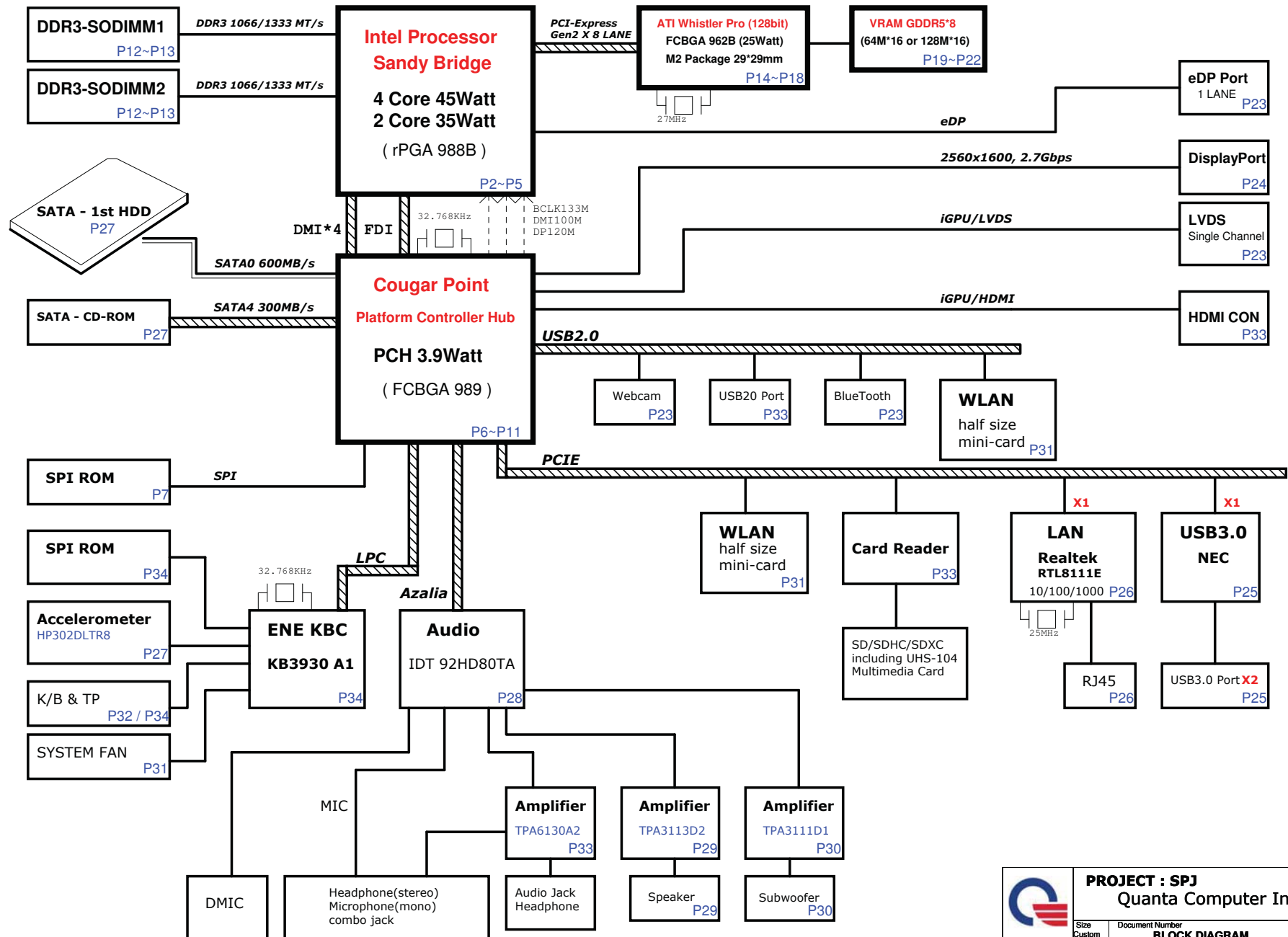
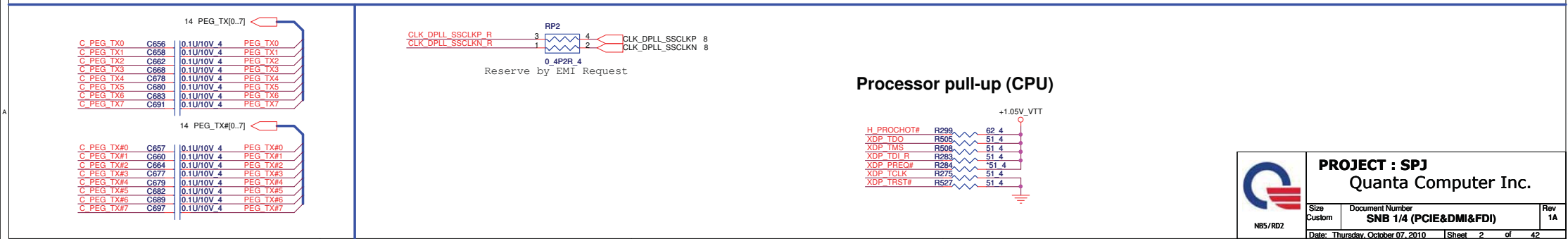
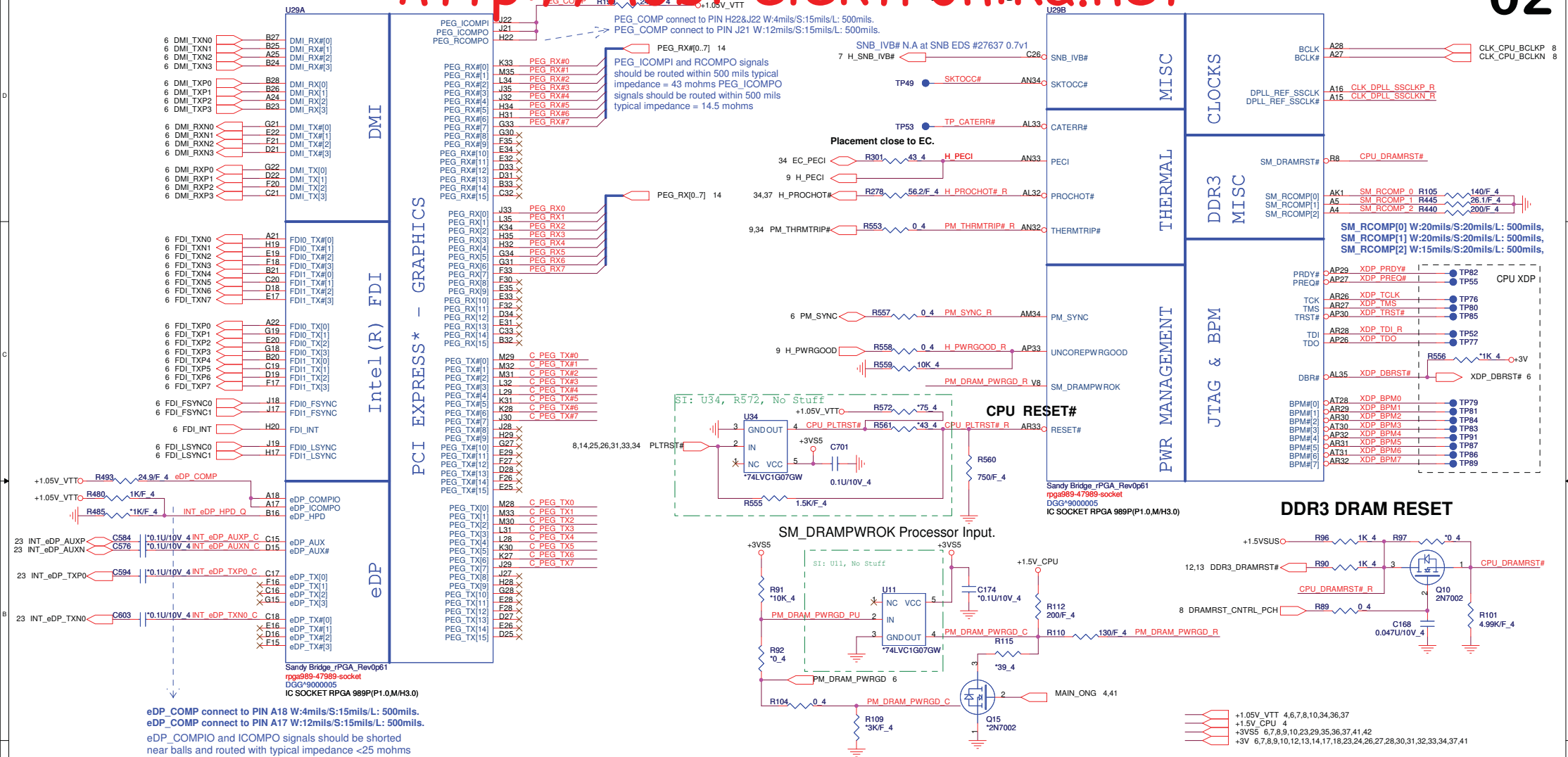


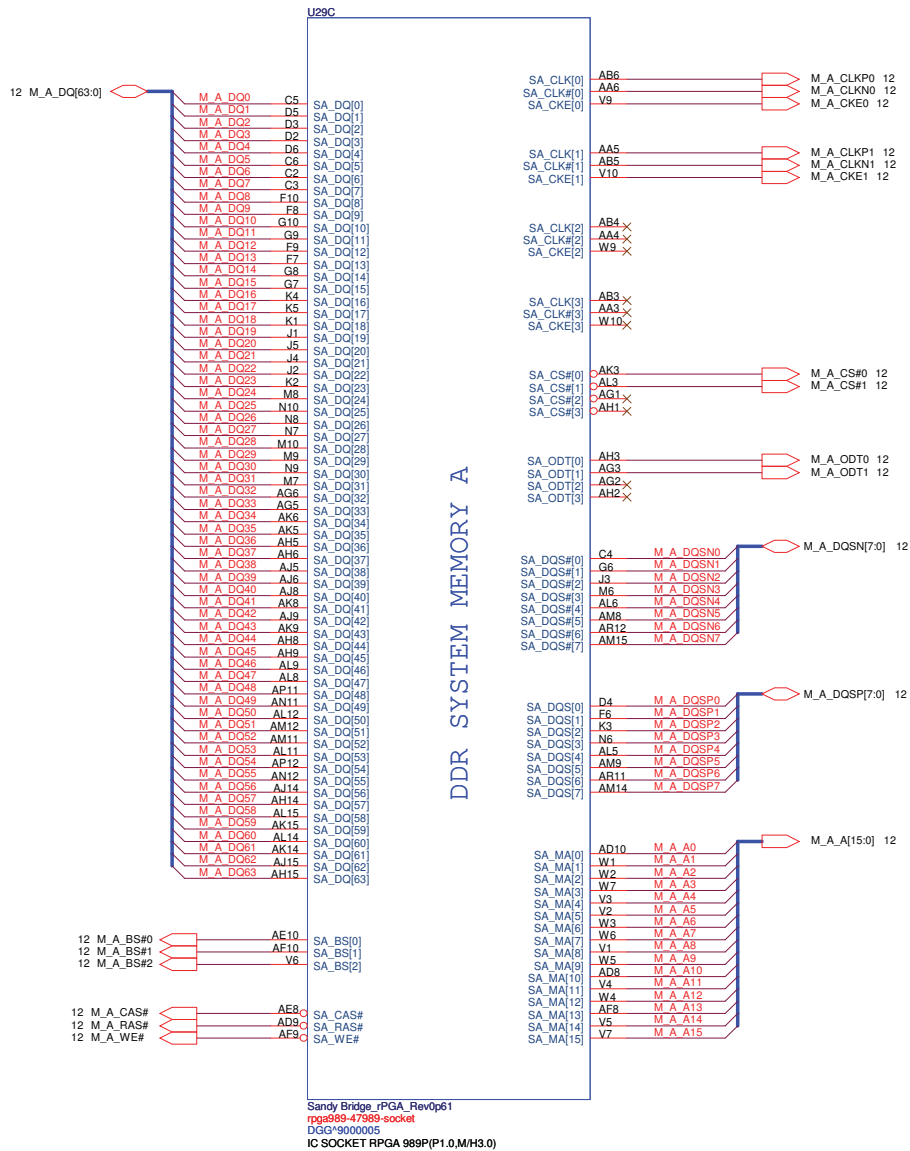
# 14.5 Envy (Huron River+Whistler Pro+GDDR5) BLOCK DIAGRAM

## Dis. PCB 10L STACK UP

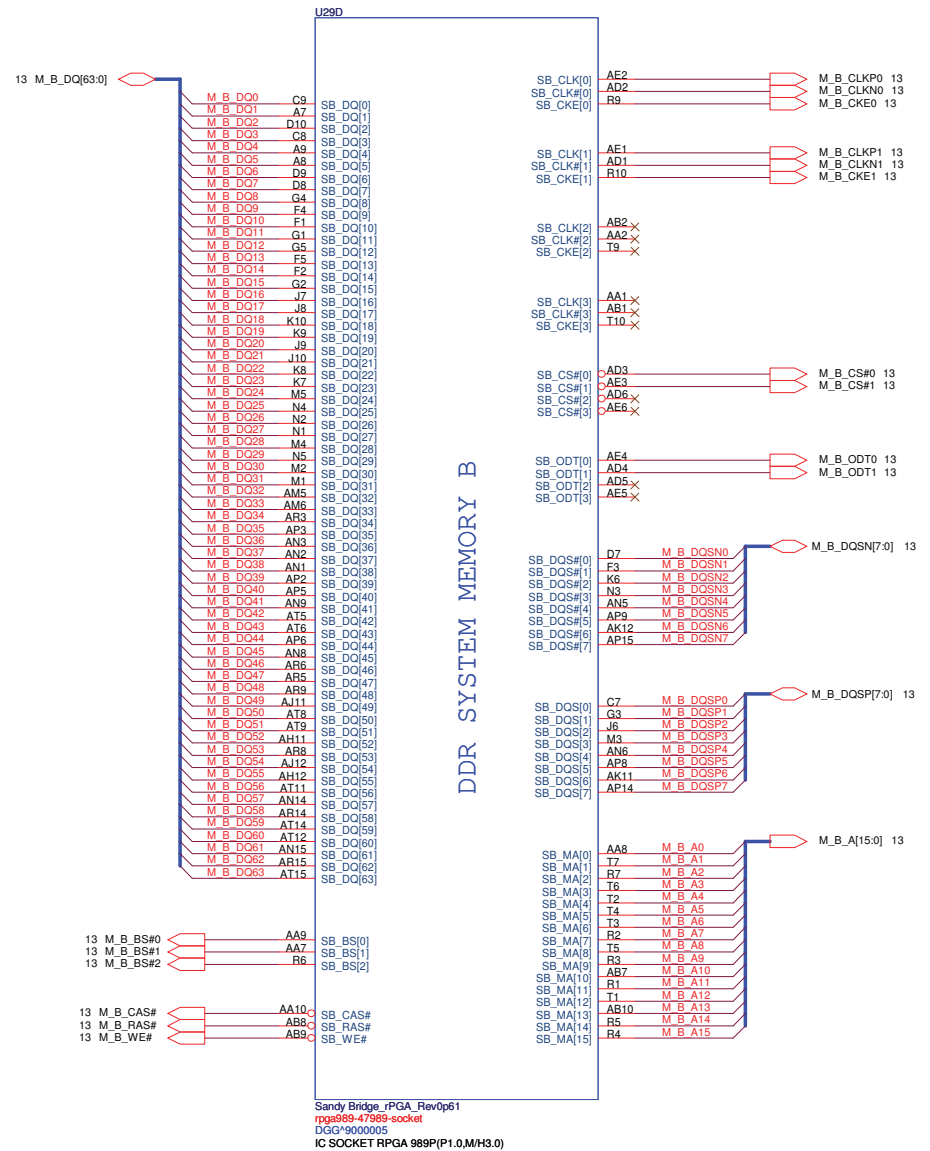
LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2(Low)  
LAYER 5 : SVCC  
LAYER 6 : IN3(High)  
LAYER 7 : SGND  
LAYER 8 : IN4(High)  
LAYER 9 : SGND  
LAYER 10 : BOT



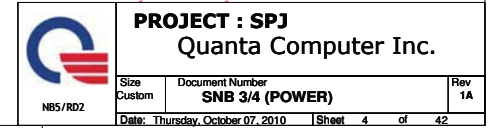


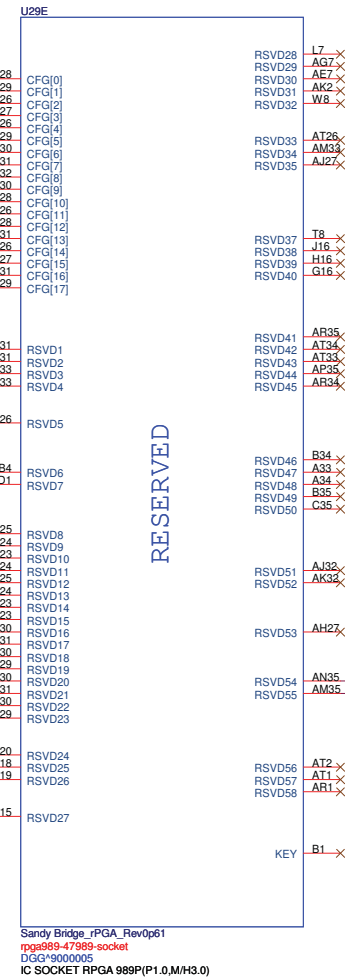
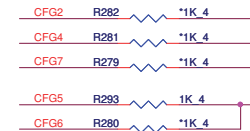
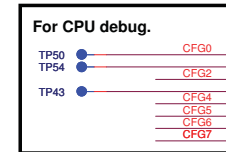
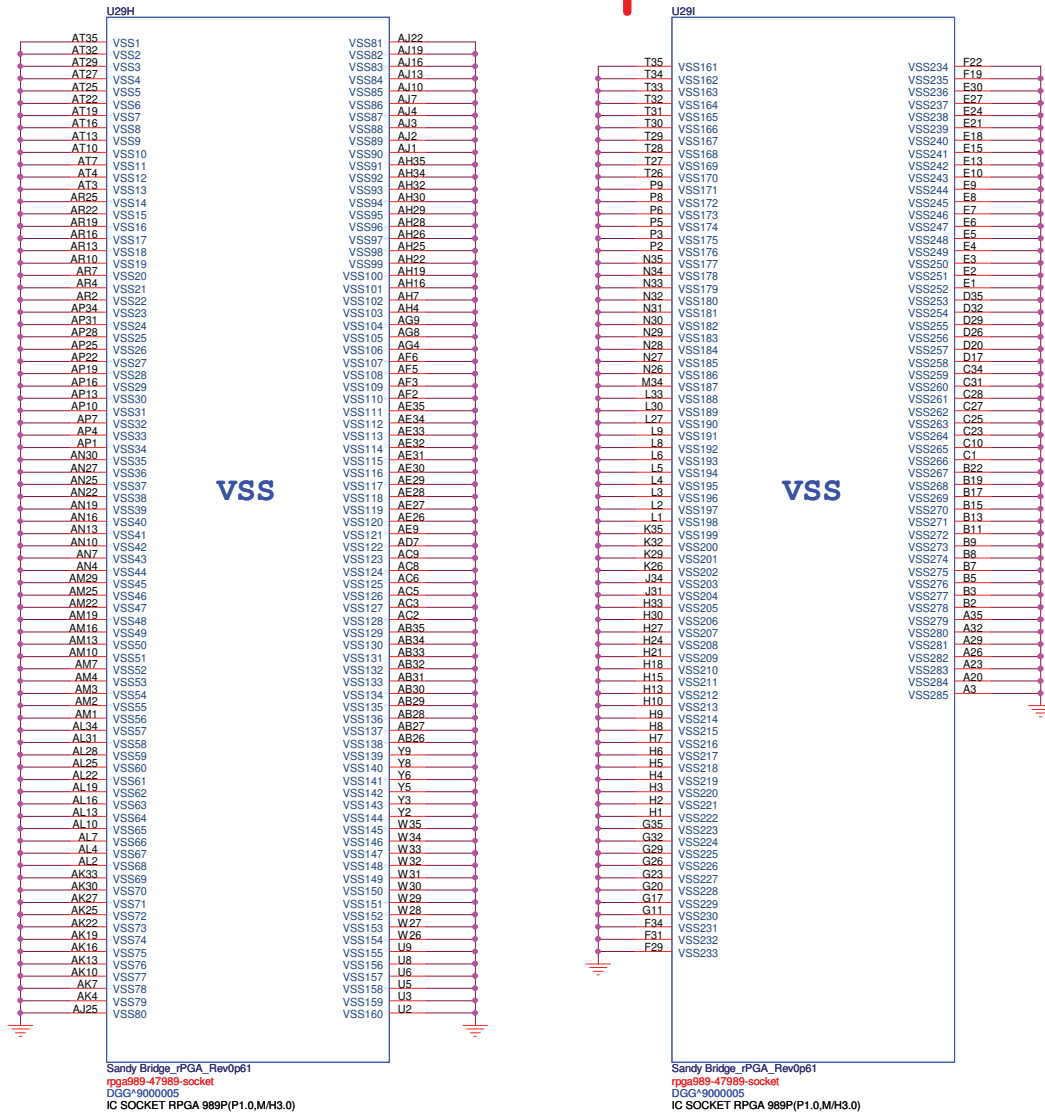


Sandy Bridge\_rPGA\_Rev0p61  
rpg989-47989-socket  
DGG\*9000005  
IC SOCKET RPGA 989P(P1.0,M/H3.0)



Sandy Bridge\_rPGA\_Rev0p61  
rpg989-47989-socket  
DGG\*9000005  
IC SOCKET RPGA 989P(P1.0,M/H3.0)





## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

## CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled  
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled  
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



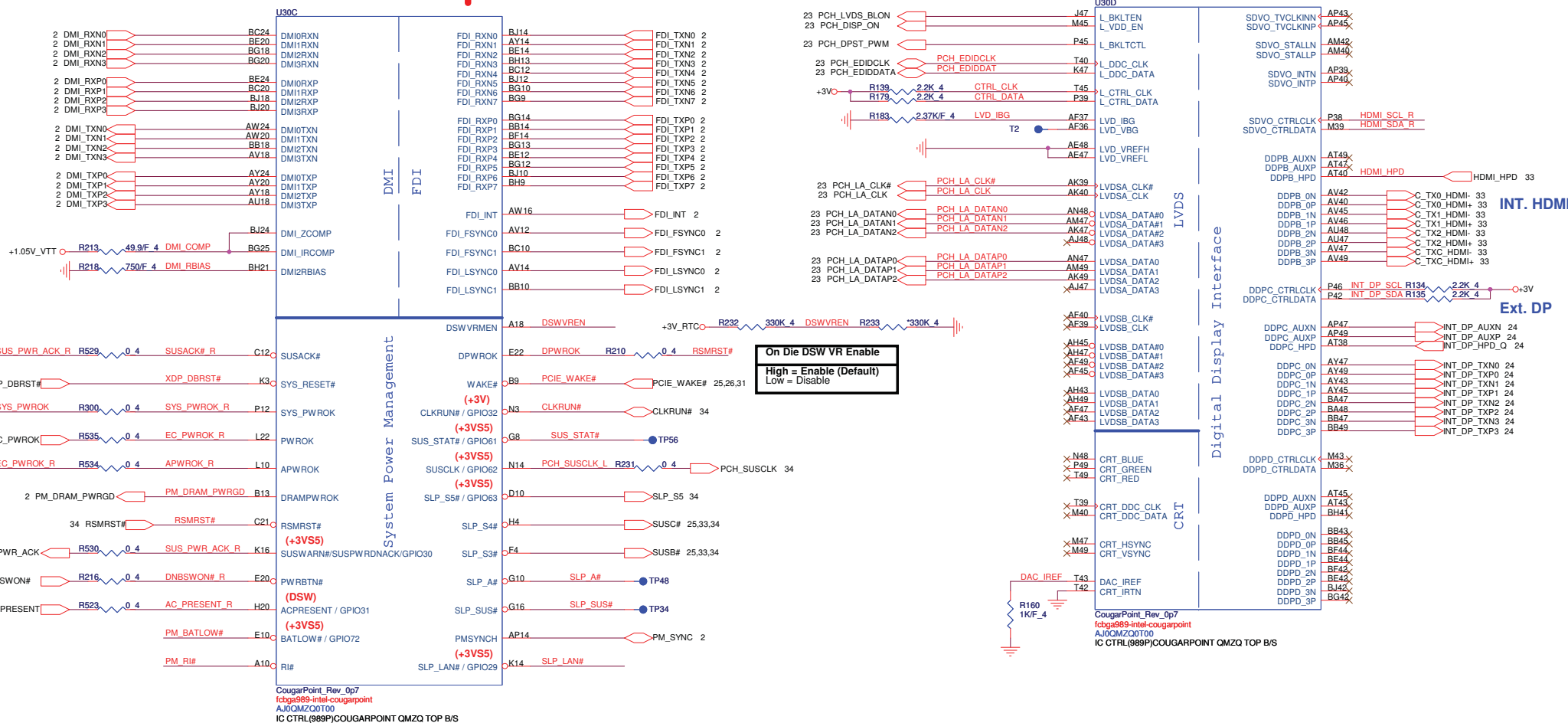
**PROJECT : SPJ**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>SNB 4/4 (GND)</b>	1A
Date: Thursday, October 07, 2010   Sheet 5 of 42		

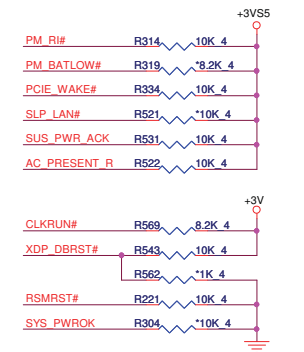


Cougar Point (DMI, FDI, PM)

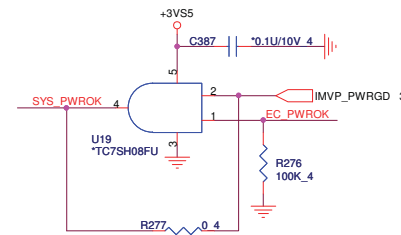
Cougar Point (LVDS, DDI)



PCH Pull-high/low(CLG)



System PWR\_OK(CLG)

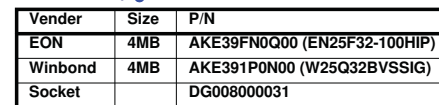



- +1.05V\_VTT 2,4,7,8,10,34,36,37
- +3V\_RTC 7,10
- +3VPCU 7,23,32,33,34,35,40
- +3VS5 2,7,8,9,10,23,29,35,36,37,41,42
- +3V 2,7,8,9,10,12,13,14,17,18,23,24,26,27,28,30,31,32,33,34,37,41
- +5V 7,10,16,23,24,27,28,31,32,33,41

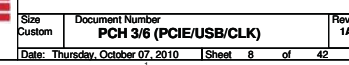


**PROJECT : SPJ**  
**Quanta Computer Inc.**

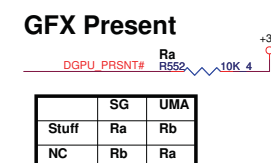
Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A
Date: Thursday, October 07, 2010	Sheet 6 of 42	



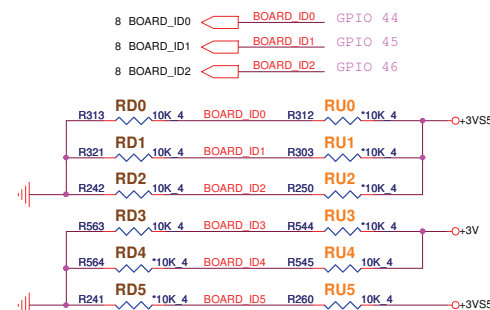
 NBS/RD2	<b>PROJECT : SPJ</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>PCH 2/6 (SATA/HDA/SPI)</b>	Rev 1A
Date: Friday, October 08, 2010		Sheet 7 of 42	



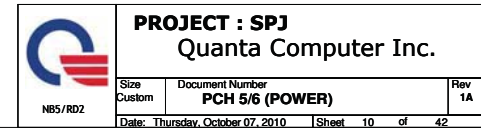
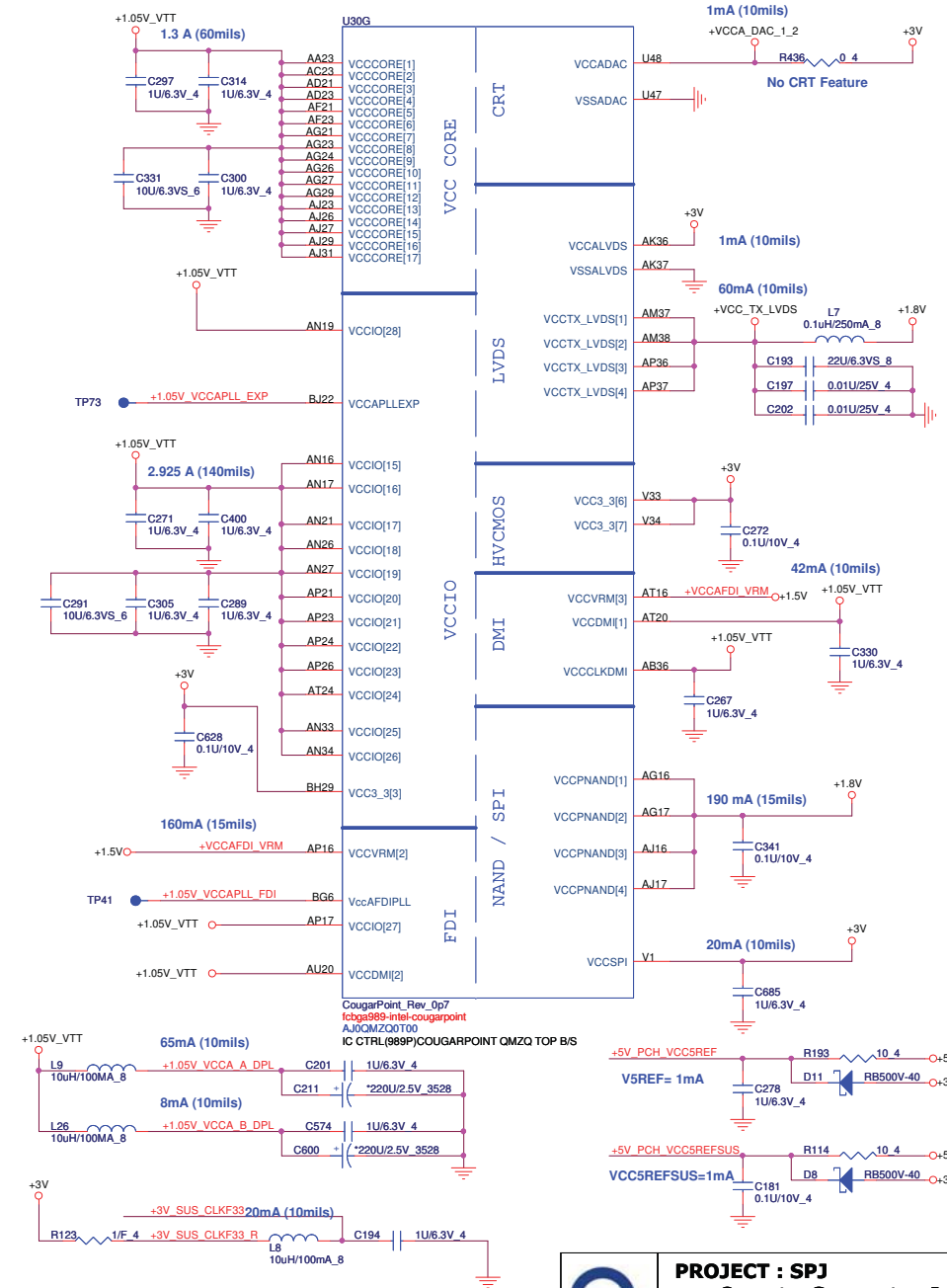


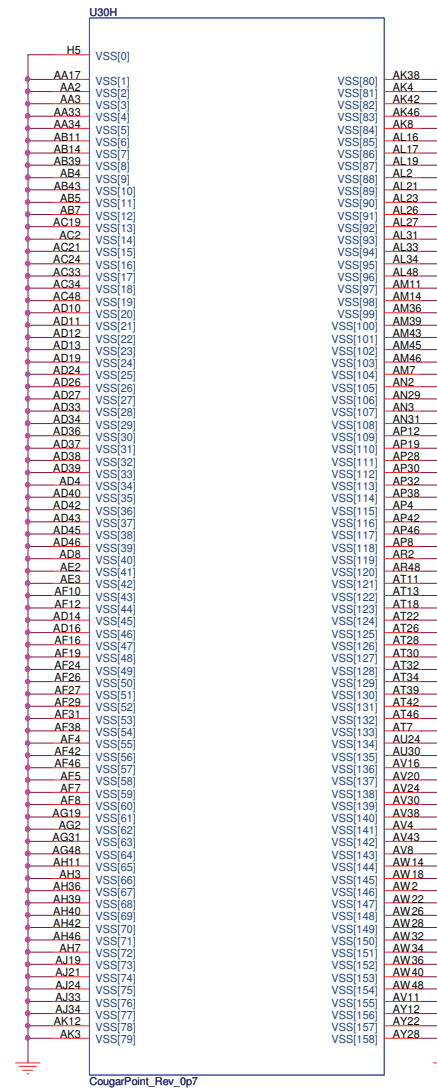
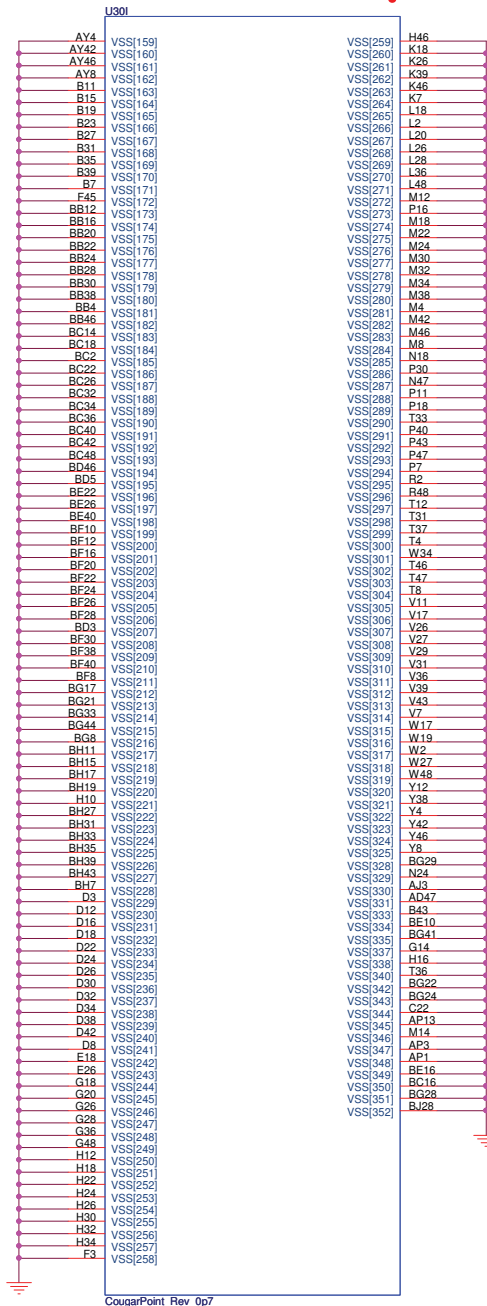


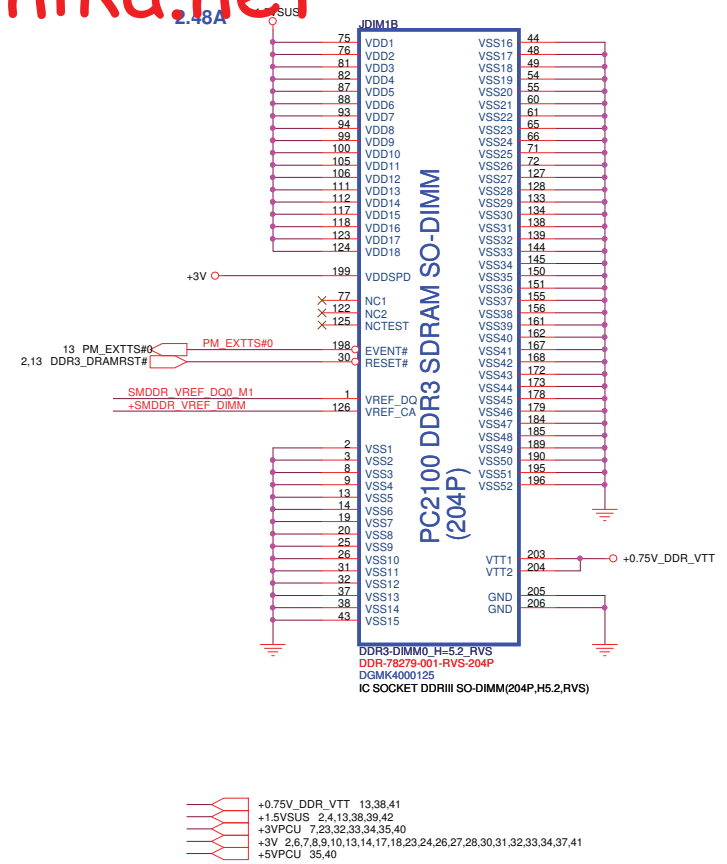
BOARD ID SETTING	0	1
BOARD_ID0 GPIO 44	14"	15"
BOARD_ID1 GPIO 45	CPU 35W	CPU 45W
BOARD_ID2 GPIO 46	LVDS	eDP
BOARD_ID3 GPIO 34	RESERVE	RESERVE
BOARD_ID4 GPIO 35	RESERVE	RESERVE
BOARD_ID5 GPIO 24	RESERVE	RESERVE



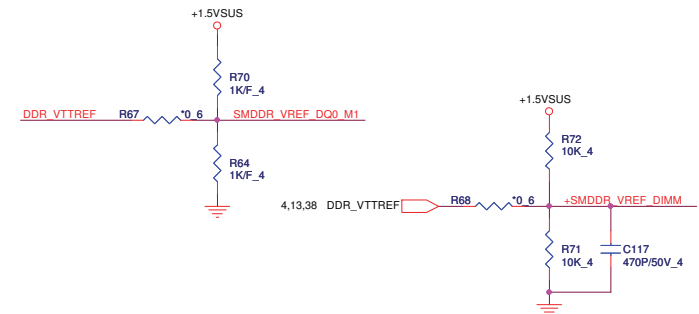
COUGAR POINT (POWER)



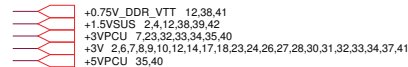




### VREF DQ0 M1 Solution

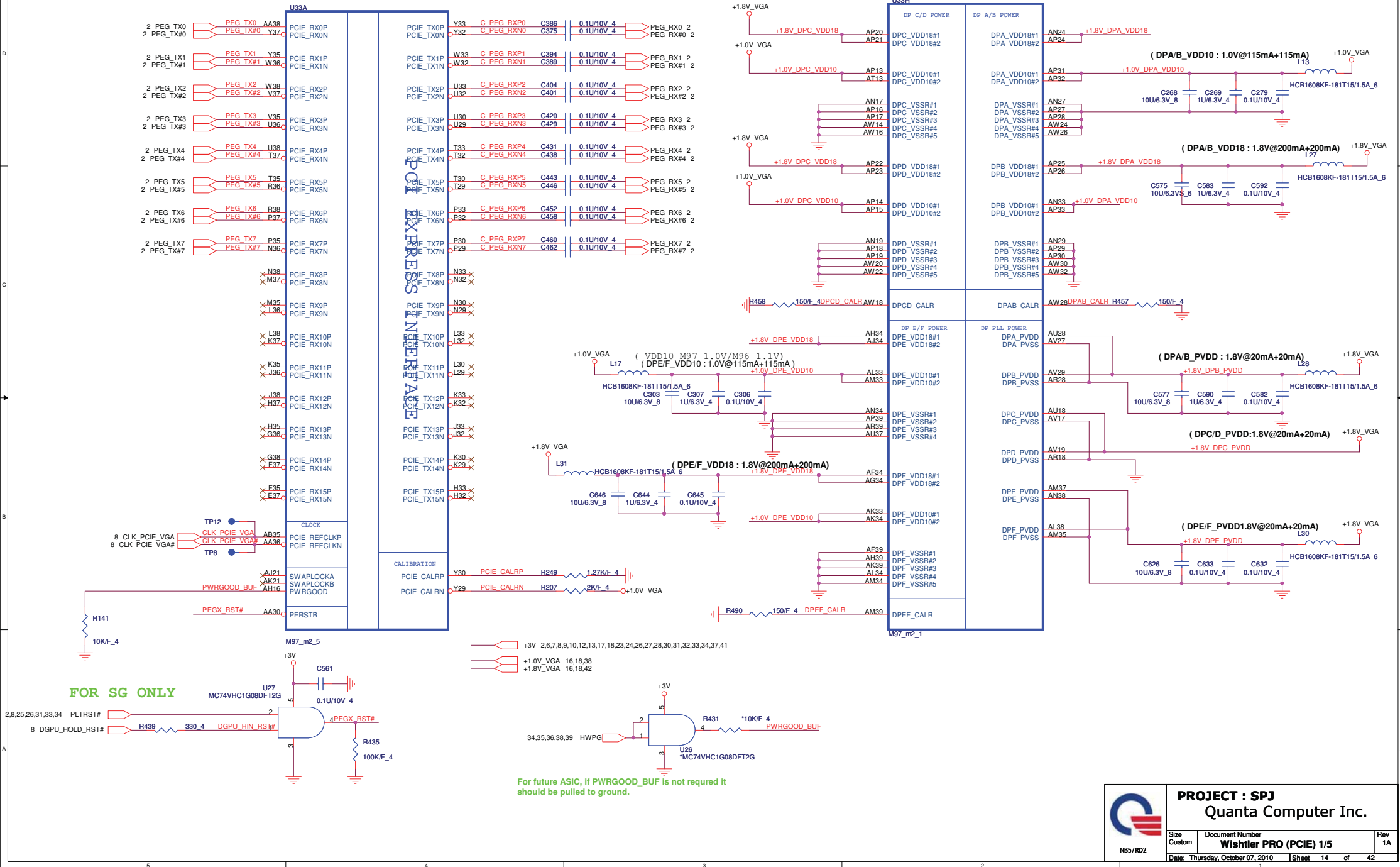


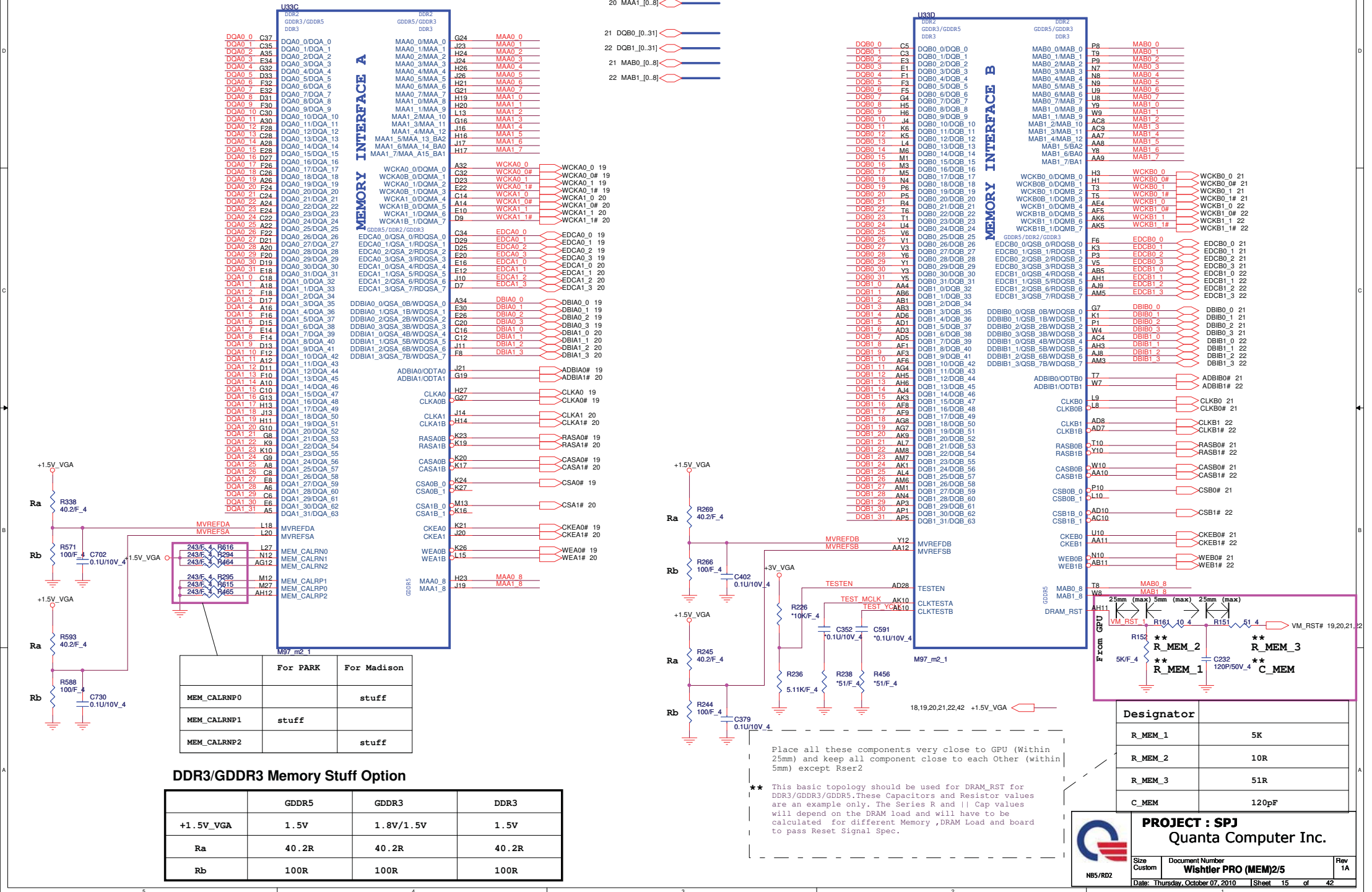
Size Custom	Document Number <b>DDR3 DIMM0-RVS (5.2H)</b>	Rev 1A
Date: Thursday, October 07, 2010		Sheet 12 of 42

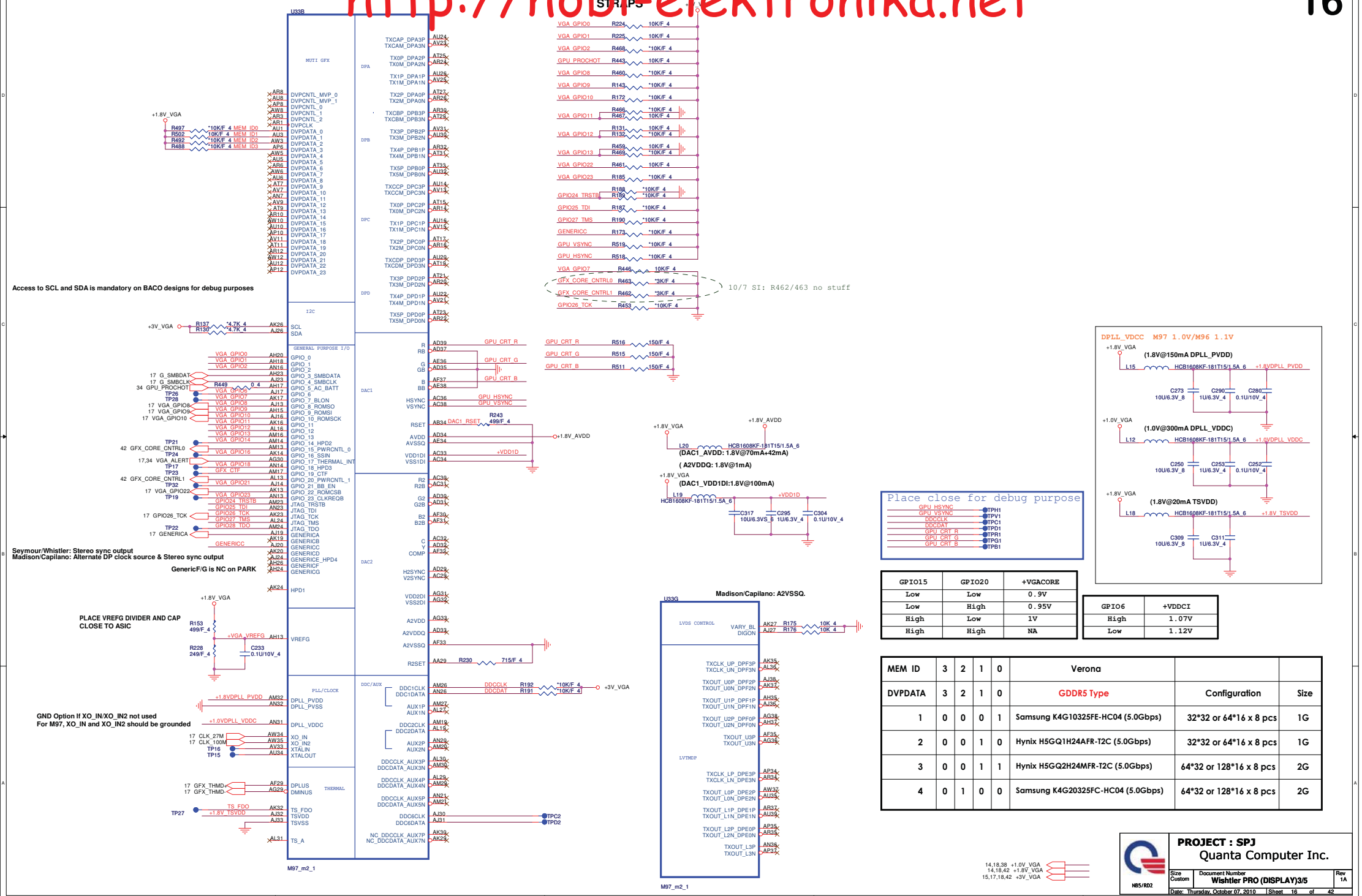


Size Custom	Document Number <b>DDR3 DIMM1-RVS (9.2H)</b>	Rev 1A
Date: Thursday, October 07, 2010		Sheet 13 of 42










GPIO15	GPIO20	+VGAORE
Low	Low	0.9V
Low	High	0.95V
High	Low	1V
High	High	NA

GPIO6	+VDDCI
High	1.07V
Low	1.12V

MEM ID	3	2	1	0	Verona	Configuration	Size
DVPDATA	3	2	1	0	GDDR5 Type		
1	0	0	0	1	Samsung K4G10325FE-HC04 (5.0Gbps)	32*32 or 64*16 x 8 pcs	1G
2	0	0	1	0	Hynix H5GQ2H24AFR-T2C (5.0Gbps)	32*32 or 64*16 x 8 pcs	1G
3	0	0	1	1	Hynix H5GQ2H24MFR-T2C (5.0Gbps)	64*32 or 128*16 x 8 pcs	2G
4	0	1	0	0	Samsung K4G20325FC-HC04 (5.0Gbps)	64*32 or 128*16 x 8 pcs	2G

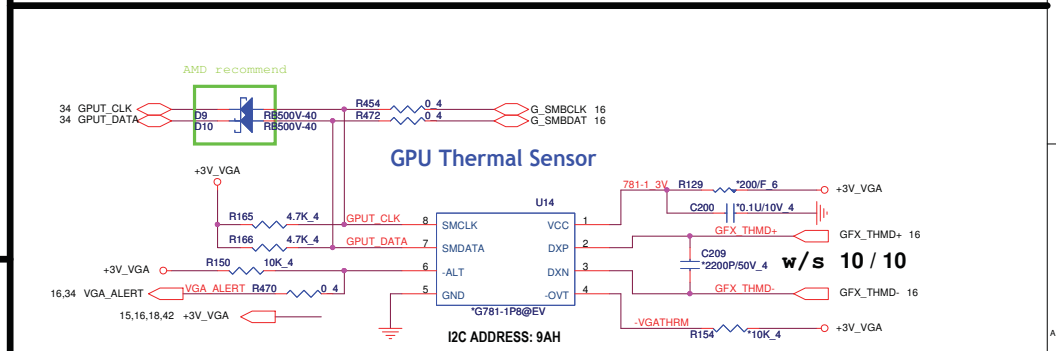
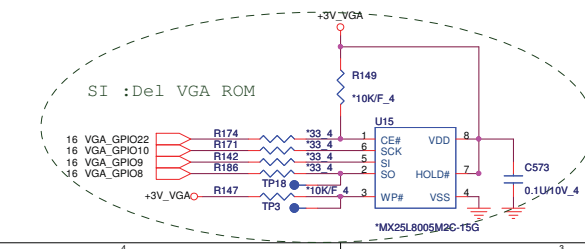



**PROJECT : SPJ**  
**Quanta Computer Inc.**

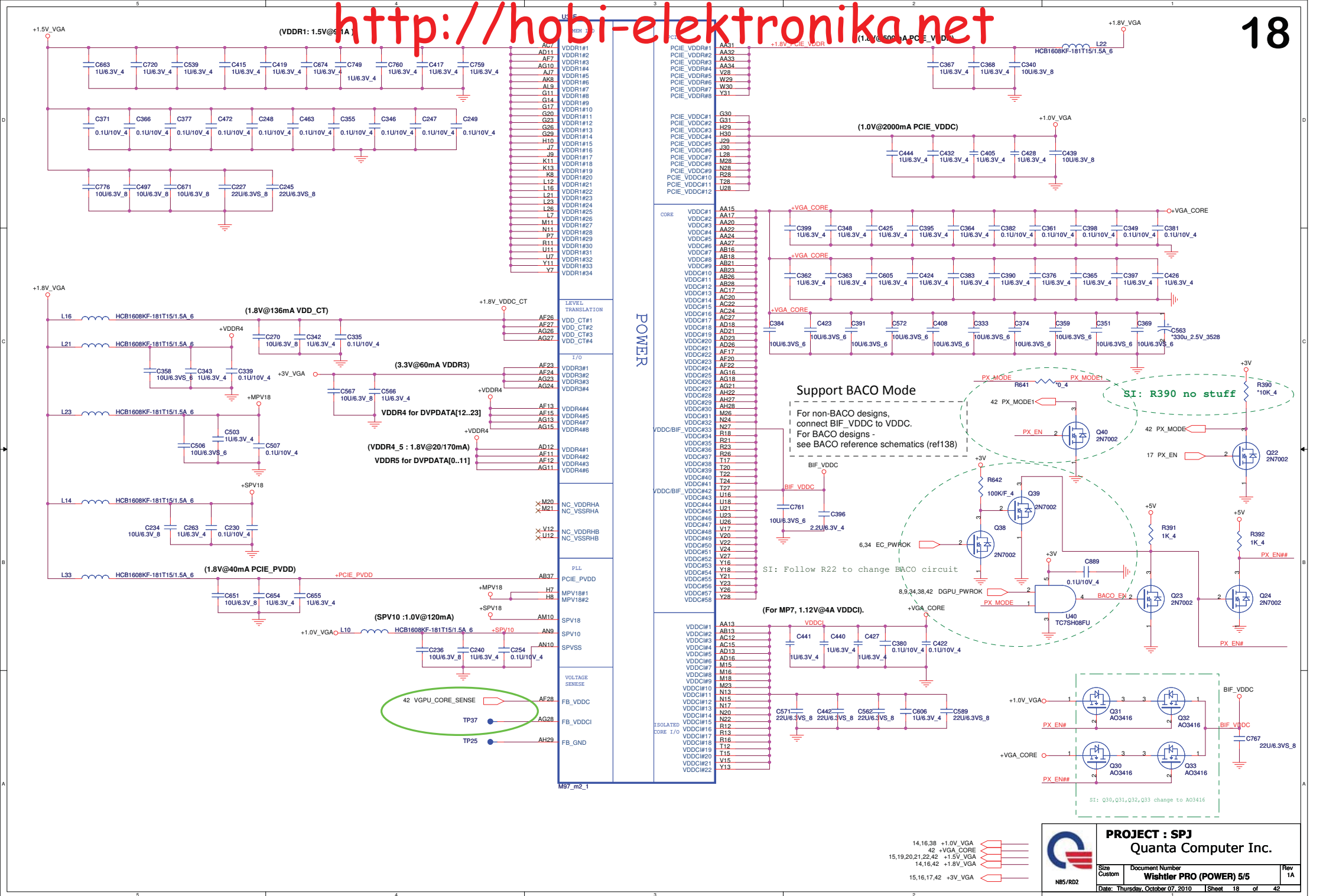
Size	Custom	Document Number	Wishnet PRO (DISPLAY)3/5	Rev	1A
Date: Thursday, October 07, 2010   Sheet 16 of 42					

14,18,38 +1.0V\_VGA  
14,18,42 +1.8V\_VGA  
15,17,18,42 +3V\_VGA

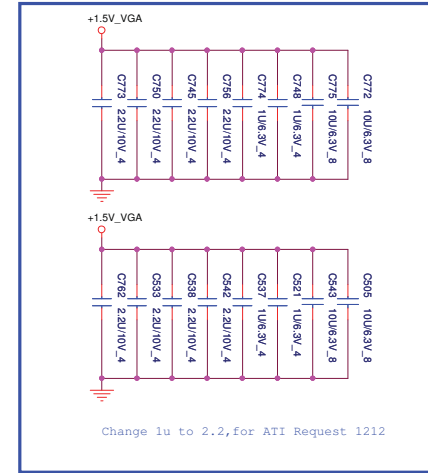
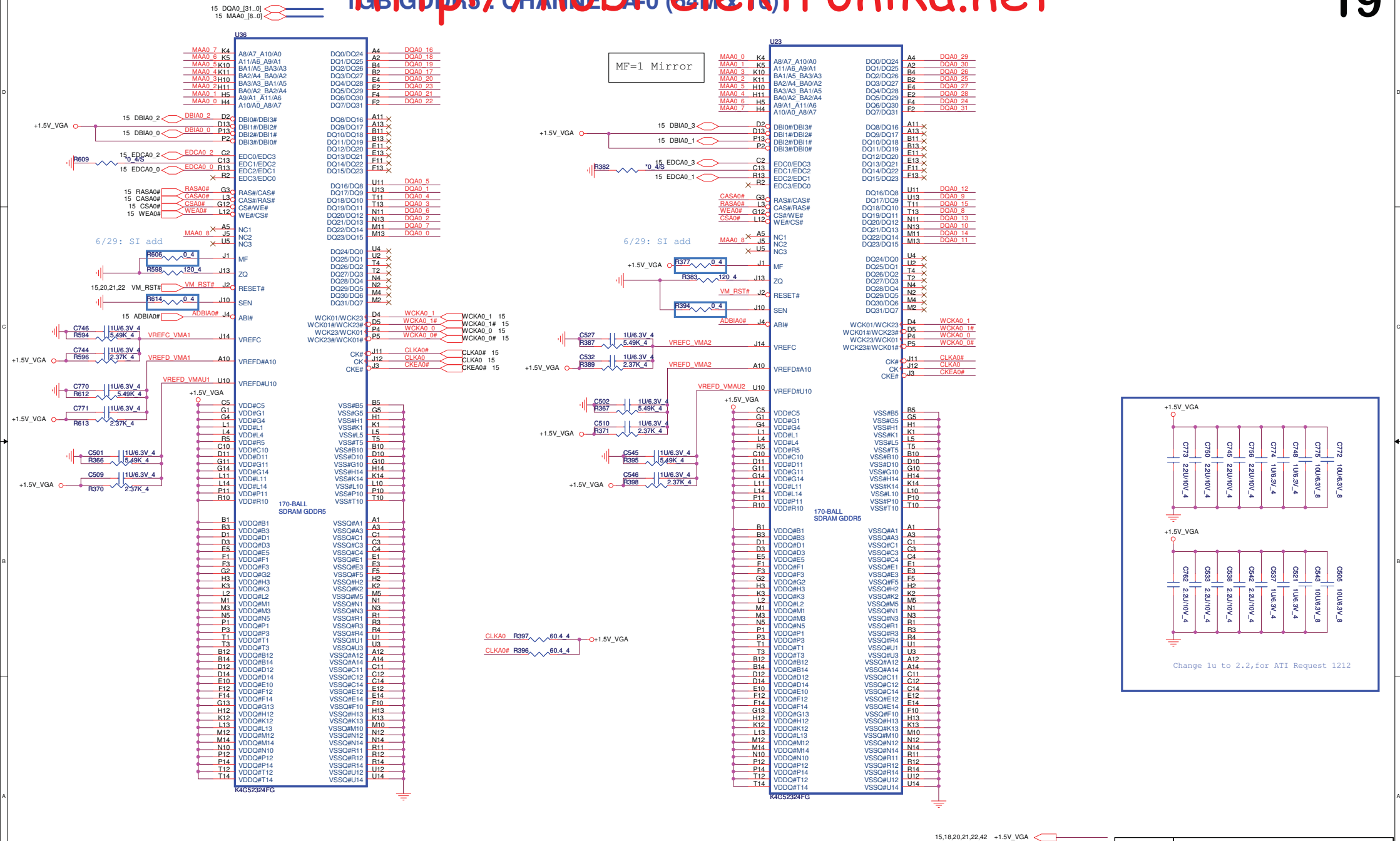
SSEL1(Pin3)	SSEL0 (Pin7)	Spread Percent (Fin5)
Low	Low	No Spread/Off
Low	Floating	-0.5%
Low	High	-2.5%
Floating	Low	-0.25%
Floating	Floating	-0.75%
Floating	High	-1.00%
High	Low	-1.5%
High	Floating	-2.0%
High	High	-3.0%

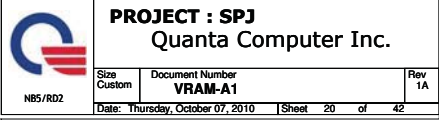


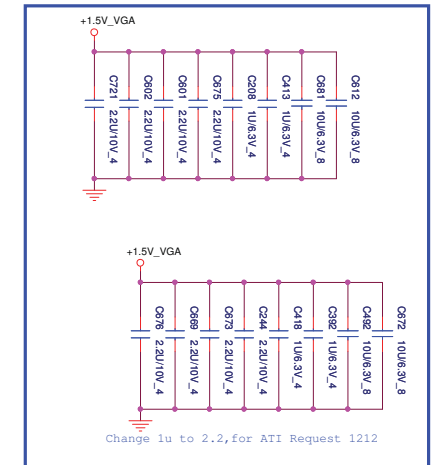
 NBS/RDZ	<b>PROJECT : SPJ</b> <b>Quanta Computer Inc.</b>		
	Size Custom <b>Wishtler PRO (GD&amp;Str)4/5</b>	Document Number <b>Wishtler PRO (GD&amp;Str)4/5</b>	Rev 1A
Date: Thursday, October 07, 2010		Sheet 17 of 42	

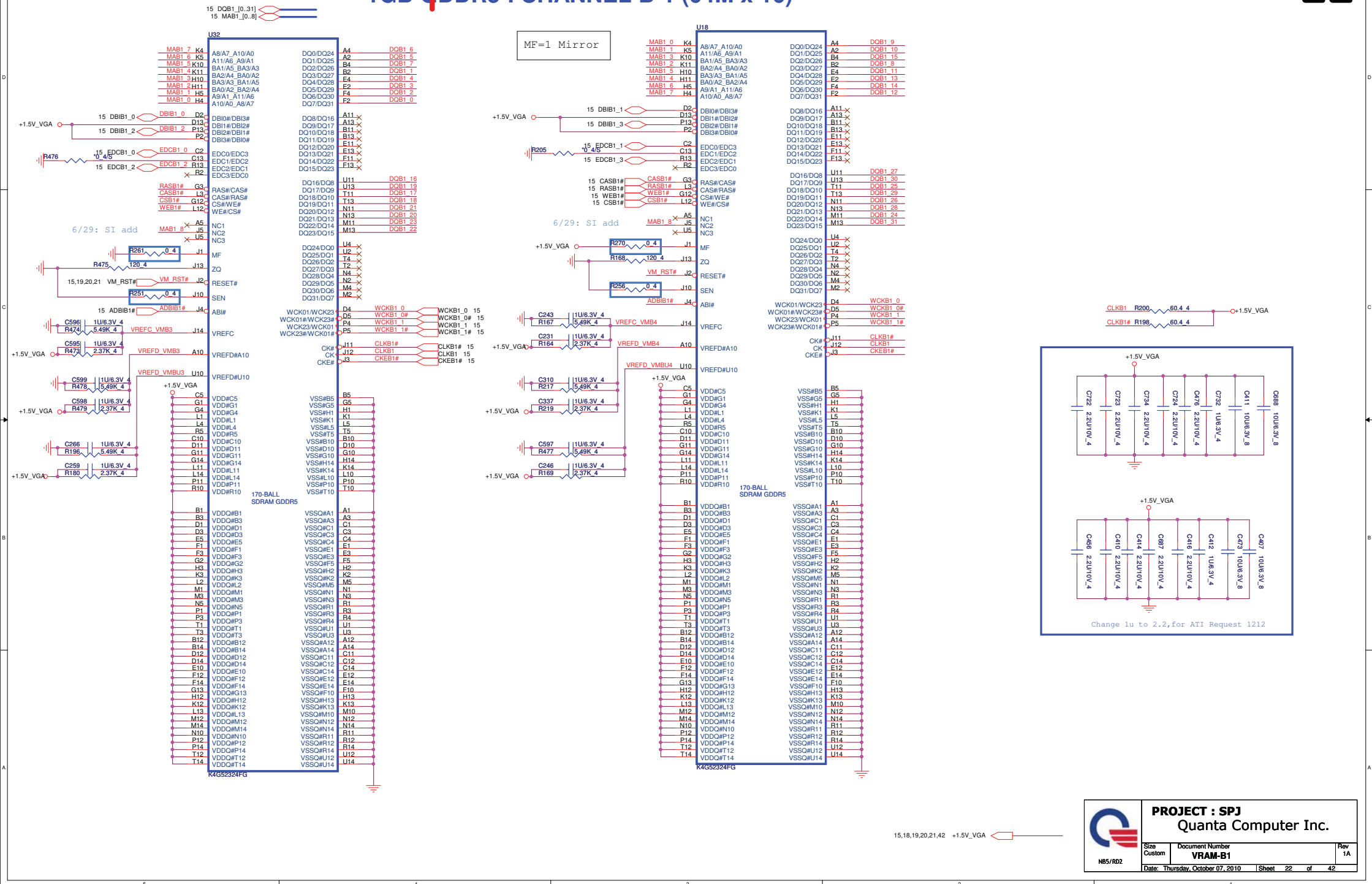




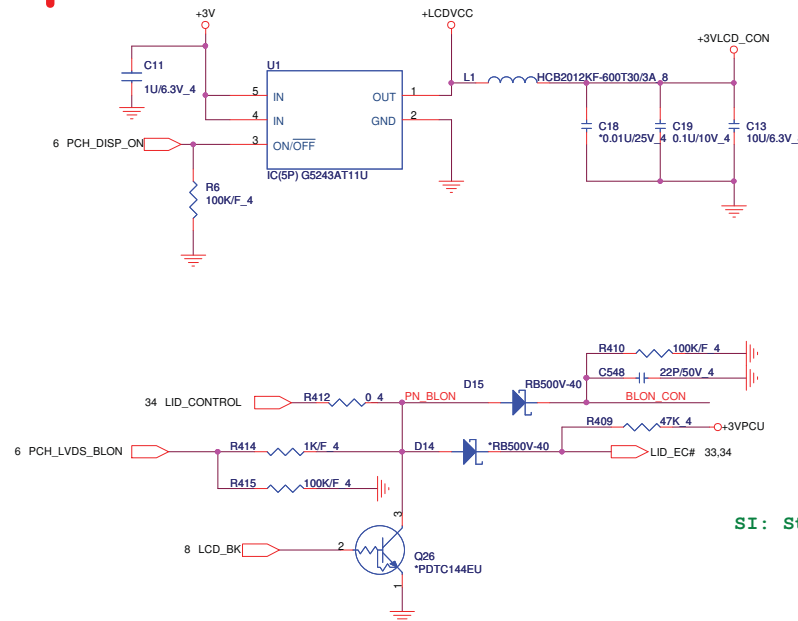
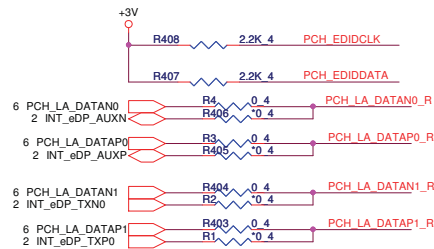






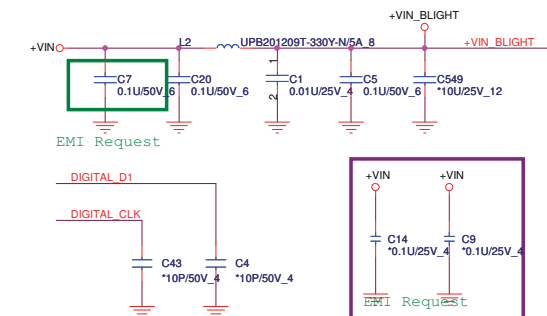
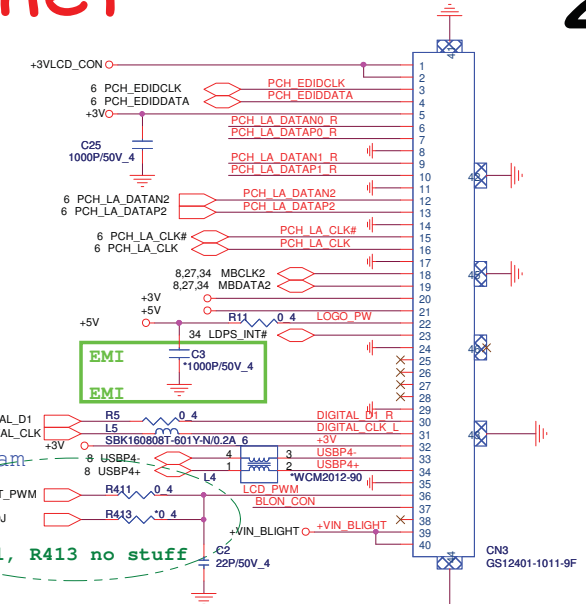


## eDP/LVDS Option

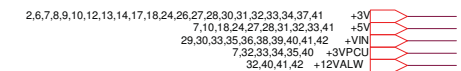
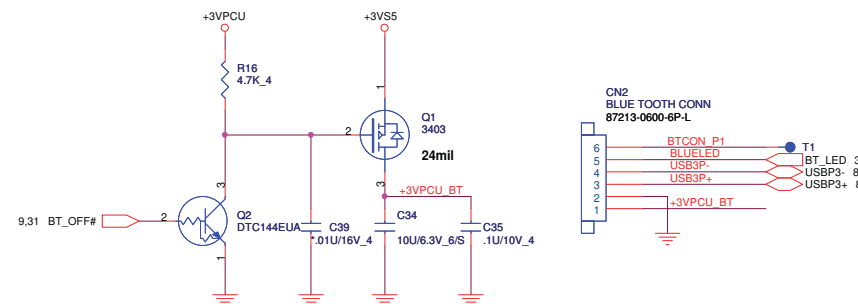


webcam

SI: Stuff R411, R413 no stuff

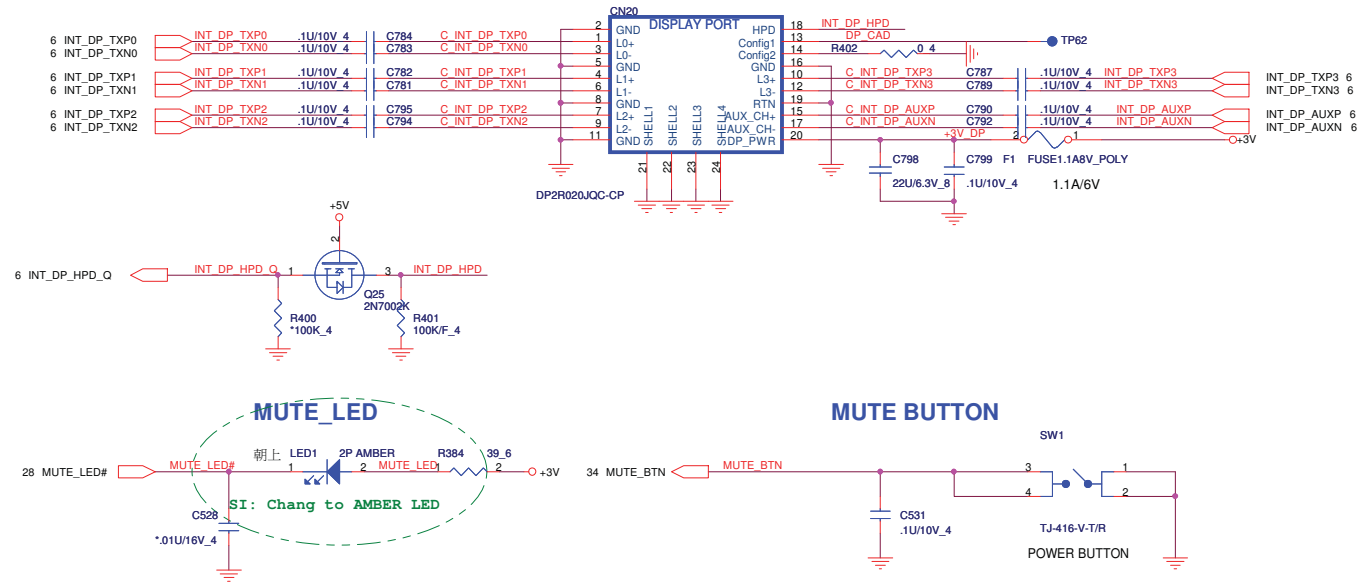


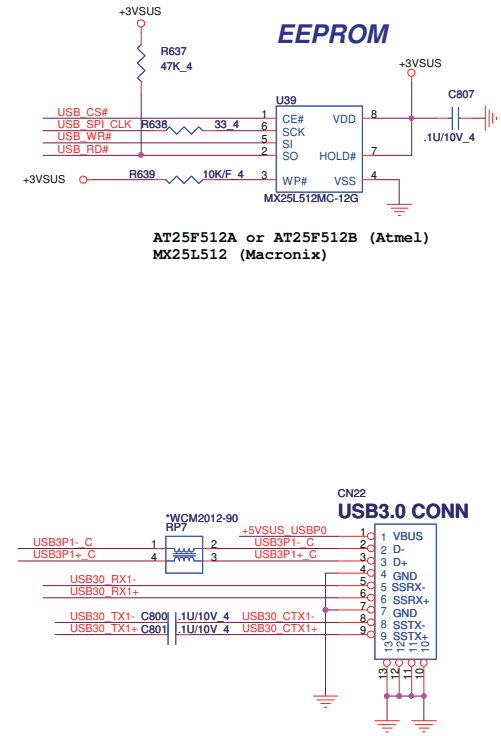
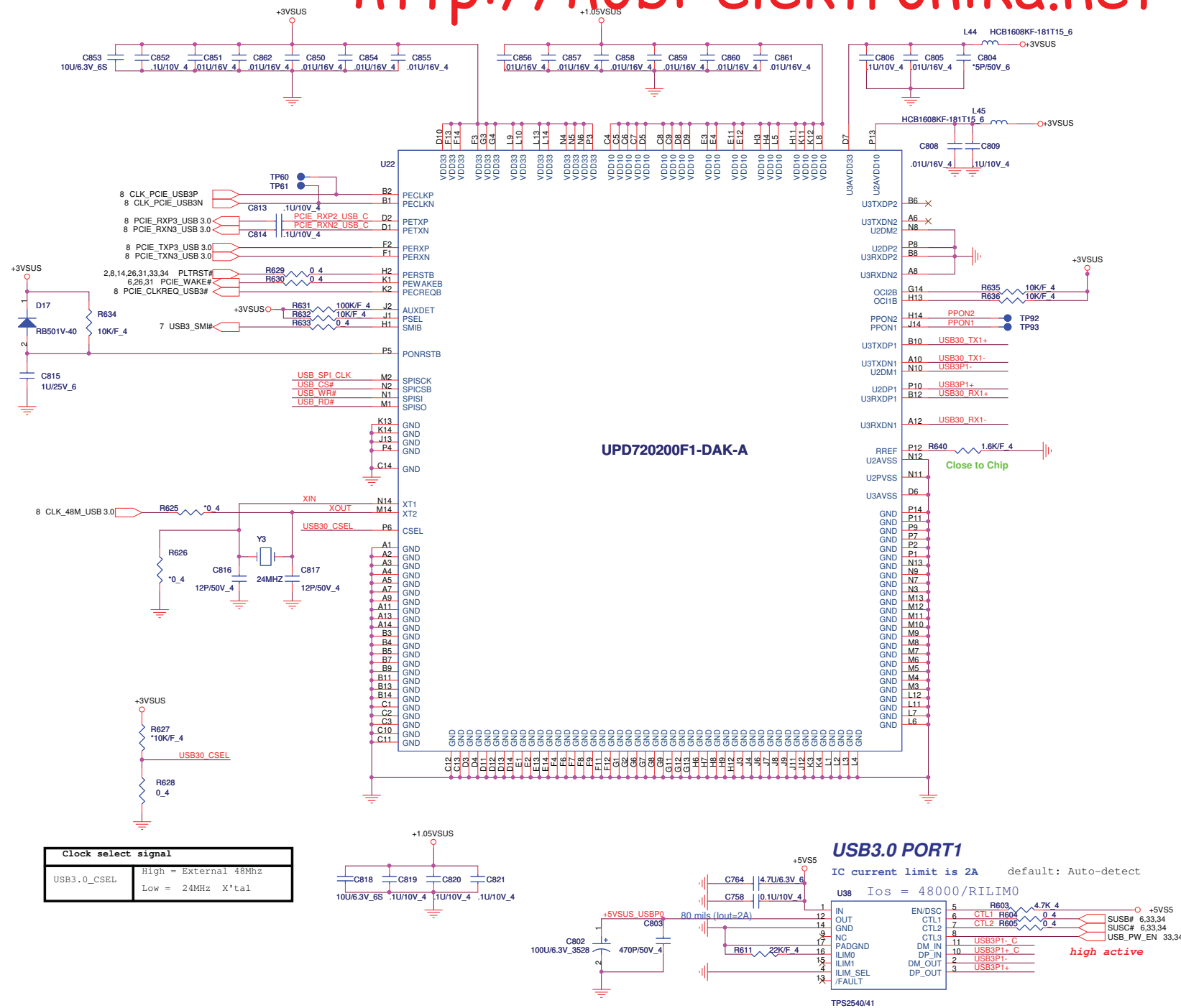
## Softbreeze Bluetooth





## Standard Display Port Connector

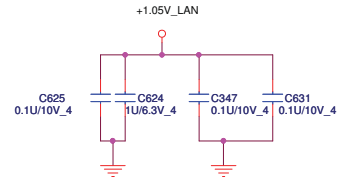
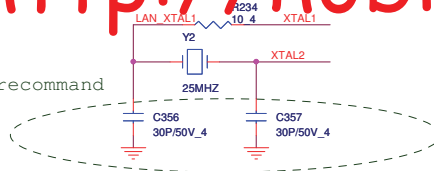




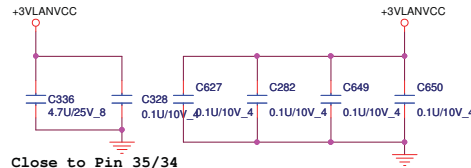
Clock select signal	
USB3.0_CSEL	High = External 48Mhz
	Low = 24MHz X'tal

<b>PROJECT : SPJ</b> Quanta Computer Inc.
--

SI: change to 30P. TXC reccomand



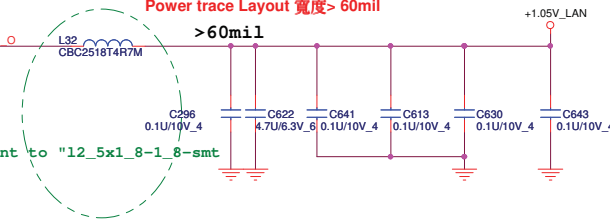
Close to Pin 21



Close to Pin 35/34

IND SMD 4.7UH +-20% 680MA (CBC2518T4R7M)  
CV-4707MZ00

Power trace Layout 寬度 >60mil

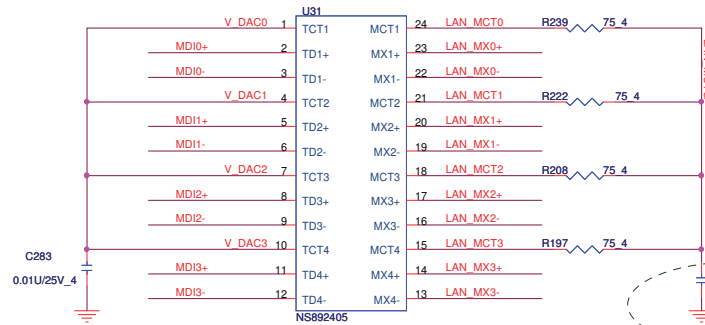


>60mil

Trace <30 mil  
Width > 60 mil

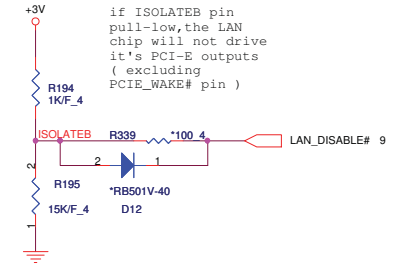
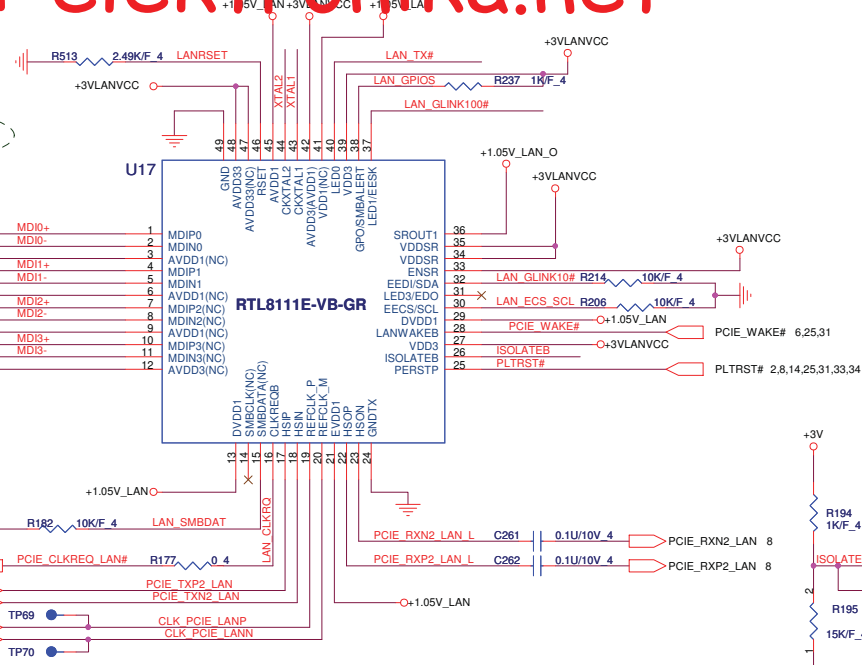
SI: Change L32 footprint to "12\_5x1.8-1.8-smt"

AL08111DB00 RTL8111DL-GR

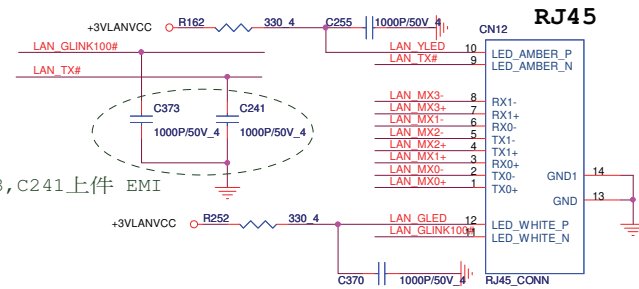


9/29 SI :C373,C241上件 EMI

9/29 SI :C659 1000P to 47P EMI

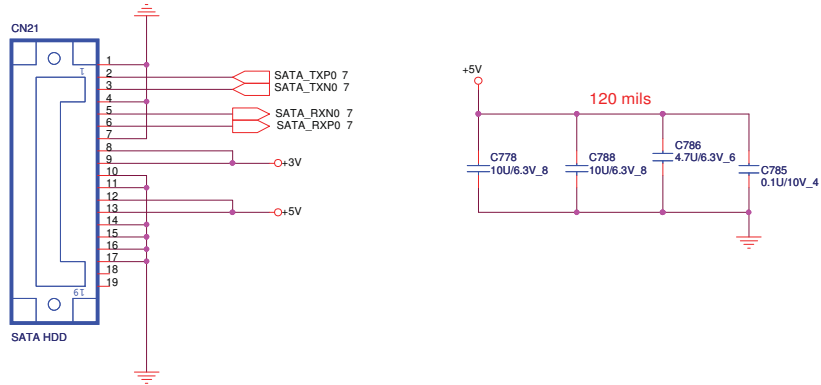


if ISOLATEB pin  
pull-low, the LAN  
chip will not drive  
it's PCI-E outputs  
( excluding  
PCIE\_WAKE# pin )



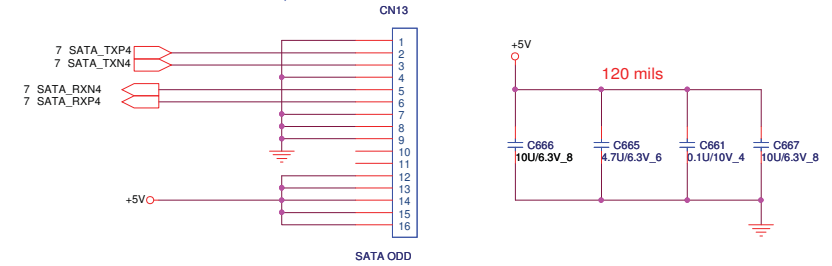
+3VLANVCC 41  
+3V 2,6,7,8,9,10,12,13,14,17,18,23,24,27,28,30,31,32,33,34,37,41

## SATA\_1 HDD CONNECTOR



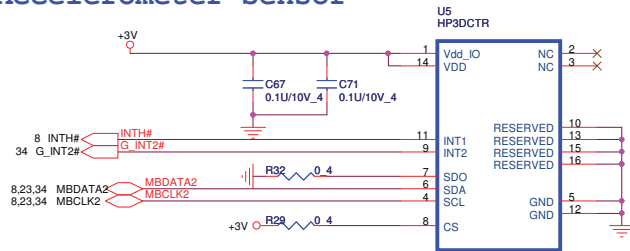
## SATA\_2 ODD CONNECTOR

2.5A >100mils TO M/B



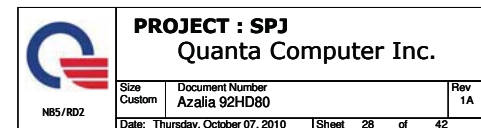
## Accelerometer Sensor

SGT-HP3DCTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low

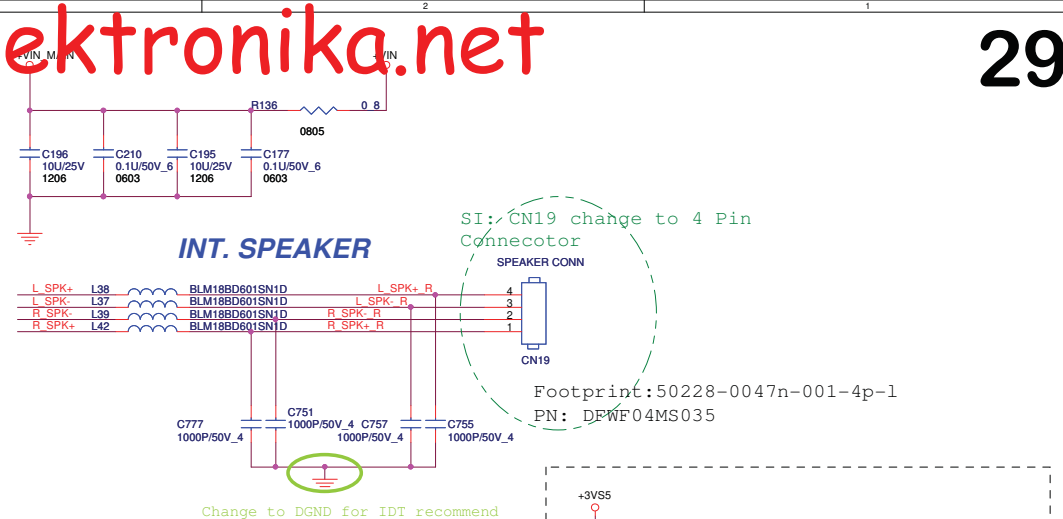


Pin 12: Low 38hex  
Pin 12: unconnected/floating 3Ahex

**A minimum of 15 mils separation should be used between L/R signals to audio jacks and docks.**



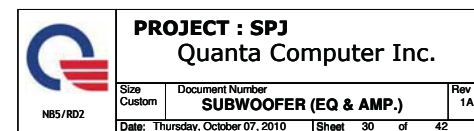


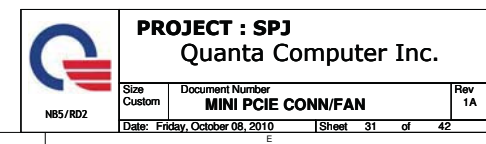
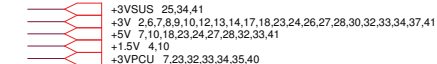


GAIN2	GAIN1	GAIN
0	0	20dB
0	1	26dB
1	0	32dB
1	1	36dB



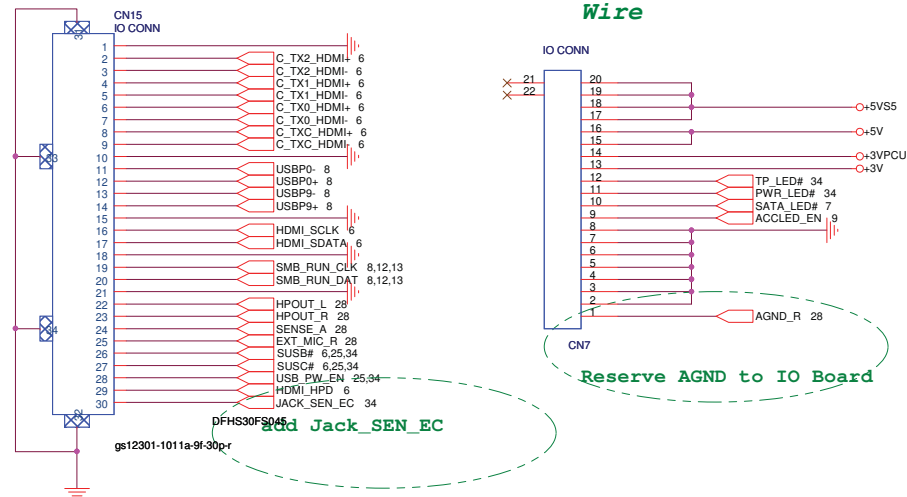
## C

1



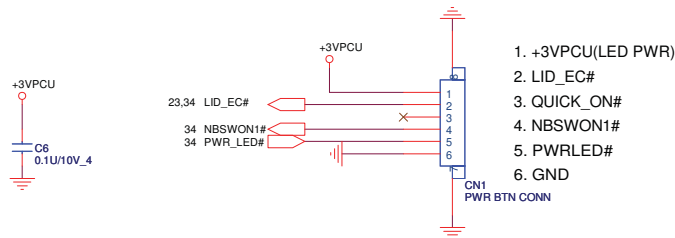
Size Custom	Document Number <b>KB/Hyper power/Hole</b>	Rev 1A
Date Thursday, October 07, 2010	Sheet 32 of 42	

To HDMI/ 2x USB2.0/Audio/HDD\_LED/PowerLED

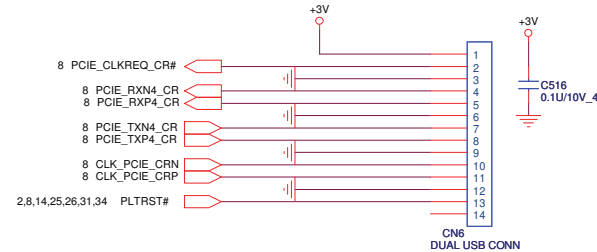


SI: Change CN15 Connector type, follow R11 LCD Conn. PN DFHS30FS045

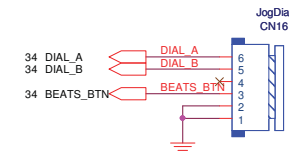
To PW\_BT/Quick Board



To CR Board



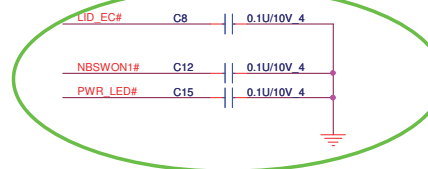
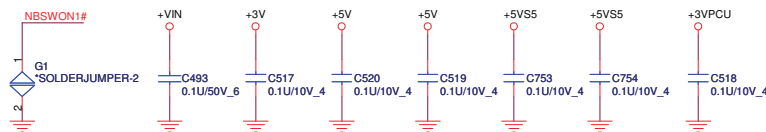
To JogDial Module



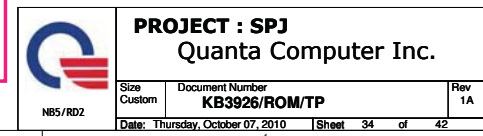
SI :Del C10

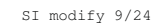
9/29 SI :C8,C12,C15 土件 EMI

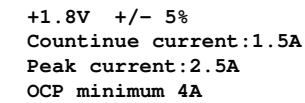
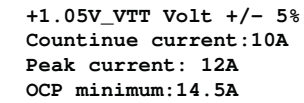
8/11 for EMI (DB)

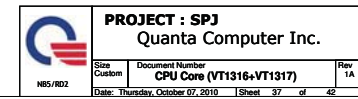


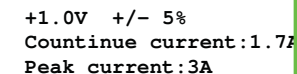
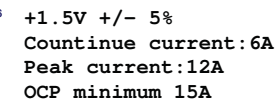






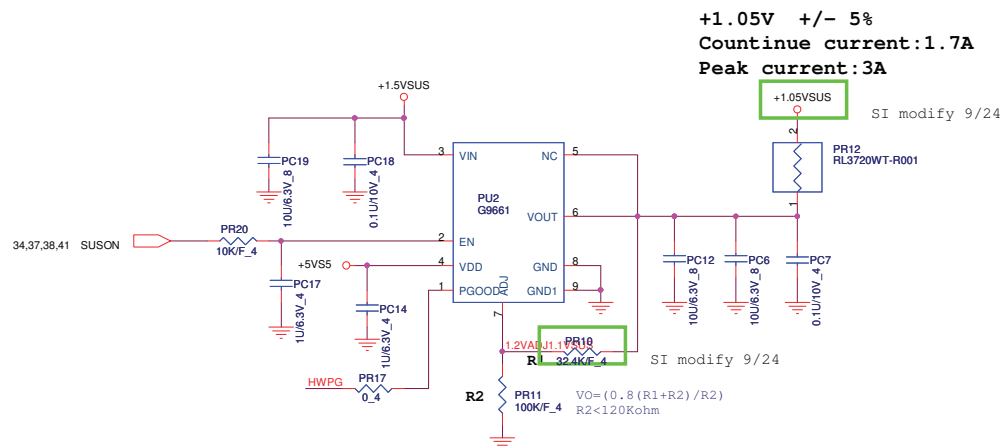
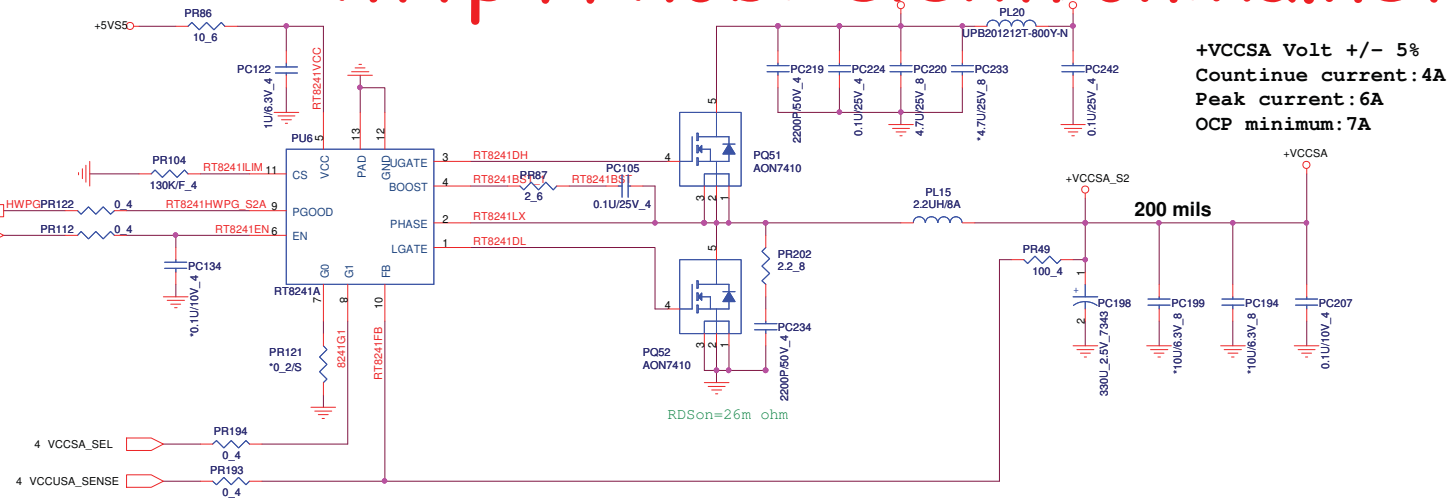


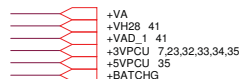


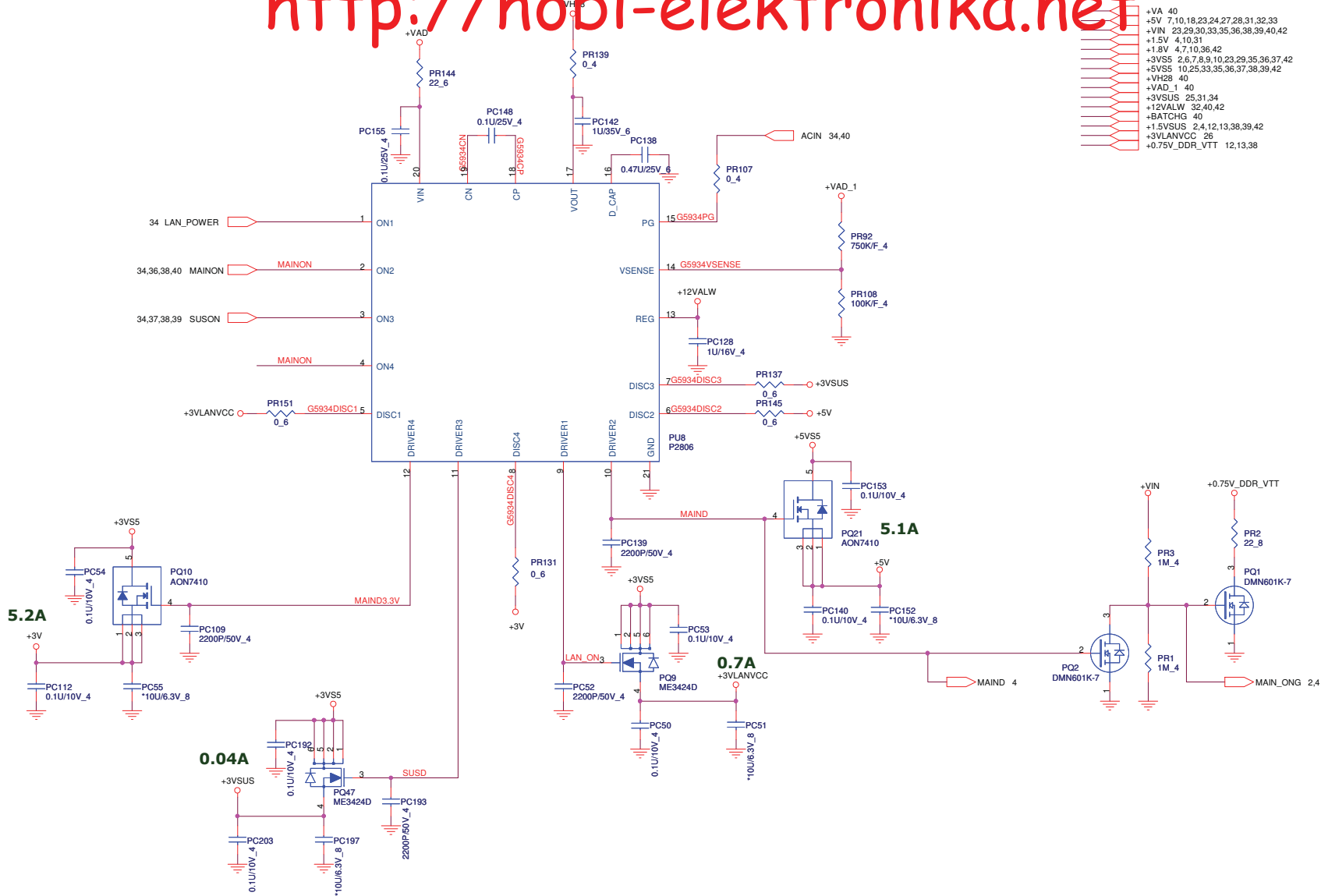


Size Custom	Document Number <b>DDR3 (RT8207)</b>	Rev 1A
Date: Thursday, October 07, 2010		Sheet 38 of 42









Size Custom	Document Number +VGACORE (RT8208/1.8V)	Rev 1/
Date: Friday, October 08, 2010	Sheet 42 of 42	