

Compal confidential

Low Cost Los Angeles 10AL+

NBWAE LA-5831P Schematics Document

Mobile AMD S1G2

RS780MN & RS780MC / SB700

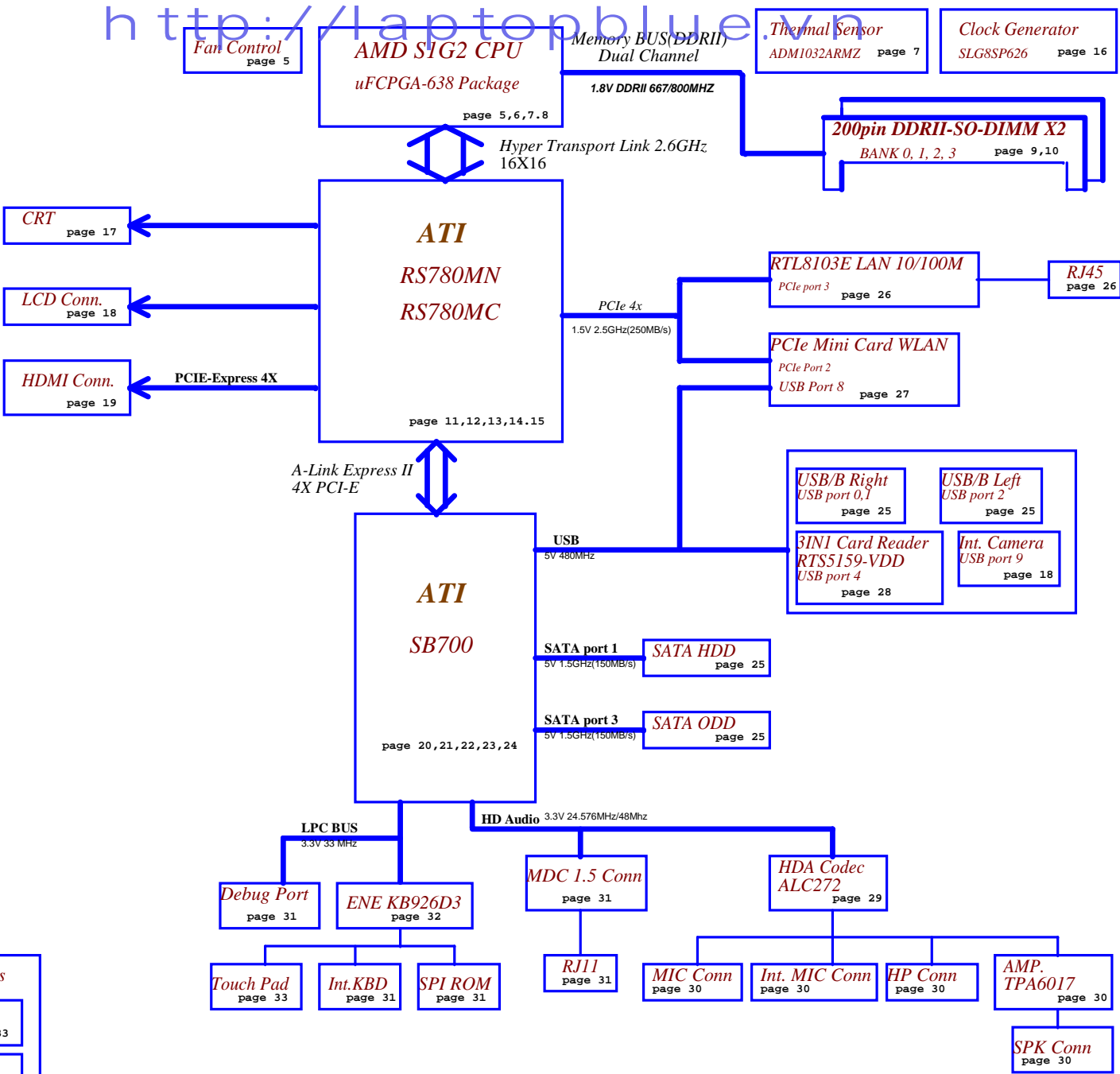
2009-08-12 Rev. 1.0

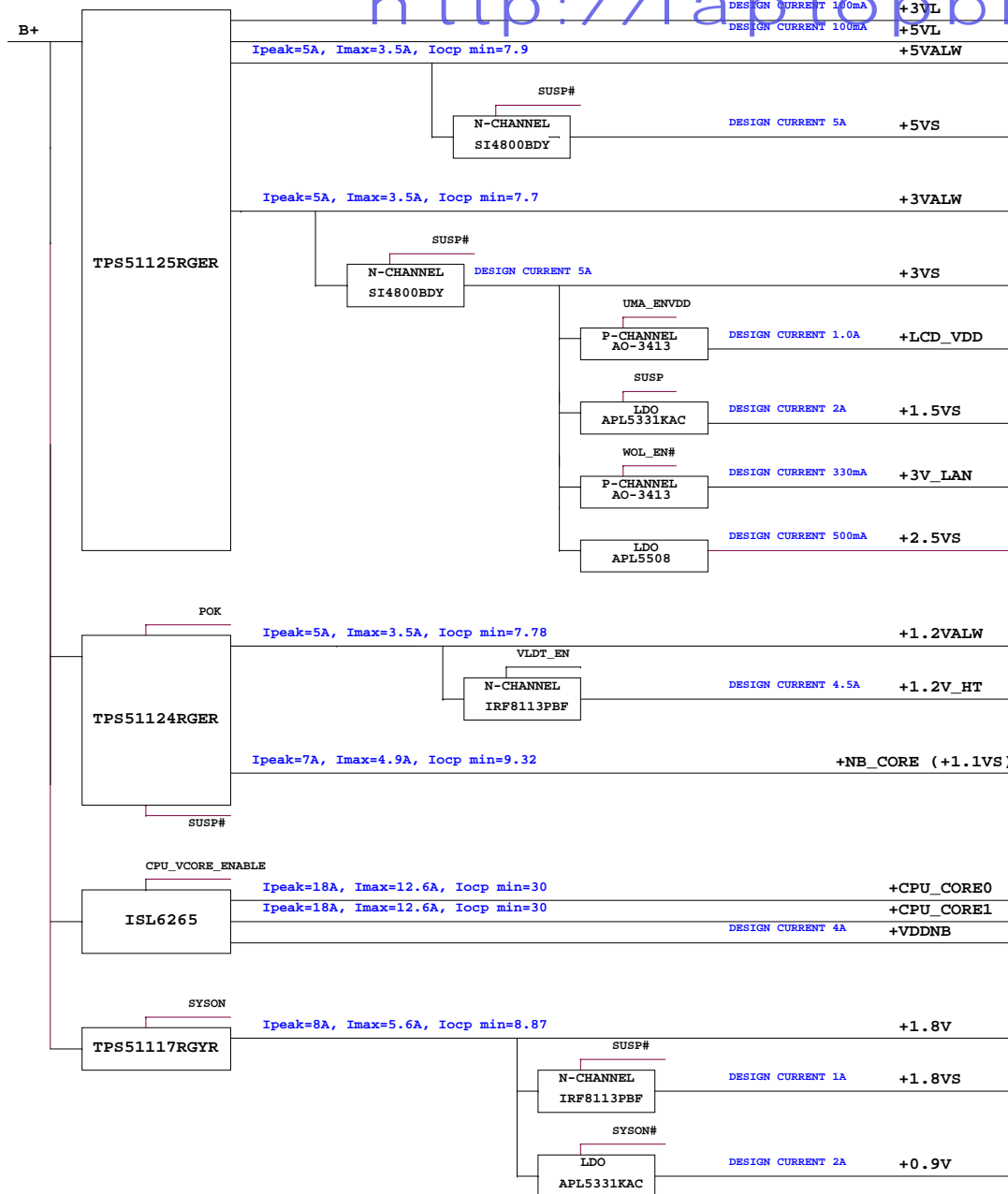
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	Title Cover Sheet	
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Model Name : NBWAE

File Name : LA-5831P





Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	Title	Power Map
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Voltage Rails

O : ON
X : OFF

State \ power plane				
	B+ +3VL +5VL +RTCVCC	+5VALW +3VALW +1.2VALW +3V_LAN	+1.8V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +1.2V_HT +VDDNB +CPU_CORE_0 +CPU_CORE_1
	S0	O	O	O
	S1	O	O	O
	S3	O	O	X
	S5 S4/AC	O	O	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SB700 SM Bus0 Address				SB700 SM Bus1 Address			
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b	+3VALW	WLAN/WIMAX		
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b				
+3VS	Clock Generator	D2 H	1101 0010 b				

KB926 SM Bus1 Address				KB926 SM Bus2 Address			
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 011X b	+3VS	CPU_ADM1032-1	98 H	1001 100X b
KB926 ESB Address							
Power	Device	HEX	Address				
+3VL	Cap. Sensor		Virtual I2C				

Platform	CPU	NB	SB
PUMA@	S1G2	RS780MC	SB700
	S1G2	RS780MN	SB700
TIGRIS@	S1G3	RS880MC	SB710
	S1G3	RS880M	SB710

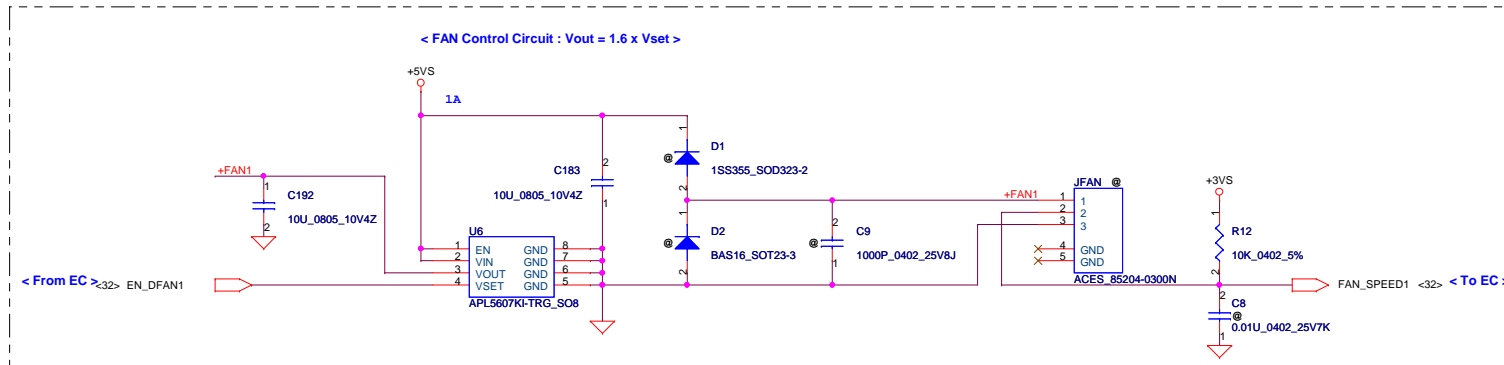
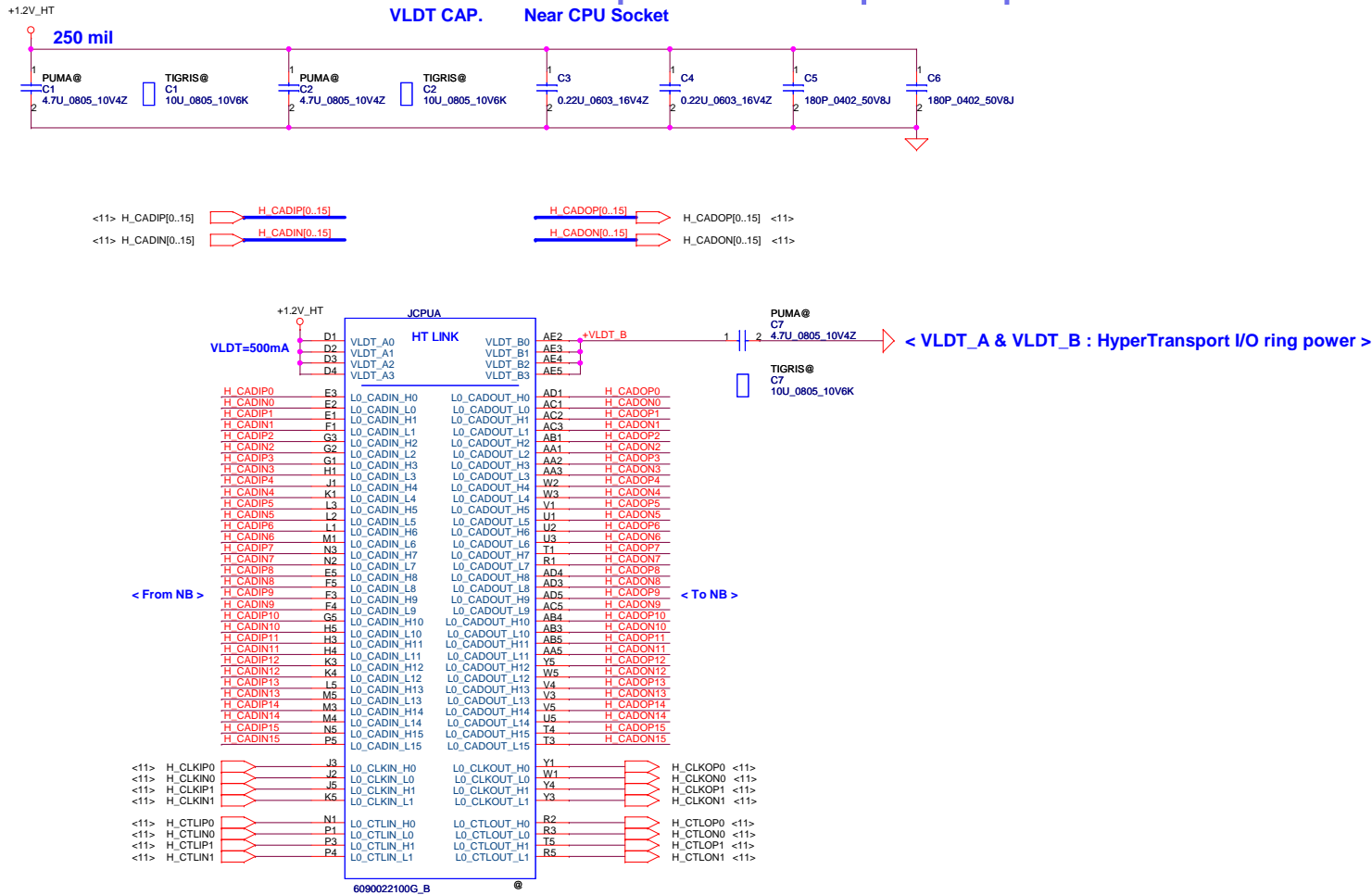
@ : just reserve , no build

BTO (Build-To-Order) Option Table

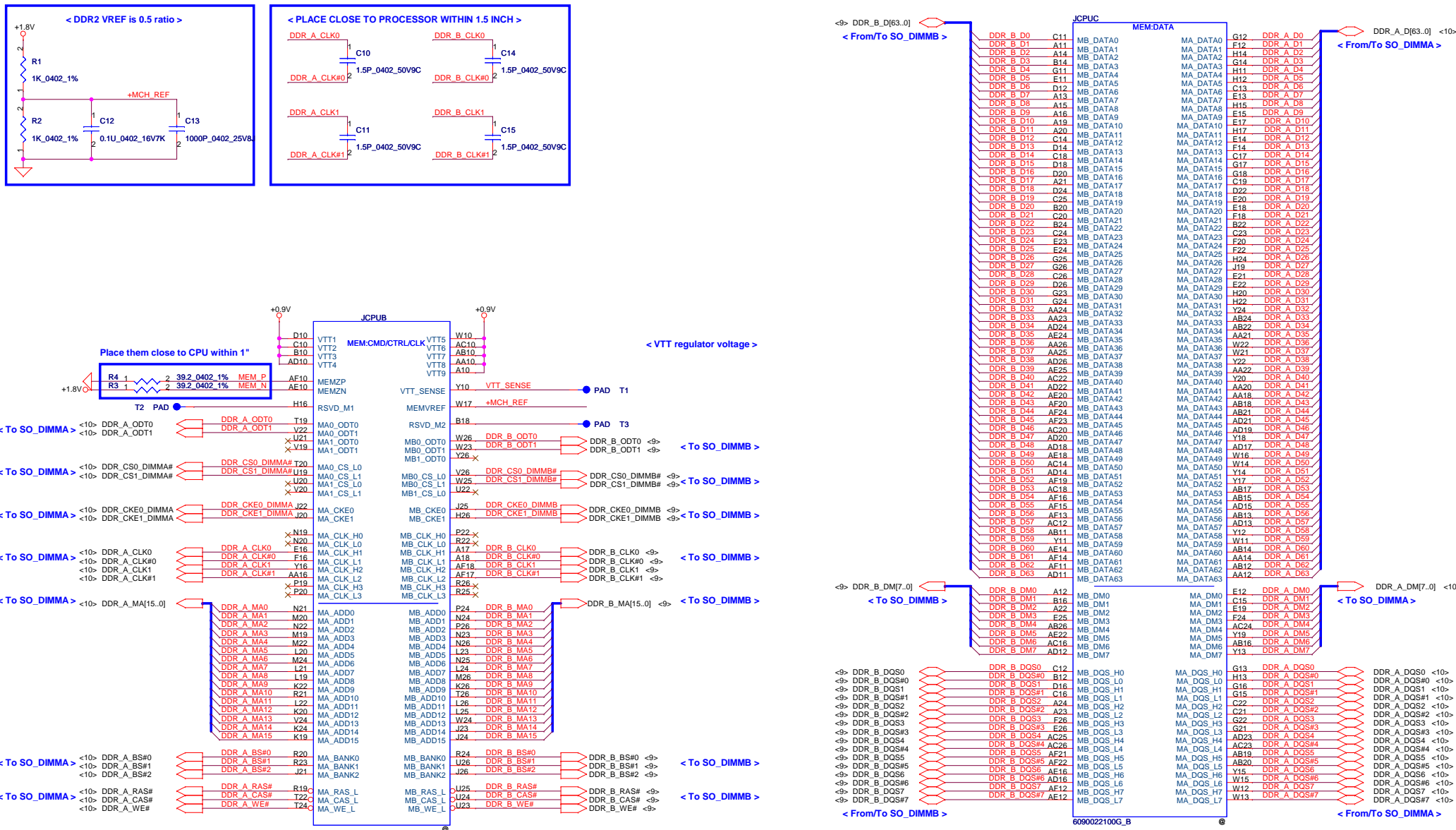
Function	Modem	HDMI	CAMERA & MIC	
Description	(R)	(Y)	(X)	
Explain			CAMERA	MIC
BTO	MDC@	HDMI@	CAM@	MIC@

SMBUS Control Table

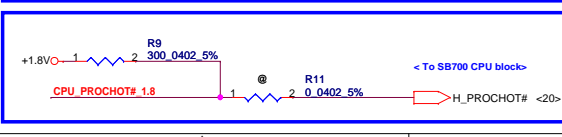
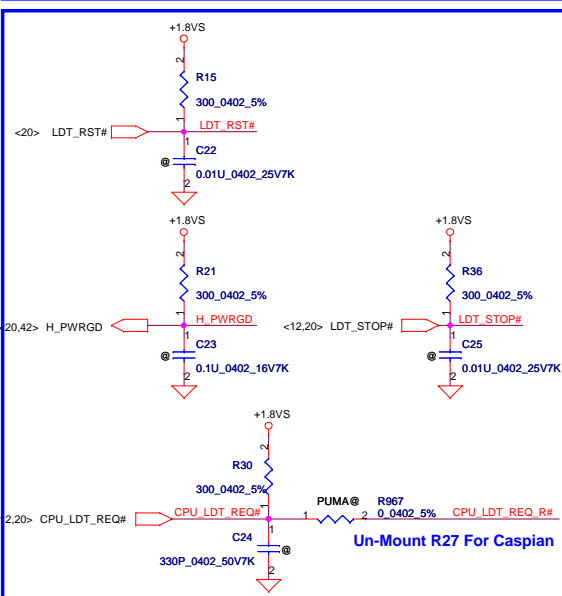
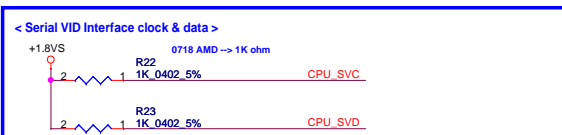
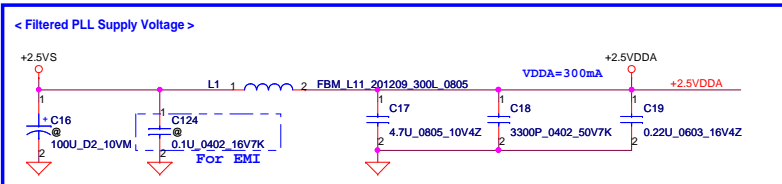
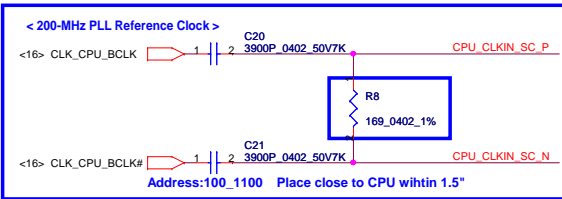
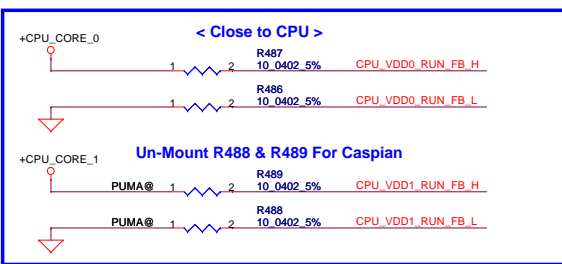
	SOURCE	INVERTER	BATT	HDMI CEC	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM	NEW CARD
EC_SMB_CK1 EC_SMB_DA1	KB926		V								
EC_SMB_CK2 EC_SMB_DA2	KB926				V						
I2C_CLK I2C_DATA	RS780MN RS780MC								V		
DDC_CLK0 DDC_DATA0	RS780MN RS780MC									V	
DDC_CLK1 DDC_DATA1	RS780MN RS780MC										
SCL0 SDA0	SB700					V	V				
SCL1 SDA1	SB700							V			
SCL2 SDA2	SB700										
SCL3 SDA3	SB700										



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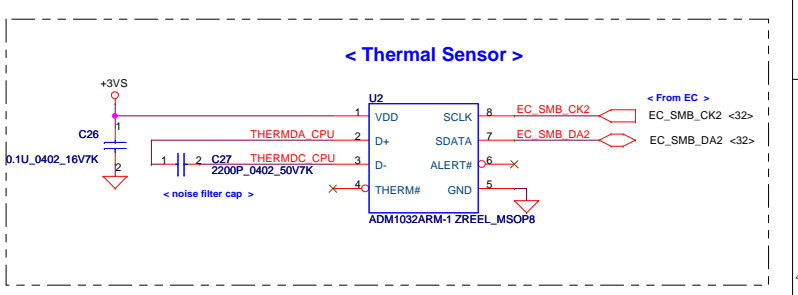
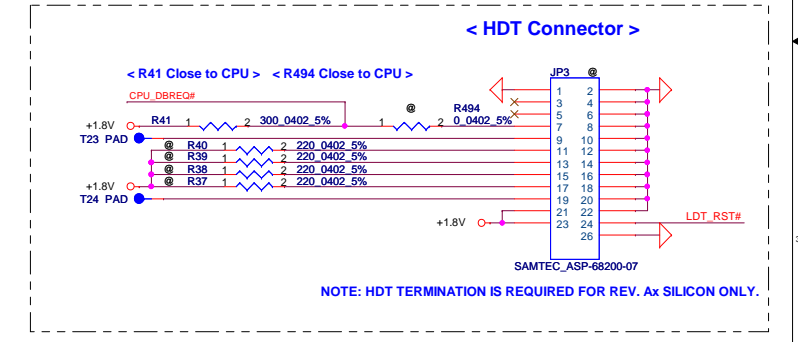
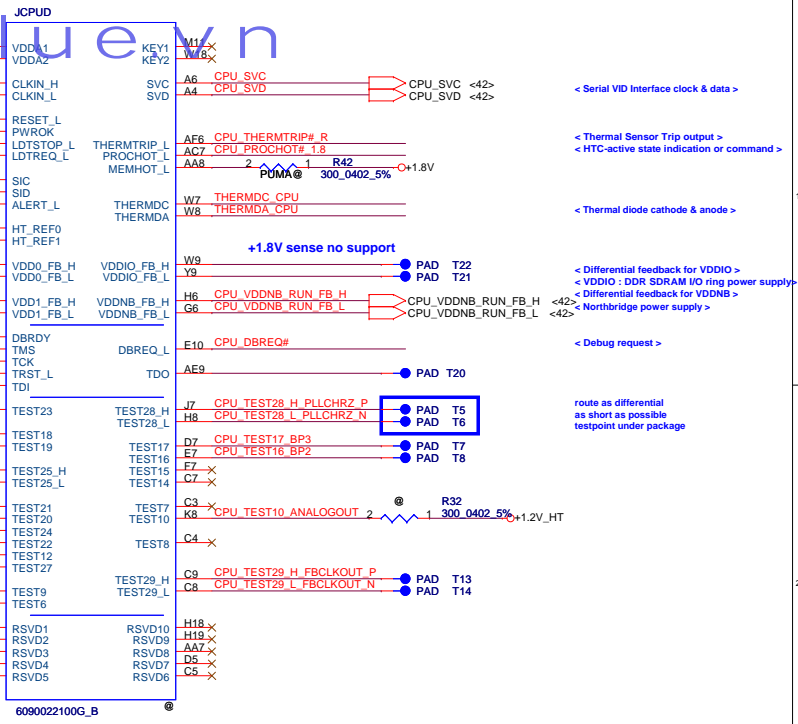
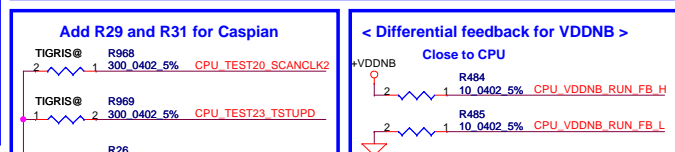
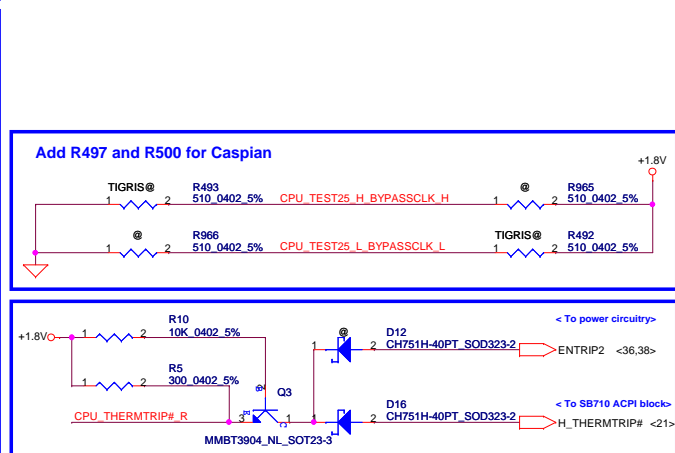
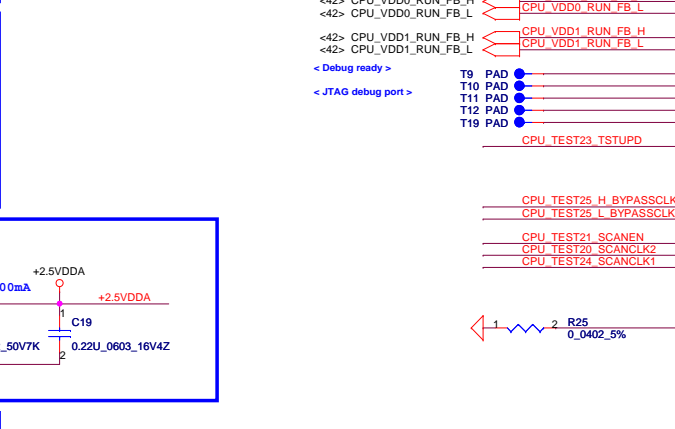


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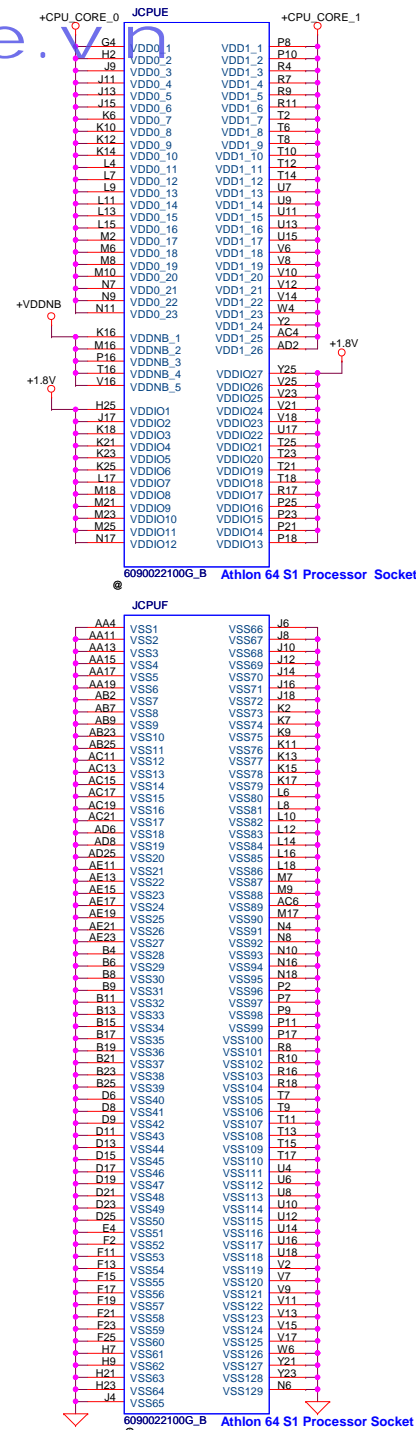
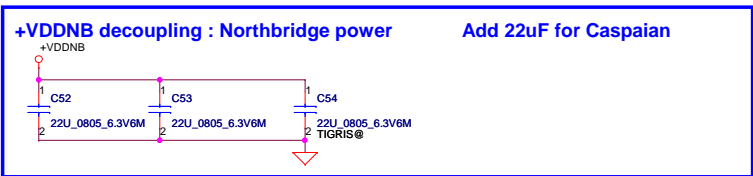
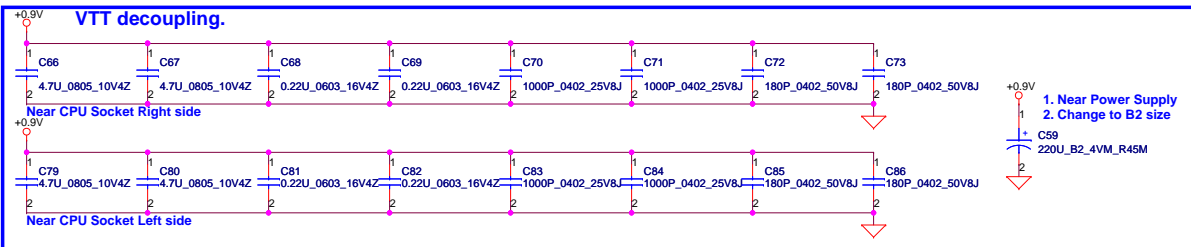
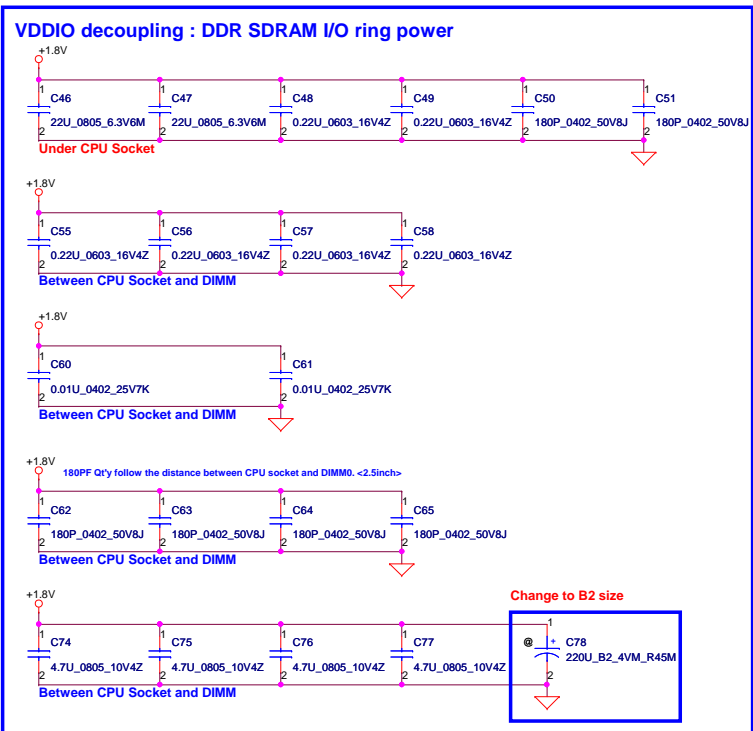
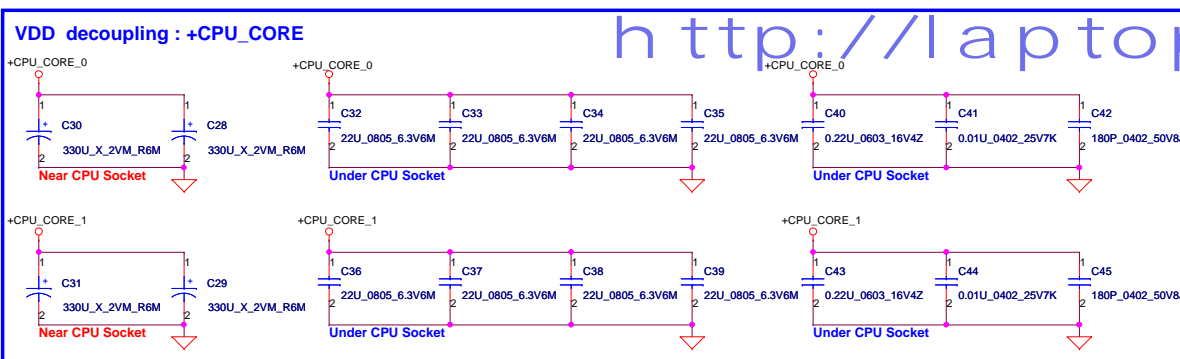
< Sideband-Temperature Sensor Interface interrupt >

< Compensation Resistor to VSS >

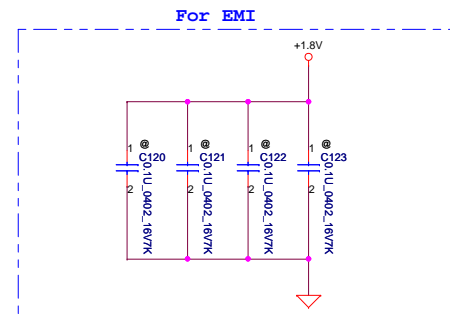
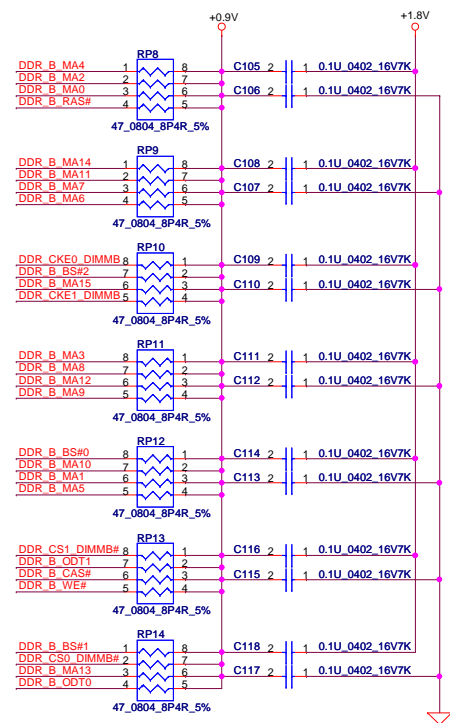
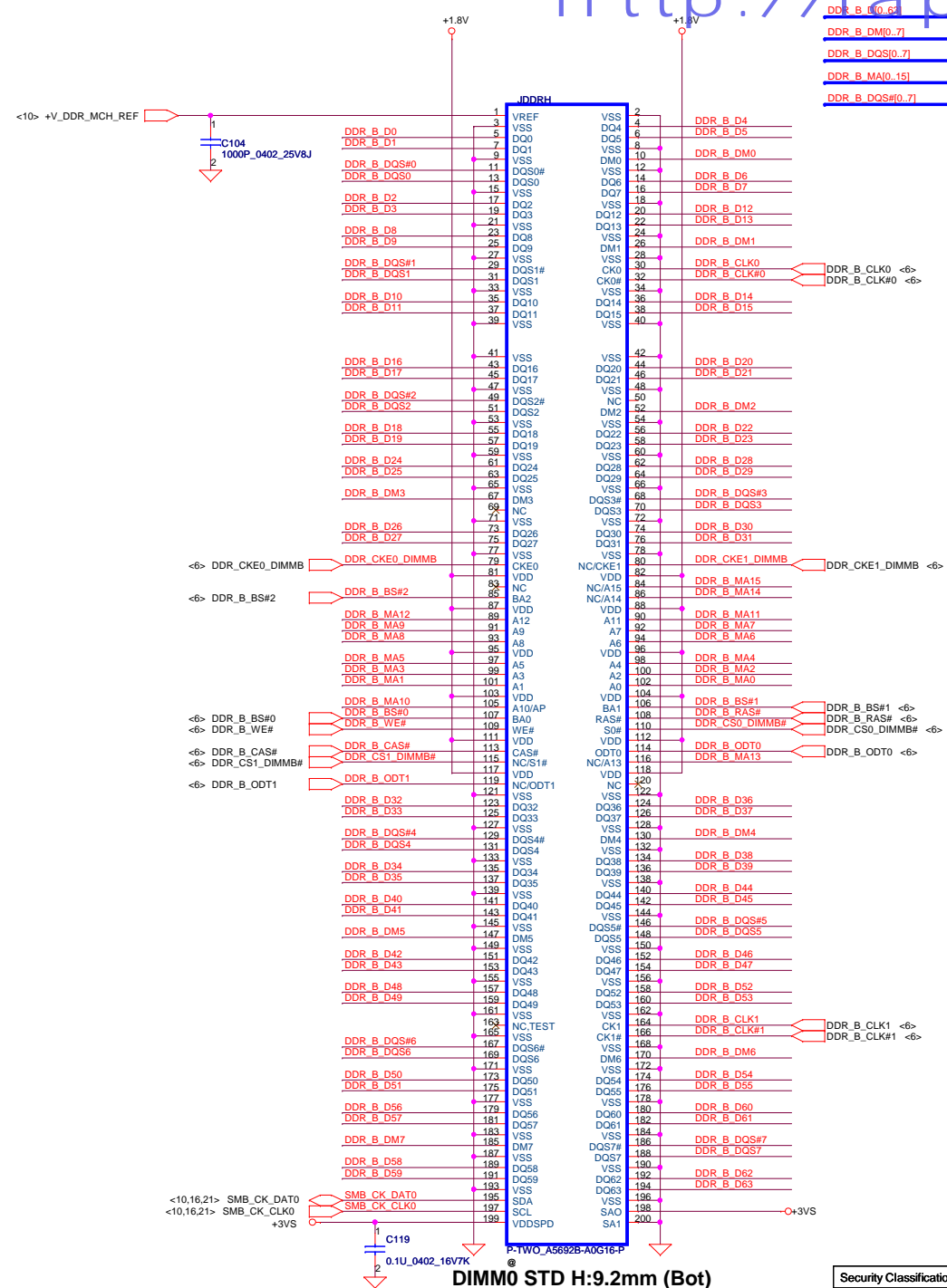
< Compensation Resistor to VLDIT >



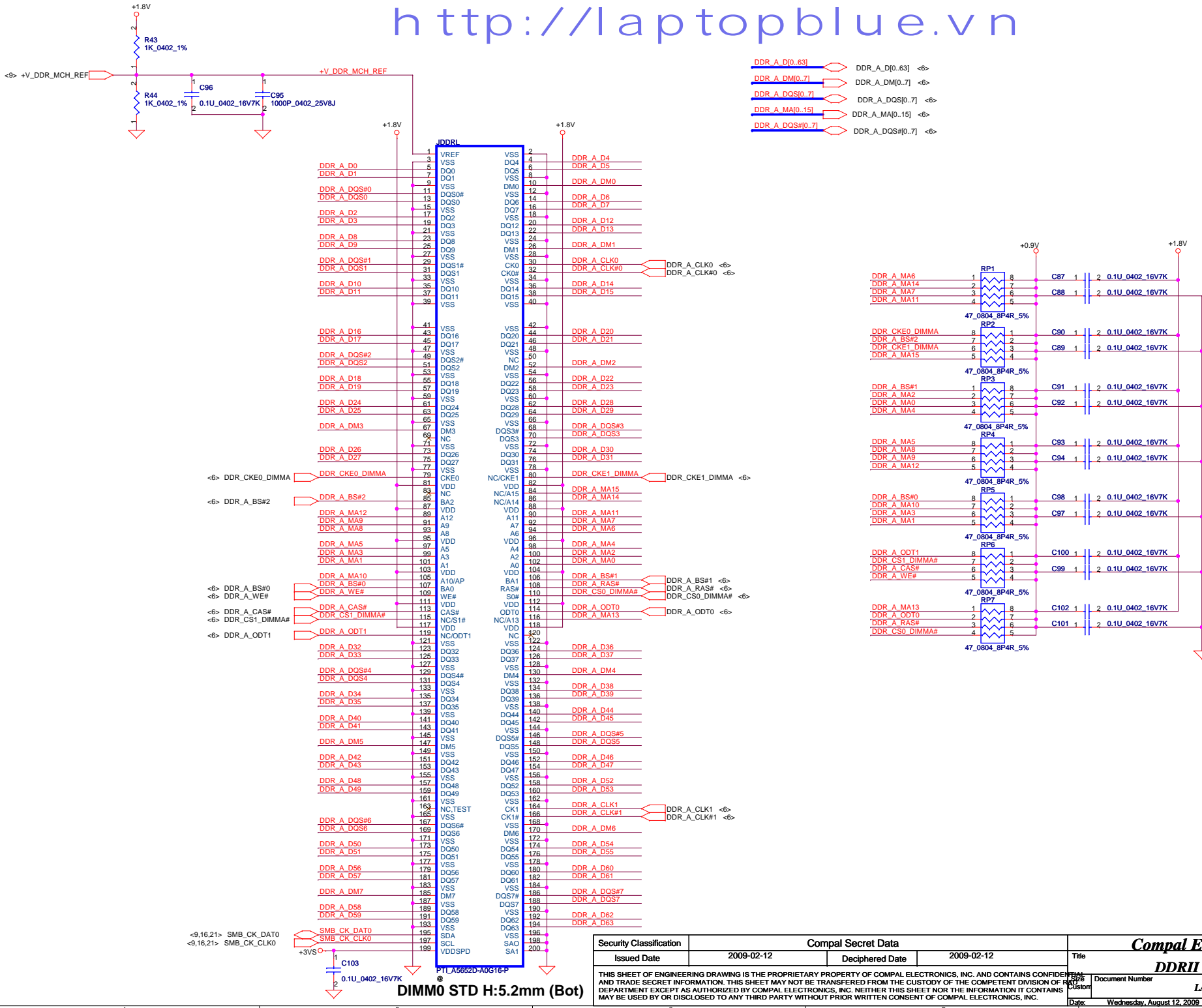
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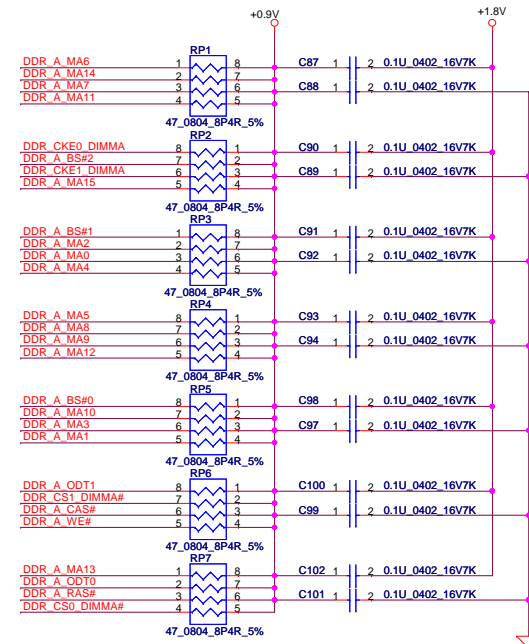
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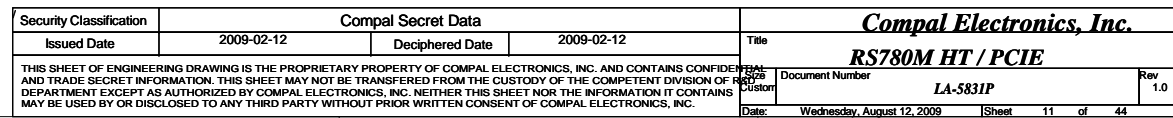
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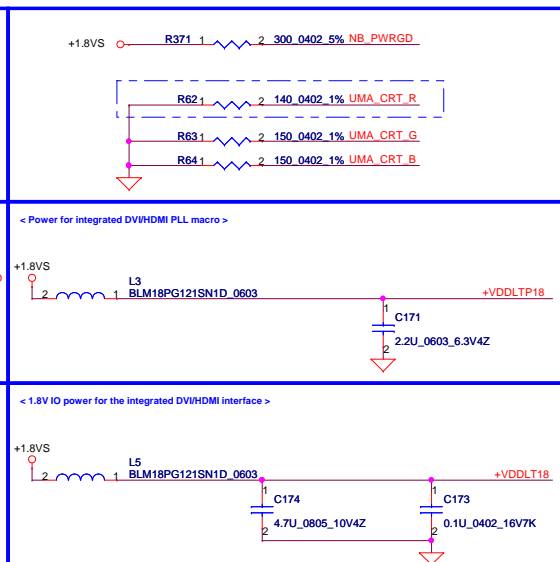
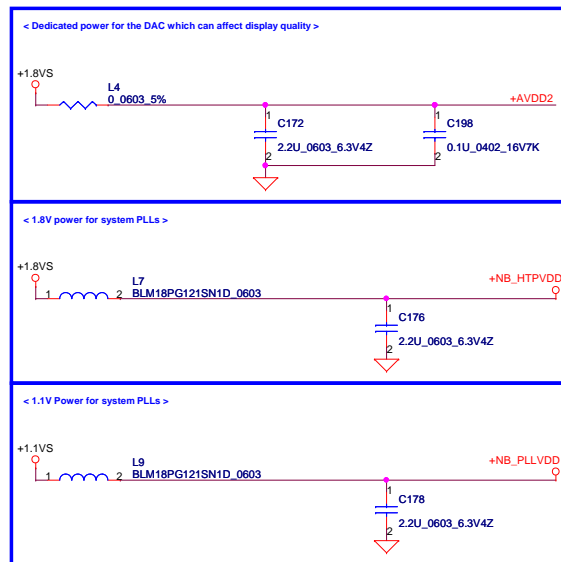
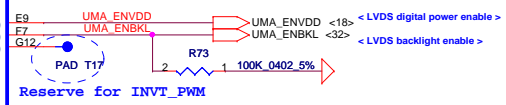


- DDR A D[0..63] <6>
- DDR A DM[0..7] <6>
- DDR A DQS[0..7] <6>
- DDR A MA[0..15] <6>
- DDR A DQS# [0..7] <6>



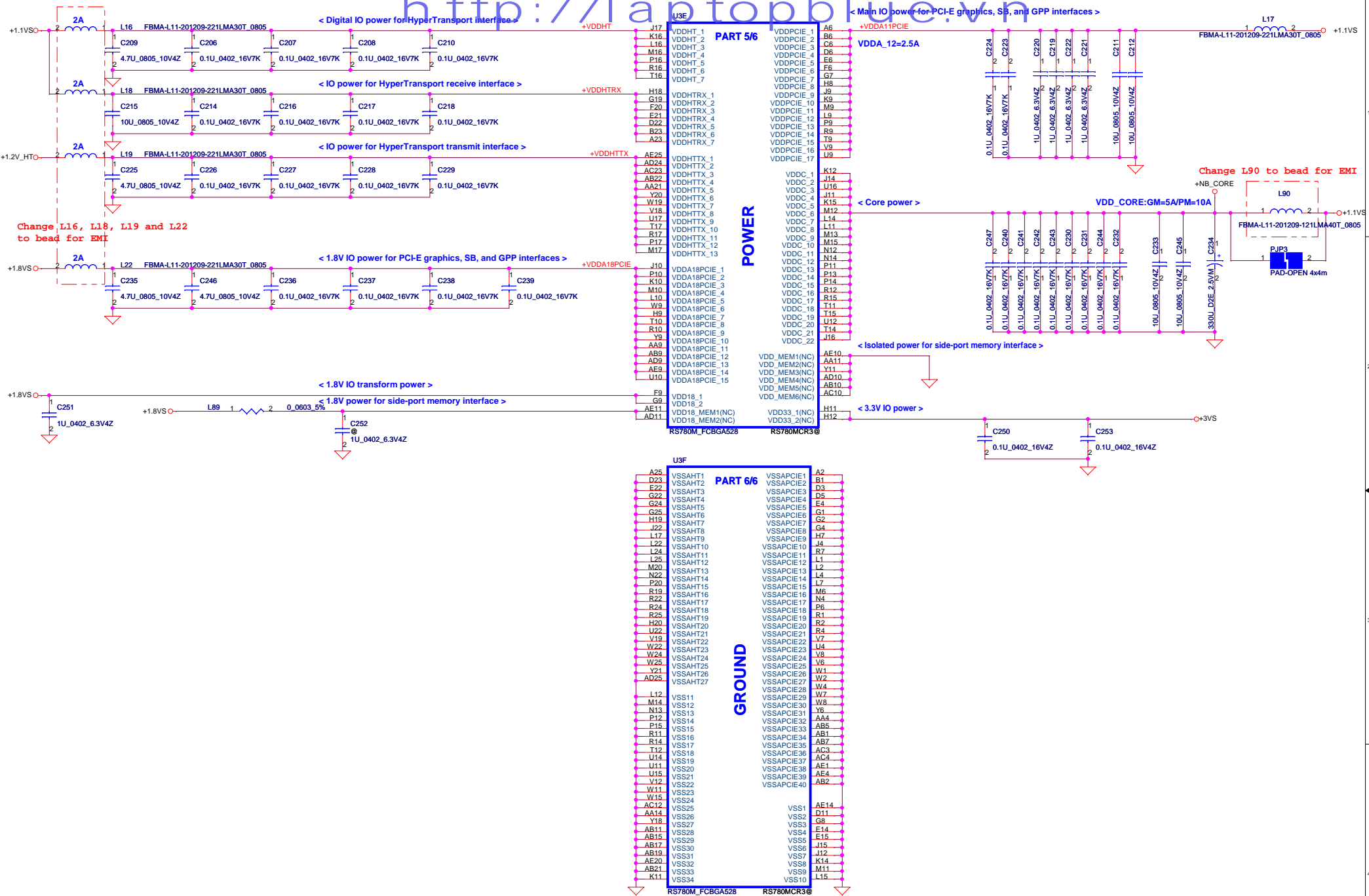
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Issued Date	2009-02-12	Deciphered Date	2009-02-12	DDR2 SO-DIMM 1	
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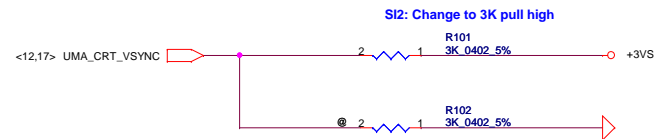
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Issued Date	2009-02-12	Deciphered Date	2009-02-12	Title	RS780M VEDIO/CLK GEN
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< RS780 DFT_GPIO5 mux at CRT_VSYNC pull High to 3K >



< DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLED >

Enables the Test Debug Bus using GPIO.

1 : Enable (RX780, RS780)
0 : Disable (RX780, RS780)

PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#

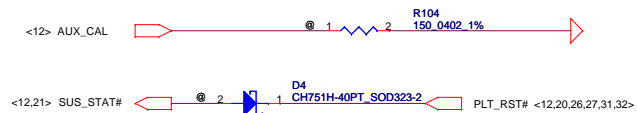
< RS780 use register to control PCI-E configure >

< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] >

These pin straps are used to configure PCI-E GPP mode.

000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011

< RS780 DFT_GPIO1 >



< DFT_GPIO1 : LOAD_EEPROM_STRAPS >

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS740/RX780: DFT_GPIO1 RS780:SUS_STAT

< RS780 use HSYNC to enable SIDE PORT (internal pull high) >



< DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb >

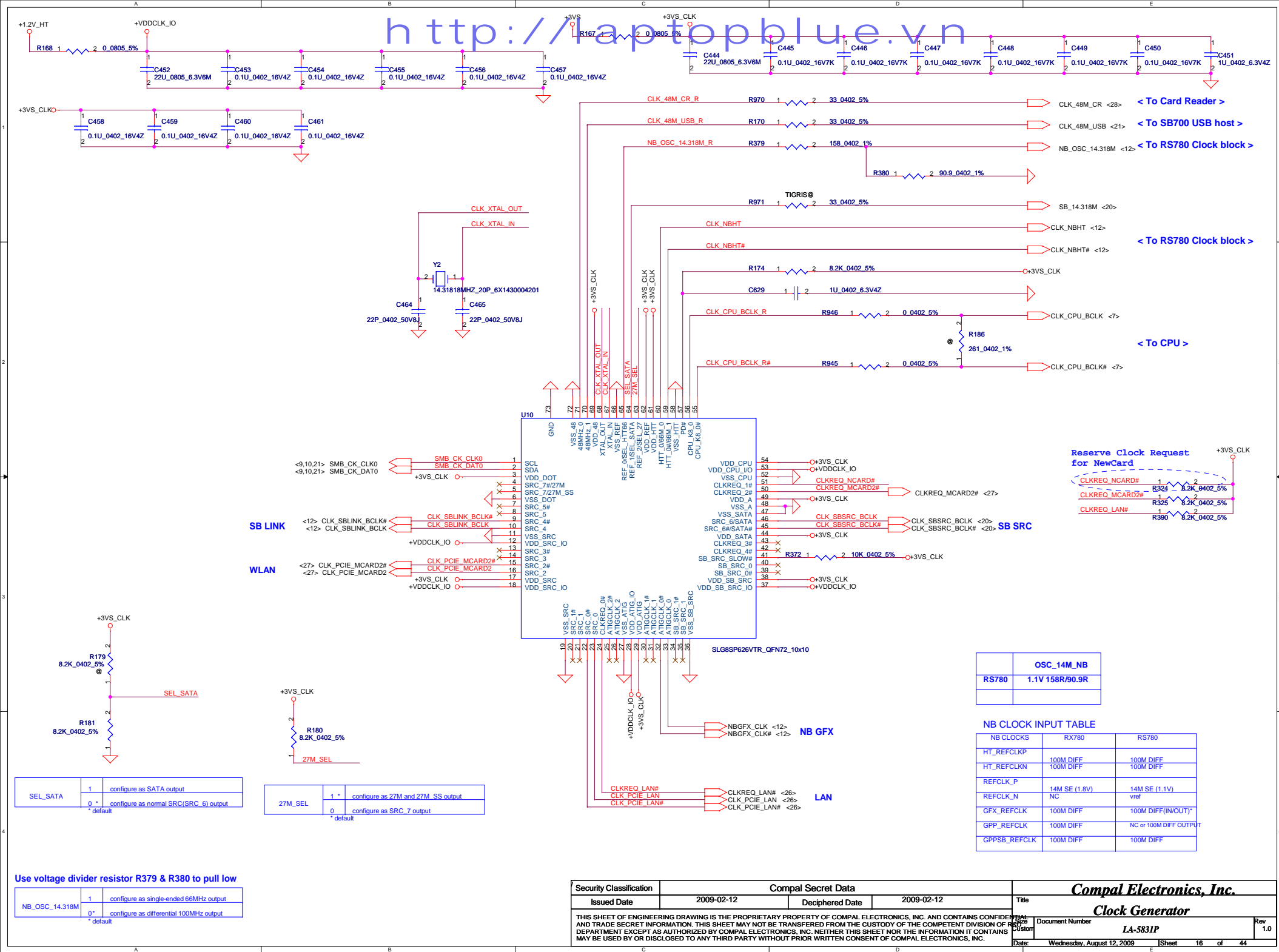
RX780: Enables the Test Debug Bus using PCIE bus

1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS780)
0 : Enable (RS780)

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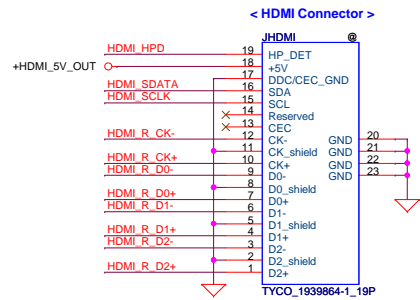
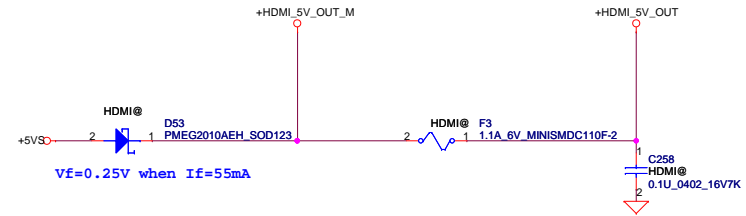


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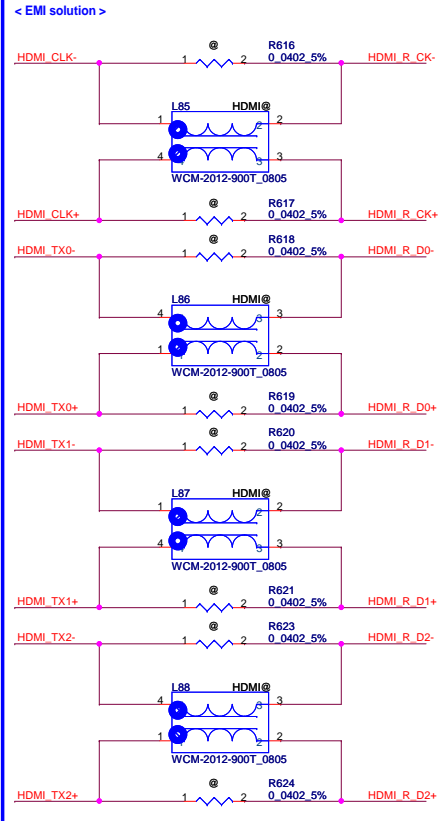
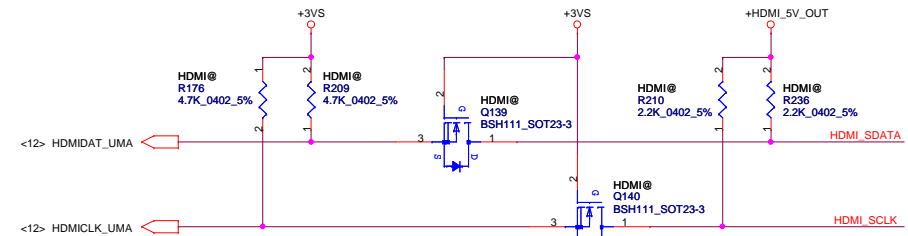
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Issued Date	2009-02-12	Deciphered Date	2009-02-12	Title	
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<11>	HDMI_TXD0+	HDMI@	C189	1	2	0.1U_0402_16V7K	HDMI_TX0+
<11>	HDMI_TXD0-	HDMI@	C188	1	2	0.1U_0402_16V7K	HDMI_TX0-
<11>	HDMI_TXD1+	HDMI@	C190	1	2	0.1U_0402_16V7K	HDMI_TX1+
<11>	HDMI_TXD1-	HDMI@	C184	1	2	0.1U_0402_16V7K	HDMI_TX1-
<11>	HDMI_TXD2+	HDMI@	C187	1	2	0.1U_0402_16V7K	HDMI_TX2+
<11>	HDMI_TXD2-	HDMI@	C191	1	2	0.1U_0402_16V7K	HDMI_TX2-
<11>	HDMI_CLK0+	HDMI@	C185	1	2	0.1U_0402_16V7K	HDMI_CLK+
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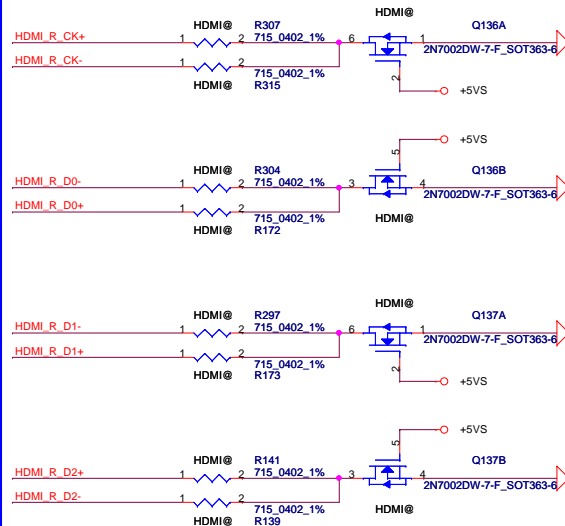


< HDMI DDC channel to device >

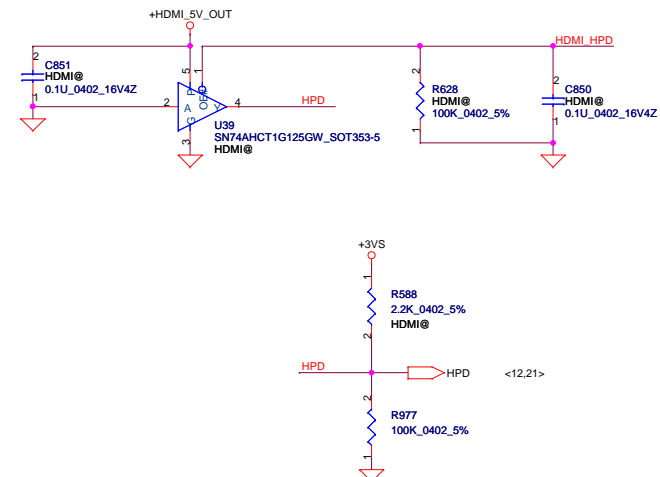
< Place MOSFET close to HDMI connector >



< Termination resistor >



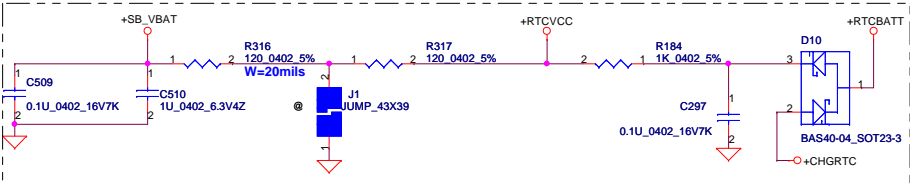
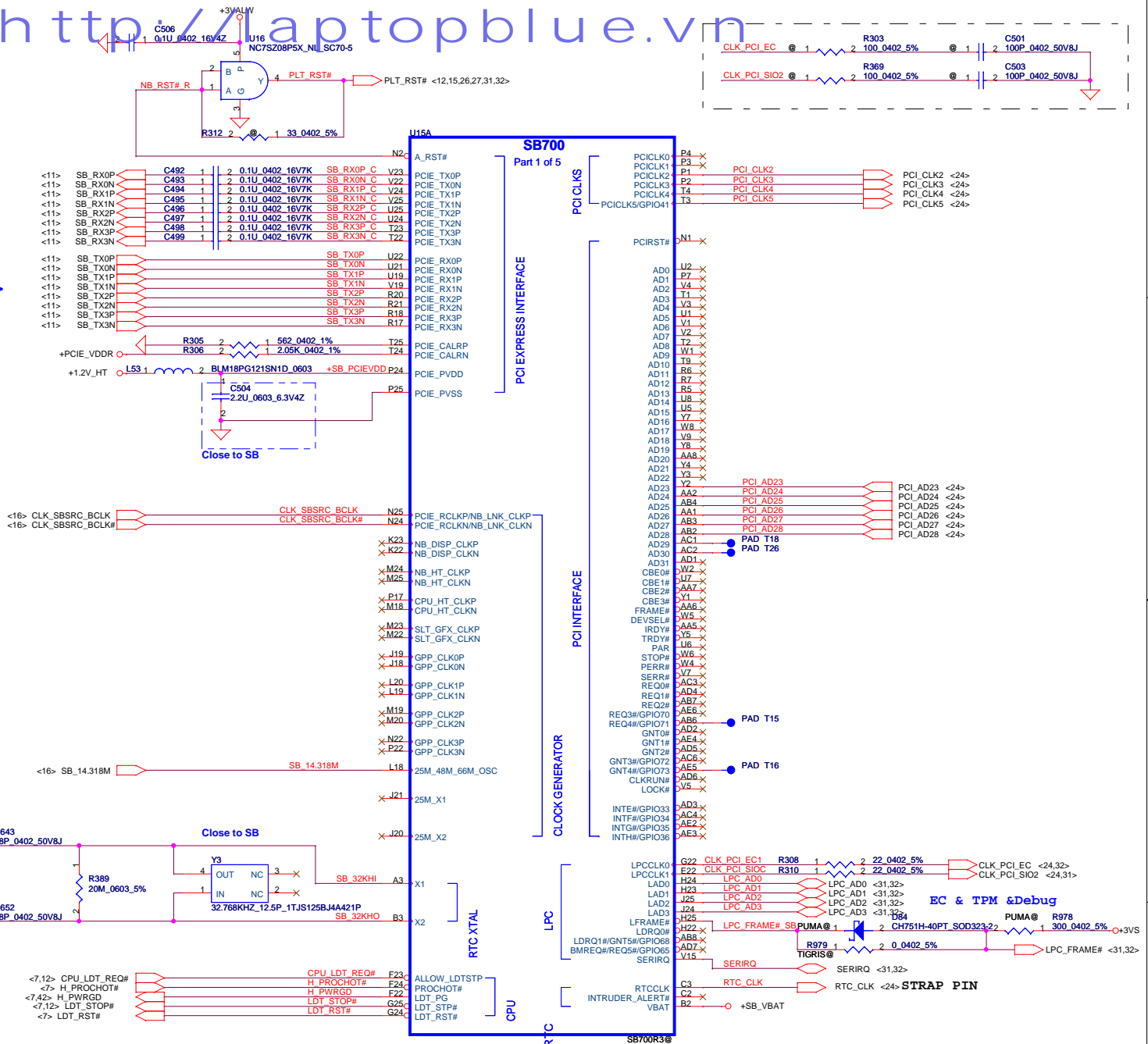
< Hot-plug detection & level shift >



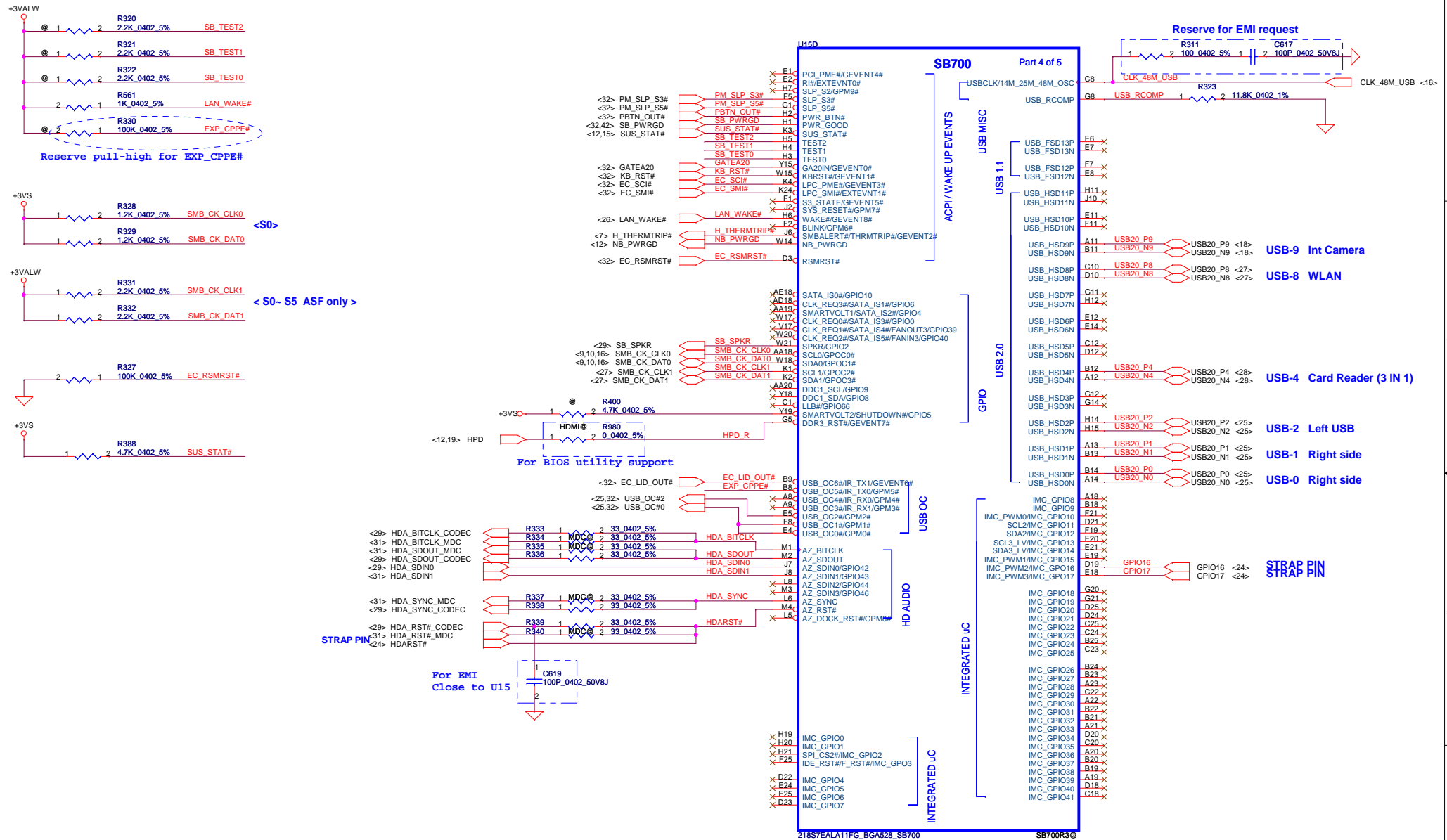
Security Classification	Compal Secret Data			Title	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	HDMI	
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< x4 PCIE A-link To NB >

< x4 PCIE A-link from NB >



Security Classification		Compal Secret Data		Title	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	SB700 - PCIE / PCI / ACPI / LPC / RTC	
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				Rev	1.0
				Date	Wednesday, August 12, 2009
				Sheet	20 of 44

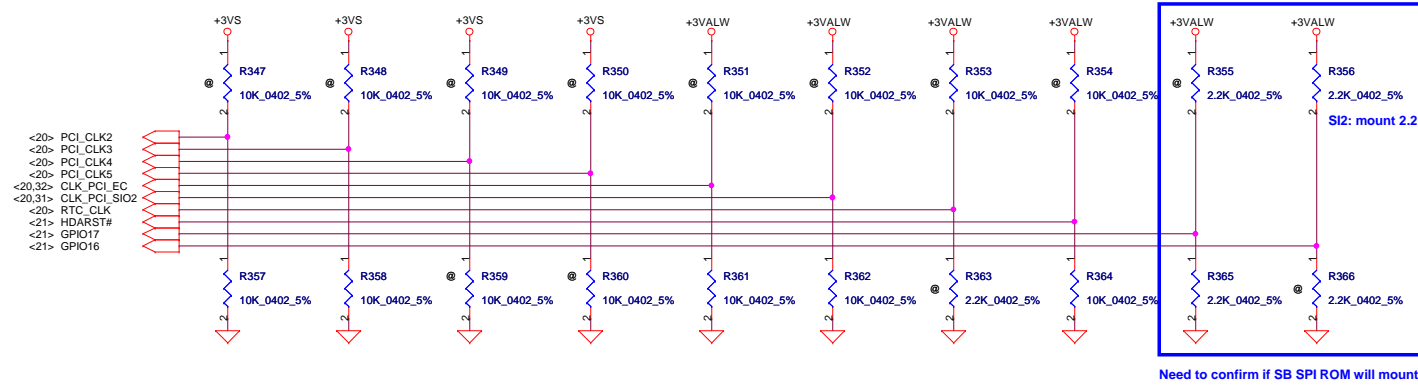


Security Classification		Compal Secret Data		Compal Electronics, Inc. SB700 USB / AC97	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	Title	
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Date:		Wednesday, August 12, 2009		Sheet	21 of 44

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

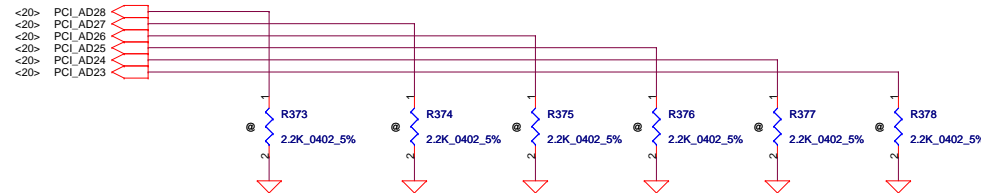
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		



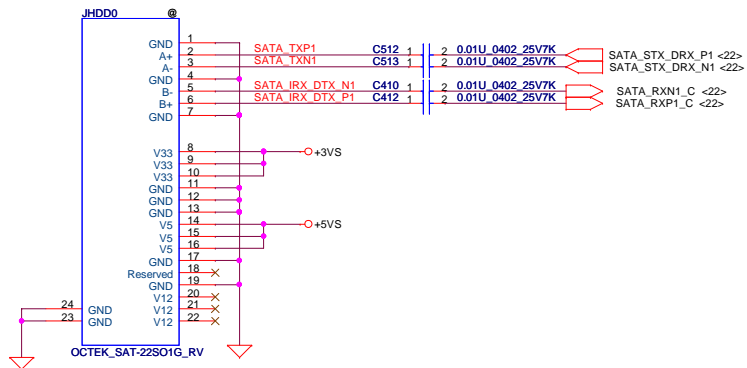
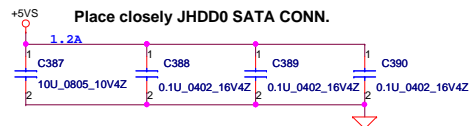
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

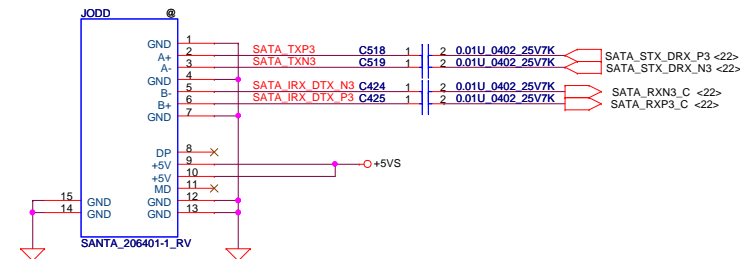
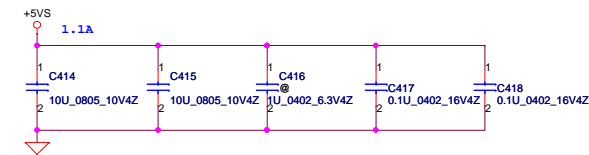
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



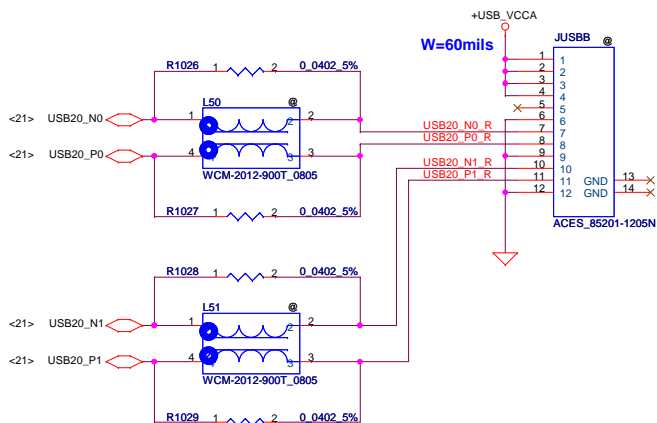
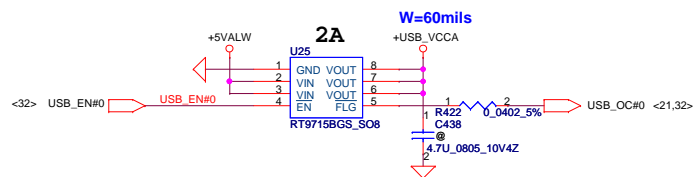
SATA HDD Conn.



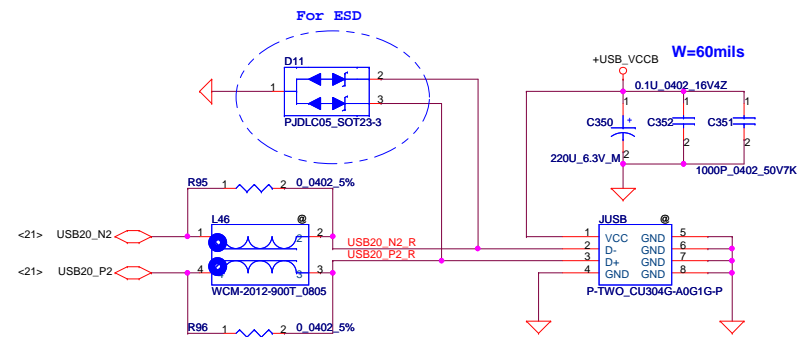
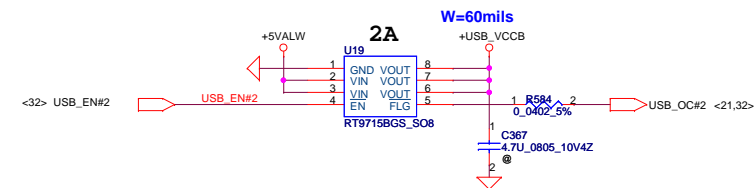
SATA ODD Conn



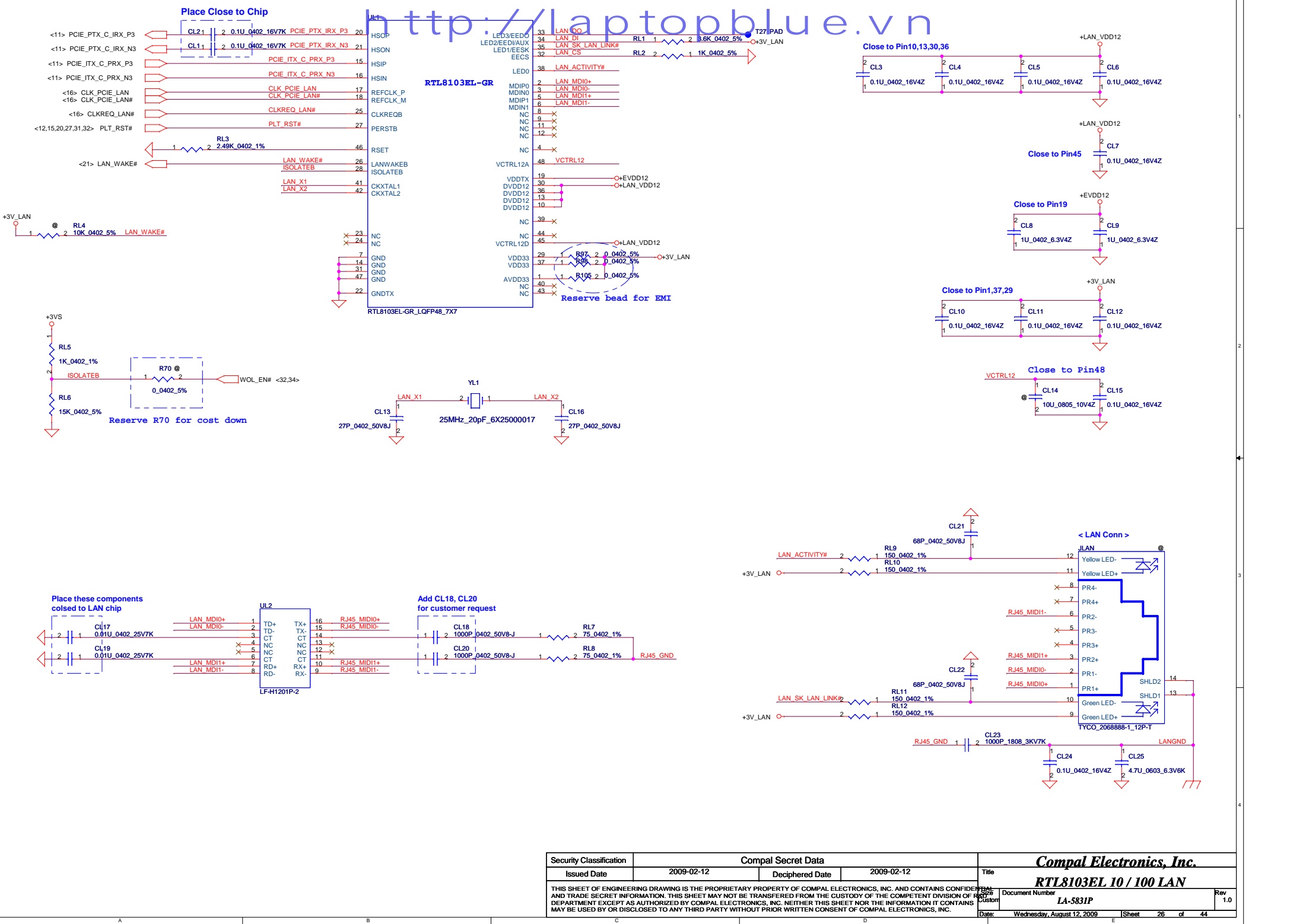
USB Right Board



USB Left Conn

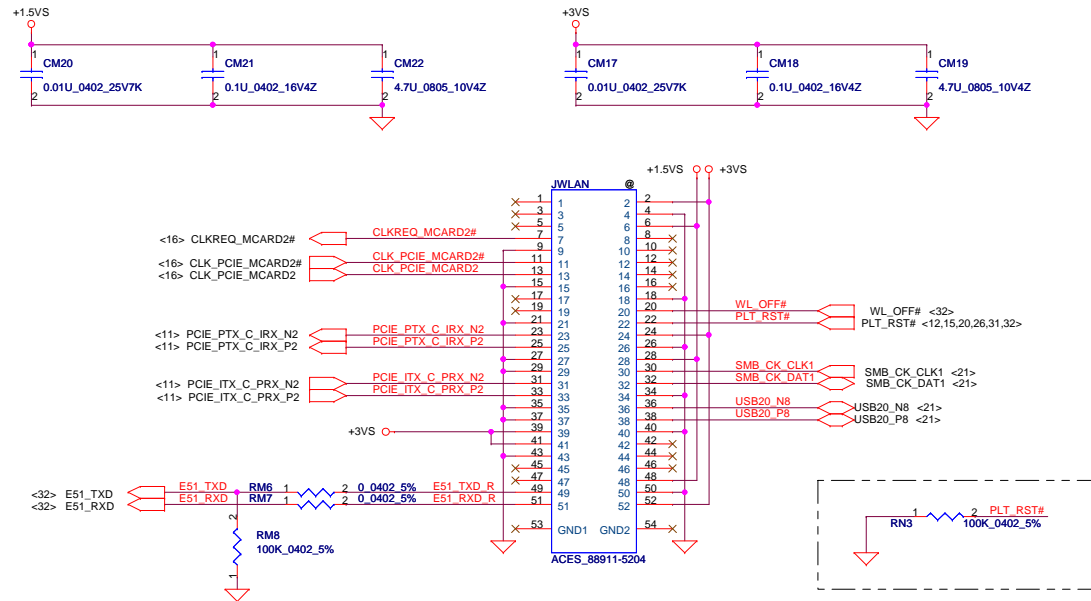


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2008/04/14				Title			
Deciphered Date				2009/04/14				SATA HDD/ODD			
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Security Classification				Compal Secret Data				Title			
Issued Date				2009-02-12				Deciphered Date			
2009-02-12				2009-02-12				Date			
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				Custom				LA-5831P			
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								Sheet 26 of 44			

< PCIe Mini Card for WLAN/ WiMAX >



<NB & SB >

< R1 for customer BOM STRUCTURE >

< R3 for mass production BOM STRUCTURE >

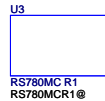
RS780MN



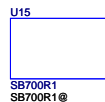
RS780MN



RS780MC



SB700



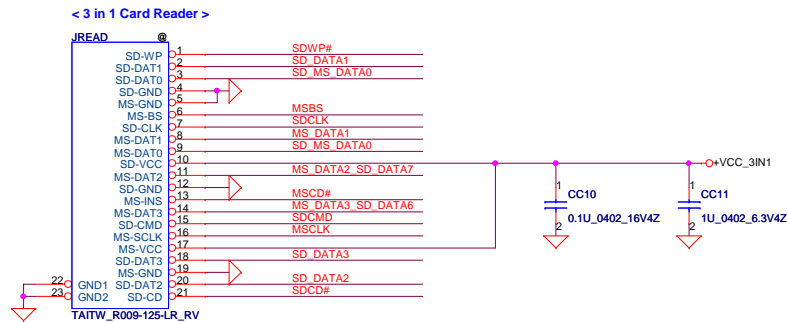
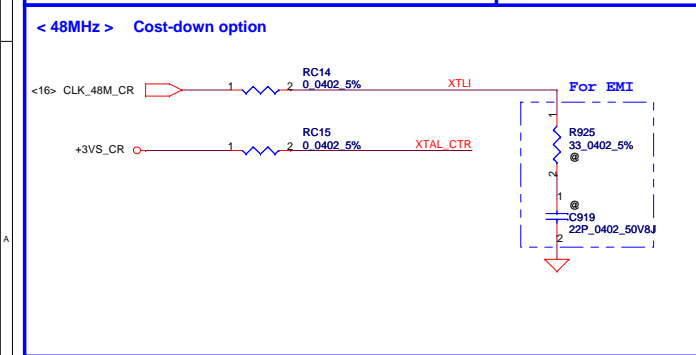
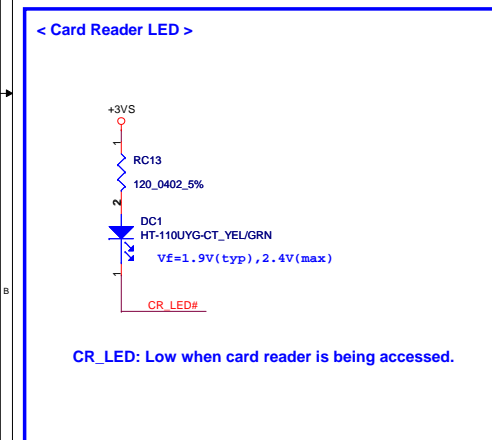
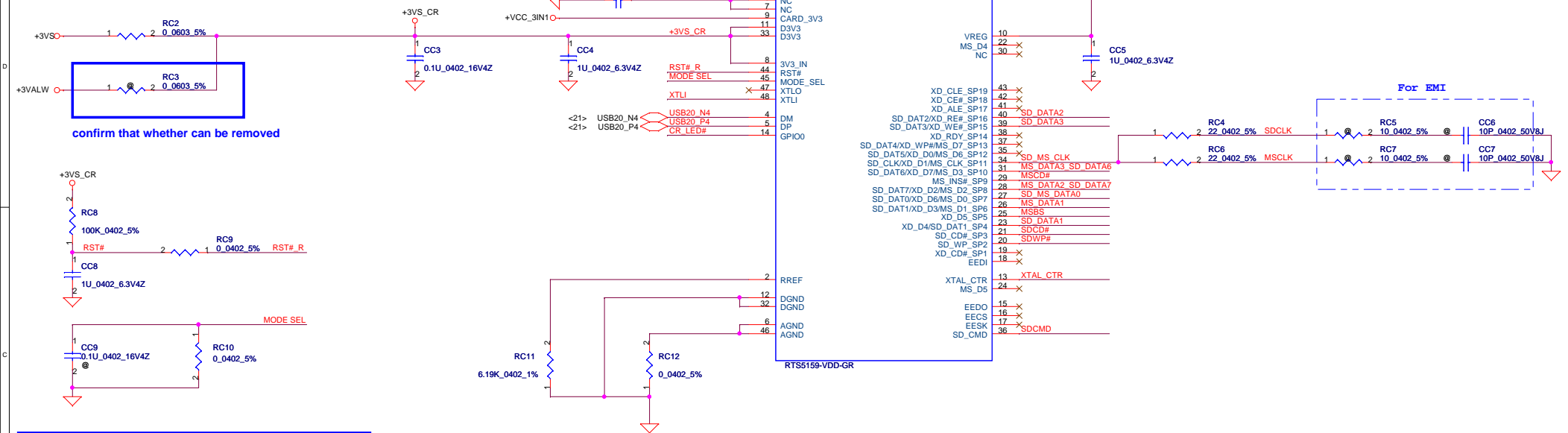
< PCB >

PCB



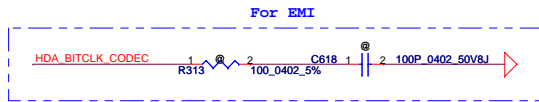
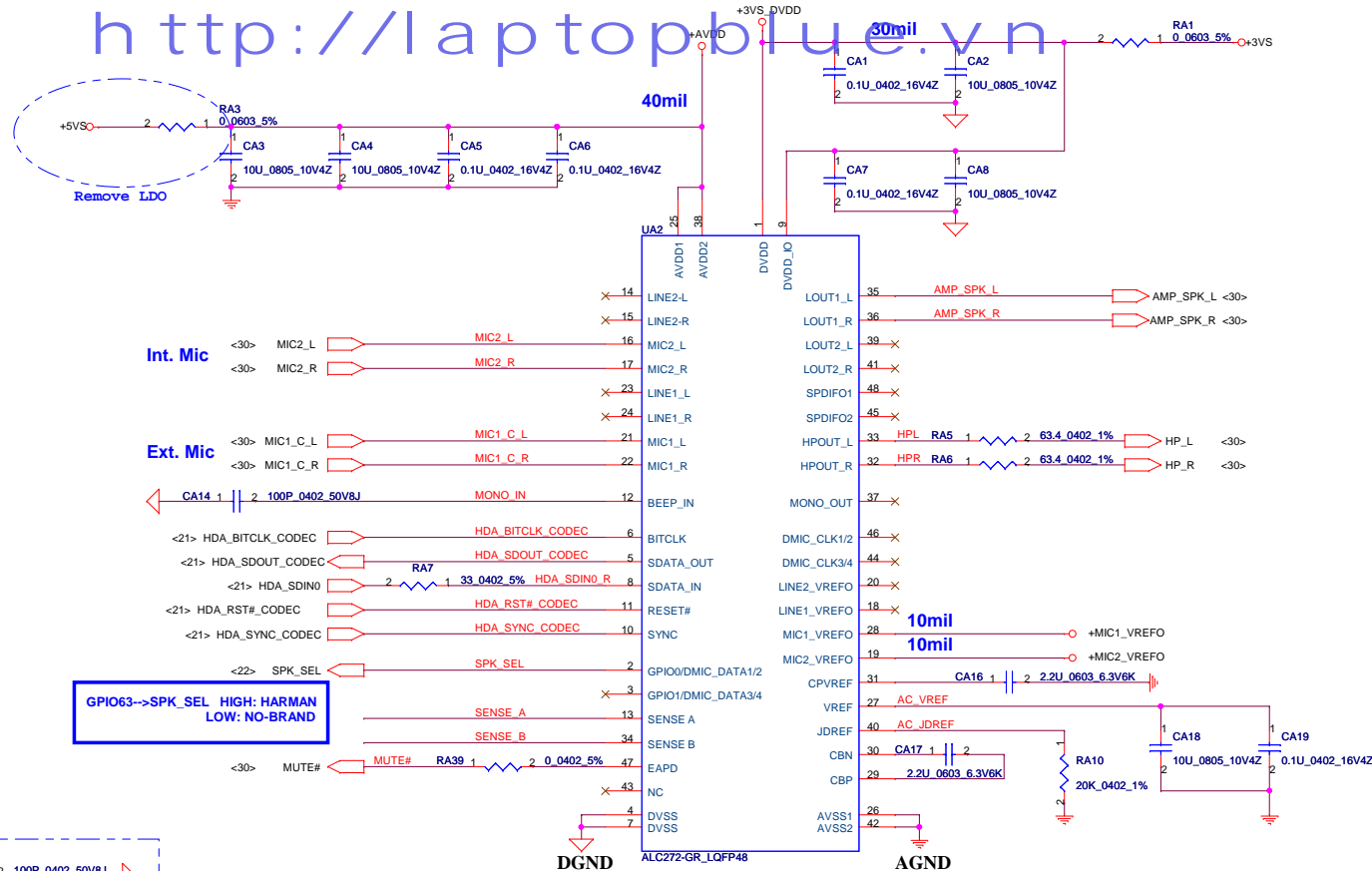
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								LA-5831P			
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								Date: Wednesday, August 12, 2009			
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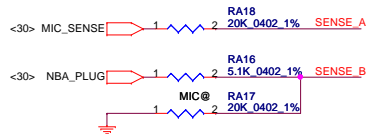


R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

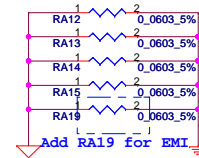
Security Classification	Compal Secret Data			Compal Electronics, Inc. RTS5159 Card Reader		
Issued Date	2009-02-12	Deciphered Date	2009-02-12	Title	RTS5159 Card Reader	
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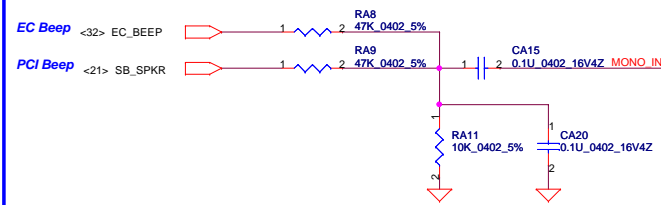
< SENSE_A & SENSE_B, place close to chip >



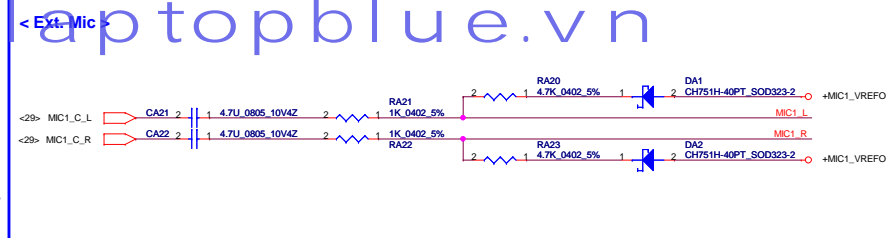
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out



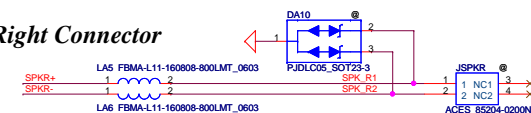
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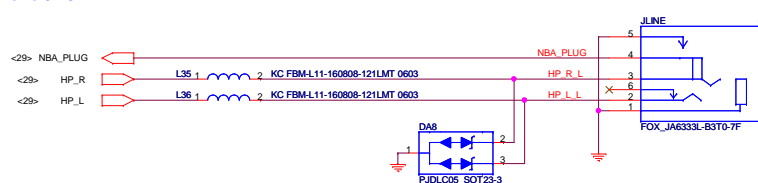
http://aptopblue.vn

[illegible]

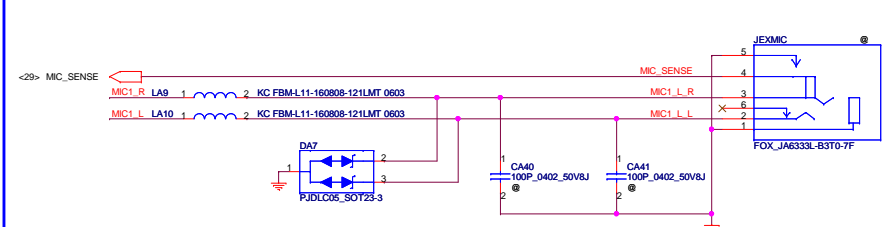
Left Connector



< Ext.MIC/LINE IN JACK >



< Ext.MIC/LINE IN JACK >

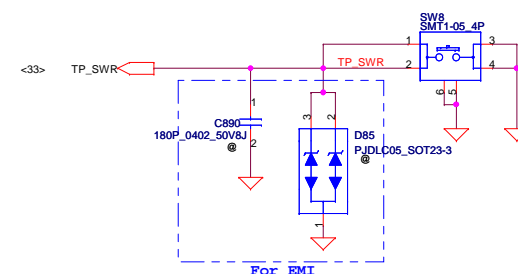
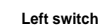


The schematic diagram illustrates the encoder interface circuit. It features a +3V5 supply connected to a network of resistors (RA32, RA33, RA34, RA35, RA36, RA37, RA38) and capacitors (CA35, CA36, CA37, CA38). A switch SW2 is connected to a common terminal (COM) and two terminals (A, B). A switch SW_XRE094_3P is also present. The circuit includes a 74LVC1G14GW_SOT363 5V inverter (U4A) and a 74LCK74M 5V Schmitt trigger (U4B). The output of the circuit is connected to an encoder with pins for CD1#, D1#, CP1#, SD1#, Q1#, Q1#, GND, ENCODER_DIR, and ENCODER_PUL.

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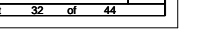
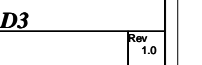
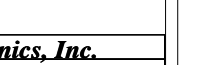
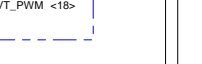
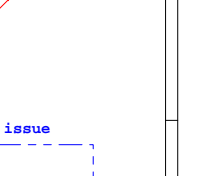
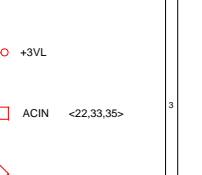
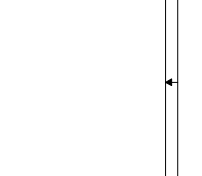
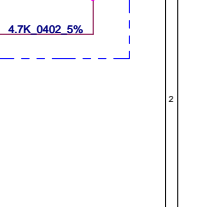
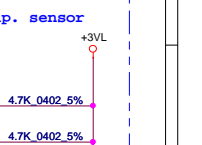
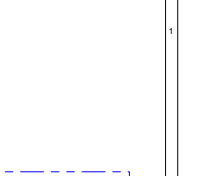
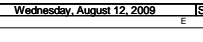
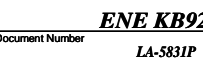
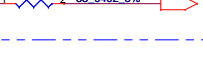
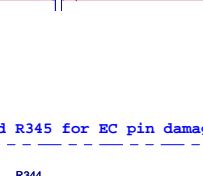
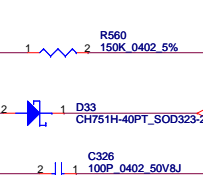
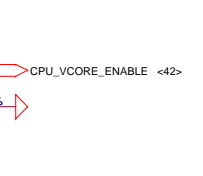
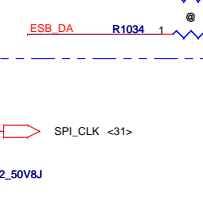
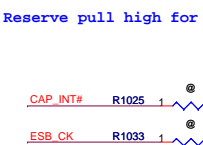
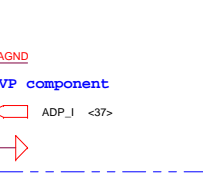
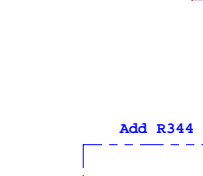
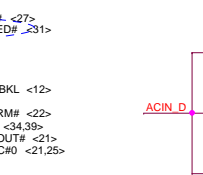
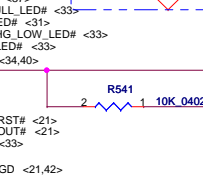
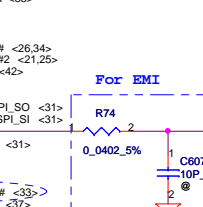
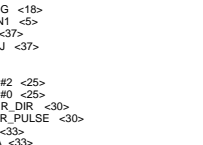
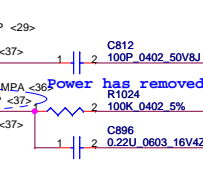
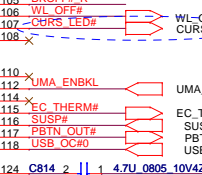
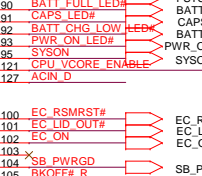
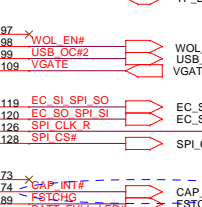
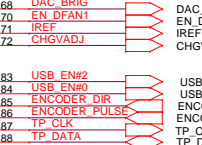
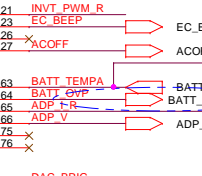
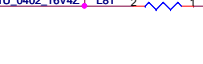
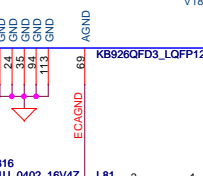
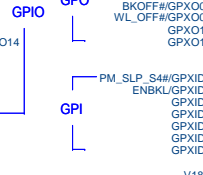
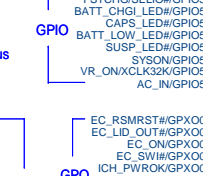
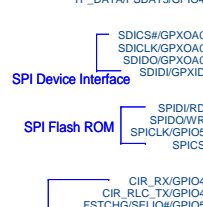
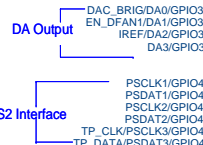
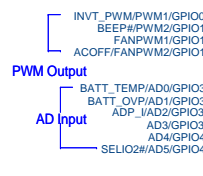
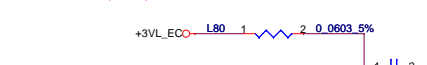
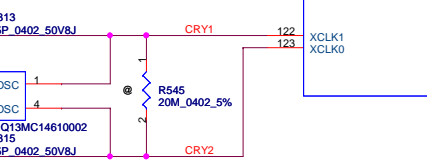
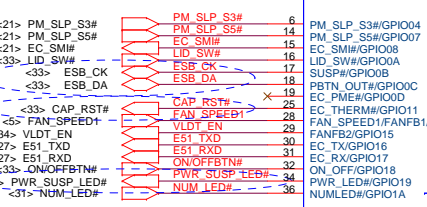
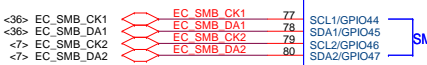
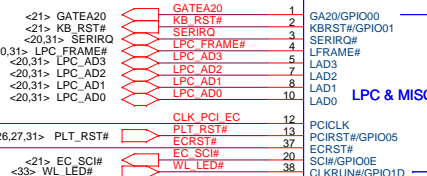
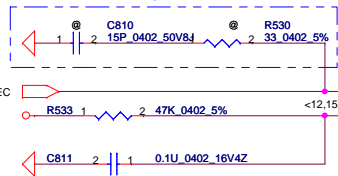


For EMI



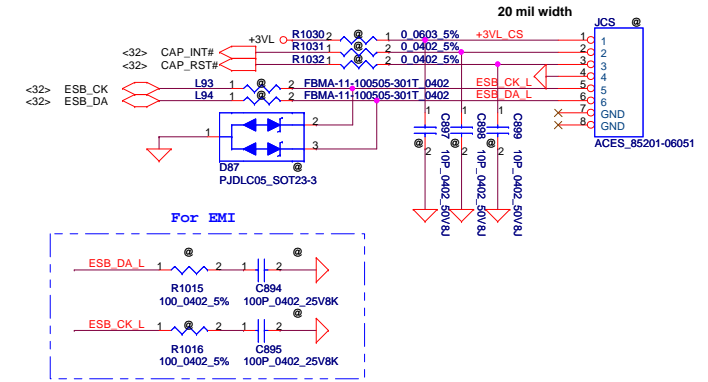
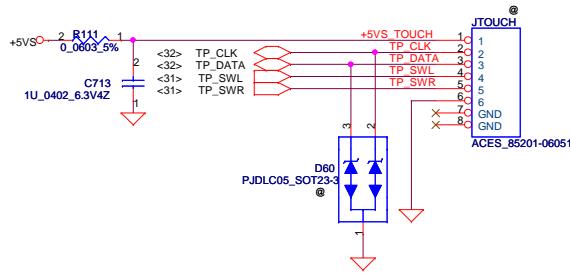
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Issued Date		2009-02-12	Deciphered Date	2009-02-12		Title
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				Document Number		LA-5831P
				Date: Wednesday, August 12, 2009 Sheet 31 of 44		

Reserve for EMI request



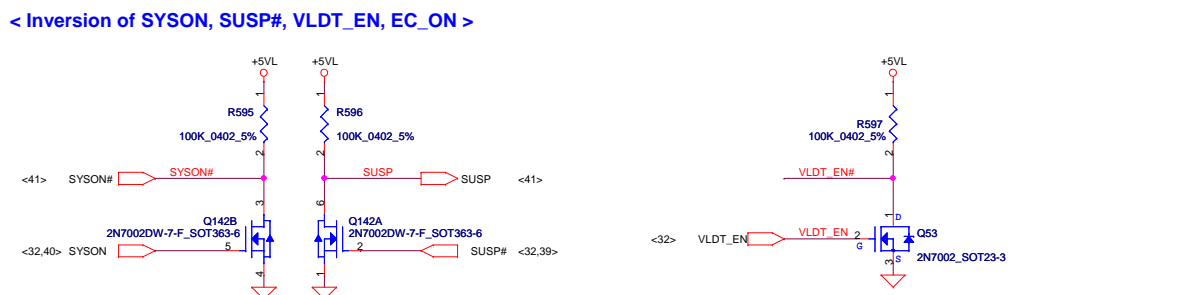
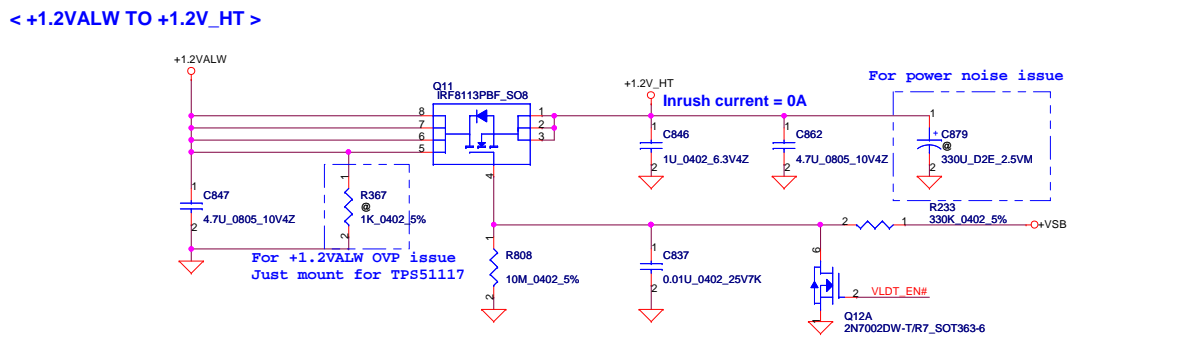
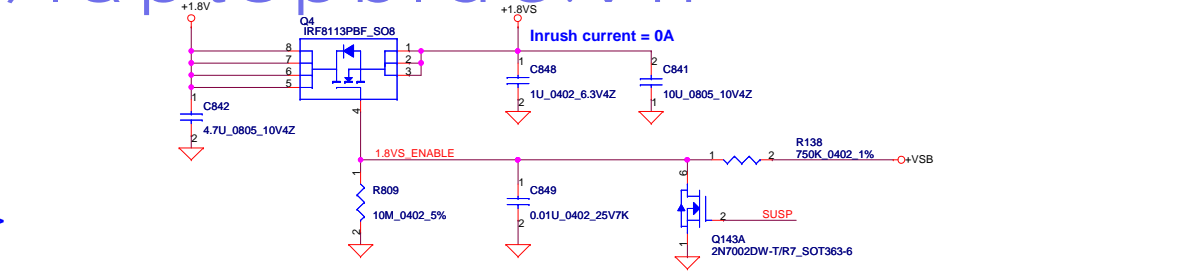
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Issued Date	2009-02-12	Deciphered Date	2009-02-12	ENE KB926 D3	
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Touch Pad Connector



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				Date: Wednesday, August 12, 2009	Sheet 33 of 44

> < +1.8V TO +1.8VS >

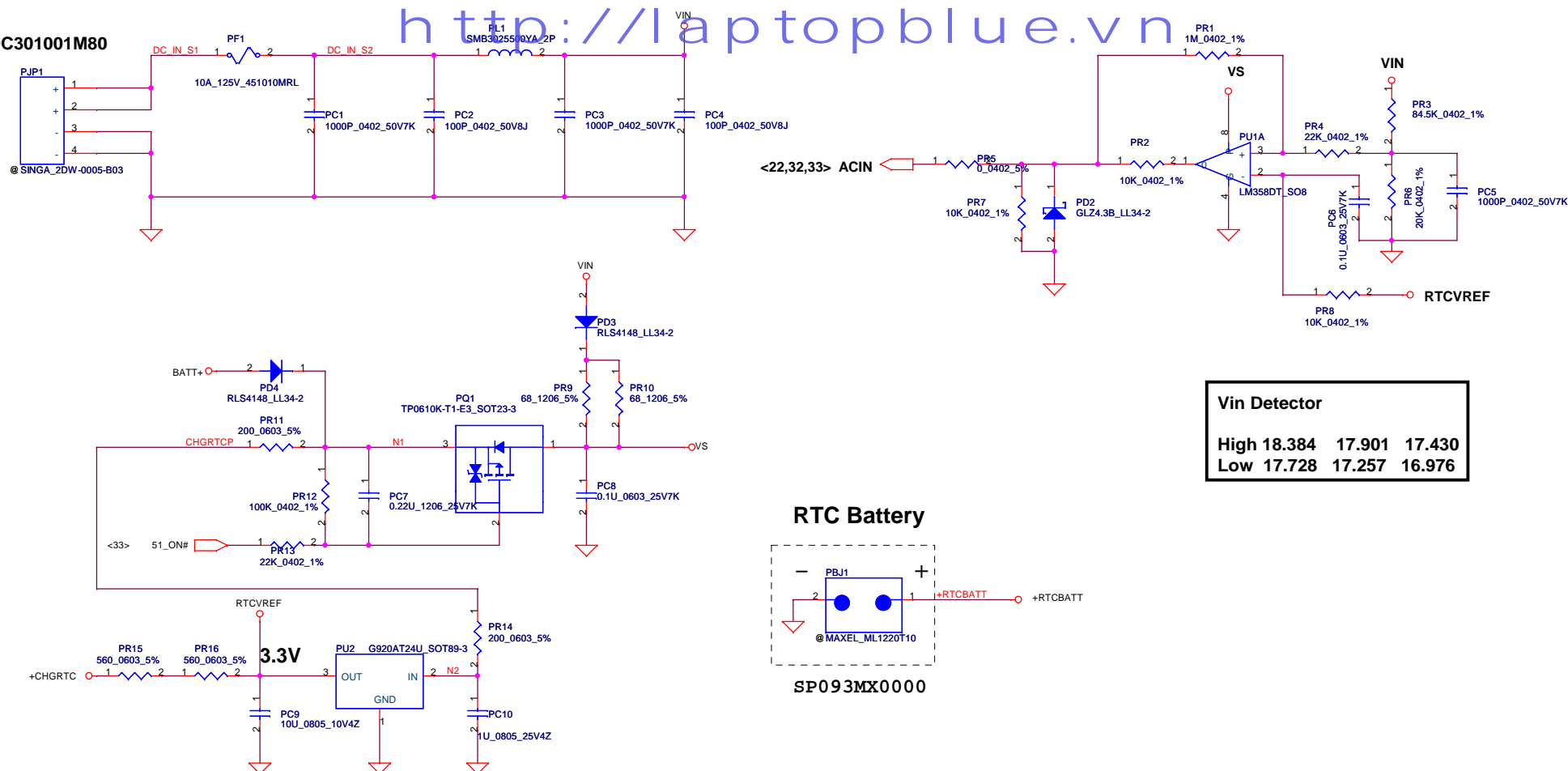


The schematic diagram illustrates the power supply section, featuring eight voltage regulators. Each regulator is composed of a resistor (R239 to R294) and a MOSFET (Q144A to Q52) connected to a specific input voltage and output voltage. The regulators are labeled with their respective input and output voltages and the MOSFET model.

Regulator	Input Voltage	Output Voltage	MOSFET Model
Q144A	+5VS	+1.8VS	2N7002DW-7-F_SOT363-6
Q48	+1.8VS	+1.2V_HT	2N7002_SOT23-3
Q12B	+1.2V_HT	+1.8V	2N7002DW-T/R7_SOT363-6
Q143B	+1.8V	+3VS	2N7002DW-T/R7_SOT363-6
Q144B	+3VS	+0.9V	2N7002DW-7-F_SOT363-6
Q49	+0.9V	+1.5VS	2N7002_SOT23-3
Q50	+1.5VS	+1.1VS	2N7002_SOT23-3
Q52	+1.1VS	+1.1VS	2N7002_SOT23-3

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				LA-5831P	
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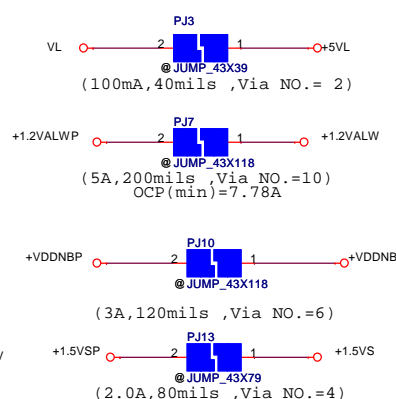
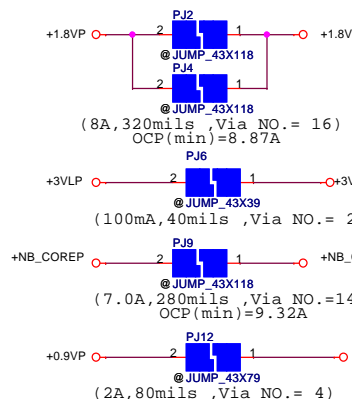
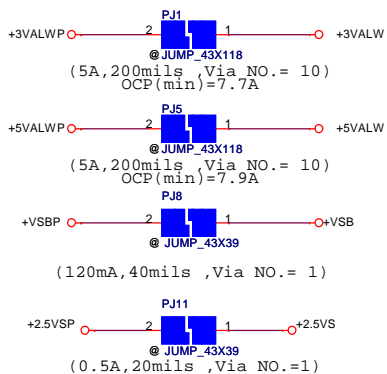
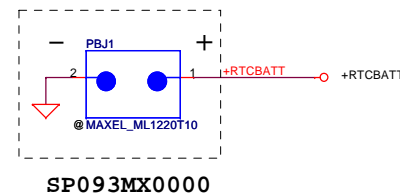
DC301001M80



Vin Detector

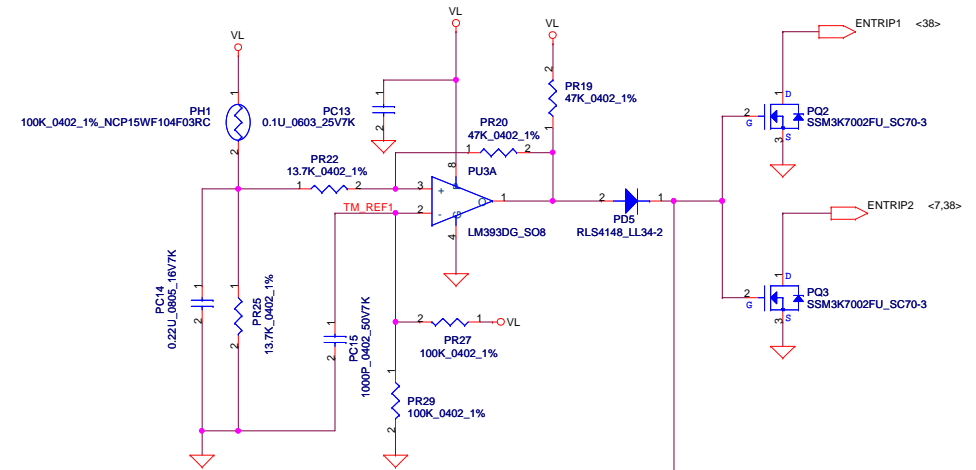
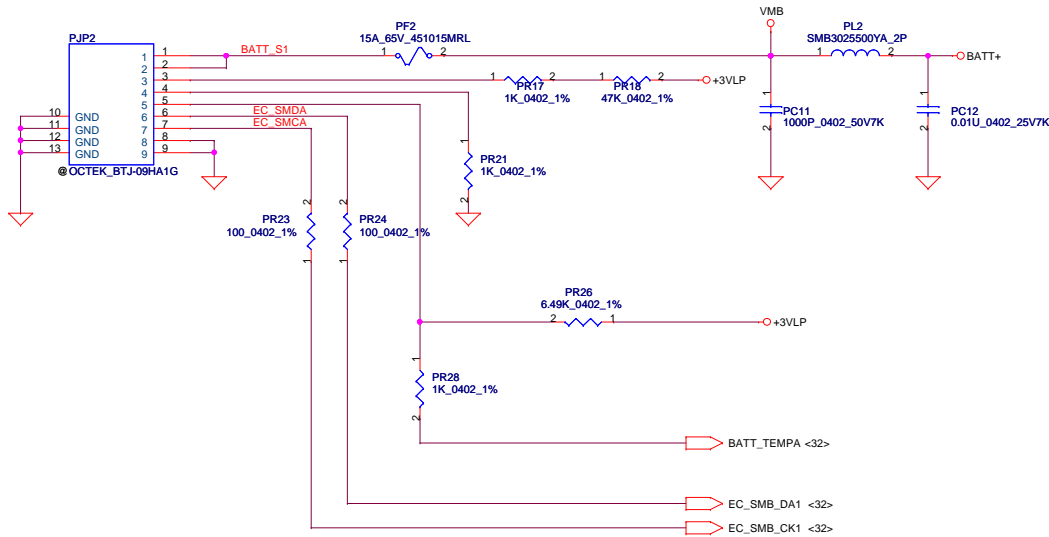
High	18.384	17.901	17.430
Low	17.728	17.257	16.976

RTC Battery

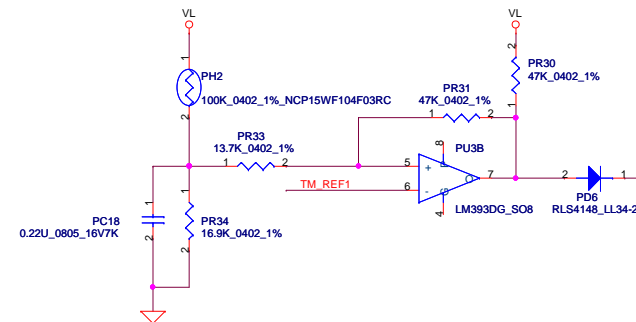
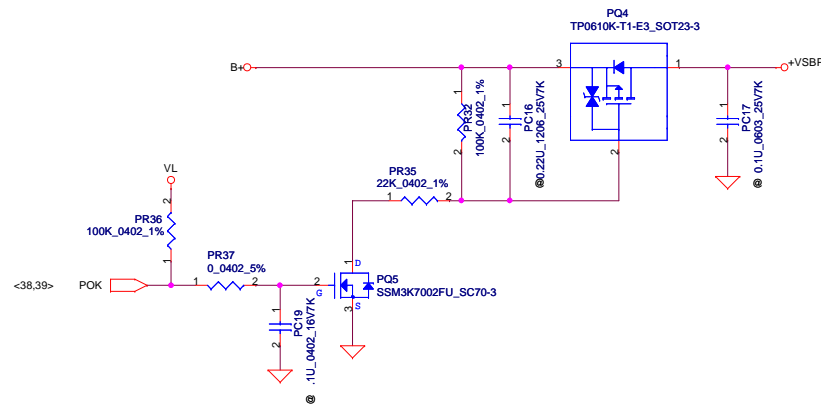


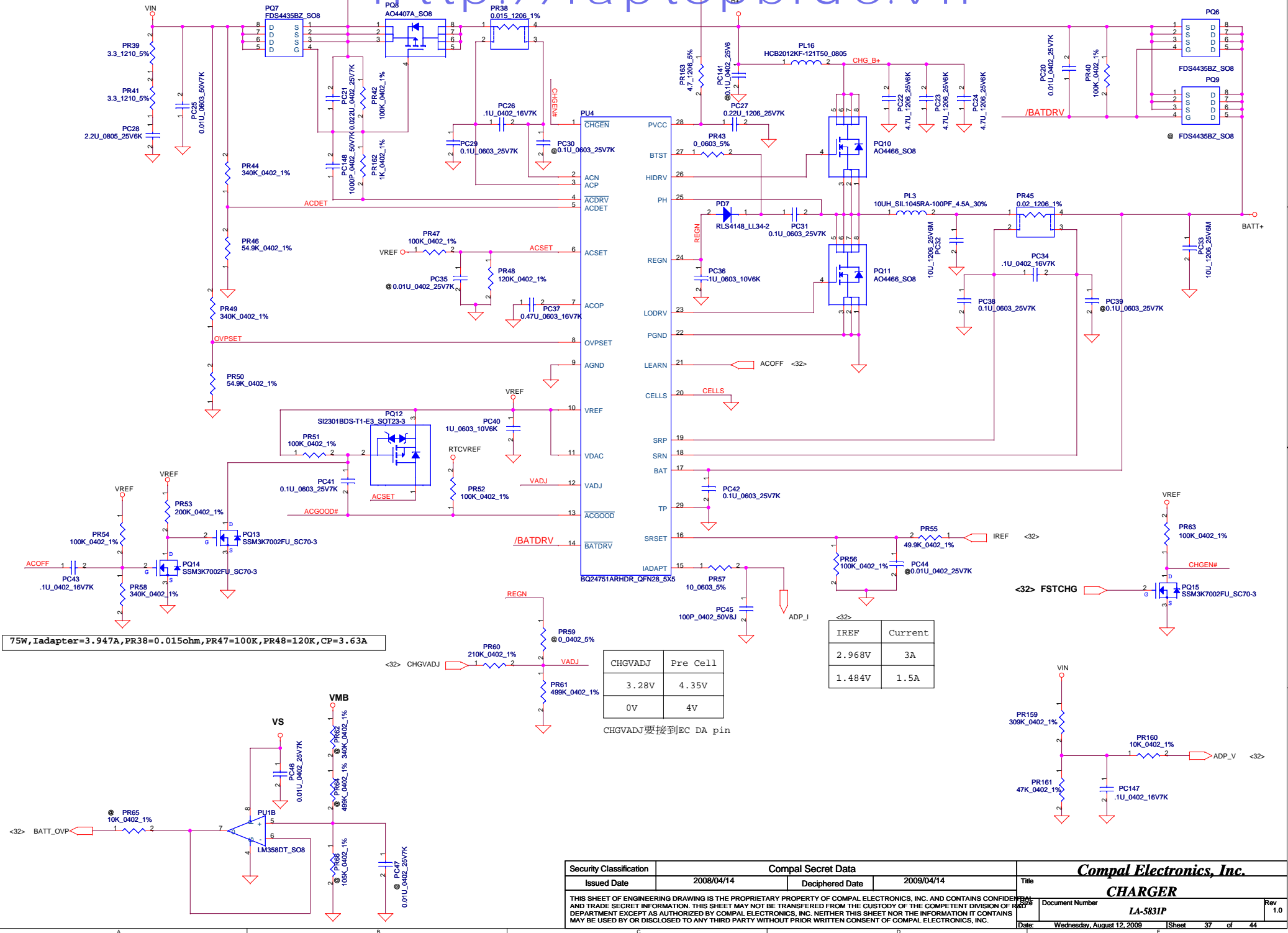
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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								Rev			
								1.0			
								Date: Wednesday, August 12, 2009			
								Sheet 35 of 44			

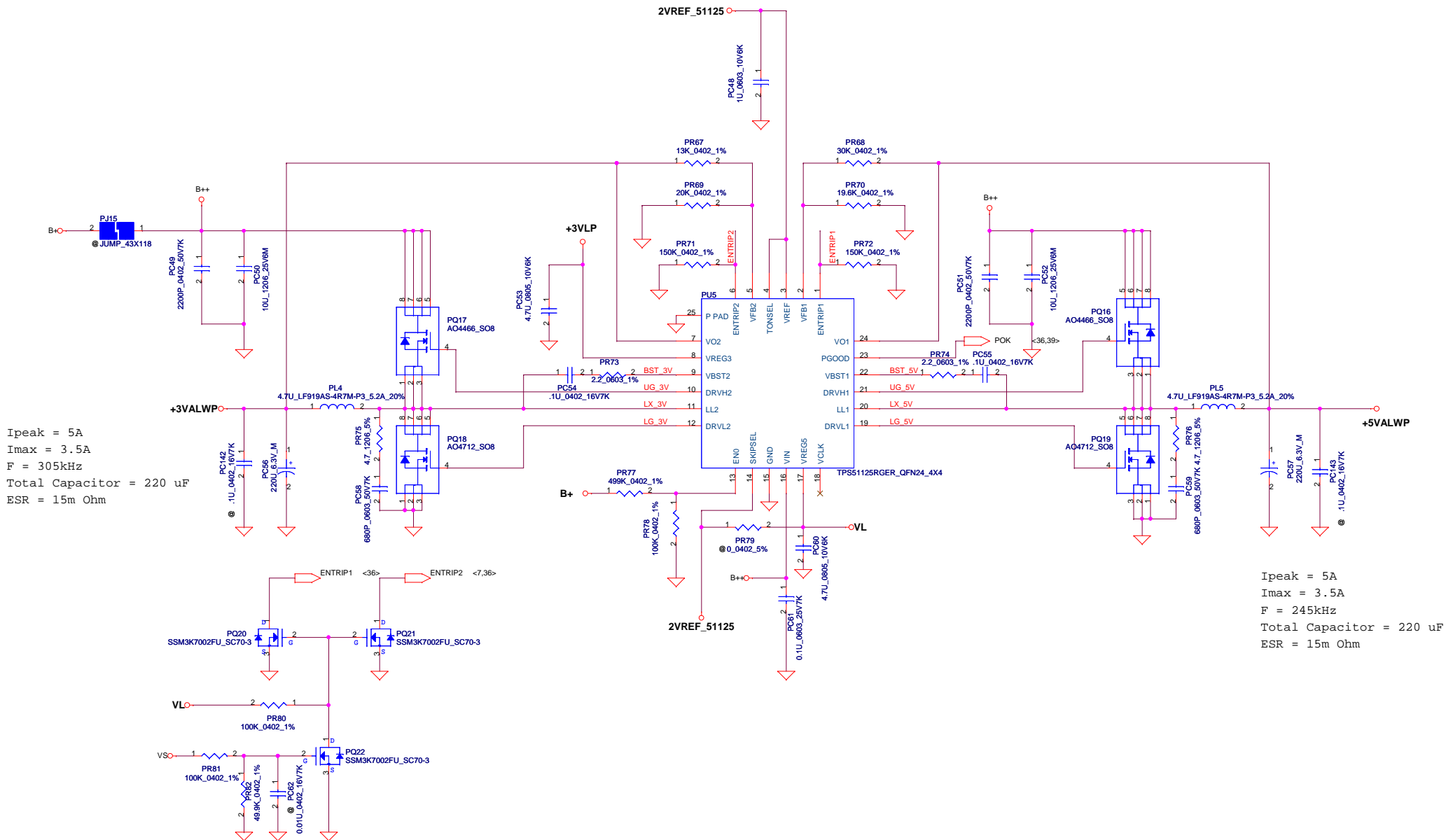
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



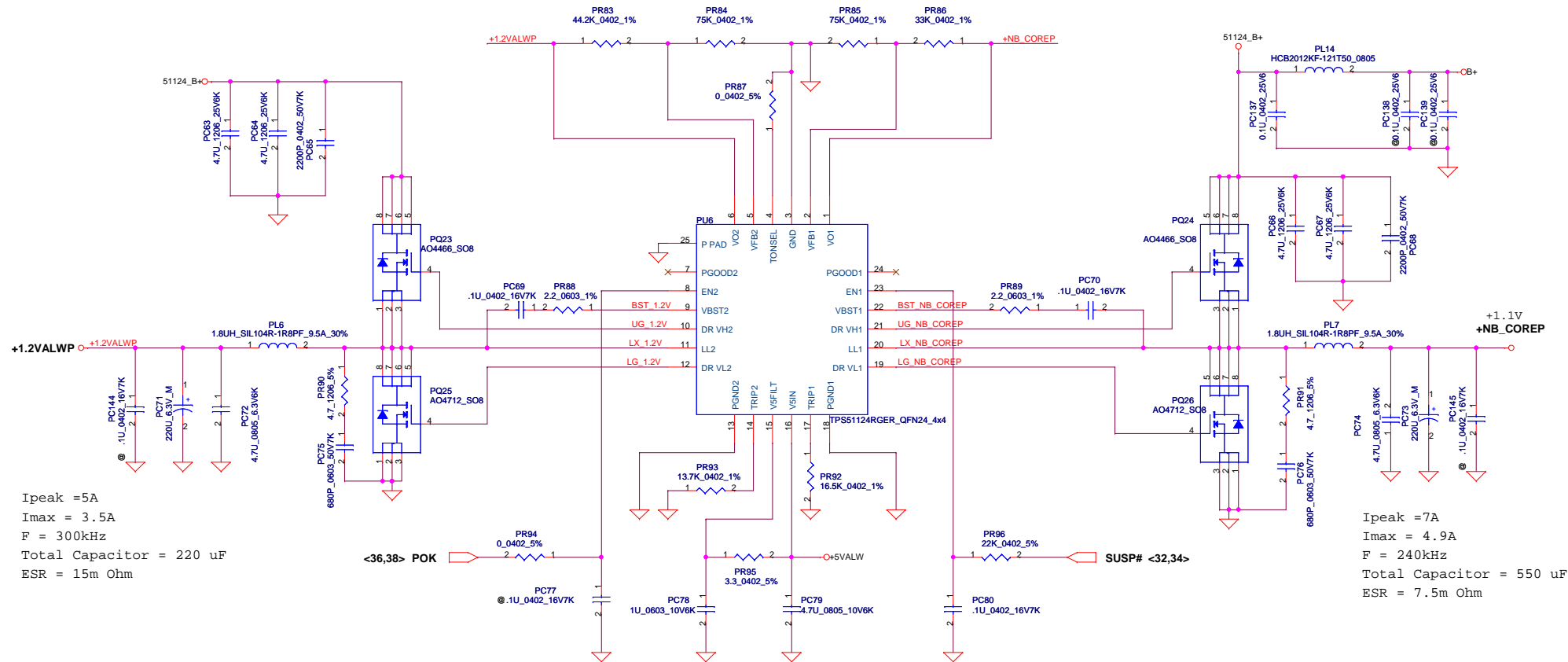
PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C



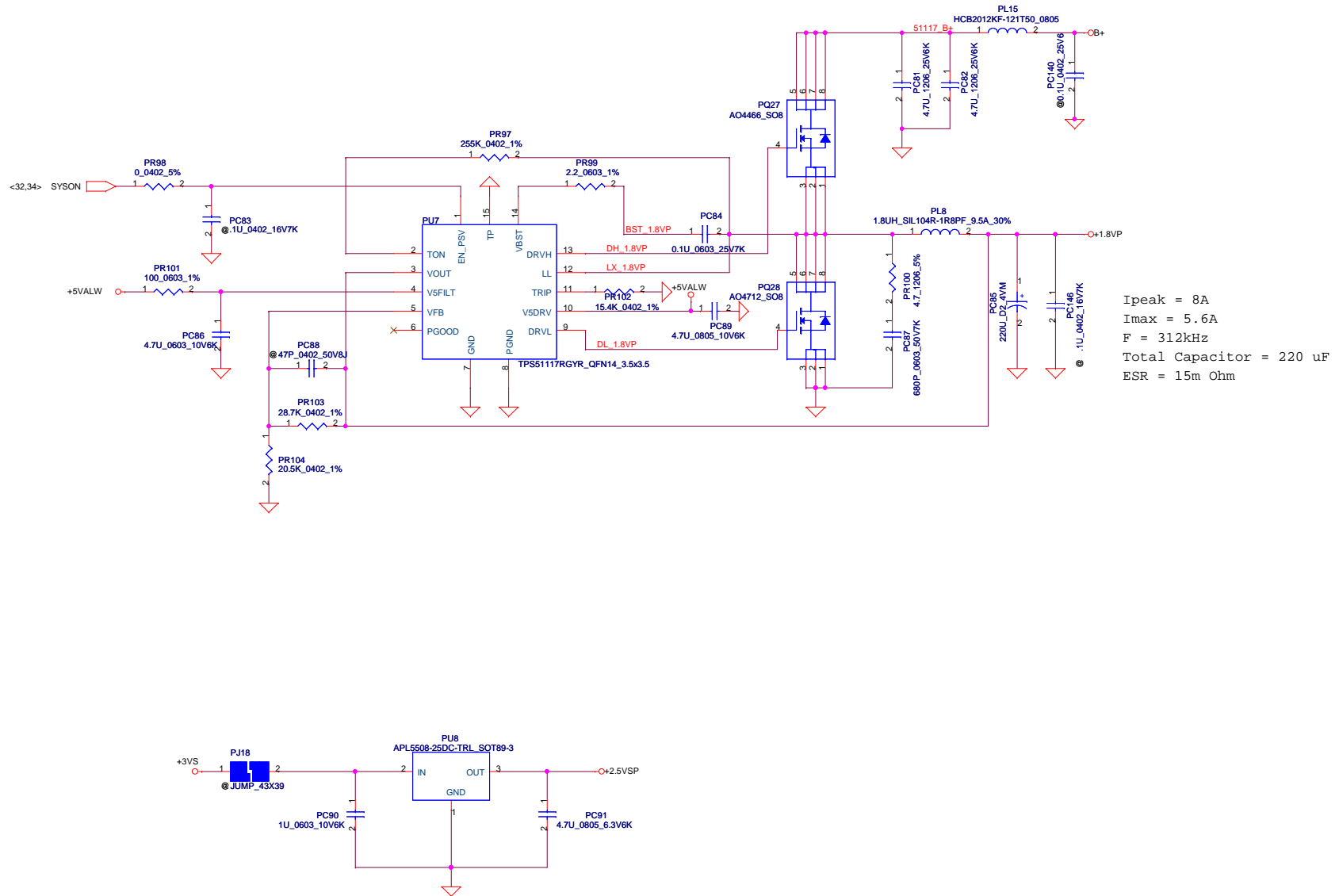




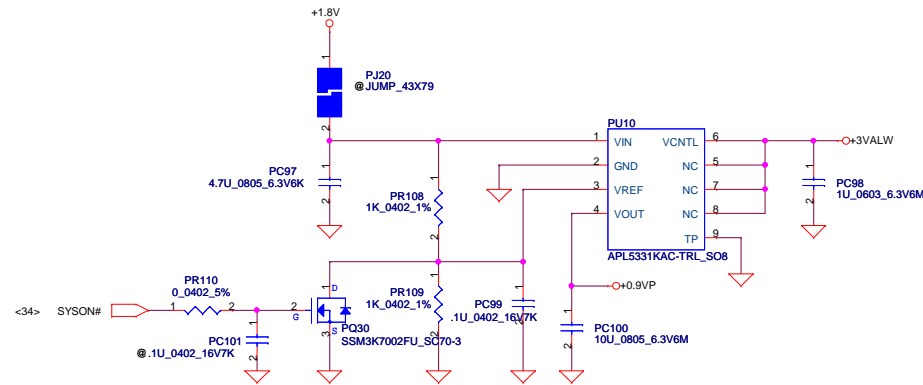
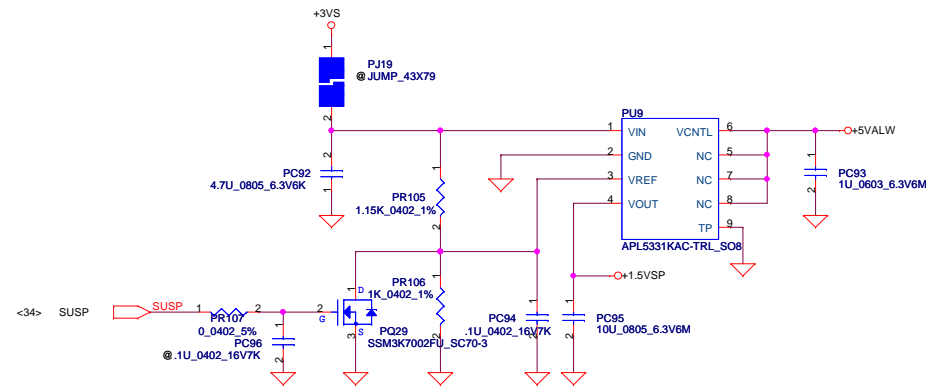
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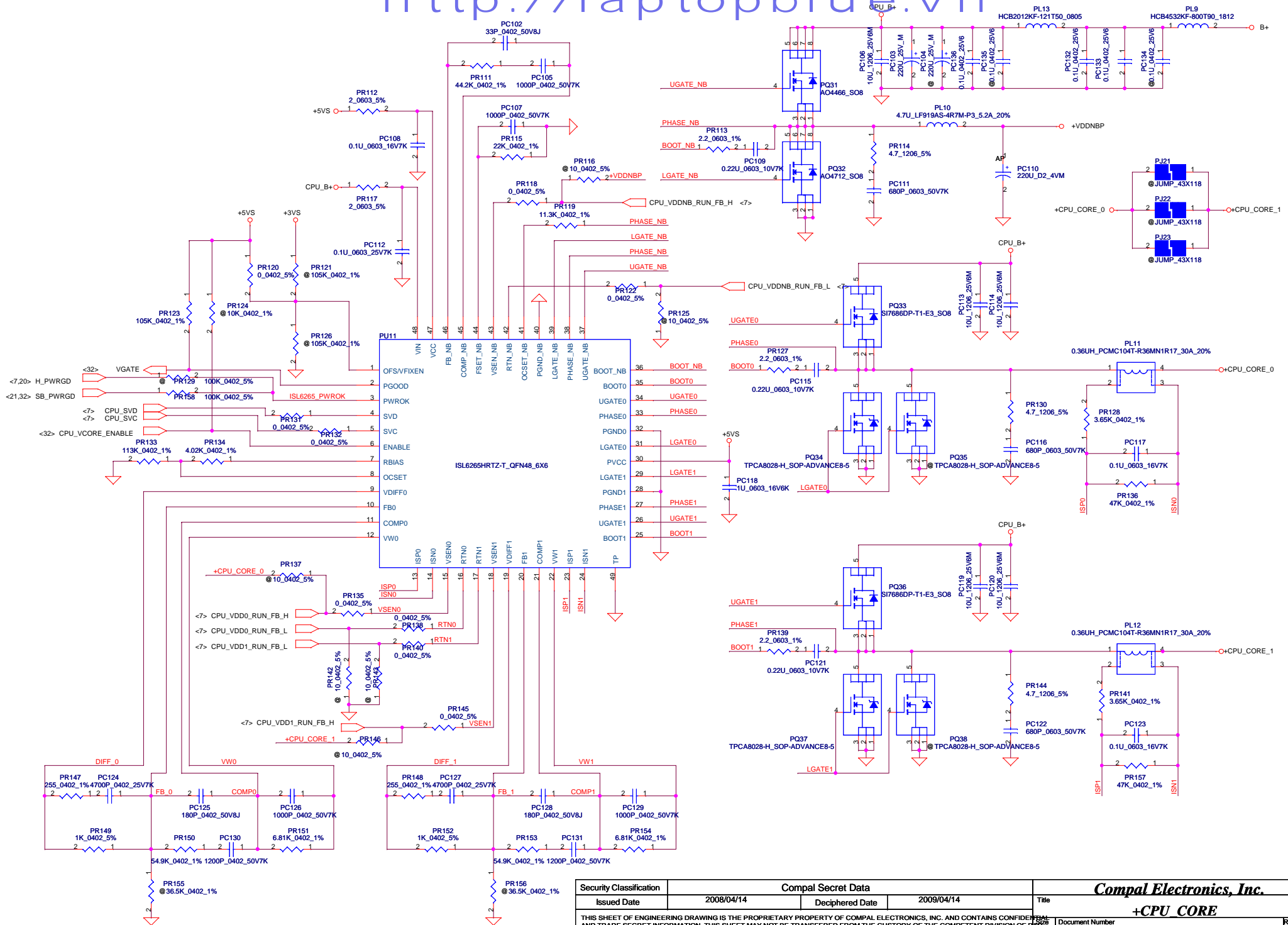
Security Classification		Compal Secret Data		Title	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	NB COREP/1.2VALWP	
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								LA-5831P			
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Version Change List (P. I. R. List)for Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
35-43	PVT		2009/07/20	Release			
39-40	Pre-MP	Change PL6 ,PL7 ,PL8	2009/07/30	POWER		Change PL6,PL7,PL8 footprint	
38	Pre-MP	Change PC56	2009/07/30	POWER		change to common circuit.	
36	Pre-MP	Change PH1 ,PH2	2009/08/4	POWER		change to common circuit.	
37	Pre-MP	Change PR38 ,PR45	2009/08/4	POWER		change to common circuit.	

http://laptopblue.vn

HW4 Product Improvement Record (P.I.R.)

NBWAE LA-5831P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 1.0
GERBER-OUT DATE: 2009/08/07

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	7/21	25	Change JUSBB footprint back to E-T_6905-E12N-00R_12P	USB/B pin define reverse
2	7/27	25	Add D11	For ESD
3	7/27	9	Add C120-C123	For EMI
4	7/27	32	Add R344 and R345	For EC pin damage issue
5	7/30	26	Add R97, R98 and R105	Reserve bead for EMI
6	8/6	18	Add C707, C708 and C709	For EMI
7	8/6	30	Add LA11 and LA12	For EMI
8	8/6	32	Add R74 and C607	For EMI
9	8/6	31	Delete R518 and C606	For EMI
10	8/6	7	Add C124	For EMI