

Compal confidential

Liverpool/Sunderland 10AT

NSWAE/NTWAE LA-5332P Schematics Document

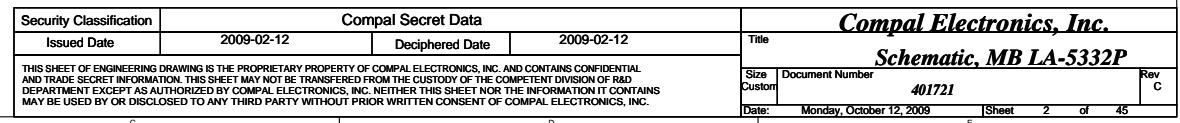
Mobile AMD S1G3/
RS880M & RS880MC / SB710

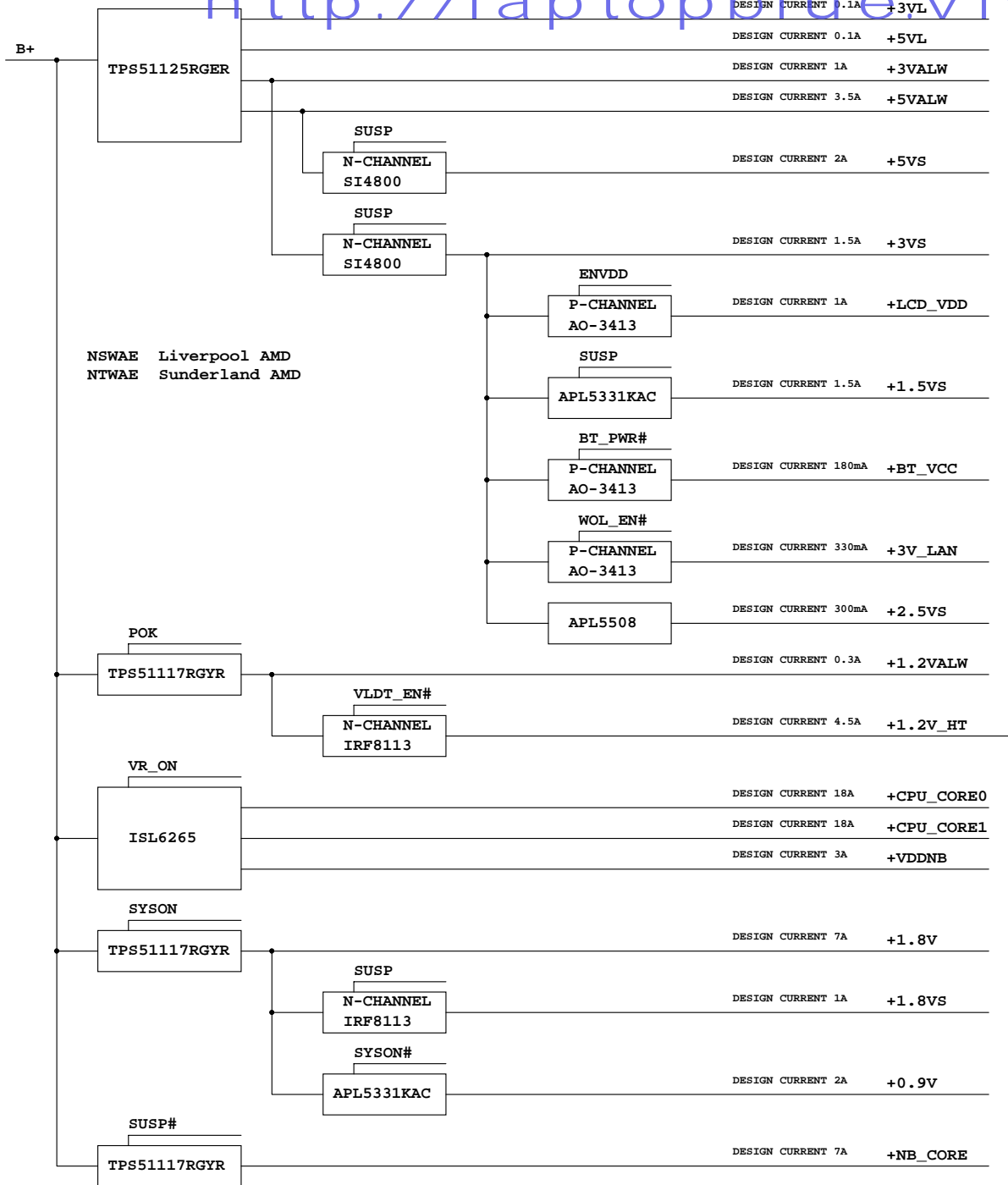
2009-11-24 Rev. 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2009-02-12	Deciphered Date	2009-02-12	Title Schematic, MB LA-5332P		
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Tigris Platform





O : ON
X : OFF

State \ power plane	+B +3VL +5VL +RTCVCC	+5VALW +3VALW +1.2VALW +3V_LAN	+1.8V +0.9V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_NB +CPU_CORE_0 +CPU_CORE_1
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

Device	HEX	Address
Smart Battery	16H	0001 011X b
HDMI-CEC	34H	0011 010X b
EC KB926D3		

Device	HEX	Address
ADI1032-1 CPU	98H	1001 100X b
ADI1032-2 VGA	9AH	1001 101X b
EC KB926D3		

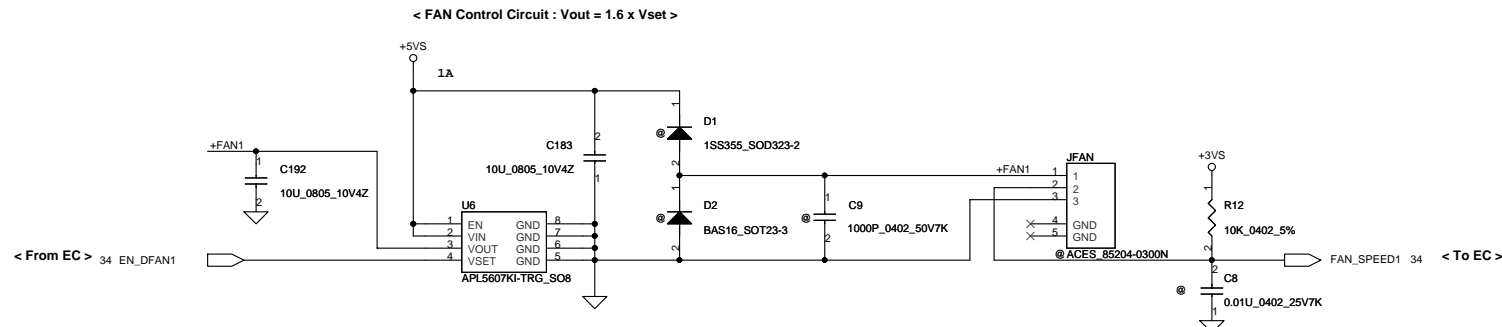
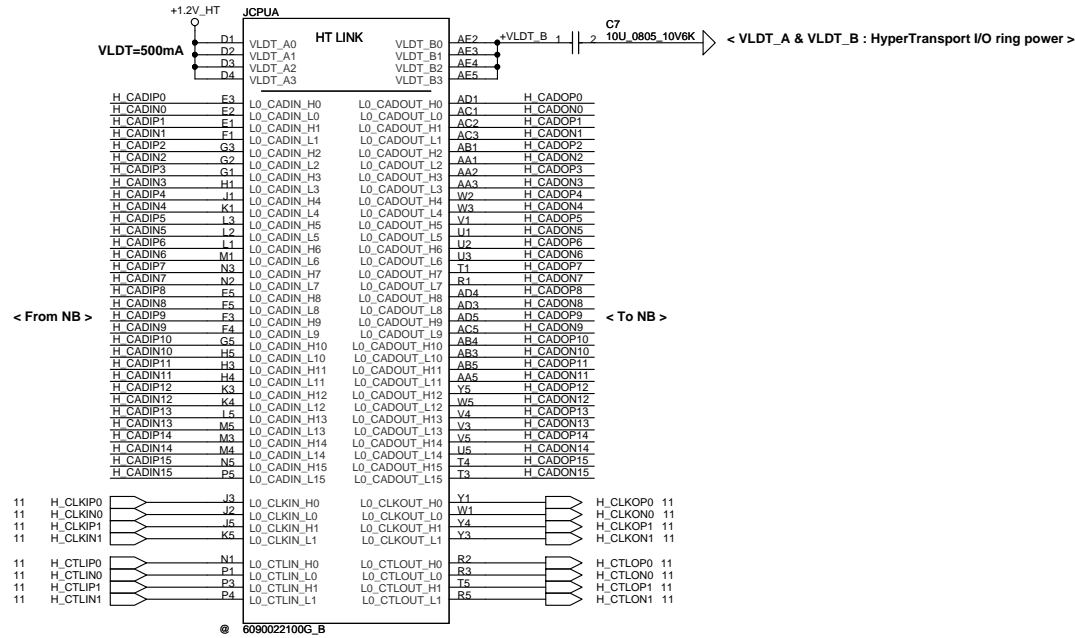
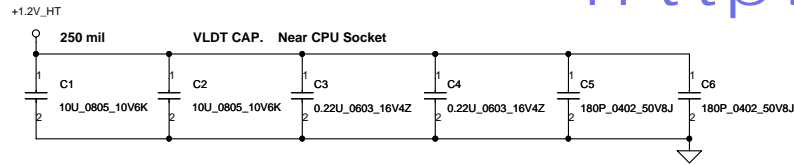
Platform	CPU	NB	VGA	SB	Comment
	S1G3	RS880MC	NA	SB710	
	S1G3	RS880M	NA	SB710	

Function	Express card / PCMCIA	BLUE TOOTH	RJ11	SSD	SATA ODD		WiFi	HDMI	G- sensor		3 in 1 card reader	FingerPrinter	CAMERA & MIC	
Description	(E / A)	(B)	(R)				(H)	(Y)	(S)		(C)	(F)	(X)	
Explain					16"	17"	Half - size		First	Second	RTS5159		CAMERA	MIC
BTO	EXPCARD@ / PCMCIA@	BT@	MDC@	SSD@	16inch@	17inch@	WLAN@	H@	G@ + G_1st@	G@ + G_2nd@	CARD@	FP@	CAM@	MIC@

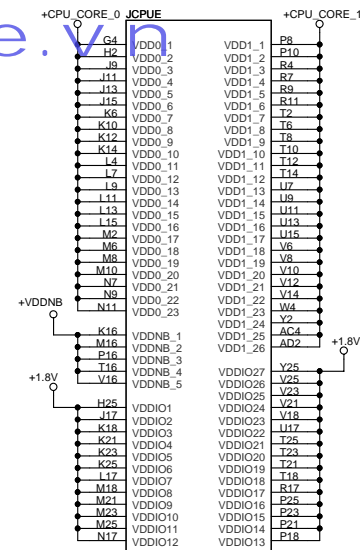
Function	DC-IN		Side port		
Description			(L)		
Explain					
BTO	16inch_45 @	17inch_45 @	SIDE@	NSIDE@	

[illegible]

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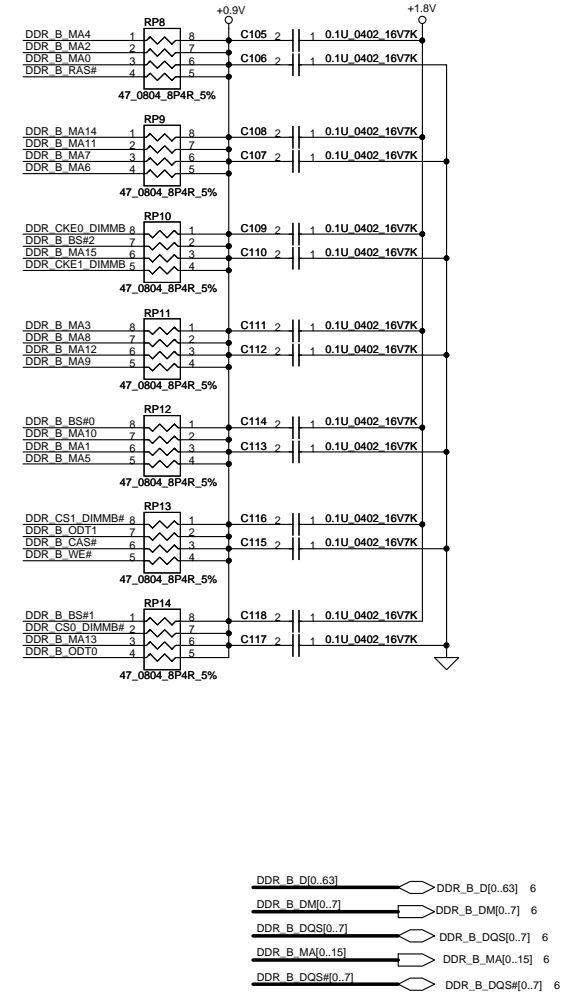
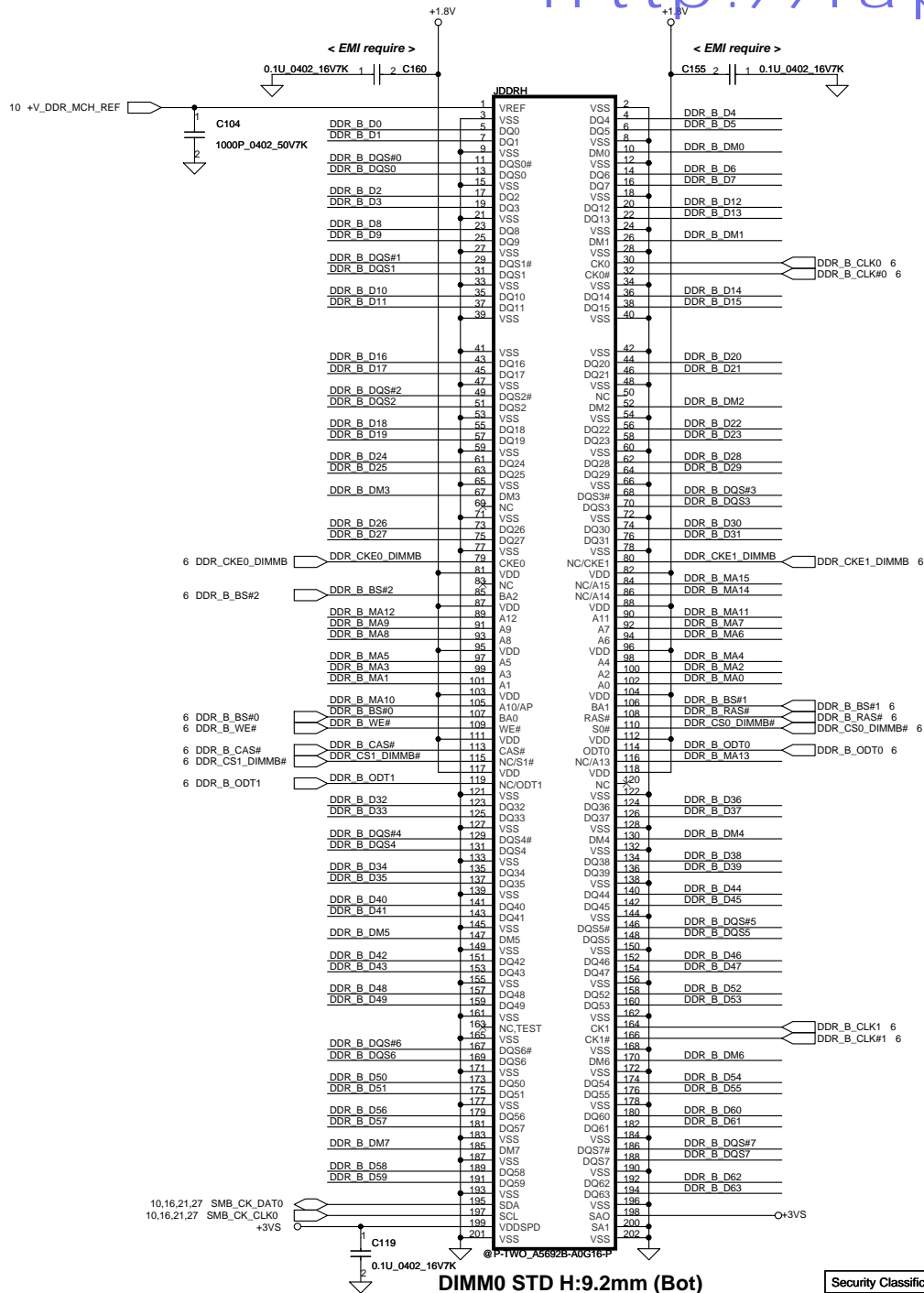
[illegible]

JCPUF			
AA4	VSS1	VSS66	J6
AA11	VSS2	VSS67	J8
AA13	VSS3	VSS68	J10
AA15	VSS4	VSS69	J12
AA17	VSS5	VSS70	J14
AA19	VSS6	VSS71	J16
AB2	VSS7	VSS72	J18
AB7	VSS8	VSS73	K2
AB9	VSS9	VSS74	K7
AB23	VSS10	VSS75	K9
AB25	VSS11	VSS76	K11
AC11	VSS12	VSS77	K13
AC13	VSS13	VSS78	K15
AC15	VSS14	VSS79	K17
AC17	VSS15	VSS80	L8
AC19	VSS16	VSS81	L10
AC21	VSS17	VSS82	L12
AD6	VSS18	VSS83	L14
AD8	VSS19	VSS84	L16
AD25	VSS20	VSS85	L18
AE11	VSS21	VSS86	M7
AE13	VSS22	VSS87	M9
AE15	VSS23	VSS88	AC17
AE17	VSS24	VSS89	N6
AE19	VSS25	VSS90	N8
AE21	VSS26	VSS91	N10
AE23	VSS27	VSS92	N14
B4	VSS28	VSS93	N16
B6	VSS29	VSS94	N18
B8	VSS30	VSS95	P2
B11	VSS31	VSS96	P7
B9	VSS32	VSS97	P9
B13	VSS33	VSS98	P11
B15	VSS34	VSS99	P13
R17	VSS35	VSS100	R8
R19	VSS36	VSS101	R10
B21	VSS37	VSS102	R16
B23	VSS38	VSS103	R18
B25	VSS39	VSS104	T7
D6	VSS40	VSS105	T9
D8	VSS41	VSS106	T9
D9	VSS42	VSS107	T11
D11	VSS43	VSS108	T13
D13	VSS44	VSS109	T15
D15	VSS45	VSS110	T17
D17	VSS46	VSS111	U4
D19	VSS47	VSS112	U8
D21	VSS48	VSS113	U10
D23	VSS49	VSS114	U10
D25	VSS50	VSS115	U12
F4	VSS51	VSS116	U14
F15	VSS52	VSS117	U16
F11	VSS53	VSS118	U18
F13	VSS54	VSS119	V7
F17	VSS55	VSS120	V9
F19	VSS56	VSS121	V11
F21	VSS57	VSS122	V13
F23	VSS58	VSS123	V15
F25	VSS59	VSS124	V17
H9	VSS60	VSS125	V19
H7	VSS61	VSS126	W6
H21	VSS62	VSS127	Y23
H23	VSS63	VSS128	N6
J4	VSS64	VSS129	
	VSS65		

Figure 1: Recommended B2 size capacitor placement. The figure shows five circuit diagrams illustrating the placement of capacitors between the CPU socket and DIMM0. Each diagram shows a power rail (1.8V or +1.8V) connected to a series of capacitors (C46-C51, C55-C58, C60-C61, C62-C65, C74-C78) connected to a common ground. The capacitors are labeled with their values: 22U_0805_6.3V6M, 0.22U_0603_16V4Z, 180P_0402_50V8J, 0.01U_0402_25V7K, and 220U_B2_4VM_R45M. The diagrams are labeled 'Under CPU Socket', 'Between CPU Socket and DIMM', and 'Between CPU Socket and DIMM'. A note indicates that 180PF Qr'y follow the distance between CPU socket and DIMM0, <2.5inch>. A final note says 'Change to B2 size'.

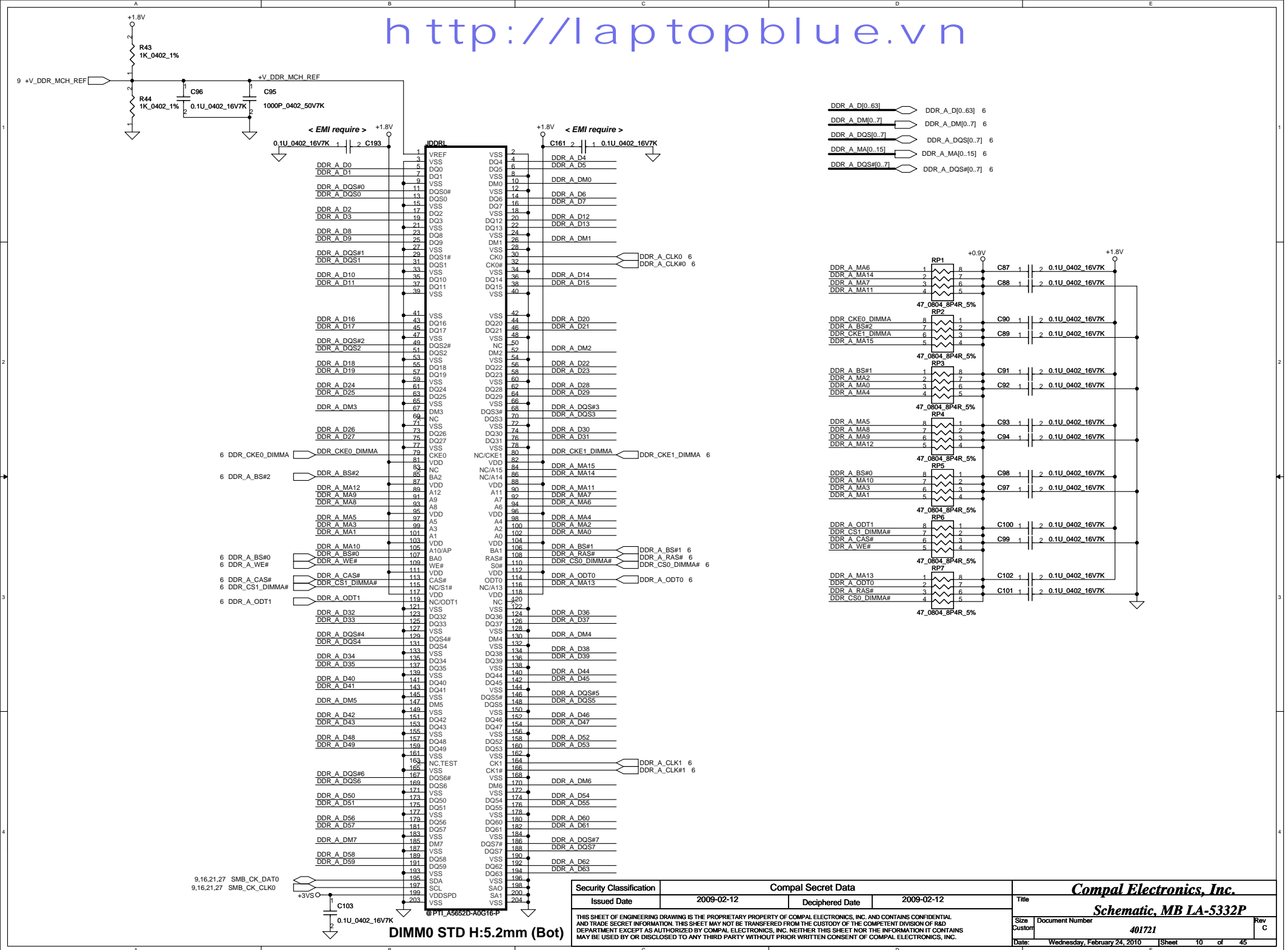
Figure 1: Schematic diagram of the power supply circuit for the CPU socket. The diagram shows two rows of components connected to a +0.9V supply. The top row, labeled "Near CPU Socket Right side", contains capacitors C66 through C73. The bottom row, labeled "Near CPU Socket Left side", contains capacitors C79 through C86. A legend on the right indicates: 1. Near Power Supply, 2. Change to B2 size, and shows capacitor C59 with value 220U_B2_4VM_R45M.

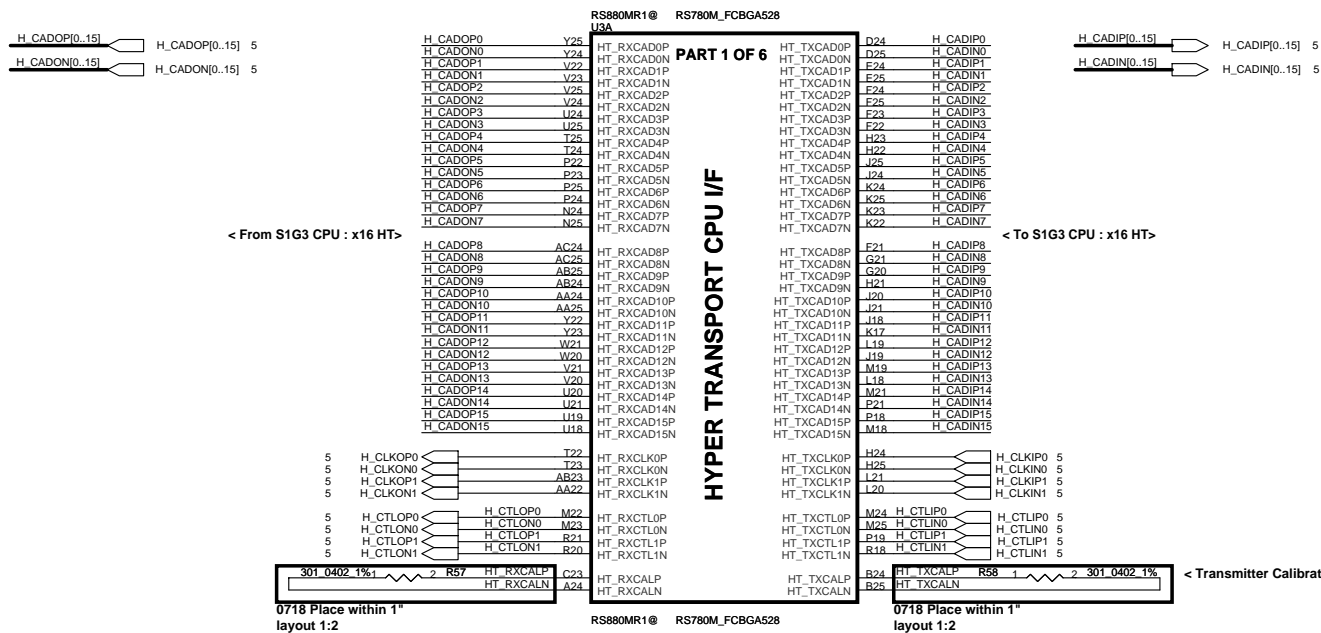
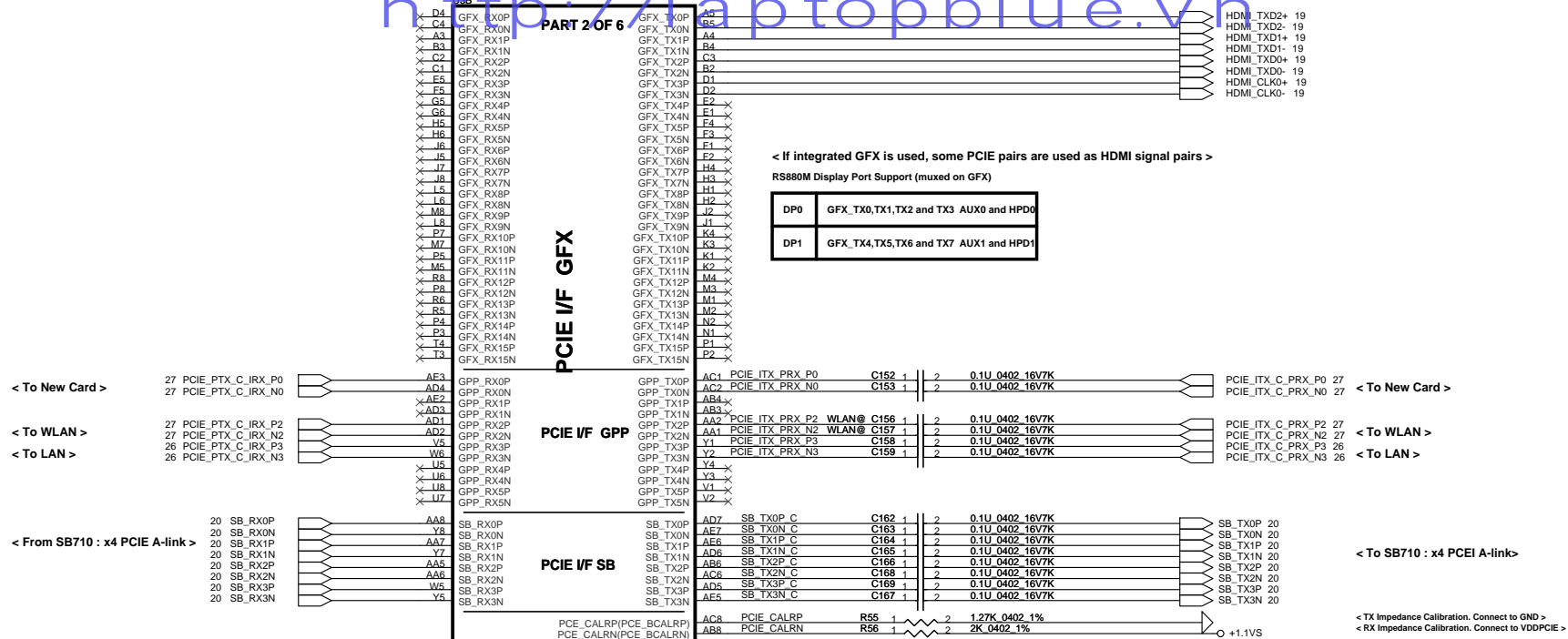
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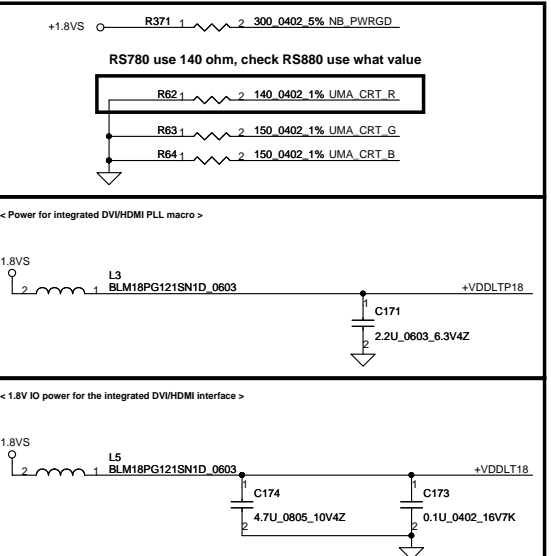
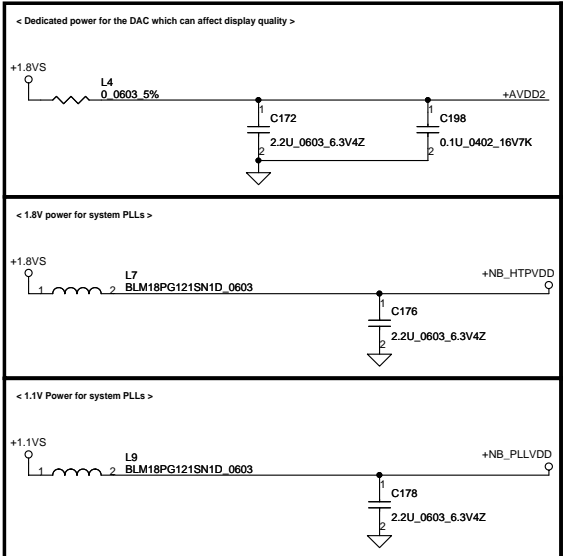
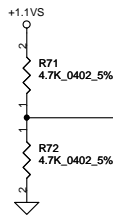


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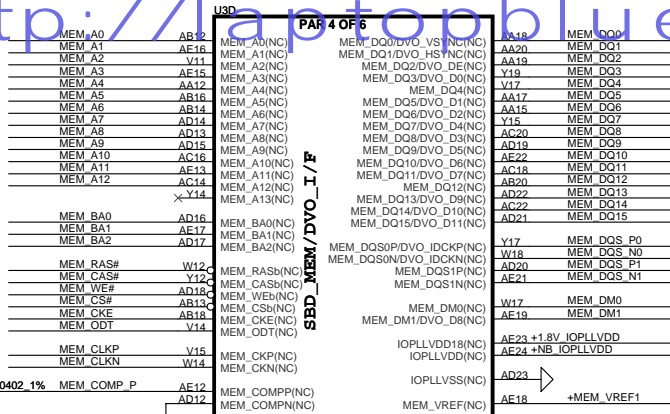
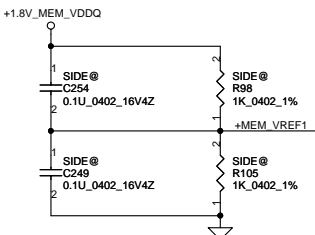
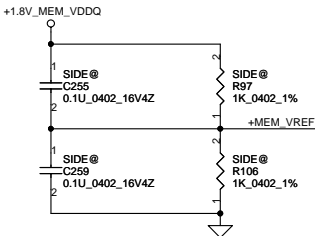
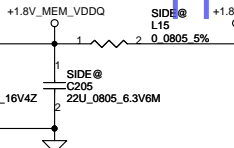






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220 ohm @ 100MHz,2A



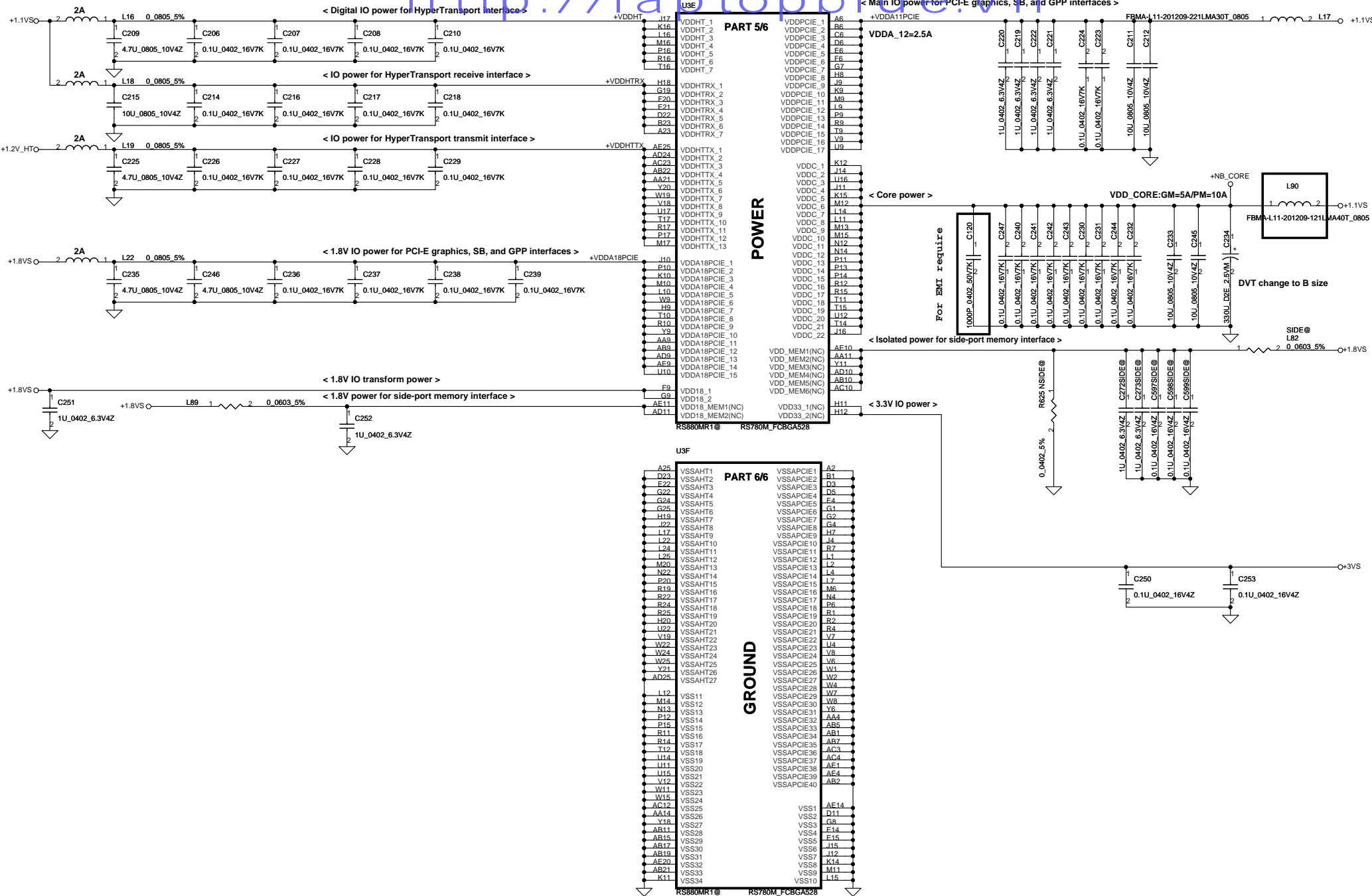
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions

MEM_BA0	L2	BA0	DQ15	B9	MEM_DQ15
MEM_BA1	L3	BA1	DQ14	B1	MEM_DQ11
			DQ13	D9	MEM_DQ13
MEM_A12	R2	A12	DQ12	D1	MEM_DQ12
MEM_A11	P7	A11	DQ11	D3	MEM_DQ8
MEM_A10	M2	A10/AP	DQ10	D7	MEM_DQ10
MEM_A9	P3	A9	DQ9	C2	MEM_DQ9
MEM_A8	P6	A8	DQ8	C8	MEM_DQ14
MEM_A7	P2	A7	DQ7	F9	MEM_DQ3
MEM_A6	N7	A6	DQ6	F1	MEM_DQ7
MEM_A5	N3	A5	DQ5	H9	MEM_DQ1
MEM_A4	N6	A4	DQ4	H1	MEM_DQ6
MEM_A3	N2	A3	DQ3	H3	MEM_DQ5
MEM_A2	M7	A2	DQ2	H7	MEM_DQ0
MEM_A1	M3	A1	DQ1	G2	MEM_DQ4
MEM_A0	M8	A0	DQ0	G8	MEM_DQ2

MEM_CLKN	K8	CK	VDDQ	A9	+1.8V_MEM_VDDQ
MEM_CLKP	J8	CK	VDDQ	C1	
MEM_CKE	K2	CKE	VDDQ	C3	
			VDDQ	C7	
			VDDQ	C9	
			VDDQ	E9	
			VDDQ	G1	
			VDDQ	G3	
			VDDQ	G7	
			VDDQ	G9	
MEM_CS#	L8	CS	VDD	A1	
MEM_WE#	K1	WE	VDD	F1	
MEM_RAS#	K7	RAS	VDD	J9	
MEM_CAS#	L7	CAS	VDD	M9	
MEM_DM0	F3	LDM	VDD	R1	
MEM_DM1	B3	UDM	VDD		
MEM_ODT	K9	ODT	VDDL	J1	+VDDL
			VSSDL	J7	
MEM_DQS_P0	F7	LDQS	VSSQ	A7	
MEM_DQS_N0	F8	LDQS	VSSQ	B2	
			VSSQ	B8	
			VSSQ	D2	
			VSSQ	D8	
			VSSQ	E7	
			VSSQ	F2	
			VSSQ	F8	
			VSSQ	H2	
			VSSQ	H8	
			VSS	A3	
			VSS	E3	
			VSS	J3	
			VSS	N1	
			VSS	P9	

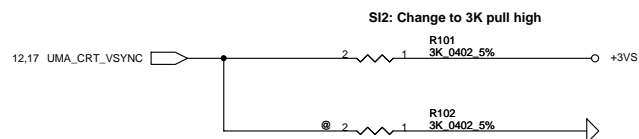
SA00002UH00 : Hynix (EVT verification)
SA0000031O00 : Samsung (DVT verification)
64M*16 DDR2 500MHZ

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< RS880 VSYNC mux at CRT_VSYNC pull High to 3K >



< VSYNC : STRAP_DEBUG_BUS_GPIO_ENABLEb >

Enables the Test Debug Bus using GPIO.

1 : Enable (RX881, RS880)
0 : Disable (RX881, RS880)

PIN: RS880--> VSYNC#

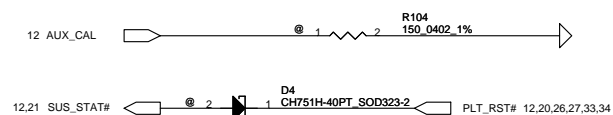
< RS880 use register to control PCI-E configure >

< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] >

These pin straps are used to configure PCI-E GPP mode.

000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011

< RS880 SUS_STAT# >



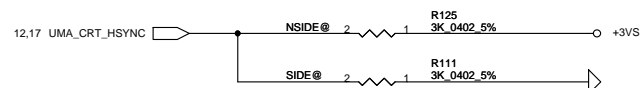
< SUS_SATA# : LOAD_EEPROM_STRAPS >

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880:SUS_STAT#

< RS880 use HSYNC to enable SIDE PORT (internal pull high) >



< HSYNC : STRAP_DEBUG_BUS_PCIE_ENABLEb >

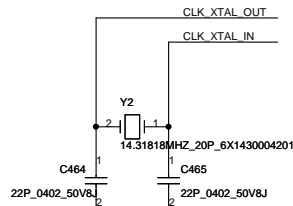
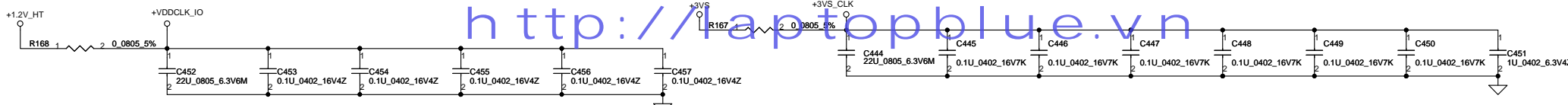
RX881: Enables the Test Debug Bus using PCIE bus

1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

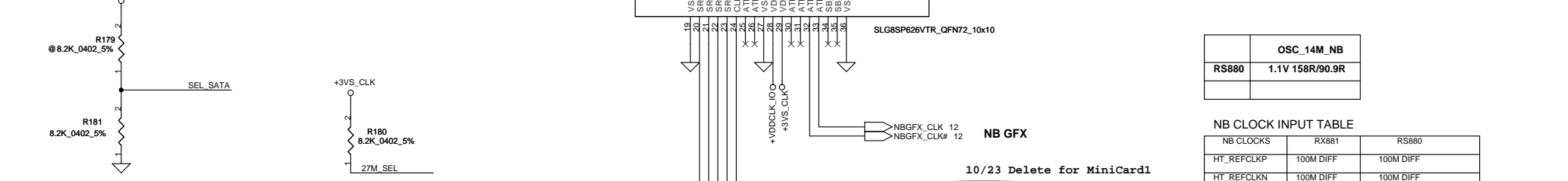
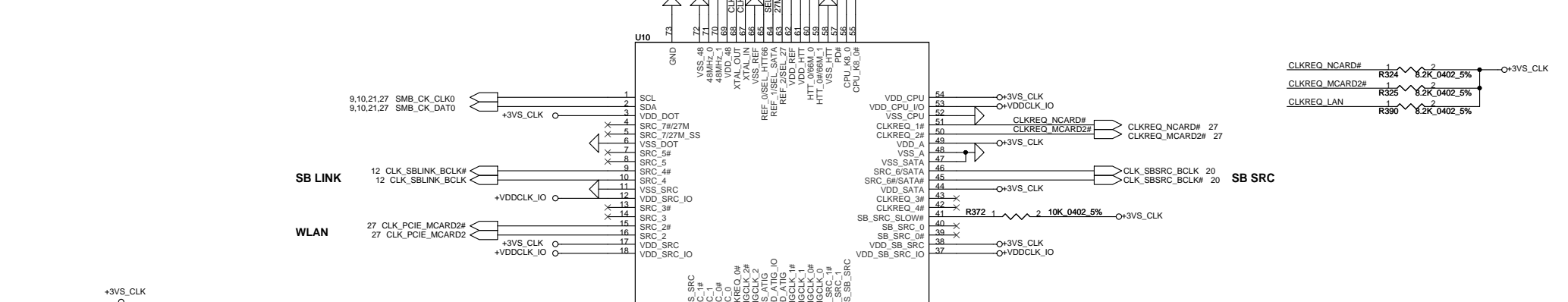
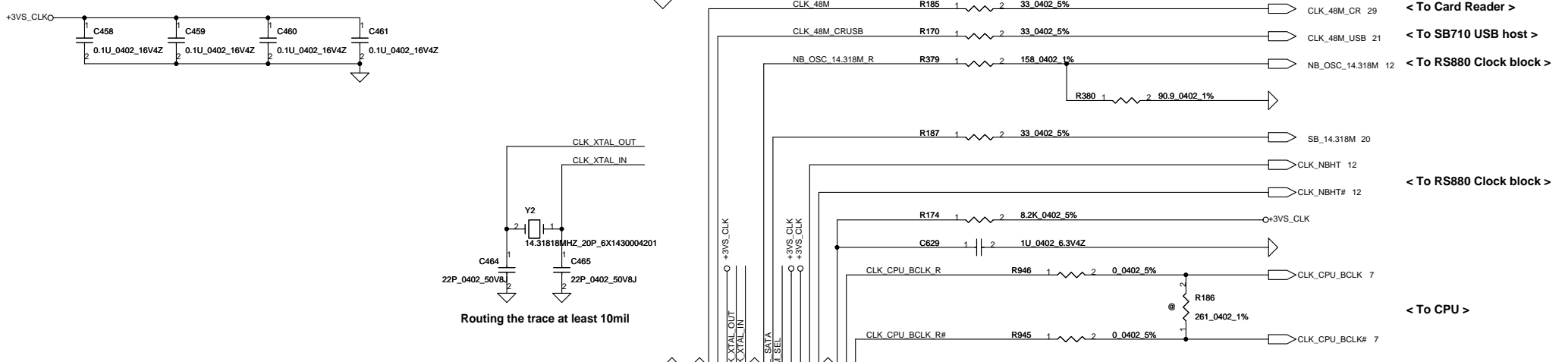
RS880: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS880)
0 : Enable (RS880)

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Routing the trace at least 10mil



SEL_SATA	1	configure as SATA output
	0 *	configure as normal SRC(SRC.6) output * default

27M_SEL	1 *	configure as 27M and 27M_SS output
	0	configure as SRC.7 output * default

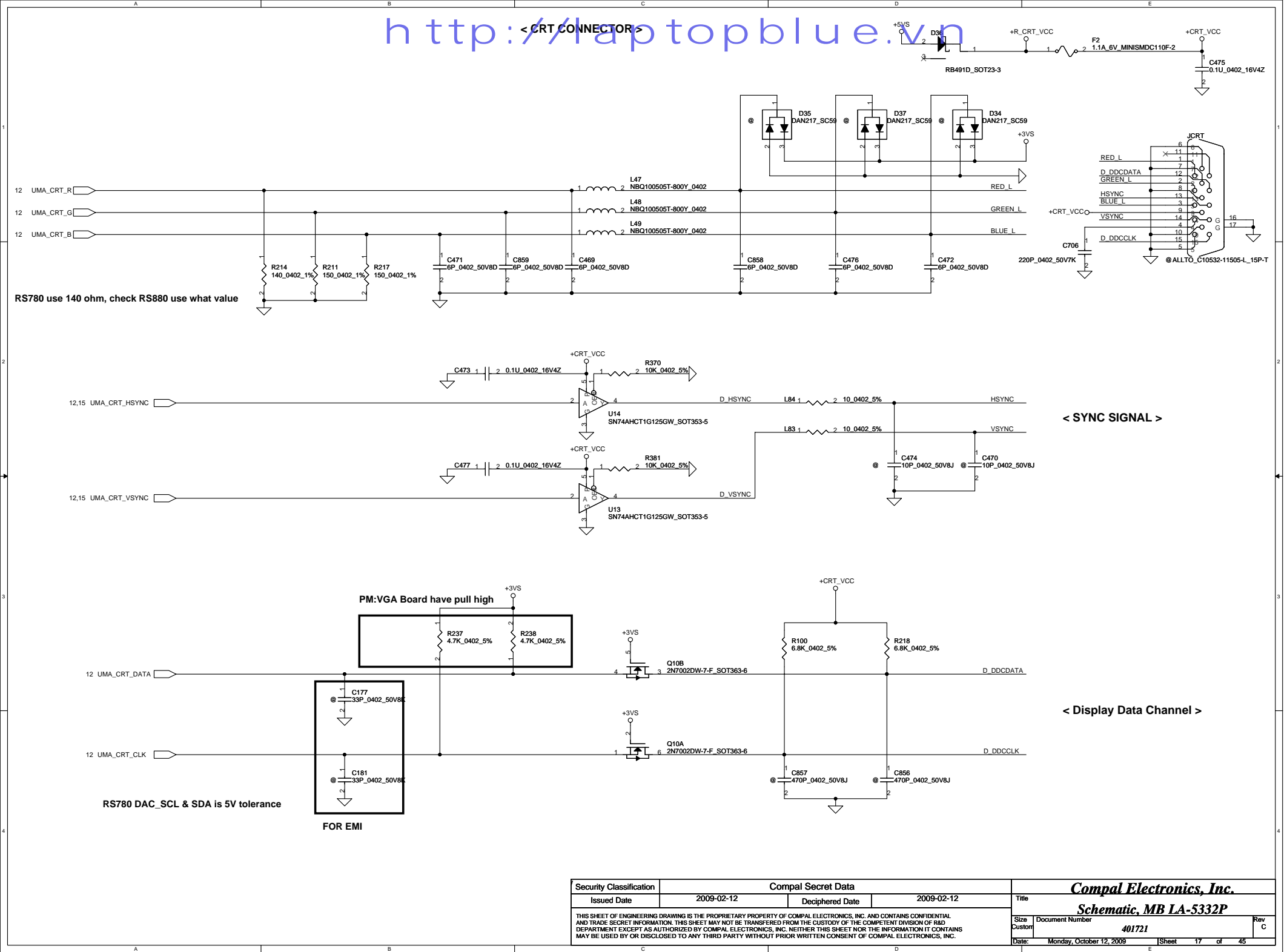
Use voltage divider resistor R379 & R380 to pull low

NB_OSC_14.318M	1	configure as single-ended 66MHz output
	0 *	configure as differential 100MHz output * default

	OSC_14M_NB
RS880	1.1V 158R/90.9R

NB CLOCK INPUT TABLE

NB CLOCKS	RX881	RS880
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF



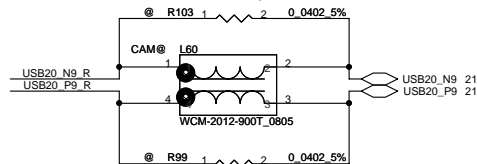
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				Date:	Monday, October 12, 2009
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Schematic, MB LA-5332P

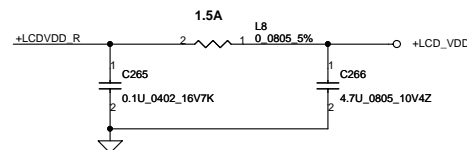
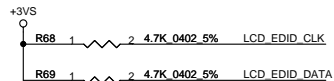
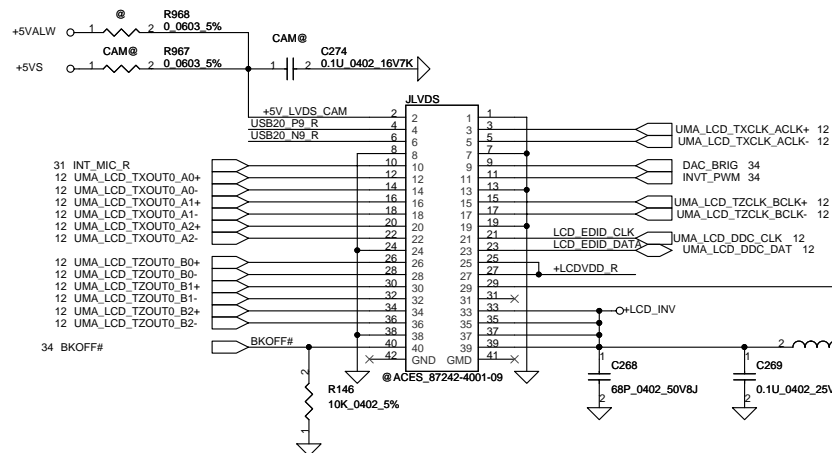
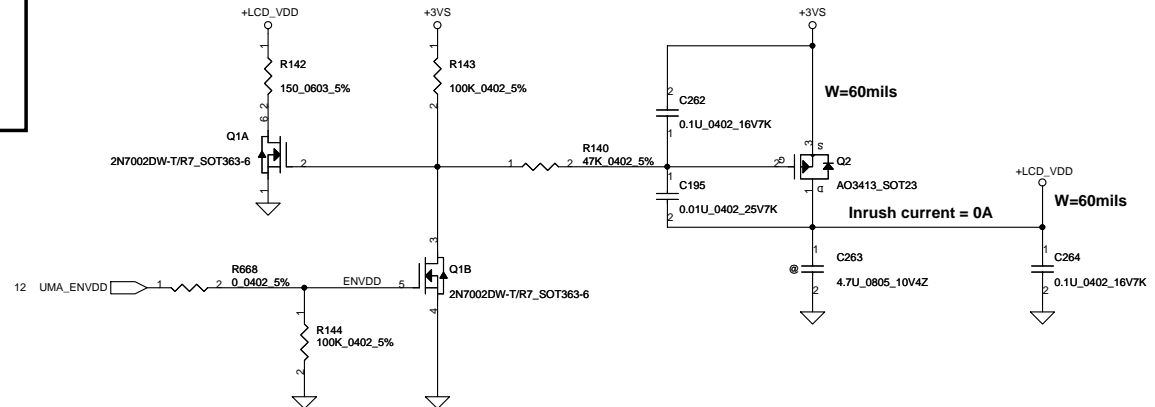
< Int. Camera, USB port 9 >

http://laptopblue.vn

< EMI require >

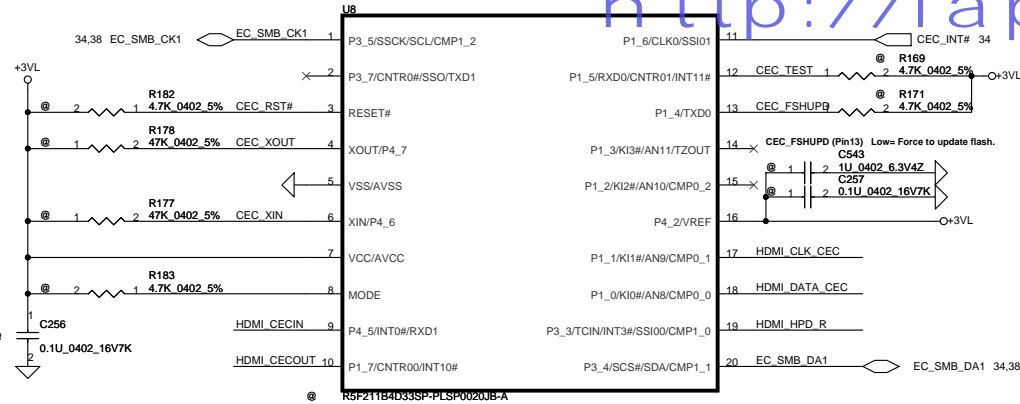


LCD/PANEL BD. Conn.

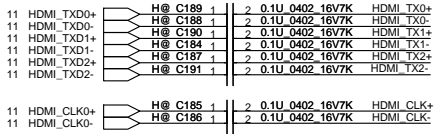


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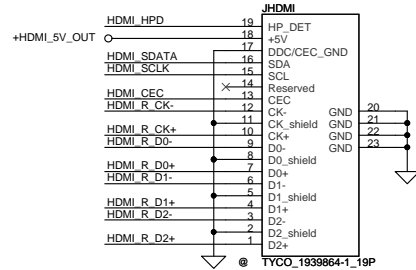
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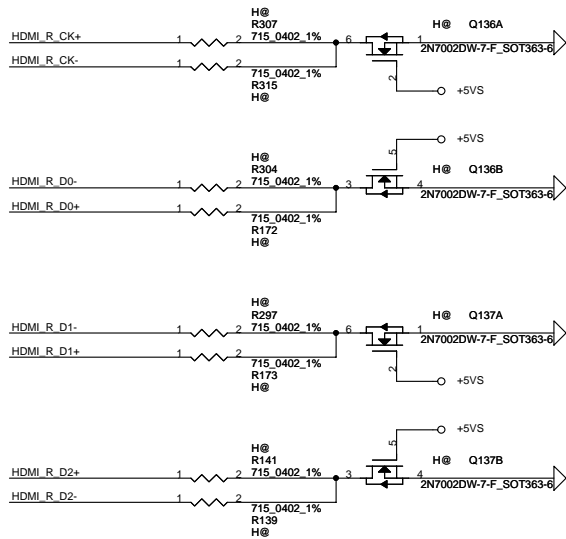
SI:Add R616~R624 for EMI request



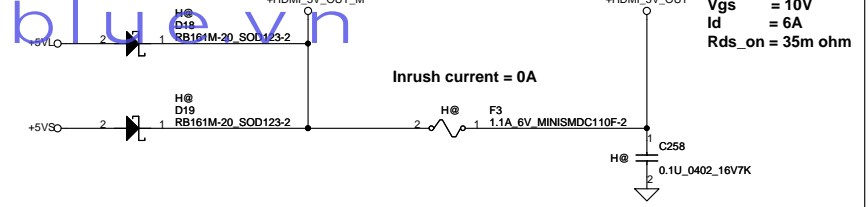
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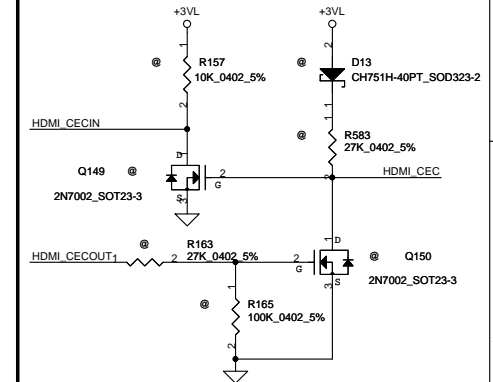
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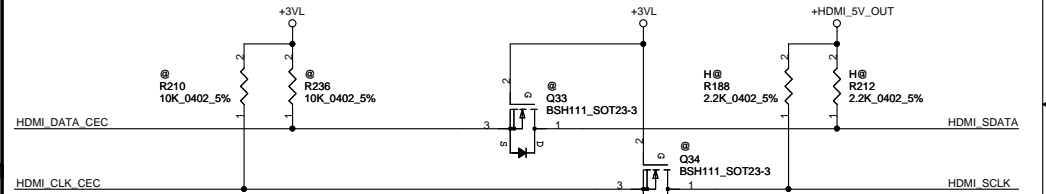
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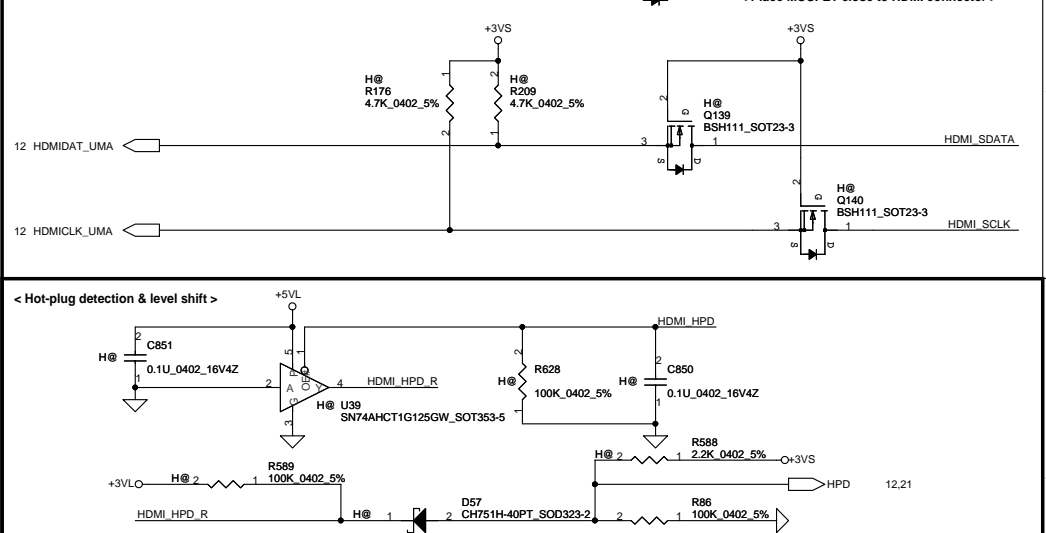
< HDMI_CEC level shift > < Place MOSFET close to HDMI connector >



< HDMI DDC channel to device >



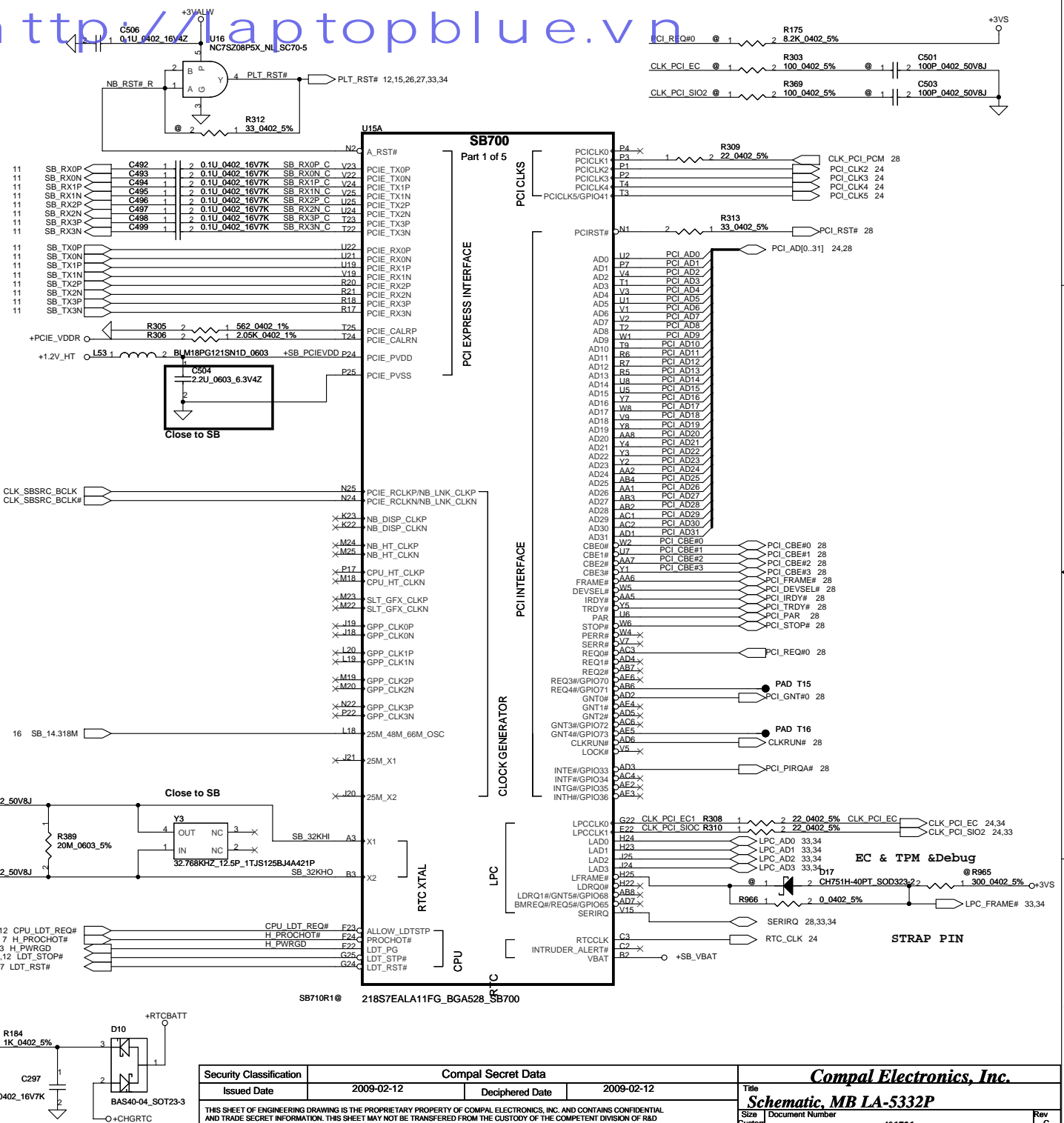
< Hot-plug detection & level shift >



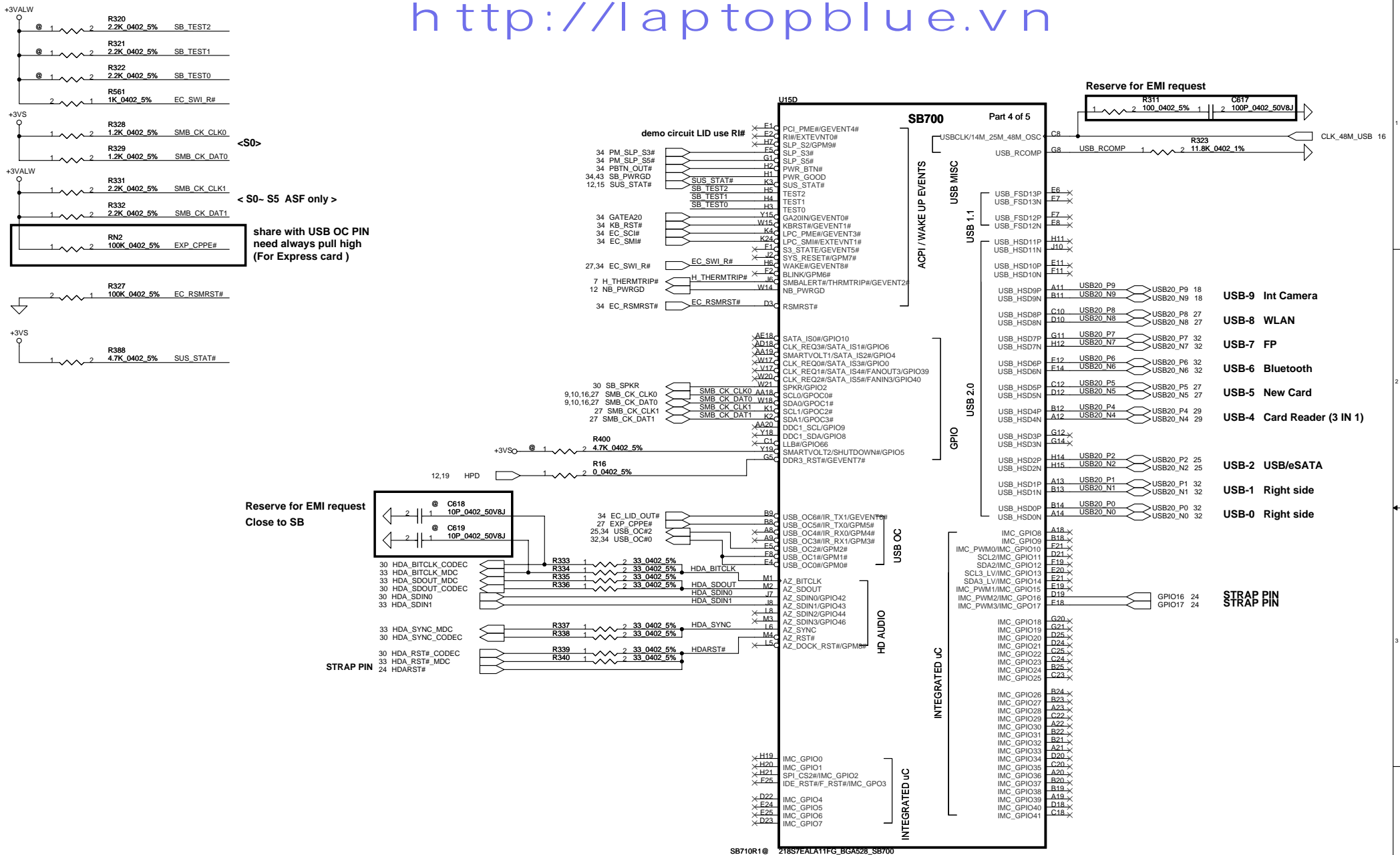
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Schematic, MB LA-5332P



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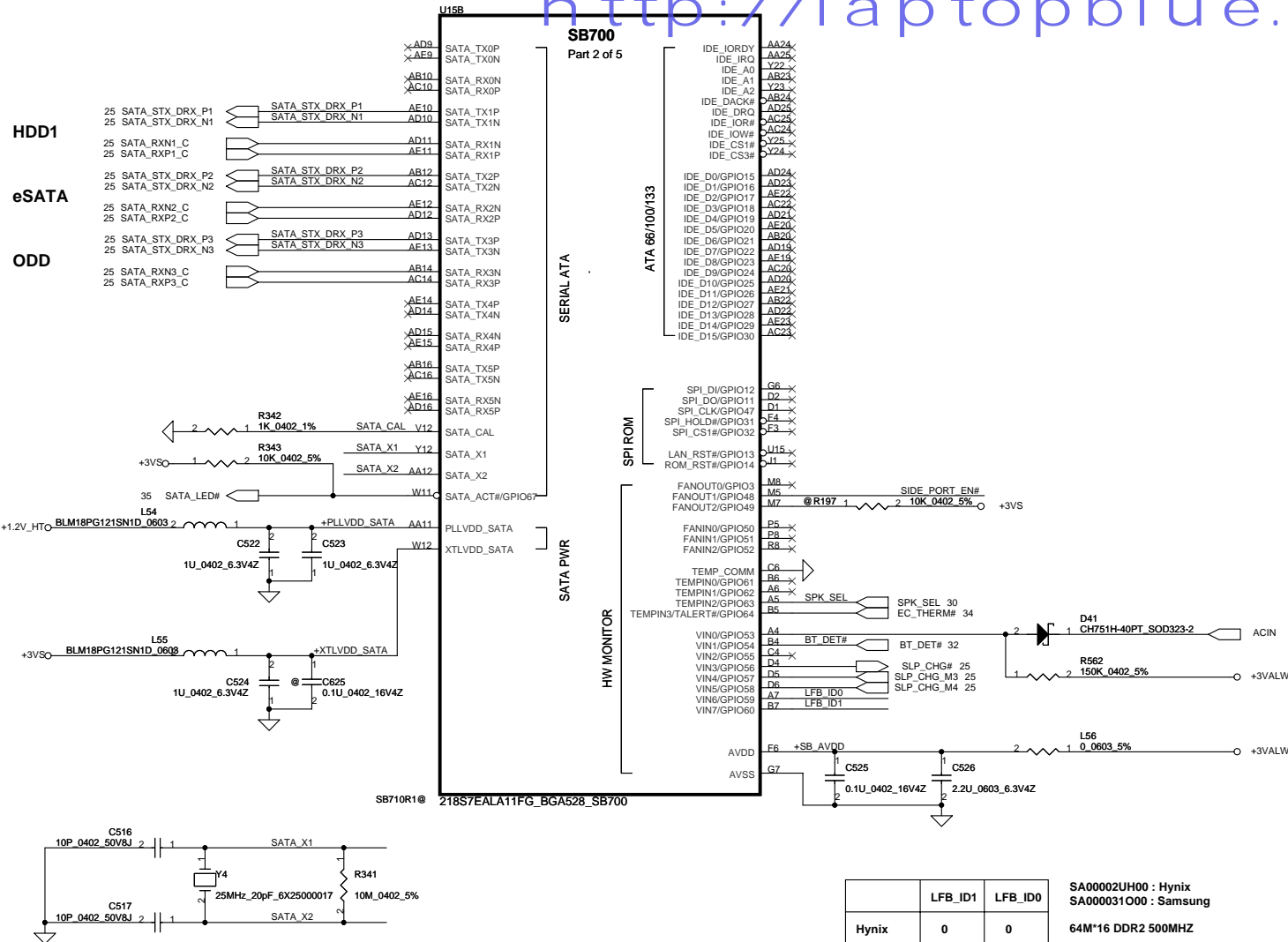


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HDD1

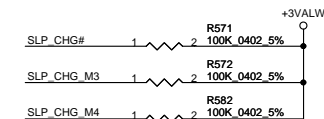
eSATA

ODD



	HDMI DISABLE	HDMI ENABLE
SIDE_PORT_EN#	0	1

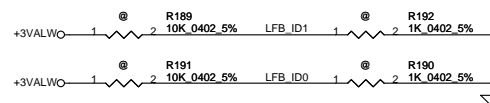
GPIO48,GPIO49 GOT INTERNAL PU 8.2K TO S0



	LFB_ID1	LFB_ID0
Hynix	0	0
Samsung	0	1
	1	0
	1	1

SA00002UH00 : Hynix
SA000031O00 : Samsung
64M*16 DDR2 500MHZ

LFB_ID0 to LFB_ID1 got internal PU 10K to S5.

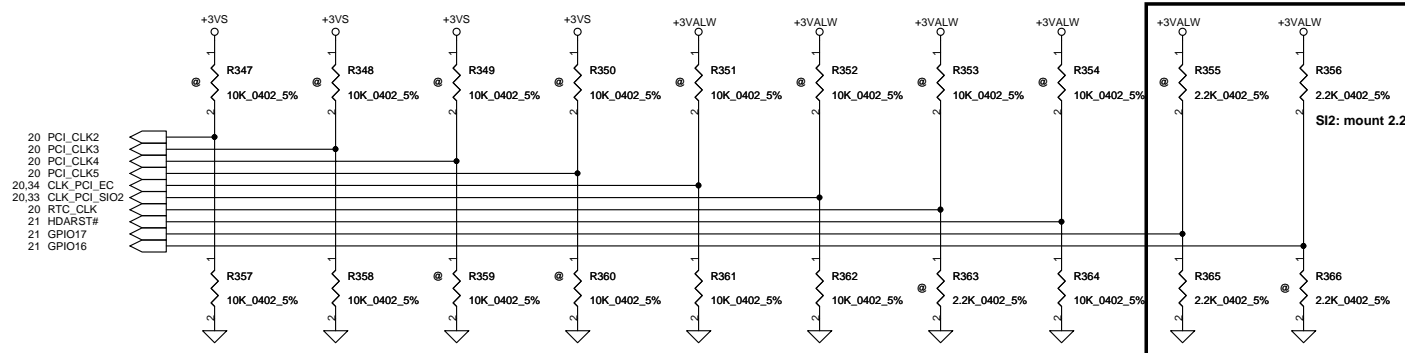


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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default) L,L = FWH ROM

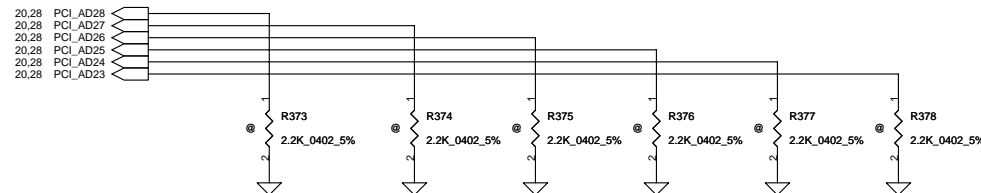


Need to confirm if SB SPI ROM will mount

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

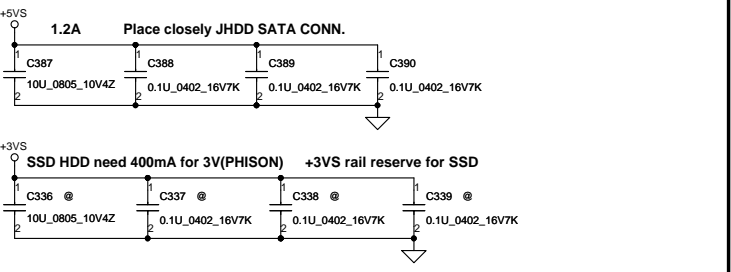
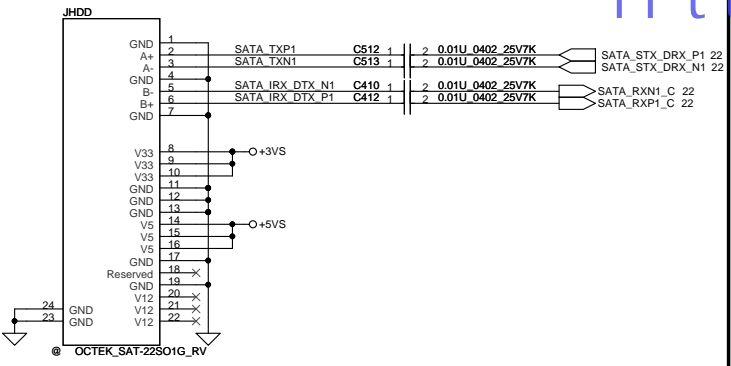


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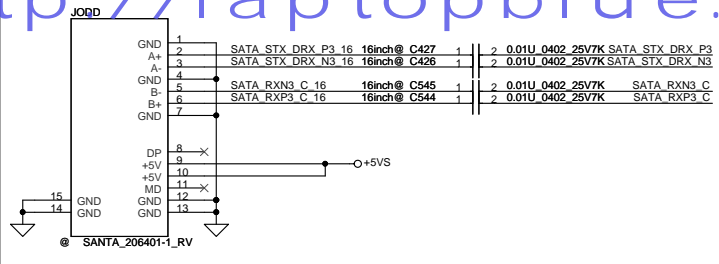
Schematic, MB LA-5332P

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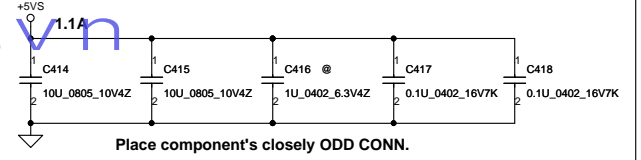
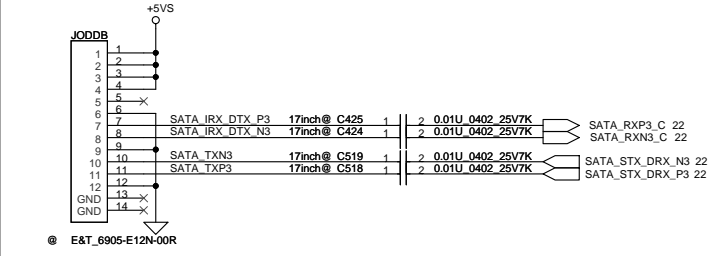
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< 16" SATA ODD Conn >

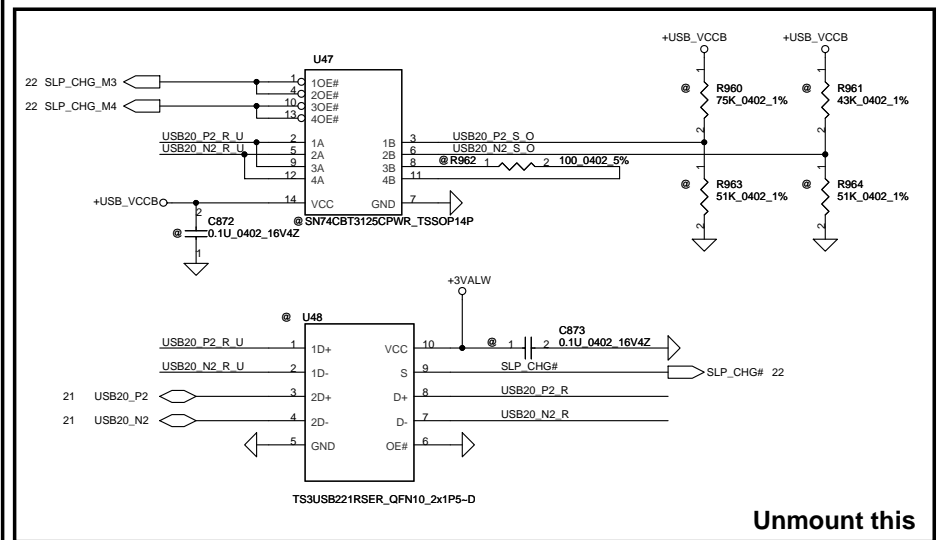


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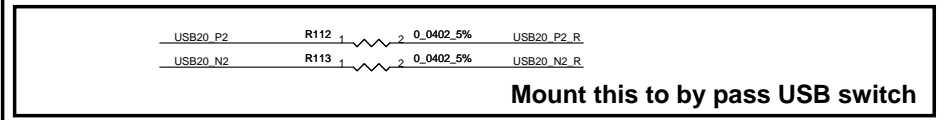


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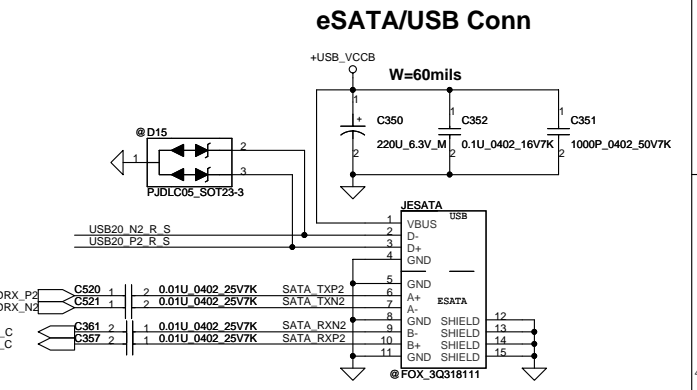
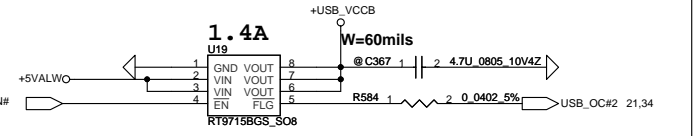
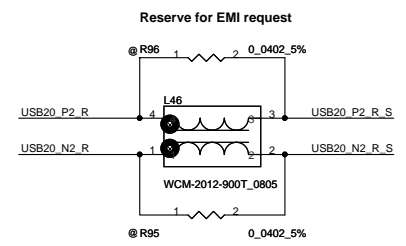
10/22 Add for USB Sleep & Charge M3/M4



Unmount this



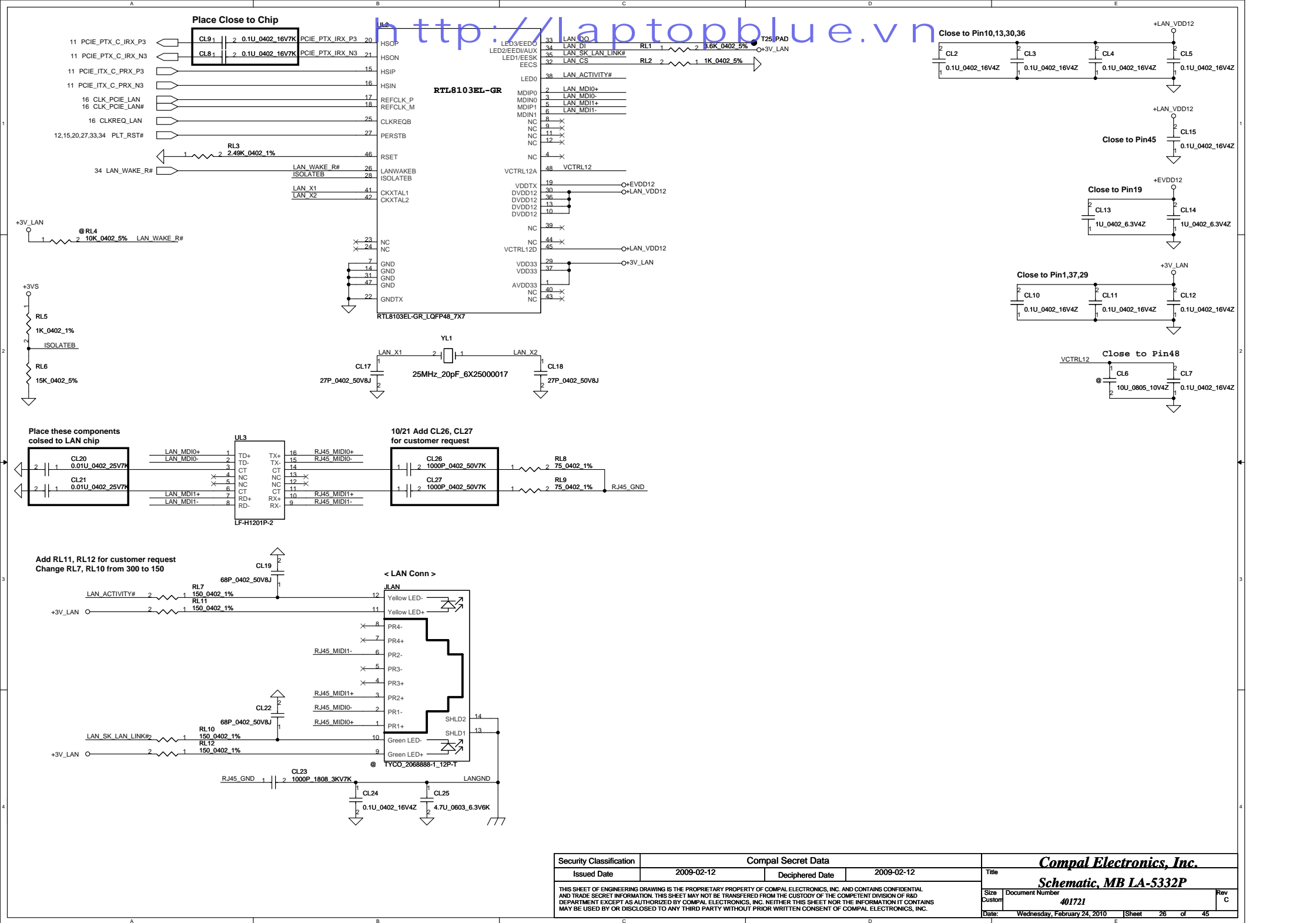
Mount this to by pass USB switch



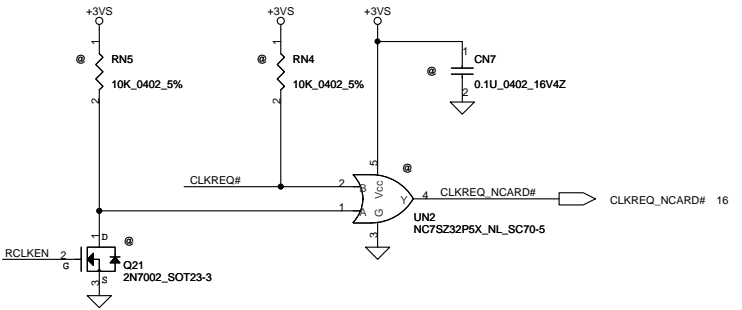
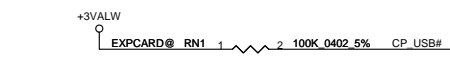
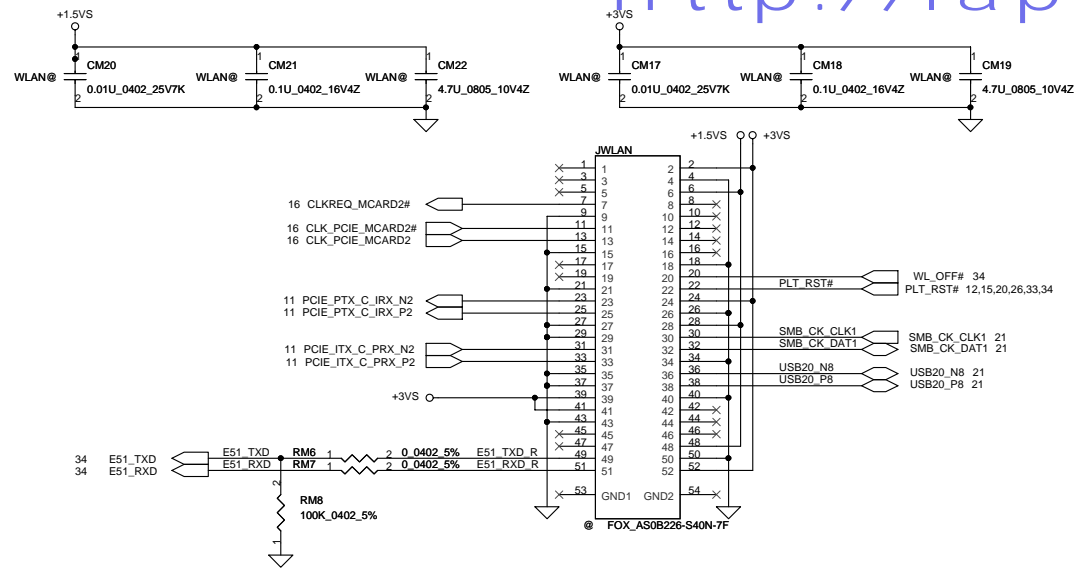
	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

SLP_CHG#	FUNCTION
LOW	D=1D
HIGH	D=2D

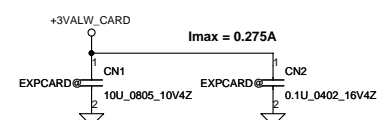
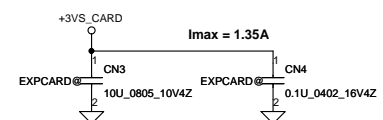
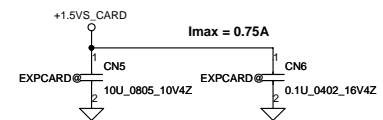
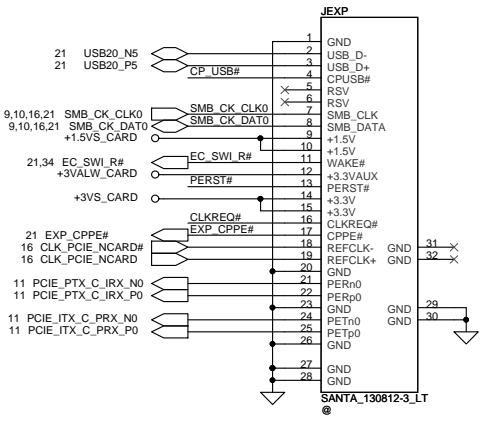
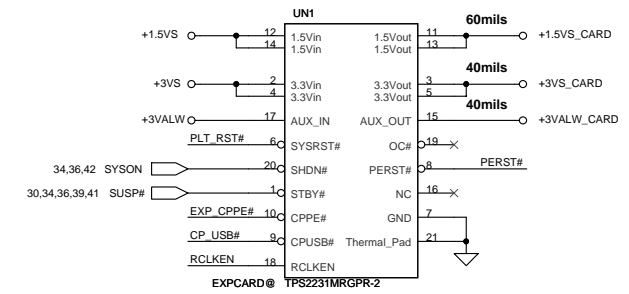
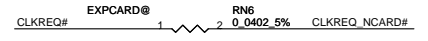
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< PCIe Mini Card for WLAN >

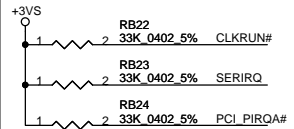


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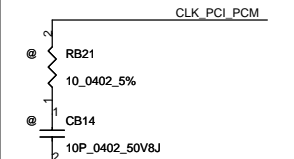


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22K TO 47K PULL-UPS MUST BE PLACED ON INTA#, PME#, SERIRQ# & CLKRUN#.



For EMI



NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME.

IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

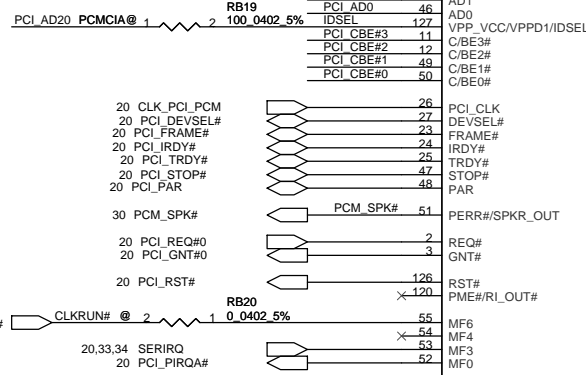
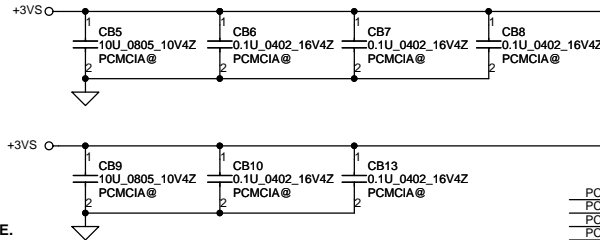
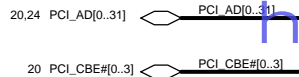
22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS.

THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

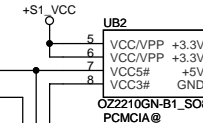
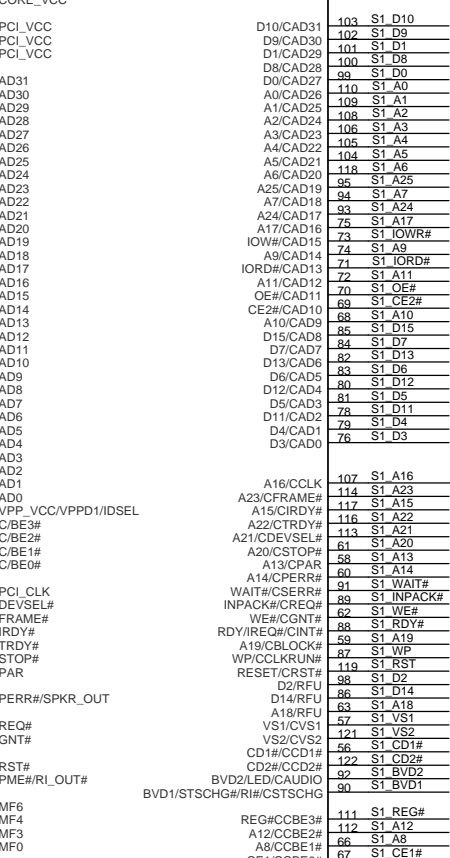
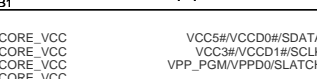
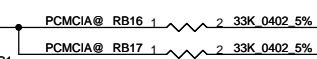
CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127 ball F4

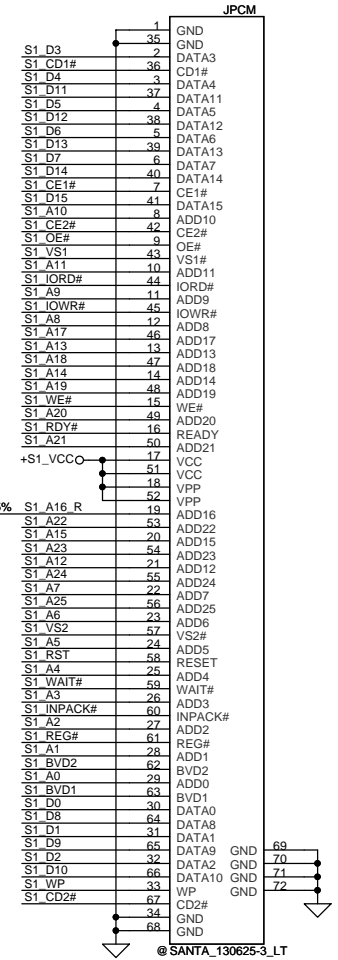
must check IDSEL, PCI_PIRQ#,



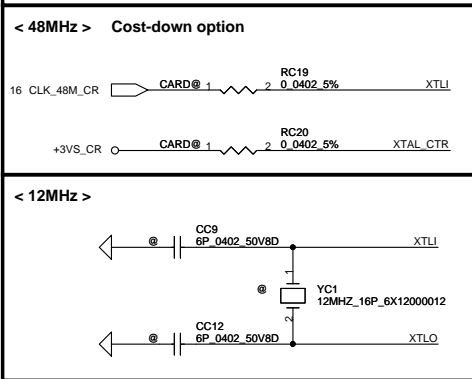
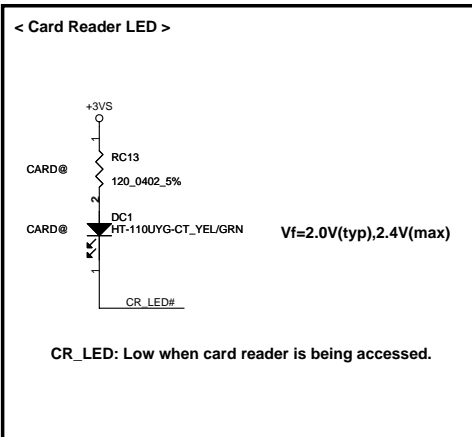
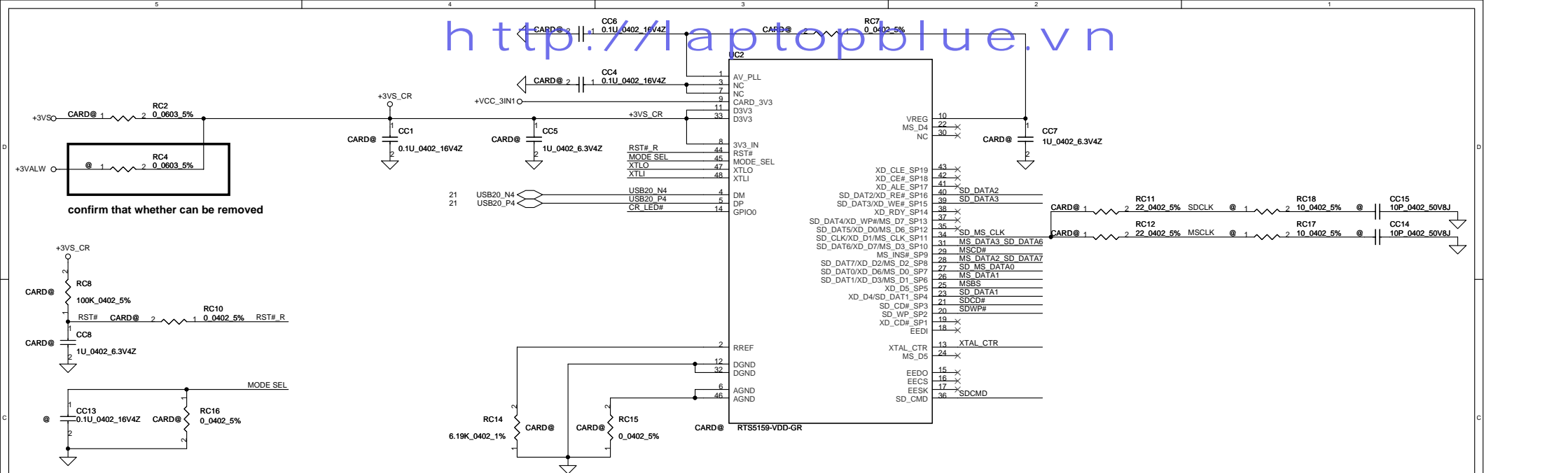
IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)



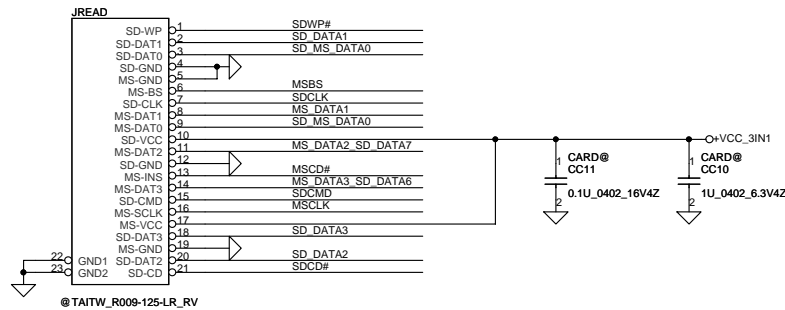
PCMCIA Socket



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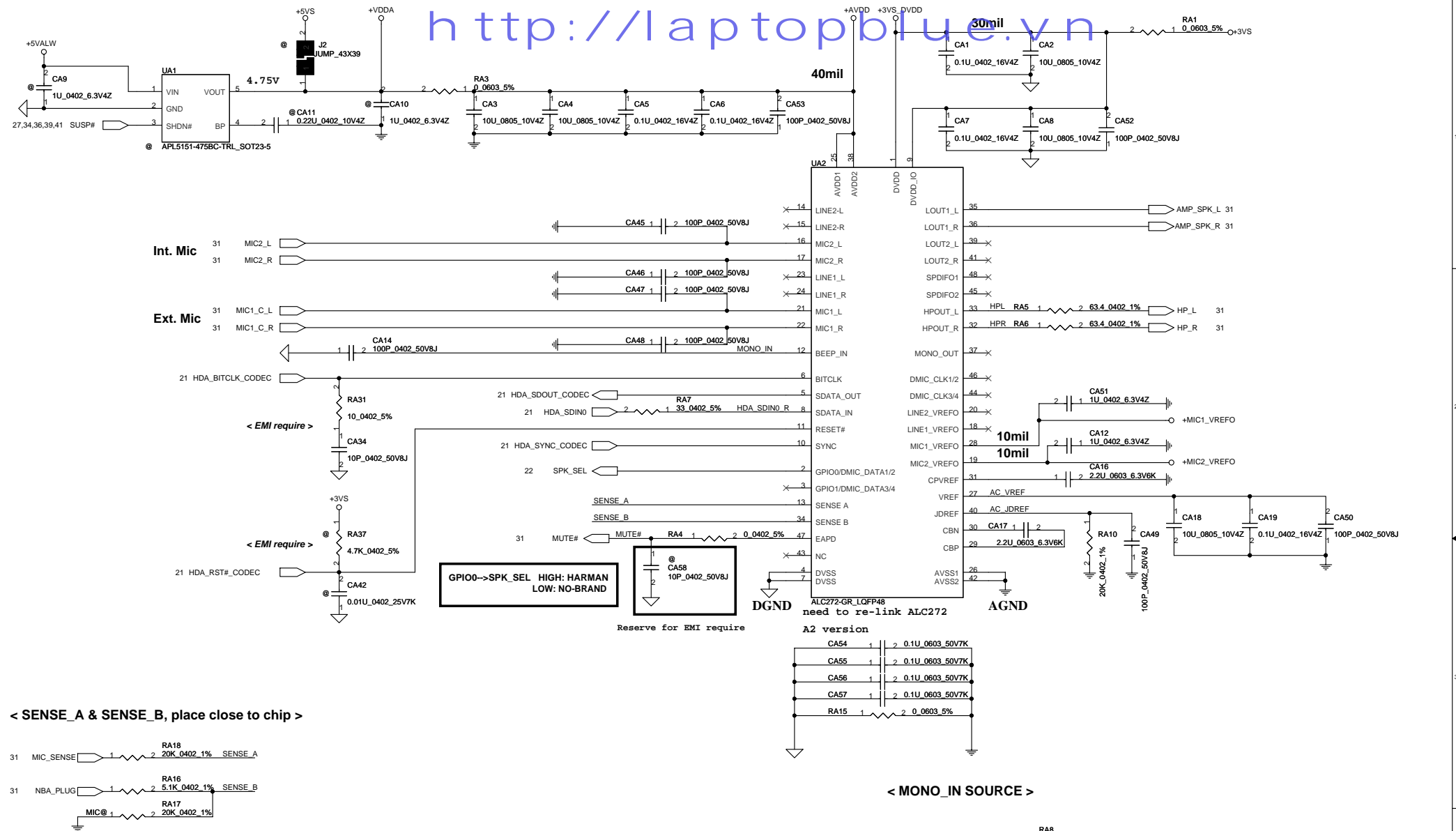


< 3 in 1 Card Reader >

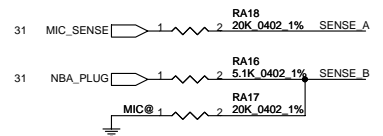


R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

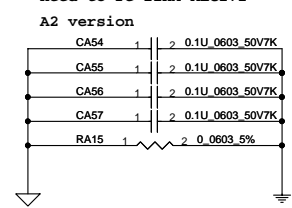
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						Size	Document Number			Rev		C
							401721					
						Date:	Monday, October 12, 2009		Sheet	29	of	45



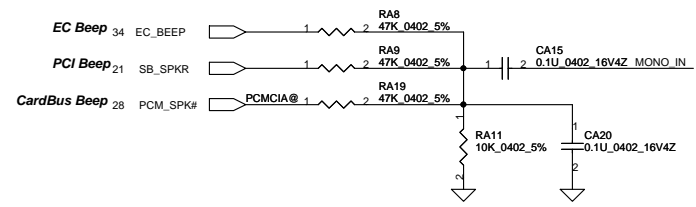
< SENSE_A & SENSE_B, place close to chip >



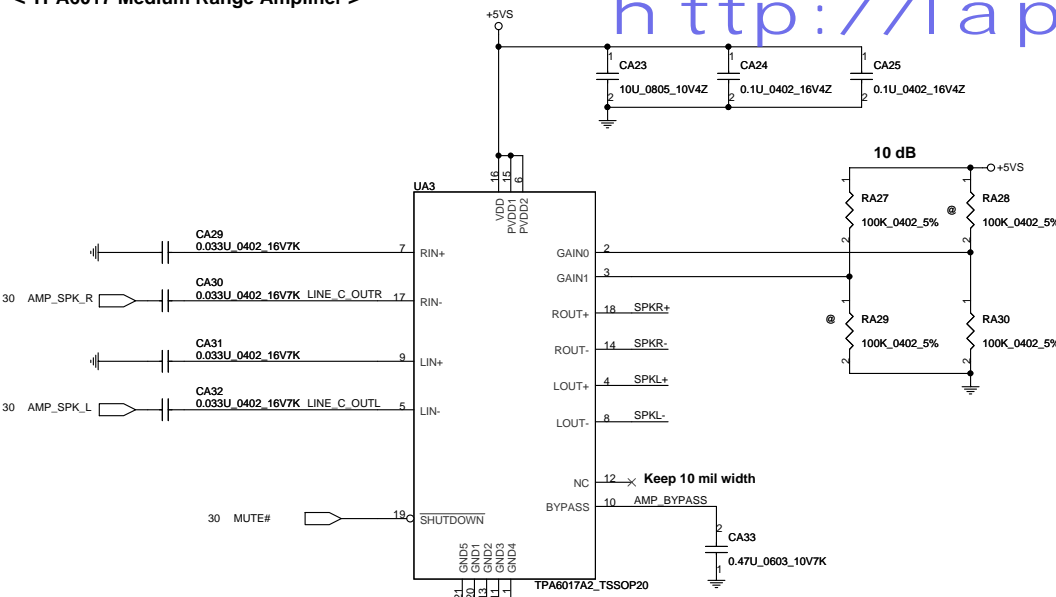
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	Ext. MIC
	20K	PORT-B (PIN 21, 22)	
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	Int. MIC
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out



< MONO_IN SOURCE >

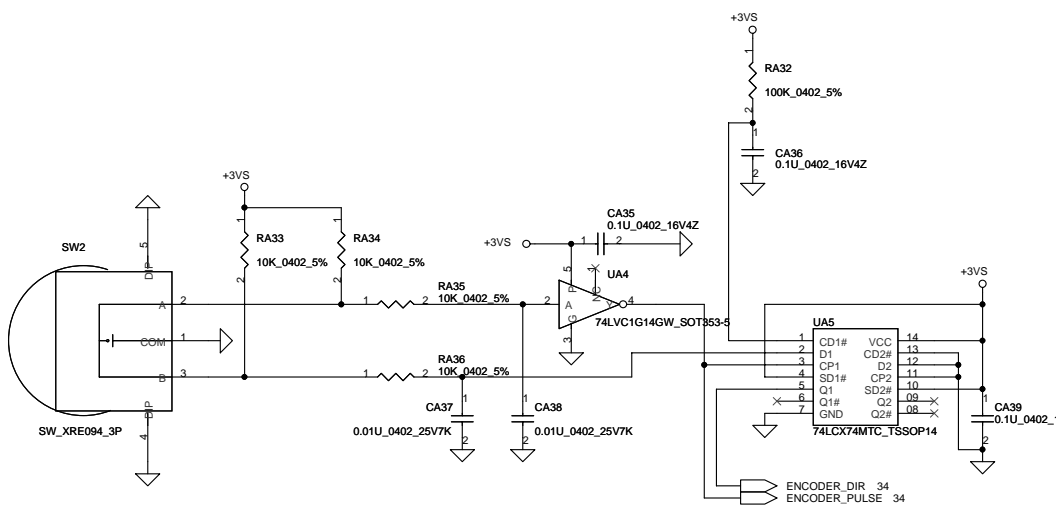


< TPA6017 Medium Range Amplifier >

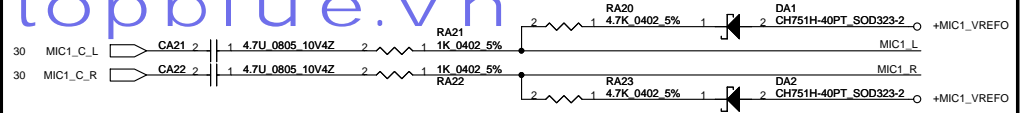


GAIN0	GAIN1	Av(db)	Rin(ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

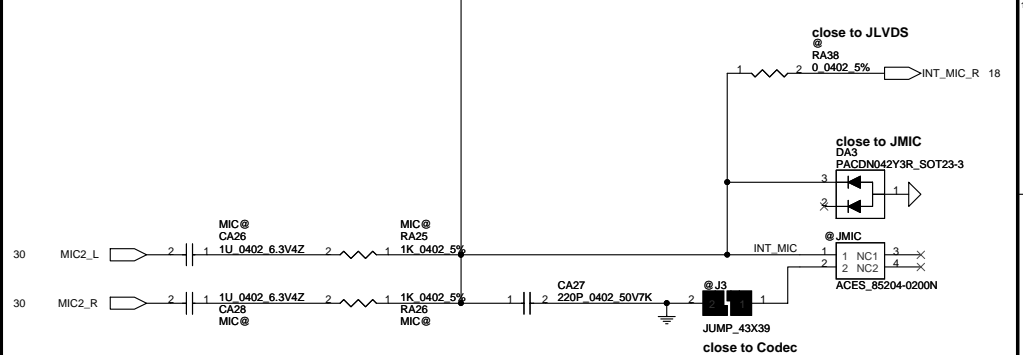
< Volume Control >



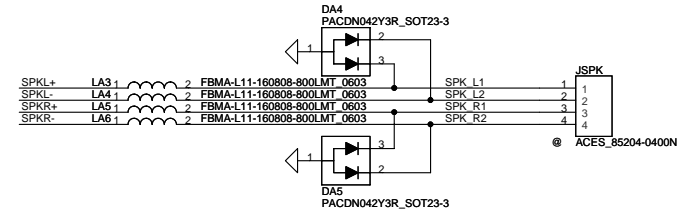
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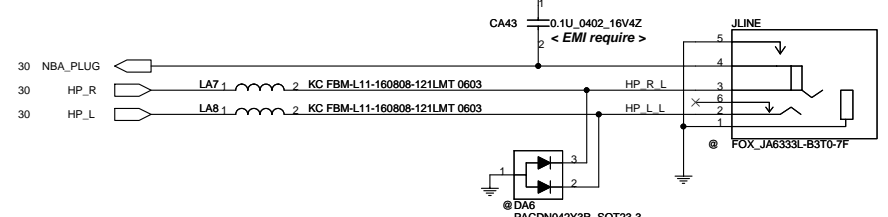
< Int. Mic >



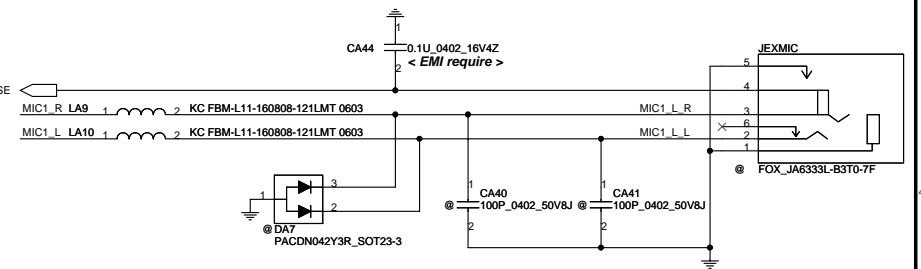
< Speaker Connector >



< HeadPhone JACK >



< Ext.MIC/LINE IN JACK >

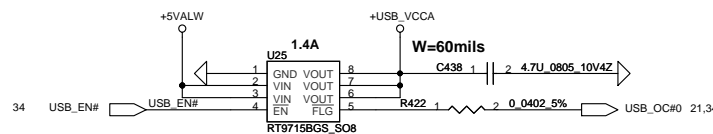


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				Custmr	401721	C
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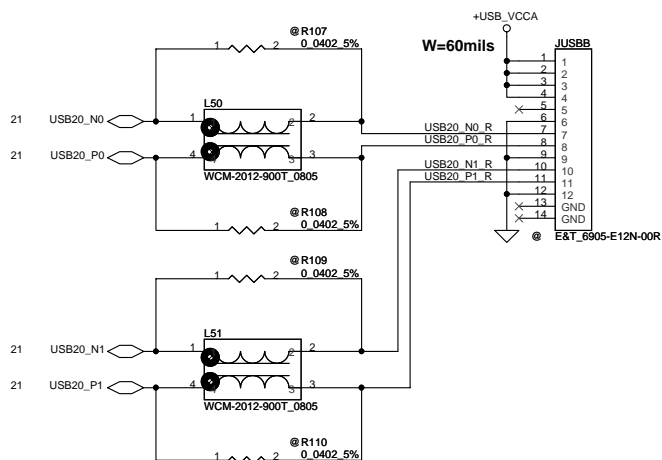
Compal Electronics, Inc.

Schematic, MB LA-5332P

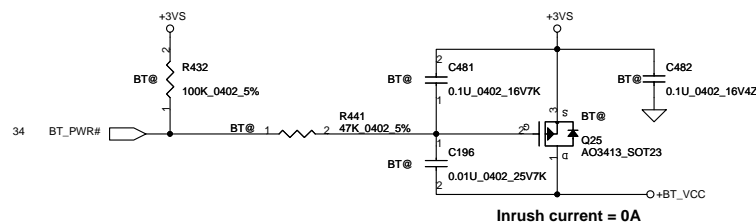
< USB Right-side Board, USB port 0,1 >



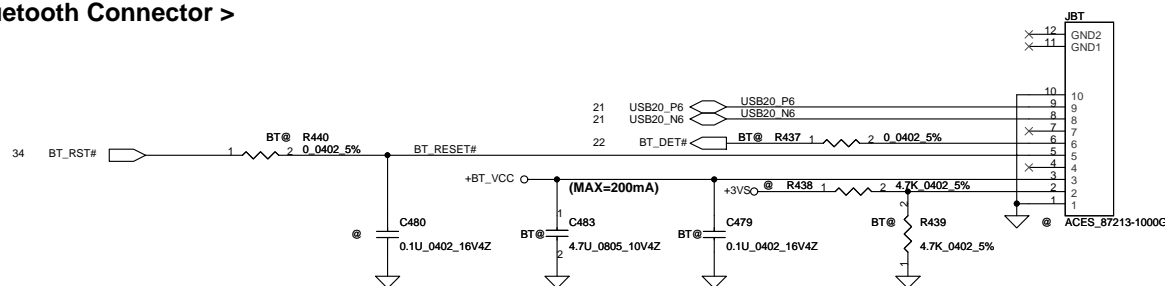
< Reserve for EMI request >



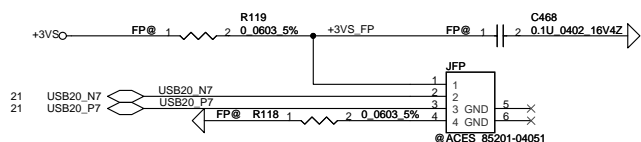
< Bluetooth Interface, USB port6 >



< Bluetooth Connector >



< Finger Printer, USB port 7 >

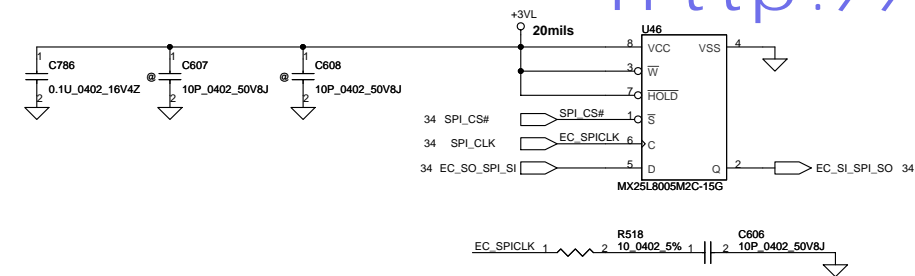


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								401721		Rev C	
Date:						Wednesday, February 24, 2010		Sheet 32 of 45			

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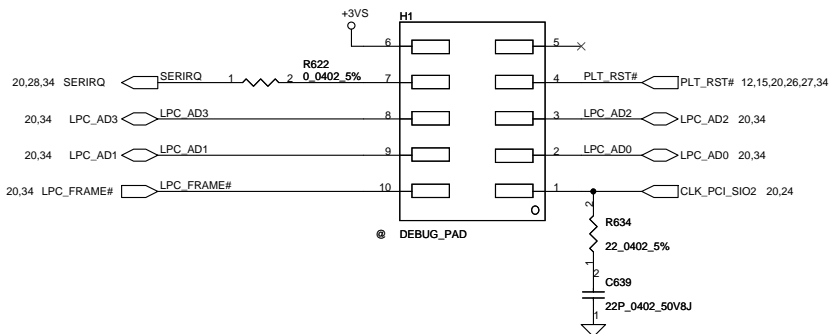
Schematic, MB LA-5332P

< SPI Flash 8Mb*1 >

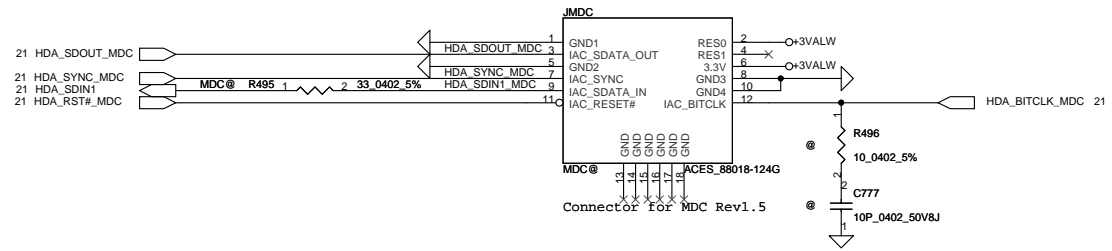


< LPC Debug Port >

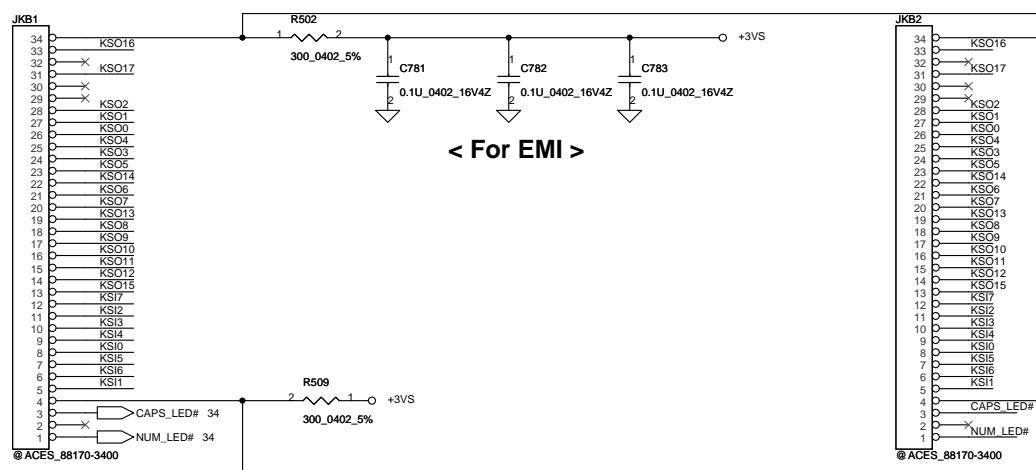
Please place the PAD under DDR DIMM.



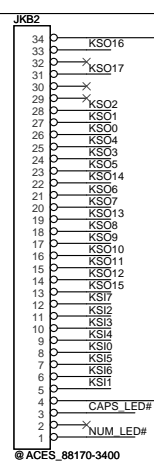
< MDC 1.5 Conn >



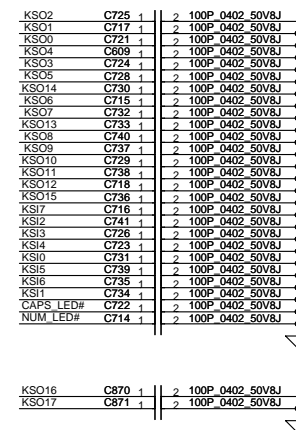
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< KEYBOARD CONN 17" >



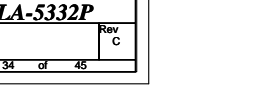
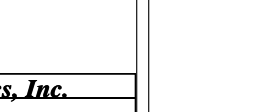
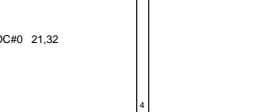
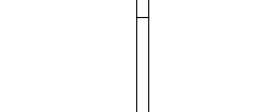
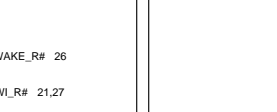
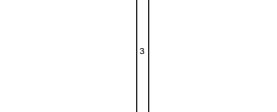
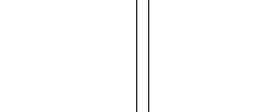
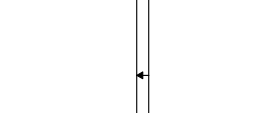
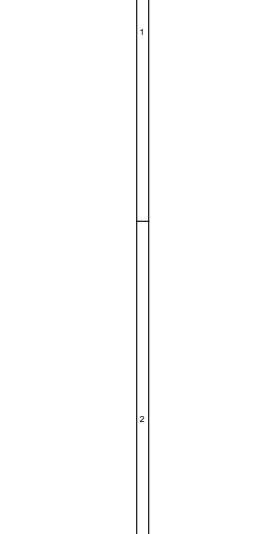
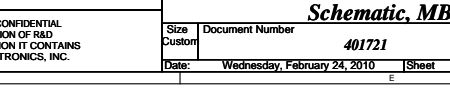
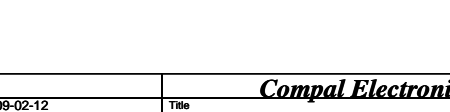
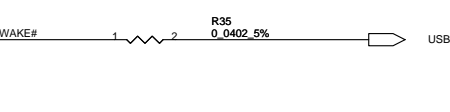
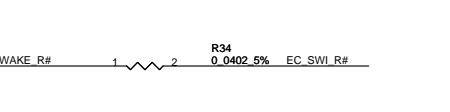
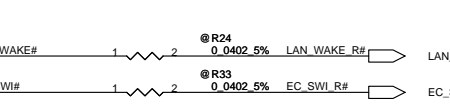
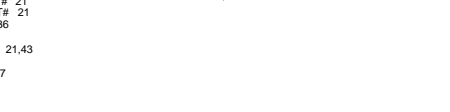
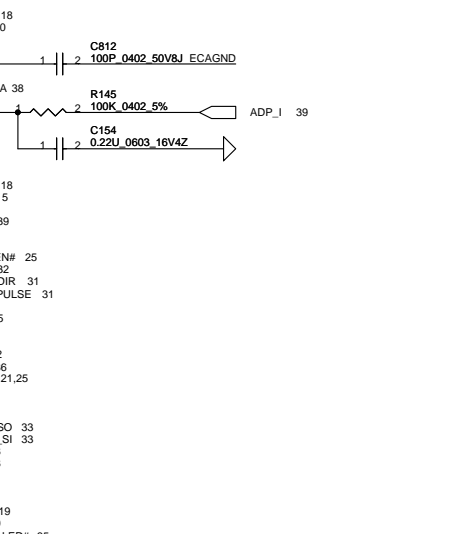
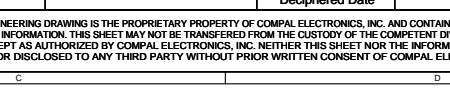
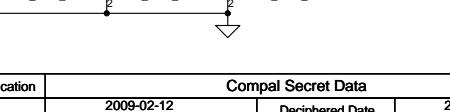
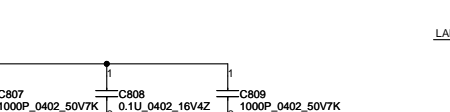
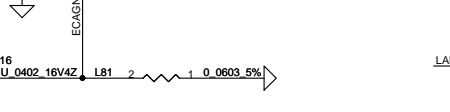
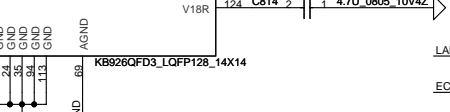
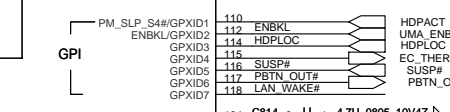
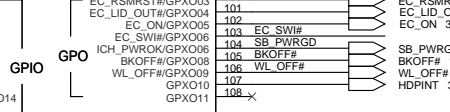
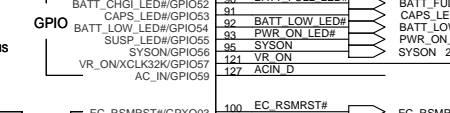
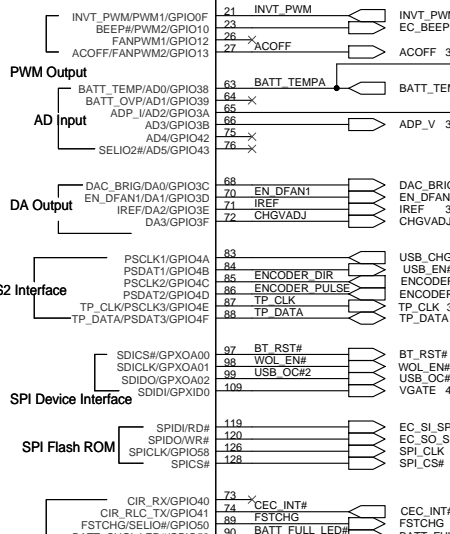
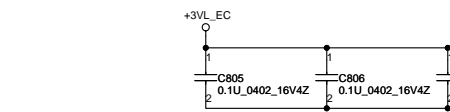
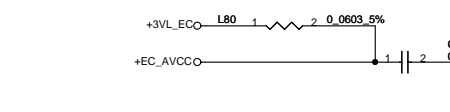
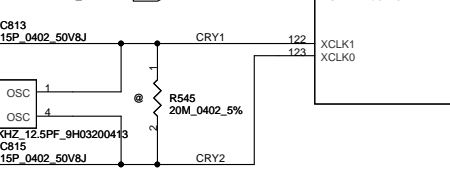
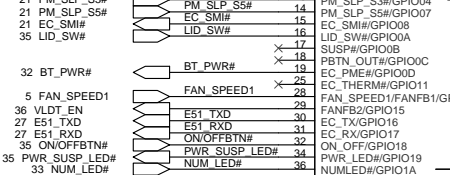
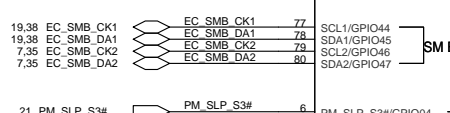
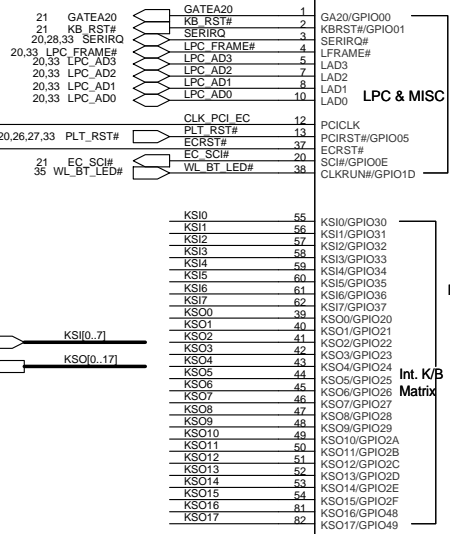
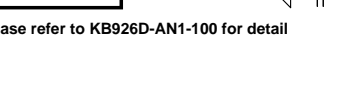
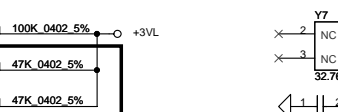
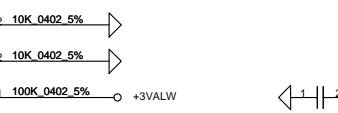
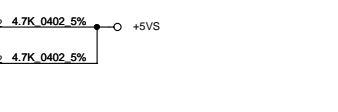
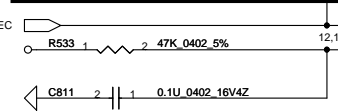
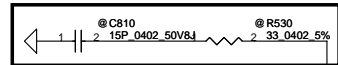
< For EMI >



KSI[0..7] KSI[0..7] 34,35
KSO[0..17] KSO[0..17] 34,35

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Reserve for EMI request

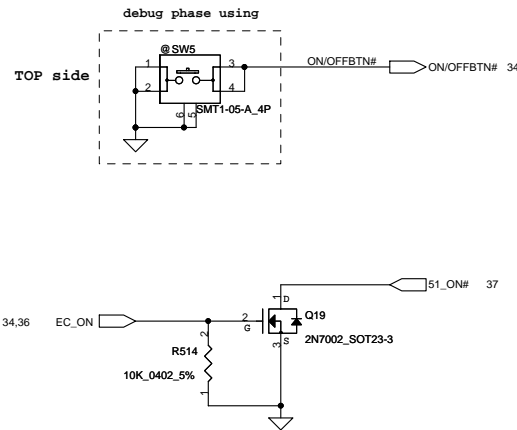


Add for KB926D2 issue. Please refer to KB926D-AN1-100 for detail

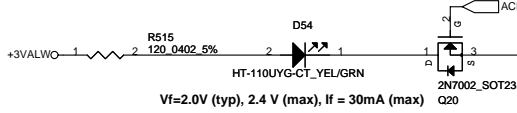
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				Date: Wednesday, February 24, 2010	Sheet 34 of 45

Compal Electronics, Inc.
Schematic, MB LA-5332P

< Power Button for Debug >

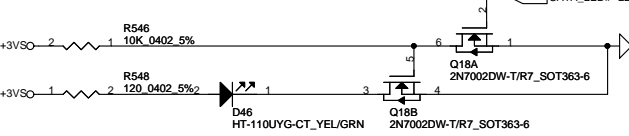


< DC-IN LED >



Remove WiMAX LED control circuit

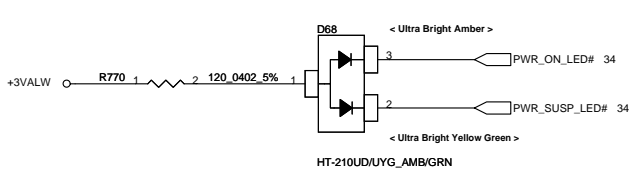
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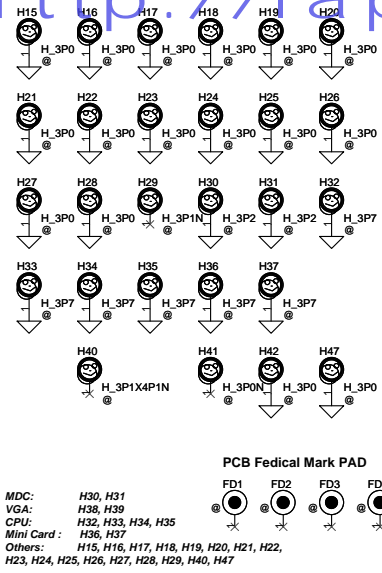
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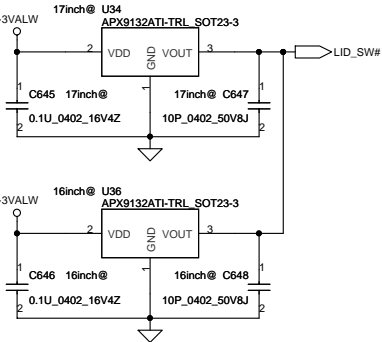
< POWER-ON & SUSPEND LED >



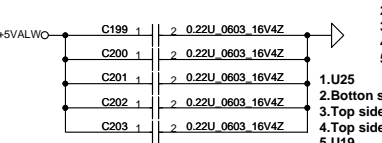
< Screw Hole >



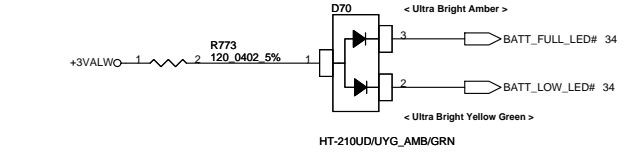
< LID Switch >



< EMI reserve >

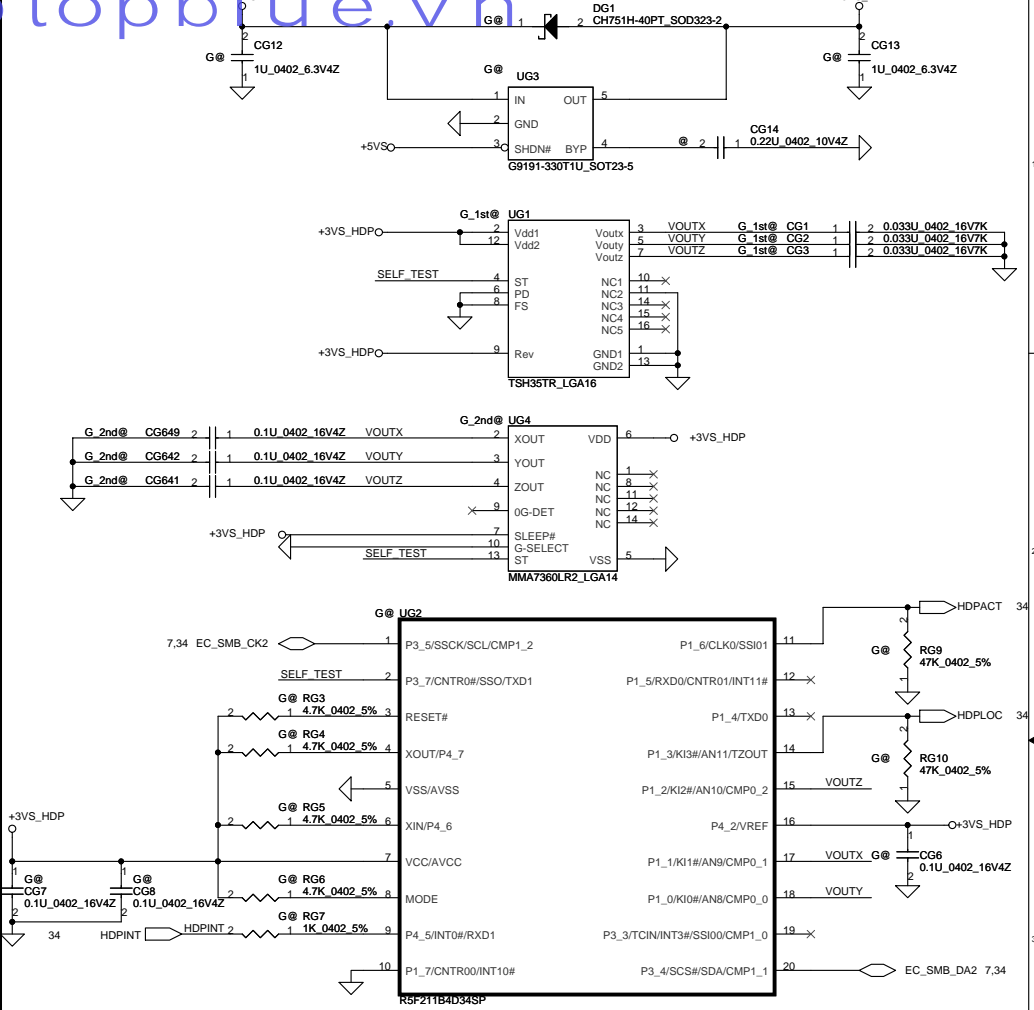


< BATT CHARGE/FULL LED >

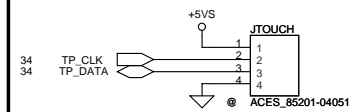


Vf=1.9V(typ),2.4V(max) for amber
Vf=2.0V(typ),2.4V(max) for green
If=30mA(max)

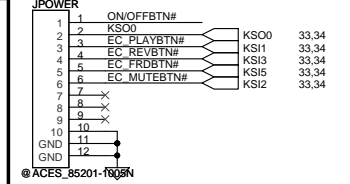
< G - Sensor >



< Touch/B Connector >

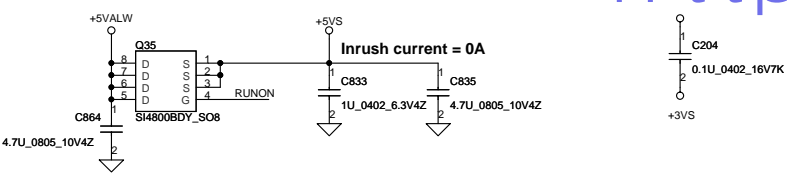


< SW/B Connector >



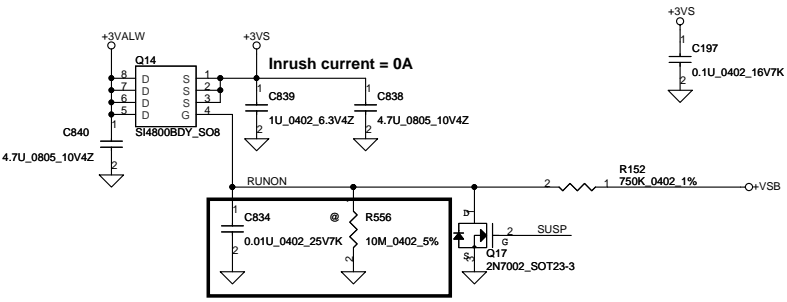
http://laptopblue.vn

< +5VALW TO +5VS >



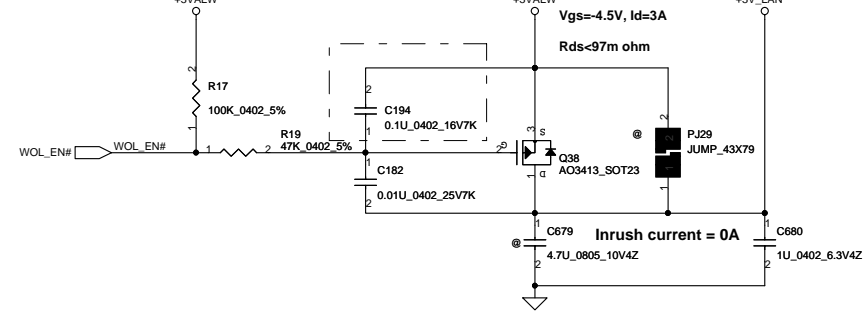
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< +3VALW TO +3VS >

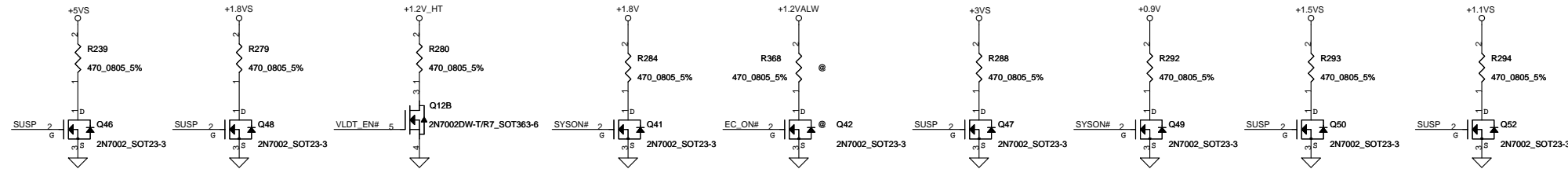


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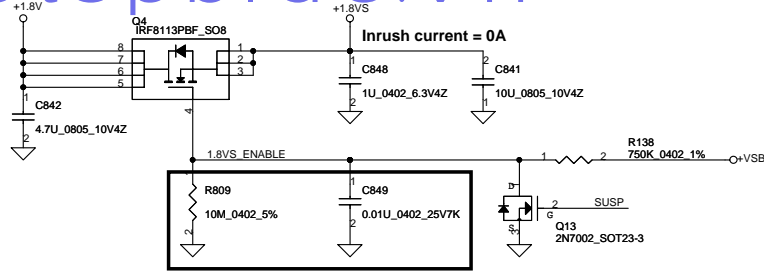
< +3VALW TO +3V_LAN >



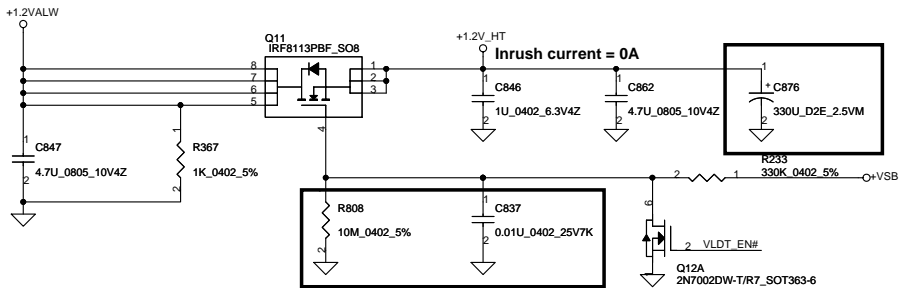
< Discharge circuit >



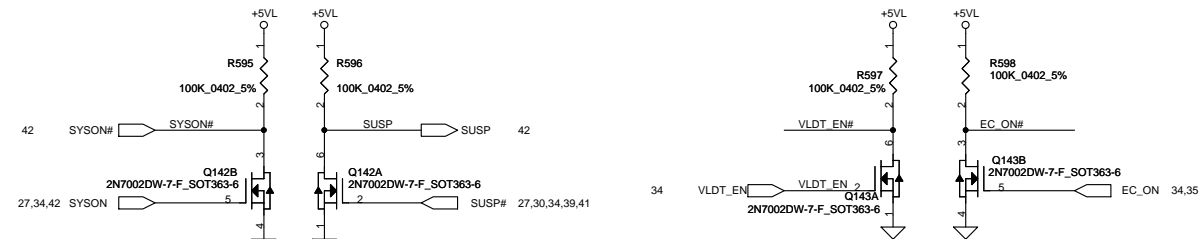
< +1.8V TO +1.8VS >



< +1.2VALW TO +1.2V_HT >



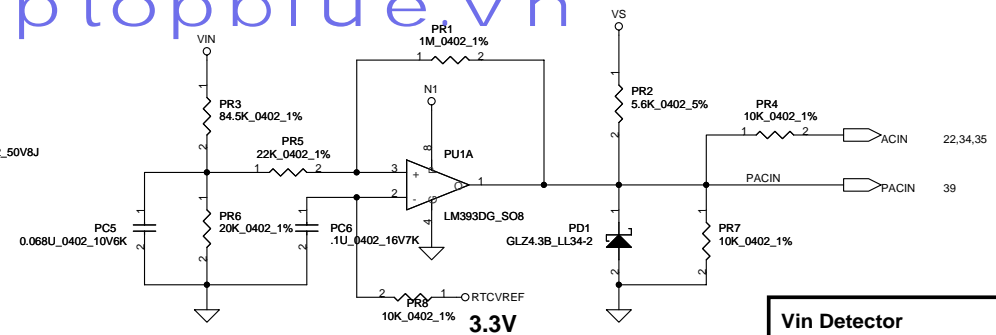
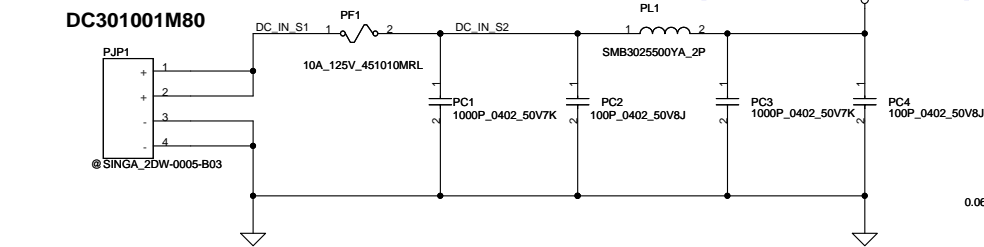
< Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >



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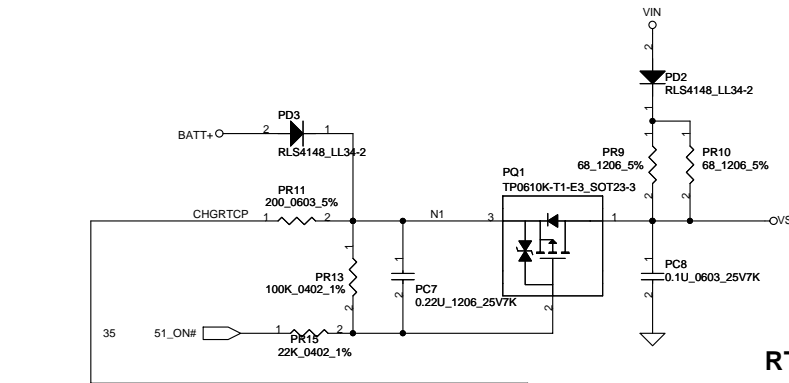
Schematic, MB LA-5332P

DC301001M80

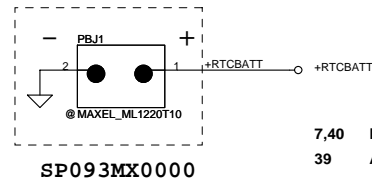


Vin Detector

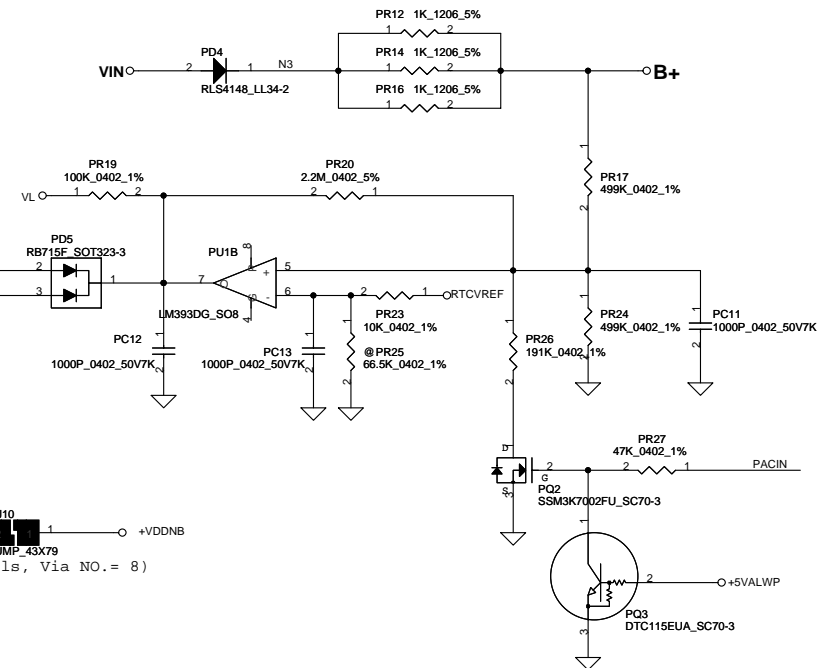
High 18.384 17.901 17.430
Low 17.728 17.257 16.976



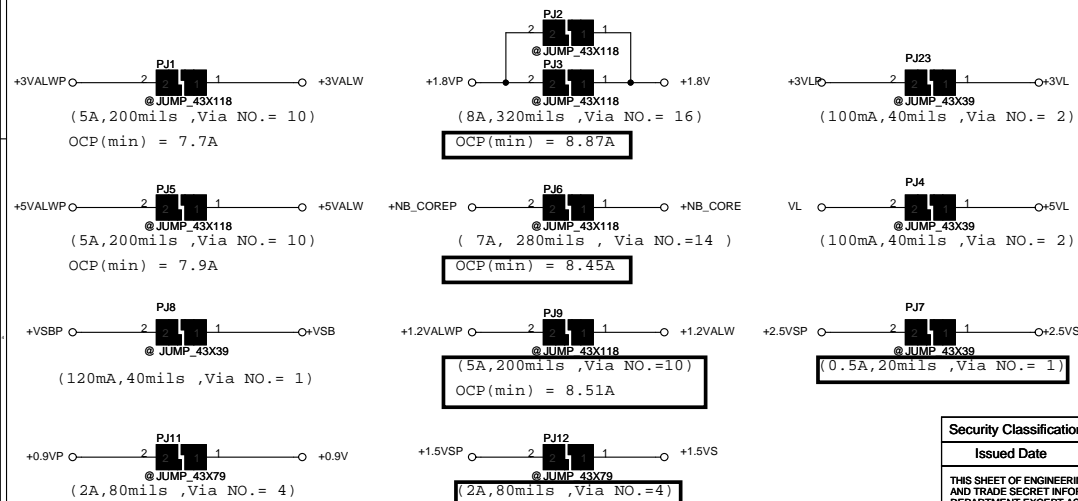
RTC Battery



SP093MX0000

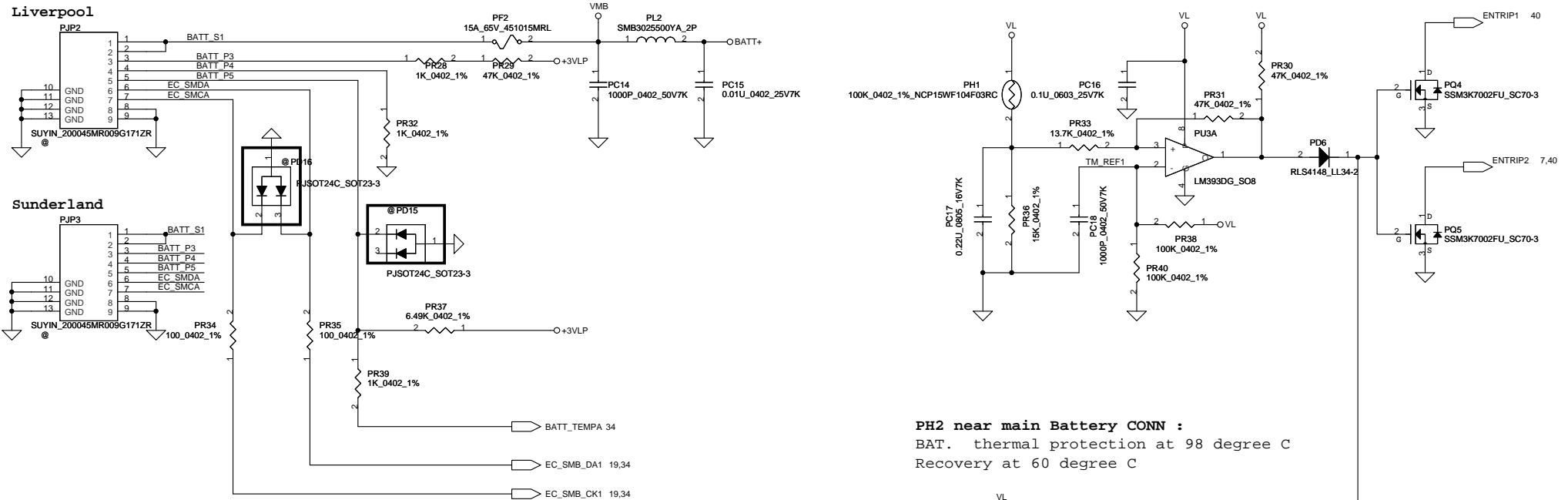


Precharge detector 15.97V/14.84V FOR ADAPTOR

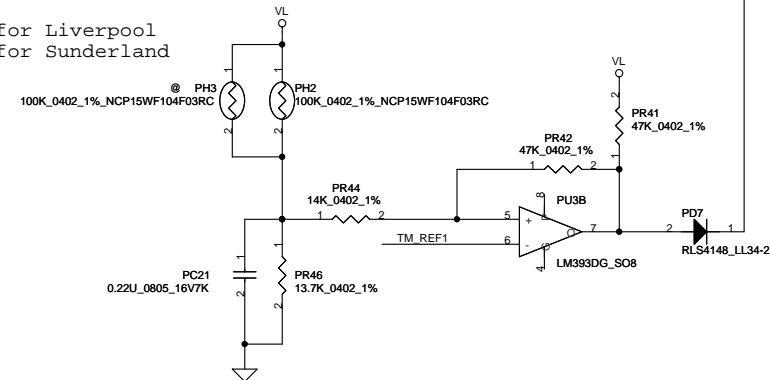


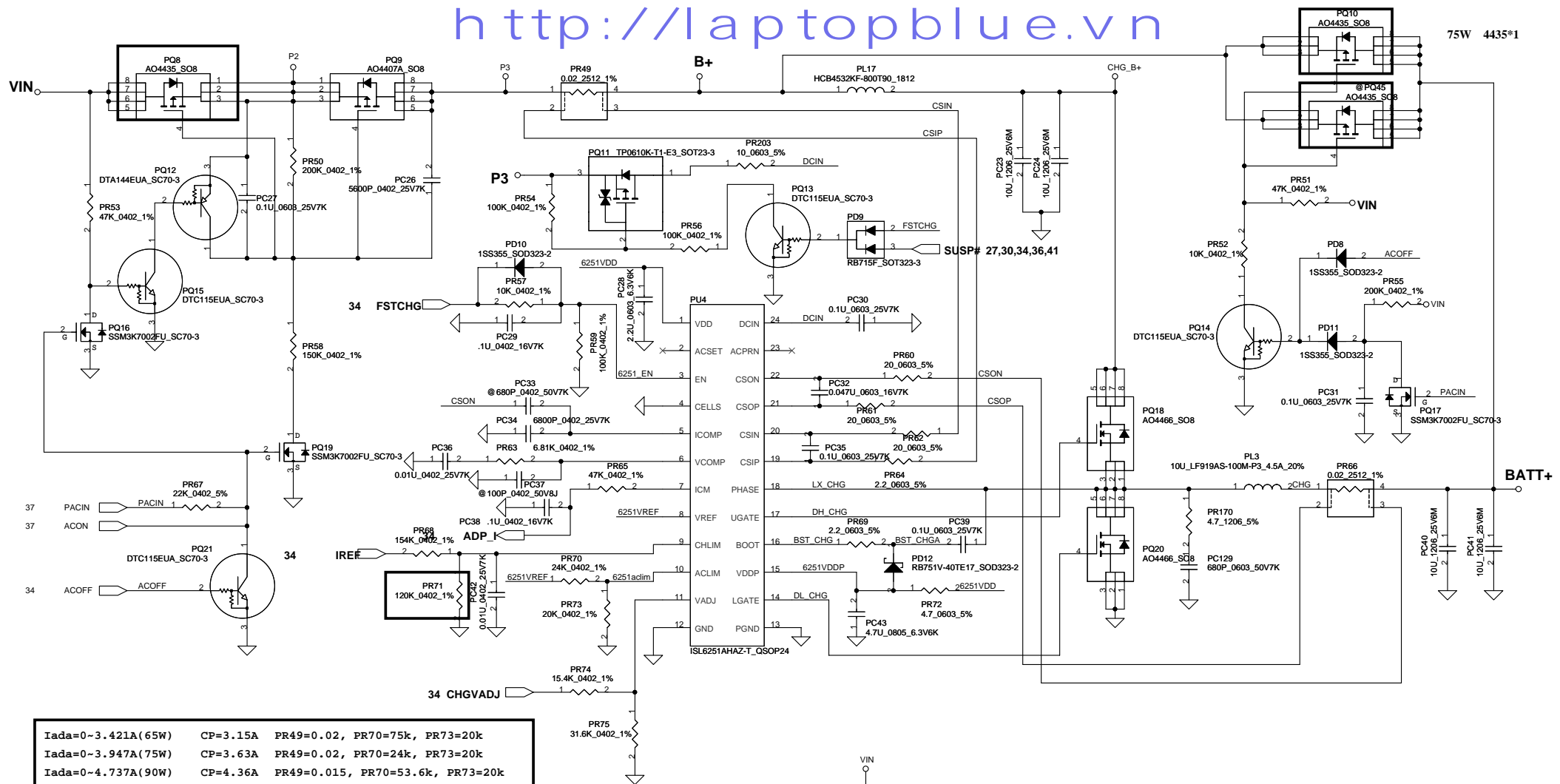
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PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 57 degree C



PH2 for Liverpool
PH3 for Sunderland





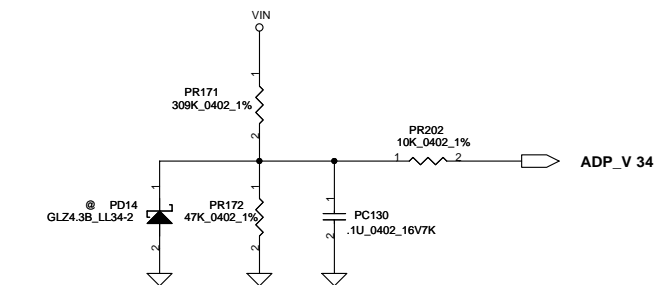
$I_{ada} = 0 \sim 3.421A (65W)$ $CP = 3.15A$ $PR49 = 0.02$, $PR70 = 75k$, $PR73 = 20k$
 $I_{ada} = 0 \sim 3.947A (75W)$ $CP = 3.63A$ $PR49 = 0.02$, $PR70 = 24k$, $PR73 = 20k$
 $I_{ada} = 0 \sim 4.737A (90W)$ $CP = 4.36A$ $PR49 = 0.015$, $PR70 = 53.6k$, $PR73 = 20k$
 $I_{ada} = 0 \sim 6.316A (120W)$ $CP = 5.81A$ $PR49 = 0.015$, $PR70 = 8.25k$, $PR73 = 26.7k$
 $CP = 92\% \cdot I_{ada}$

CP mode
 $V_{ac1m} = 2.39 \cdot (R_b / (152K) + (R_t / (152K + R_b) / (152K)))$
 $I_{input} = (1 / PR49) \cdot ((0.05 \cdot V_{ac1m}) / (2.39 + 0.05))$
 where $V_{ac1m} = 1.09986V$, $I_{input} = 3.65A$
 $V_{ac1m} = 0.7717V$, $I_{input} = 4.41A$
 $V_{ac1m} = 0.4204V$, $I_{input} = 5.88A$

$CC = 0.25A \sim 3A$
 $I_{REF} = 1.016 \cdot I_{charge}$
 $I_{REF} = 0.254V \sim 3.048V$
 V_{CHLIM} need over 95mV

CHGVADJ = (Vcell - 4) / 0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

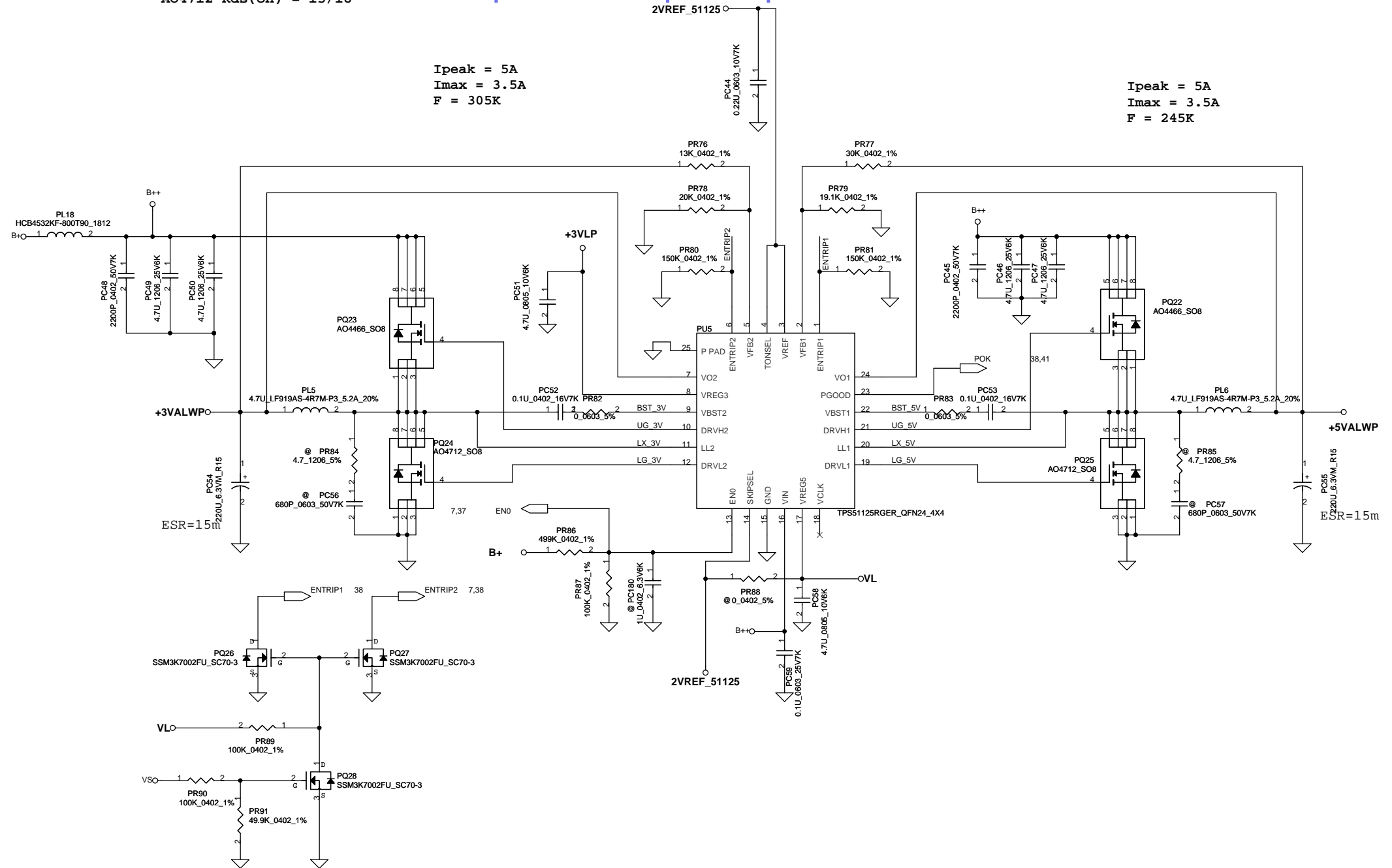
CELLS	VDD	GND	Float
CELL number	4	3	2



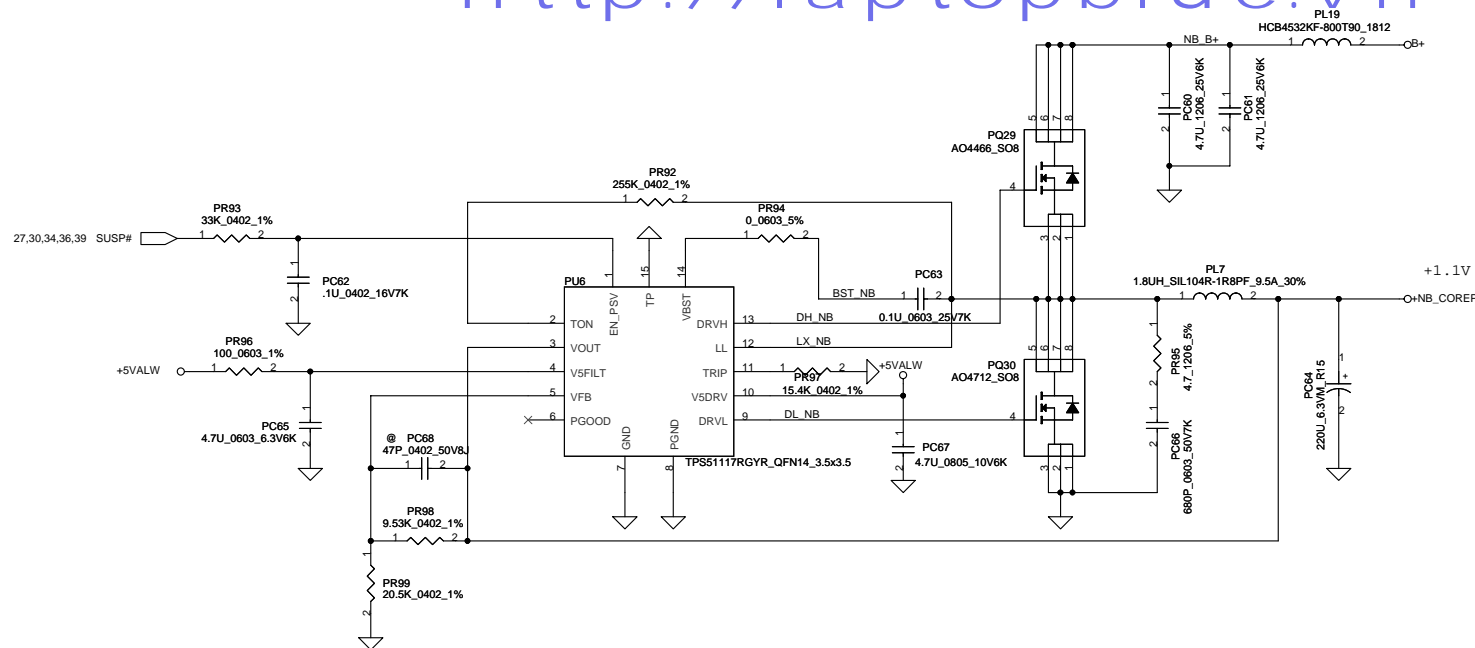
AO4712 $R_{ds(on)} = 15/18$

$I_{peak} = 5A$
 $I_{max} = 3.5A$
 $F = 305K$

$I_{peak} = 5A$
 $I_{max} = 3.5A$
 $F = 245K$

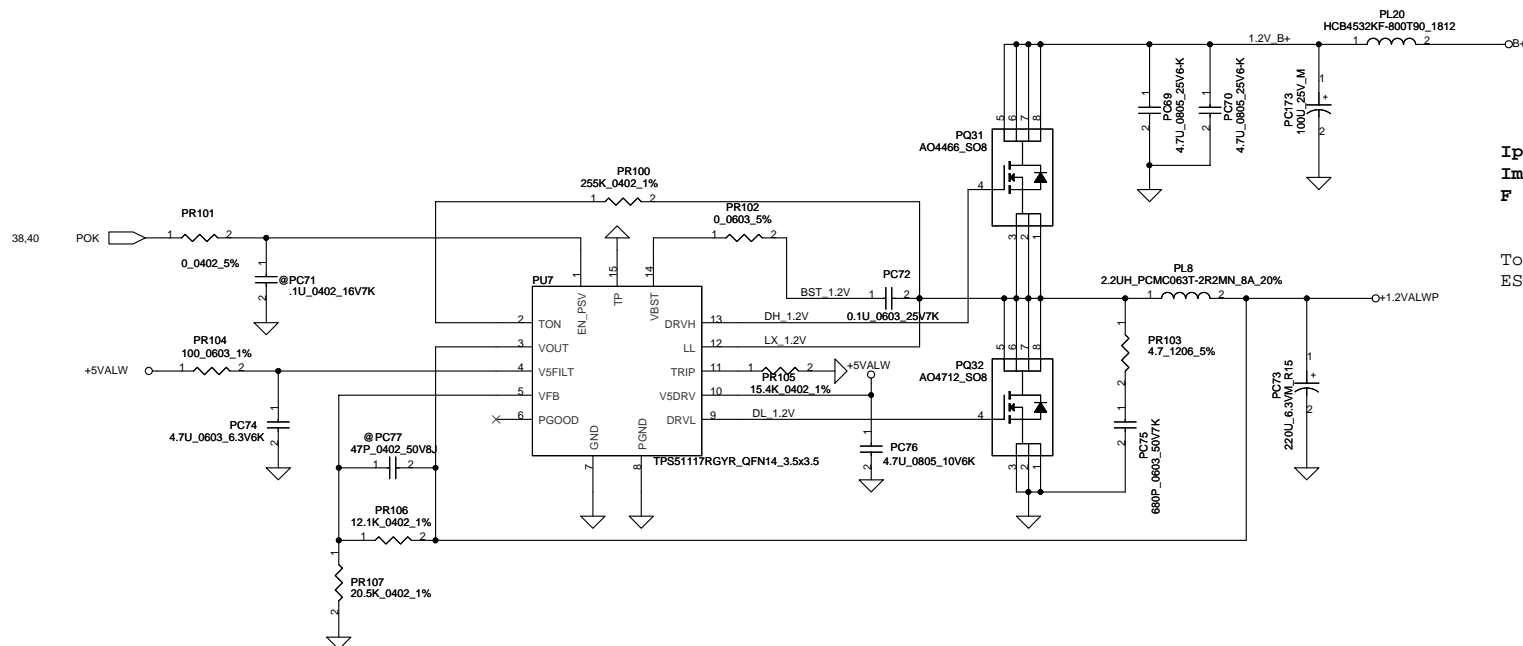


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I_{peak} = 7A
I_{max} = 4.9A
F = 315K

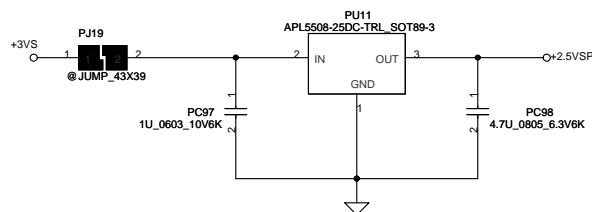
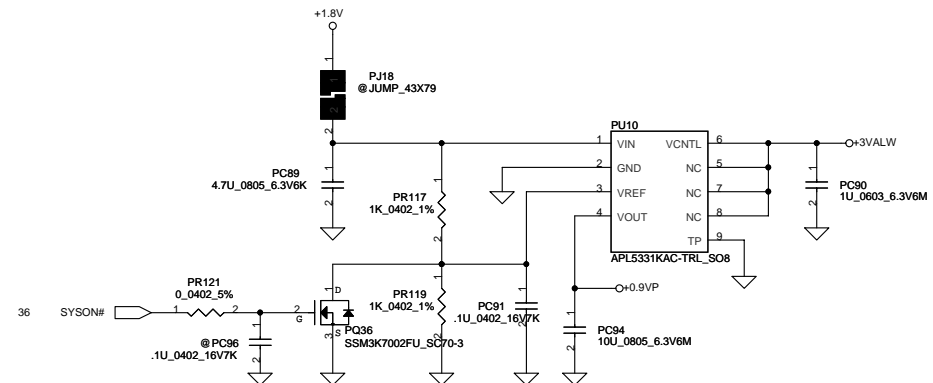
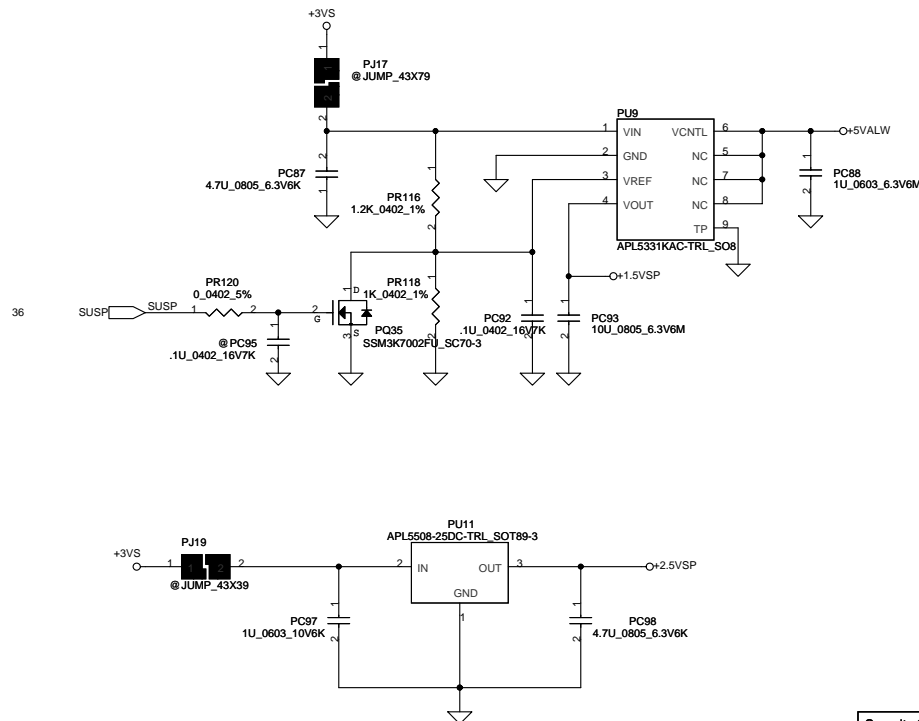
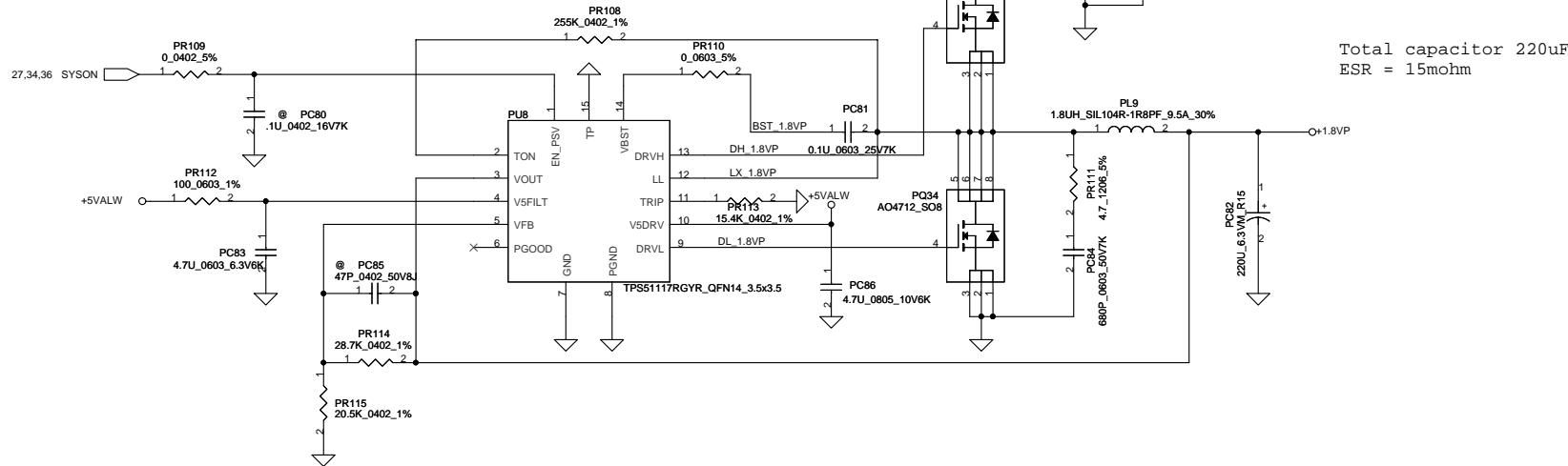
Total capacitor 550uF
ESR = 7.5mohm



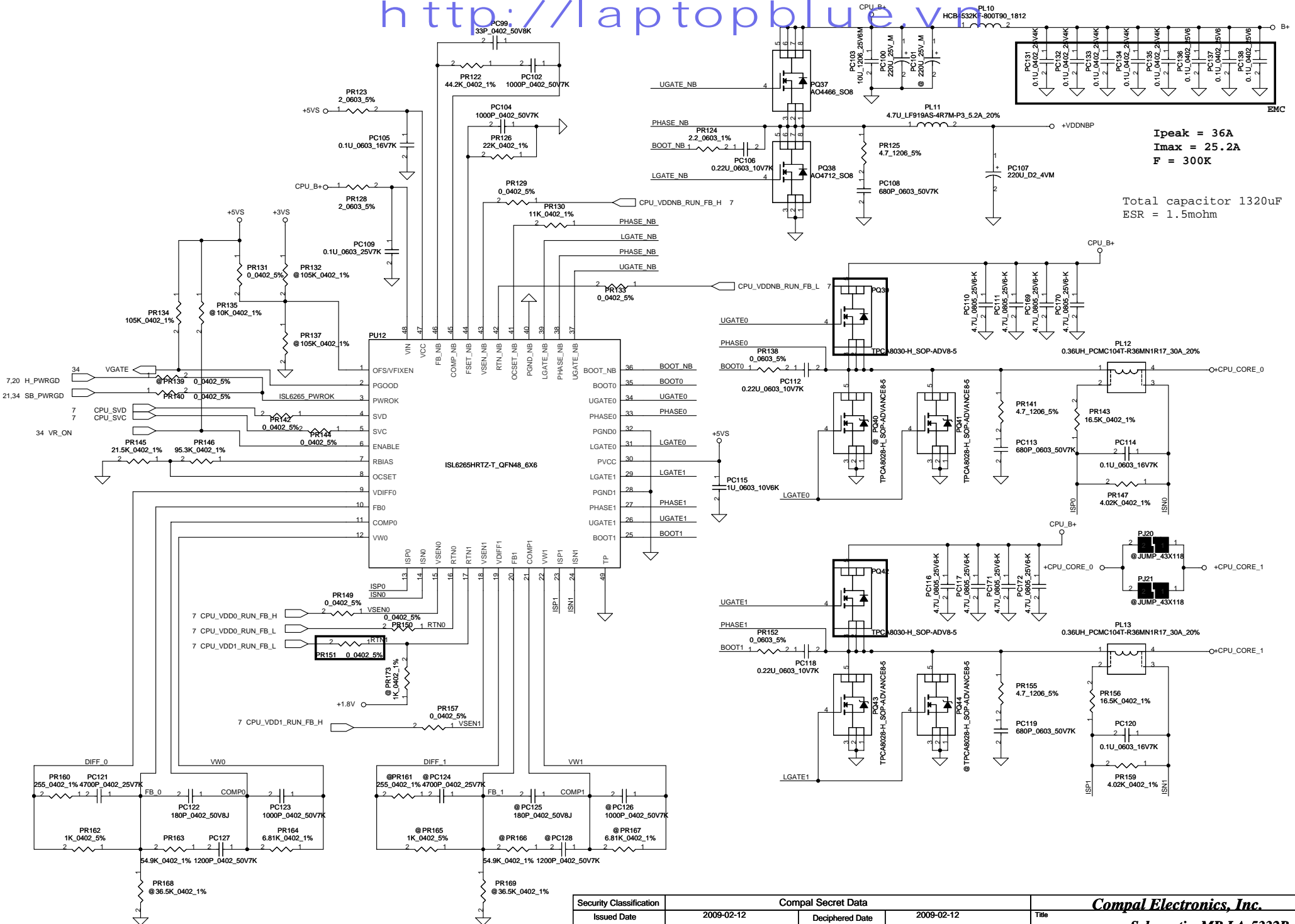
I_{peak} = 5A
I_{max} = 3.5A
F = 315K

Total capacitor 220uF
ESR = 15mohm

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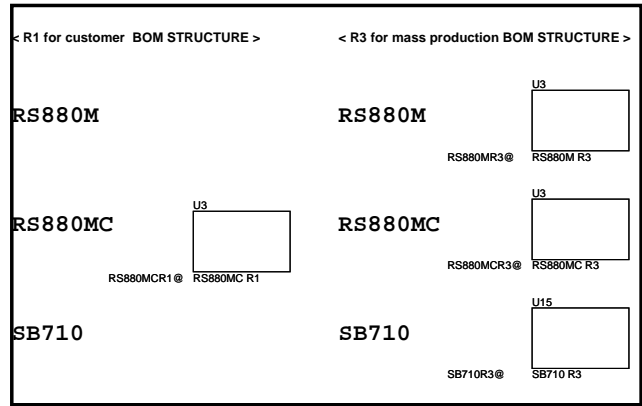
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Version Change List (P. I. R. List) for Circuit

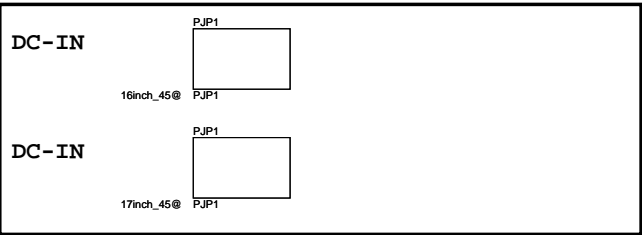
http://laptopblue.vn

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.																																				
1.	2009/02/26	--> Change D36 from ROHM to PANJI				55. 2009/11/24 --> Modify R195, R195 BOM structure for RS880M UMA with non-HDMI function																																					
2.	2009/02/26	--> Remove H38, H39																																									
3.	2009/02/27	--> Change the footprint of T9, T10, T11, T12, T19, T20 from TPC12 to TPC24																																									
4.	2009/02/27	--> Change 5V power of LCD connector																																									
5.	2009/03/02	--> Unmount D17, R965 and mount R966																																									
6.	2009/03/02	--> Unmount R556																																									
7.	2009/03/05	--> Change side-port memory to Hynix SA00002UH00																																									
8.	2009/03/05	--> Change RA16 from 5% to 1%																																									
9.	2009/03/10	--> Change R146 from 100k ohm to 10k ohm																																									
10.	2009/03/10	--> Change Y2 from SJ114P3M730 to SJ114P3MG00																																									
11.	2009/03/11	--> Change C686, C699, C702, C705, C706, C708, CA27 from SE074221K00SE to SE074221K80 for Green part																																									
12.	2009/03/11	-->Change LAN_WAKE# & EC_SWI#																																									
13.	2009/03/12	--> Unmount USB sleep & charge, add R112 & R113																																									
14.	2009/03/12	--> Unmount HDMI CEC controller and related components.																																									
15.	2009/03/12	--> Connect USB_OC#0 to LAN_WAKE# through 0 ohm																																									
16.	2009/03/12	--> Change H42 from NPH to PH																																									
17.	2009/03/24	--> Change F2 footprint to F_MINISMDC110F-2																																									
18.	2009/03/24	--> Add R370 & R381																																									
19.	2009/03/24	--> Change R557's BOM structure from H@ to @																																									
20.	2009/03/24	--> Change R440 from 0 ohm to 100k ohm																																									
21.	2009/04/06	--> Remove PCMCIA page and function																																									
22.	2009/04/06	--> Add RM8 100K ohm																																									
23.	2009/04/06	--> Change R440 from 100K ohm to 0 ohm for Askey BT module																																									
24.	2009/04/06	--> Change C480's BOM structure from BT@ to @																																									
25.	2009/04/10	--> Add C876 for power noise issue																																									
26.	2009/04/10	--> Add D20 for power noise issue																																									
27.	2009/04/10	--> Replace PJ13, PJ30, PJ14, PJ15, PJ16 by PL17, PL18, PL19, PL20, PL21																																									
28.	2009/04/20	--> Change D12's BOM structure to @																																									
29.	2009/04/22	--> Change C876 & C234 PN from 330u to 470u (SGA00001U00) for Power noise issue																																									
30.	2009/04/28	--> Add PCMCIA function on page 27																																									
31.	2009/04/29	--> Change R42's BOM structure to @																																									
32.	2009/05/06	--> Change C876 & C234 from 470u to 330u for COST reduce																																									
33.	2009/05/07	--> Mount R367 for can't power on issue (AMD SB leakage)																																									
34.	2009/05/18	--> Change RA38's BOM structure from LVDSSET @ to @																																									
35.	2009/05/19	--> Change C876 from SGA00001Q80 to SGA19331D00																																									
36.	2009/05/19	--> Add C618 & C619 for EMI request																																									
37.	2009/06/03	--> Change PJP9 to L90 (SM010024220) for EMI request																																									
38.	2009/06/03	--> Add C120 for EMI request																																									
39.	2009/06/03	--> Add C618, C619 for EMI reserve																																									
40.	2009/06/03	--> Combine camera with LVDS Delete R430, R428, R20, R18, C744, JCAM																																									
41.	2009/06/03	--> Change BOM structure of RA31 and CA34 from @ to mount for EMI require																																									
42.	2009/06/03	--> Add CA58 for EMI reserve																																									
43.	2009/06/03	--> Delete JPWR1 for ME portion																																									
44.	2009/06/04	--> Change UL3 from SP050005V00 to SP050005W00 (for AP issue)																																									
45.	2009/06/10	--> Change R125 and R625 BOM Structure from @ to NSIDE@																																									
46.	2009/07/07	--> Change C643 and C652 value from 18P to 12P																																									
47.	2009/07/07	--> Change C350 from SF22001M200 to SF000001H00 as main source																																									
48.	2009/08/06	--> Change Y7 from SJ100003D00 to SJ132P7KW10 for green review																																									
49.	2009/08/11	--> Change RN3 BOM Structure from EXPCARD@ to always mount on and relocated to SB side (Page 20).																																									
50.	2009/09/21	--> Change CL26, CL27 from SE00000H180 to SE074102K80, due to shortage																																									
51.	2009/09/21	--> Change C9, C13, C70, C71, C83, C84, C95, C104, C120 from SE068102J80 to SE074102K80, due to main source shortage																																									
52.	2009/09/21	--> Change U34, U36 from SA00001WP00 to SA00003GI00, due to main source E3 code																																									
53.	2009/10/02	--> Delete RN2's BOM structure and move to SB side (Page 21).																																									
54.	2009/10/12	--> Change Q13,Q17 PN to SB770020010 for common use																																									
				<table><tr><td>Security Classification</td><td colspan="3">Compal Secret Data</td></tr><tr><td>Issued Date</td><td>2009-02-12</td><td>Deciphered Date</td><td>2009-02-12</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td></tr></table>			Security Classification	Compal Secret Data			Issued Date	2009-02-12	Deciphered Date	2009-02-12	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				<table><tr><td colspan="3">Title</td><td>Rev</td></tr><tr><td colspan="3">Compal Electronics, Inc.</td><td>C</td></tr><tr><td colspan="3">Schematic, MB LA-5332P</td><td></td></tr><tr><td>Size</td><td colspan="2">Document Number</td><td></td></tr><tr><td>Custom</td><td colspan="2">401721</td><td></td></tr><tr><td>Date:</td><td>Wednesday, February 24, 2010</td><td>Sheet</td><td>44 of 45</td></tr></table>	Title			Rev	Compal Electronics, Inc.			C	Schematic, MB LA-5332P				Size	Document Number			Custom	401721			Date:	Wednesday, February 24, 2010	Sheet	44 of 45
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< Tigris >



< DC Jack >



< PCB >

