

TE4 Block Diagram

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND1
LAYER 3 : IN1
LAYER 4 : VCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : GND2
LAYER 8 : BOT

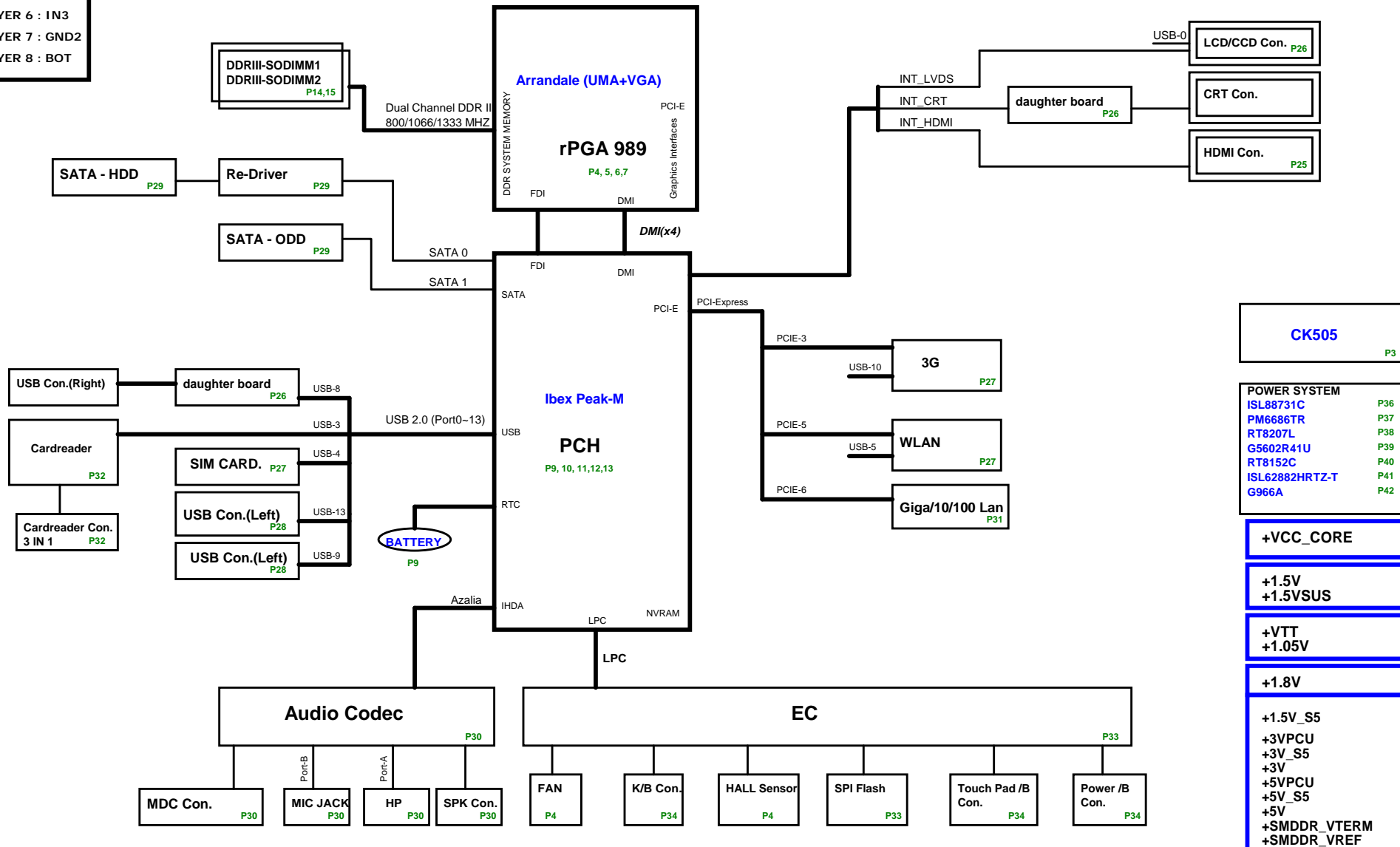







Table of Contents

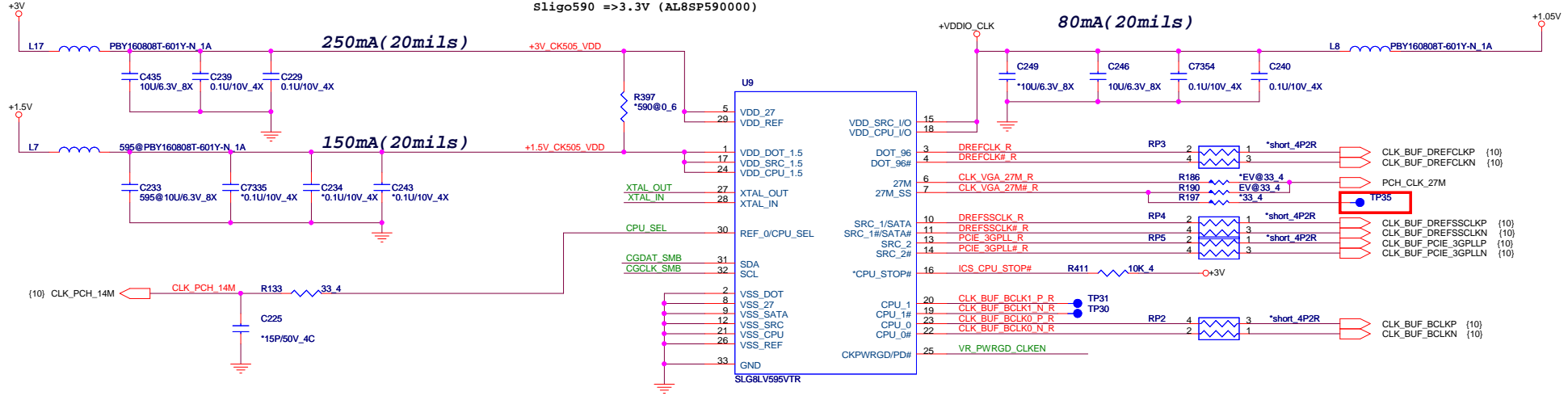
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3	Clock Gen
4-7	Processor
8	S3 Power Reduction
9-13	PCH
9	RTC
14-15	DDRIII SO-DIMM
25	HDMI comm part
26	LCD Panel
	CRT & CRT BUS SWITCH
	CCD
	HALL SENSOR&BACK LIGHT SWITCH
27	MINI Card (Wi-Fi & WIMAX)
	MINI Card 2nd
	MINI Card 3rd
28	USB 2.0
29	SATA ODD
	Main SATA HDD & 2nd SATA HDD
30	Codec (CX20587)
31	Atheros LAN
32	3 IN 1 Card reader
33	EC NPCE791L
34	INT Keyboard & K/B LED Power
	TP board
	Power SW
	HOLE
35	LED / EMI
36	Charger (ISL88731C)
37	System 5V/3V (PM6686TR)
38	DDR1.5V(RT8207L)/1.05VSUS
39	+VTT/+1.05V (G5602R41U)
40	VAXG_CORE RT8152C FOR UMA
41	+VCC_CORE(ISL62882HRTZ-T)
42	+1.8V (G966A)/Discharge

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0-S5
+VCCRTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0-S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		MPWROK	S0

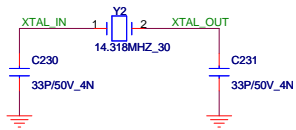
GND PLANE	PAGE
 8769AGND	33
 Audio_GND	30
 Shield_GND	30
 GND	ALL
 ISL95870A_AGND	30

CLOCK Gen [CLK]

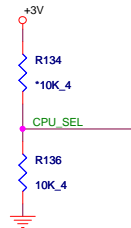
Pin1/17/24
Sligo595 =>1.5V (AL000595000)
Sligo590 =>3.3V (AL8SP590000)



CLK CRYSTAL

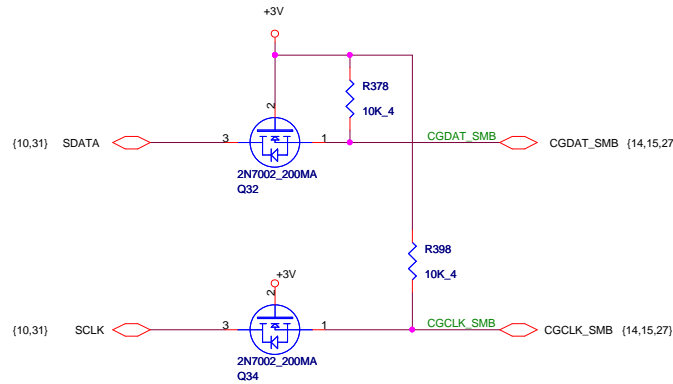


CLK CPU_SEL

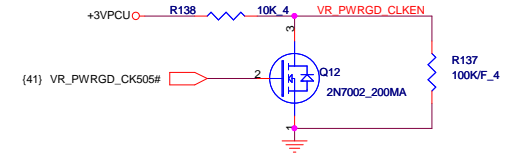


	0	1
CPU_SEL	CPU =133MHz (default)	CPU=100MHz

CLK I2C

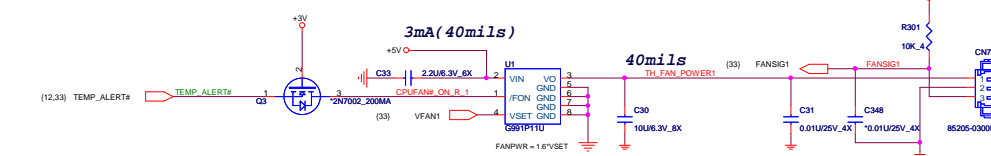
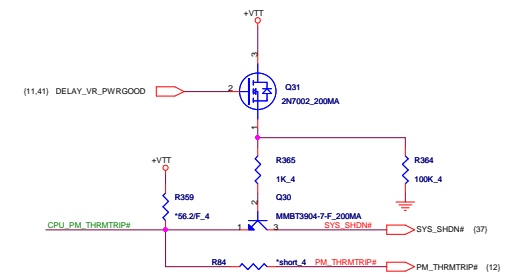
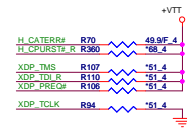
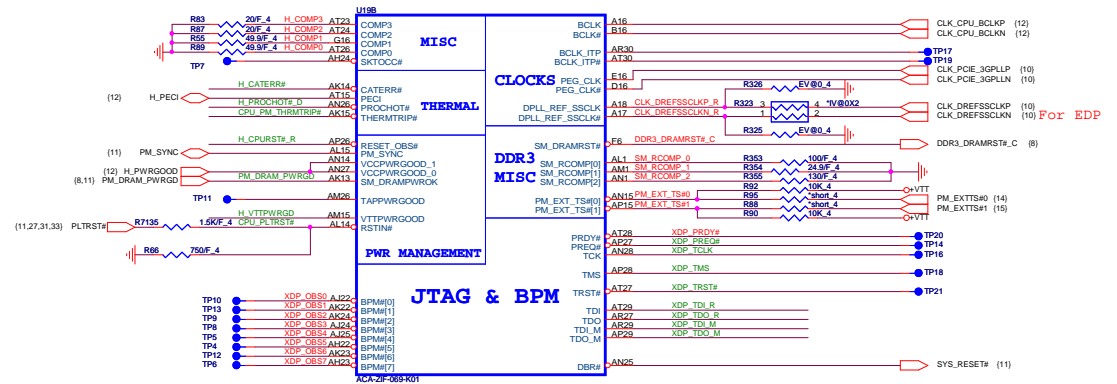


CLK POWERGOOD



Quanta Computer Inc.
PROJECT : TE4

Size	Document Number	Rev
	CLOCK GENERATOR	A1A
Date	Monday, January 24, 2011	Sheet 3 of 46

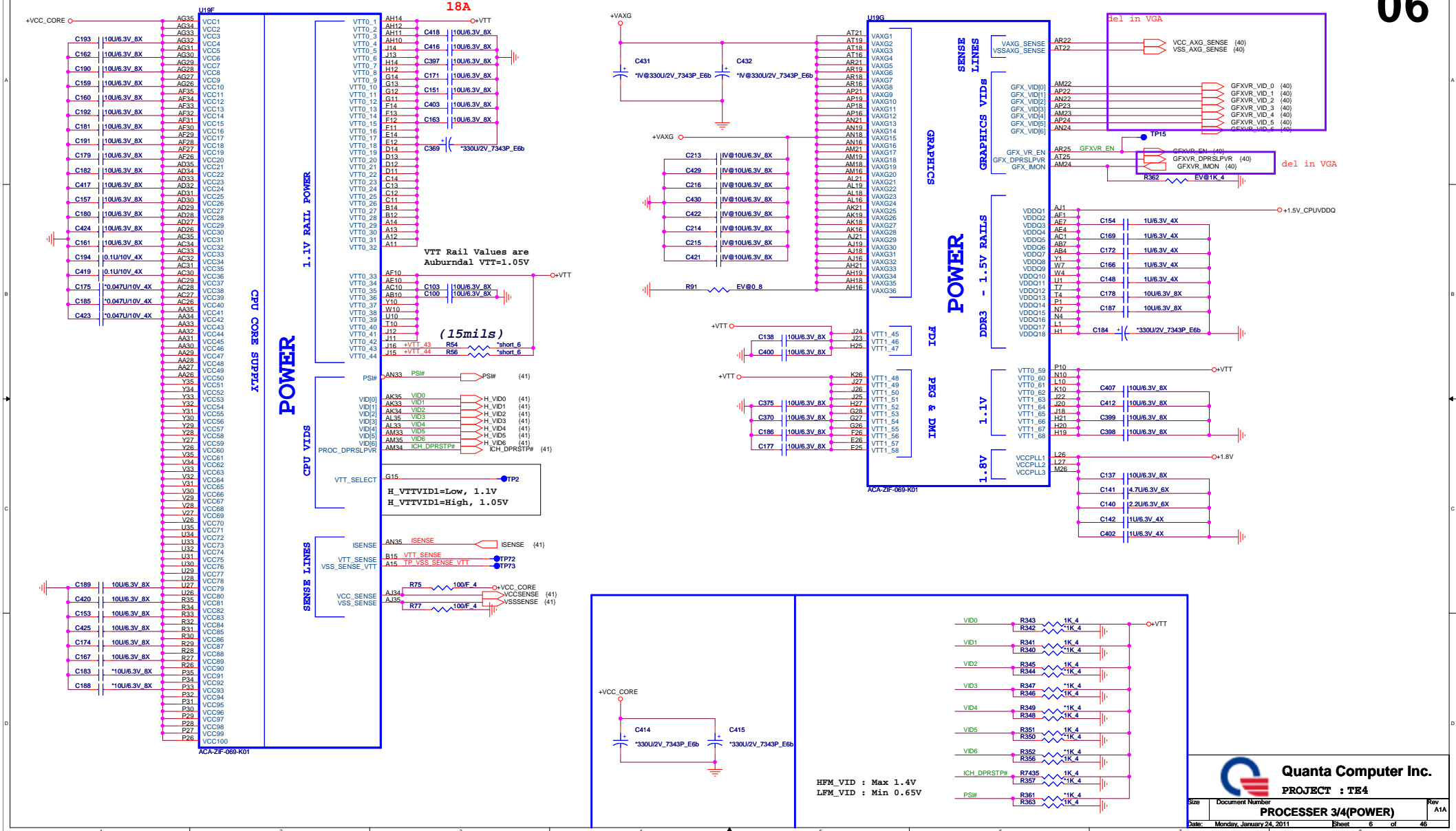


[illegible]

Quanta Computer Inc.

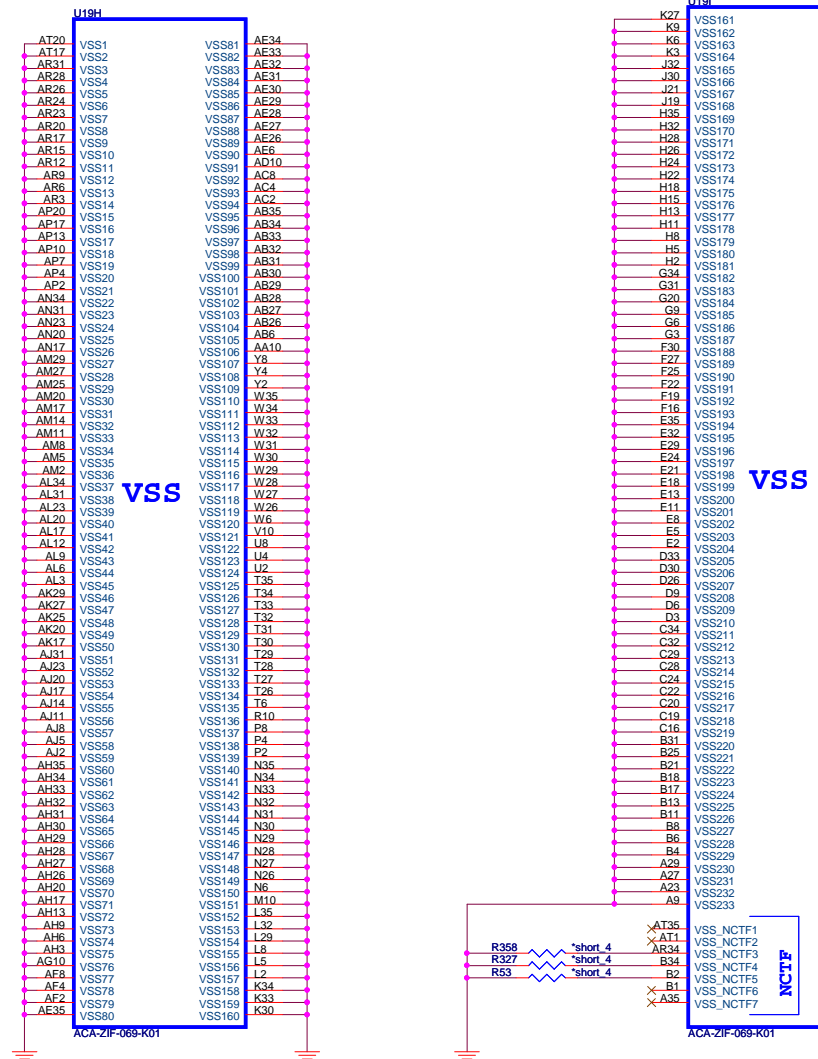
PROJECT : TE4

Size	Document Number	Rev
	PROCESSER 2/4(DDR)	A1A
Date:	Monday, January 24, 2011	Sheet 5 of 46

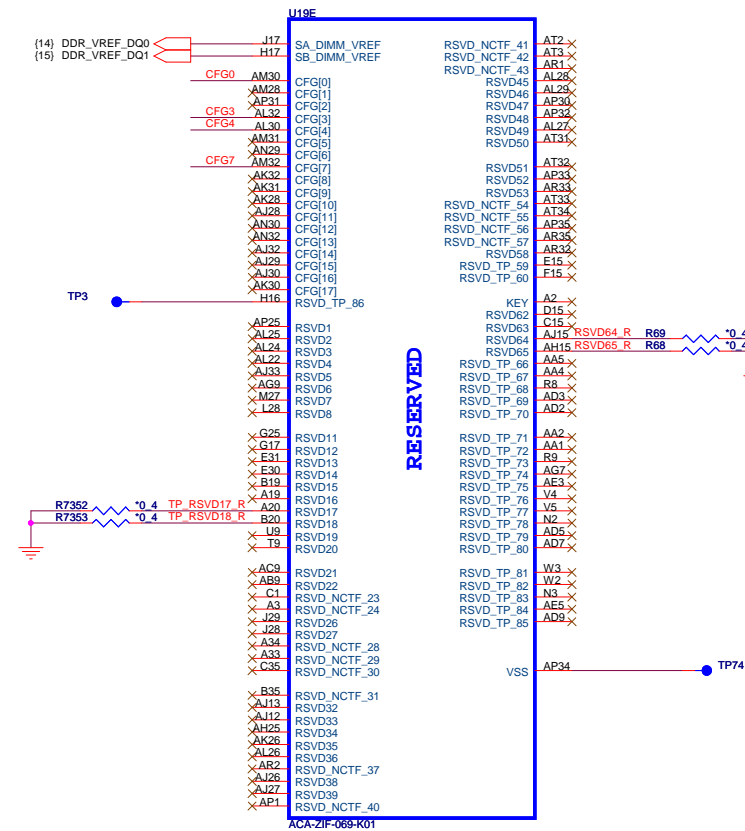


AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



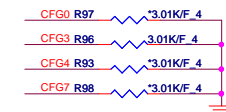
CFG[1:0] - PCI_Epress Configuration Select

* 11= 1 x 16 PEG

* 10= 2 x 8 PEG

For Discrete only

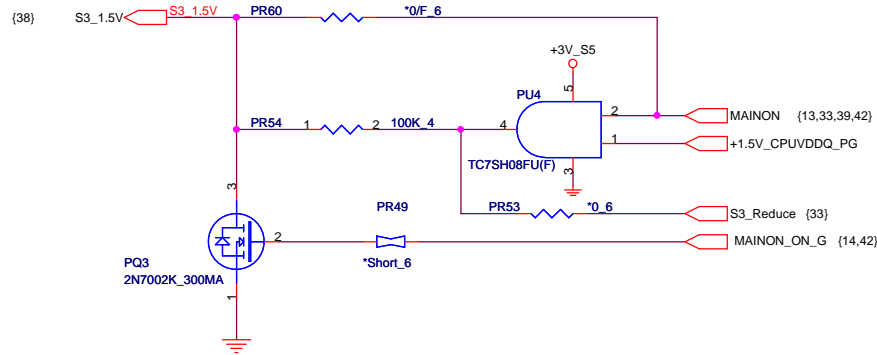
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1



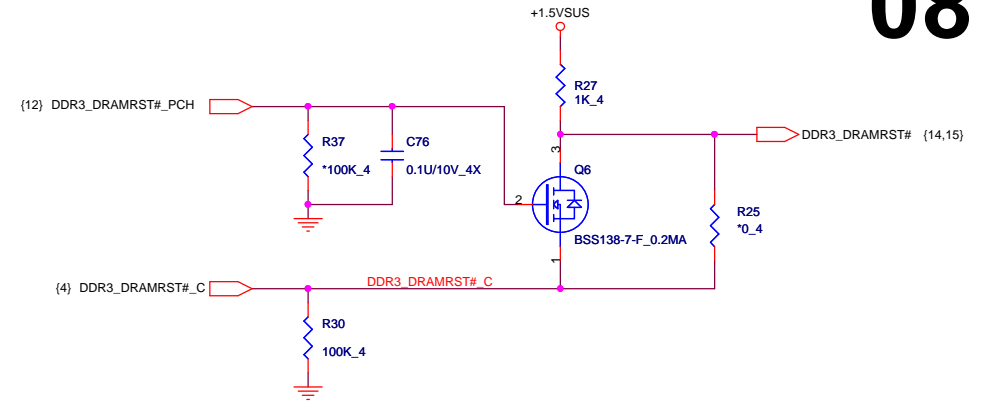
Quanta Computer Inc.
PROJECT : TE4

Size	Document Number	Rev
	PROCESSOR 4/4 (GND)	A1A
Date: Monday, January 24, 2011	Sheet 7 of 46	

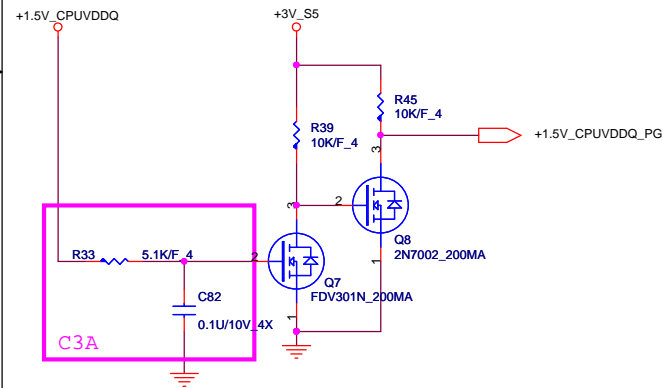
S3 Power Enable



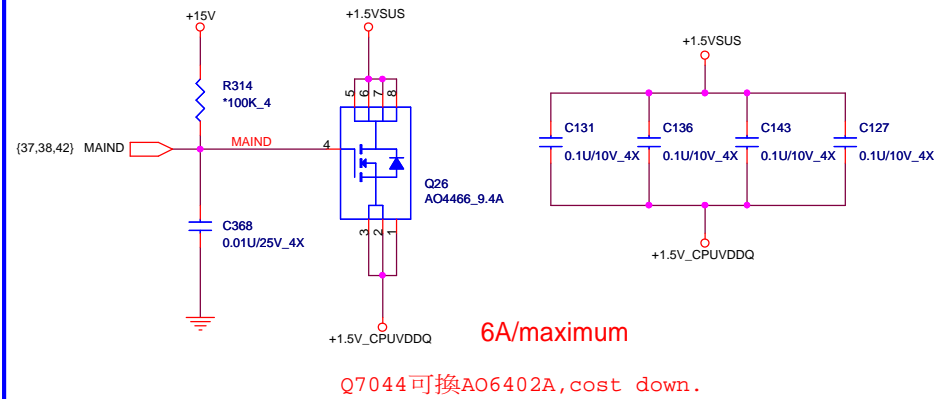
DRAM Reset



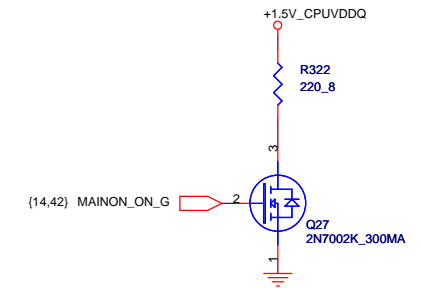
VDDQ Power Good



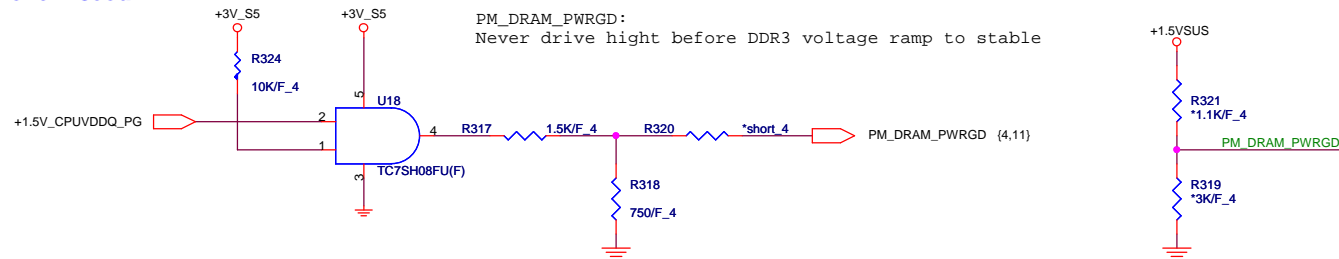
VDDQ Power Switch




VDDQ Discharge

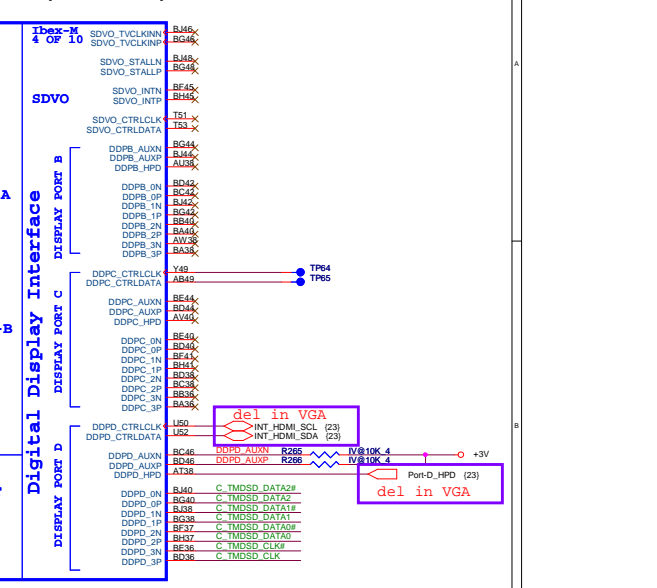
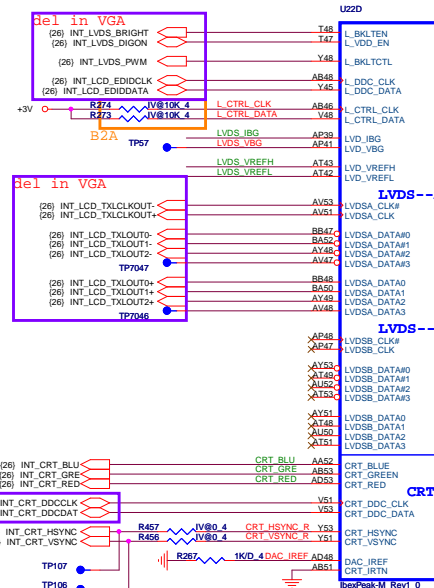


DRAM Power Good



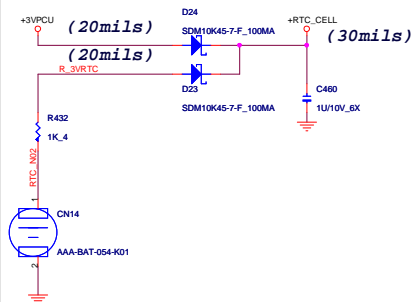
 Quanta Computer Inc. PROJECT : TE4		
Size	Document Number	Rev
	S3 Power Reduction	A1A
Date:	Monday, January 24, 2011	Sheet 8 of 46

IBEX PEAK-M (LVDS,DDI)



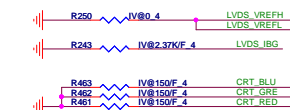
[RTC]

RTC BATTERY



DDP Setting

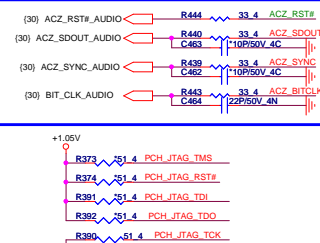
Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DDC_DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC



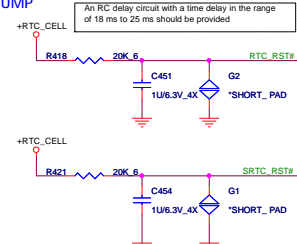
HDMI



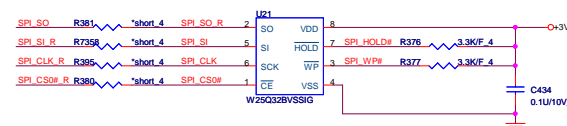
Alzia



RESET JUMP



4M byte SPI ROM



PCH	2MB	4MB	8MB
PM55	●		
HM55		●	
HM57/PM57		●	●
QM57/QS57			●

**Quanta Computer Inc.**

PROJECT : TE4

Rev	A1A
-----	-----

IBEX PEAK-M (PCI-E,SMBUS,CLK)



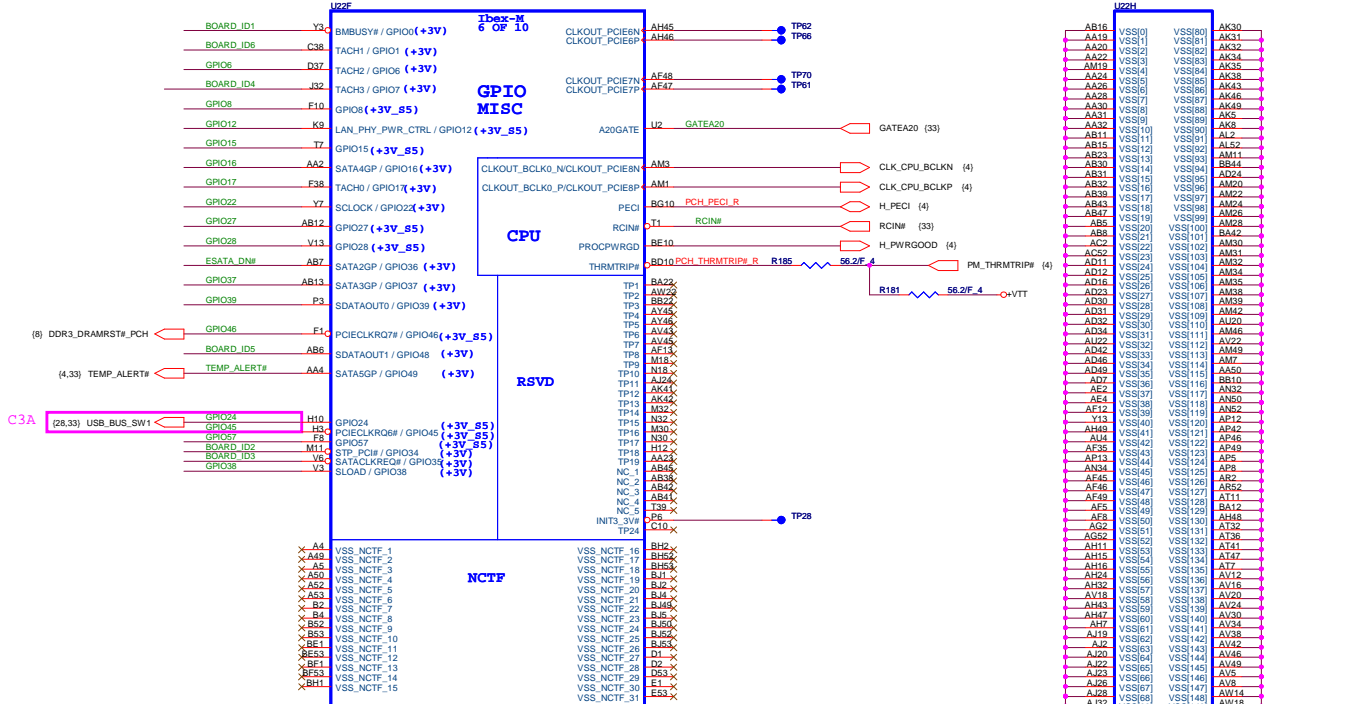
IBEX PEAK-M (DMI,FDI,GPIO)



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)

12



PCH Strap Pin Configuration Table

SPKR

(9,30) PCBEEP \rightarrow *1K/F 4 \rightarrow R388 \rightarrow +3V

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

GNT3# / GPIO55

(11) GNT3# \rightarrow R460 \rightarrow *10K/F 4 \rightarrow +3V

0 = Default Mode (Internal weak Pull-down)
1 = No Reboot Mode with TCO Disabled

HDA_DOCK_EN #GPIO33

(9,33) PCH_GPIO33 \rightarrow R237 \rightarrow 1K/F 4 \rightarrow JP1 \rightarrow *SHORT PAD \rightarrow +3V

0 = Top Block Swap Mode
1 = Default Mode (Internal pull-up)

GNT0#, GNT1#

(11) GNT0# \rightarrow R270 \rightarrow *1K/F 4 \rightarrow +3V
(11) GNT1# \rightarrow R271 \rightarrow *1K/F 4 \rightarrow +3V

Boot BIOS Strap		
PCH_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

SPI_MOSI

(9) SPI_MOSI \rightarrow R7355 \rightarrow *1K 4 \rightarrow +3V

NV_ALE

(11) NV_ALE \rightarrow R403 \rightarrow *10K 4 \rightarrow +1.8V

1 = Enabled
0 = Disabled (Default)

GPIO8

GPIO8 \rightarrow R149 \rightarrow *10K 4 \rightarrow +3V_S5

This signal has a weak internal pull up.
NOTE: This signal should not be pulled low

GPIO15

GPIO15 \rightarrow R128 \rightarrow *1K 4 \rightarrow +3V_S5

0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

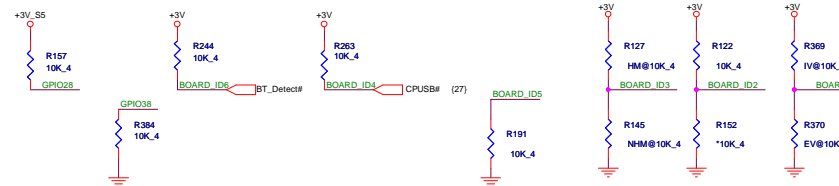
GPIO27

GPIO27 \rightarrow R182 \rightarrow *10K 4 \rightarrow +3V

0 = Disables the VccVRRM. Need to use on-board filter circuits for analog rails.
1 = Enables the internal VccVRRM to have a clean supply for analog rails.
No need to use on-board filter circuit.
This signal has a weak internal pull-up.

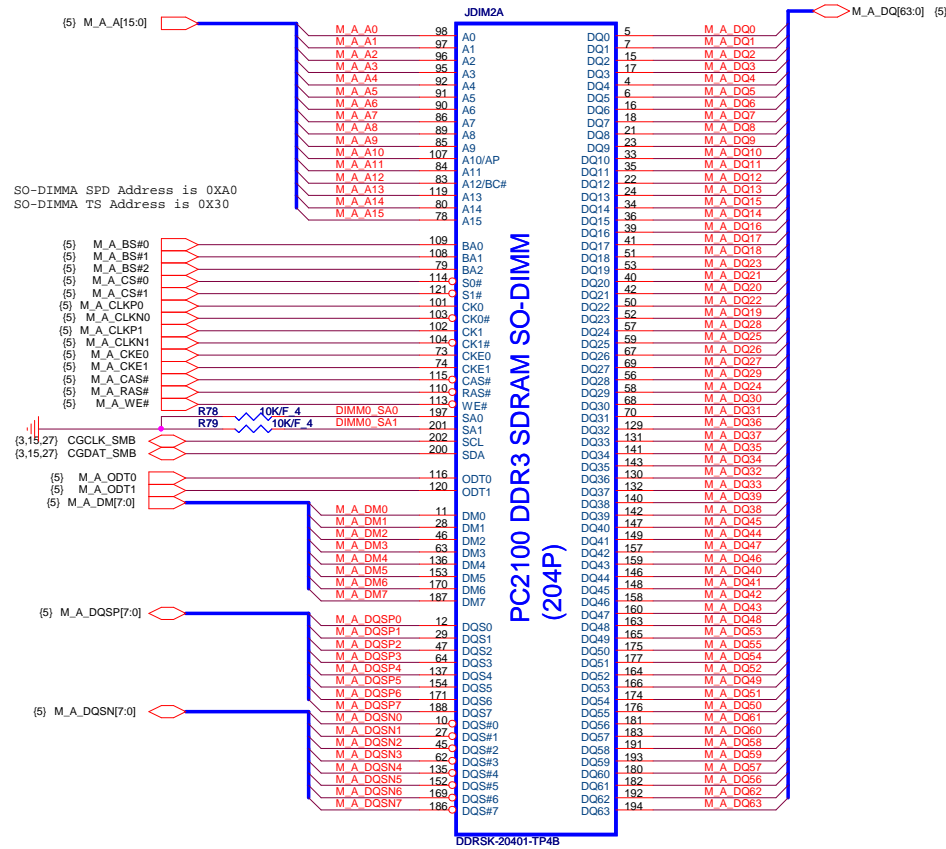
BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	GPIO28	GPIO38
UMA SKU	H	L						
VGA SKU								
W/ MDC		H						
W/O MDC		L						
W/ HDMT			H					
W/O HDMT			L					
W/O 3G				H				
W/ 3G				L				
15"					H			
14"					L			
W/O BT						H		
W/ BT						L		
14 or 15							H	
13							L	
Old HW(2010)								H
New HW(2011)								L



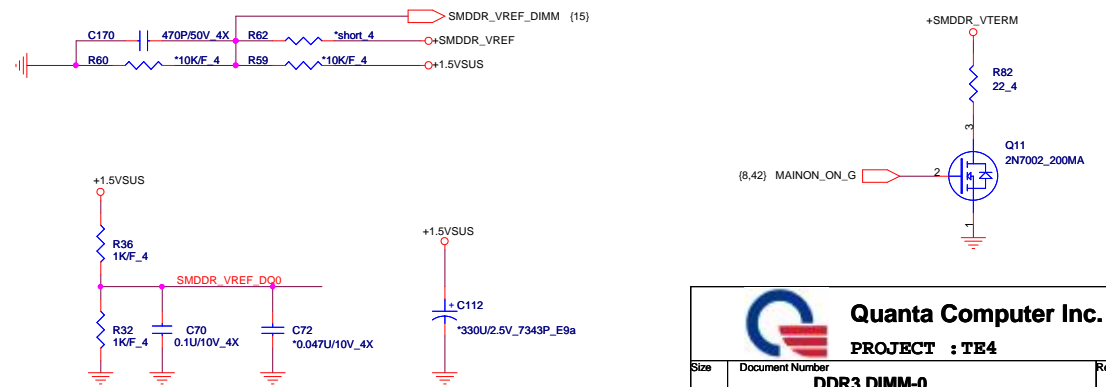
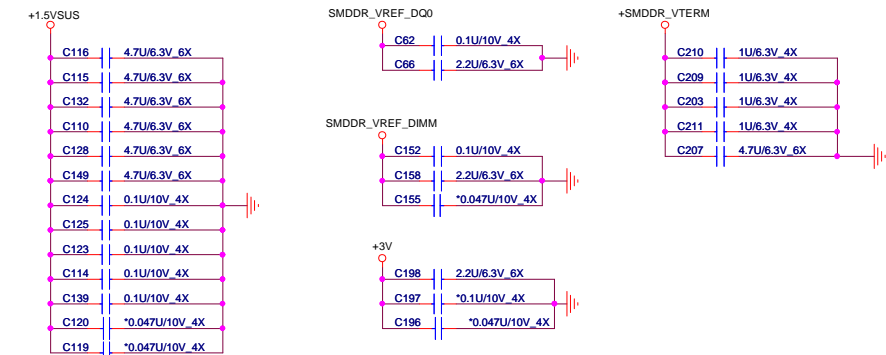


H=4

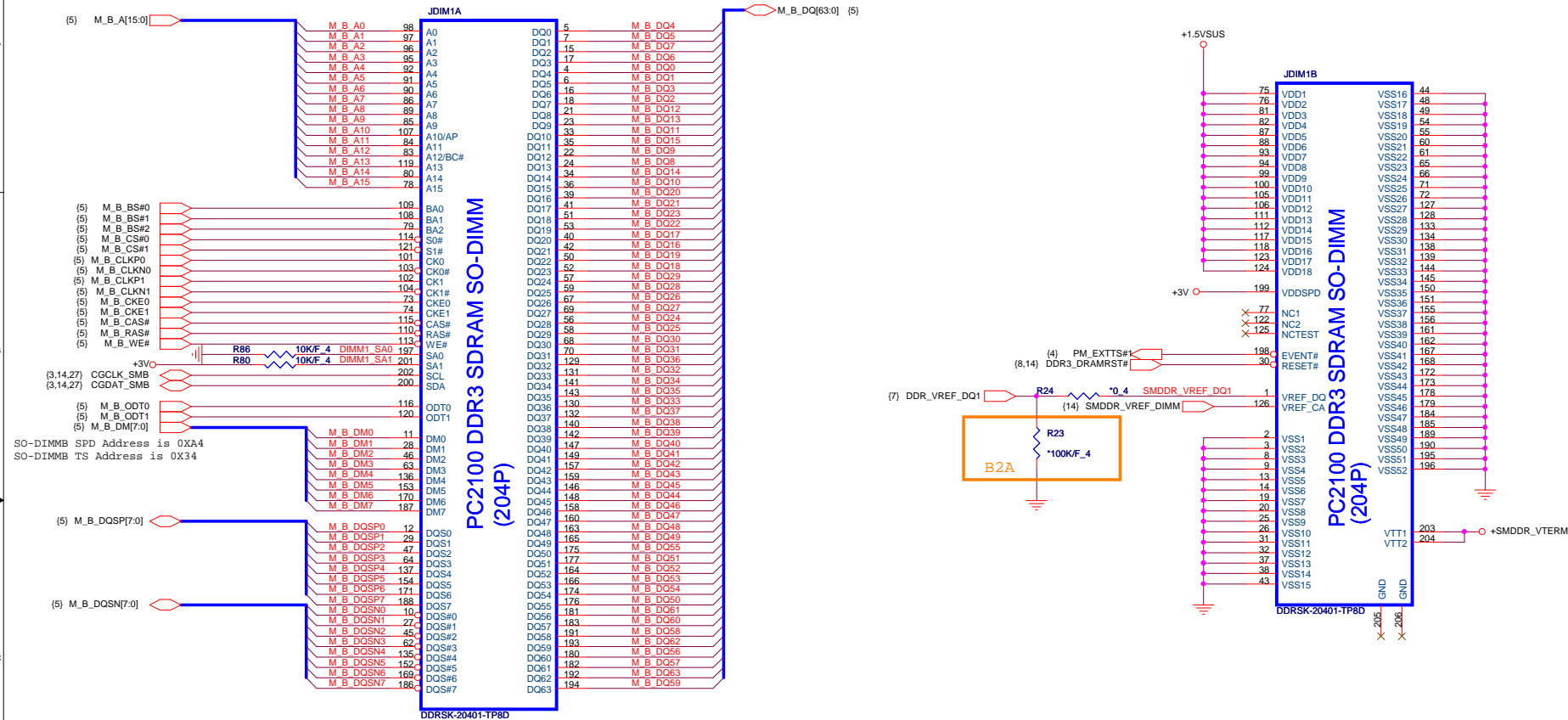


Place these Caps near So-Dimm0.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%

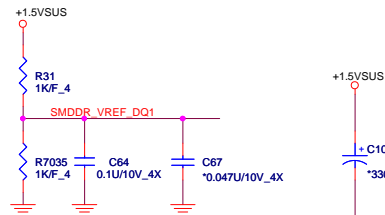
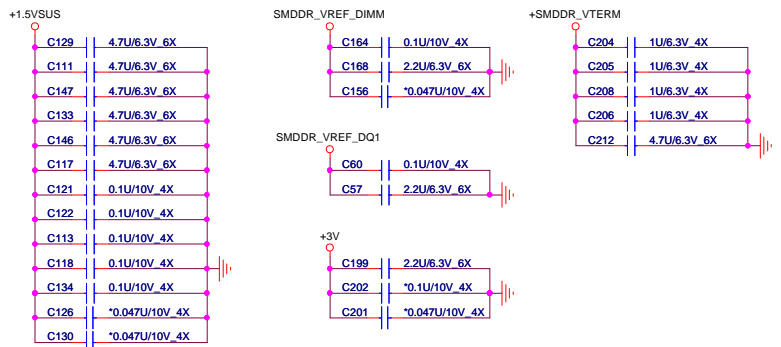


H=8



Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%

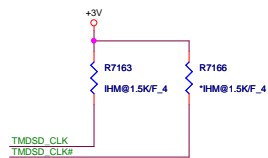


Quanta Computer Inc.
PROJECT : TE4

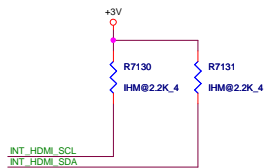
Size	Document Number	Rev
	DDR3 DIMM-1	A1A
Date:	Monday, January 24, 2011	Sheet 15 of 46

Display Port Enable

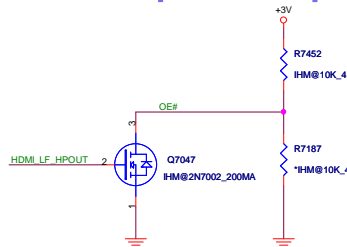
[HDM]



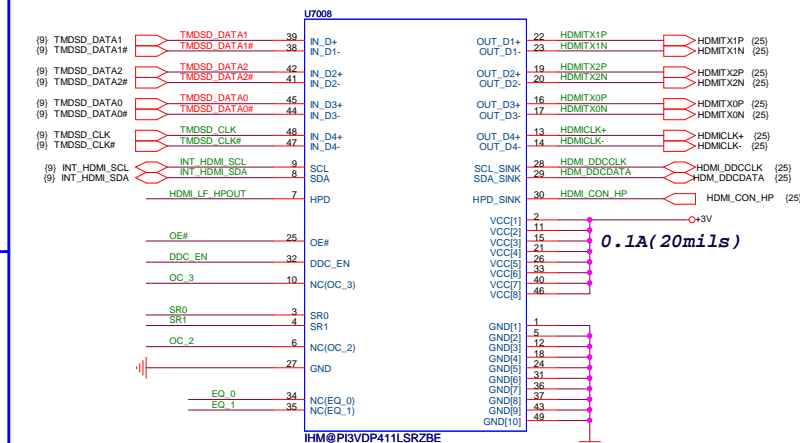
I2C PU



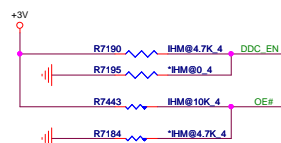
LEVEL SHIFT ENABLE



HDMI LEVEL SHIFT (UMA)



LEVEL SHIFT SETTING



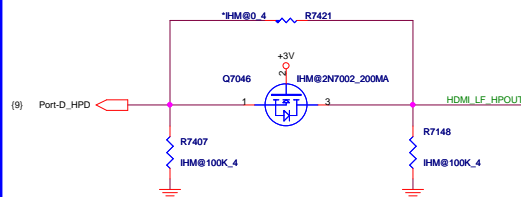
Slew Rate Control Function

SR1	SR0	Rise/Fall Time
1	1	140ps
1	0	130ps
0	1	120ps
0	0	110ps

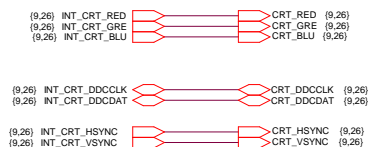
Reserve



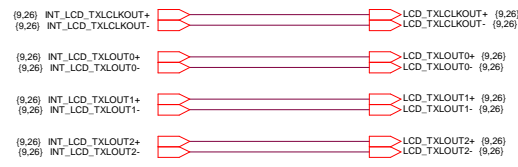
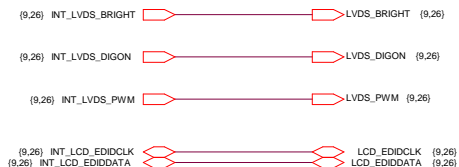
Hot Plug Detector (UMA)



CRT (UMA)

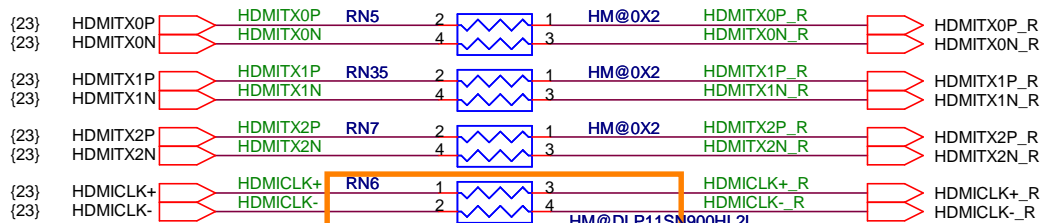
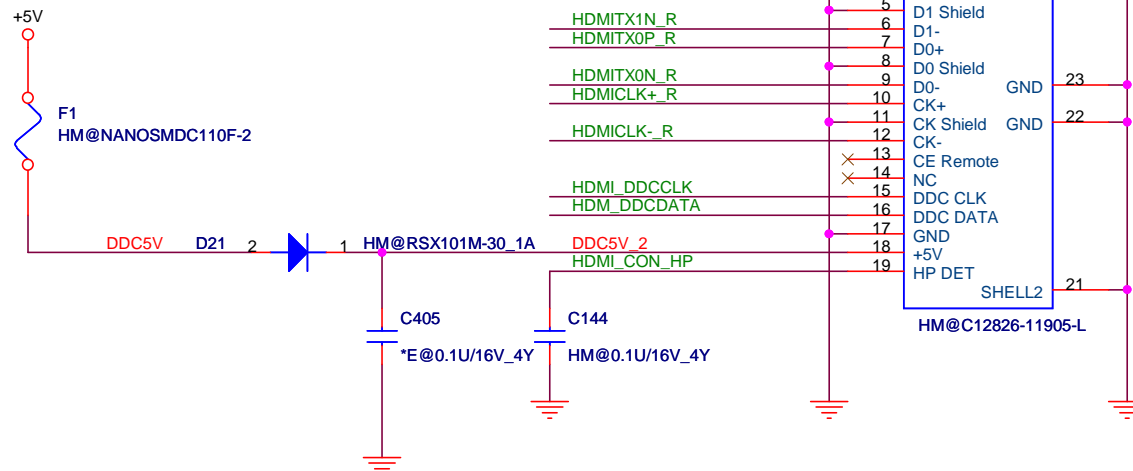


LVDS (UMA)

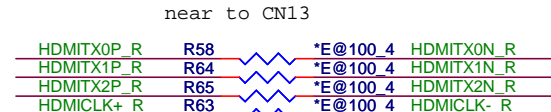
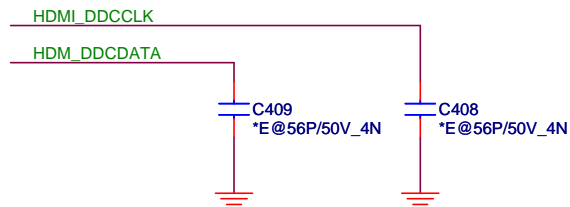
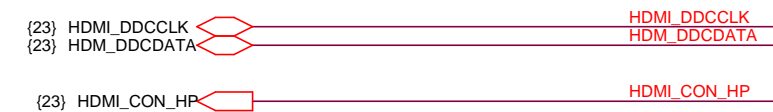


HDMI Conn [HDM]

25



B2A
RN38: footprint is choke model



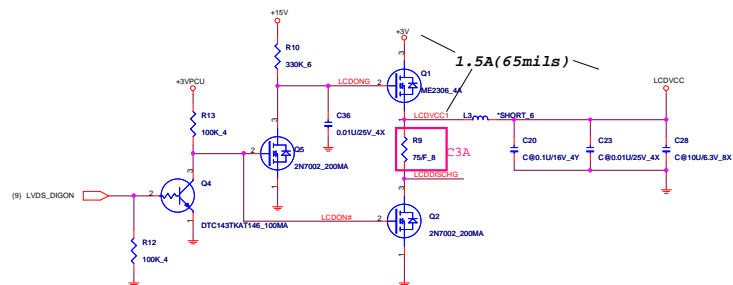
B2A
EMI
此組之後可以刪掉，重覆到了

Quanta Computer Inc.
PROJECT : TE4

Size	Document Number	Rev
	HDMI CONN	A1A
Date:	Monday, January 24, 2011	Sheet 25 of 46

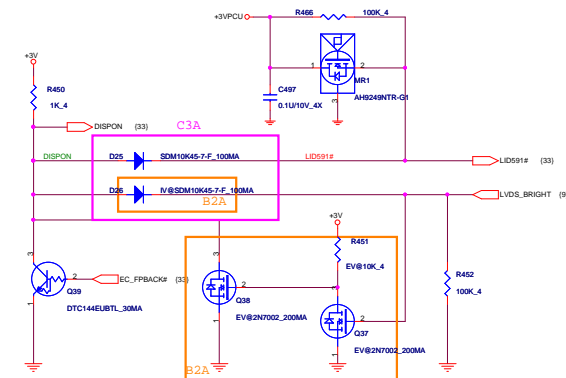
LCD POWER SWITCH

<LDS>



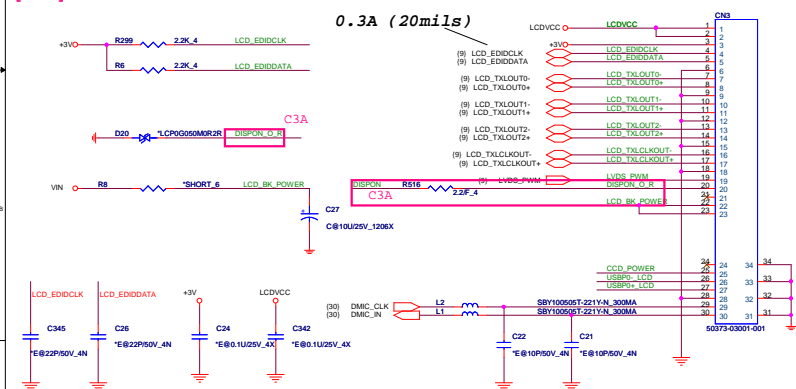
HALL Sensor

<HSR>



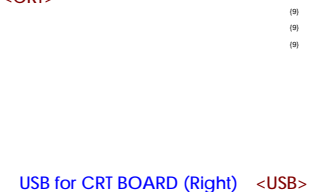
LCD Panel Module

<LDS>

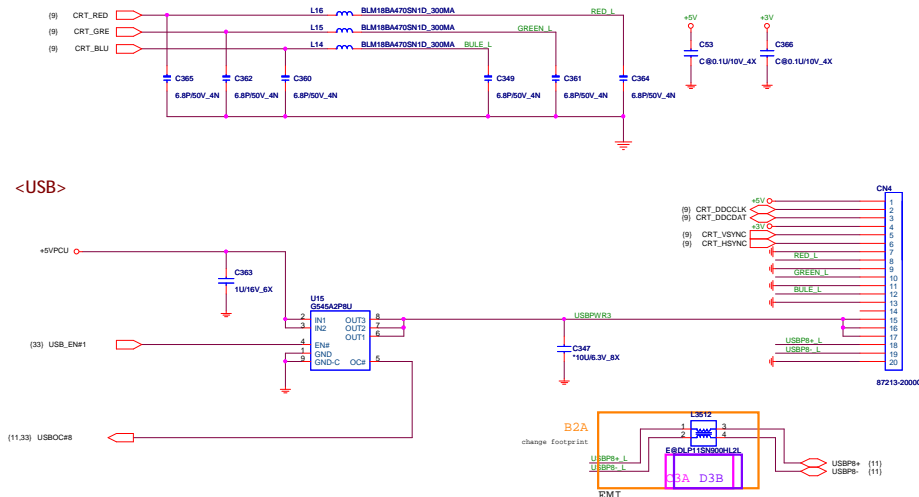


CRT

<CRT>

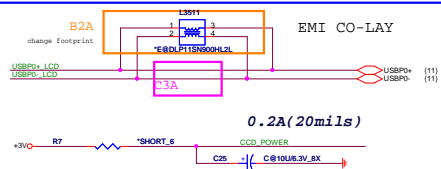


USB for CRT BOARD (Right) <USB>

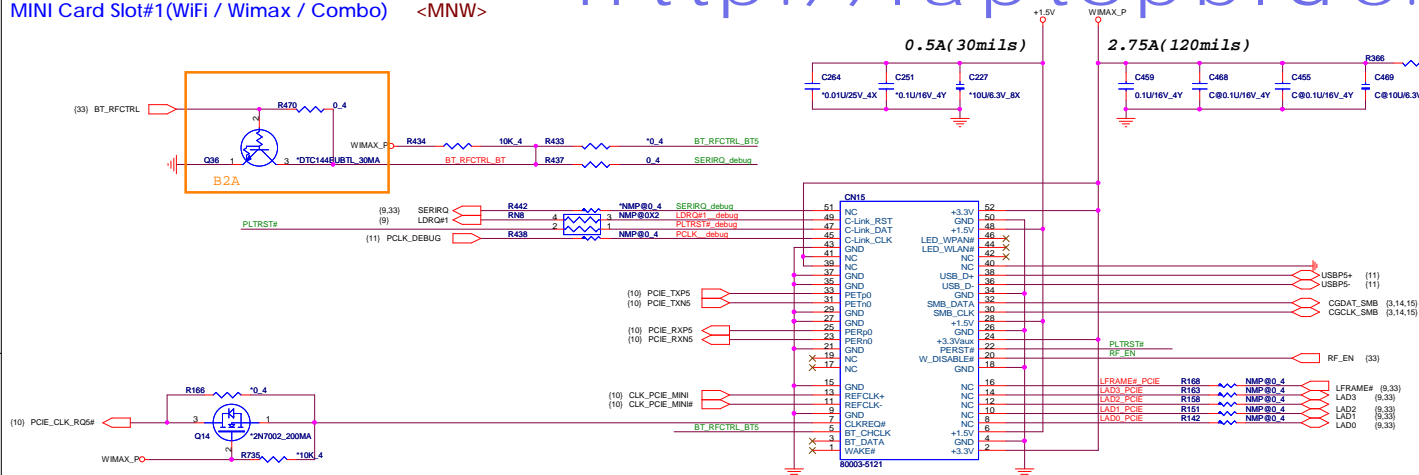


CCD

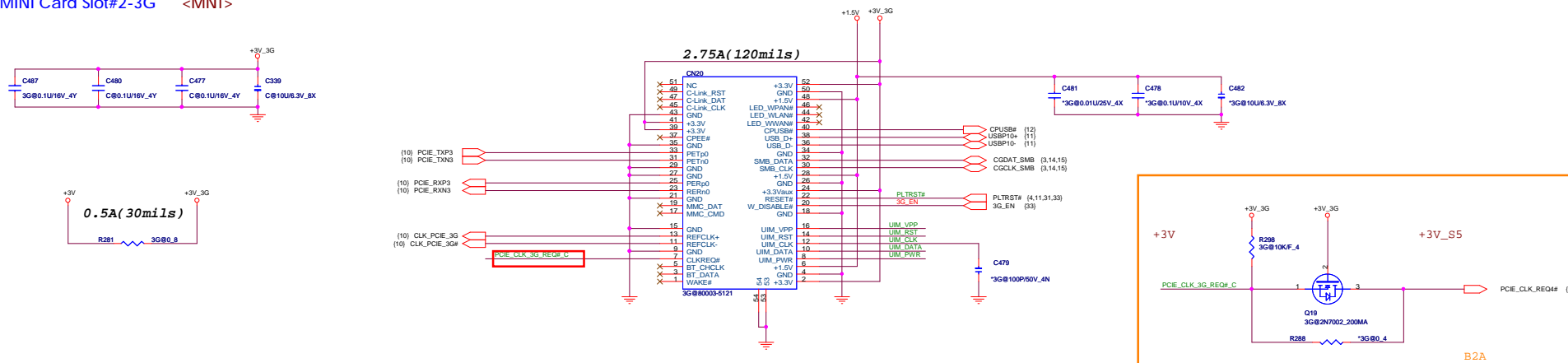
<CCD>



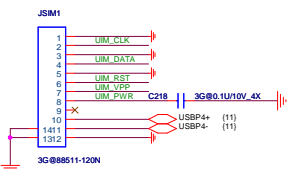
MINI Card Slot#1(Wifi / Wimax / Combo) <MNW>



MINI Card Slot#2-3G <MNT>



SIM CARD

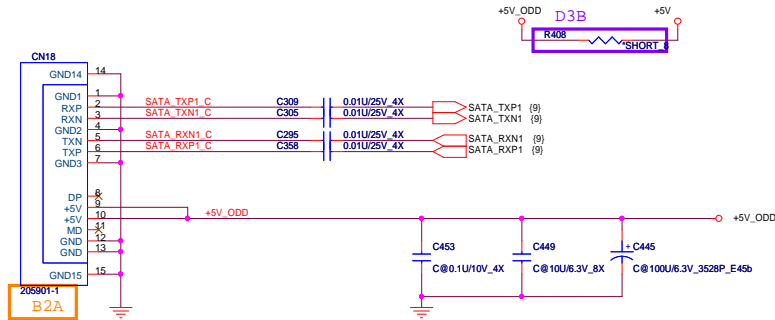


[HTTP://FAQP.RU/](http://FAQP.RU/)

SATA ODD

[ODD]

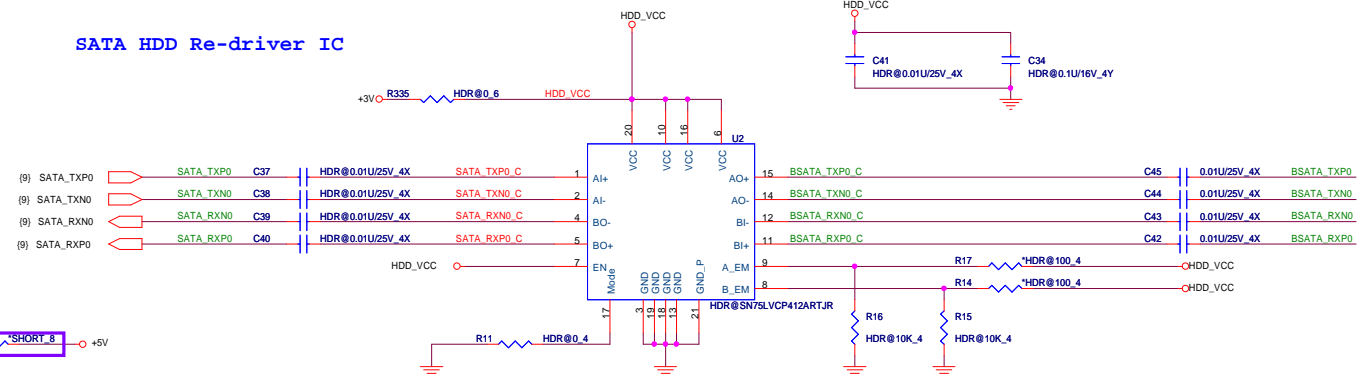
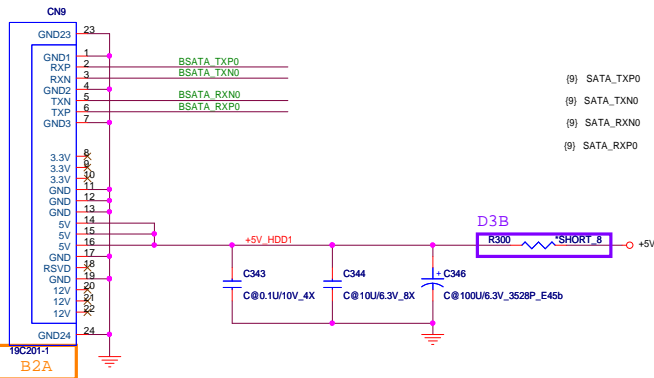
ODD Zero power . (Only for Intel) <OZP>



SATA HDD

[HDD]

SATA HDD Re-driver IC



Colay with Redriver IC

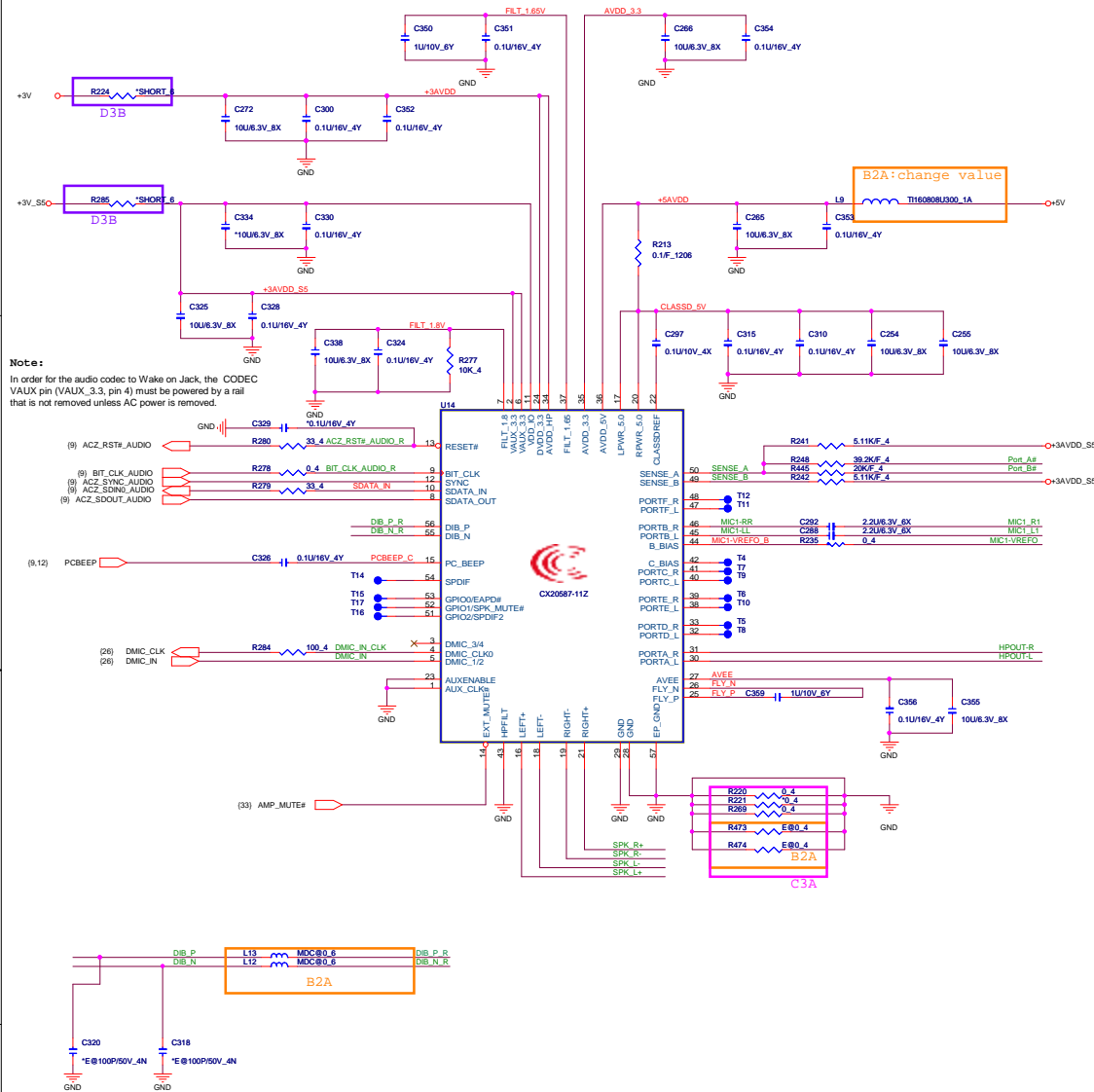
SATA Re-driver Bypass



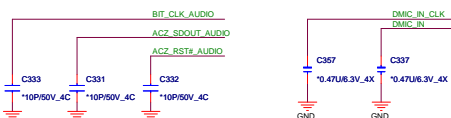
Quanta Computer Inc.
PROJECT : TE4

Size	Document Number	Rev
	HDD/ODD/MDC	A1A
Date:	Monday, January 24, 2011	Sheet 29 of 46

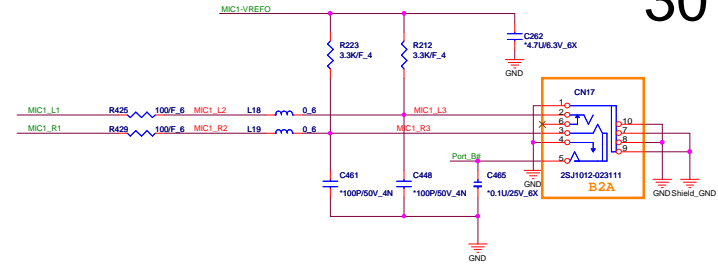
Codec(CX20587-112) <ADO/MDC/AMP>



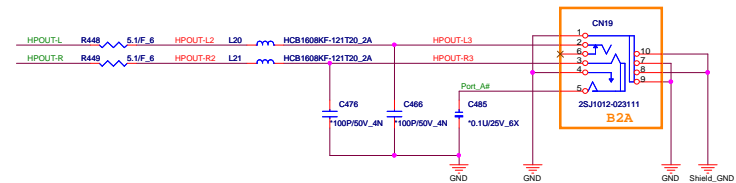
EMI part



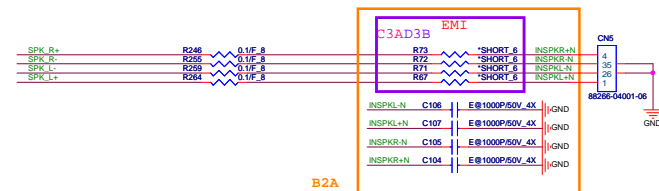
EXT MIC <ADO/AMP>



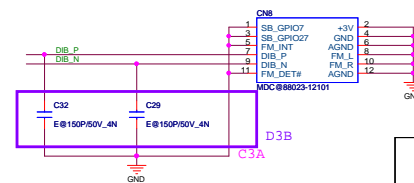
EXT H.P / Beats <ADO/AMP>



INT SPK <ADO/AMP>

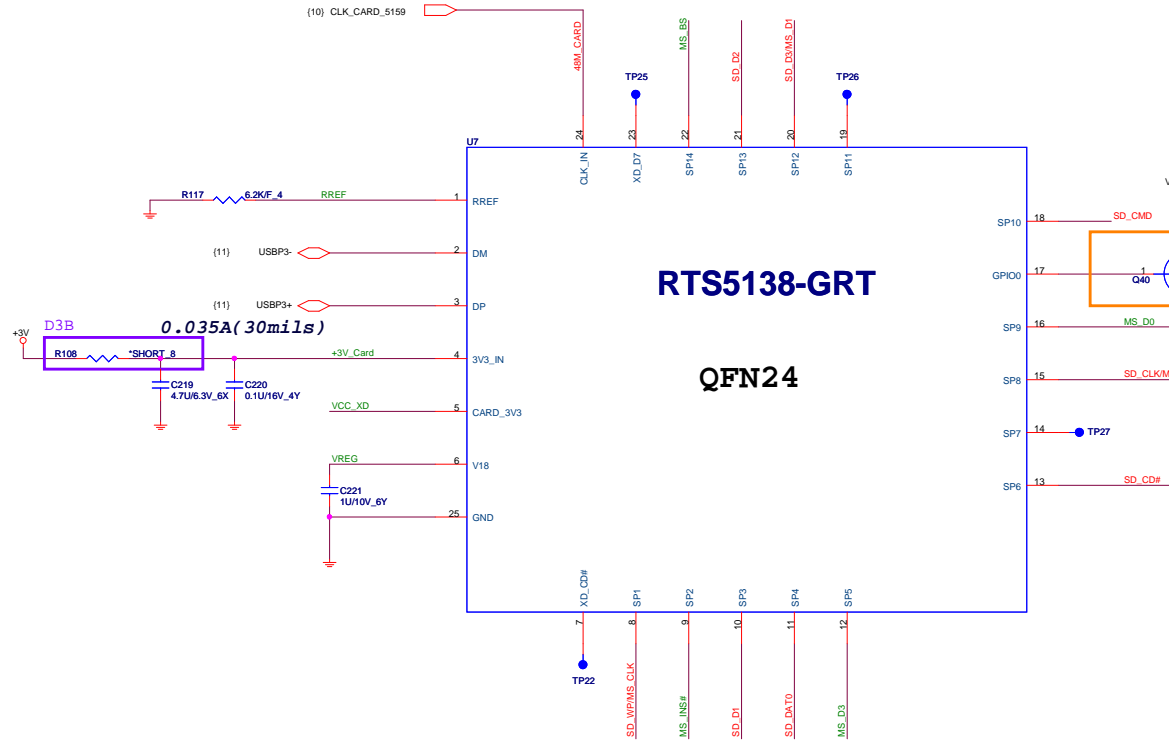


MDC <MDC>



3 IN 1 CARD READER

Card reader controller <MMC>

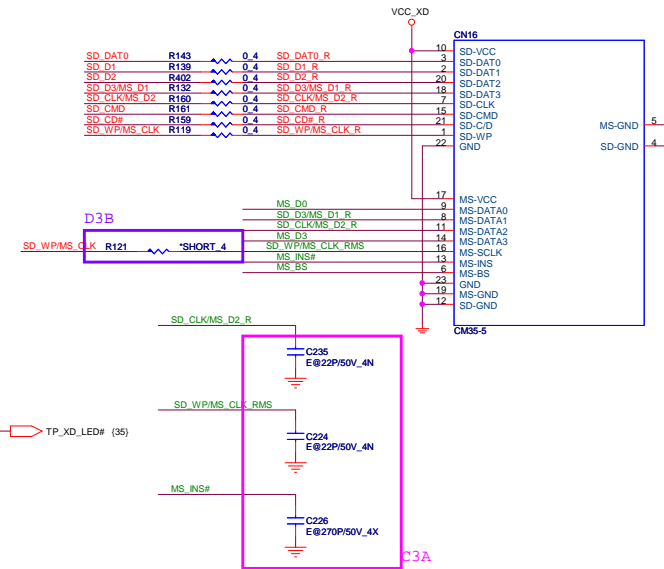


RTS5138-GRT

QFN24

3 IN 1 CARD READER




<MMC>



32



I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MOD	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

BADDR0	BADDR0	R229		*10K_4
BADDR1	BADDR1	R228		10K_4
SHBM	RF_EN	R194		10K_4

0.003A (20mils)

ADDRESS: A0H

0.025A (20mils)

3V3VCC

3V3VCC

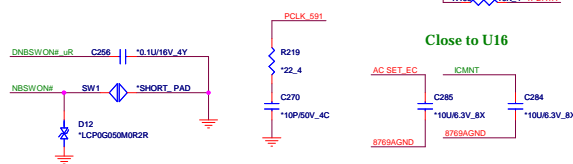
0.1uF/16V

W25X40BVSSIG

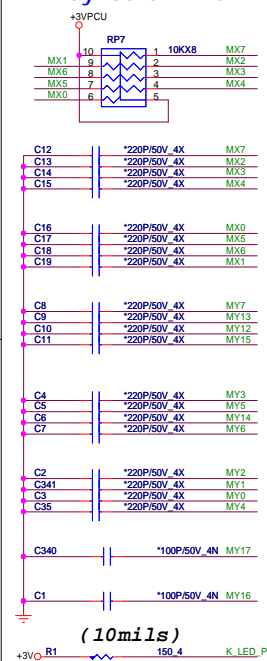
Intel	512KB	W25X40BVSSIG
AMD	2MB	25Q16BVSSIG

The schematic diagram illustrates the power plane for the D3B board. It shows the connection of various power pins to the board's internal power distribution network. The diagram includes components like resistors (R426, R482, R164, R493, R495, R496, R498, R499), diodes (D4, D6, D8, D10), and capacitors (D3B). It shows connections for TP1, TP23, GFX_PG, HWPQ_VGA, HWPQ, HWPQ_1.5V, and HWPQ_VTT. The board is labeled D3B.

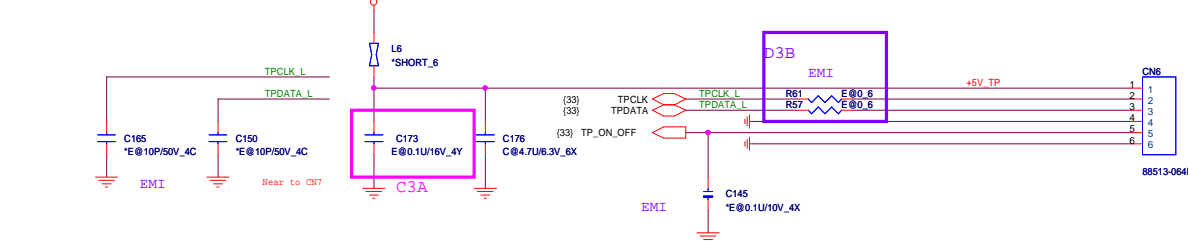
SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	AMD SMBus	98H
	EC EEPROM	A0H
	VGA Board Thermal Sensor	98H
3		



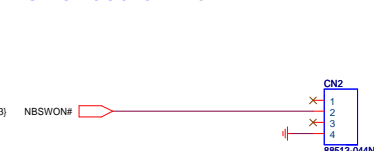
INT KeyBoard <KBC>



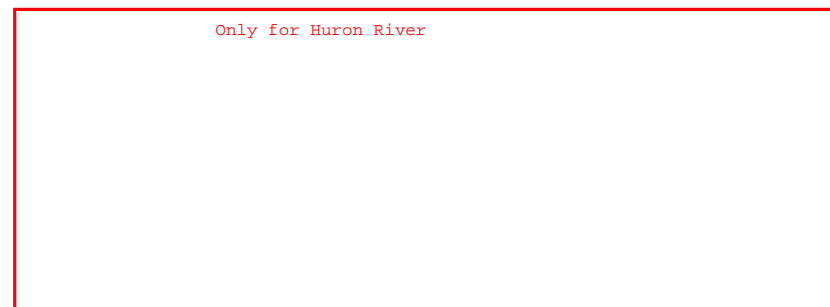
TP board <TPD>



Power board <PSW>

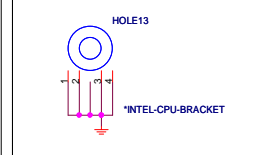


K/B LED power <KBP>

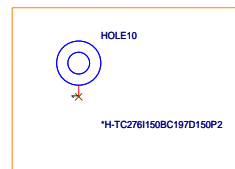
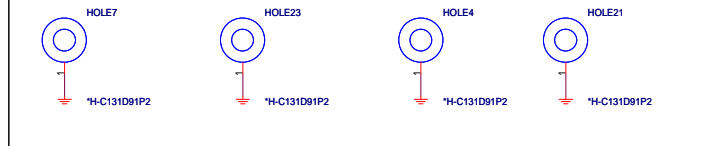


HOLE

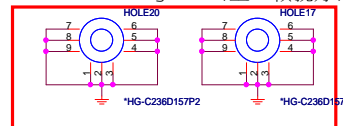
CPU



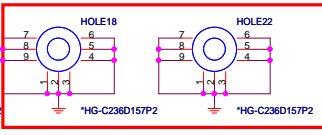
HDD&ODD



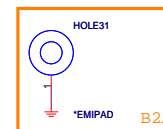
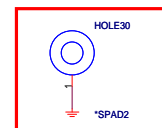
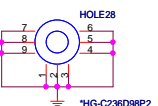
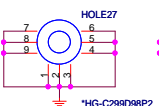
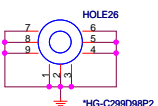
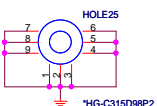
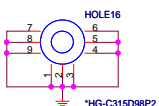
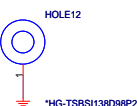
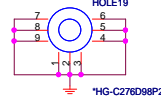
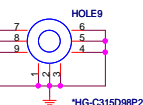
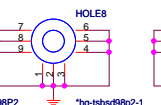
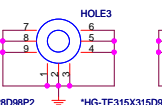
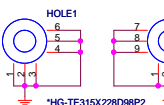
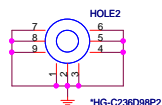
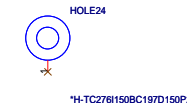
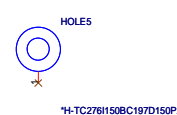
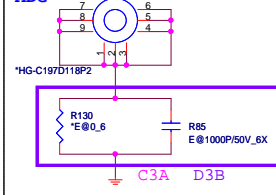
MINI CARD debug Card(上一顆就好)



3G Card(上一顆就好)

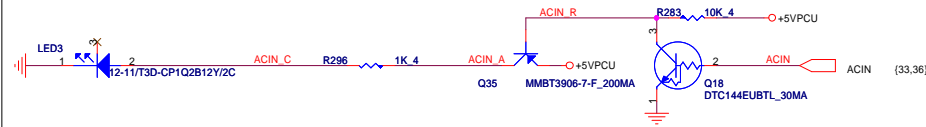


MDC

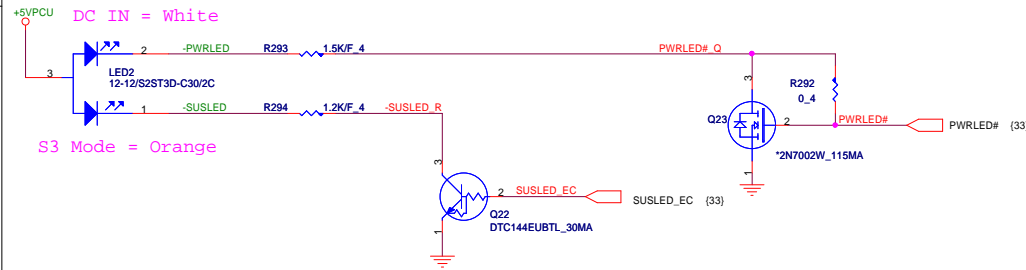


LED

AC-IN



POWER

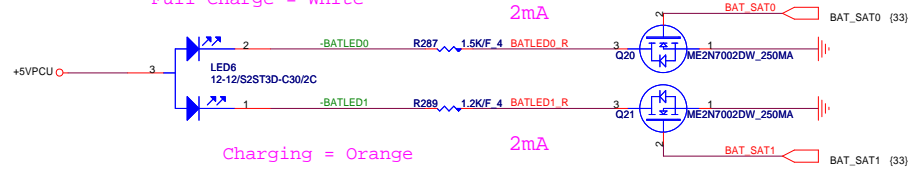


RF LED

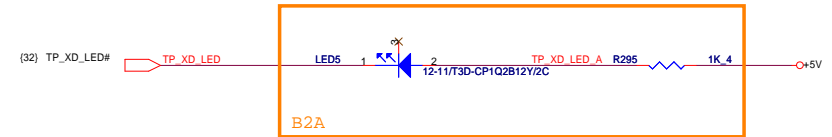


BATTERY

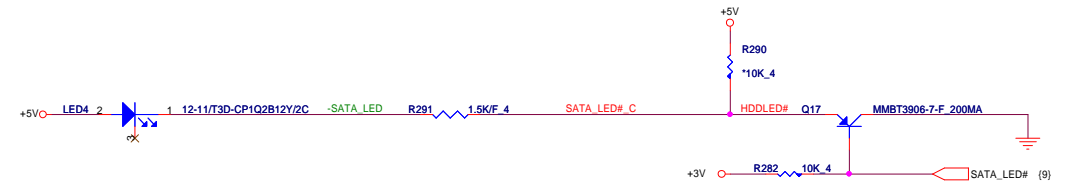
Full Charge = White



CARDREADER

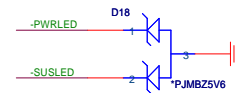


HDD/ODD

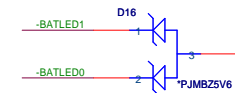


ESD Protect

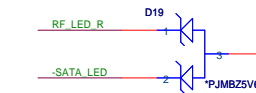
FOR POWER LED



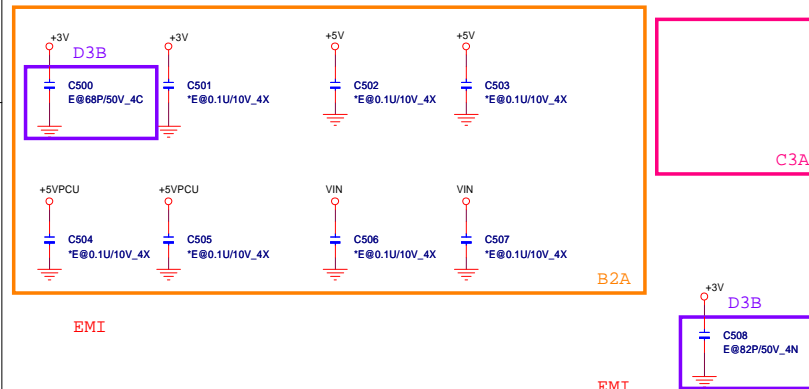
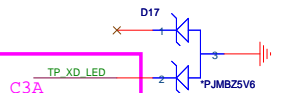
FOR BATTERY LED

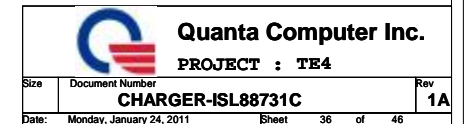


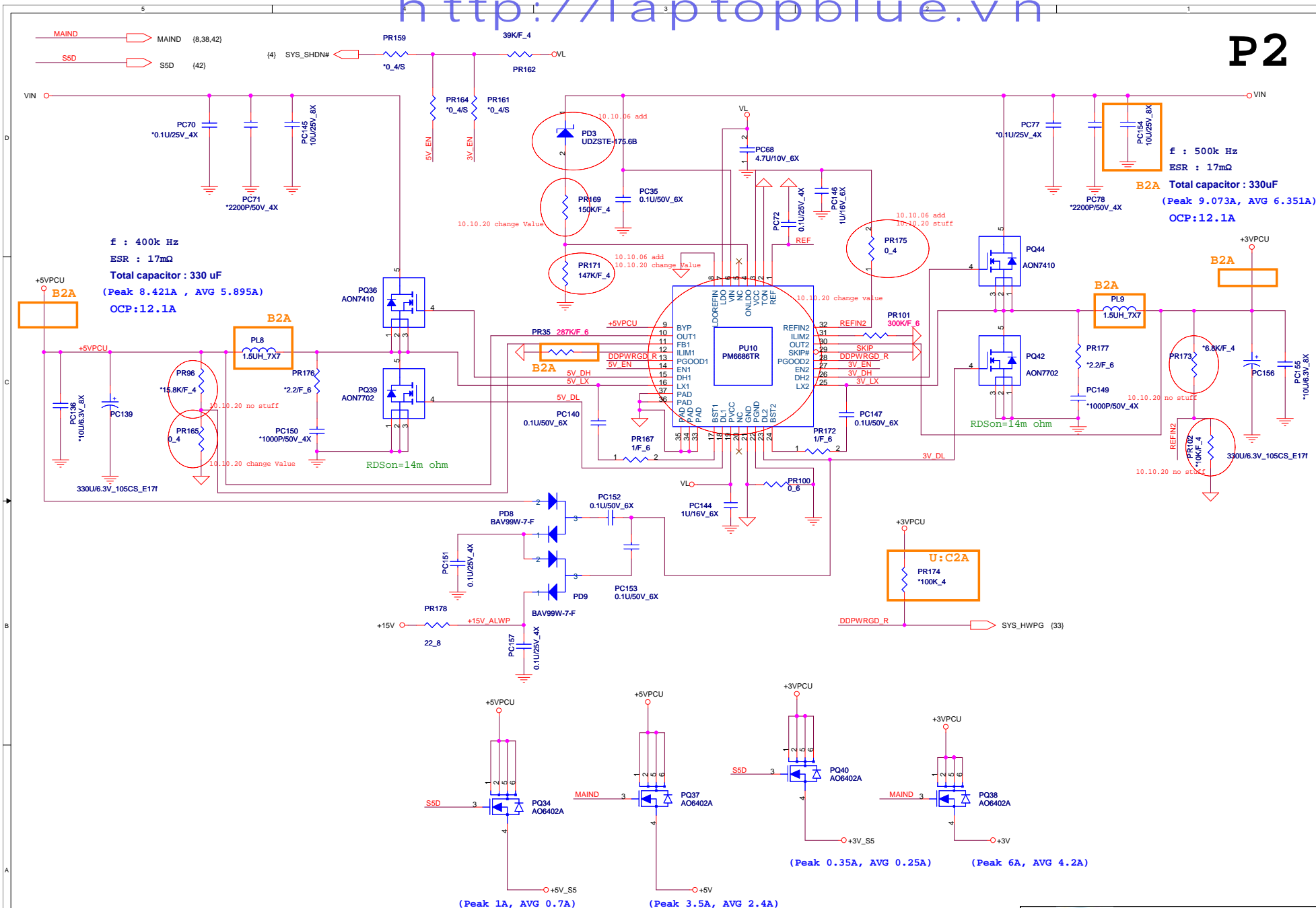
FOR HDD/RF LED

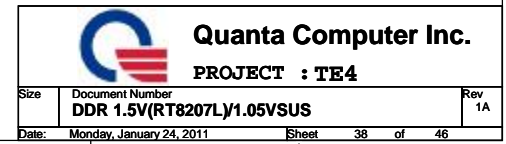


FOR CARDREADER LED



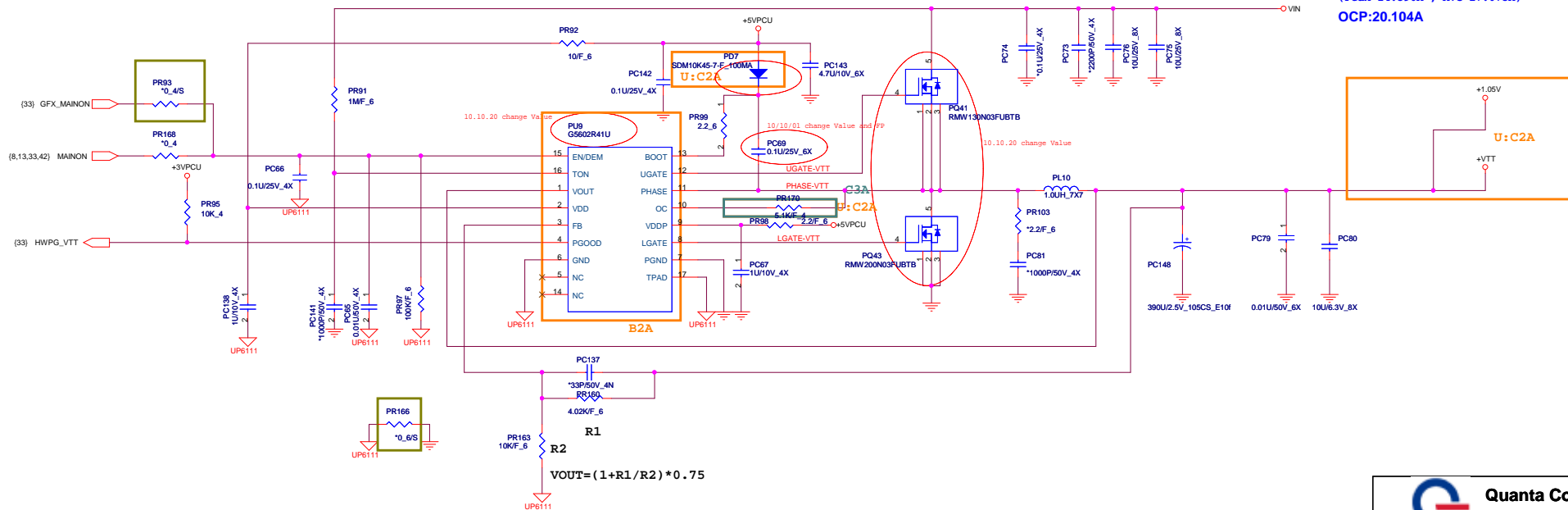





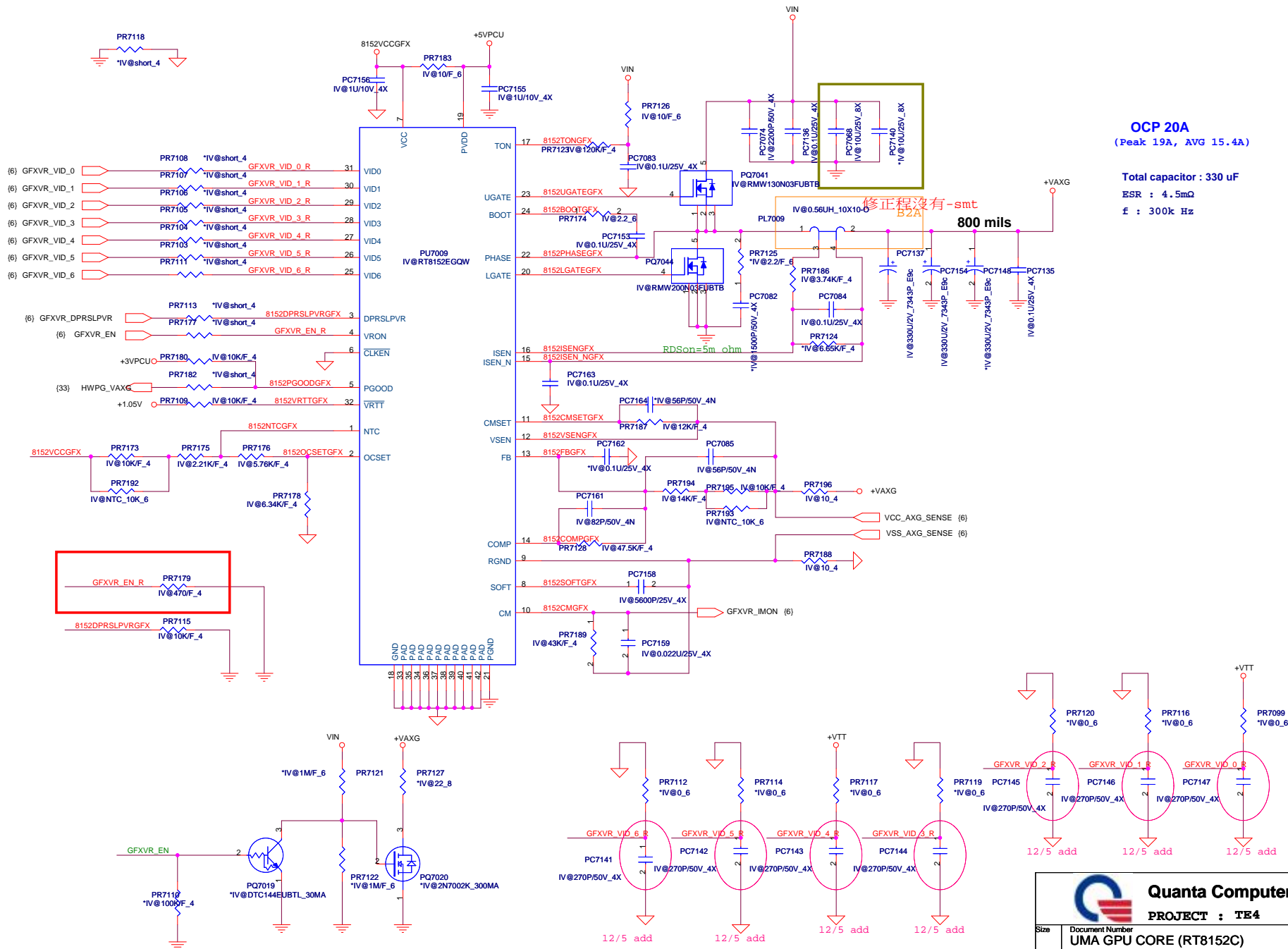


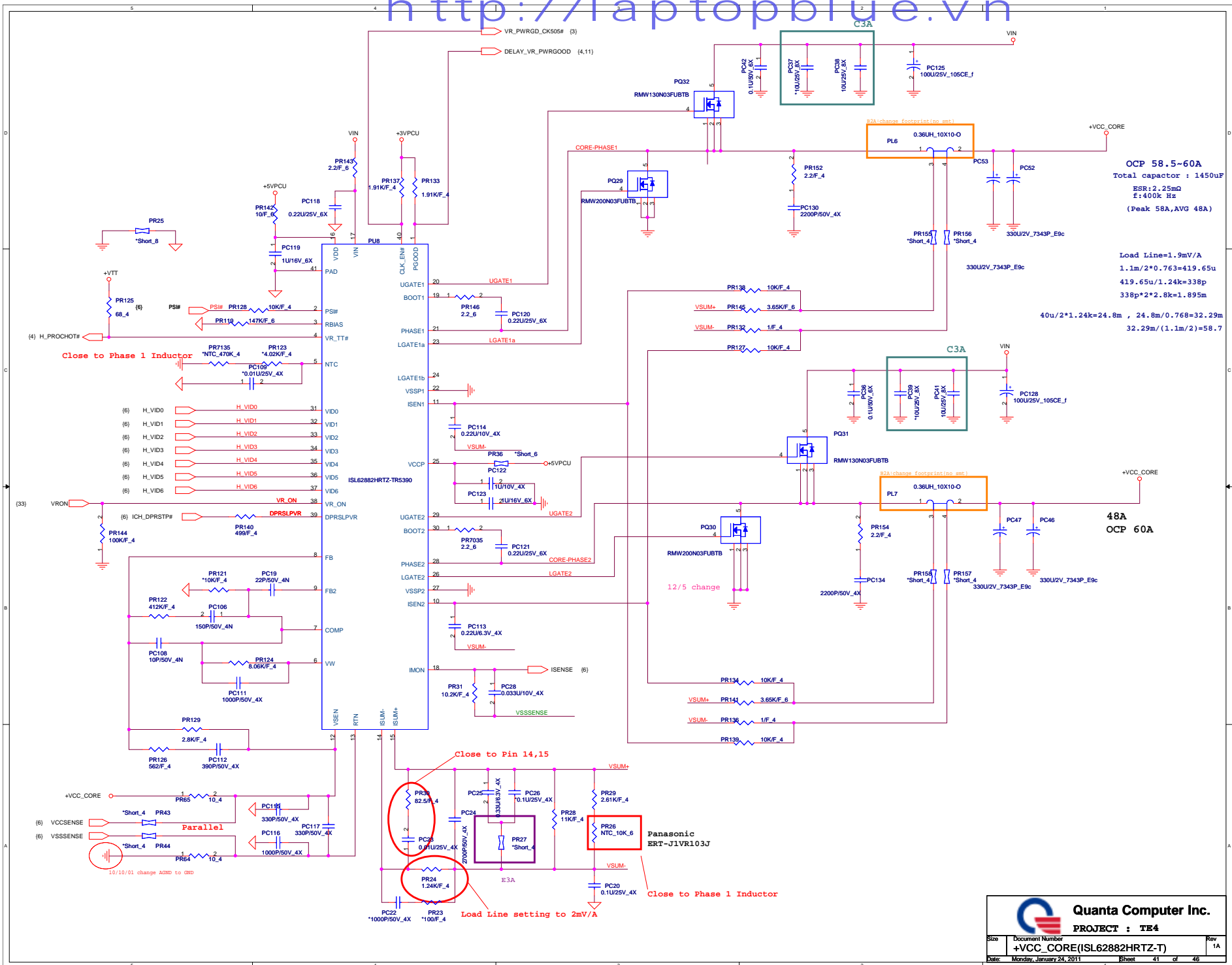
P4

Total capacitor : 390uF
F: 320k Hz
(Peak 24.390A , AVG 17.073A)
OCP:20.104A

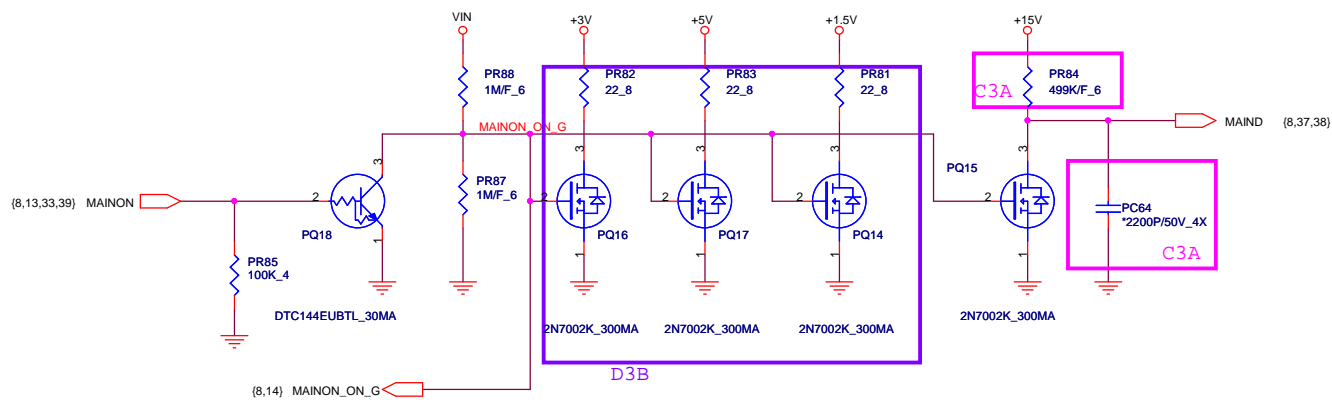
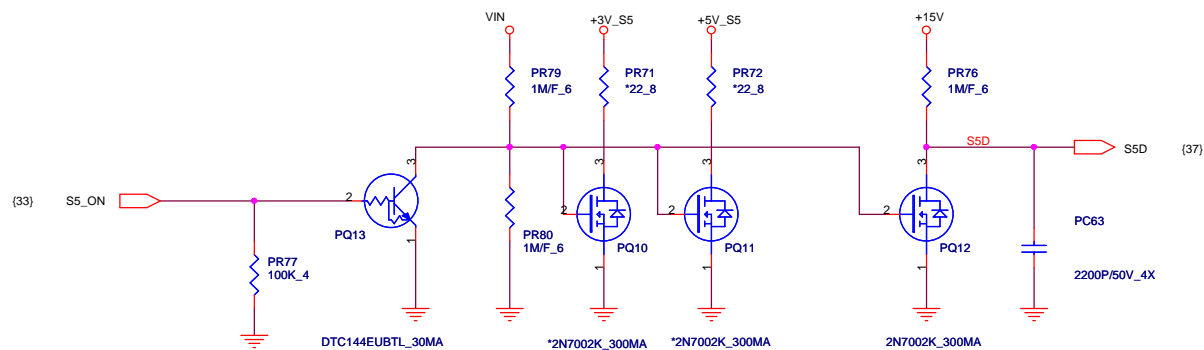
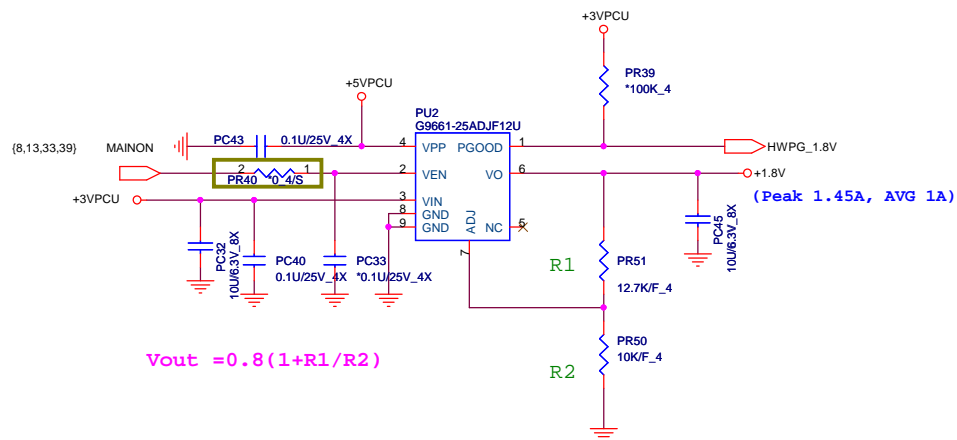


 Quanta Computer Inc. PROJECT : TE4	
Size	Document Number +VTT/+1.05V (G5602R41U)
Date:	Monday, January 24, 2011
Sheet	39 of 46



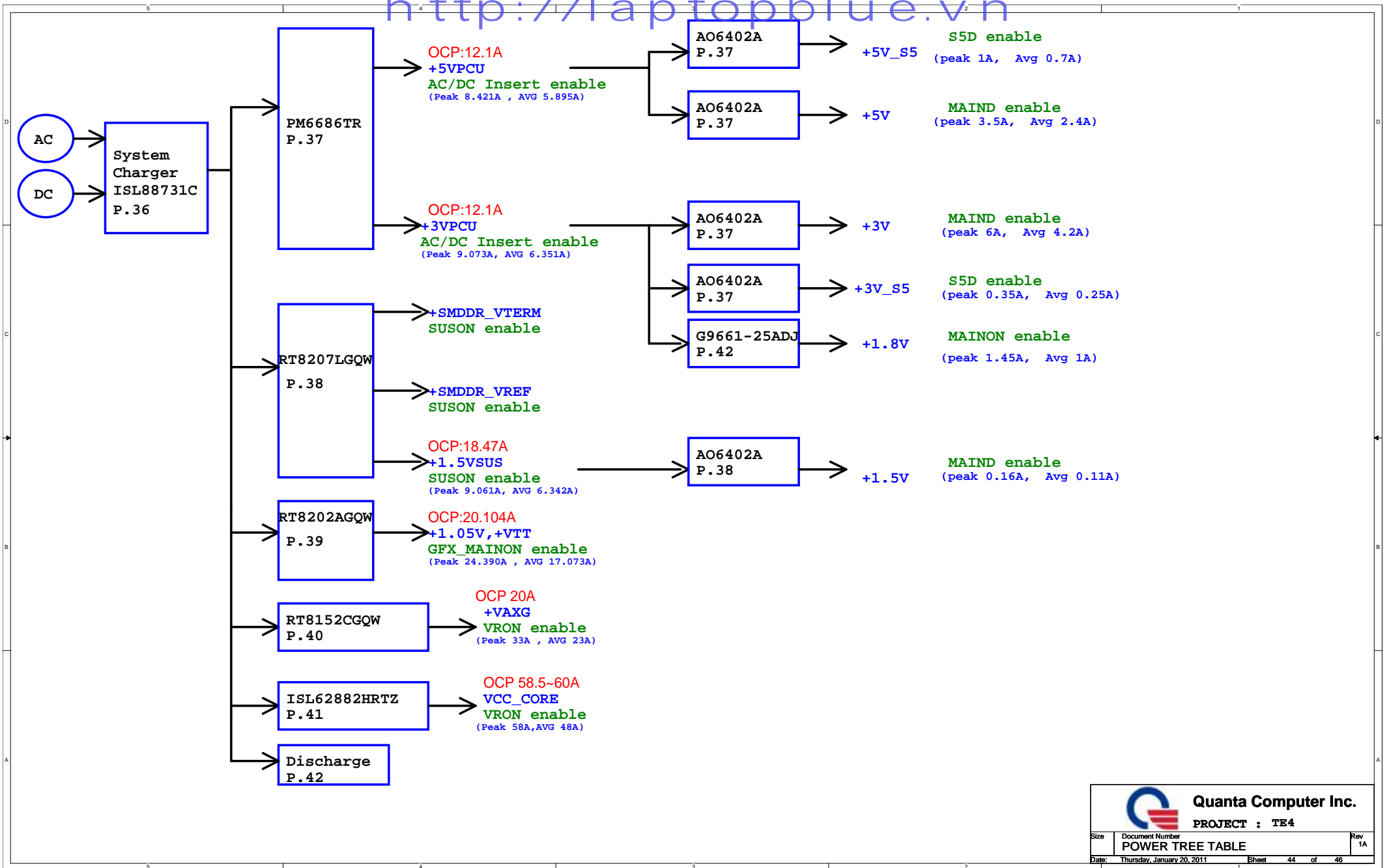


P7




Quanta Computer Inc.
PROJECT : TE4

Size	Document Number	Rev
	+1.8V (G966A)/Discharge	1A
Date:	Monday, January 24, 2011	Sheet 42 of 46



http://laptopblue.vn

Model	REV	CHANGE LIST	MODEL				
			PAGE	FROM	To		
TE4 MB	2A	PAGE 14: R22 no stuff	1	1A			
		PAGE 15: R23 no stuff	2	1A			
		PAGE 27: add R470	3	1A			
		PAGE 28: add Q1100/R1015 and no stuff	4	1A			
		PAGE 32: add Q40	5	1A			
			6	1A			
			7	1A			
			8	1A			
			9	1A			
			10	1A			
			11	1A			
			12	1A			
			13	1A			
			14	1A			
			15	1A			
			16	1A			
			17	1A			
			18	1A			
			19	1A			
			20	1A			
			21	1A			
			22	1A			
			23	1A			
			24	1A			
			25	1A			
			26	1A			
			27	1A			
			28	1A			
			29	1A			
			30	1A			
DOC NO. 204		PROJECT MODEL :	TE4	APPROVED BY:	Kent Su	DATE:	2010/11/12
		PART NUMBER:		DRAWING BY:	Kent Su	REVISION:	1A
						PROJECT : TE4	
				Size		Rev	
				Document Number		1A	
				Block Diagram			
				Date: Thursday, December 02, 2010		Sheet 46 of 46	

1