

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

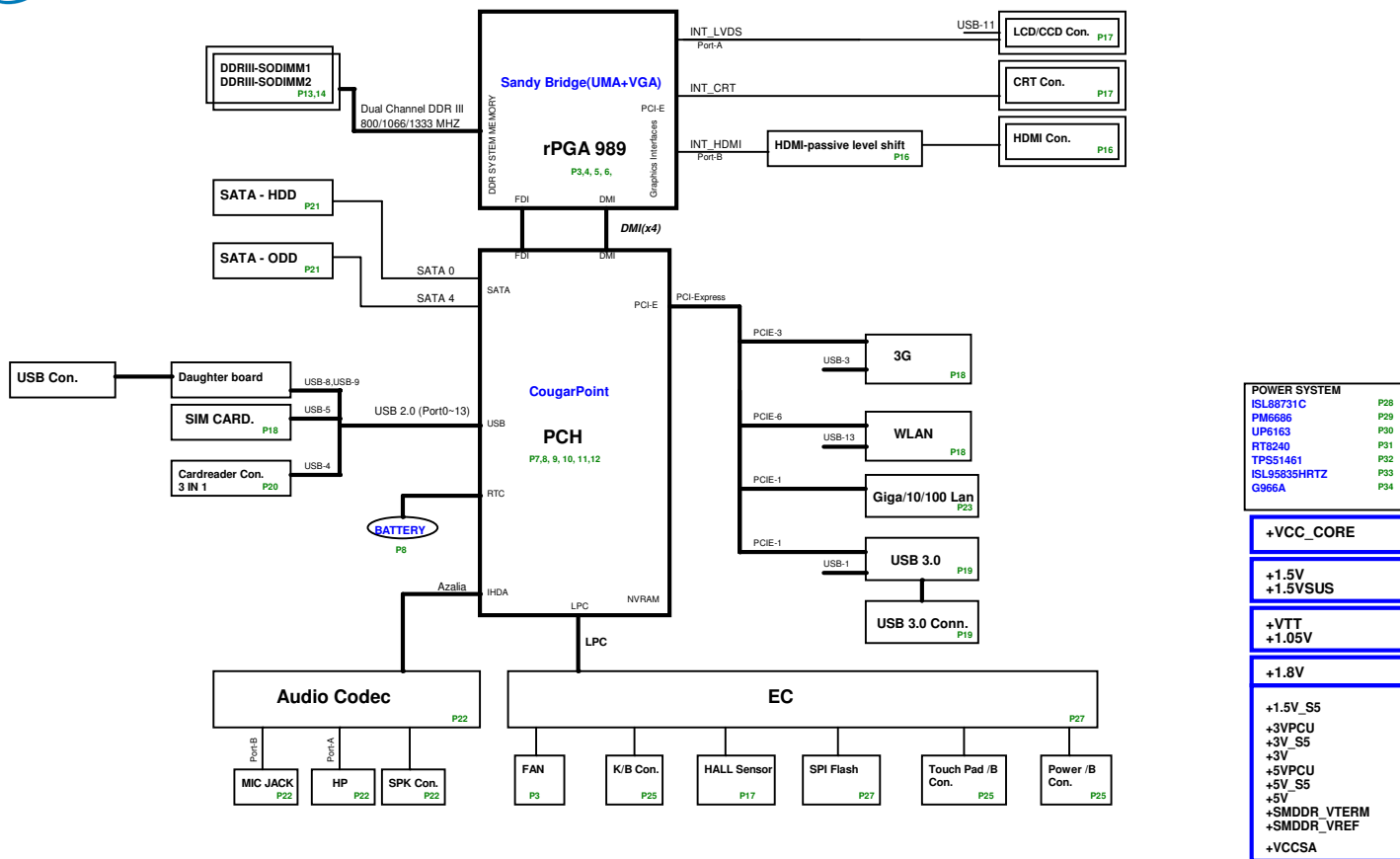






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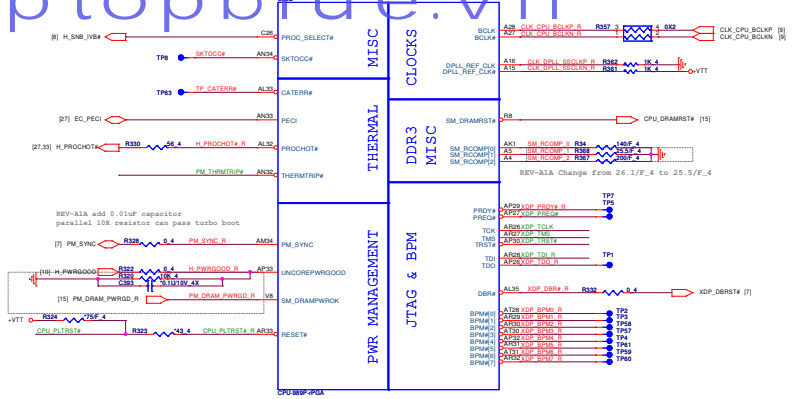
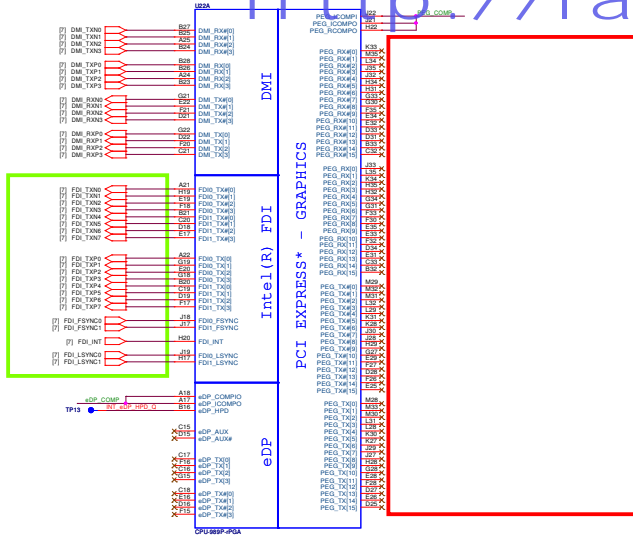
POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0-S5
+VCCRTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
+5V_TMA	+5V	MAIN_ON	S0
WIMAX_P	+3.3V	WMAX_P for EC	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_S5	+1.5V	S5_ON	S0-S5
+1.5V_SUS	+1.5V	SUSON	S0-S3
+VCC_CORE		VRON	S0
+VTT	+1.05V~+1.1V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		GFXVR_EN	S0

GND PLANE	PAGE
 GND_SIGNAL	32
 CARD_GND	21
 AGND_DC/DC	31
 GND	ALL

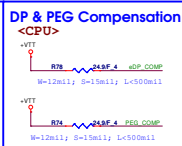
ITEM	Value Code	FUNCTIONS
1	EV@	DISCRETE
2	IV@	UMA
3	U3@	USB 3.0
4	U2@	USB 2.0 (colay W USB 3.0)
5	HM@	HDMI
6	IHM@	Internal HDMI
7	EHM@	External HDMI
8	3G@	3G
9	C@	Cost issue
10	MDC@	Modem
11	S3@	S3 Power Reduction
12	NS3@	No S3 Power Reduction
13	E@	EMI
14	51@	1G LAN
15	52@	10/100 LAN
16	GS@	G-SENSOR
17	NGS@	No G-SENSOR

PAGE	DESCRIPTION	BOI-FUNCTIONS
34	VAXG (ISL62881)	PWM
35	+VTT (UP6111A)	PWM
36	+1.05V (UP6111AQDD)	PWM
37	DDR 1.5V (TPS51116)	PWM
38	Discharge (1.5V_S5/1.8V)	PWM
39	Power Tree Table	
40	PCH Power Plane	
41	Power Management	
42	Change List	

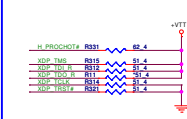
Sandy Bridge Processor (DMI,PEG,FDI)



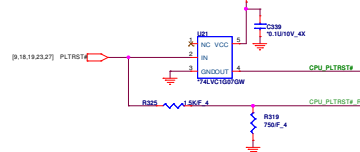
FDI Disabling (Discrete Only)
<CPU>



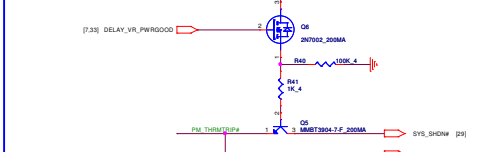
Processor pull-up <CPU>	Level Shift <CPU>
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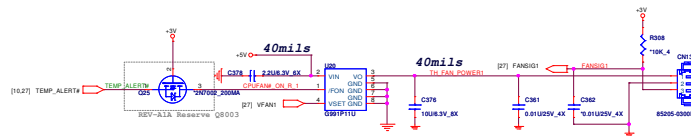
Level Shift <CPU>



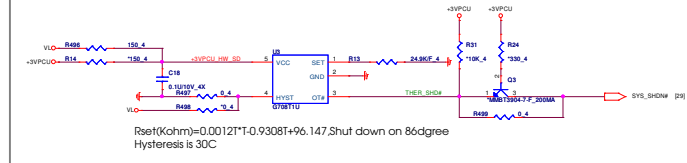
Thermal Trip<CPU>



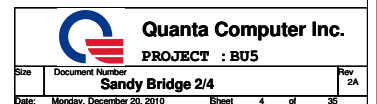
FAN Control-->For one FAN solution <THC>



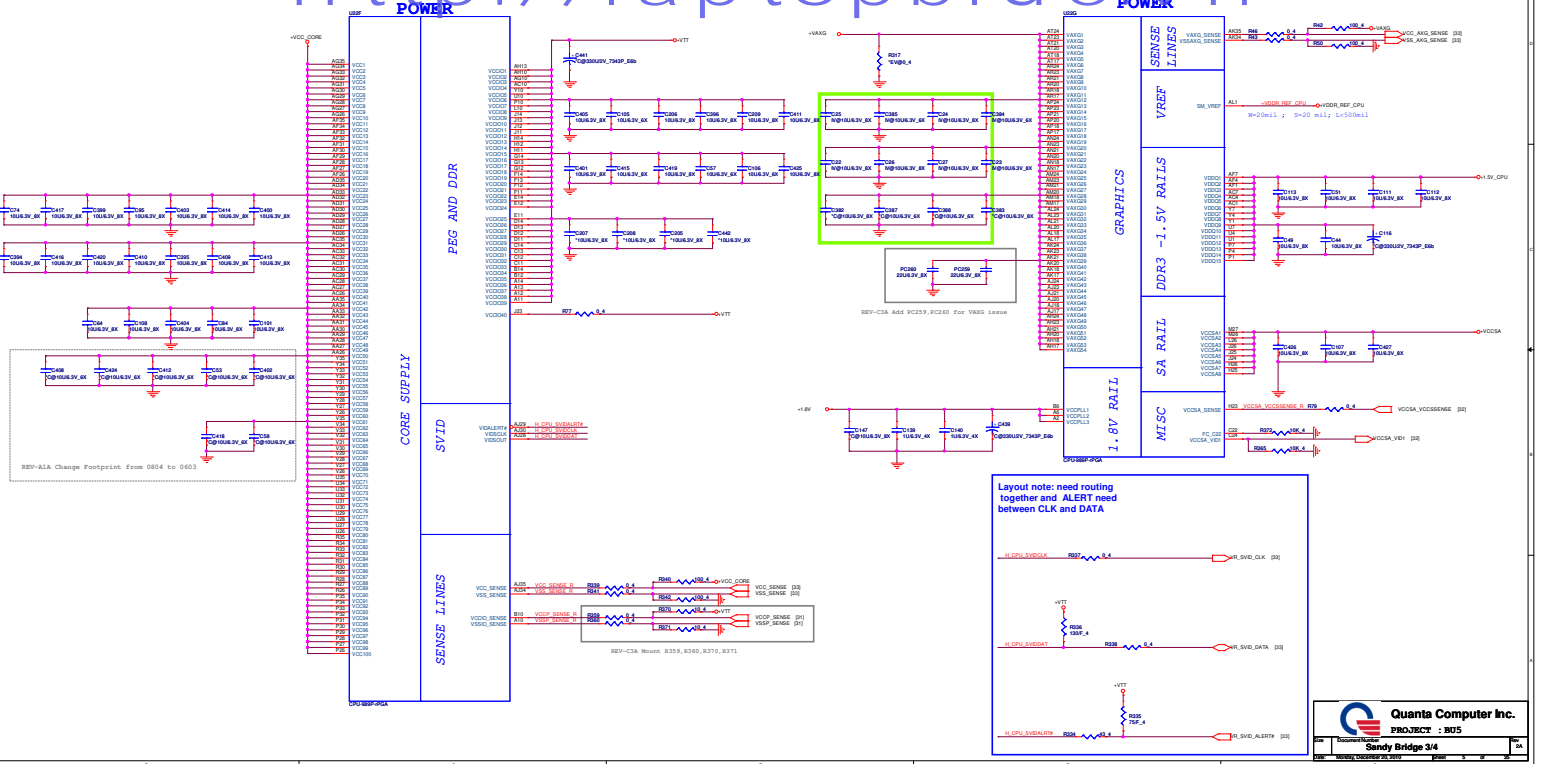
CPU Thermal sensor / MB Local TEMP <THC>

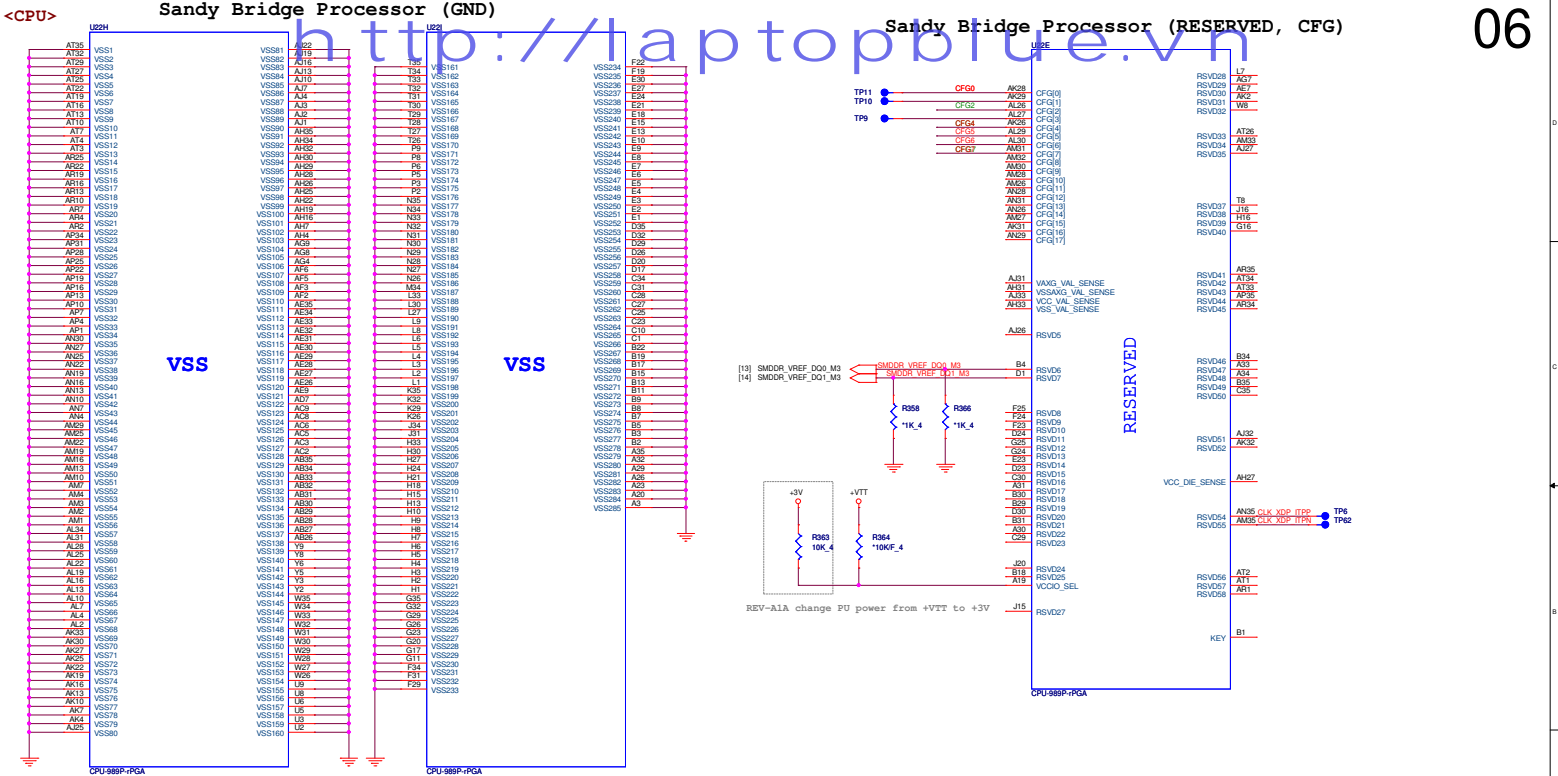


REV-C3A Change VCC PIN5 of U3 from +3VPCU to V2
Add R496,R497,R499
Reverse R14,R498,R31,R24,Q3



Sandy Bridge Processor (POWER) Sandy Bridge Processor (GRAPHIC POWER)





Processor Strapping
The CFG signals have a default value of "1" if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB of assertion	PEG wait for BIOS training

REV-A1A change PU power from +VTT to +3V

CFG2 R9 1K4 5V0 1K 4

CFG4 R93 1K 4

CFG7 R92 1K 4

REV-A1A change to 5% tolerance

CFG6[6.5] (PCIe Port Bifurcation Straps)

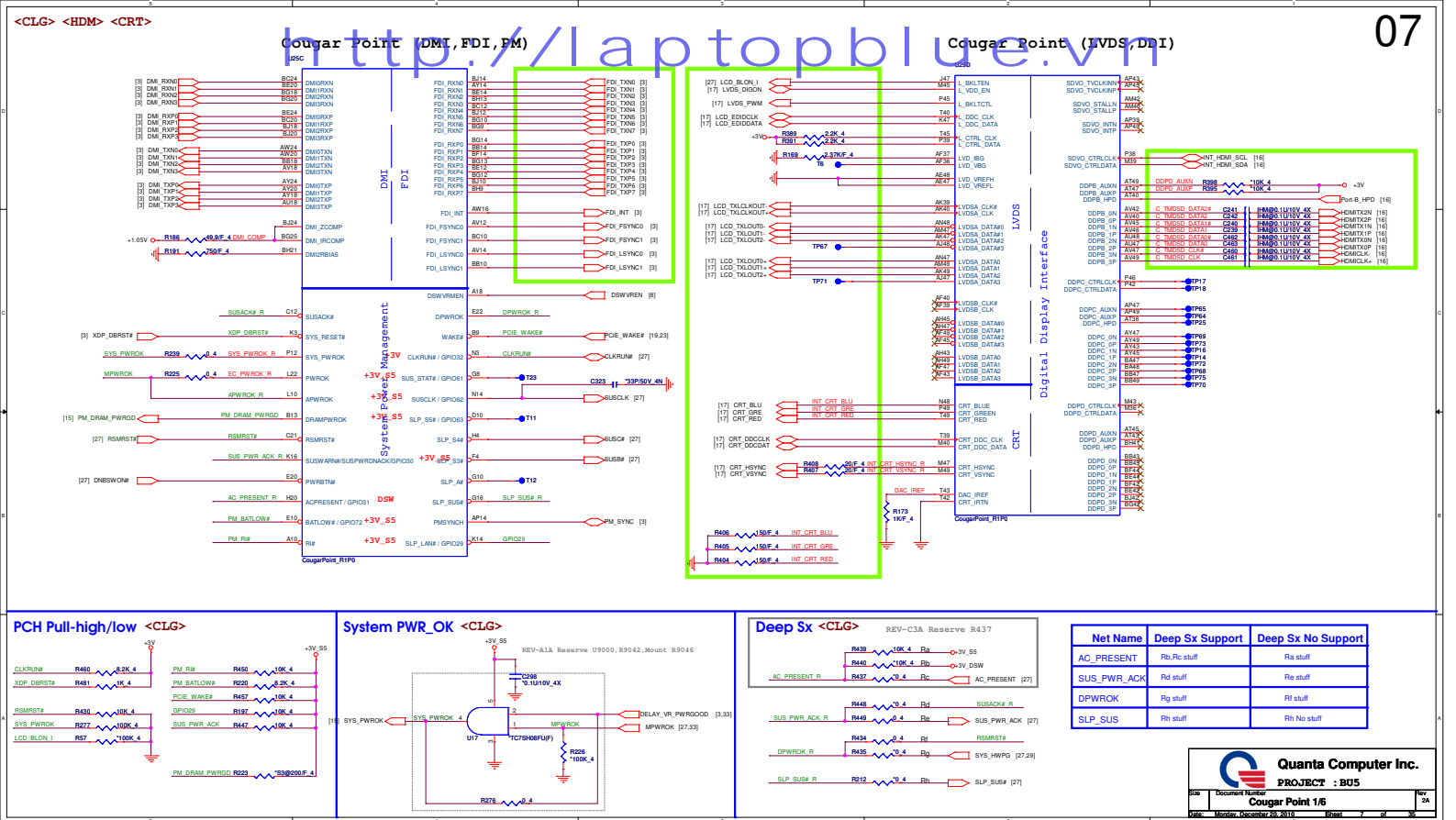
11: (Default) x16 - Device 1 functions 1 and 2 disabled

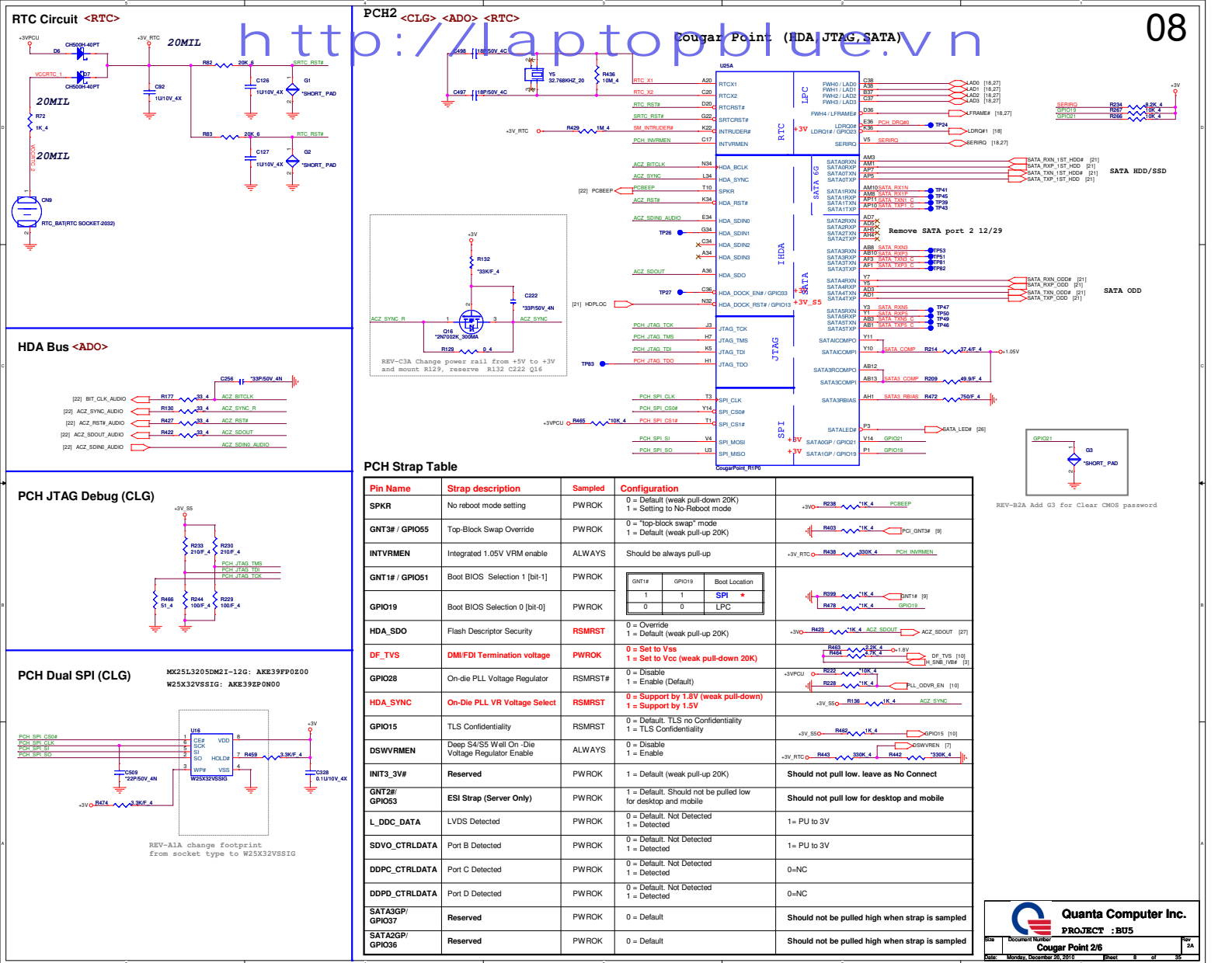
10: x8, x8 - Device 1 function 1 enabled; function 2 disabled

01: Reserved - (Device 1 function 1 disabled; function 2 enabled)

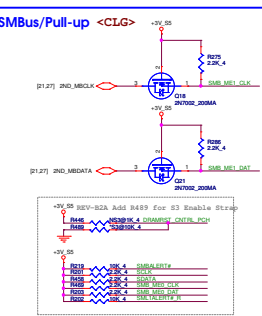
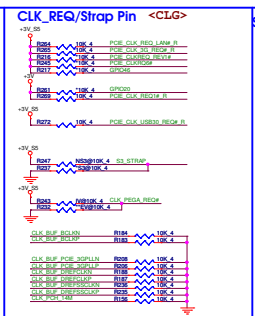
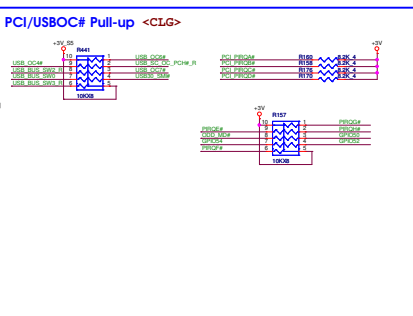
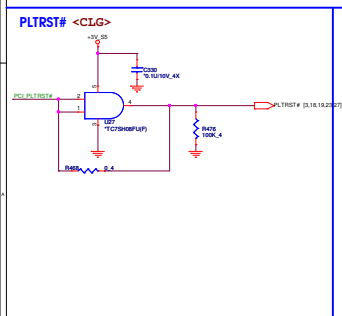
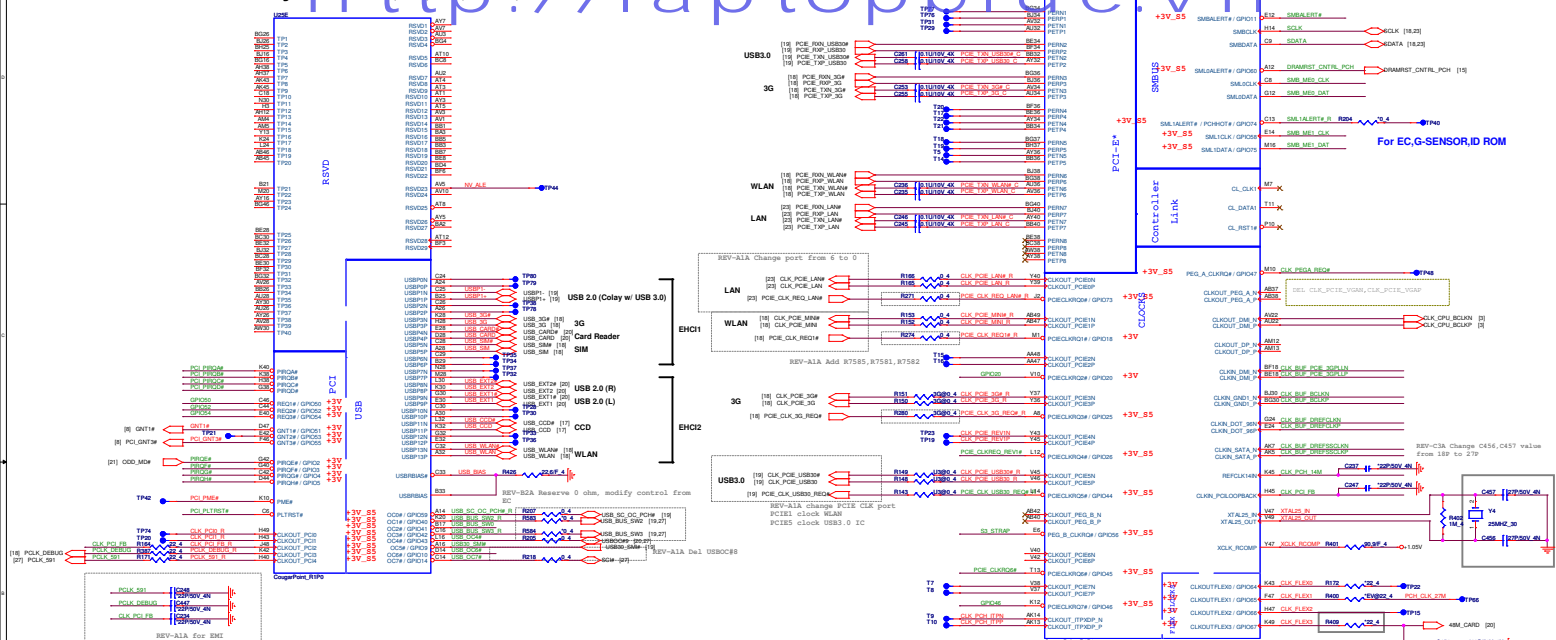
00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

Quanta Computer Inc.
PROJECT :BU5
Size Document Number
Sandy Bridge 4/4
Date Monday, December 25, 2010 Page 6 of 35 Rev 2A





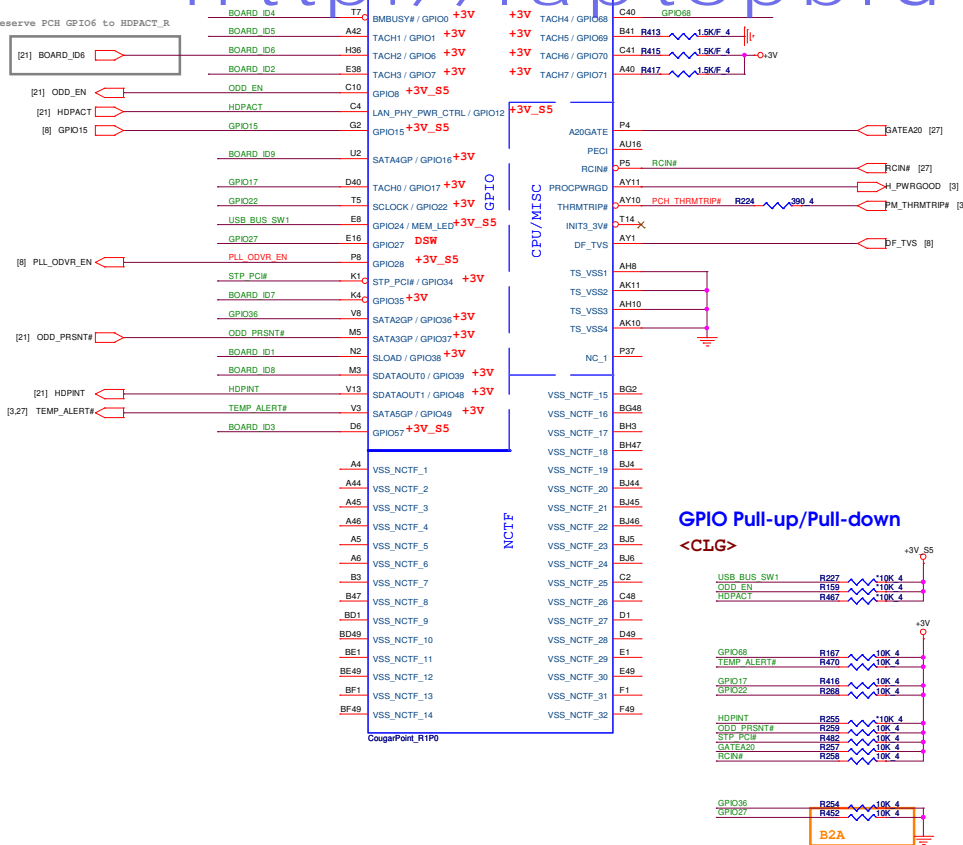
Cougar Point-M (PCI, USB, NVRAM)



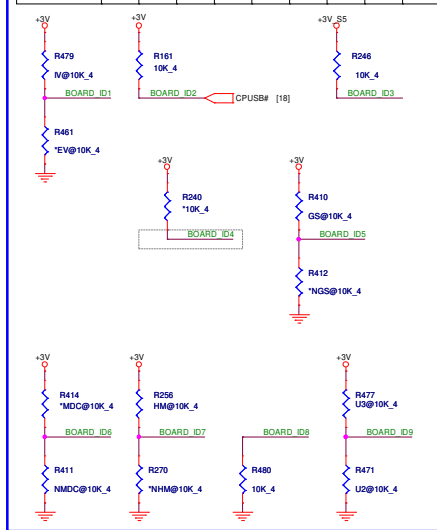
	33MHz	27MHz	48/24MHz	14.318MHz	25MHz
CLK_FLEX0					
CLK_FLEX1					
CLK_FLEX2					
CLK_FLEX3					

Quantia Computer Inc.
PROJECT : BUS
Date: November 26, 2013
Page: 9 of 10

REV-B2A Reserve PCH GPIO6 to HDPACT_R



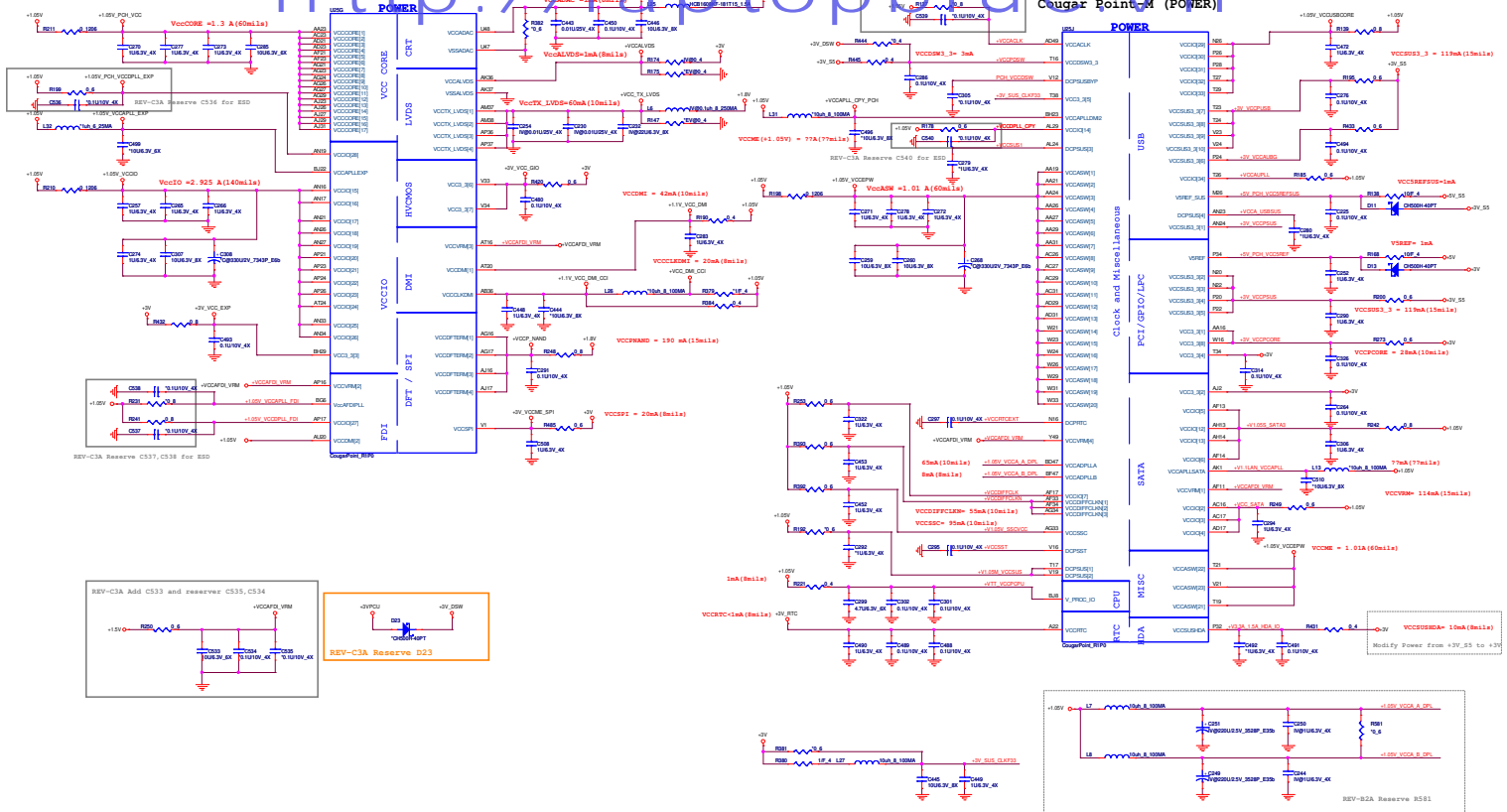
Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9
UMA SKU	H	L							
VGA SKU									
W/O 3G		H	L						
W/O 3G									
W/O LED KB			H	L					
W/O LED KB									
14" 15"				H	L				
W G-SNR					H	L			
W/O G-SNR									
W/ MDC						H	L		
W/O MDC									
W/ HDMI							H	L	
W/O HDMI									
NC								H	L
13"									
W/ USB3.0									H
W/O USB3.0									L



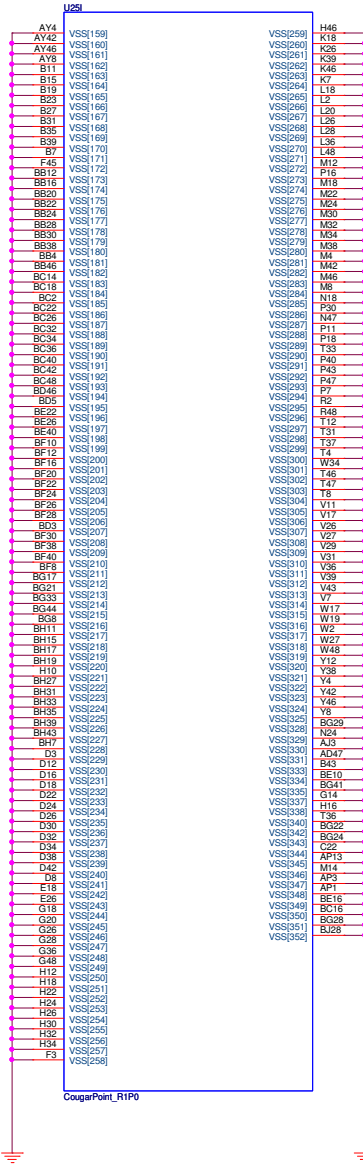
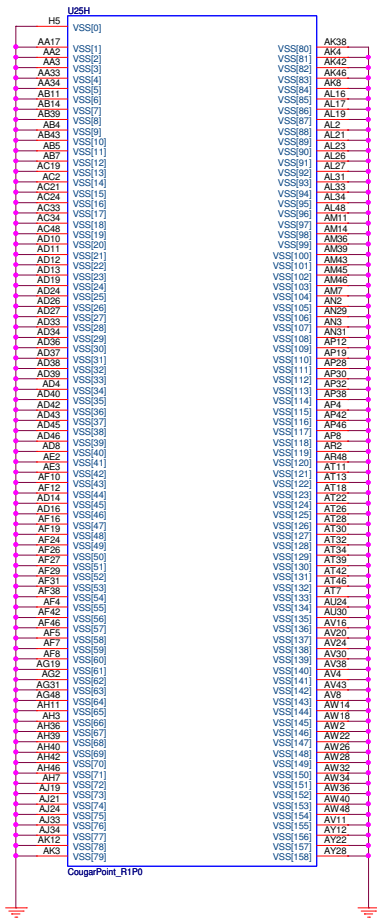
h t t p : / / l a p t o p . c o m C o u p e r P o i n t (P O W E R)

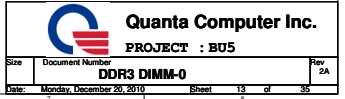
COUPAR POINT (POWER)

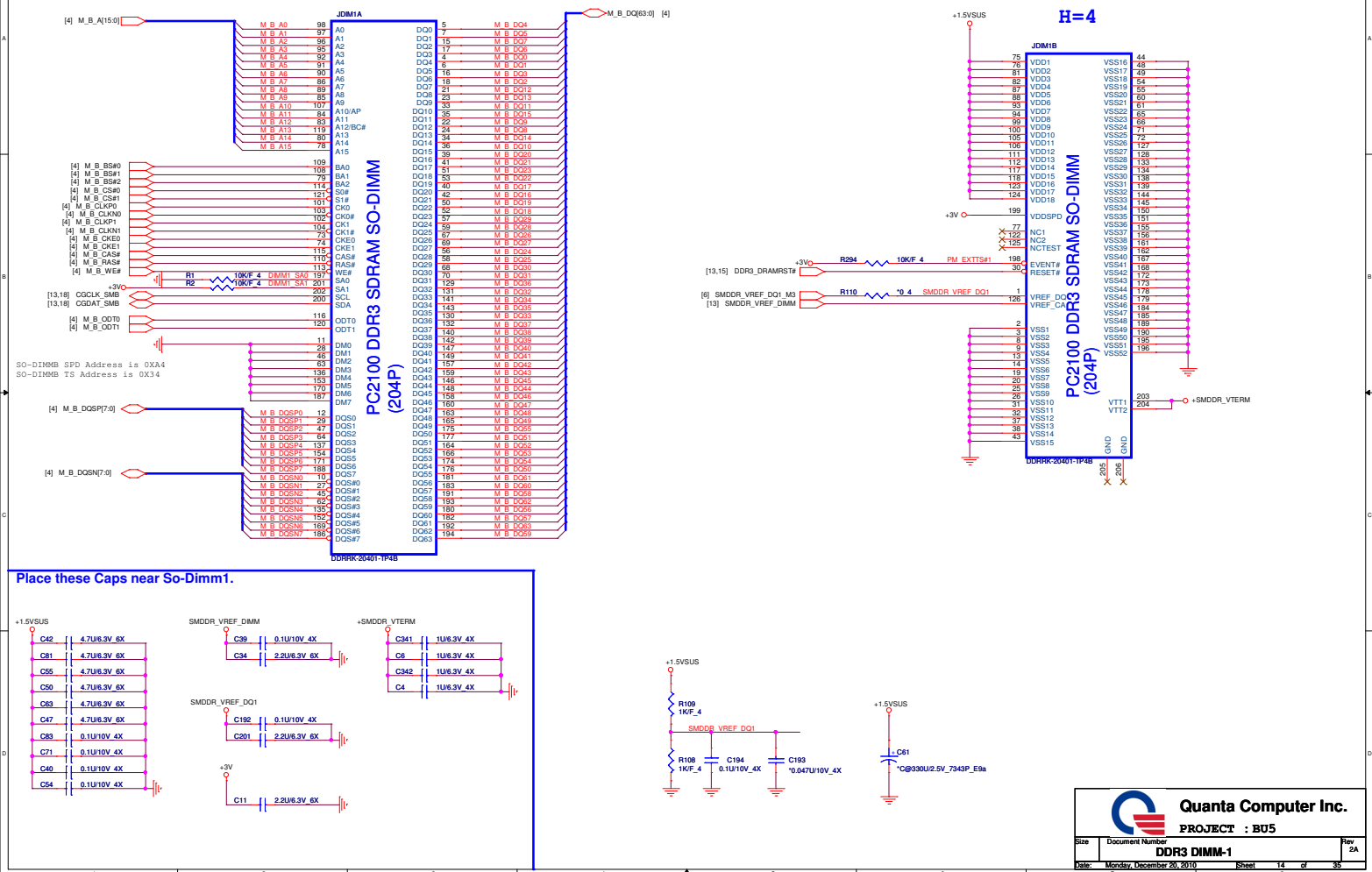
Cougar Point (POWER)



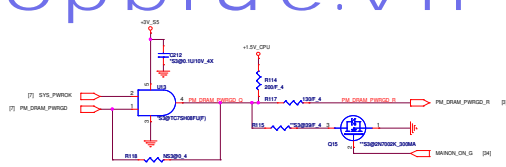
IBEX PEAK-M (GND)



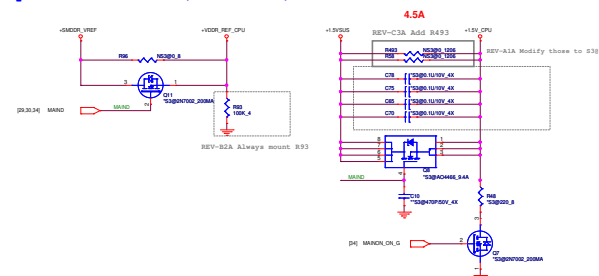


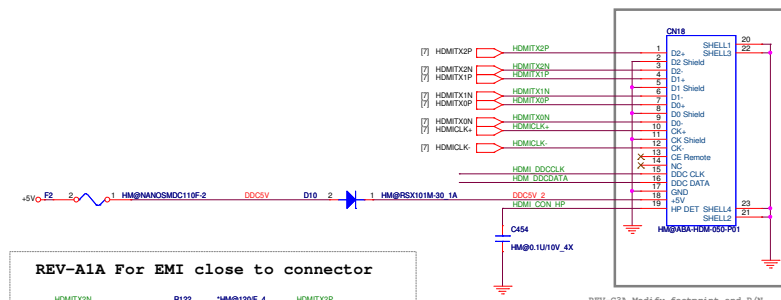


S3 power Reduction (SM_DRAMPWROK) <S3P> <3>



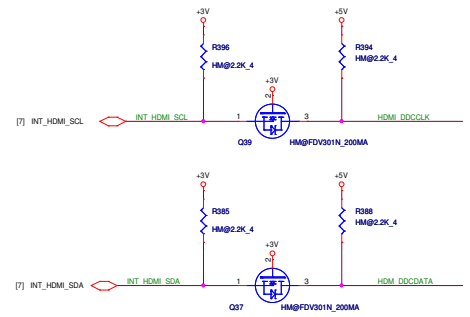
S3 power Reduction (CPU Power) <S3P> <5>





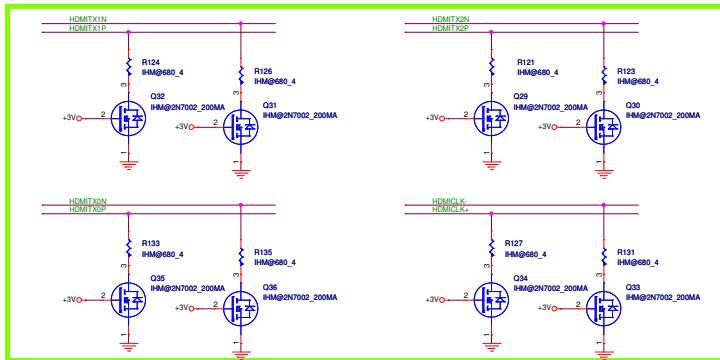
REV-A1A For EMI close to connector

HDMITX2N	R122	*HBM120F 4	HDMITX2P
HDMITX1N	R125	*HBM120F 4	HDMITX1P
HDMITX0N	R134	*HBM120F 4	HDMITX0P
HDMICLK ₋	R128	*HBM120F 4	HDMICLK ₊

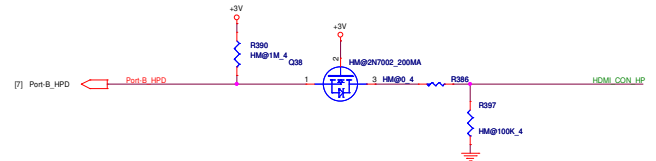


REV-A1A Nvidia Comment +3V_GFX to instead of +3V
as below power rails to avoid power leakage issue

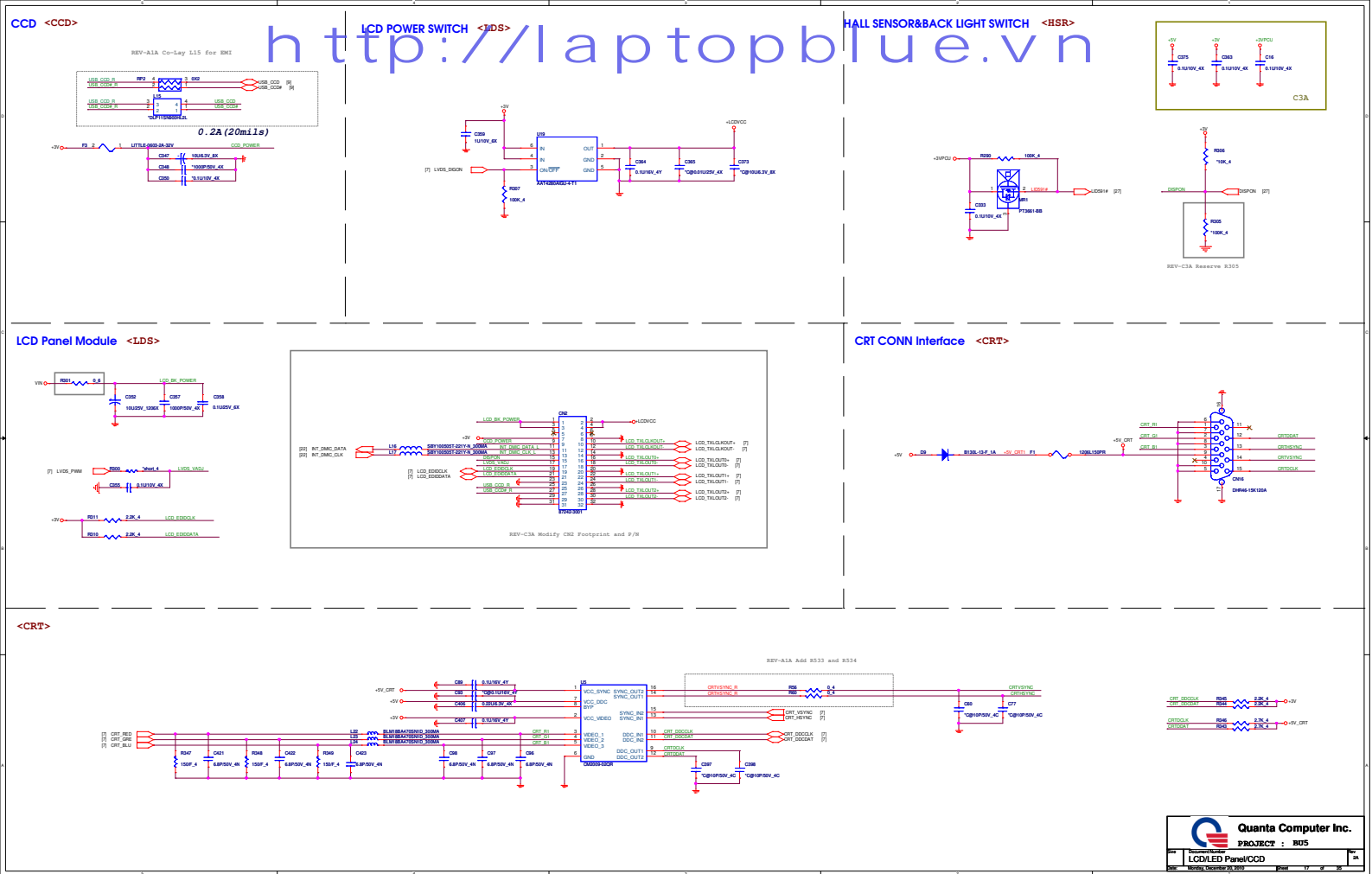
HDMI-passive level shift <HDM>



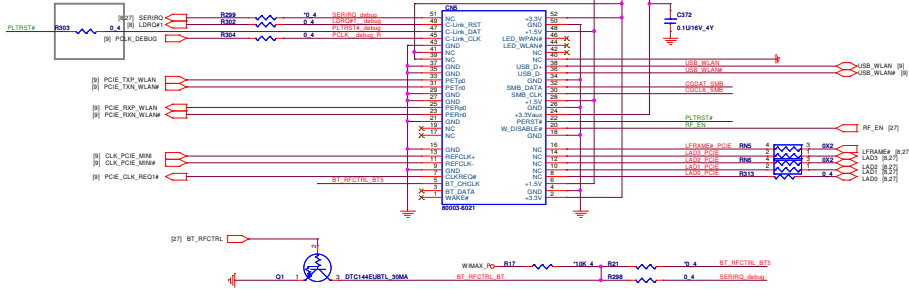
HDMI-HPD <HDM>



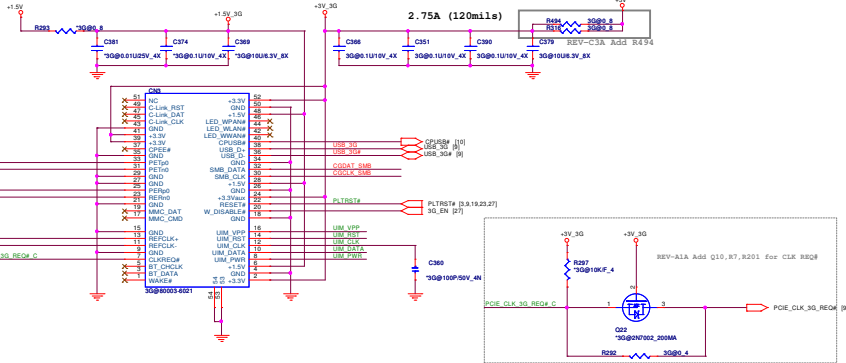
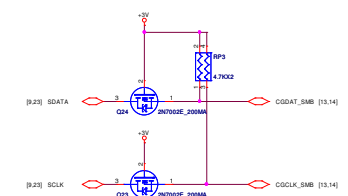
REV-A1A Del External HDMI-HPD



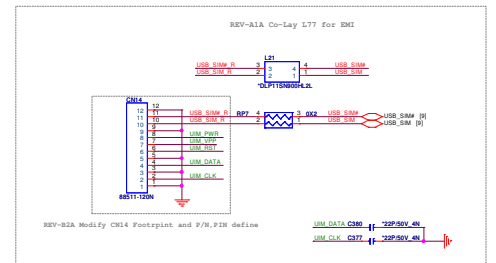
REV-C3A Modify R303 Value from 100K to 0

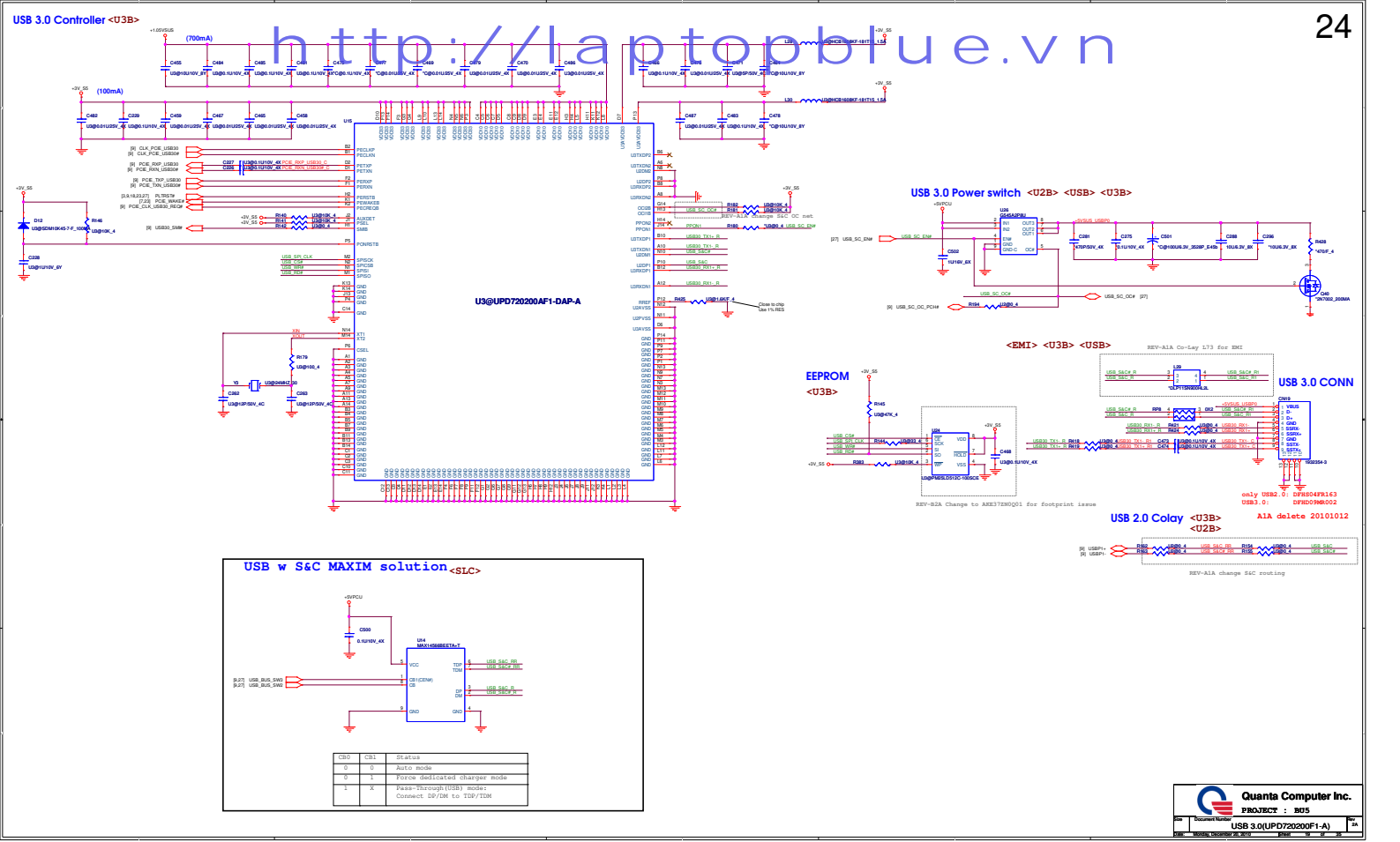


SMBus(DDR3/WLAN/3G)



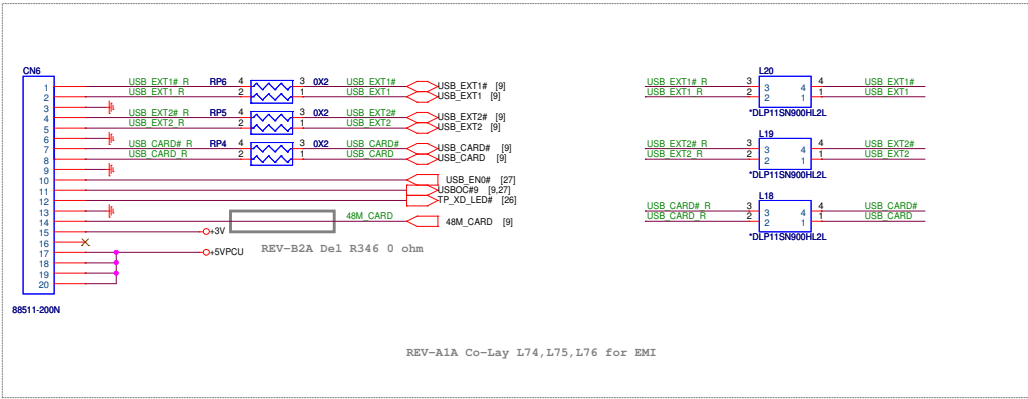
For SIM Card on daughter board

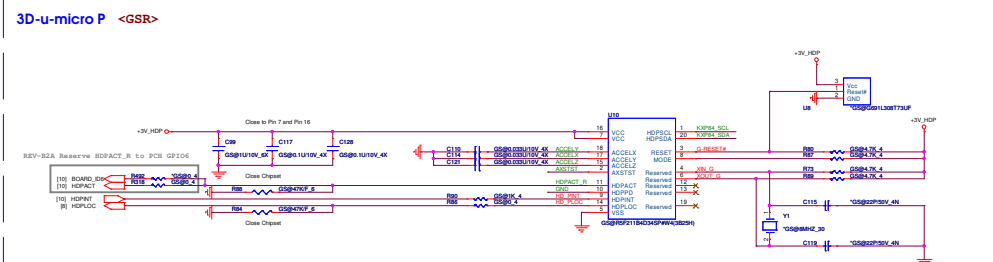
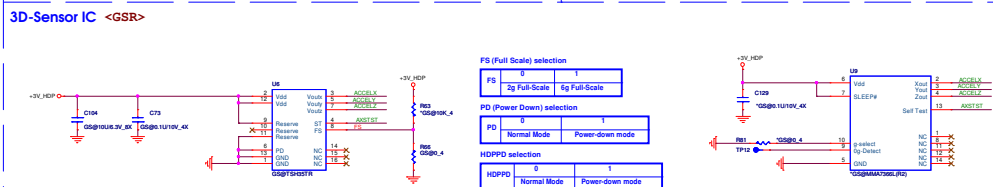
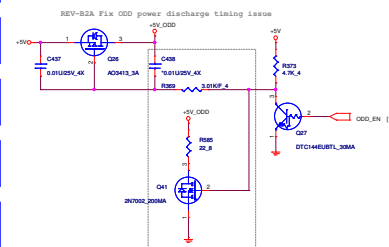


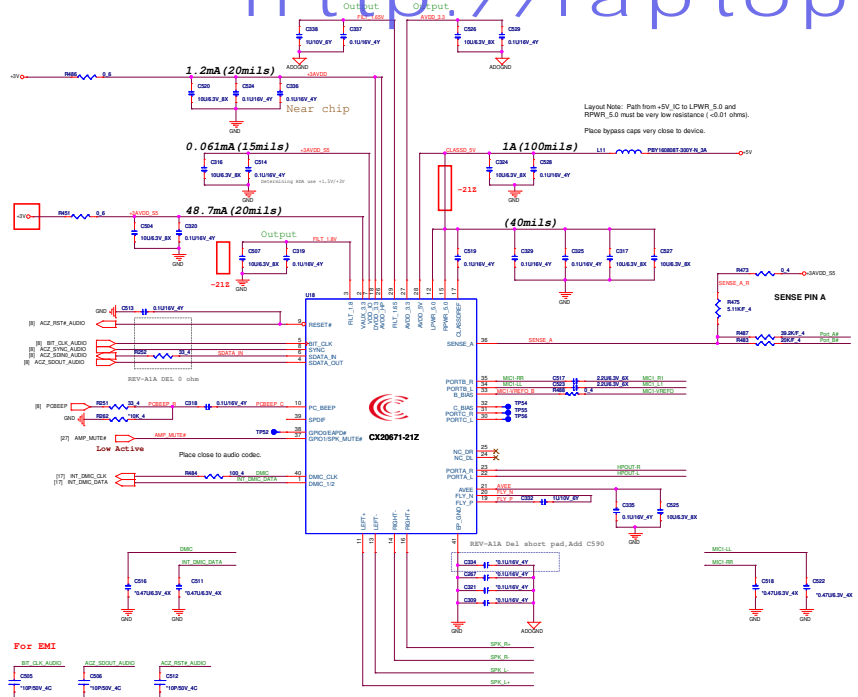


USB2.0 Left 1
USB2.0 Left 2 <U2B> <MMC> <USB> <EMI>

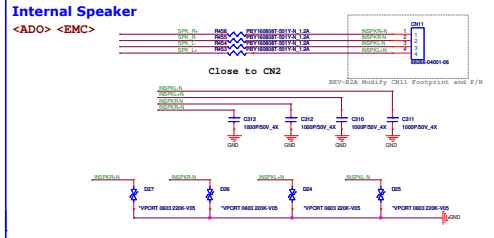
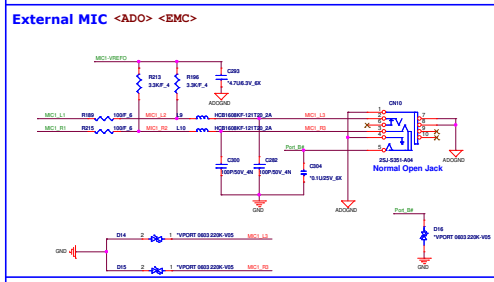
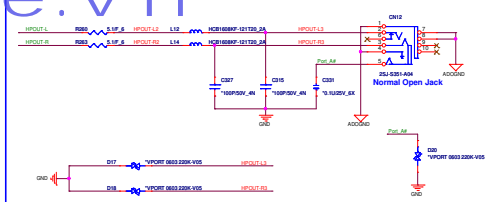
http://laptopblue.vn

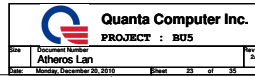
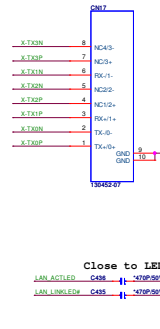
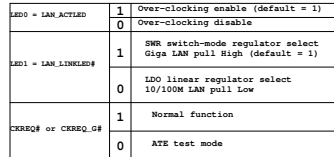
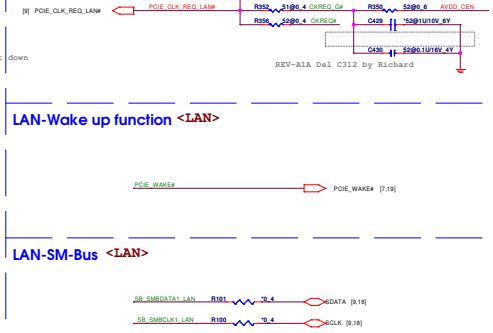




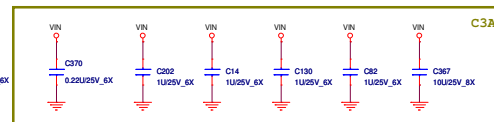
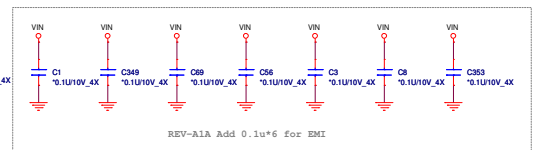
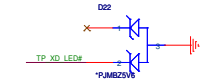
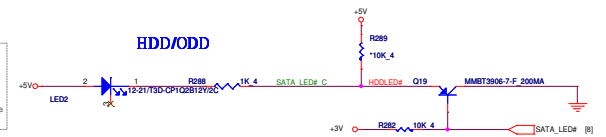


Need to change 20671-21Z footprint









0.01A (20mils)



Close to U12

AC SET_EC

8769AGND

ICMNT

8769AGND

C28

*10

C29

*10

