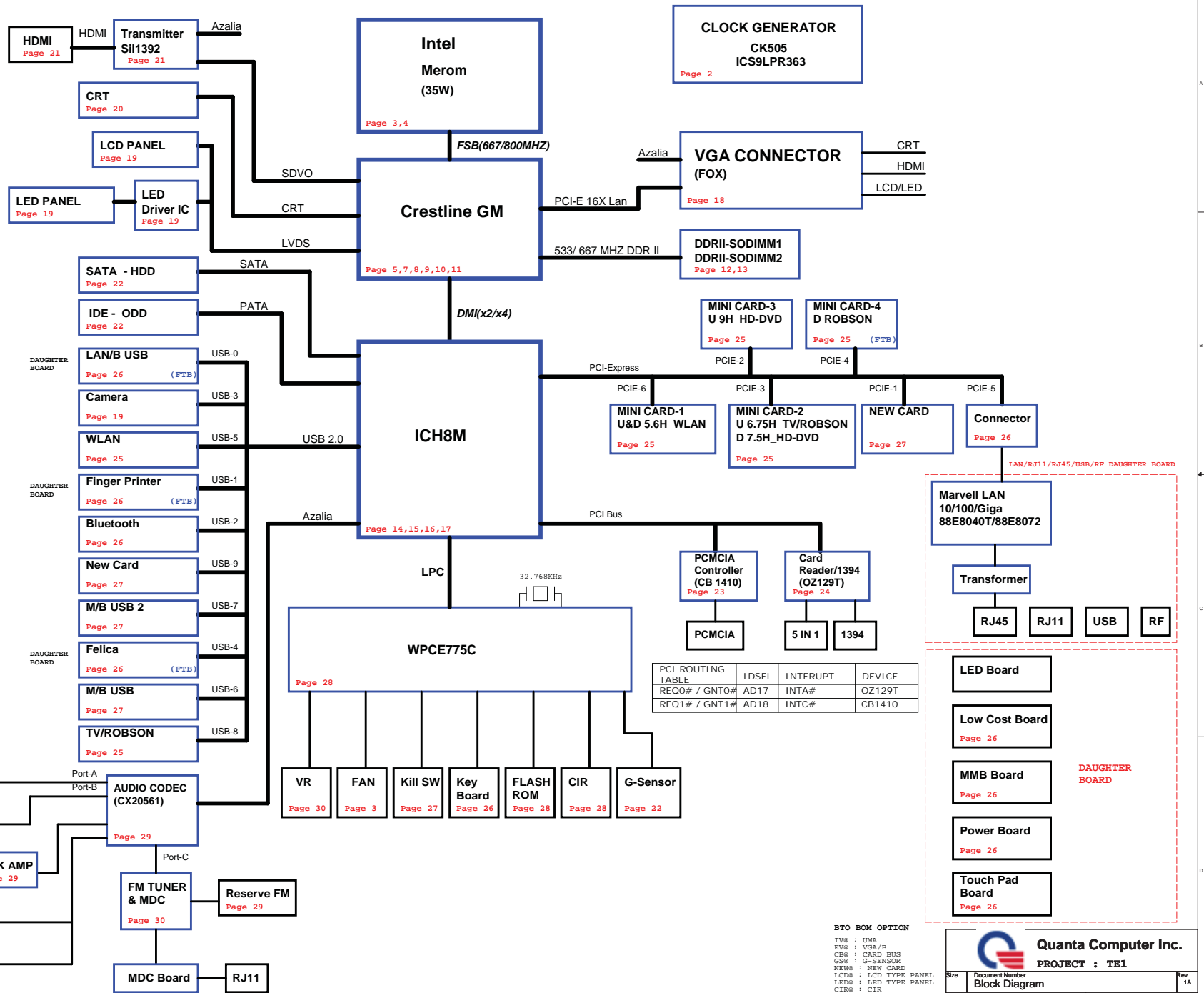


LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : VCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

+3VPCU
+3V_S5
+3VSUS
+3V
+5VPCU
+5V_S5
+5V
+SMDDR_VTERM
+SMDDR_VREF

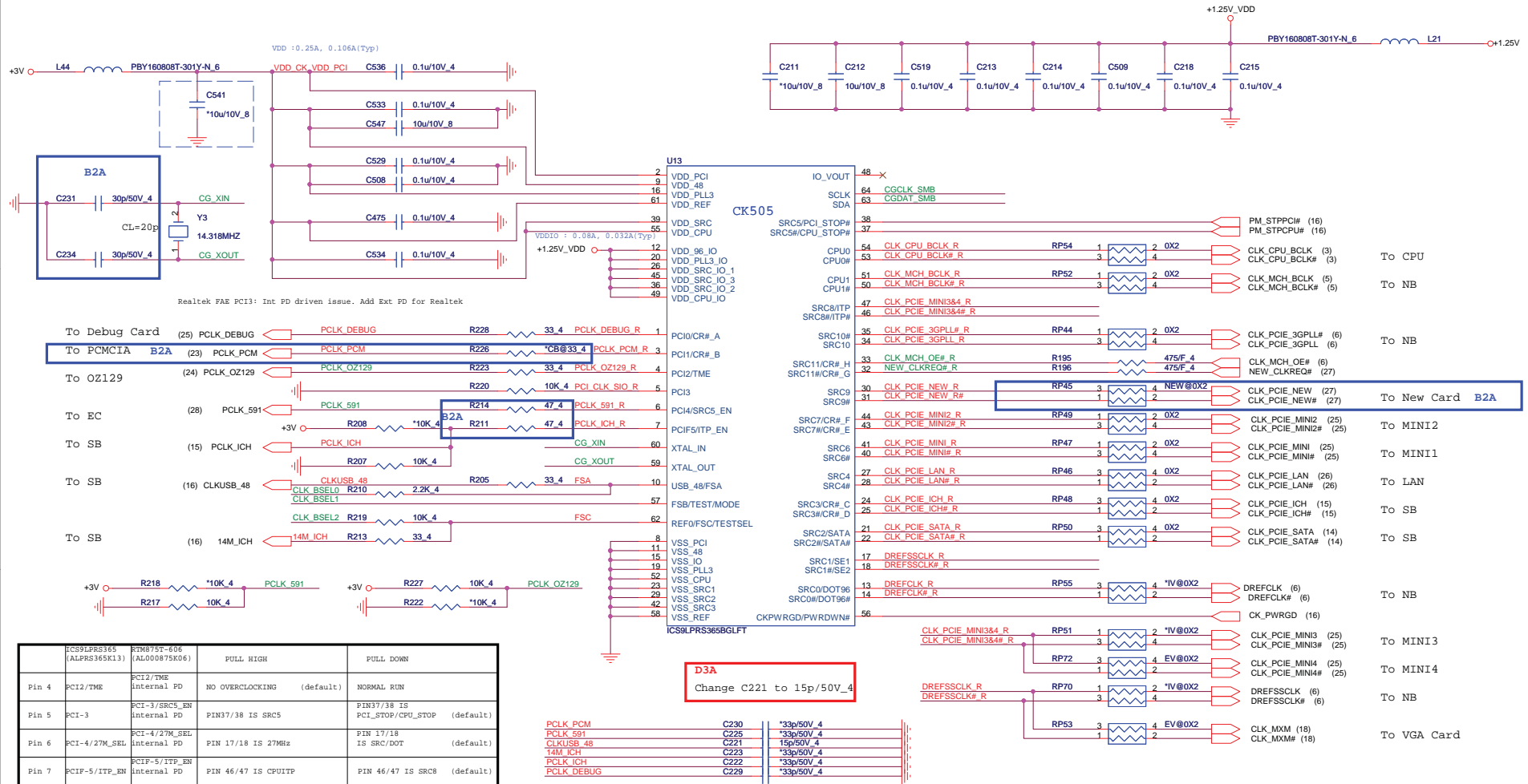


```

IV@  : UMA
EV@  : VGA/B
CB@  : CARD BUS
GS@  : G-SENSOR
NEW@ : NEW CARD
LCD@ : LCD TYPE PANEL
LED@ : LED TYPE PANEL
CIR@ : CIR

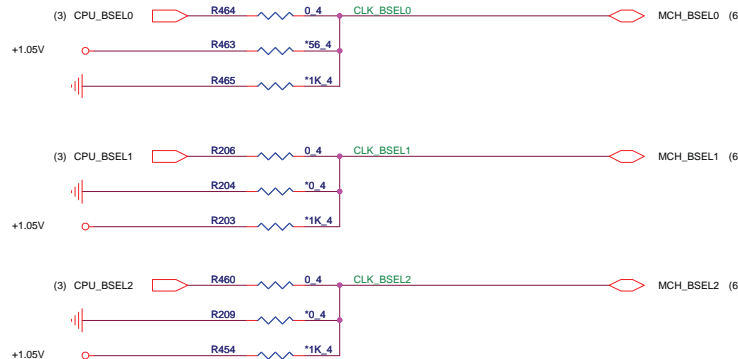
```

Clock Generator

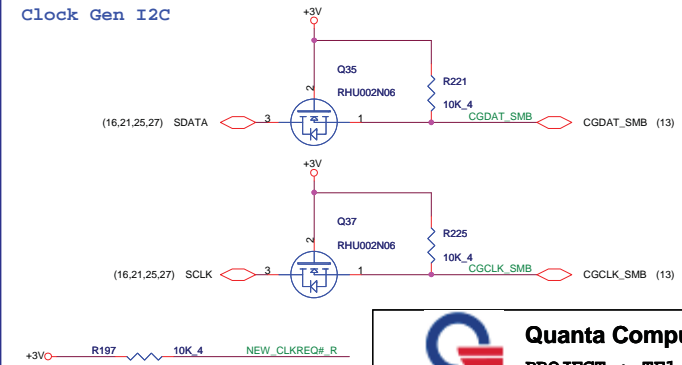


BSEL Frequency Select Table

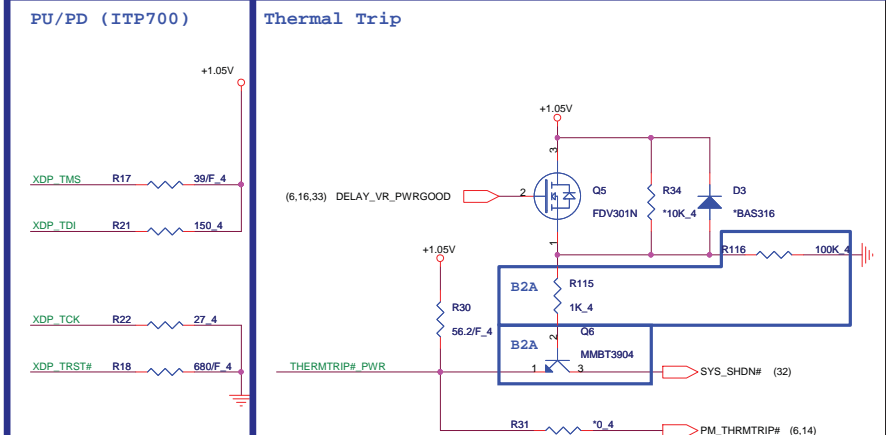
FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



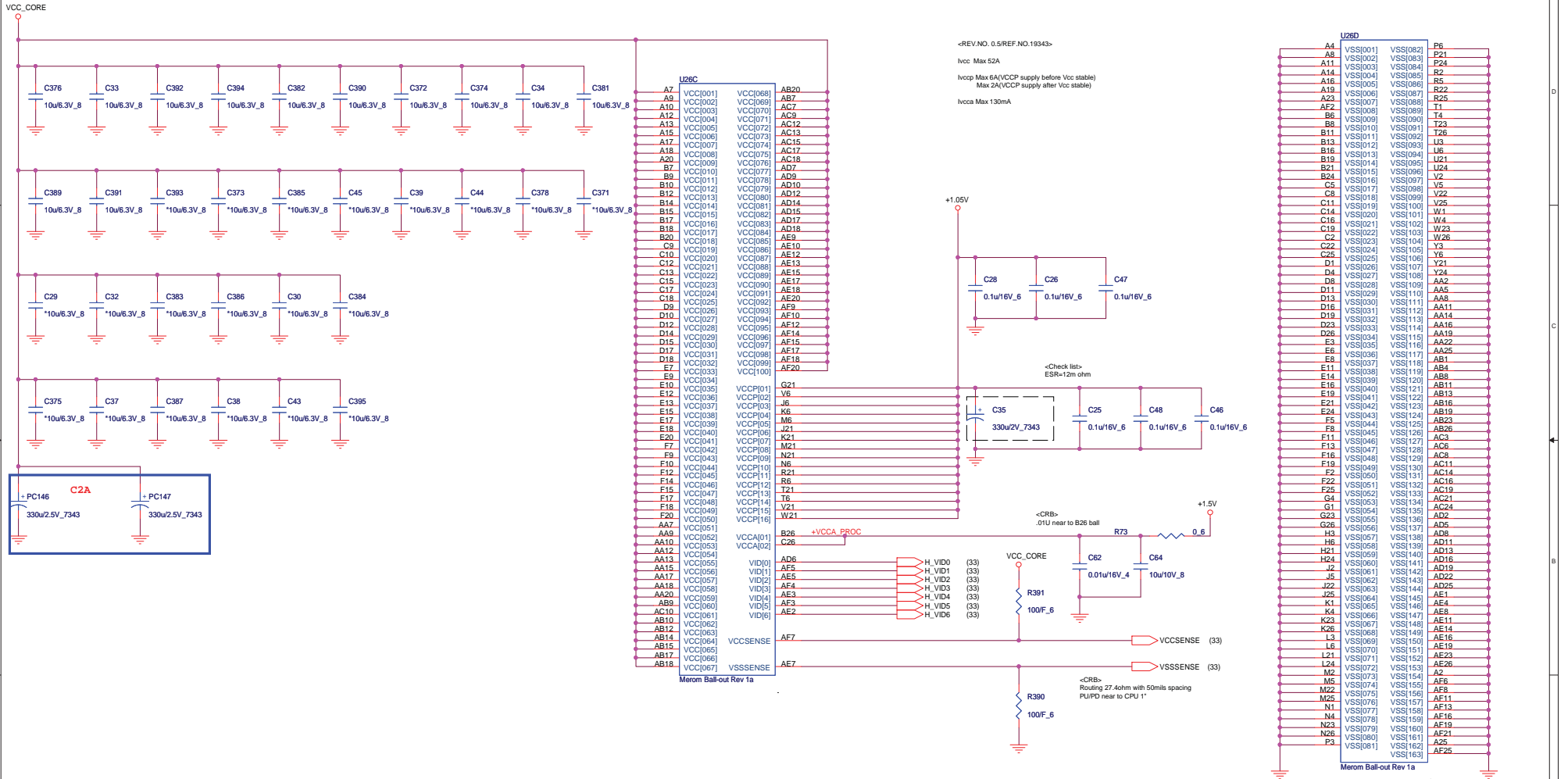
Clock Gen I2C



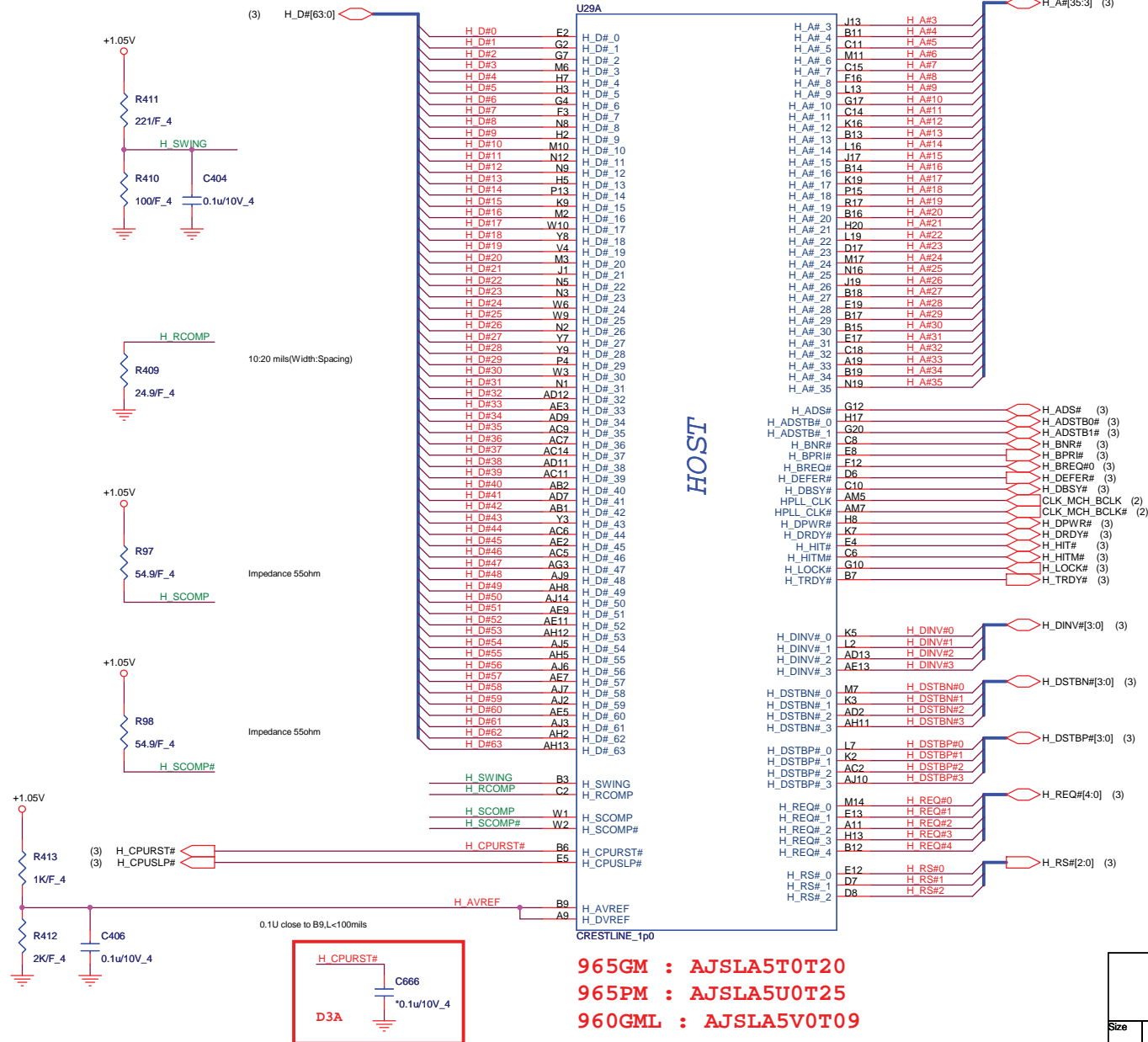
Thermal Trip



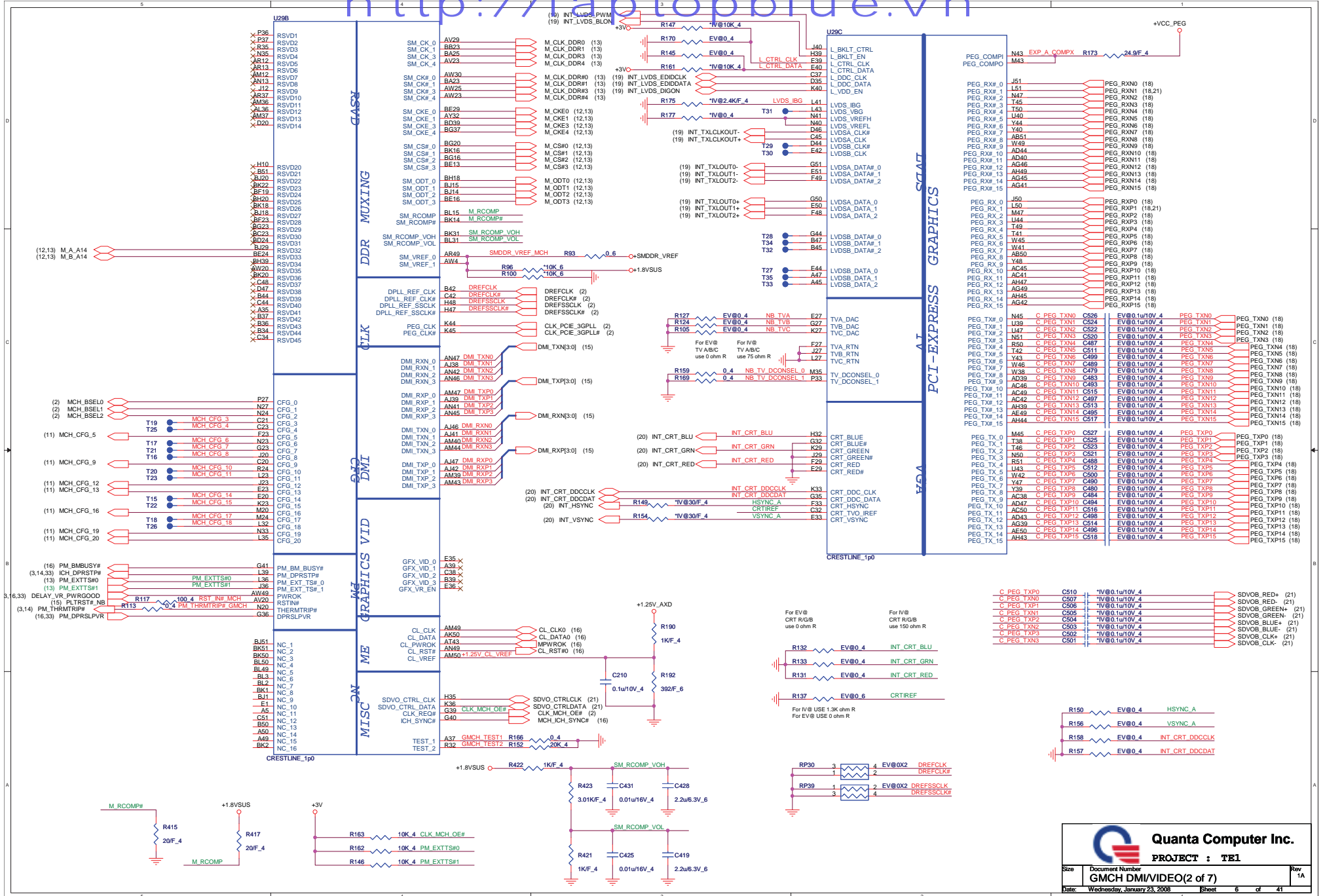
CPU (Power)

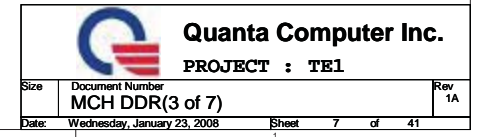


NB (HOST)

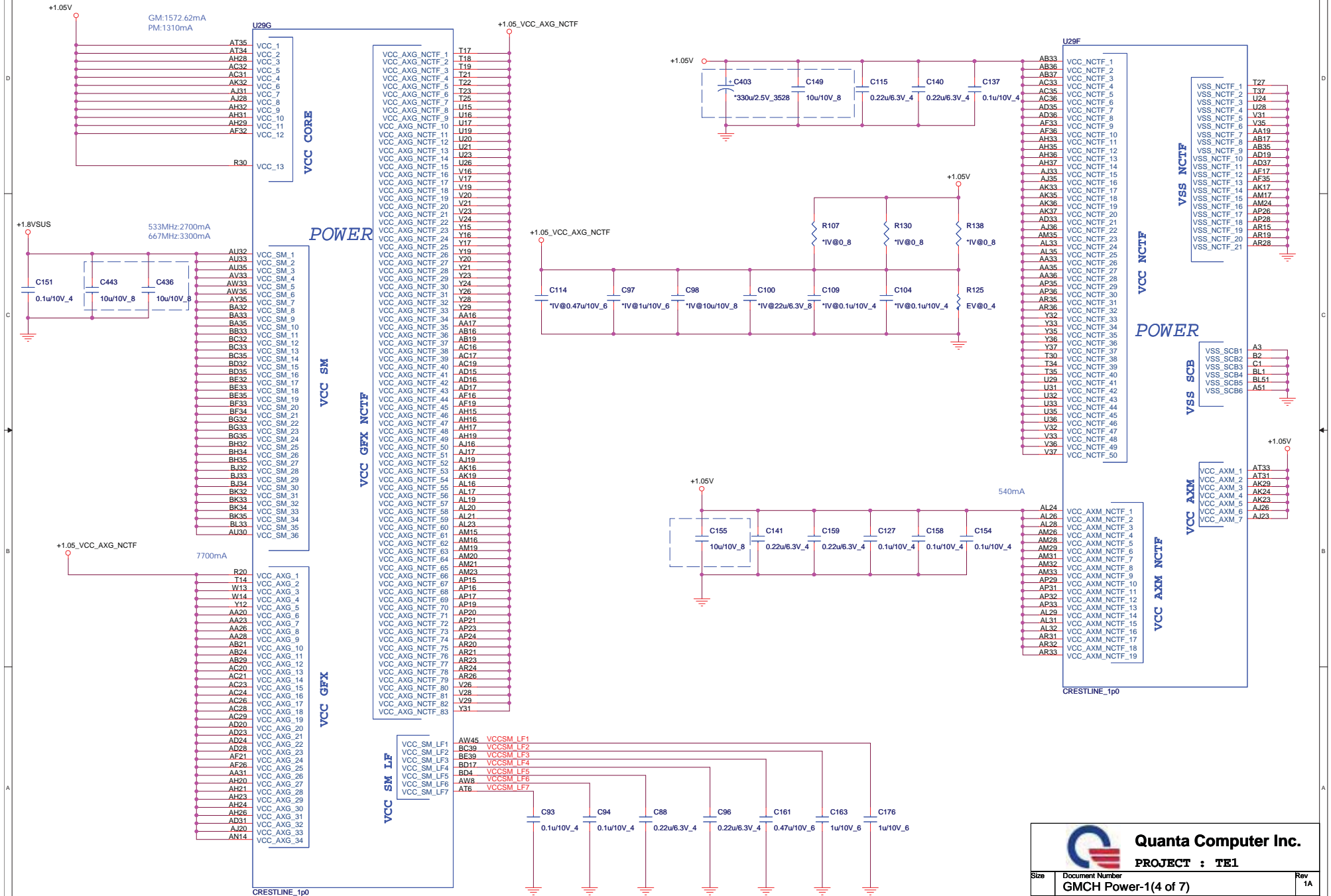


965GM : AJSLA5T0T20
965PM : AJSLA5U0T25
960GML : AJSLA5V0T09





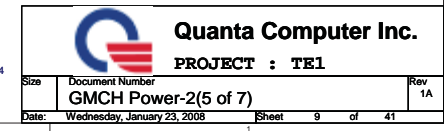
NB(Power-1)



LVDS Disable/Enable guideline

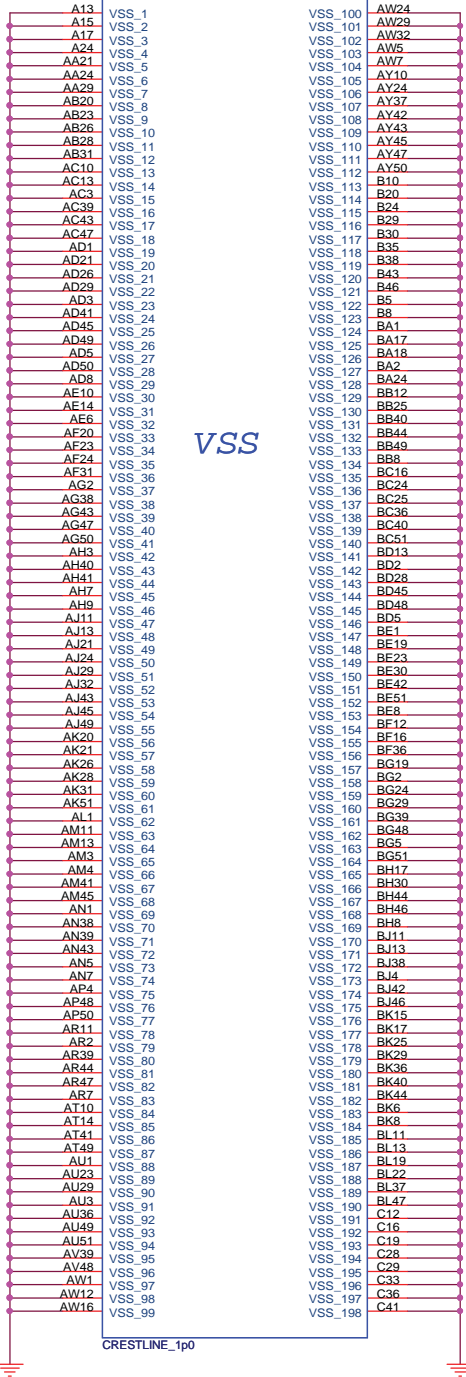
	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO LVDS
--	---------------------------------	--------------------------------	-----------------

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V
	EXTERNAL		INTERNAL



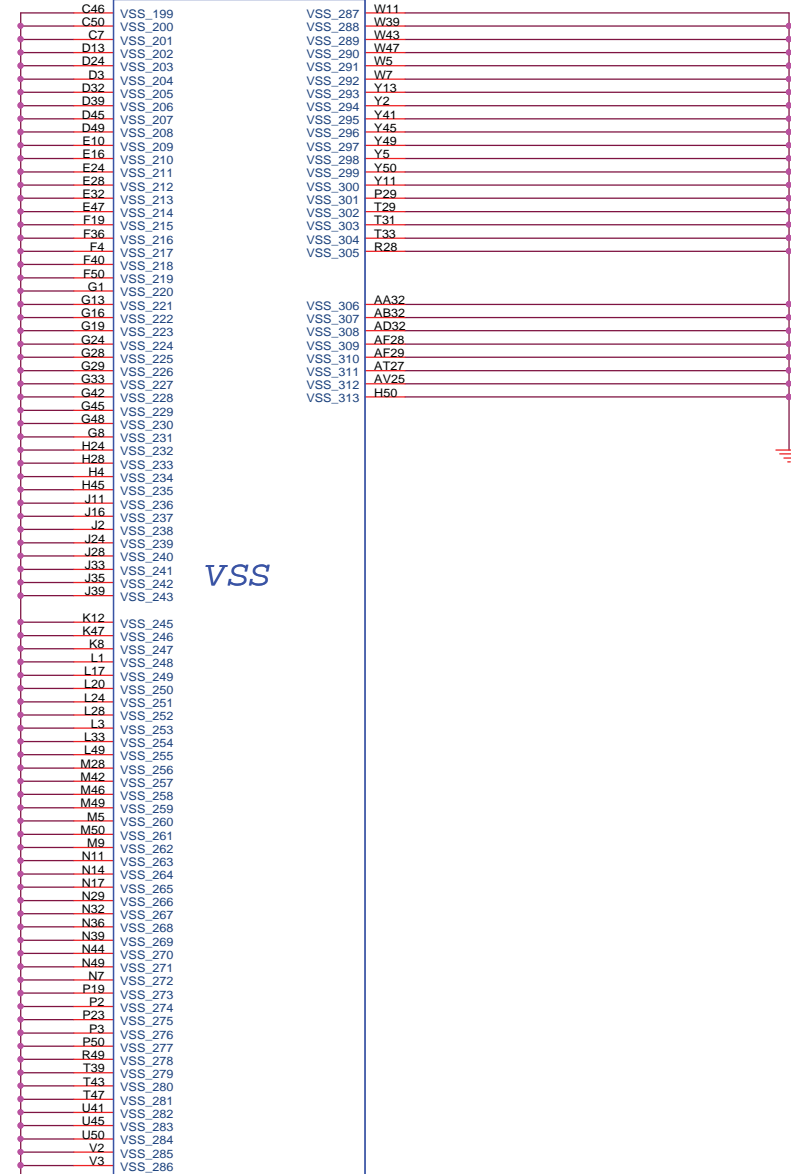
NB(Power-3)

U29I



CRESTLINE_1p0

U29J



CRESTLINE_1p0

Strap table(base on checklist Ver1.6)

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up

CFG[18:19] Have internal Pull-down

Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	Intel? Management Engine Crypto strap	0 = Intel? Management Engine Crypto Transport Layer.Security (TLS) cipher suite with no confidentiality 1= Intel Management Engine Crypto TLS Cipher Suite with confidentiality (default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE is operation(Default) 1 = SDVO and PCIE are operating simultaneously via the PEG port

DMI X2 Select

MCH_CFG_5	Low = DMIx2 High = IDMIx4(Default)
-----------	---------------------------------------



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
------------	--



FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
------------	---



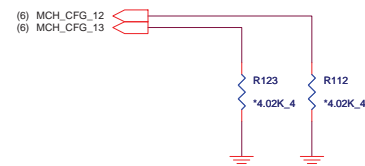
SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE is operational(Default) High = SDVO and PCIE are operating simultaneously via the PEG port
------------	---



XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
-----------	--

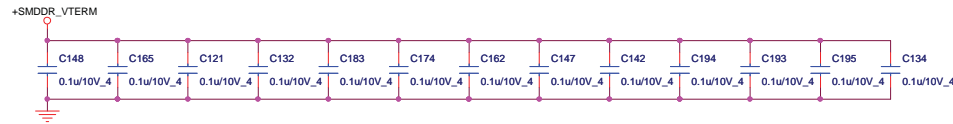


SDVO Present

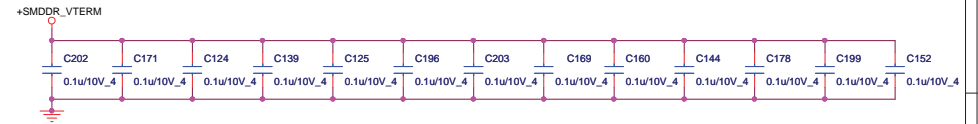
Strap define at External
HDMI control page

DDR2 A CHANNEL

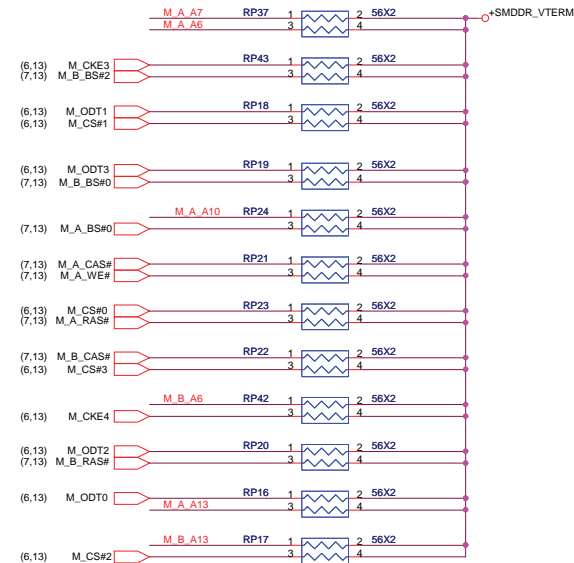
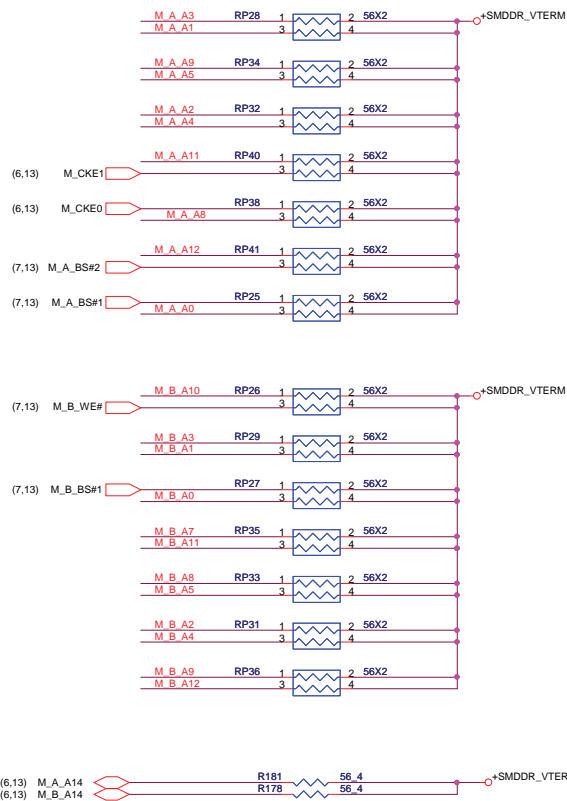
M_A_A[13..0] M_A_A[13..0] (7,13)
M_B_A[13..0] M_B_A[13..0] (7,13)



DDR2 B CHANNEL

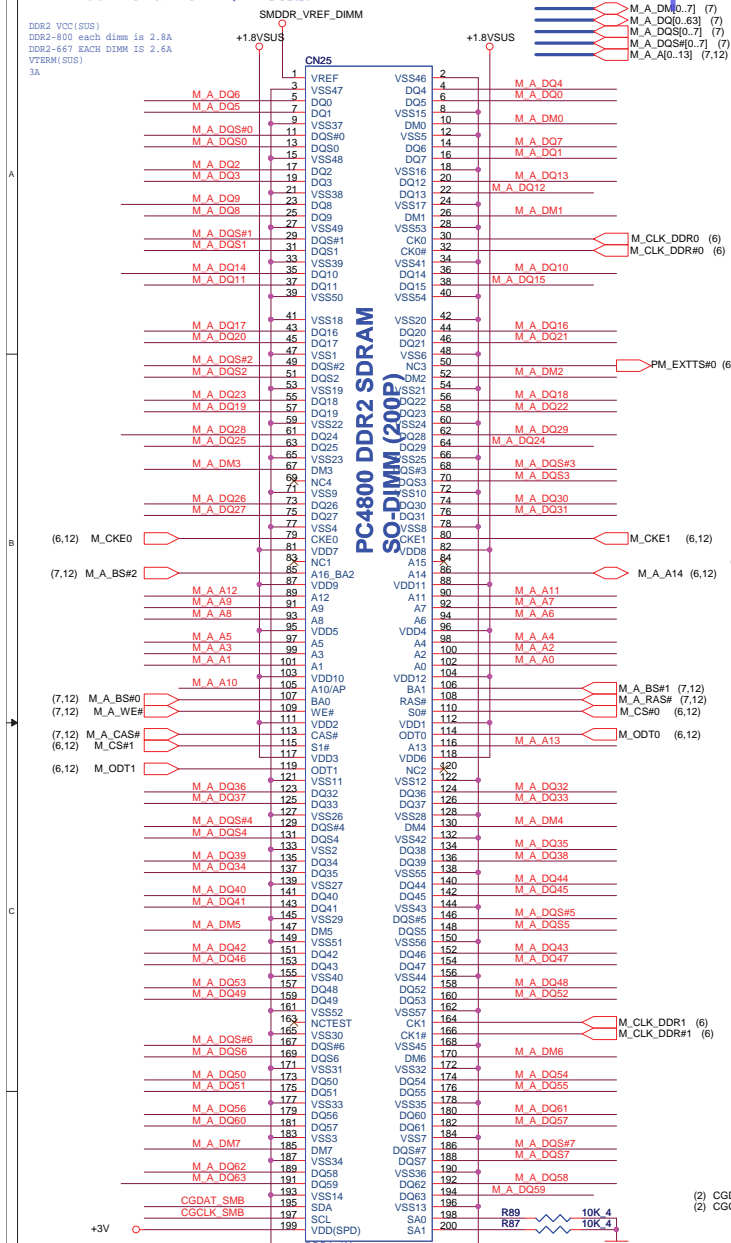


Place one cap close to every 2 pull-up resistor terminated to SMDDR_VTERM



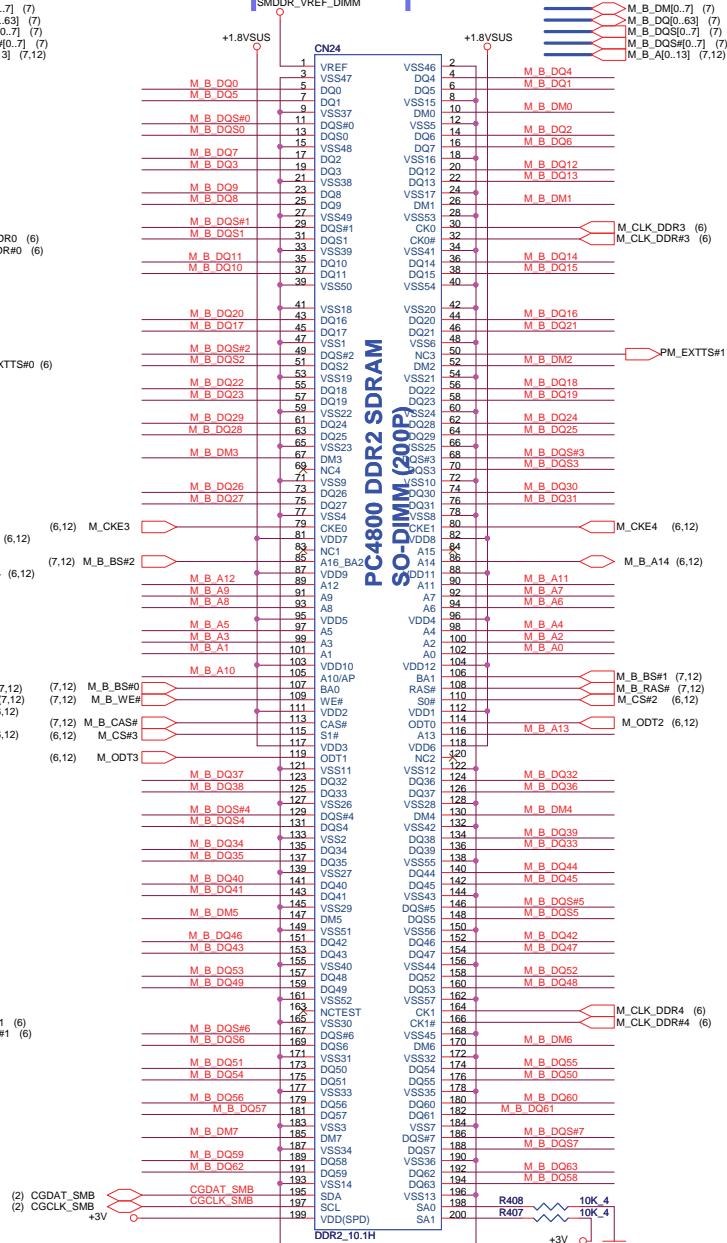
	DDR2 Dual channel A/B CONN	
--	----------------------------	--

```
DDR2 VCC(SUS)
DDR2-800 each dimm is 2.8A
DDR2-667 EACH DIMM IS 2.6A
VTERM(SUS)
3A
```



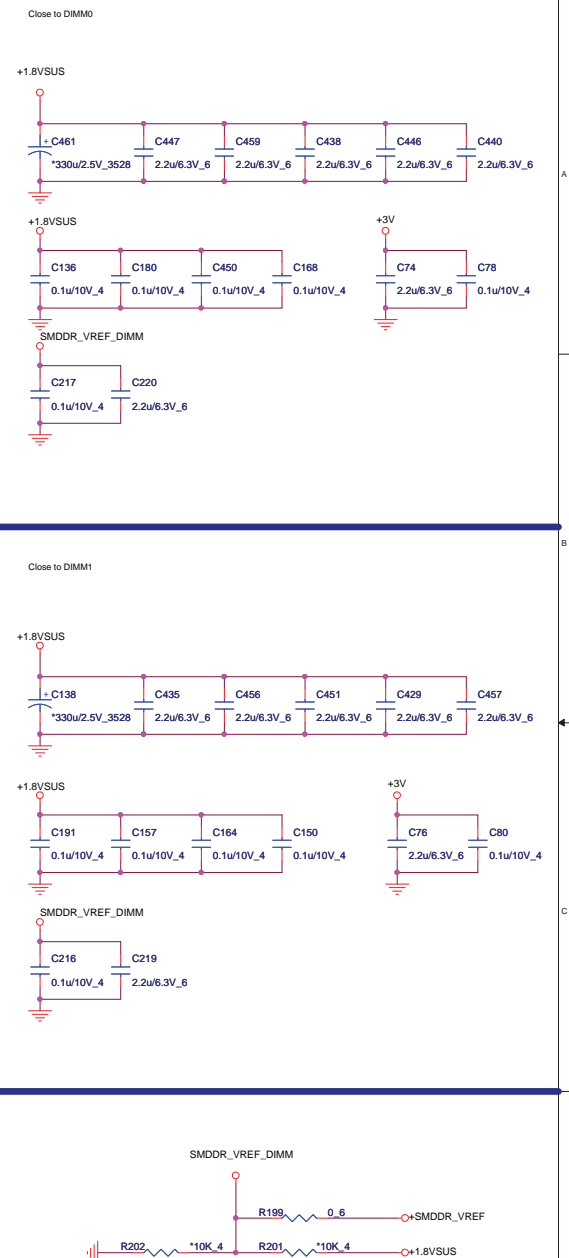
H: 6mm

CLOCK 0,1
CKE 0,1



H: 10.1mm

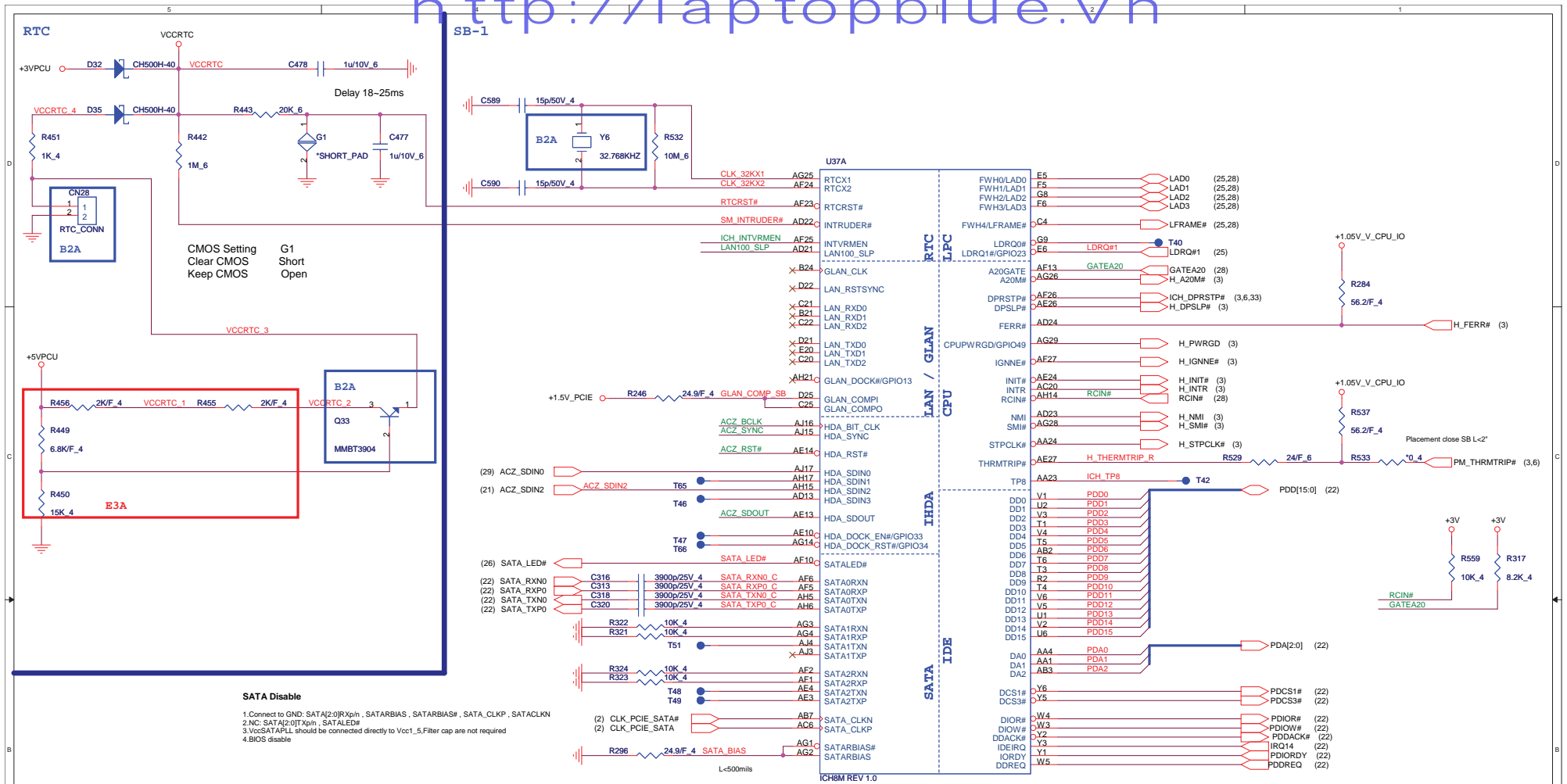
CLOCK 3,4
CKE 2,3



Quanta Computer Inc.

PROJECT : TE1

Size	Document Number DDR SO-DIMM(200P)	Rev 1A
Date:	Wednesday, January 23, 2008	Sheet 13 of 41

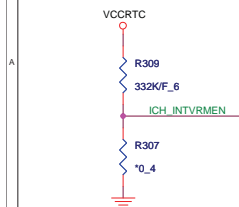


SB Strap

ICH8-M Internal VR Enable strap

(Internal VR for Vccsus1_05, Vccsus1_5 and VccCL1.5)

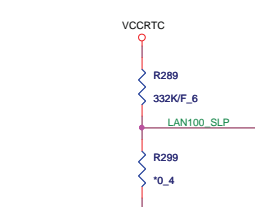
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
----------	---



ICH8-M LAN100_SLP Strap

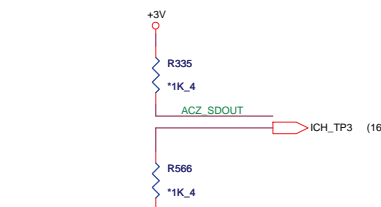
(Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---

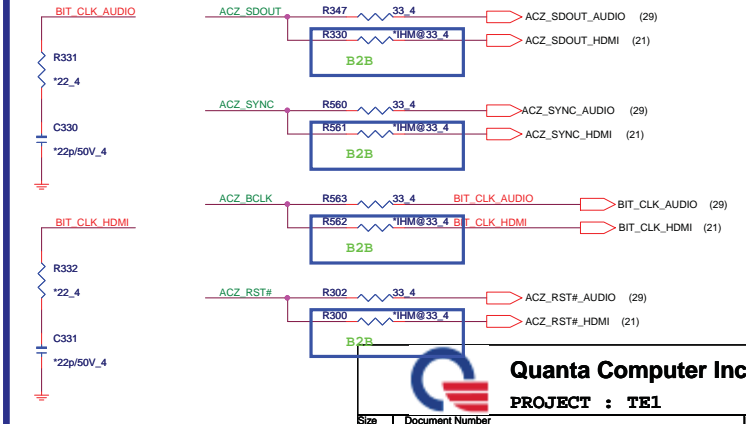


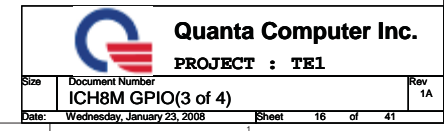
XOR Chain Entrance Strap

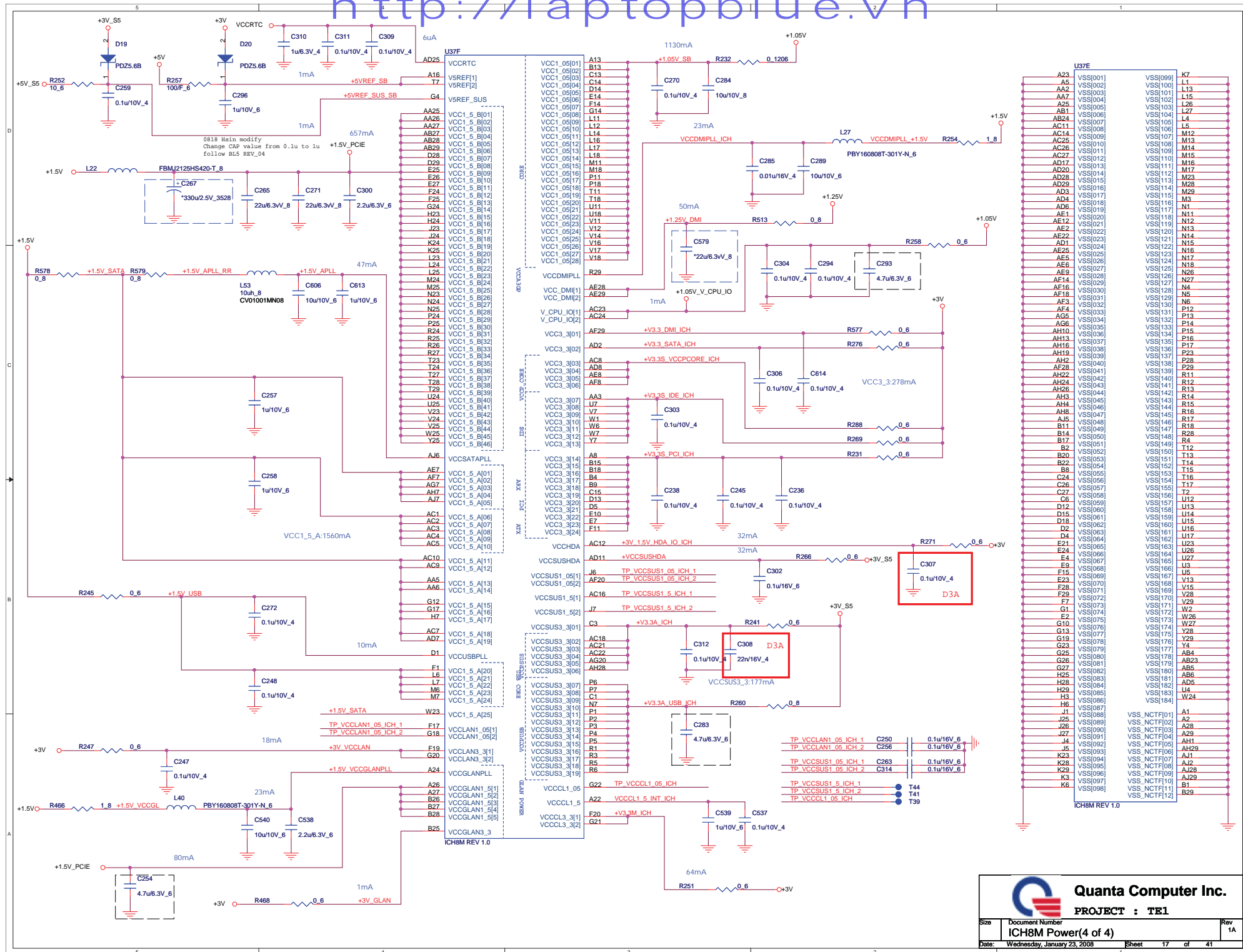
ICH_RSVO	HDA_SDOOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCI port config bit 1

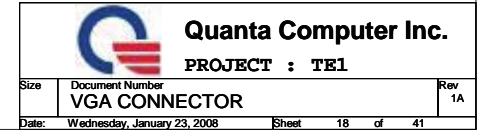


HDA

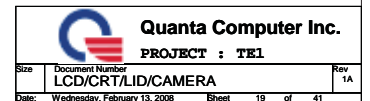




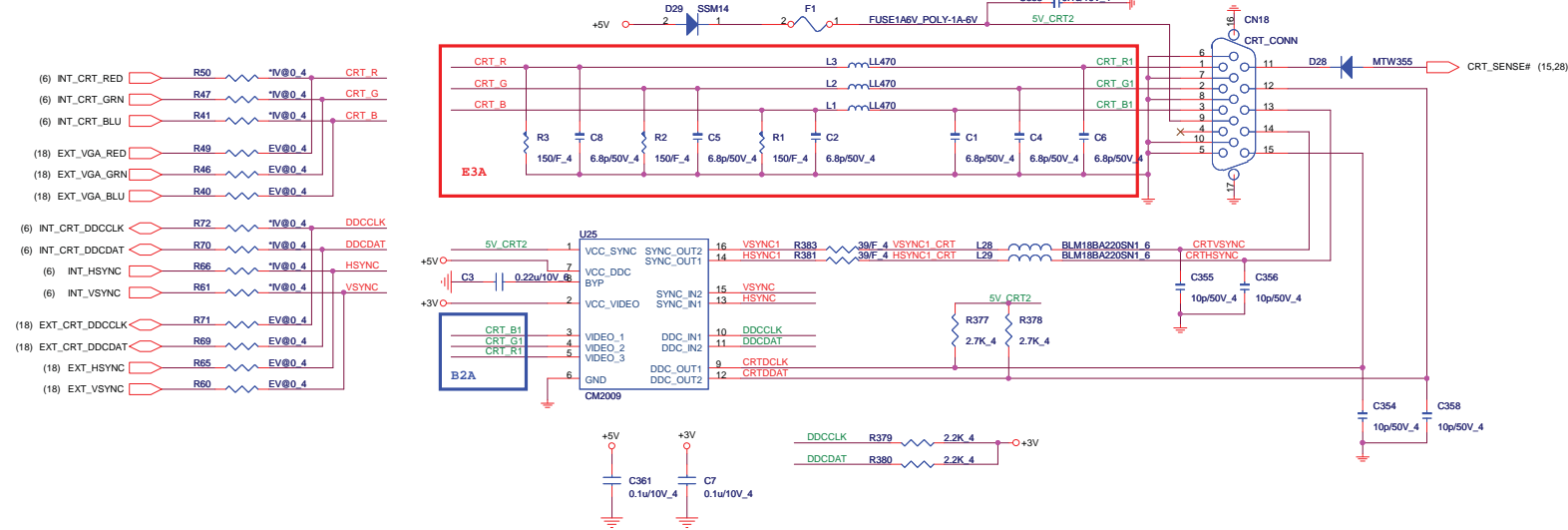




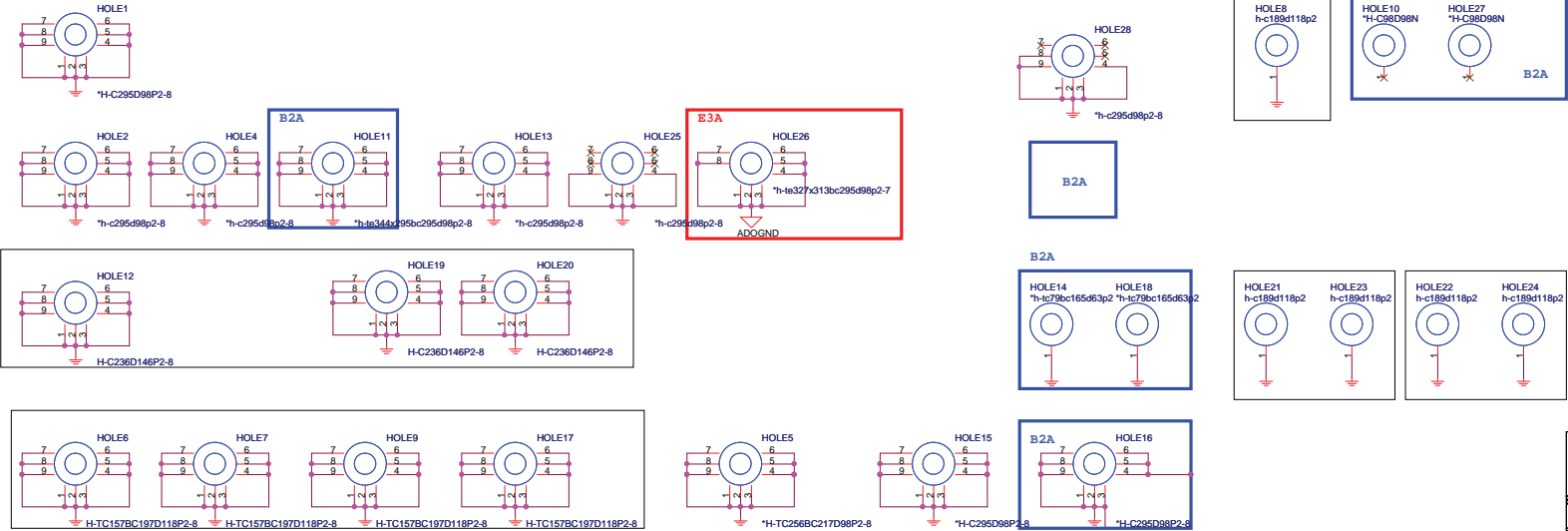
Panel source



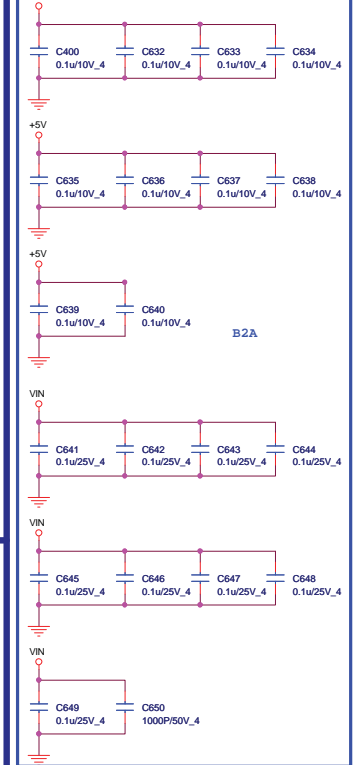
CRT



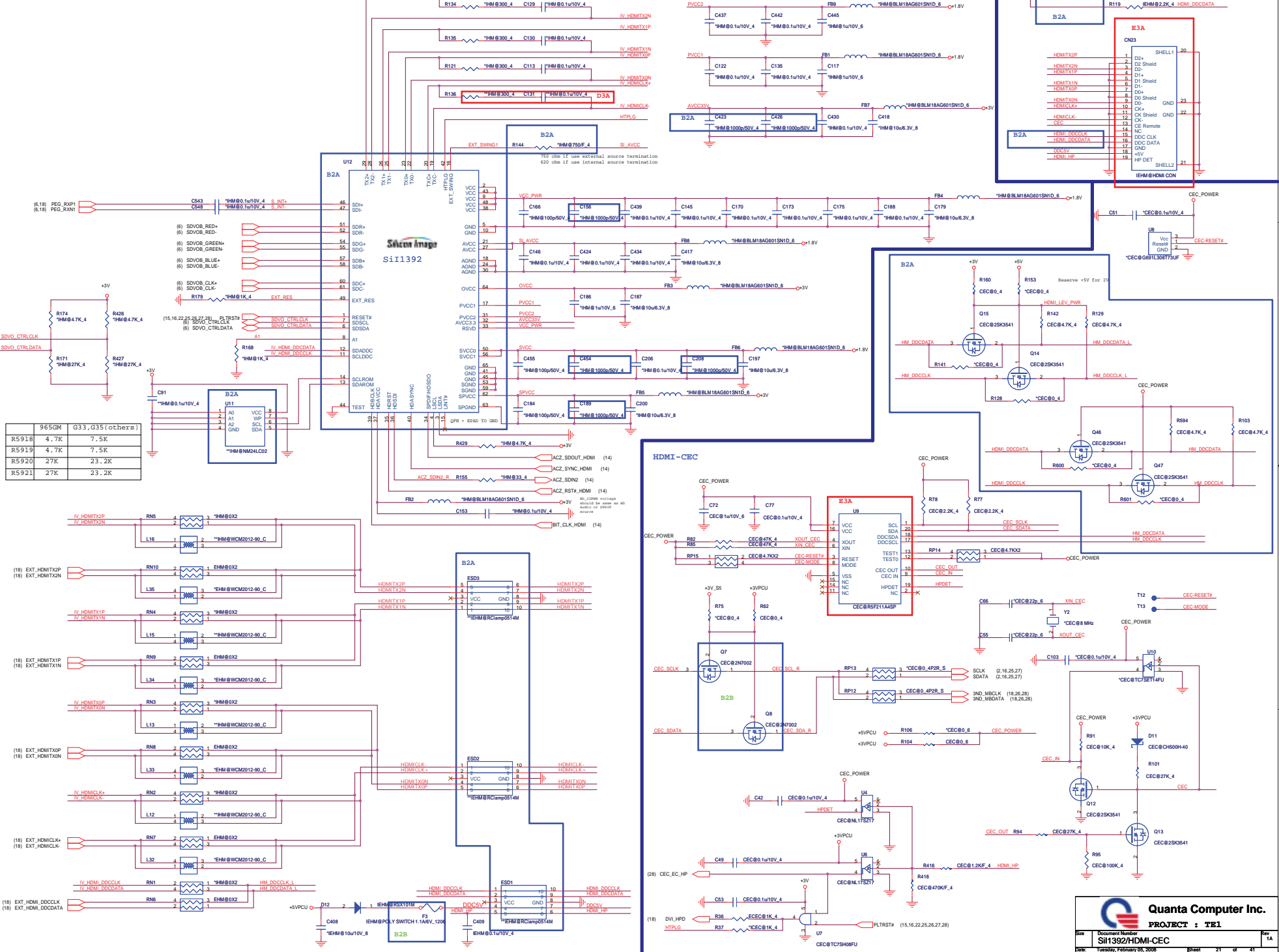
HOLE



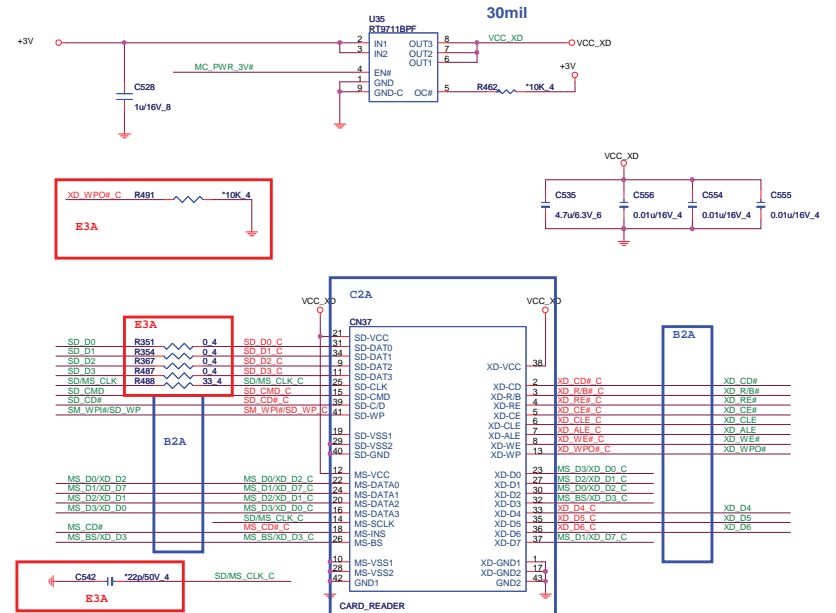
EMI



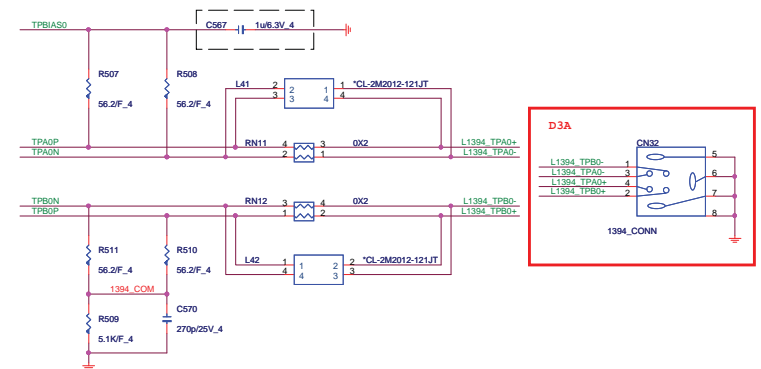
Si11392 HDMI

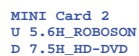



5 IN 1 Card reader



1394



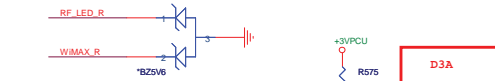


 Quanta Computer Inc. PROJECT : TE1	
Size	Document Number MINI CARD
Date: Thursday, January 31, 2008	Sheet 25 of 41

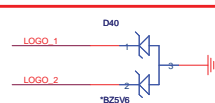
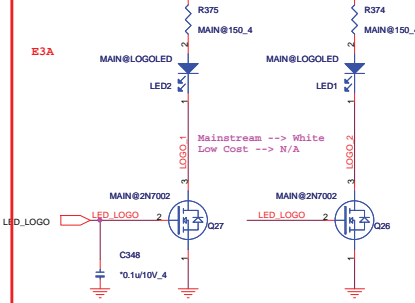
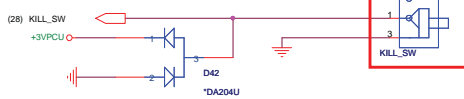




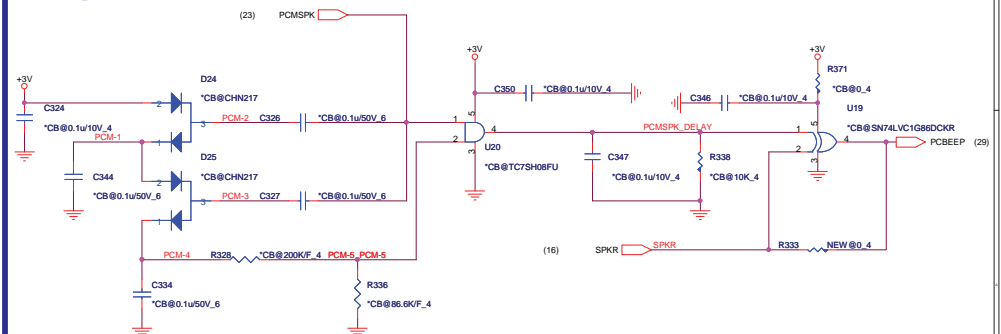
Mainstream --> Orange
Low Cost --> Orange



Kill SW



PC-Beep



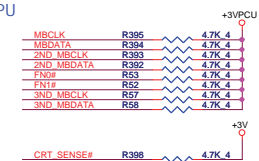


SMBUS	Devices
1	Battery
2	CPU Thermal Sensor 3D Sensor EC EEPROM
3	VGA Board Thermal Sensor Touch Sensor

To: Battery connector

To: CPU Thermal Sensor, 3D Sensor, EC EEPROM

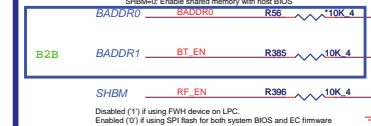
To: VGA Board Thermal Sensor, Touch Sensor



I/O Base Address

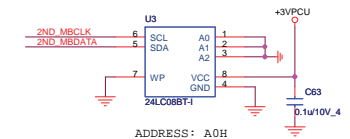
	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

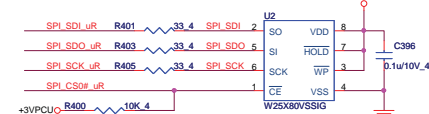


Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID



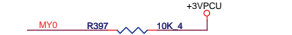
SPI FLASH



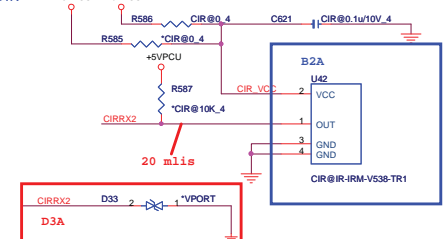
2nd source

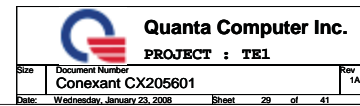
MXIC	MX25L8005M2C-15G	AKE5GFK0Z
Winbond	W25X80VSSIG	AKE3GFP0N
RON	EN25F80-75HCP	AKE3GZP0Q

INTERNAL KEYBOARD STRIP SET

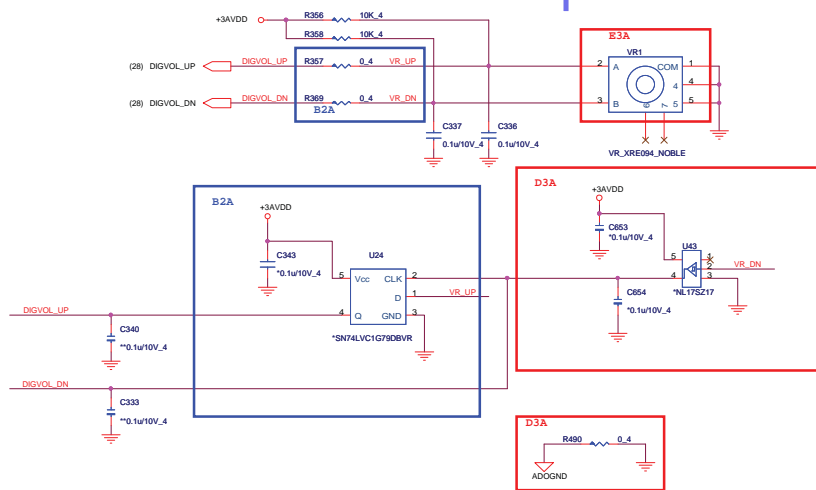


C

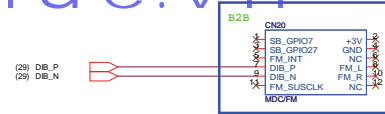




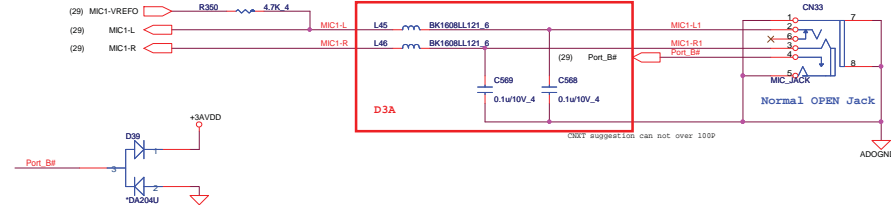
VR



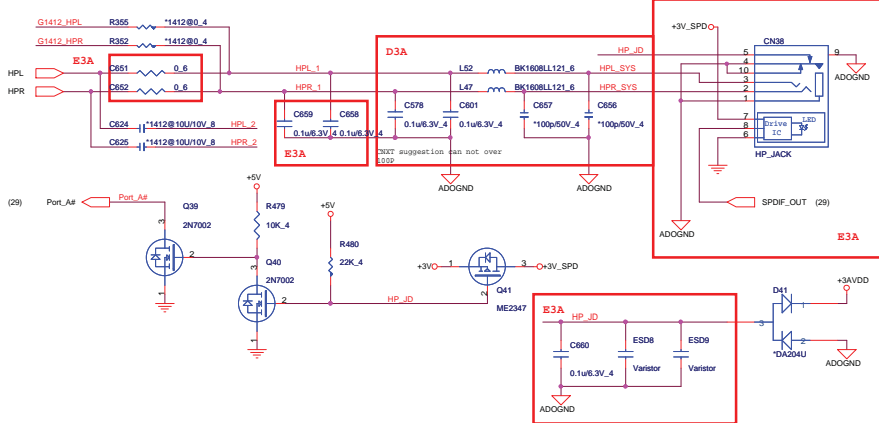
MDC



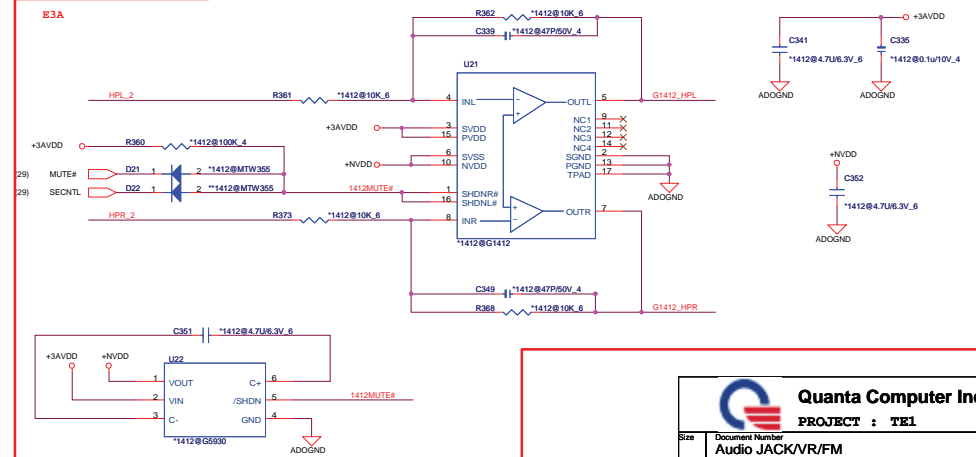
SYSTEM MIC

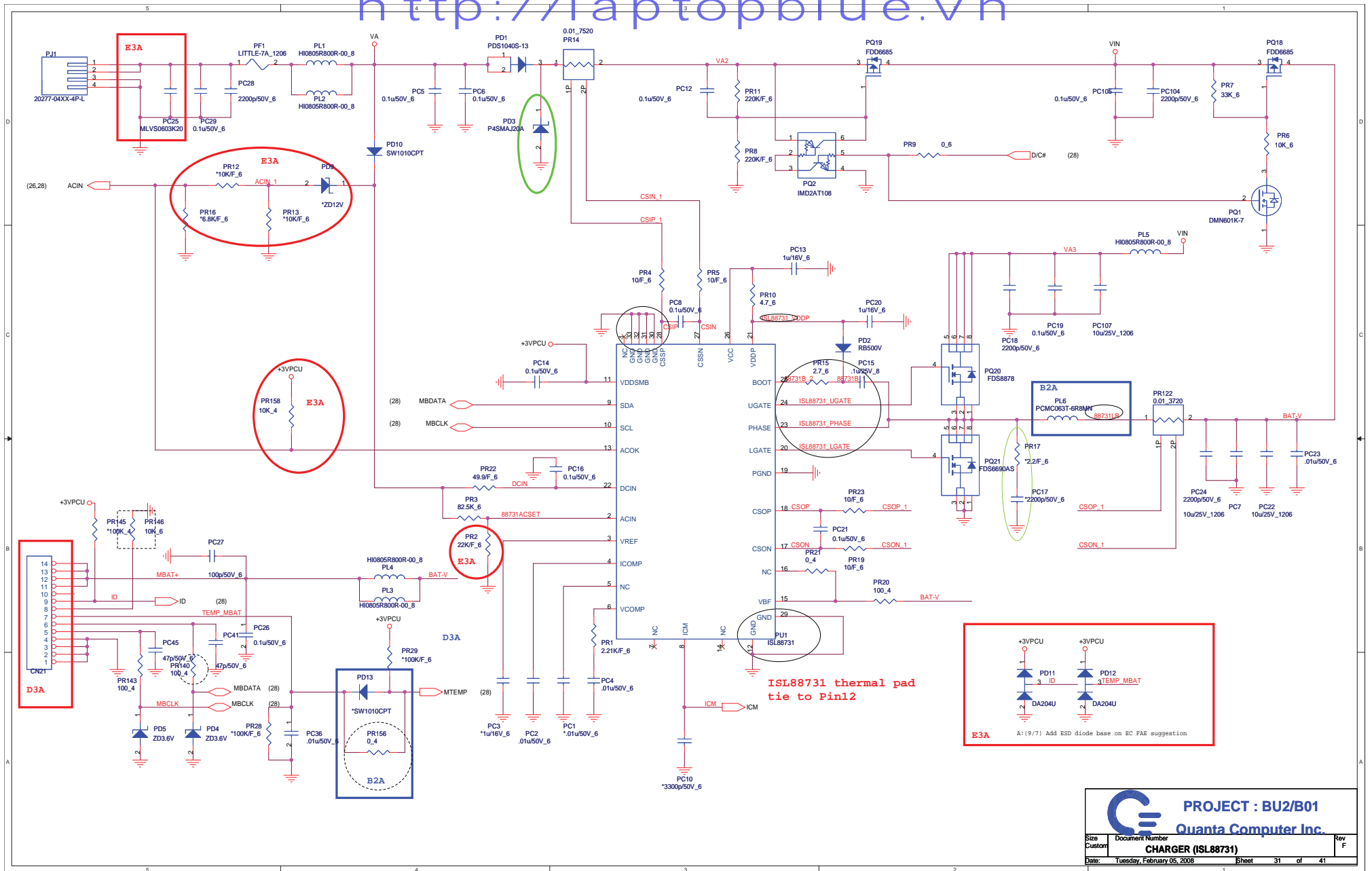


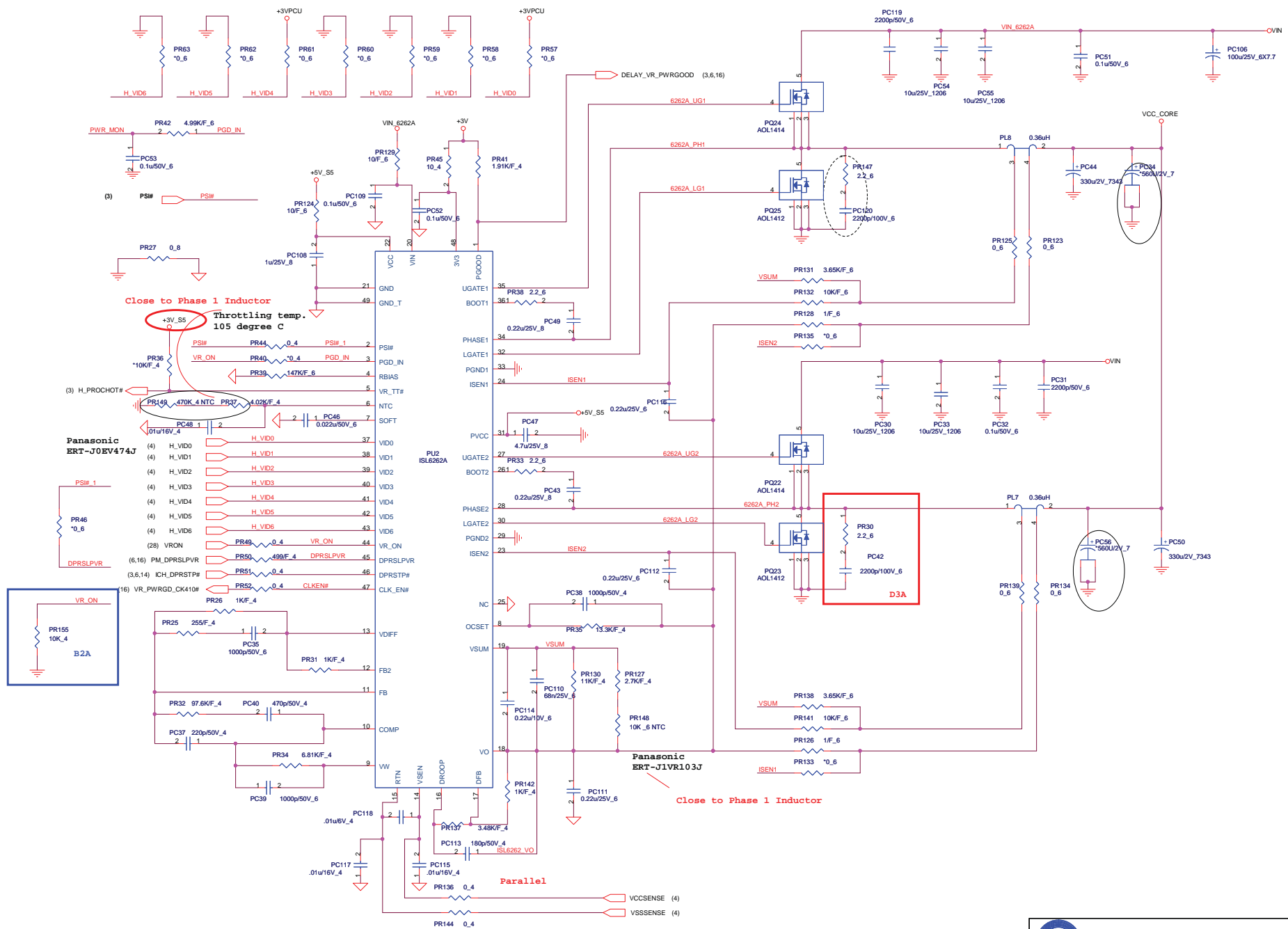
HP

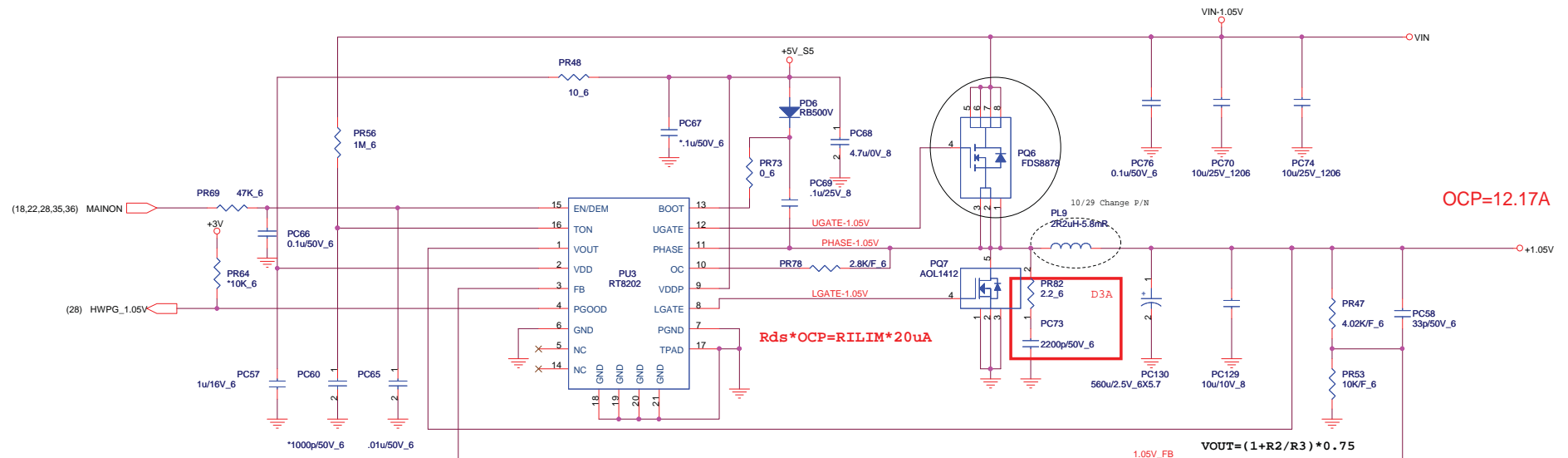


HP Amplifier









OCP=12.17A

$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$R_{ds} * OCP = R_{ILIM} * 20uA$$

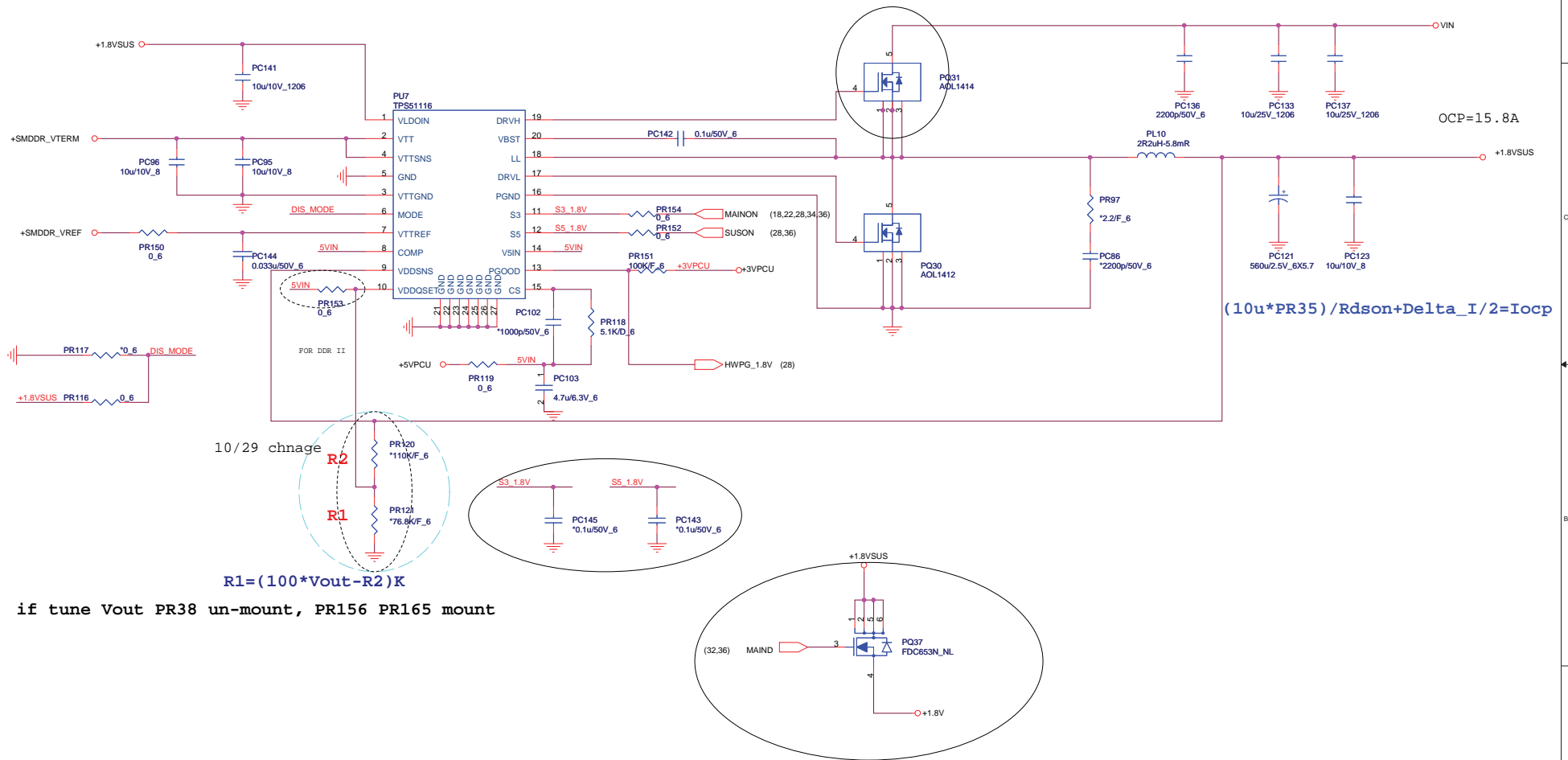
$$AO1412 \quad R_{ds} = 4.6m\Omega$$

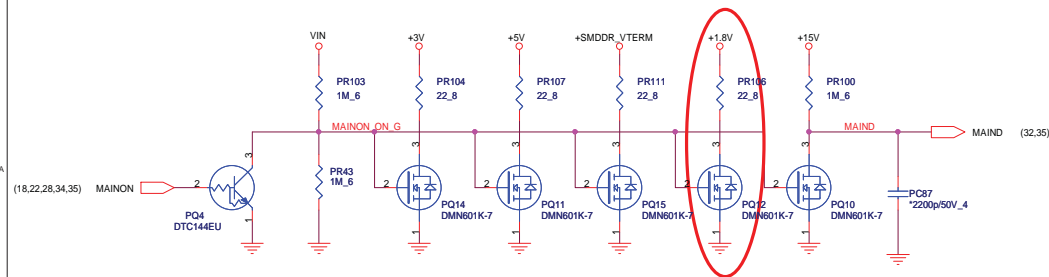
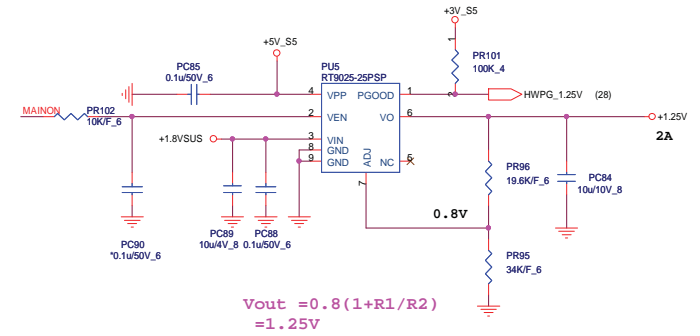
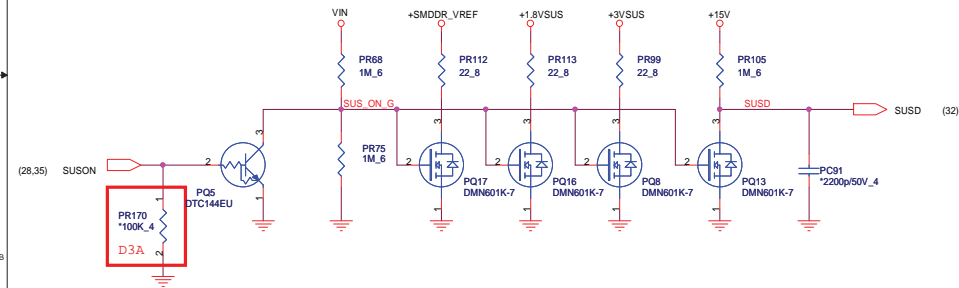
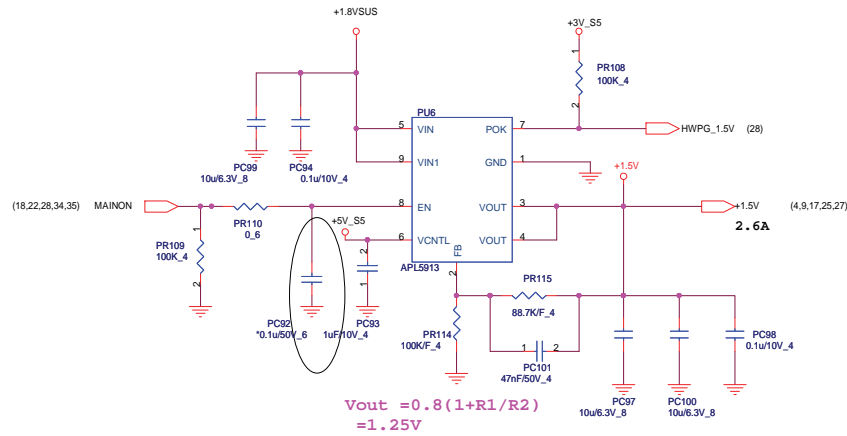
$$12.17A \quad OCP \quad --- \quad OC = 2.8K (CS22803F914)$$



PROJECT : BU2/B01
Quanta Computer Inc.

Size	Document Number	Rev
	VT1 1.05V (RT8202)	1D
Date:	Wednesday, January 23, 2008	Sheet 34 of 41





Model	REV	DATE	CHANGE LIST	NOTE
TE1	01	20070824	FIRST RELEASED : 20070824	
	A1A	20070927	FIRST RELEASED : 20070927	
	B2A		<p>Page 22 : U31 for G-sensor SKU must stuff, and add GS@ for BOM clear.</p> <p>Page 22 : Change Y4/C476/C485 Value from * to **, because Sensor function default not need that.</p> <p>Page 3/14 : Q6/Q9/Q33 BA039040039 change to BA0390400H0 for before BA039040039 cause RTC charger issue</p> <p>Page 28 : Change SW1 to short PAD for debug only</p> <p>Page 19 : For LED Panel C9/R10 always reserve</p> <p>Page 14/28 : Y1/Y6 shortage issue change from BG332768909 to BG332768224</p> <p>Page 3 : R81 stuff 10K for OD pin</p> <p>Page 31 : CN21 BOM error, change DFHD07MR000 to DFHD14MS011</p> <p>Page 17 : C540/C606/C289 CH6102ME904(EOL) change to CH6102M1909</p> <p>Page 22 : U34 G-sensor P/N change same as BU1 from AL021174C00 to AR0BU1R0000</p> <p>Page 21 : ESD1/ESD2/ESD3 always reserve for ESD solution. Change value to **</p> <p>Page 18 : CN31/R471/R459/C530/C531/C553/C552/C486/R453/R457/R452/R458 add EV@</p> <p>Page 27 : CN15(New card) change PCB Footprint to "ncard-13180151-u-26p-1"</p> <p>Page 27 : U17 Value change from NEW @ Q227C10LN-B1 to NEW @ Q227C10LN-C1. Let P/N and Value match.</p> <p>Page 21 : U11 P/N error, so change to "new part number" avoid before use error BOM. U11 reserve for sil1392.</p> <p>Page 21 : U12 Value add IHM@ to BOM clear. To avoid BOM build error.</p> <p>Page 21 : U9 Value must modify from "CEC@R5F211A4SP to CEC@R5F211A4SP. To clear BOM.</p> <p>Page 25 : CN27/CN34 MINI Card clock connect error. CN27 must connect to CLK_PCIE_MINI3/3#. CN34 must connect to CLK_PCIE_MINI2/2#.</p> <p>Page 24/25 : C261/C246 must stuff. Before NC for A-test layout issue only.</p> <p>Page 3 : RP45 Value add NEW @ for new card clock BOM clear and better EMI result.</p> <p>Page 2 : R226 Value add "CB@" for PCMCIA clock BOM clear and better EMI result.</p> <p>Page 31 : PL6 Change PCB Footprint to "CHOKA-PCMC0631-3R3MN-BD3A" for SMT issue.</p> <p>Page 19 : U1 add pin27 to GND to meet PCB Footprint.</p> <p>Page 20 : U25 Pin3/Pin5 SWAP for layout smooth</p> <p>Page 30 : Del FM interface. Move to LAN/B and Del C400.</p> <p>Page 26 : LAN/B CONN change to 30pin (BL121-30R-30P-L-TE1, DFFC30FR009), and add FM interface</p> <p>Page 22 : C31 change Footprint from 7343 to 3528 for placement no space for EC Xtal move.</p> <p>Page 26 : CN13 Change Footprint to 88060-12001-12P-L for ME assembly issue.</p> <p>Page 28 : U42(CIR) Change PCB Footprint for SMT suggestion, And change P/N from BEBK0076200 to BEBK0038200</p> <p>Page 29/30 : HP AMP NC. Reserve only.</p> <p>Page 26 : Del R103, TP(Mainstream/low cost control by TP/B)</p> <p>Page 15/27 : Add R592/R593 for USB port match OC port</p> <p>Page 21 : Add R103/R594/Q46/Q47/R600/R601 for CEC level shift (BOI mail). And adjust net name for ESD protect ESD1 close to connector.</p> <p>Page 29 : Reserve R595-R598 for Audio WHQL issue. (Can not multite stream when FM not support.</p> <p>Page 27 : LED1/LED2 change type for ME. And modify LED4 Wimax LED circuit</p> <p>Page 20 : HOLE 16 add GND for ESD</p> <p>Page 21 : Del D13/R115/R116/D14 same as BL55</p> <p>Page 28 : EC del MMB (10pin) LED0#1/#2# And move BT_EN/CRT_SENSE#</p> <p>Page 26 : CN2 modify Footprint to BL123-06R-6P-L-BL5, P/N to DFFC06FR336</p> <p>Page 26 : CN4 modify Footprint to BL123-04R-4P-L-BL5, P/N to DFFC04FR012. And SWAP pin list for different Footprint</p> <p>Page 26 : CN11/CN14 modify Footprint to BL121-06R-6P-L-BL5, P/N to DFFC06FR003.</p> <p>Page 25 : CN8 modify Footprint to BL123-14R-14P-L-TE1, P/N to DFFC14FR009.</p> <p>Page 22 : CN19 change HDD Footprint to SATA-070820-QU001-22P-R-TE1</p> <p>Page 2 : C231/C234 for Y3 TxC measurement suggestion change from 33p to 30p</p> <p>Page 24 : C580/C575 for Y3 TxC measurement suggestion change from 10p to 15p</p> <p>Page 20 : Del HOLE3 for ME request</p> <p>Page 26/28 : Add LOM_DISABLE# for LAN power consumption</p> <p>Page 2 : Change R214/R211 from 33ohm to 47ohm for EA fail.</p> <p>Page 29 : CN30 use same parts for BOI project. Change to SCY DFWF04MS002.</p> <p>Page 20 : HOLE14/HOLE18 modify footprint for new card move 2mm for BOI request.</p> <p>Page 27 : Kill switch (SW2) change part for ME request. P/N is DHLLSS12P07</p> <p>Page 14 : RTC Circuit R455/R456/R449/R450 follow standar circuit value (Eric Lee)</p> <p>Page 13 : CN24 Change Footprint from DDR-C-292564-200P to DDR-C-292564-200P-TE1 for connector fixed pad not meet Footprint.</p> <p>Page 15/25 : Not support TV. Del USB8 and add T71/T73/T74/T75</p> <p>Page 24 : C542 stuff 22p for EMI issue.</p> <p>Page 29 : Add R517/R518 0 ohm for EMI issue.</p> <p>Page 20 : +5V/VIN add 0.1u to shape for EMI issue</p> <p>Page 17 : SB CAP cost down C579/C267</p> <p>Page 8/9 : NB CAP cost down C119/C458/C68/C155/C403/C149/C443/C436</p> <p>Page 2 : CLK CAP cost down C541</p> <p>Page 24 : Card reader cost down, del 0 ohm</p> <p>Page 19 : C16 change BOM/Footprint from CH6101M9905 to CH61001ME96 for cost down</p> <p>Page 27 : C262/C266/C84 change BOM/Footprint from CH5472K9A02 to CH5471M9907 for cost down</p>	



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TE1	B2A		<p>Page2429 : C567/C338/C610/C605 change BOM from CH5102K9B06 to CH5101K9B01 for cost down</p> <p>Page?? : C566/C261/C607/C321/C482/C532/C201/C583/C582/C345/C626/C325/C623/C360/C24/C281 change BOM from CH6102K9A01 to CH61001ME96 for cost down</p> <p>Page4 : CPU CAP C35 BOM change for cost down from CH733LM8812 to CH733RM8858</p> <p>Page9/17 : C293/C254/C283/C102 cost down from CH5472M9901 to CH5471M9907</p> <p>Page19 : C27 change BOM/Footprint from CH61004M398 to CH61004M291 for cost down</p> <p>Page16 : Add FM_Detect pin to GPIO12</p> <p>Page3 : Del C50,Add R115/R116 for shut down circuit</p> <p>Page16 : Add FM_Detect pin to GPIO12</p> <p>Page20 : HOLE11/HOLE28 modify Footprint for ME issue</p> <p>Page29 : Del R528 for no space adjust modem trace</p> <p>Page32 : Del JP1/JP2</p> <p>Page19 : Reserve R473/R474 200K for LED drive IC</p> <p>Page33 : Add PR155 for VRON stable</p> <p>Page31 : MTEMP add PD13/PR156</p> <p>Page21 : CN23(HDMI) Connect chnge Footprint and library pin define for correct library from HDMI-C12815-119A5-L-19P-V to HDMI-C12815-119A5-L-19P-V-TE1</p> <p>Page26 : CNe apply pin 31 and pin32, modify new footprint : BL121-32P-L-TE1</p> <p>Page29 : Change C224, C226, C227 and C228 to 'ESD PROTECT'(ESD4, ESD5, ESD6 and ES07 : DIODE SMD V-PORT-0603-220K-V05)</p> <p>Page20 : C650 change to 1000P from EMi request</p> <p>Page28 : Apply isolate TP_LED_ON from EC to Mainstream TP</p> <p>Page20 : C641 - C649 apply to CC0402 = CH4104K9B03</p> <p>Page31-38 : Update power circuit to TE1, 965PM, B2A-1030-1030</p> <p>Page20 : L1-L3 change to CX9LL470000 from EMi suggestion</p> <p>Page20 : Modify Hole26, NC GND net for layout issue</p> <p>Page21 : *HM@1000p/16V_4 change to *HM@1000p/50V_4</p> <p>Page25 : C468 change Value from 0.01u/25V_4 to 0.01u/16V_4</p> <p>Page25 : CN27 change to DFHD52MS146</p> <p>Page19, 29 : INT_MIC change PN to DFHD02MR003</p> <p>Page29 : CN39 change to DFHD04MR012</p> <p>Page26 : CN13 change to DFFC12FR006</p> <p>Page14 : CN28 change to DFWF02MS000</p> <p>Page29 : R351, R354 change footprint to RC0603</p> <p>Page26 : modify Low cost MMB pin define, CN3 pin2 change to MX5</p> <p>Page28 : apply R486, R485 and R477 PU for Battery LED issue follow BL5</p> <p>Page15 : Del T73, T71 for layout isse (use via to measure)</p> <p>Page20 : del Hole10 and Hole 27 GND pin (layout issue)</p> <p>Page30 : Stuff R357 and R369, reserve C343 U24 R367 Q24 for VR smooth modify</p> <p>Page21 : R144 Value add /F</p>	
	B2B		<p>Page21 : Q7/Q8 Value add CEC@ for BOM option</p> <p>Page21 : F3 Value add IEHM@ for BOM option</p> <p>Page4 : C40/C41 stuff for power measurement issue</p> <p>Page28/31 : PR29 KC / R54 stuff 100K/F for S.Y request</p> <p>Page30 : R516/R543 stuff 1K / R354/R351 stuff 10u/10V_6</p> <p>Page30 : VR1 change P/N from CK0000RZ004 to CK0000RZ005</p> <p>Page15 : R569 Value add EV@ for BOM option</p> <p>Page14 : R300/R330/R561/R562 Value add *HM for BOM option</p> <p>Page19 : C13 change to 33n / R14 change to 499/F, and reserve R473 and R474</p> <p>Page : C289, C540, C606, R351, R354 change to CH6101M9905 for Buyer issue</p> <p>Page16 : Stuff R248 and change 0.4, and Stuff C242 change to 10p_4 for CLKUSB_48 EA tail issue</p> <p>Page30 : CN20 change PN to DFHS12F5000 with SUY forbidden issue</p> <p>Page28 : Add R385 and NC R56 for Boardcom BT issue</p>	
	C2A		<p>Page04 : C40 change Value to PC146, C41 change to PC147</p> <p>Page30 : R354 change Value to C651, R351 change to C652</p> <p>Page31 : Mirror CN21 Pin define</p> <p>Page25 : CN35 change footprint:MIPCI-88958-5204M-52P-H</p> <p>Page28 : C379 and C401 change PN to CH6102K9A19 with BOI issue</p> <p>Page25 : CN35 change to DIP type (footprint:MIPCI-88958-5204M-52P-V), Part Number (DFHS52FR013)</p> <p>Page24 : CN37 change footprint to (4IN1-CM4R-116-43P-L-V), Part Number (DFHD42MS005)</p>	



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TE1	D3A		<p>Page19 : modify MR seneor with BLON circuit to solve flashing issue when system shut-down</p> <p>Page30 : Change C24 to U43 to solve VR not smooth</p> <p>Page31,32 : Change Charger circuit to use ACOK to inform EC</p> <p>Page29 : NC D44 to solve switch mute to un-mute, sound will delay about 2seconds</p> <p>Page24 : Apply R351, R354, R367, R487 and R488 for EMI request</p> <p>Page20 : EMI suggest used LL680 + 4.7 pf x6 cap to avoid CRT issue</p> <p>Page19 : Apply U44 circuit for LED panel black light issue</p> <p>Page27 : Change LED1 and LED2 to new part</p> <p>Page3.5 : Apply L54 near CPU side and C666 near NB side for ESD issue</p> <p>Page36 : Reserve SUSON PD resistor</p> <p>Page28 : Apply R489 reserve for TP_LED_ON enable(Low Cost ID)</p> <p>Page03 : NC C71 for Fansing speed issue follow BL55</p> <p>Page-- : Logo LED, function board conn and Board ID Value apply function option</p> <p>Page21 : HDMI conn change footprint to HDMI-C12815-119A5-L-19P-V-BU2</p> <p>Page25 : Led board conn change PN and Footprint : DFFC12FR285</p> <p>Page25 : Function board conn (mainstream and lowcost) change PN</p> <p>Page20 : Hole26 change footprint to h-te327x313cc295d962-7</p> <p>Page22 : SATA conn change Footprint to SATA-070620-QU001-22P-R-TE1</p> <p>Page-- : DDR socket CN24 change PN to DGMK0000040</p> <p>WLAN minicard conn change PN to DFHS52FR016</p> <p>Battery conn change PN to DFHD14MS014</p> <p>ODD conn change PN to DFHS50FR034</p> <p>1394 conn change PN to DFHS04FR109</p> <p>Kill switch change PN to DHLLS512P02</p> <p>FP board conn change PN to DFHD04MRA75</p> <p>BT conn change PN to DFHD10MR008</p> <p>CN3 change PN and Footprint is BL136-10R-10P-L</p> <p>CN2 change PN and Footprint is BL136-06R-6P-R</p> <p>Page-- : R275, C307, C308, R326, R293, R248 change Footprint to -C (circle pad)</p> <p>Page30 : Reserve R490 near VR for ESD protect</p> <p>Page28 : Reserve C33 near CIR for ESD protect</p> <p>Page30 : Reserve C656, C657 for audio noise debug</p> <p>Page21 : NC R136 and C131 to solve HDMI I-diagram fail</p> <p>Page30 : Stuff AMP1412 circuit for audio noise test</p> <p>Page30 : Change L52, L47 to BK1608LL121 and C578 and C601 to 0.1uF to test 3G/GPRS ExpressCard noise in HP</p> <p>Page29-30 : C599, C598, C569, C568 apply to CH41002KB93, And L45, L46 change to CX8LL121002 for INT MIC recording noise.</p> <p>Page30 : NC R516 and R543 to meet HP Jack signal measure and HP plug- unplug haven't happen bobo-sound too.</p> <p>Page30 : Change C578 and C691 for 0.1u to 0.22u to enhance avoid 3G noise and meet HP Jack signal measure</p> <p>Page25 : Mini card MB11, MB8-MB11</p>	

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TE1	D3A		<p>Inner Document</p> <p>Change C221 to CH01506JBD9, and NC R248, C242 for CLKUSB48 measure pass</p> <p>Add R353 to CS00002JB38 for ESD request</p> <p>Change CN4 PN to DFFC04FR213</p> <p>Add R459 and R471 to CS00002JB38 for EV request</p> <p>Remove Felica function at EV sku</p> <p>Remove MAIN@ parts at Low Cost ID Q26,Q27,R374 and R375</p> <p>Add R542 and R490 for ESD request</p> <p>Change R516, R543, C578 and C601 to CH41002KB93</p>	
	E3A	20080116	<p>Page21 : Change HDMI connector footprint to B test (HDMI-C12815-119A5-L-19P-V-TE1)</p> <p>Page26 : Change CN6 to BL134-32RL-YA1G-32P-L</p> <p>Page20 : Hole26 apply AGND pin for ESD</p> <p>Page30 : HP jack pin9,10 apply GND for ESD</p> <p>Page19,31 : Power modify for LED panel</p> <p>Page26 : Apply CN40 for TP connector 2nd source(ACS)</p> <p>Page21 : Change U9 PN to ARBL5MV0000</p> <p>Page24 : PD XD_WPO#_C with R491(reserve) for XD measure</p> <p>Page26 : Change the footprint of DFFC34FR003 from 88171-3400L-34P-L to 91504-340N-34P-L</p> <p>Page20 : Change L1, L2 and L3 to CX8LL470000, Change C1, C2, C4, C5, C6 and C8 to CH-686T0B07 for EA CRT measure pass</p> <p>Page16 : Change R345 Value to WOHM@10K_4 and Change R548 to WOGS@10K_4</p> <p>Page26 : Apply FA@ at Felica function Parts Value</p> <p>Page27 : Apply MAIN@ at Q26,Q27,R374 and R375</p> <p>Page30 : R516 change to C659, R543 change to C658</p> <p>Page31 : Apply varistor PD11 and PD12 to BCD4204U209 for ESD request</p> <p>Page30 : Apply ESD8, ESD9(BC03220KZ19) and C660 in HP_JP for ESD solution.</p> <p>Page27 : Change R374 and R375 from 390ohm to 150ohm base on ME request for LED light not enough</p> <p>Page27 : Modify New card footprint to NCARD-13180151-U-26P-L-TE1</p> <p>Page26 : NC CN13 pin3 to follow LED board</p> <p>Page31 : PL6 change PN to CDRH104R-TE1</p> <p>Page19 : Apply PN in R10 to CS33742FB17</p> <p>Page14 : Modify RTC circuit to follow BL5S</p> <p>Page30 : Remove 1412 Amp circuit</p> <p>Page29 : Modify speaker gain to 9.7dB, R334 and R348 change to CS31053F909, R572 and R576 change to CS31603F916</p> <p>Page27 : Change new card power switch to T1 (AL002231000)</p> <p>Page24 : NC C542 for customer request. Q2 spec can't oevr 10p</p>	
	E3A-01	20080125	<p>BOM release</p> <p>E3A-01</p> <p>Page30 : Change C651 and C652 to 0_6</p> <p>Page24 : Change R488 to 33_4</p> <p>Page32 : Change PR76 to 10K/F and stuff PR77 to 64.9K/F</p> <p>Page24 : Change VR1 PN to CK0000RZ006</p> <p>E3B</p> <p>Page14 : remove T50</p> <p>Page19 : apply R14 Value to LED@</p> <p>Page25 : remove R312, R301 and R327</p> <p>Page21 : CN23 apply IEHM@ in Value</p> <p>Page31 : PC25 change to CY060320901 for ESD</p> <p>Page27 : NC C264 and R253 from CS32872FB11 change to CS000002JB38</p> <p>F3A</p> <p>Page7 : EC Pin 27 connect to DISPON</p> <p>Page22 : Q38 pin2 change to +3V_S5</p> <p>Page19 : Change CN4 to DFFC04FR012</p>	