

Boston

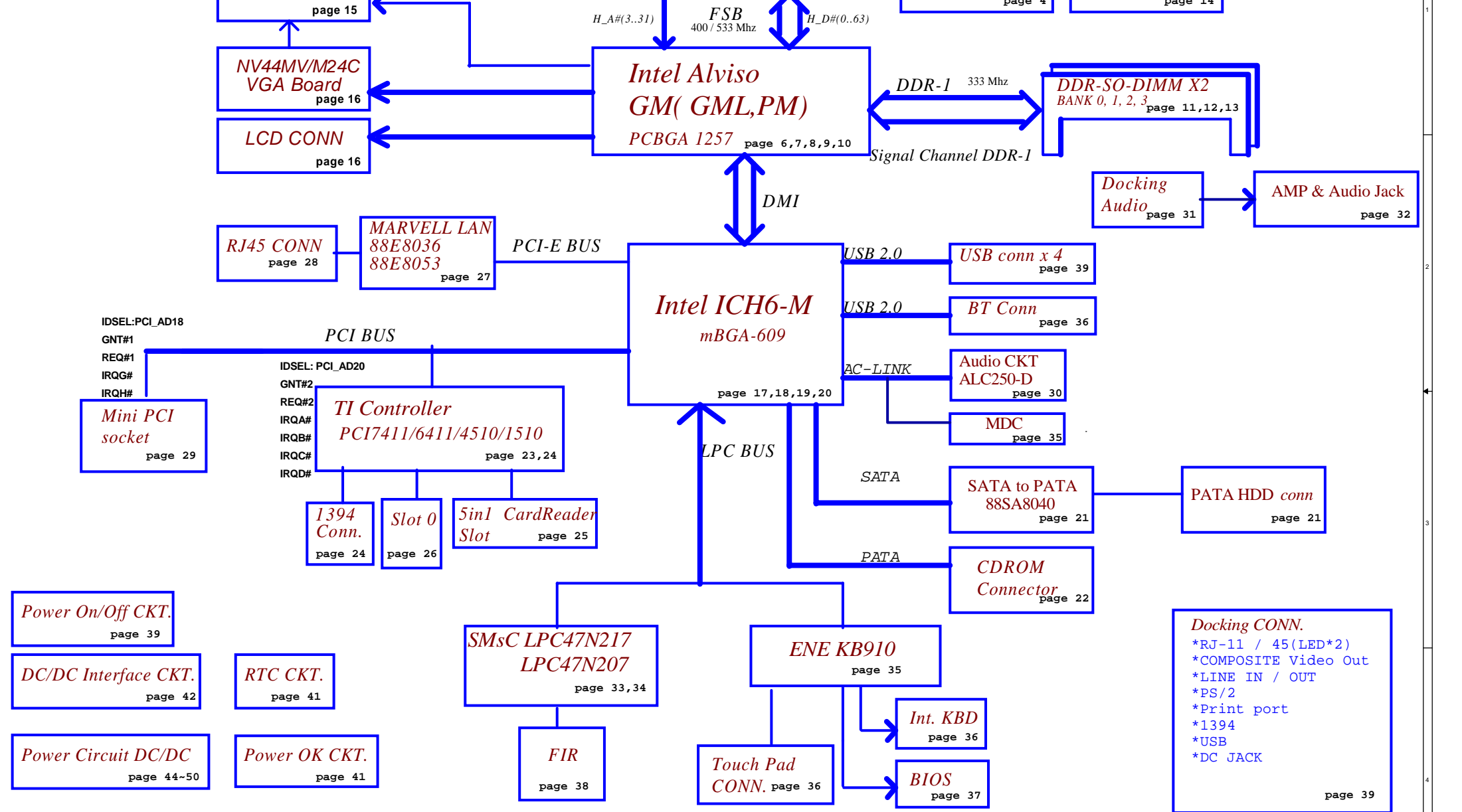
LA-2721 Schematics Document

Intel Dothan / Alviso GM(PM) / DDR-1 / ICH6-M

(nVIDIA NV44MV / ATi M24C)

Rev:1.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+DDRVTT	1.25V switched power rail for DDR terminator	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+DDRVCC	2.5V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5VCD	5V switched power rail for CDROM	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+5VAMP	5V switched power rail for amplifier	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB/PIRQC/PIRQD
1394	AD20	2	PIRQA/PIRQB/PIRQC/PIRQD
Card reader	AD20	2	PIRQA/PIRQB/PIRQC/PIRQD
Mini-PCI	AD18	1	PIRQG/PIRQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b	2nd Battery	1001 011X b
(24C04)	1011 000Xb	Docking	1010 000X b

ICH6M SM Bus address

Device	Address
Clock Generator (ICS 952623)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM1	1001 001Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 1%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0.100 V
1	8.2K +/- 1%	0.216 V	0.250 V	0.289 V
2	18K +/- 1%	0.436 V	0.503 V	0.538 V
3	33K +/- 1%	0.712 V	0.819 V	0.875 V
4	56K +/- 1%	1.036 V	1.185 V	1.264 V
5	100K +/- 1%	1.453 V	1.650 V	1.759 V
6	200K +/- 1%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

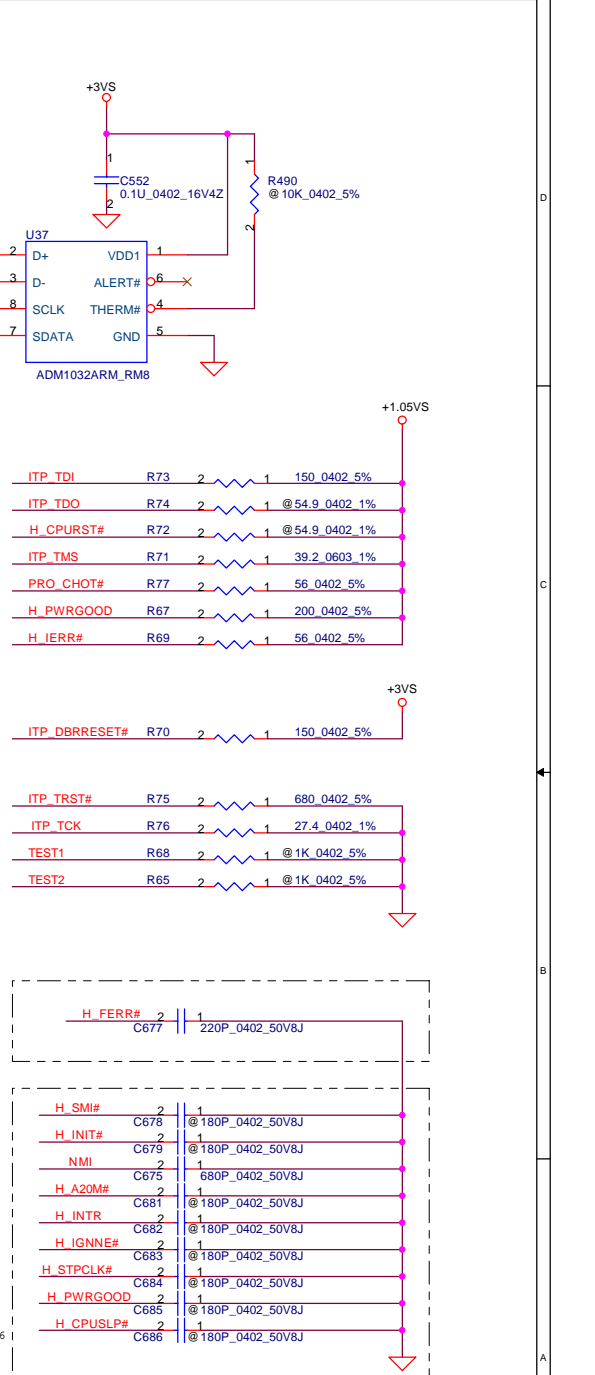
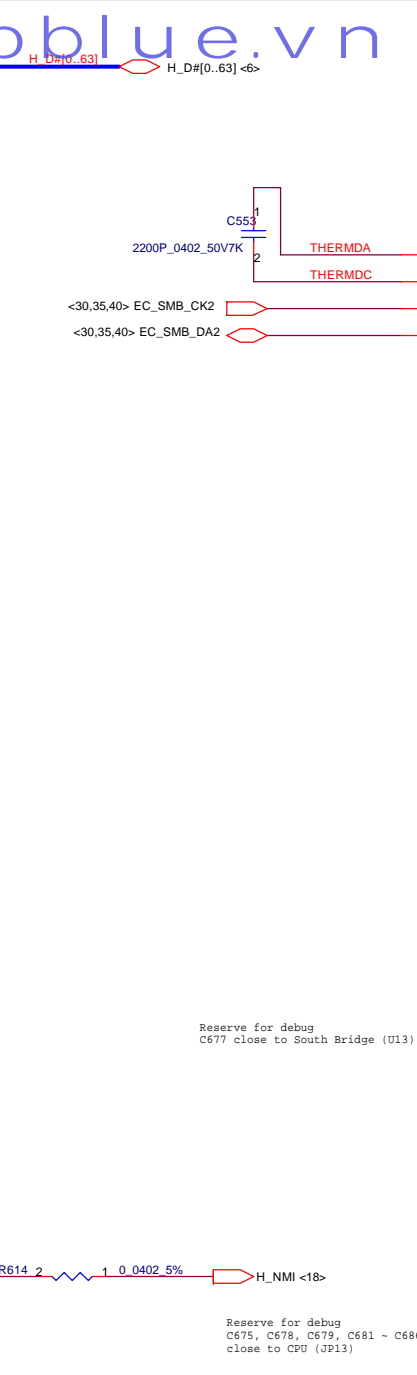
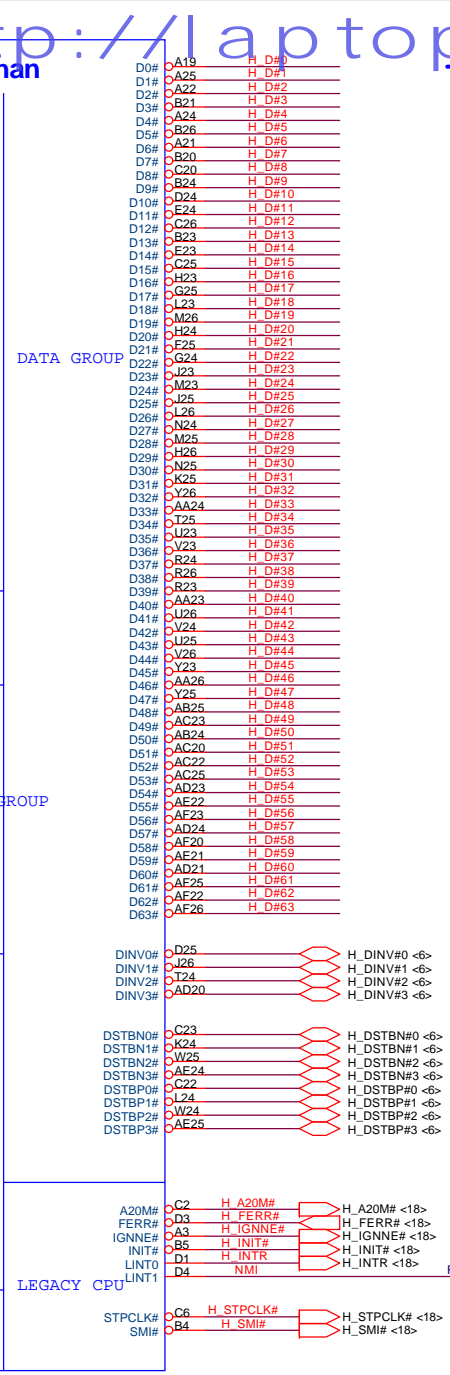
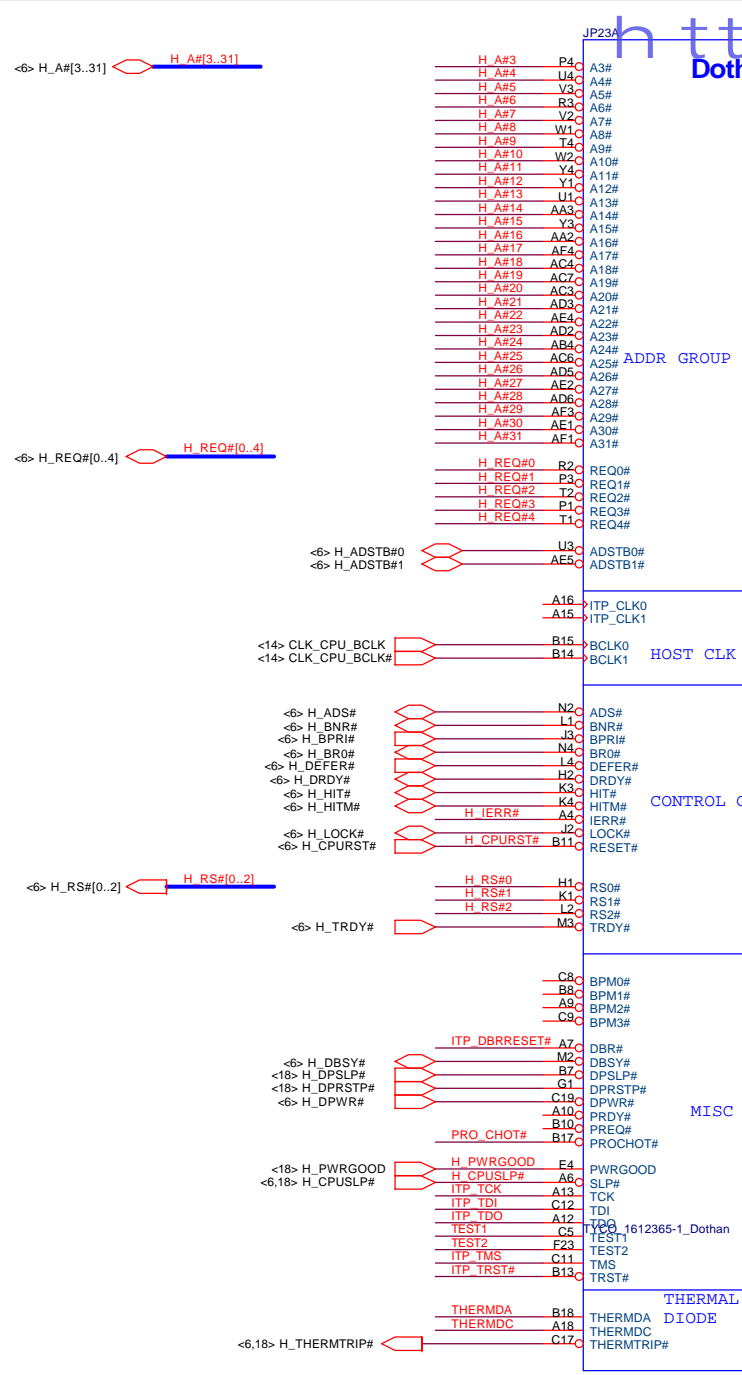
BOARD ID Table

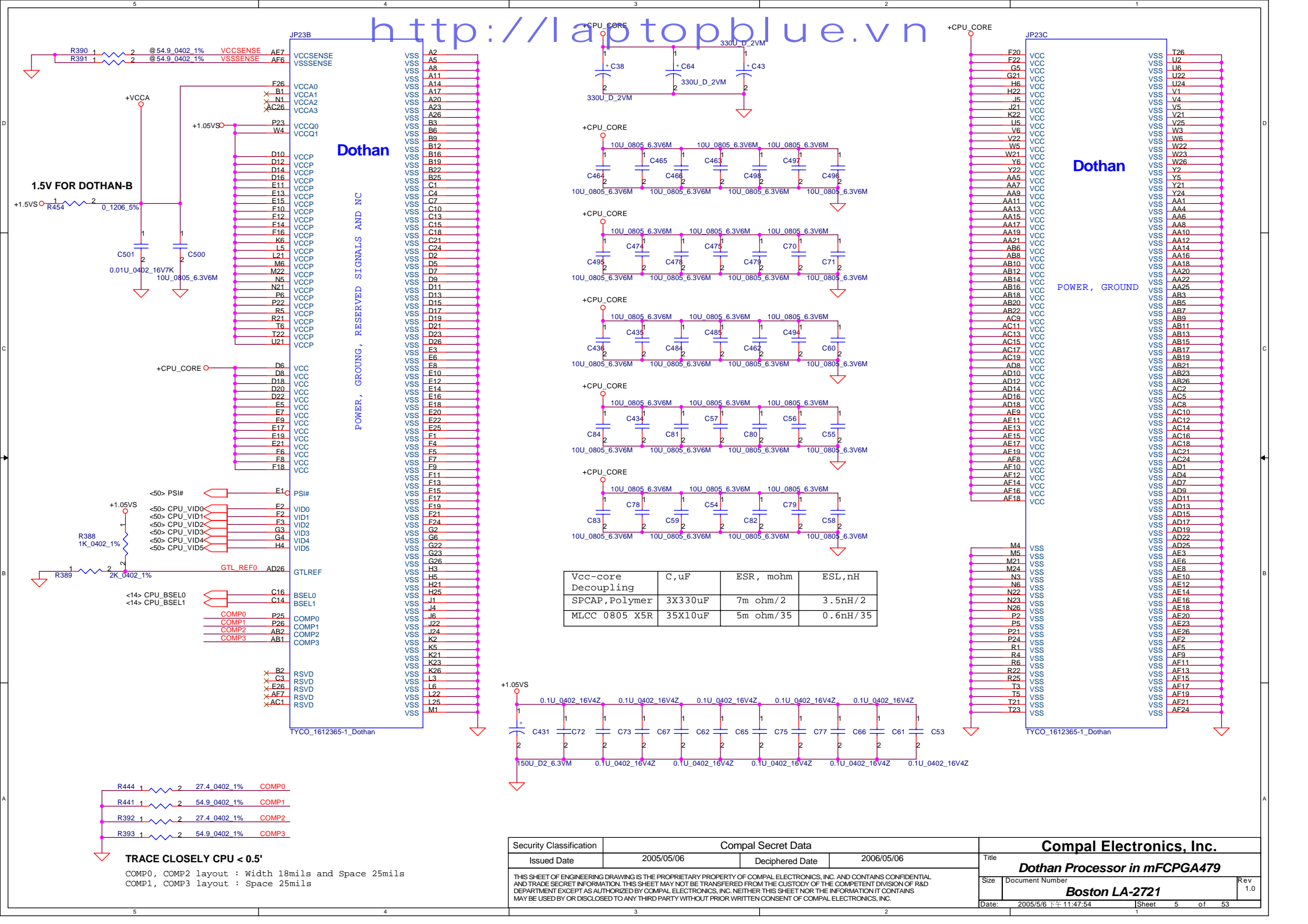
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

SKU ID Table

SKU_ID1	1 Button	3 Button	7 Button	5	6
SKU_ID	0	2	4		
0	10	8	0		
1	10C	C	2		
2	10G	9	4		
3	10GC	D	6		
4					
5					
6					
7					

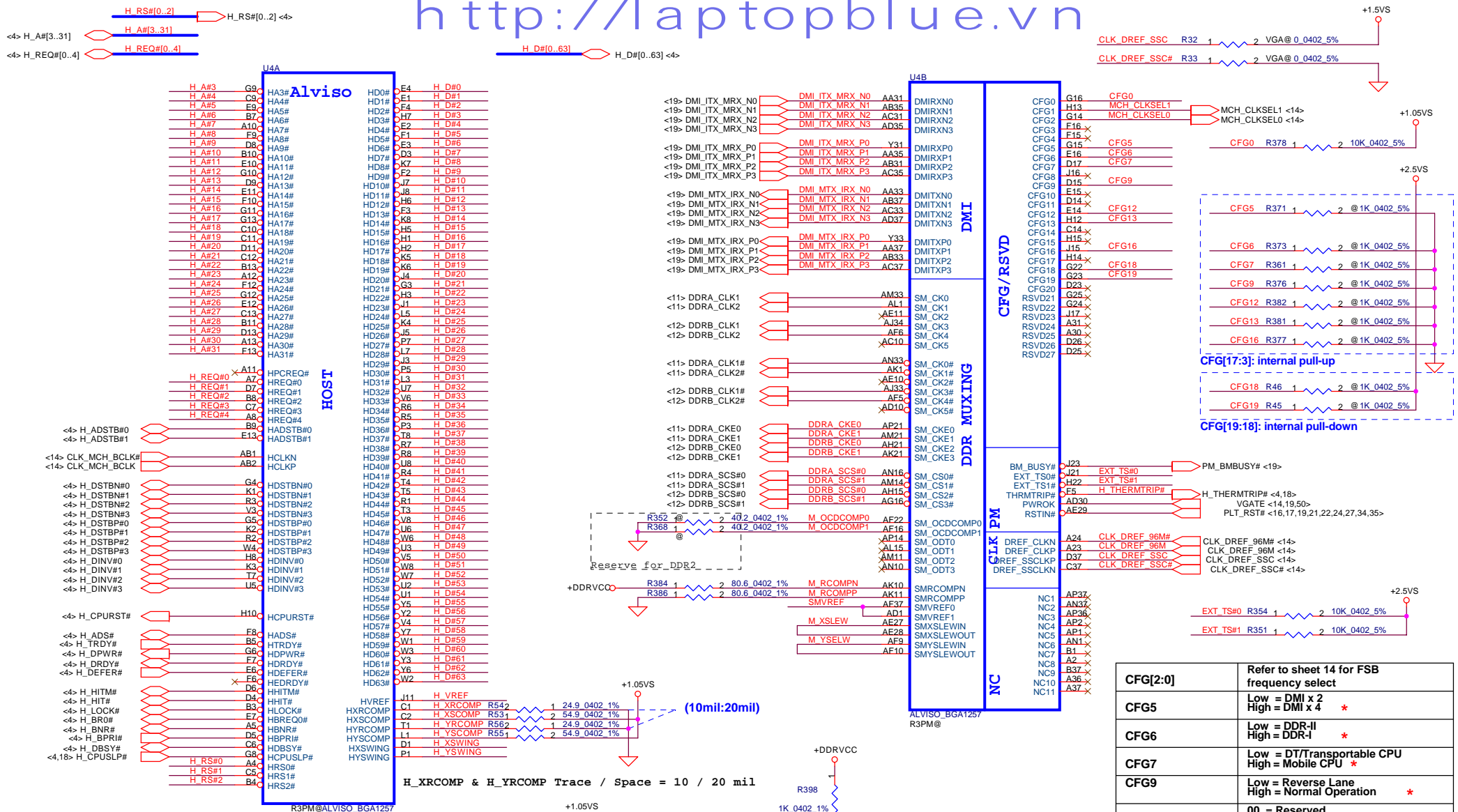
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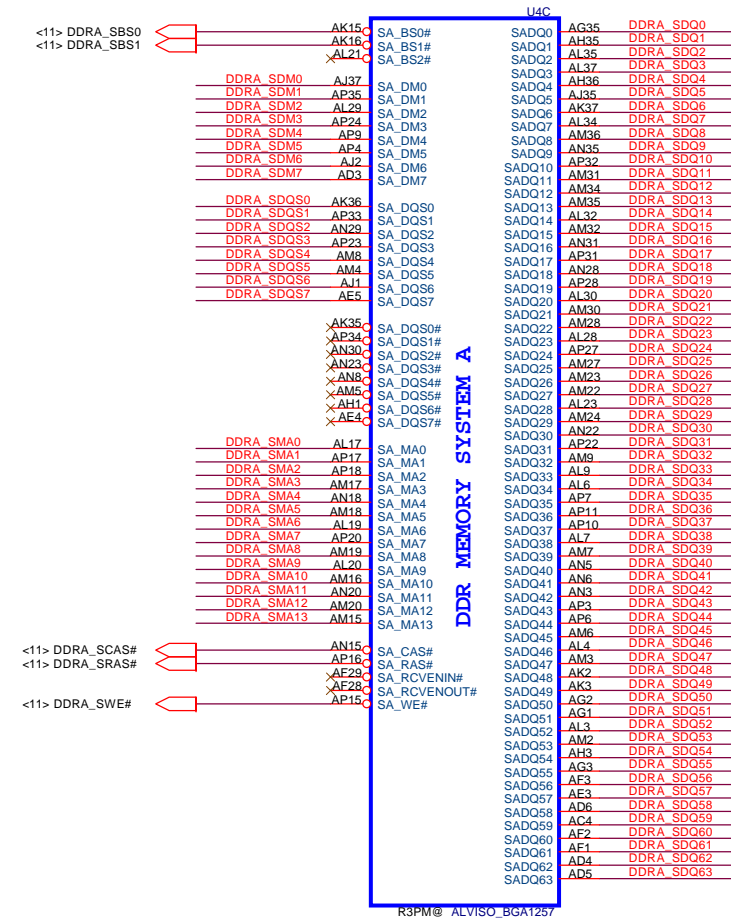


CFG[2:0]	Refer to sheet 14 for FSB frequency select
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II High = DDR-I *
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V

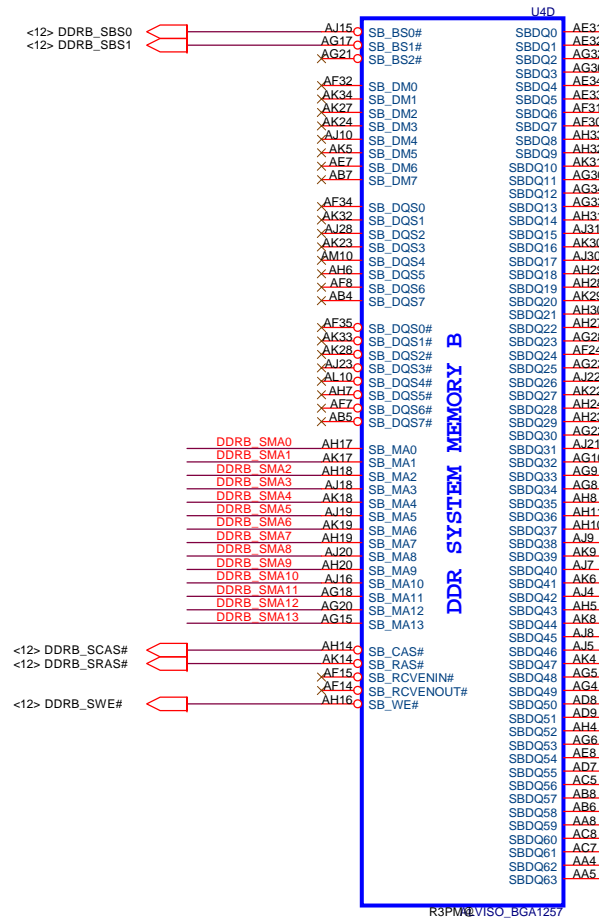
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<11> DDRA_SDQ[0..63]  DDRA_SDQ[0..63]
<11> DDRA_SDM[0..7]  DDRA_SDM[0..7]
<11> DDRA_SDQS[0..7]  DDRA_SDQS[0..7]
<11> DDRA_SMA[0..13]  DDRA_SMA[0..13]

<12> DDRB_SMA[0..13]  DDRB_SMA[0..13]

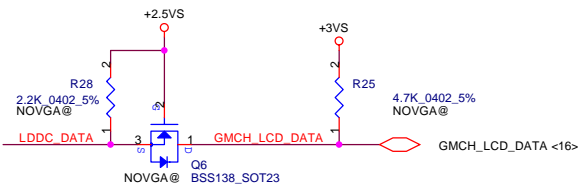
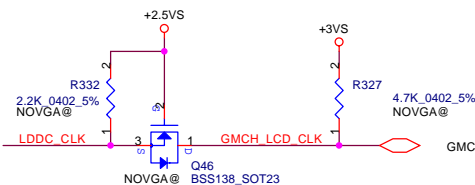
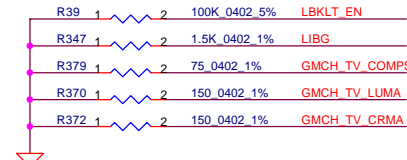
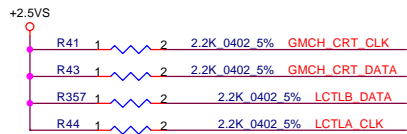
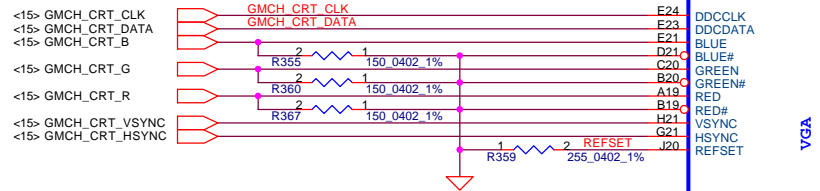
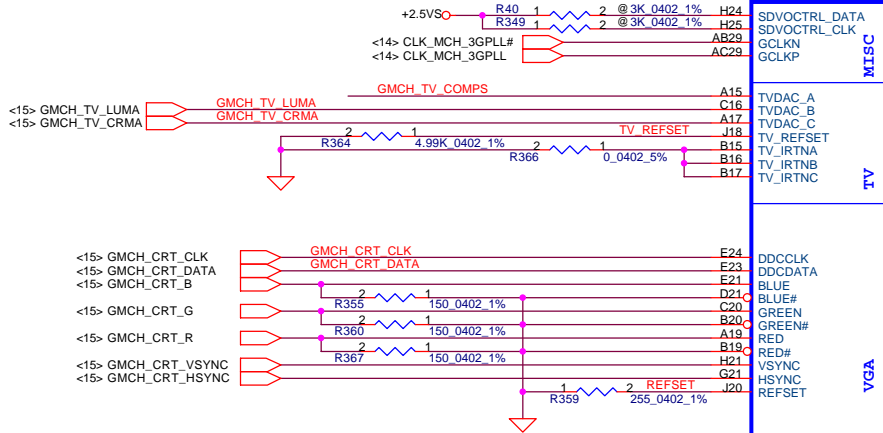
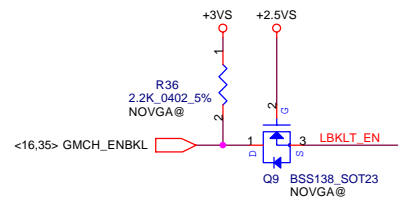


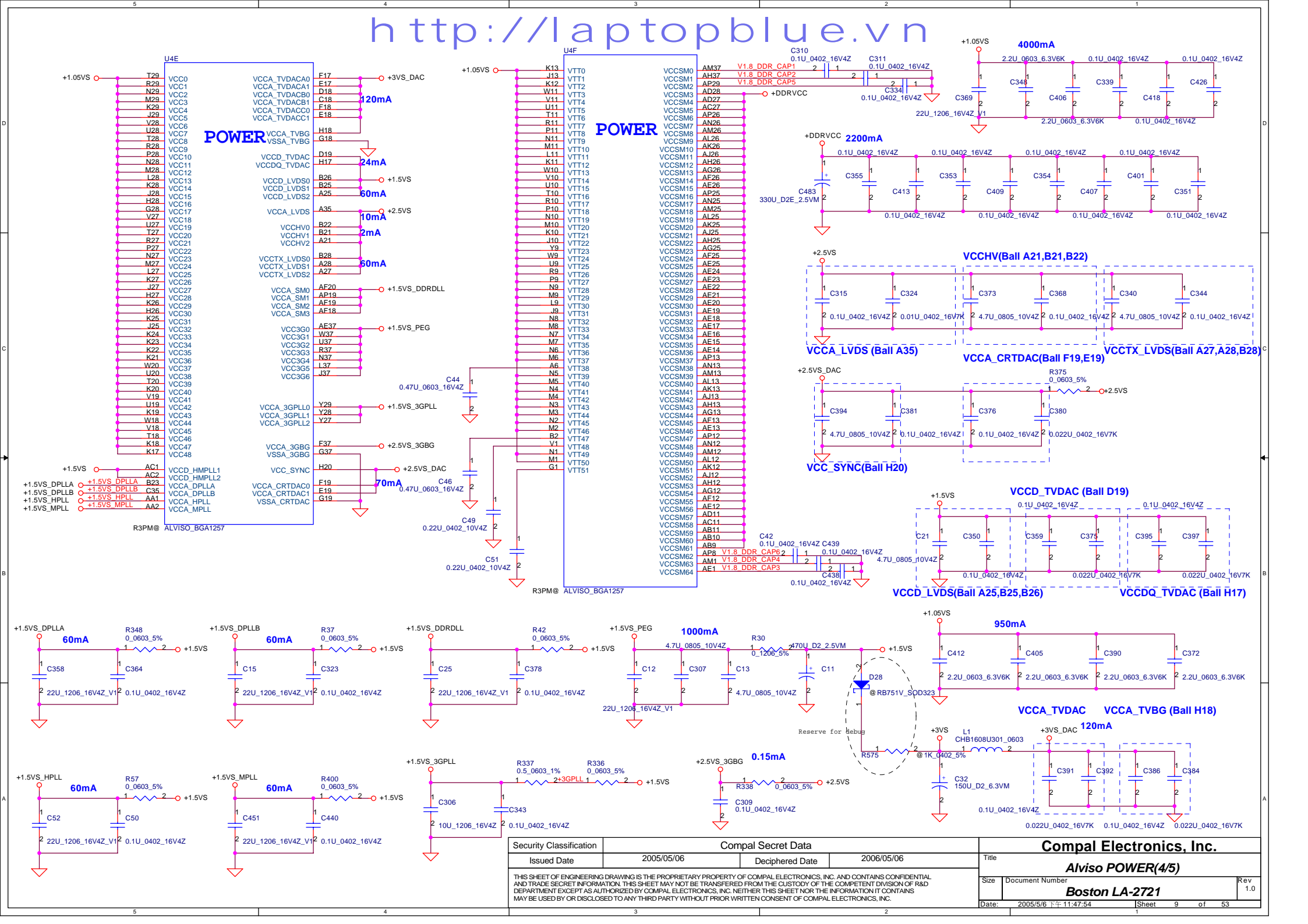
DDR MEMORY SYSTEM A

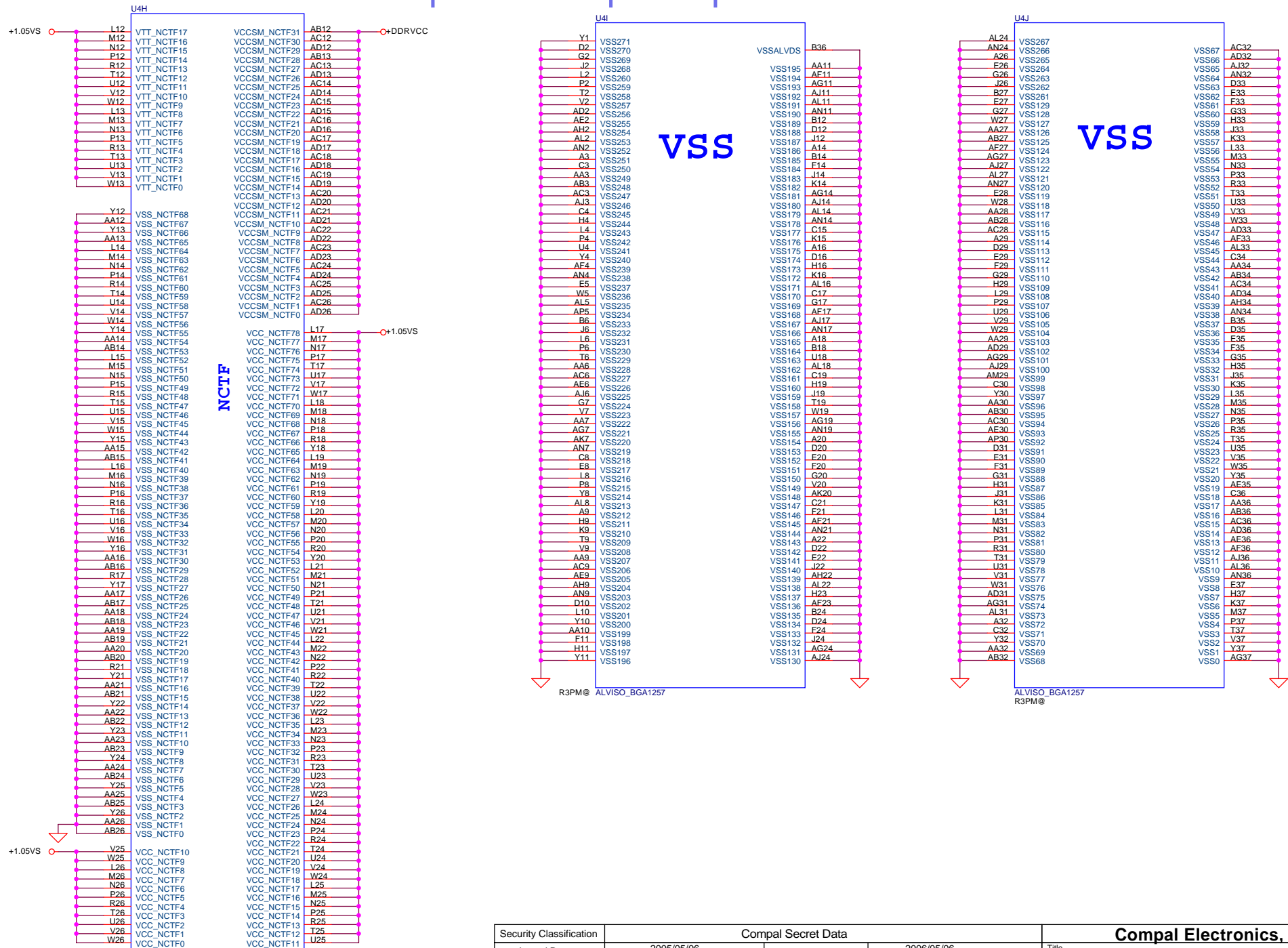


DDR SYSTEM MEMORY B

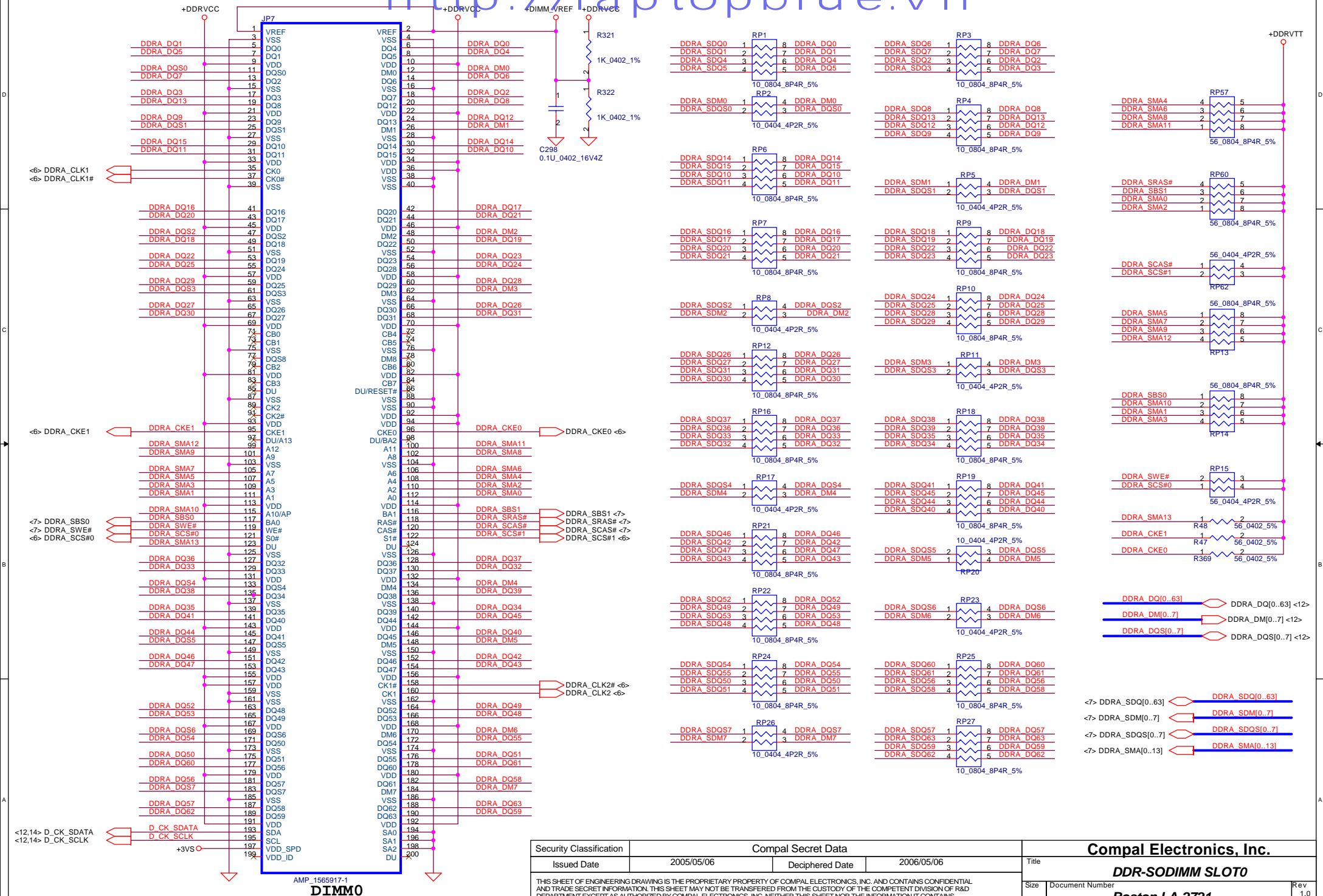
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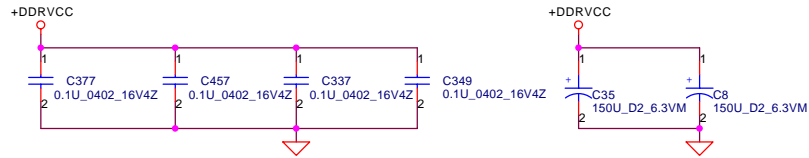
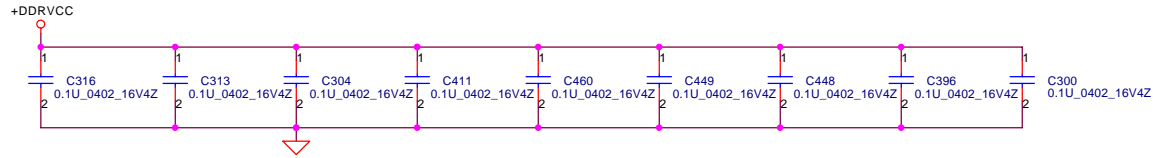
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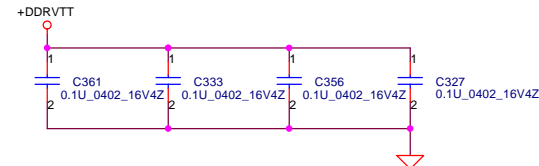
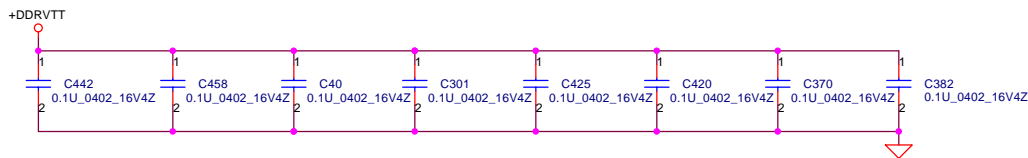
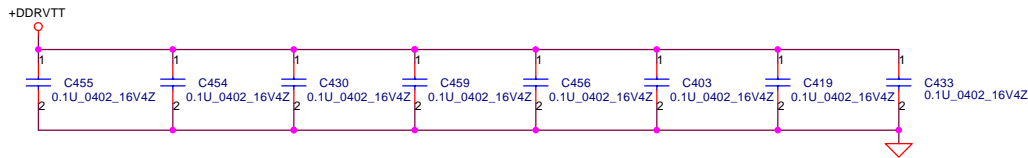
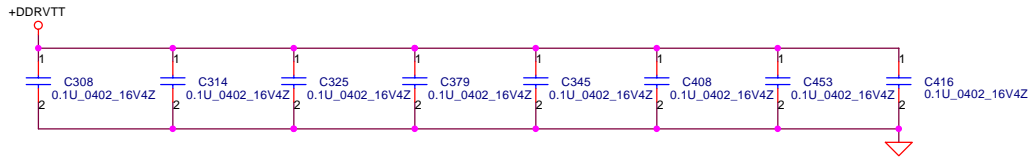
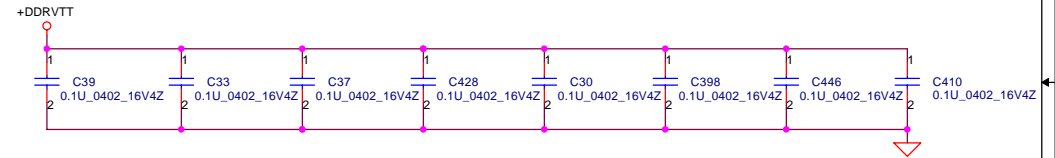
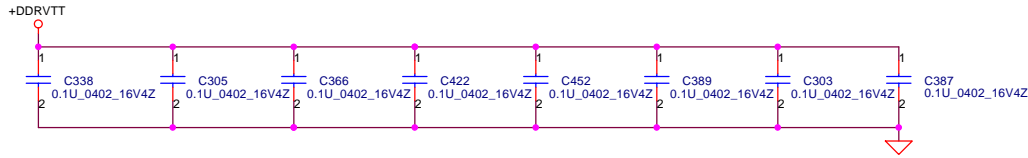
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Layout note :
Distribute as close as possible
to DDR-SODIMM.



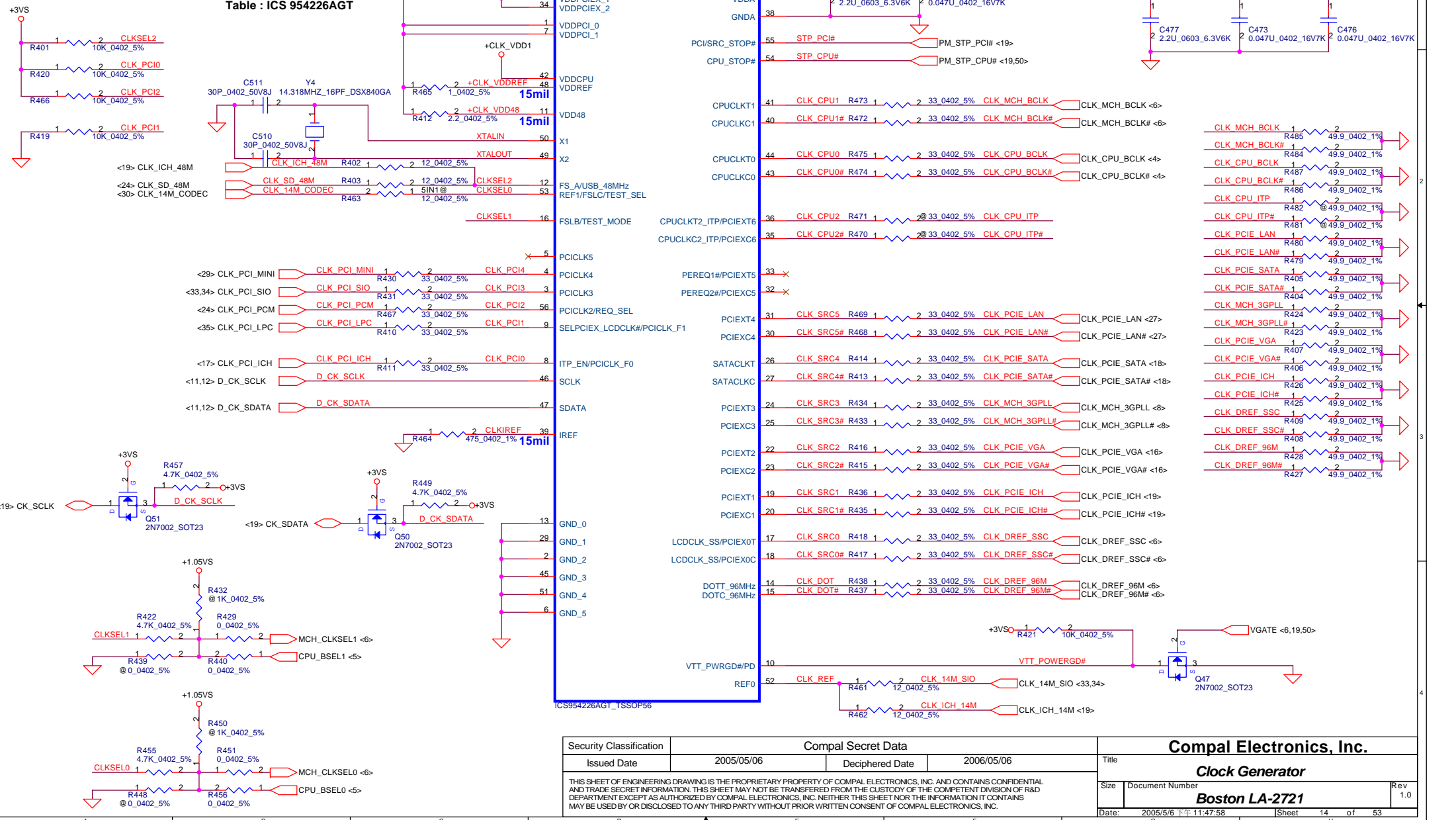
Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V



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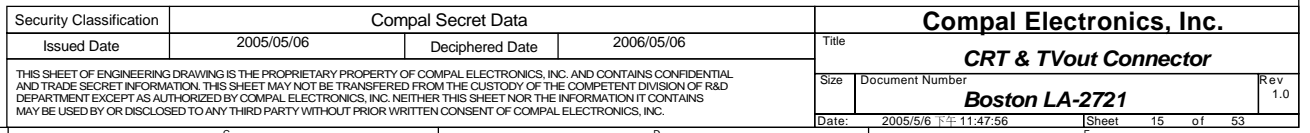
FSC	FSB	FSA	CPU	SRC	PCI
CLKSEL0	CLKSEL1	CLKSEL2	MHz	MHz	MHz
1	0	1	100	100	33.3
0	0	1	133	100	33.3
0	1	1	166	100	33.3
0	1	0	200	100	33.3

Table : ICS 954226AGT



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The diagram illustrates the pin connections for the J19 connector on the ACES 88081-1600 board. The connector is a 160-pin header, with pins numbered 1 through 160. The connections are organized into two main columns, with the left column representing pins 1-59 and the right column representing pins 60-160. The components connected to these pins include various DACs, VGA CRTs, DVI TXC+, DVI TXD0+, DVI TXD1+, DVI TXD2+, and various GTX and MTX components. The diagram also shows power connections for +3VALW, +2.5VS, +1.5VS, +5VS, and +5VALW. The bottom of the diagram shows the connection to the ACES 88081-1600 board.

Pin	Signal	Component
1	B+	
2		
3		
4		
5		
6		
7	DAC_BRIG	
8	DISPOFF#	
9	INVT_PWM	
10	VGA_DDC_CLK	VGA_DDC_CLK <15>
11		VGA_DDC_DATA <15>
12		
13		
14		
15	VGA_TV_LUMA	VGA_TV_LUMA <15>
16		
17	VGA_TV_CRMA	VGA_TV_CRMA <15>
18		
19		
20	VGA_CRT_VSYNC	VGA_CRT_VSYNC <15>
21	VGA_CRT_HSYNC	VGA_CRT_HSYNC <15>
22		
23	SUSP#	SUSP# <26,30,32,35,37,38,42,49>
24		
25	GMCH_ENBKLL	GMCH_ENBKLL <8,35>
26		
27		
28		
29	+3VALW	
30		
31		
32		
33	+2.5VS	
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VGA@ ACES_88081-1600

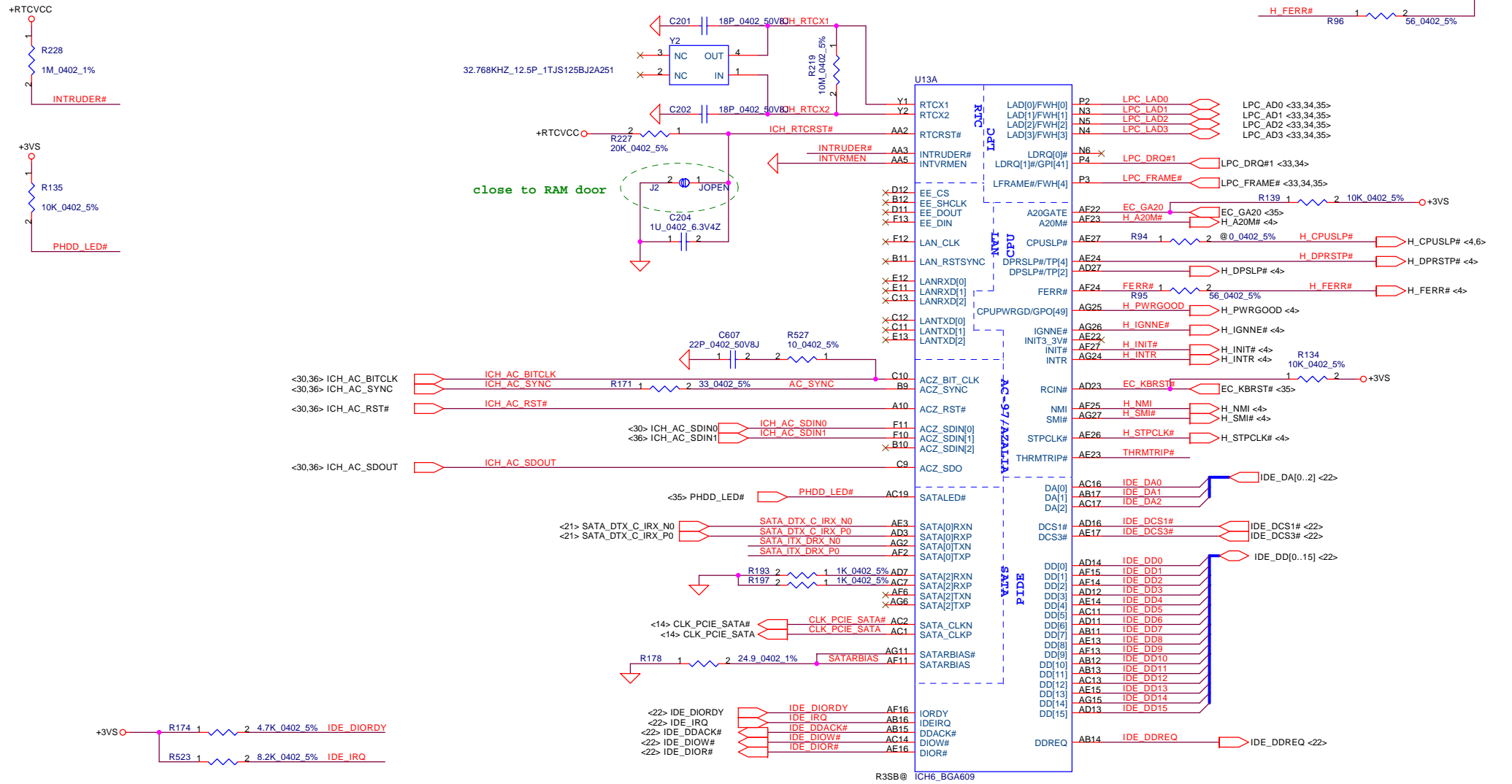
Diagram illustrating the connection of the GMCH module to the ACES_88242-3000 NOVGA module.

The GMCH module is connected to the NOVGA module via the following signals:

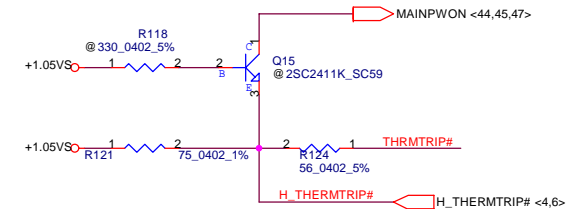
- Power:**
 - +3VS:** Connected to pin 1 of the GMCH module through capacitor C4 (0.1uF, 0402, 16V4Z).
 - +LCDVDD:** Connected to pin 2 of the GMCH module.
- Control and Data:**
 - GMCH_LCD_CLK:** Connected to pin 13 of the GMCH module.
 - GMCH_LCD_DATA:** Connected to pin 14 of the GMCH module.
 - DAC_BRIG:** Connected to pin 15 of the GMCH module.
 - INVT_PWM:** Connected to pin 16 of the GMCH module.
 - DISPOFF#:** Connected to pin 17 of the GMCH module.
- Outputs:**
 - GMCH_TXOUT0- <8>:** Connected to pin 18 of the GMCH module.
 - GMCH_TXOUT1- <8>:** Connected to pin 19 of the GMCH module.
 - GMCH_TXOUT2- <8>:** Connected to pin 20 of the GMCH module.
 - GMCH_TXCLK- <8>:** Connected to pin 21 of the GMCH module.
 - GMCH_TXCLK+ <8>:** Connected to pin 22 of the GMCH module.

The NOVGA module is labeled ACES_88242-3000 NOVGA@.

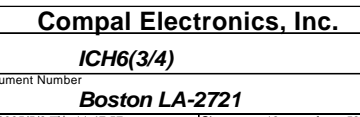
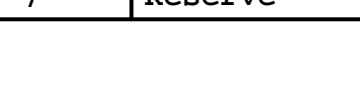
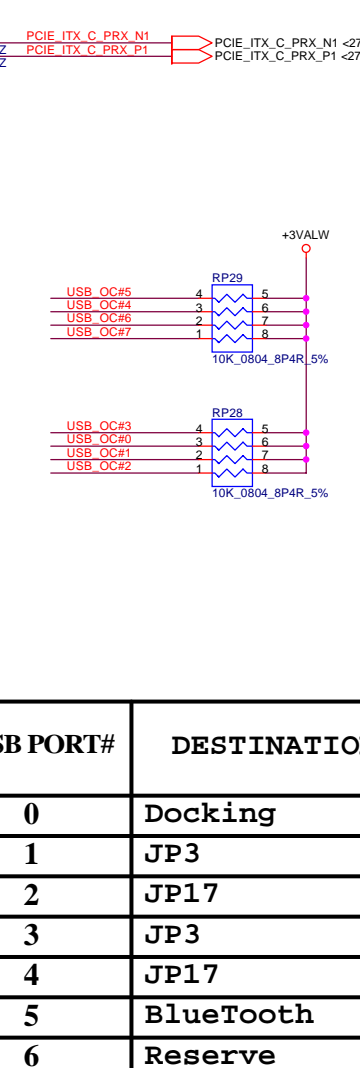
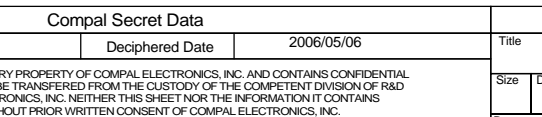
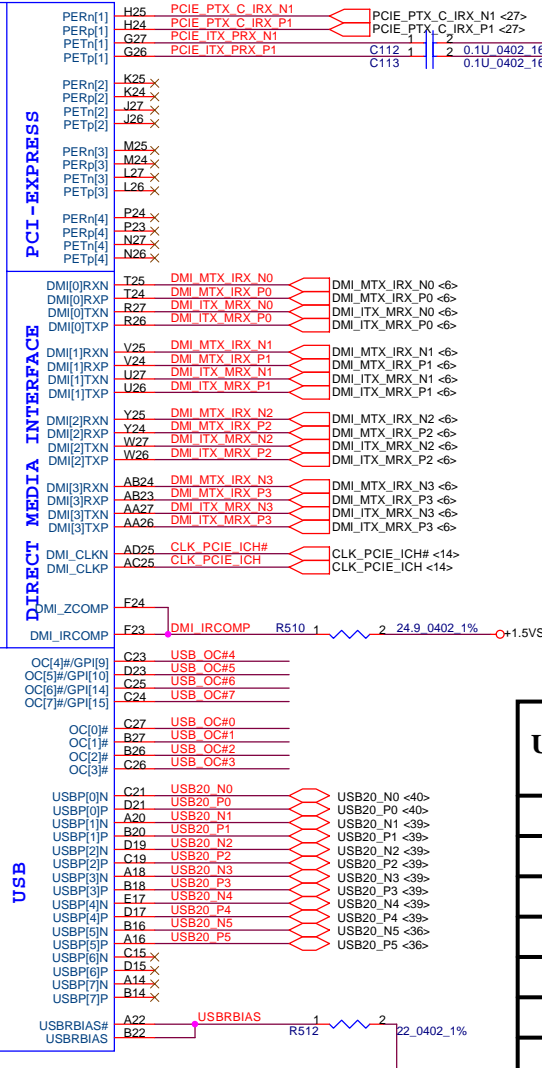
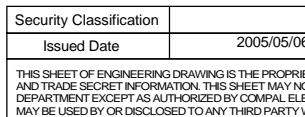
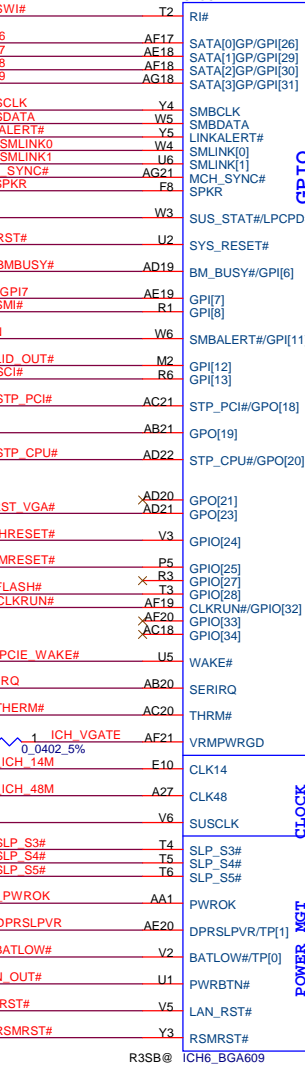
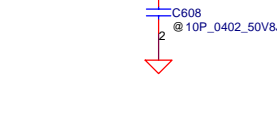
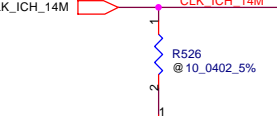
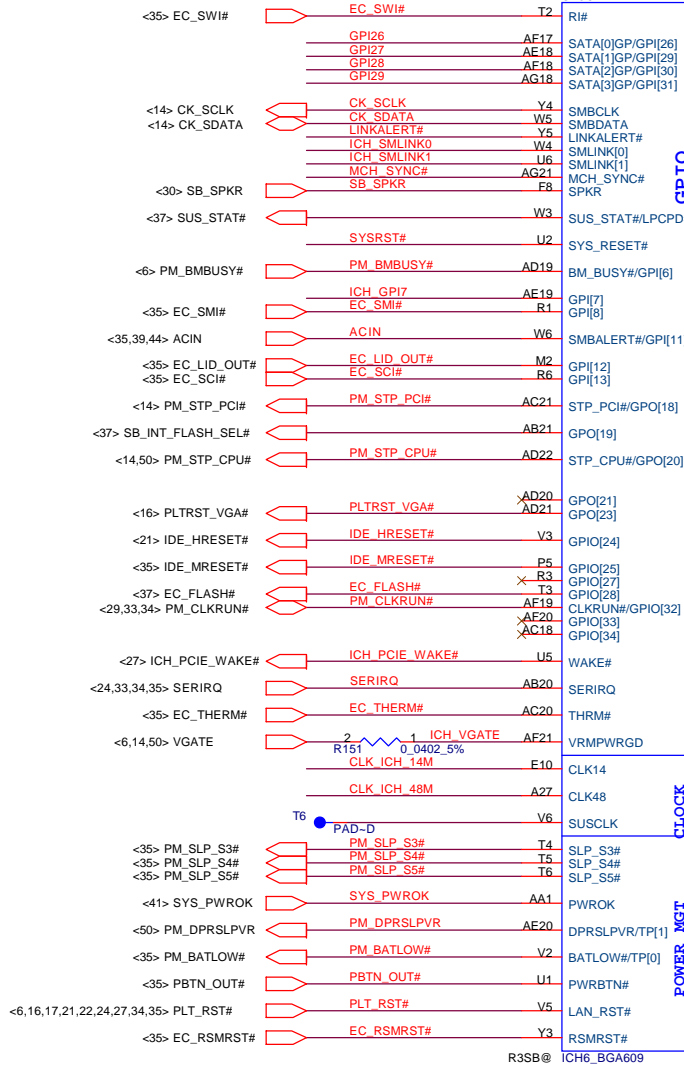
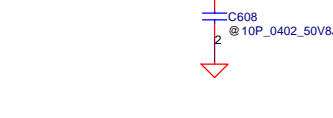
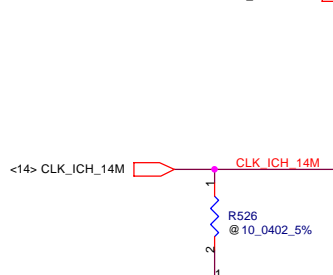
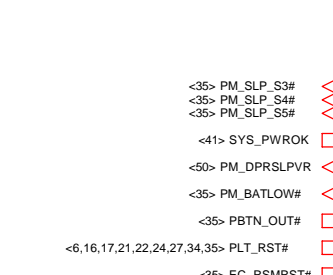
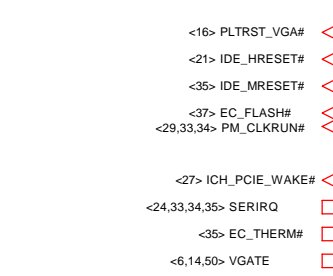
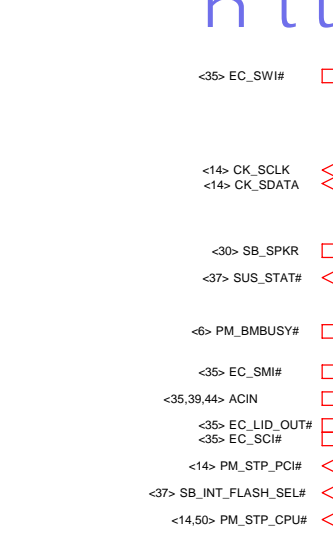
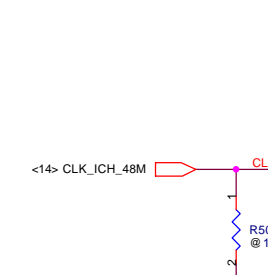
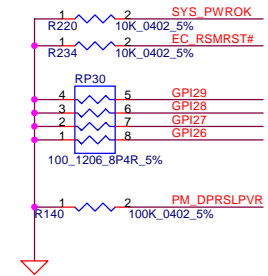
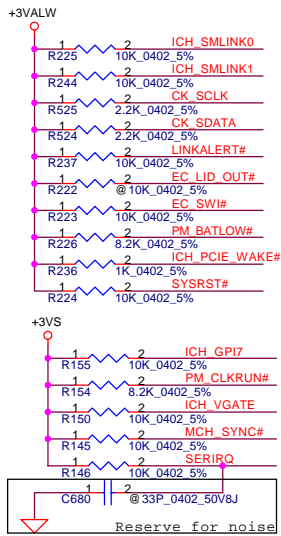
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SATA_ITX_DRX_N0
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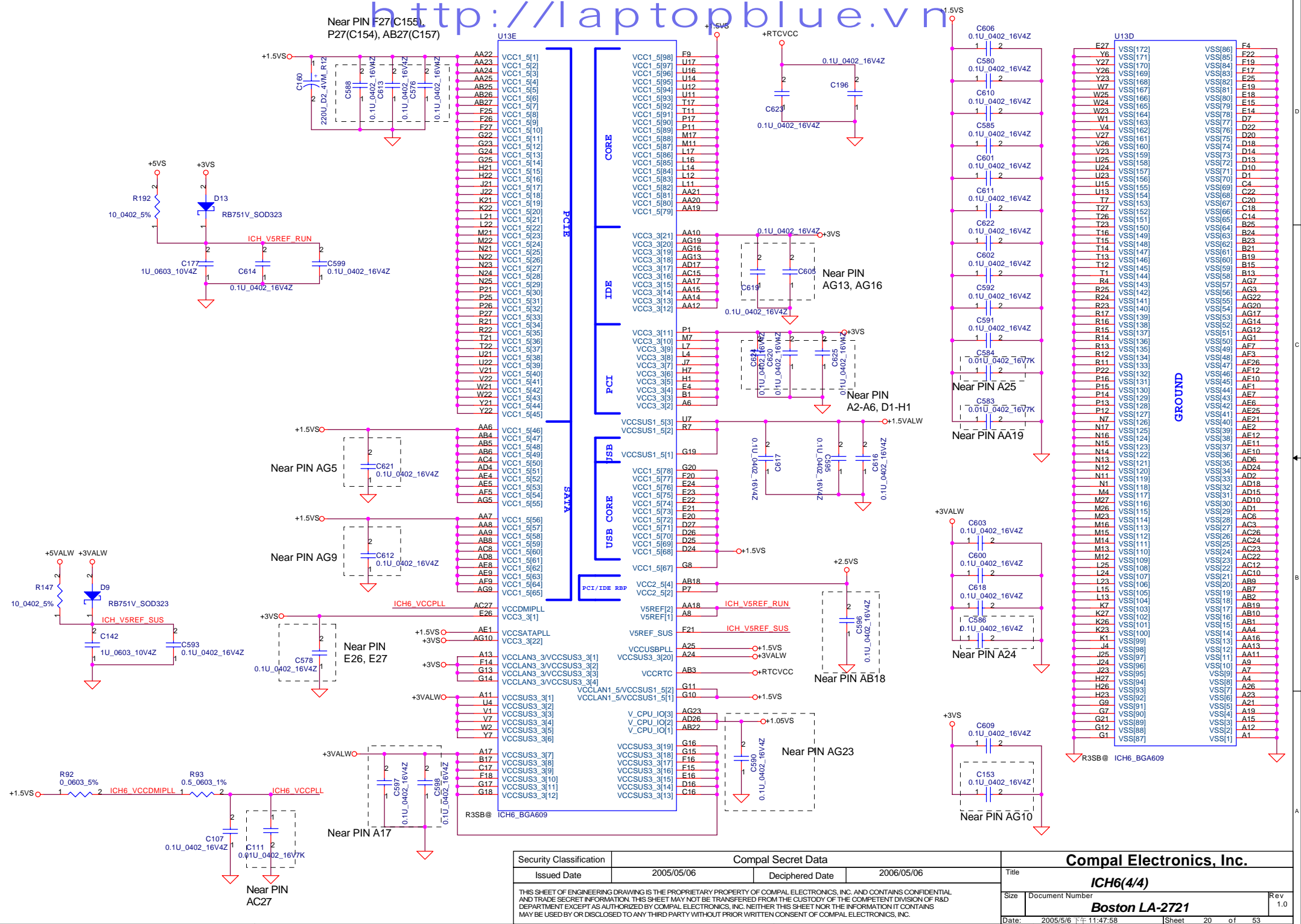
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				1.0	
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USB PORT#	DESTINATION
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2	JP17
3	JP3
4	JP17
5	BlueTooth
6	Reserve
7	Reserve

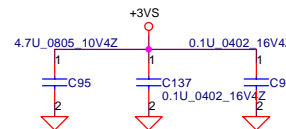
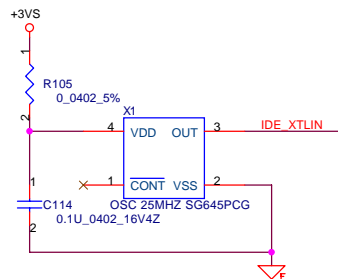
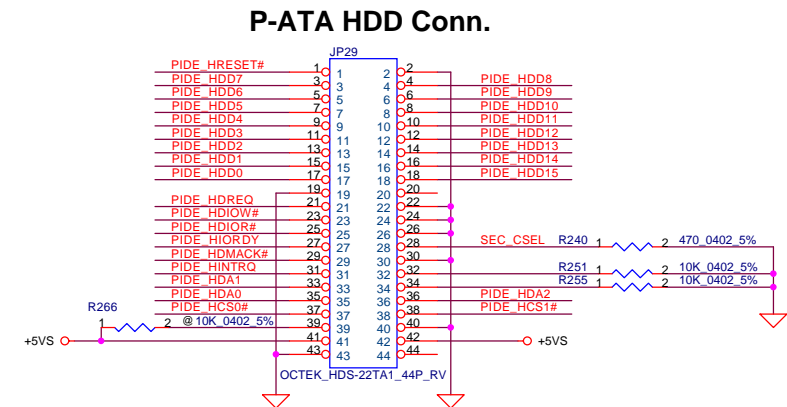
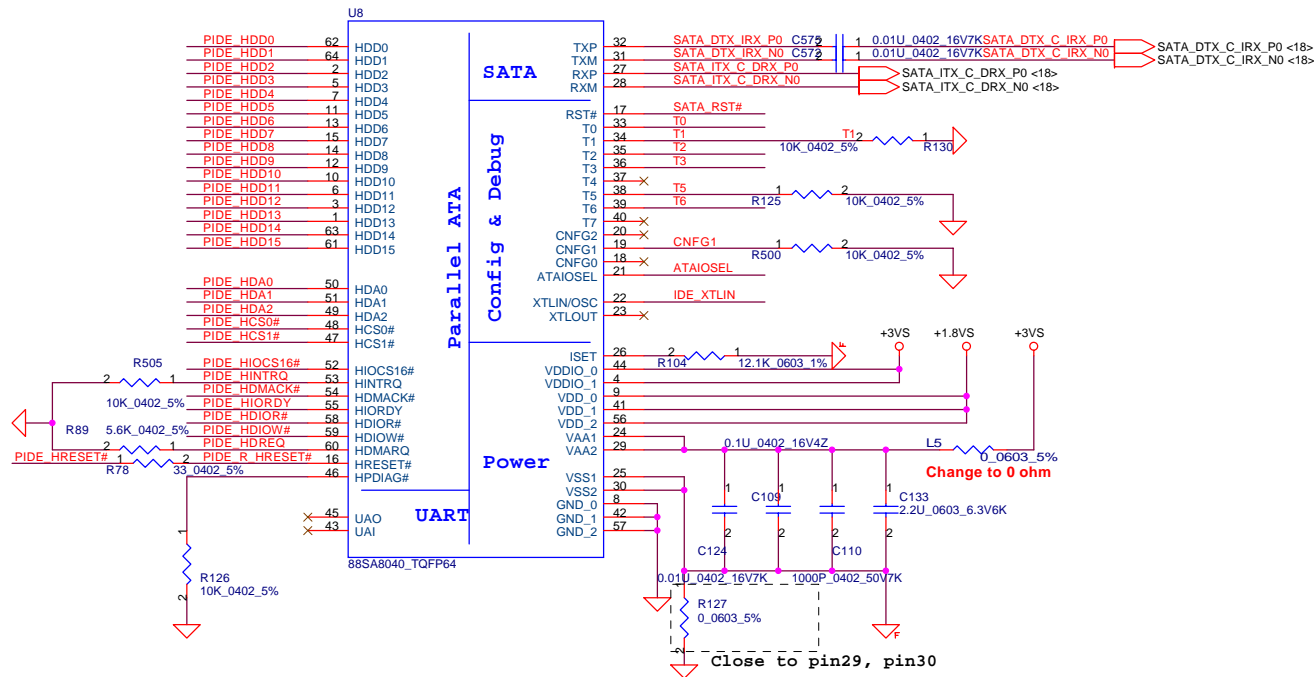
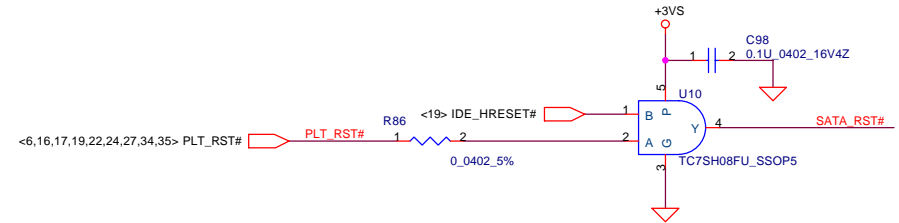
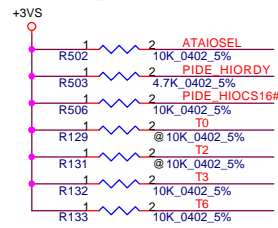
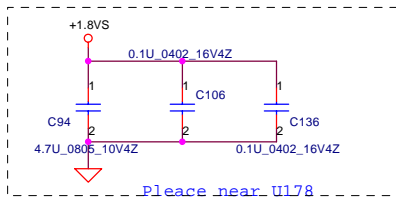
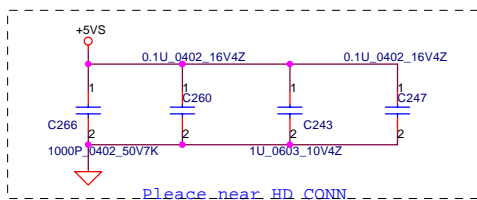
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P27(C154), AB27(C157)

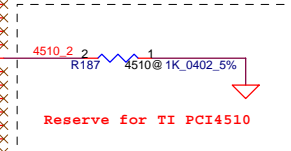
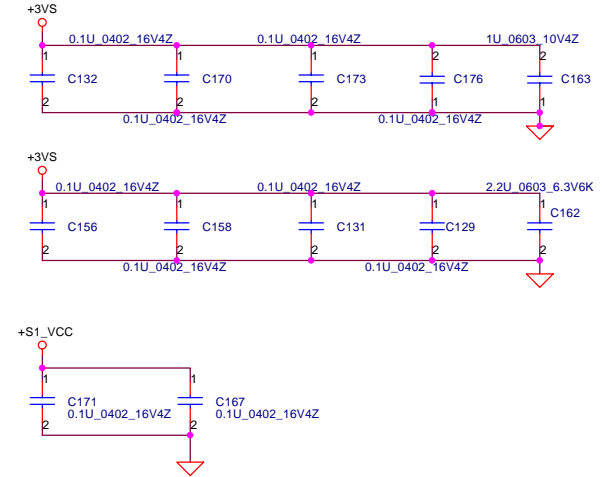
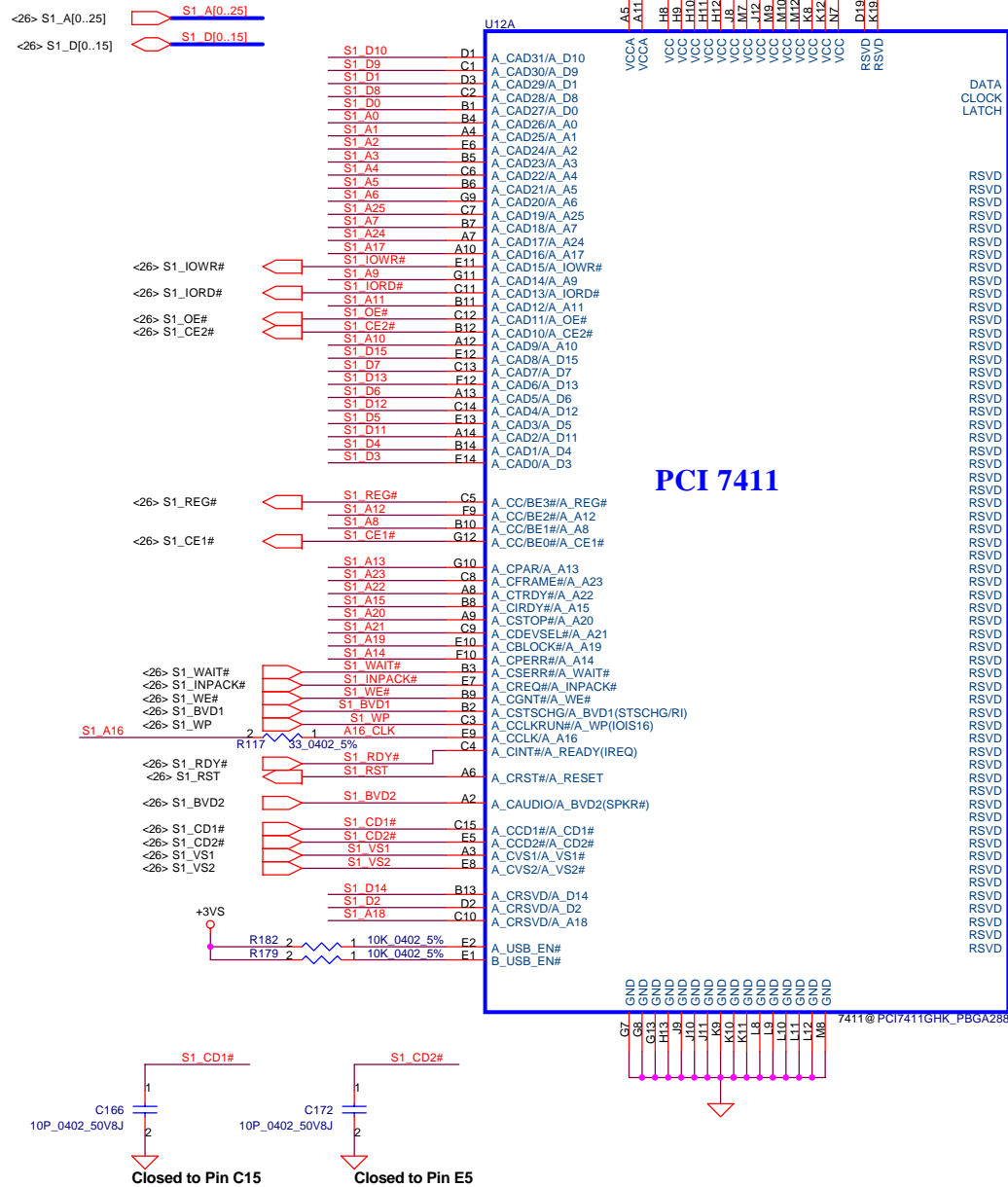


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Date:		2005/5/6 下午 11:47:58		Sheet 20 of 53	

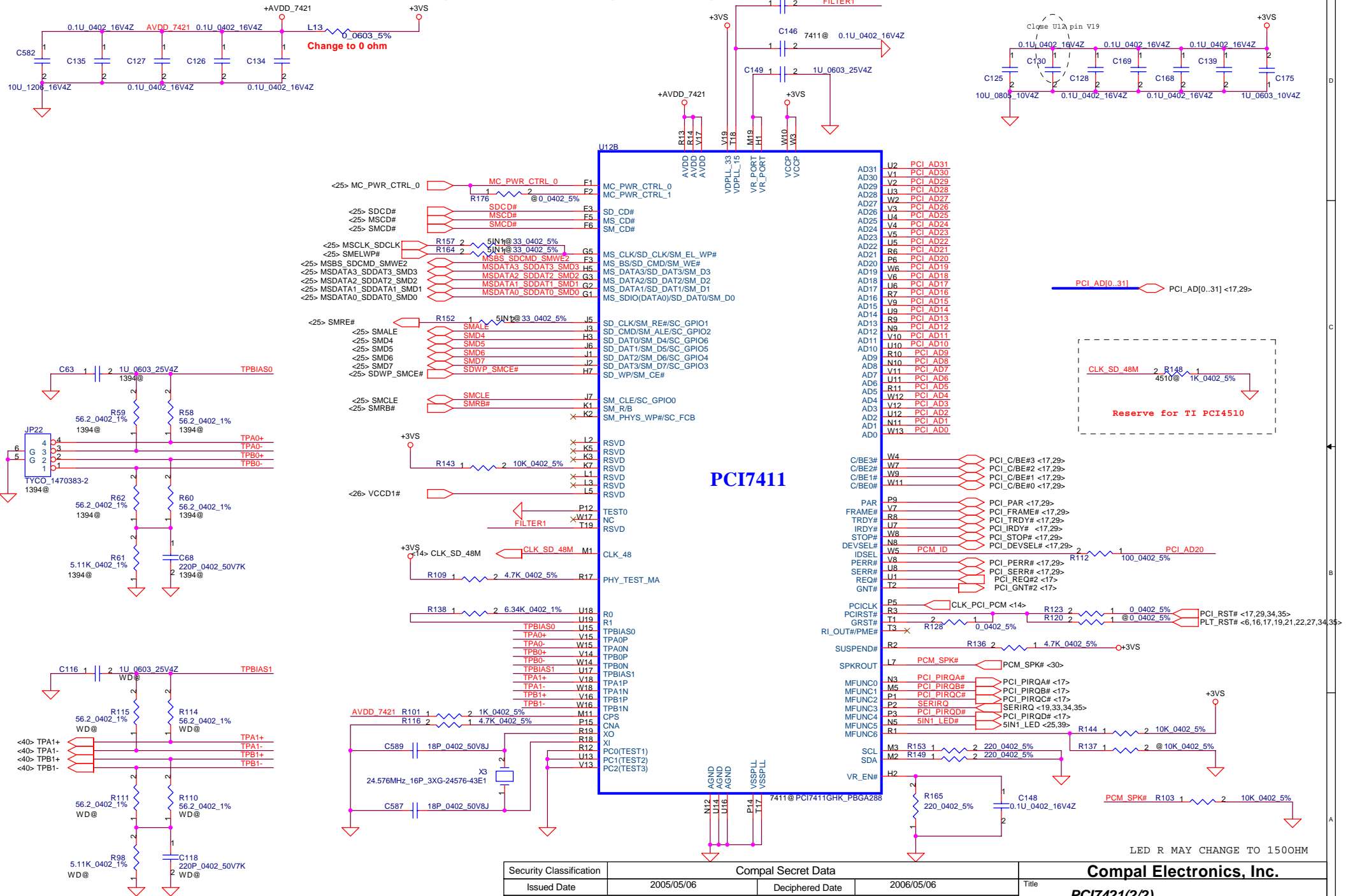
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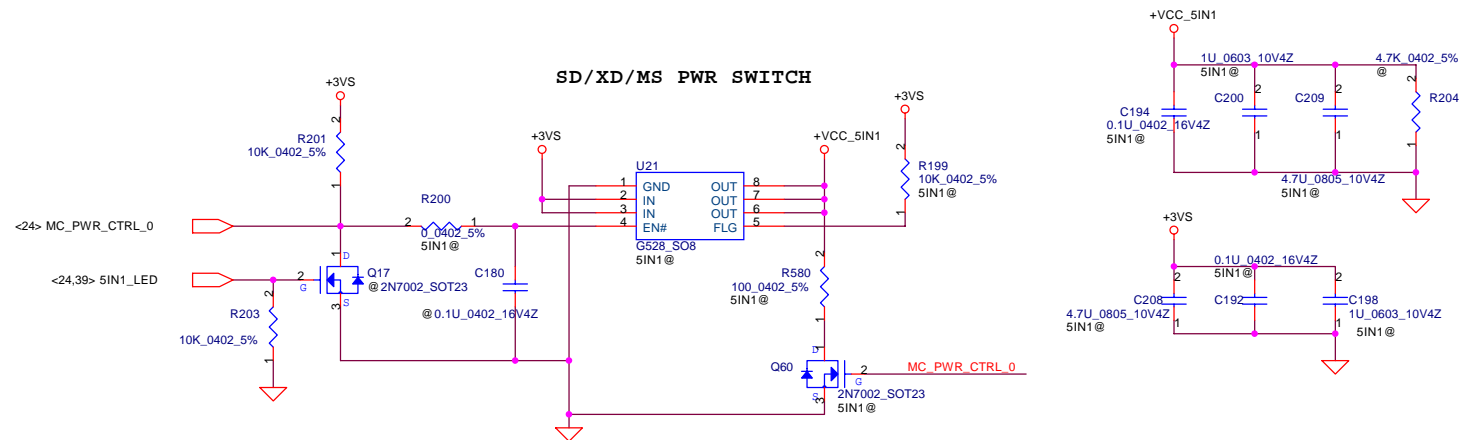
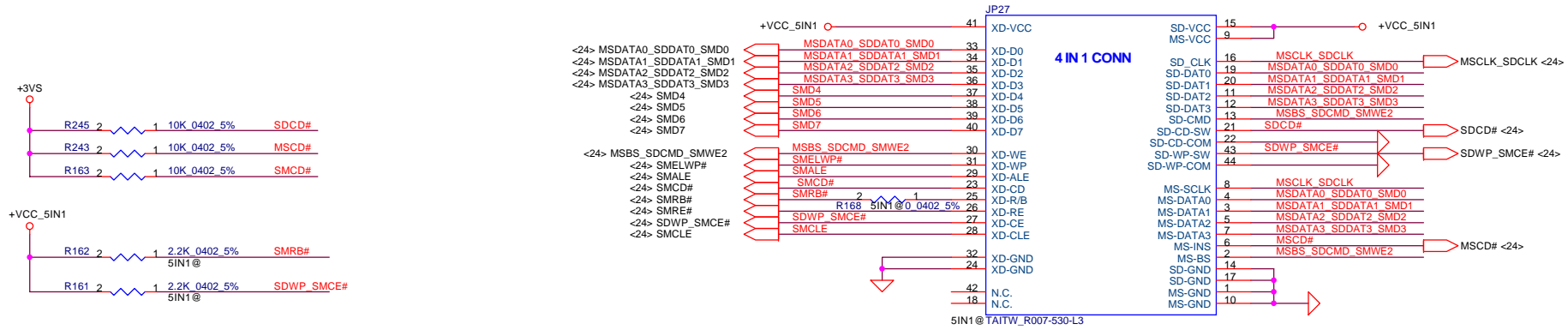


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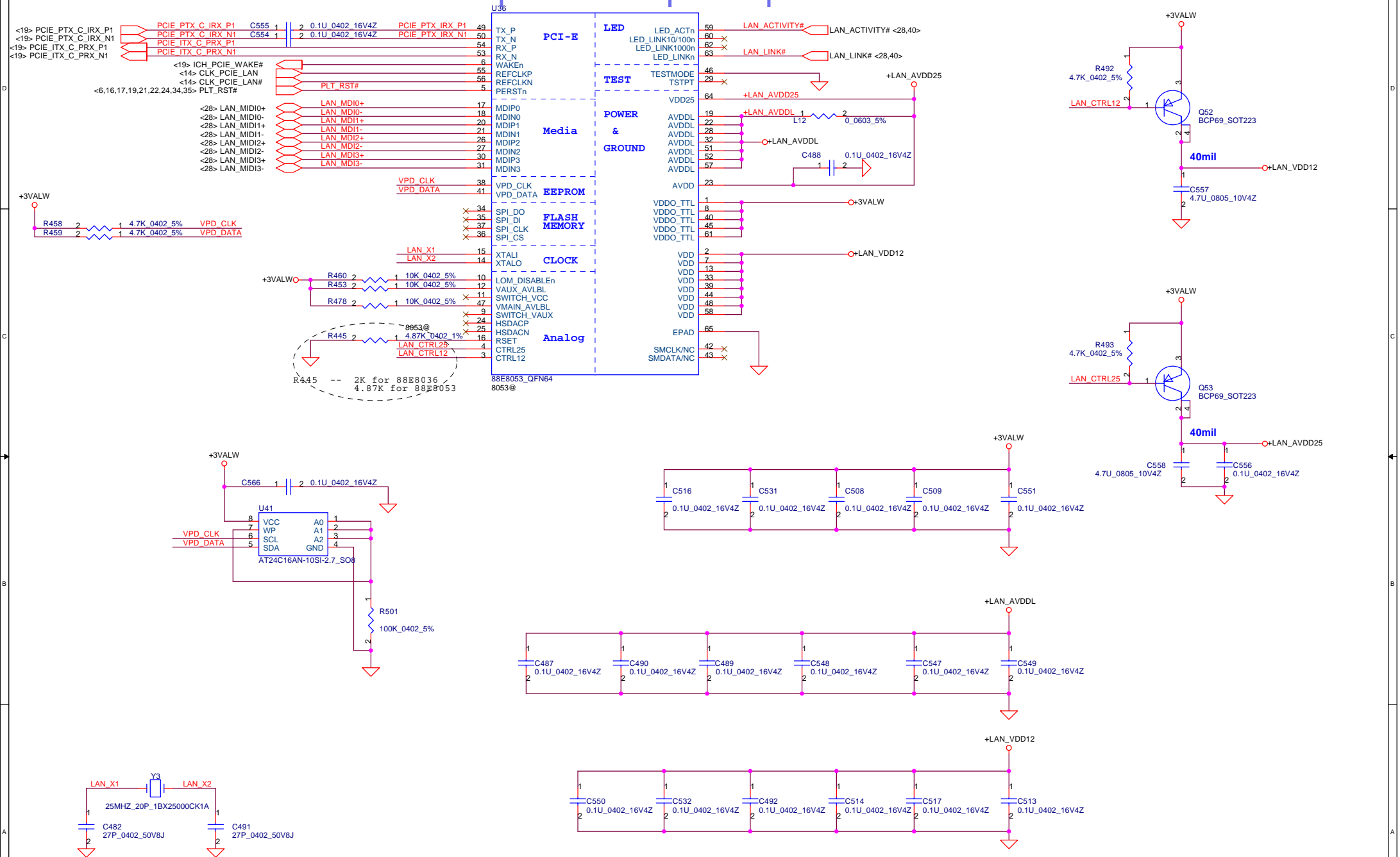


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5 in 1 CardReader Conn.



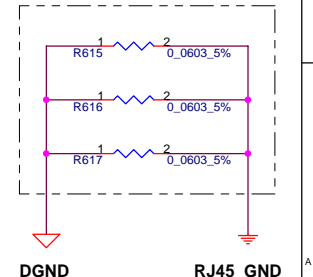
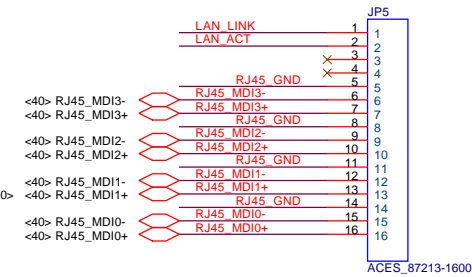
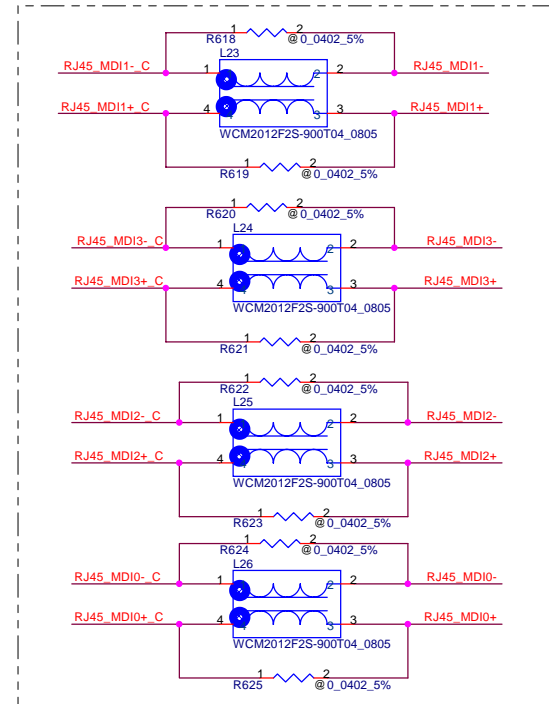
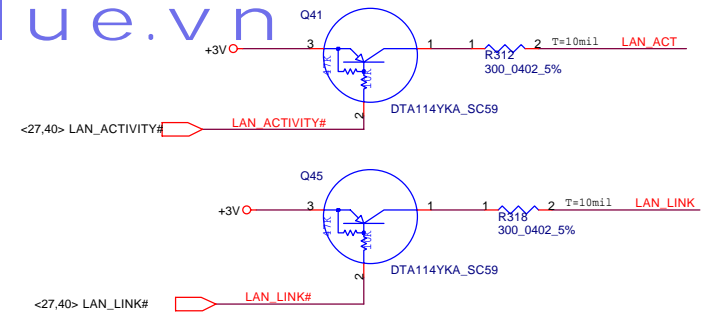
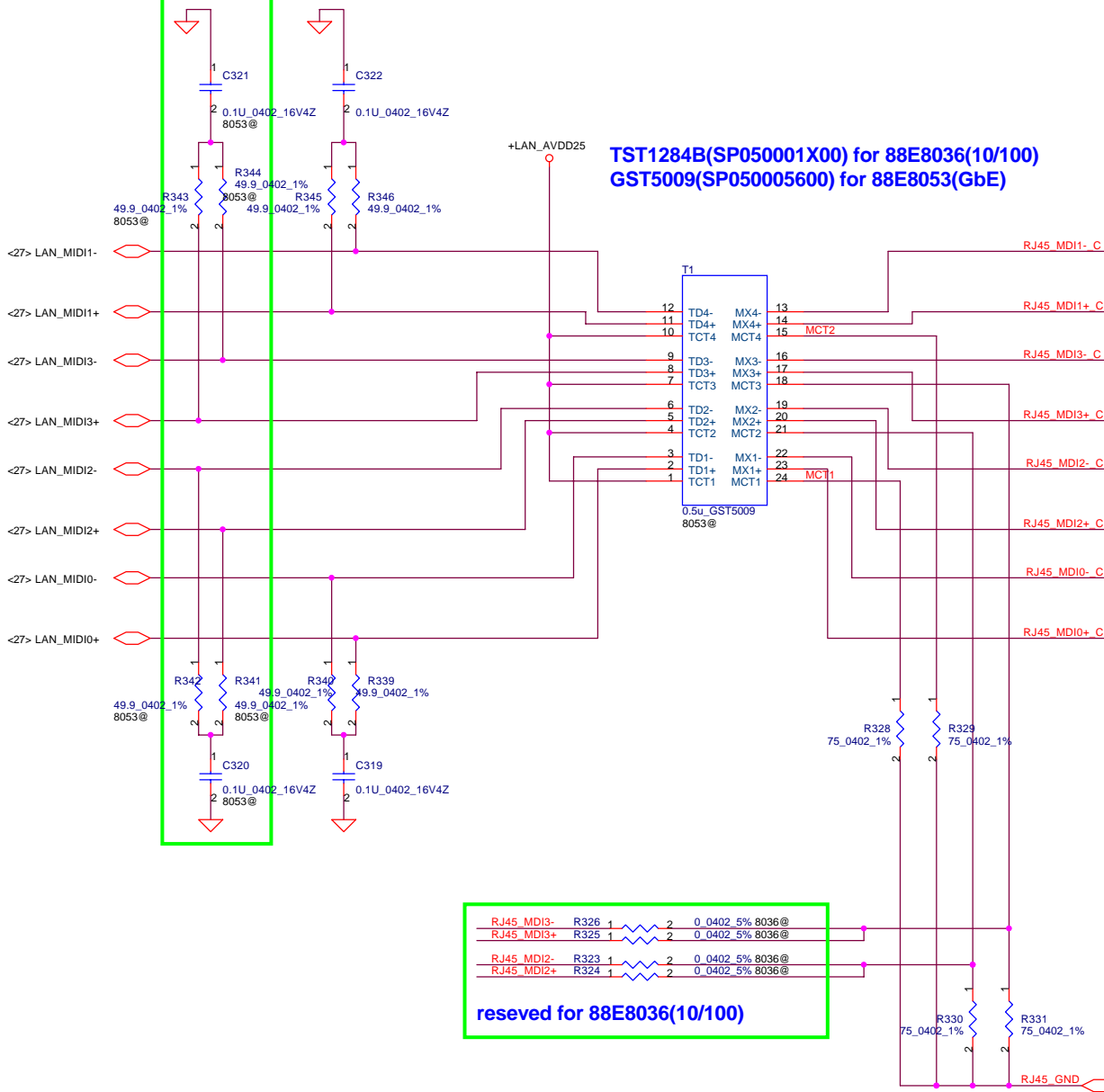
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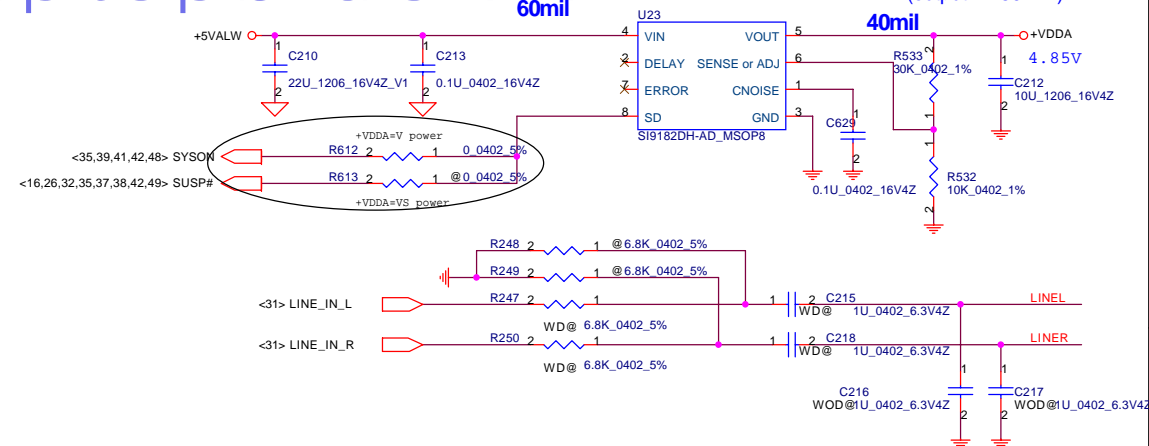
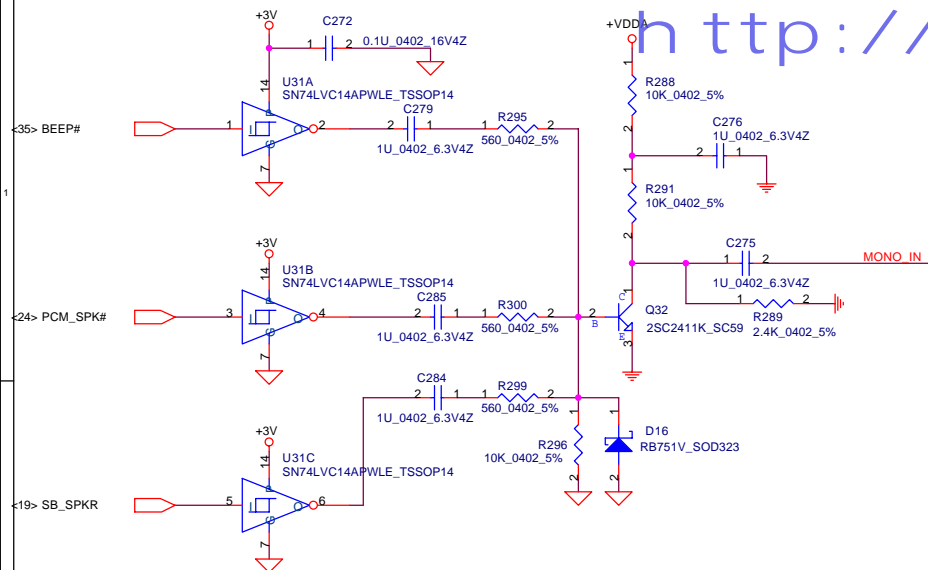
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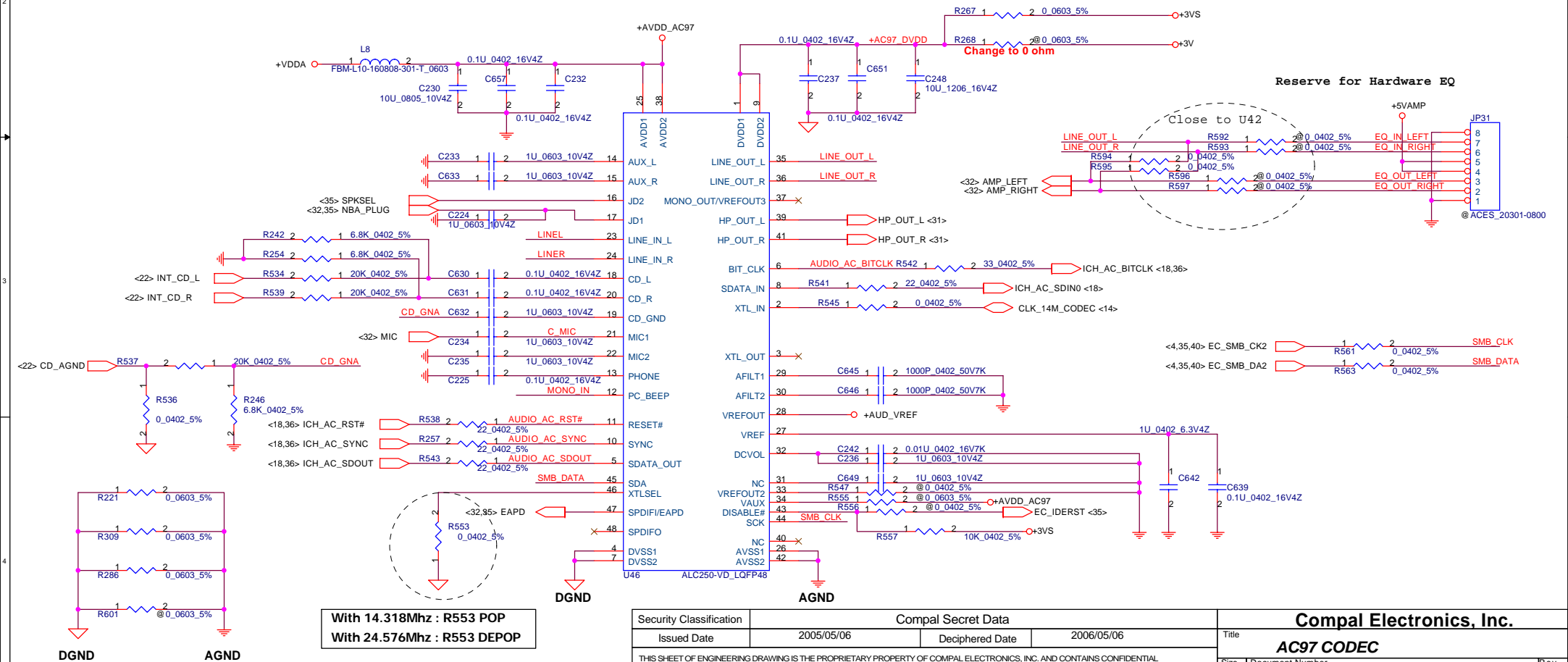
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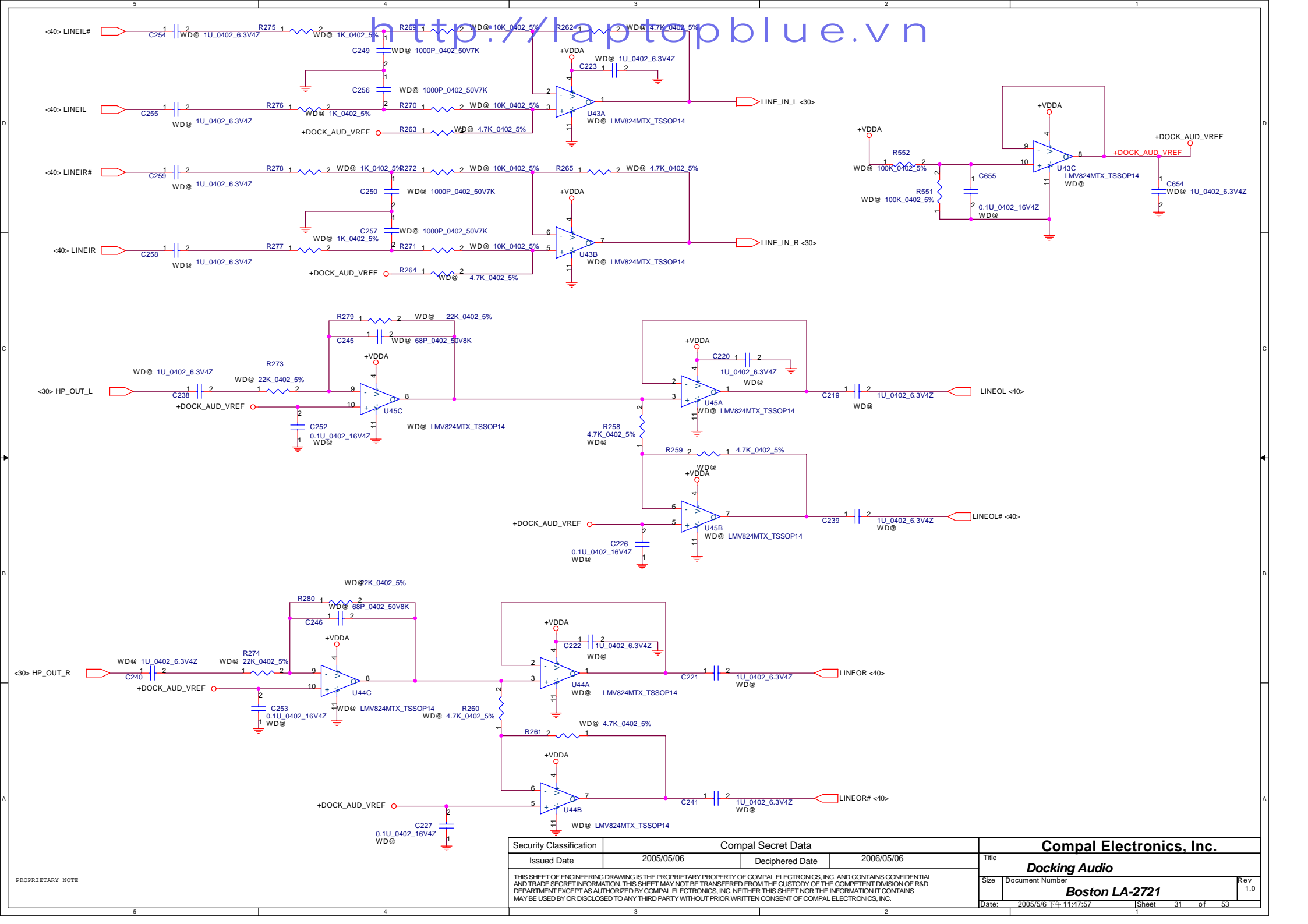


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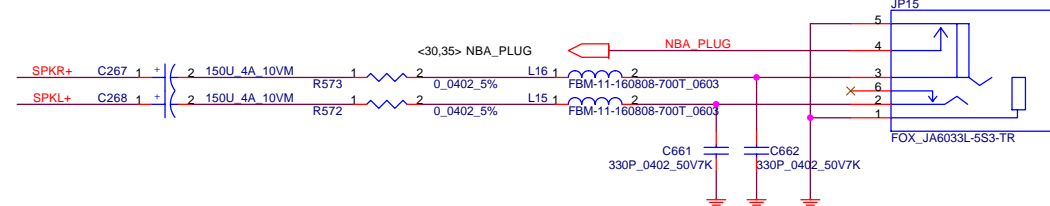
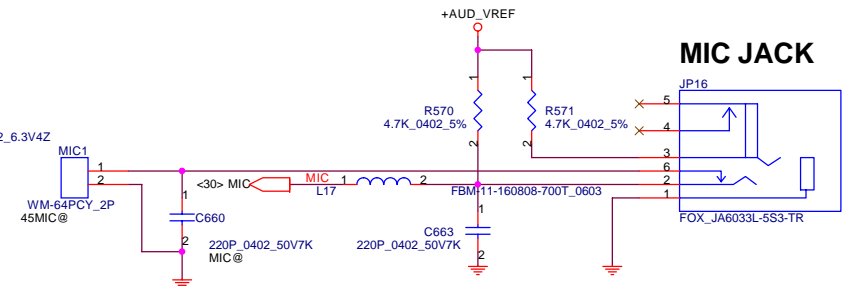
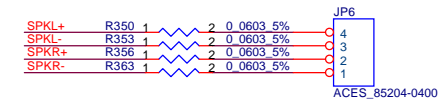
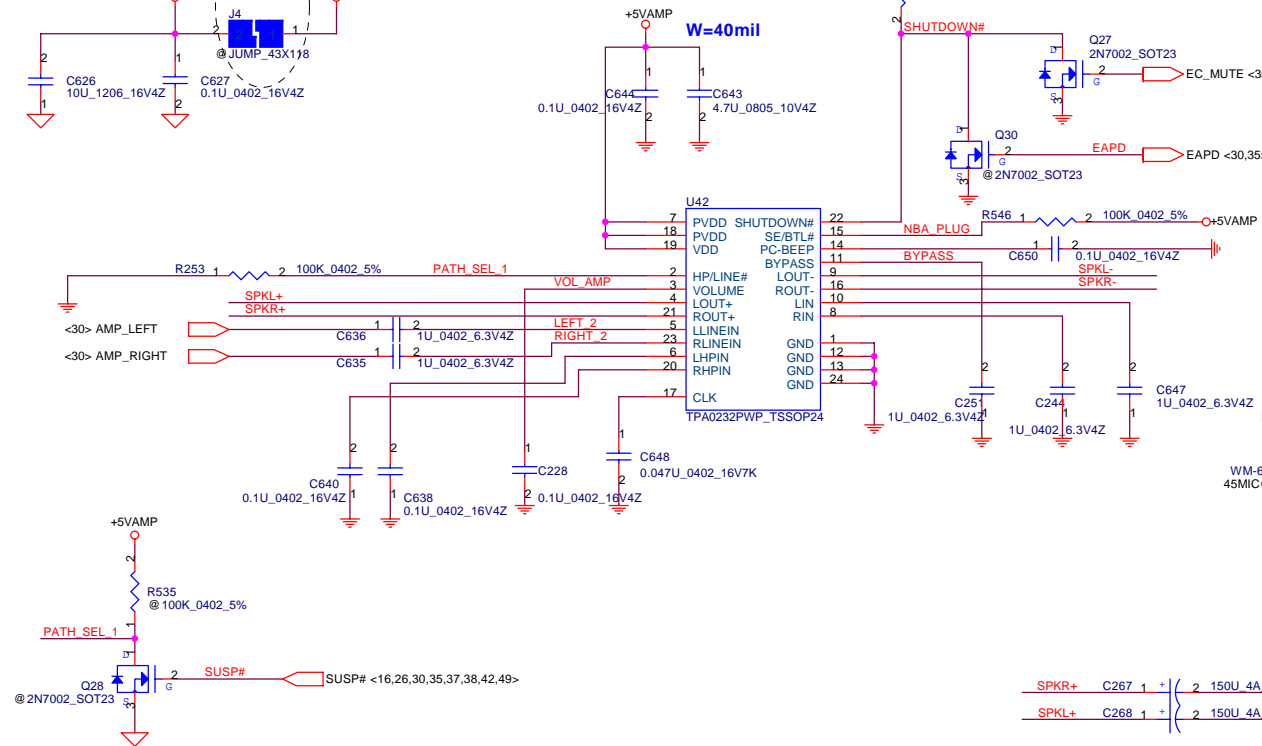
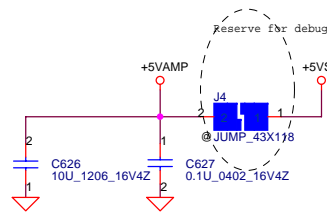


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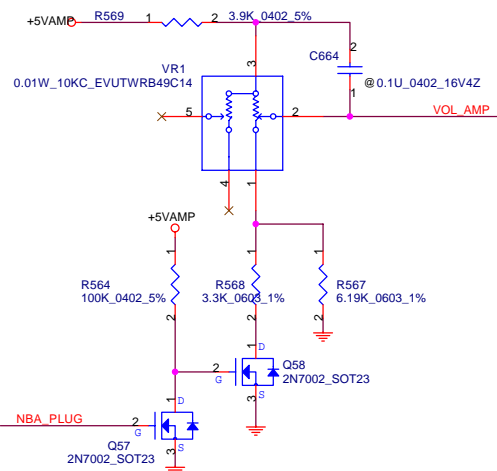




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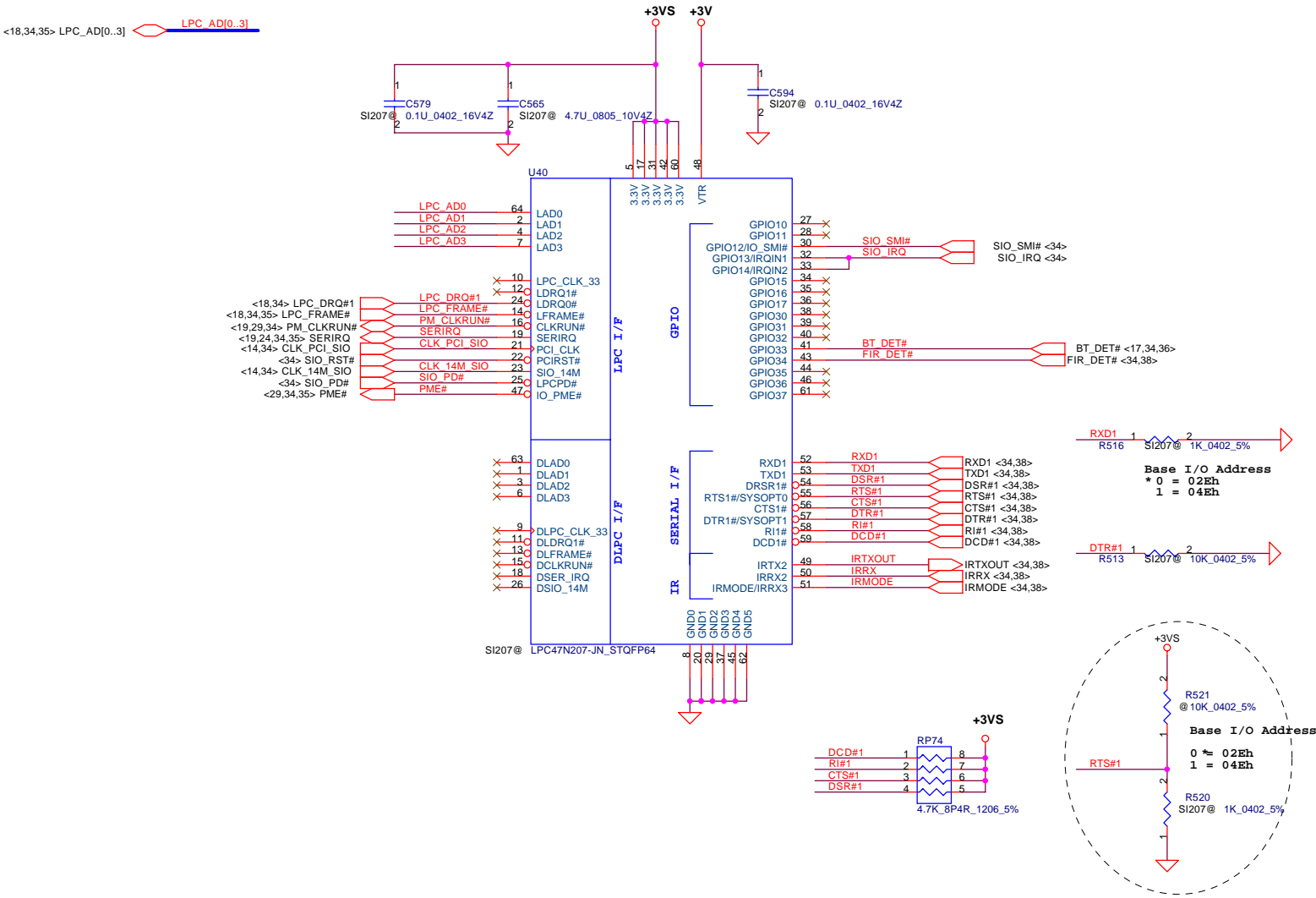


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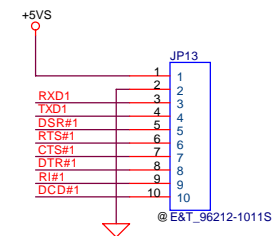
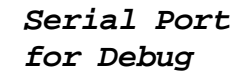
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R568	3.3K
R567	6.19K
Bias (Gain)	SPK 0.67 V 10 dB HP 1.54 V -6 dB

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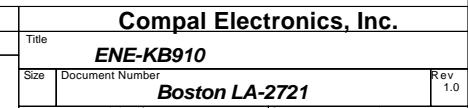


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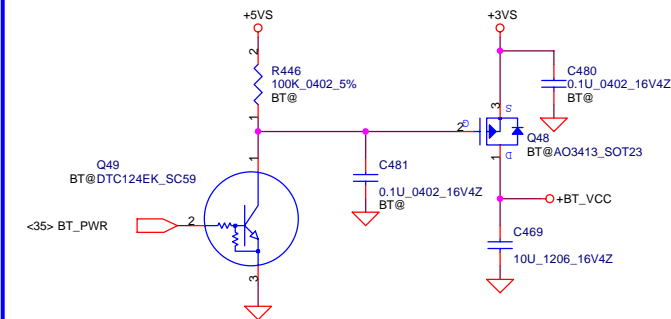


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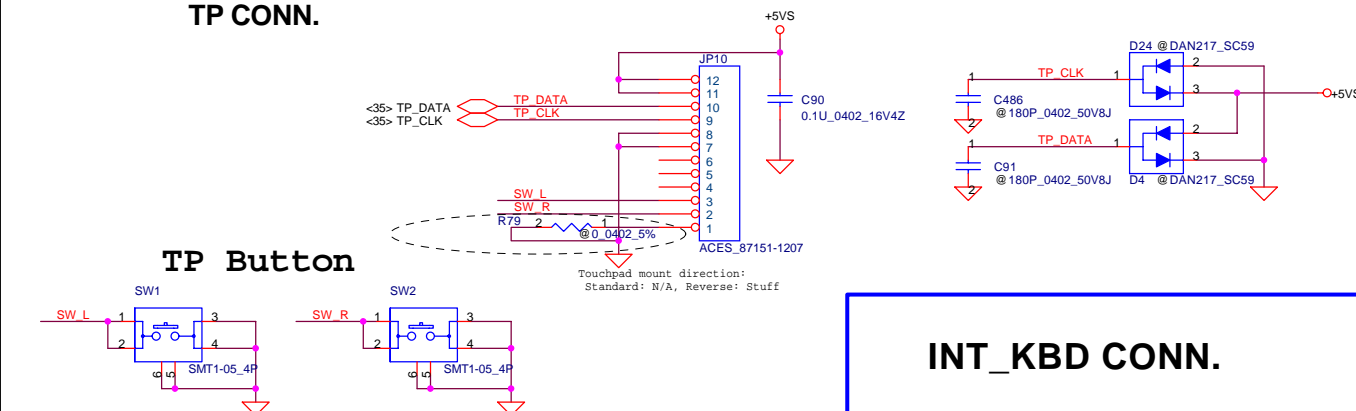
http://laptopblue.vn

BlueTooth Interface

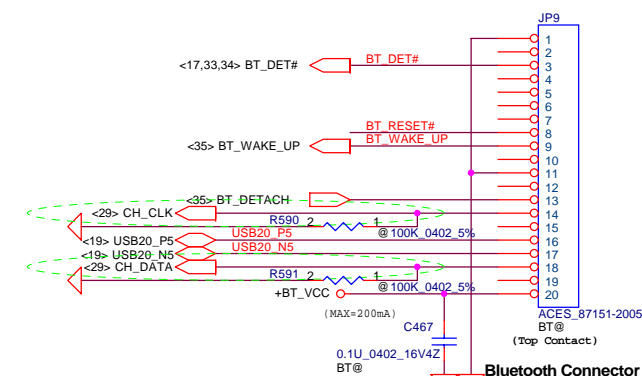
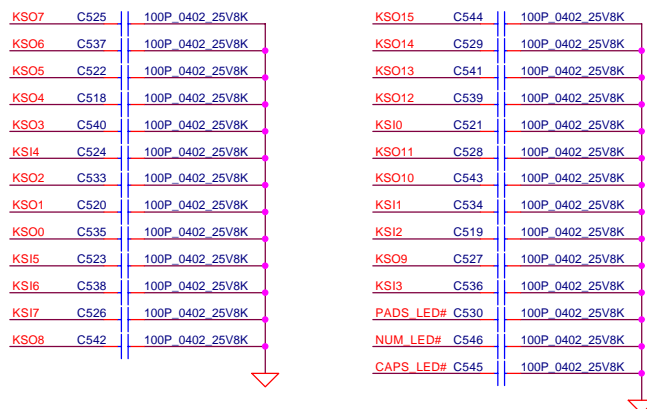


Module ID
Indication for polarity of reset
Reset input High Active --> Low ,
Reset input Low Active --> Open

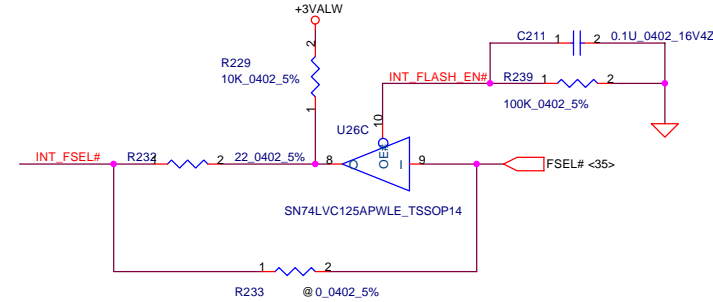
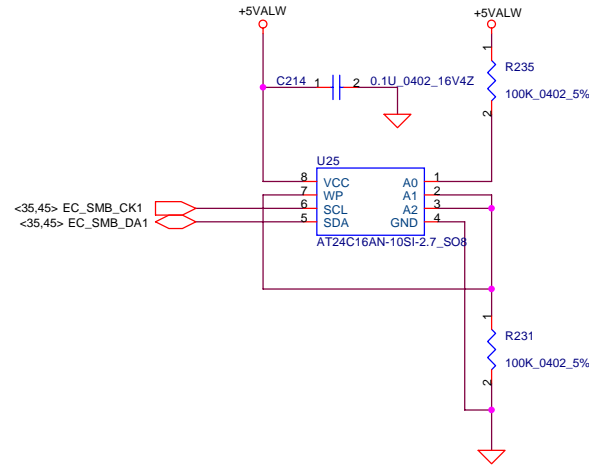
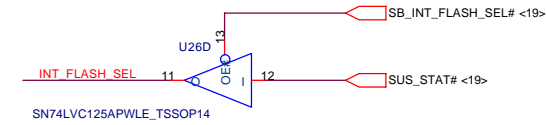
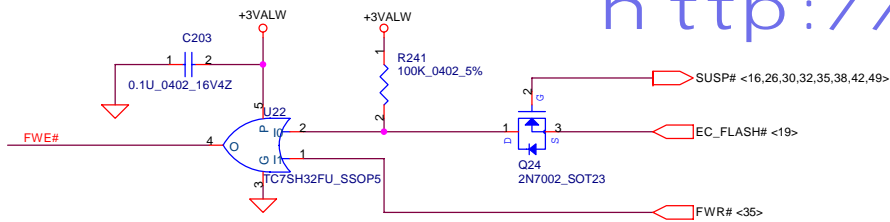
TP CONN.



INT KBD CONN.

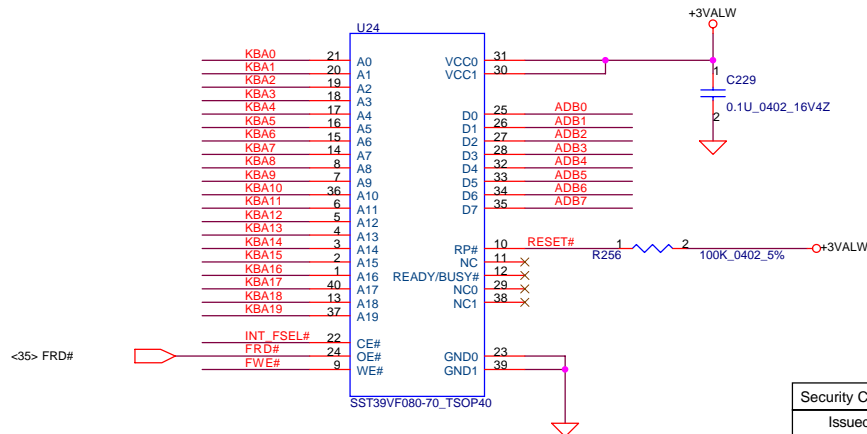


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						Size	Document Number			Rev. 1.	
						Boston LA-2721					
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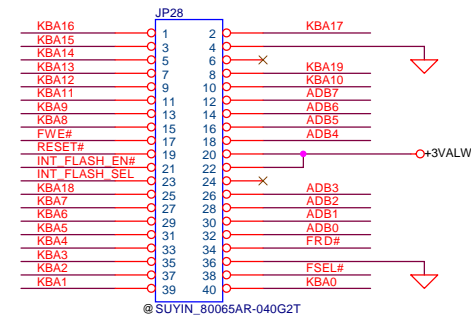


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<35> ADB[0..7] ADB[0..7]

1MB Flash ROM

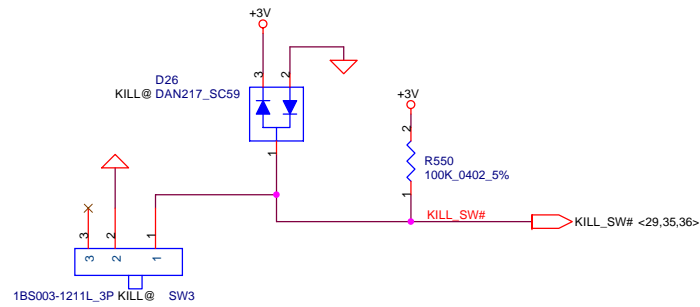


1MB ROM Socket

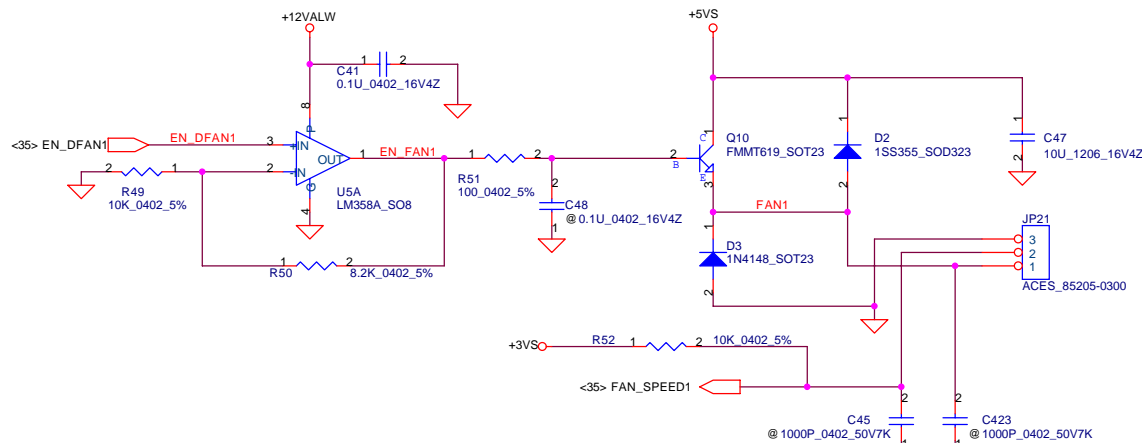


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						Size		Document Number		Rev	
								Boston LA-2721		1.0	
Date:		2005/5/6		14: 11:47:56		ISheet		37 of 53			

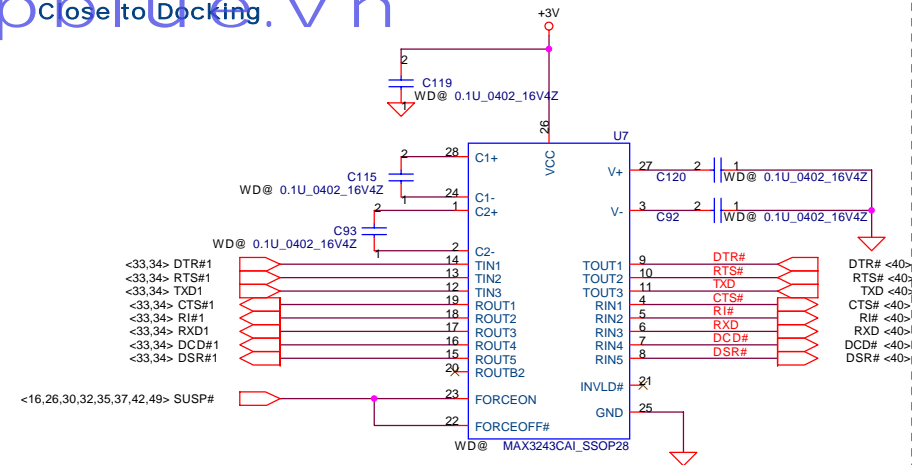
Kill SWITCH



FAN Conn

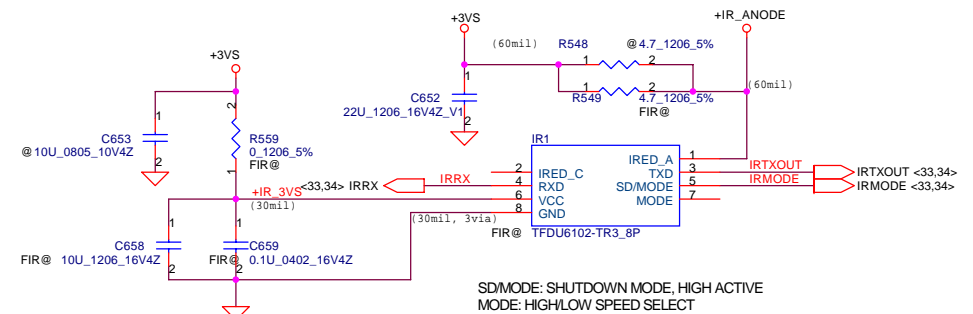
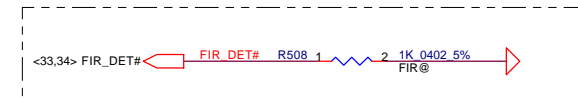


Close to Docking



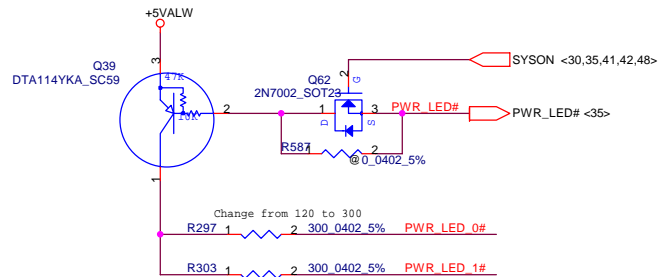
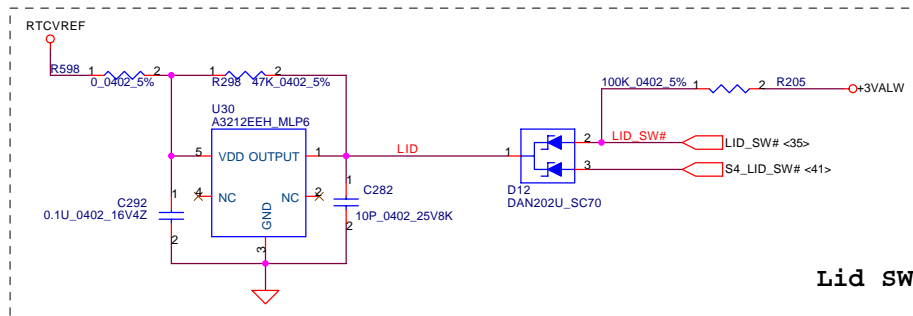
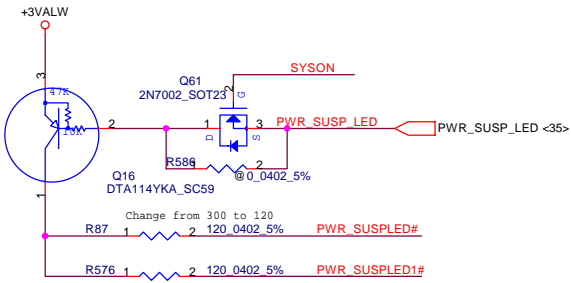
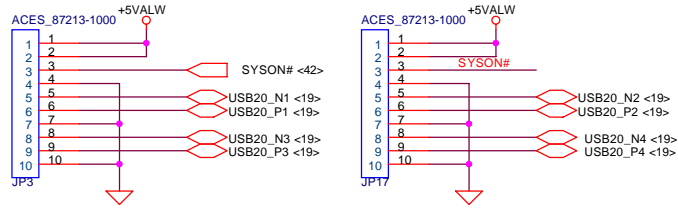
FIR Module

L: R POP; FIR Enable
H: R De-POP; FIR Disable



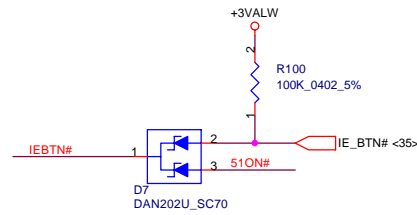
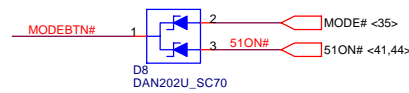
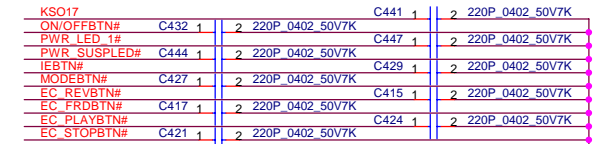
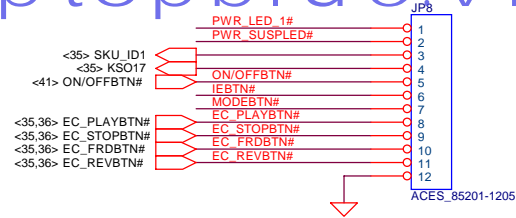
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USB Board Conn.

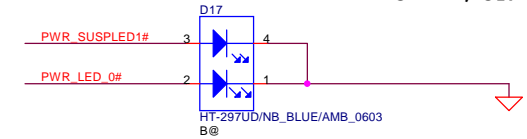


http://laptopblue.vh

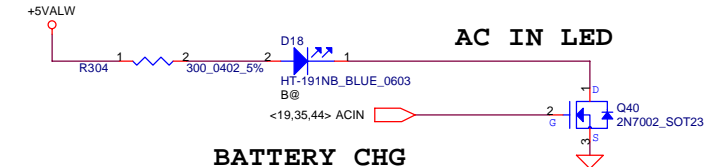
Switch Board Conn.



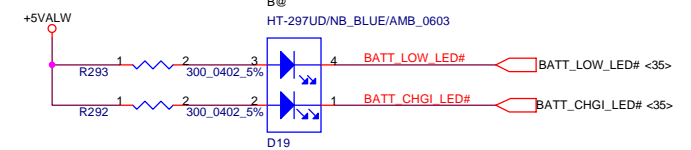
POWER/ON LED



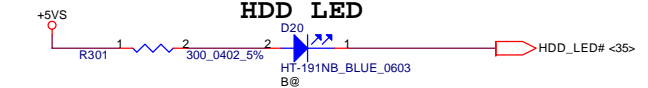
AC IN LED



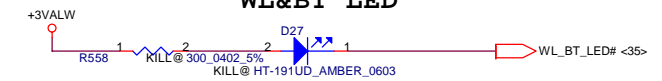
BATTERY CHG



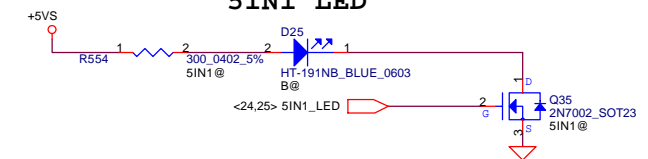
HDD LED



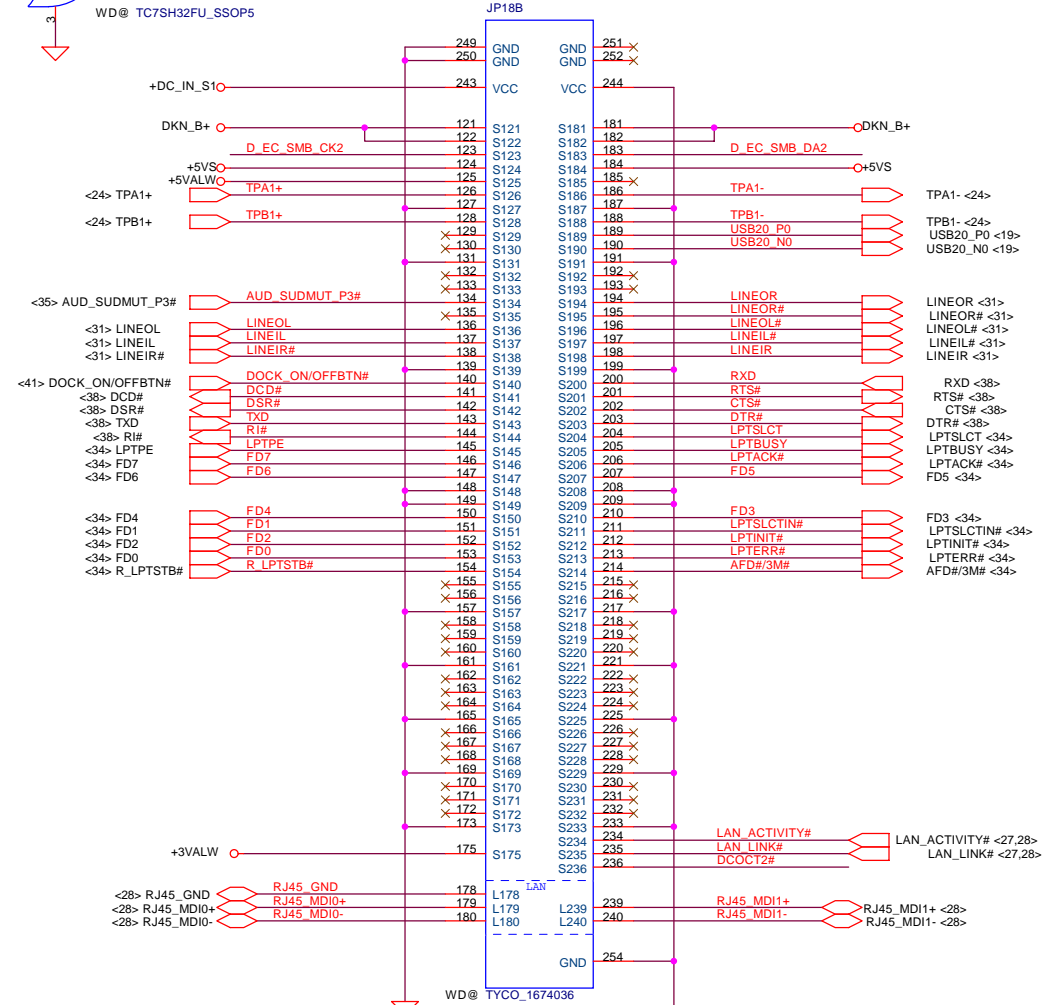
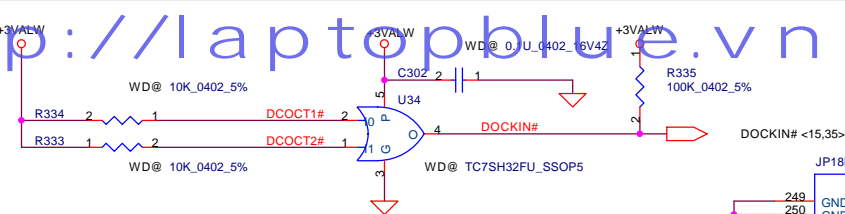
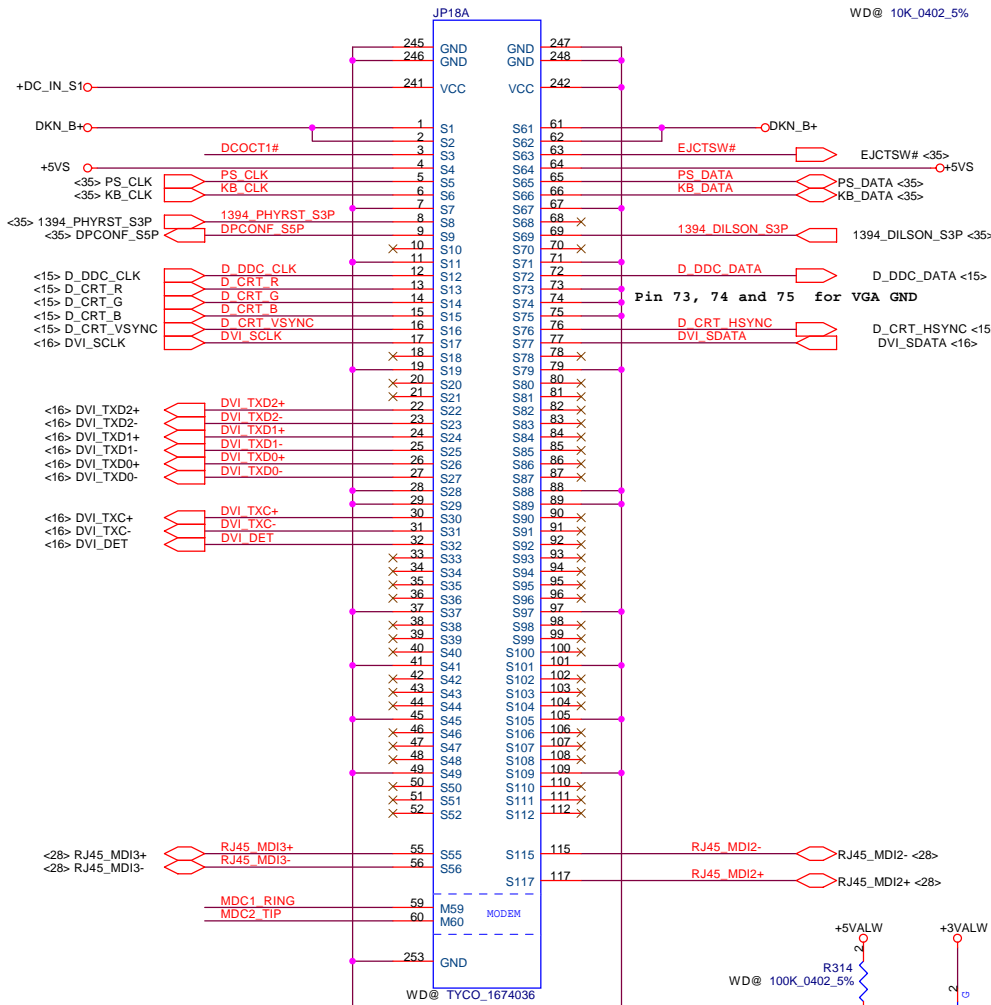
WL&BT LED



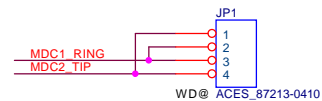
5IN1 LED



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Size		Document Number		Rev	
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MDC to Docking Conn.

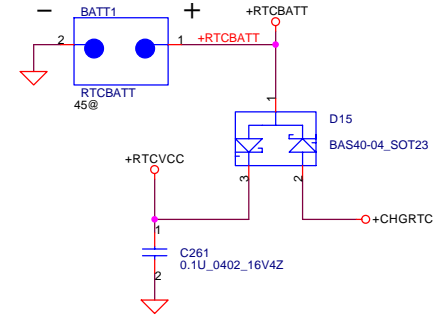
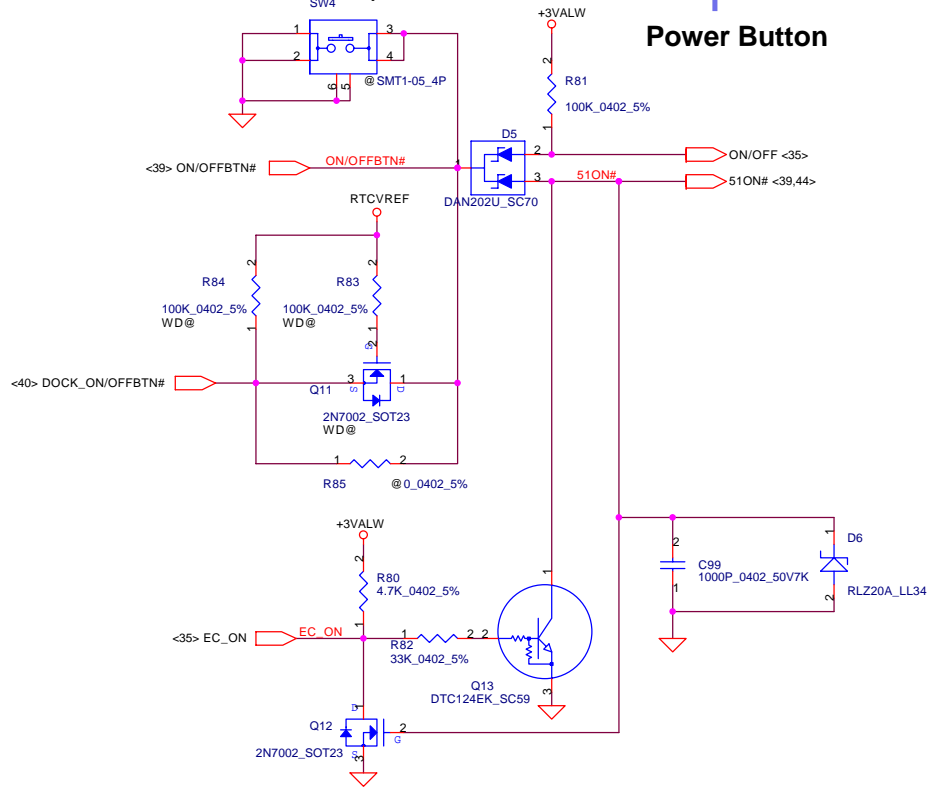


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					Boston LA-2721	1.0	
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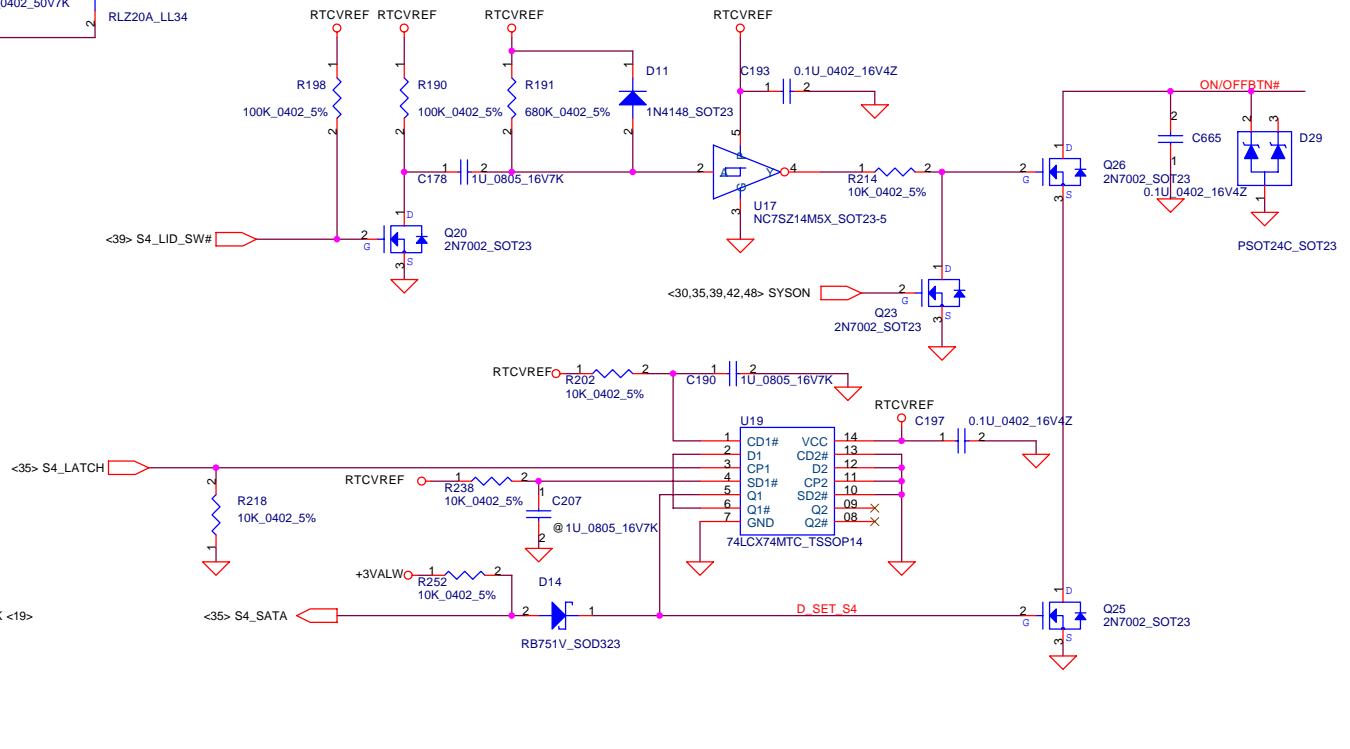
Reserved power button

Power Button

RTC Battery

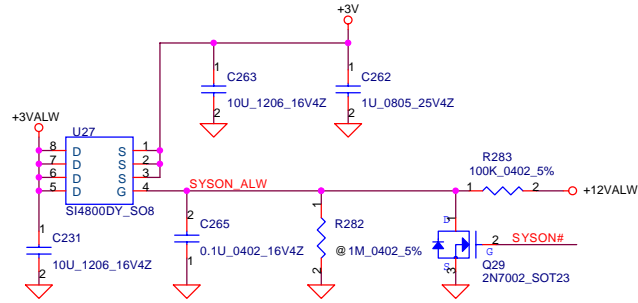


Power ON Circuit

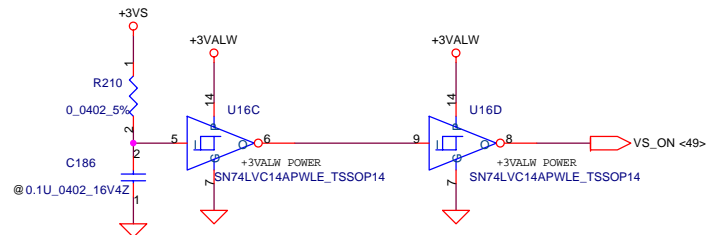
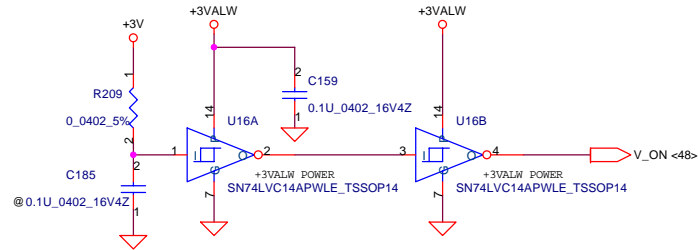
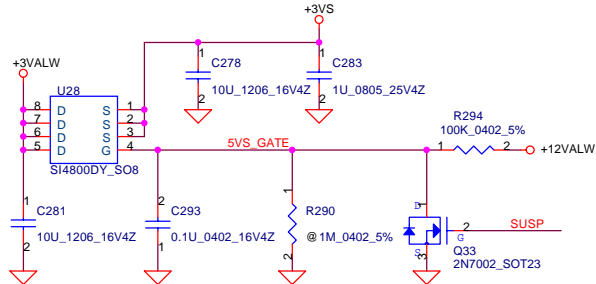


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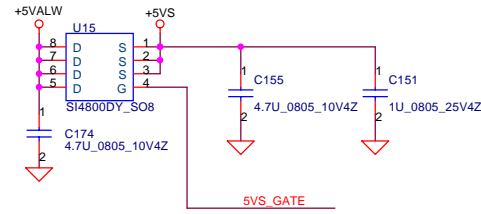
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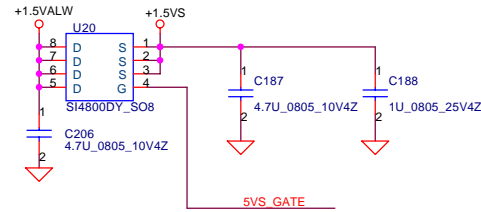
+3VALW TO +3VS



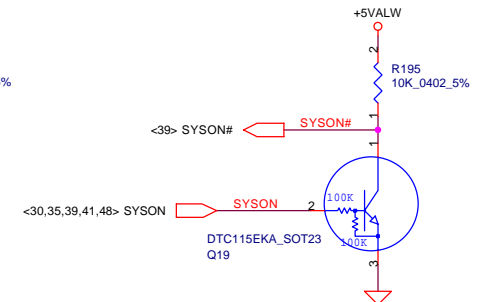
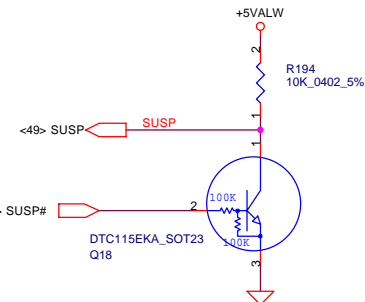
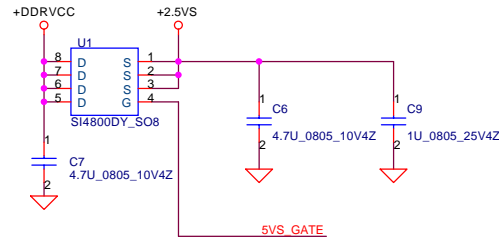
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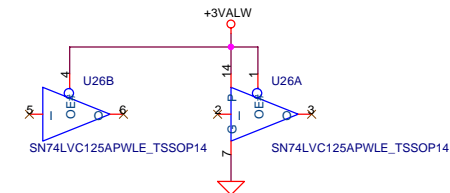
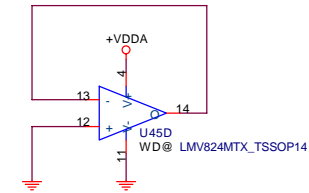
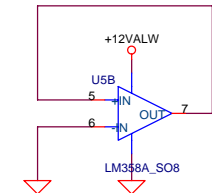
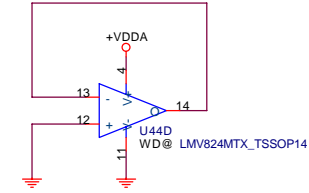
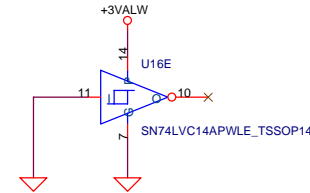
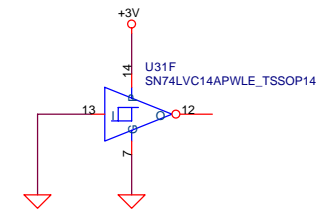
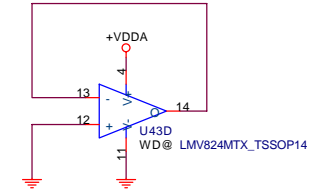
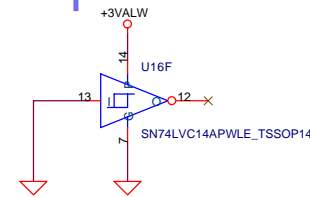
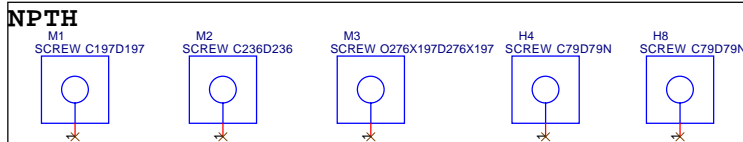
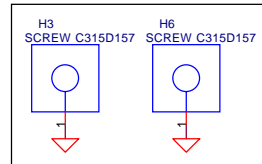
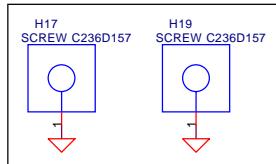
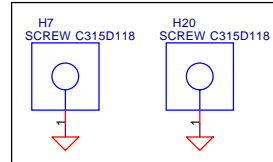
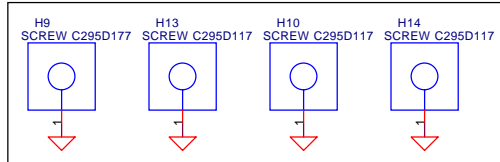
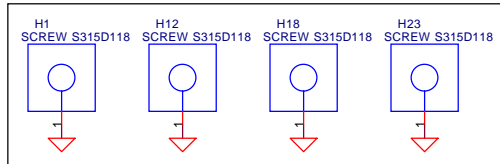
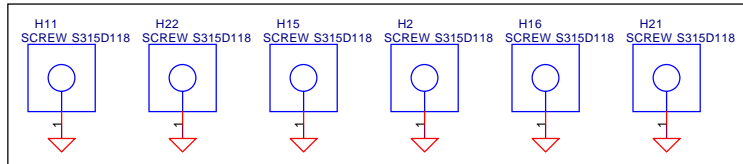
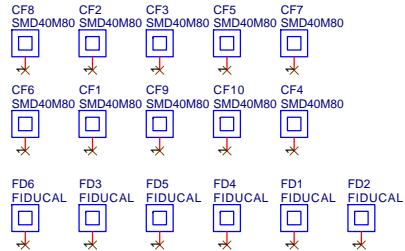
+1.5VALW TO +1.5VS



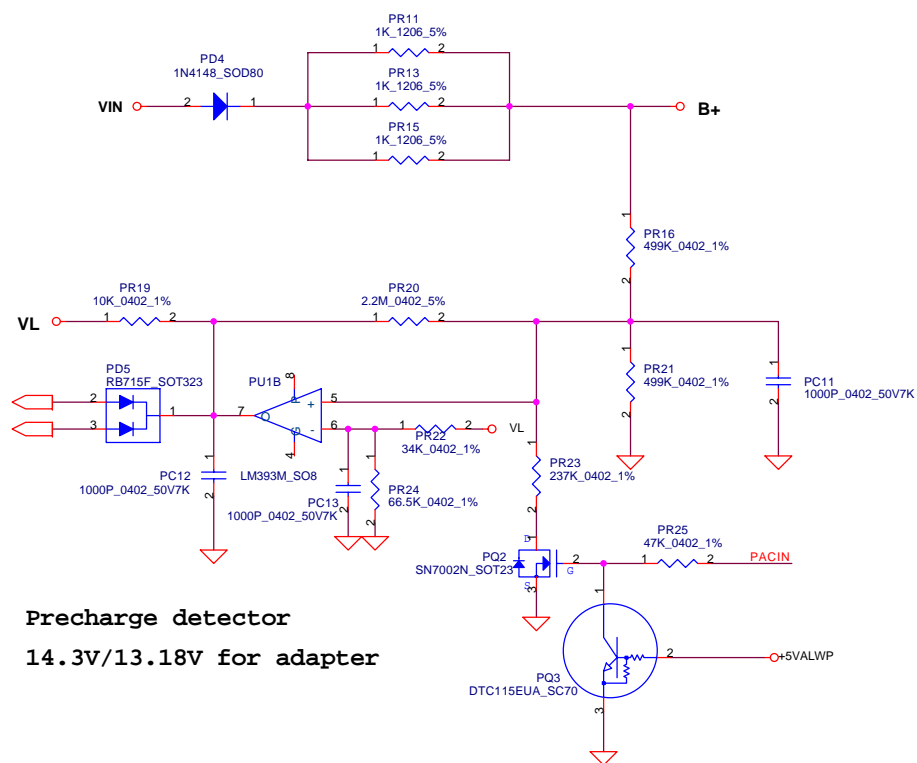
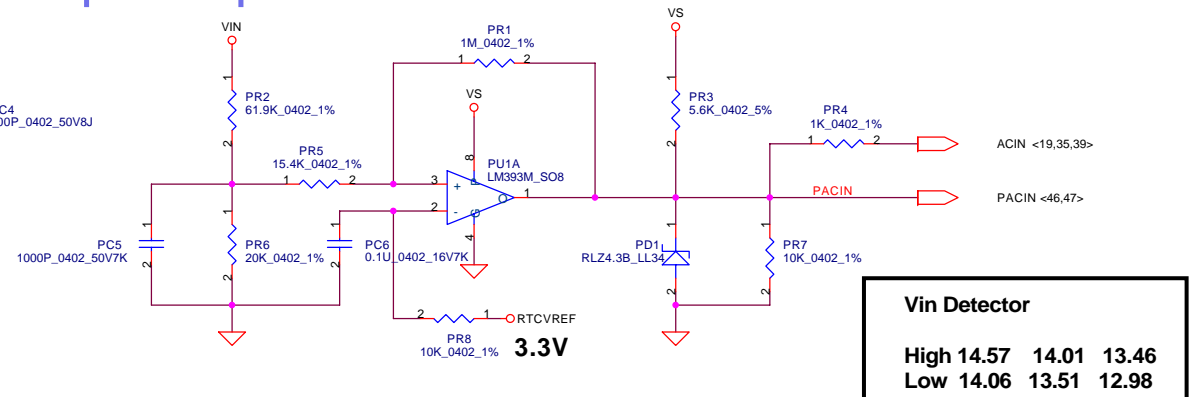
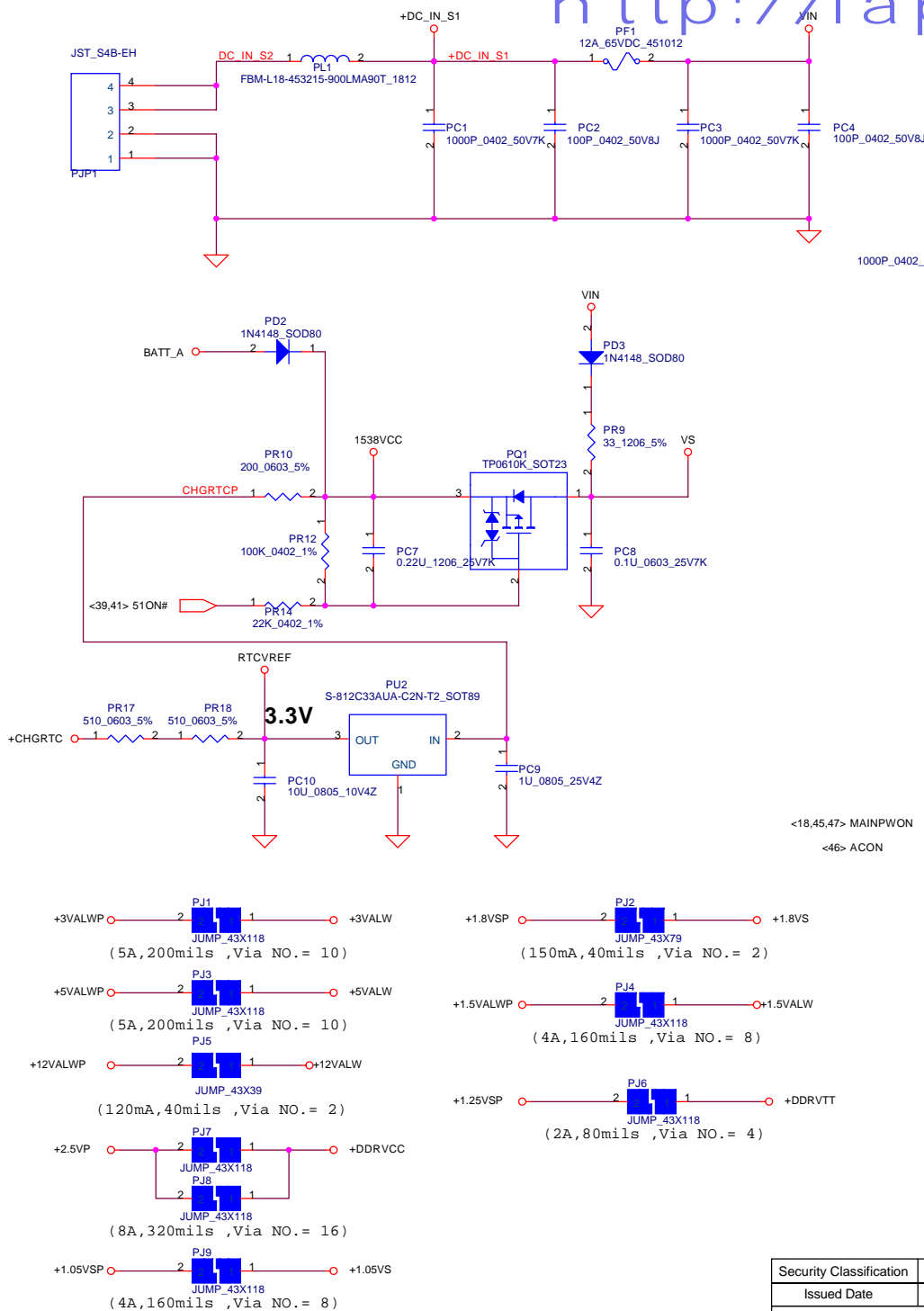
+DDRVC to +2.5VS (DDR1)



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Size	Document Number	Rev		1.0	
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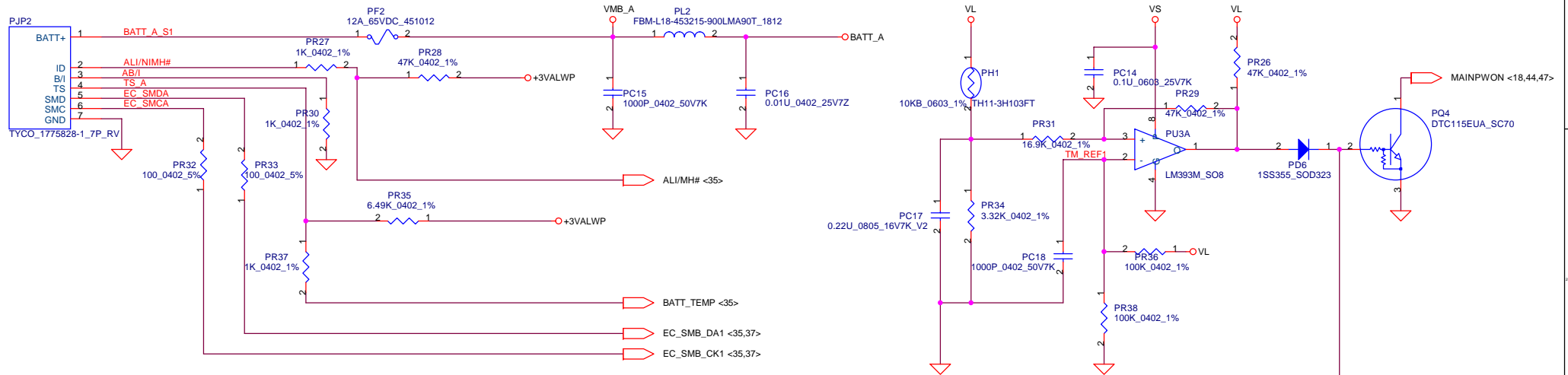
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				Rev	1.0



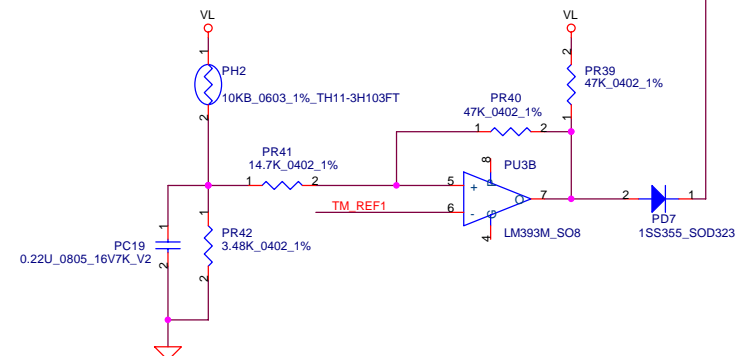
Precharge detector
14.3V/13.18V for adapter

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						Size		Document Number		Rev	
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PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C

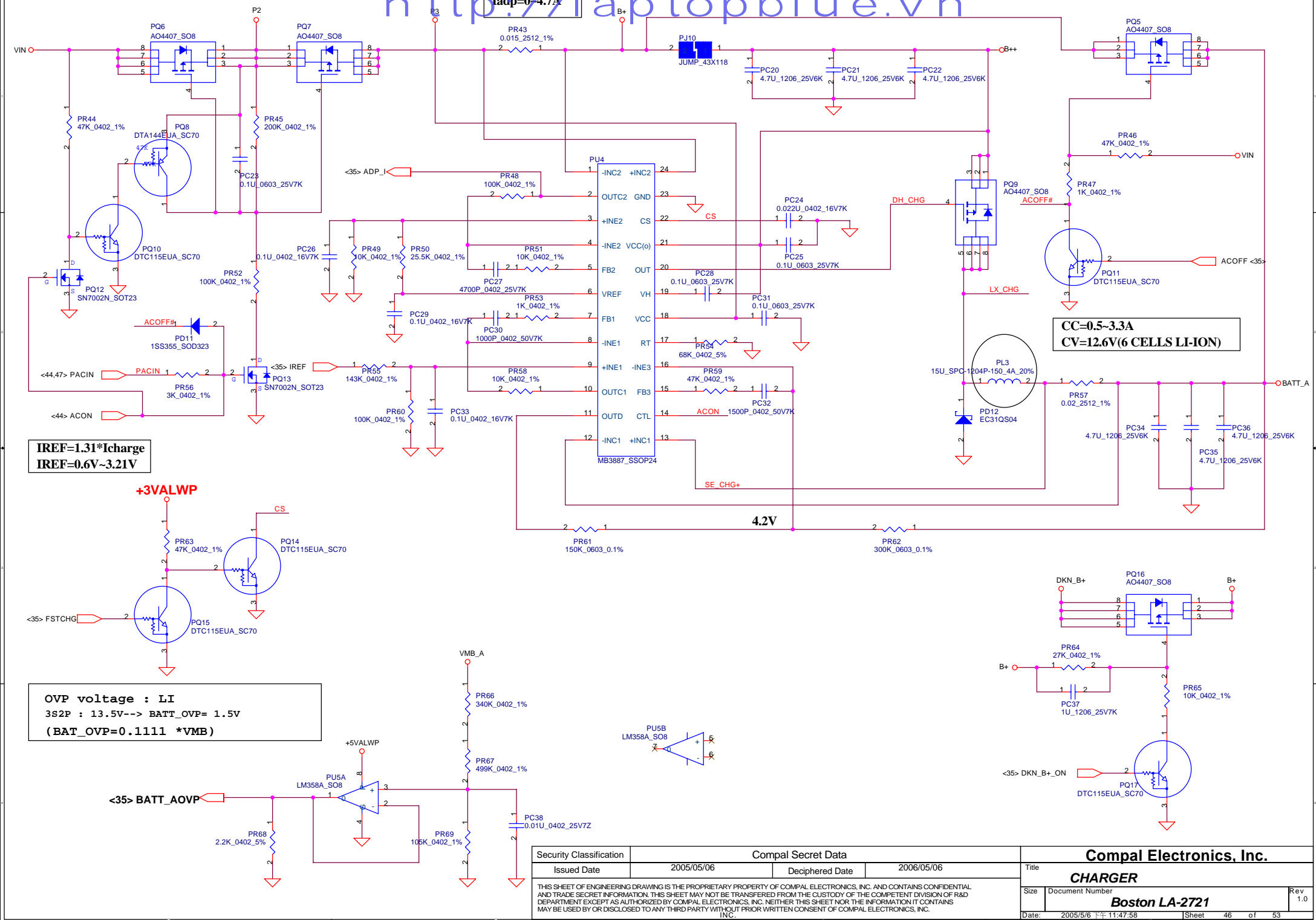


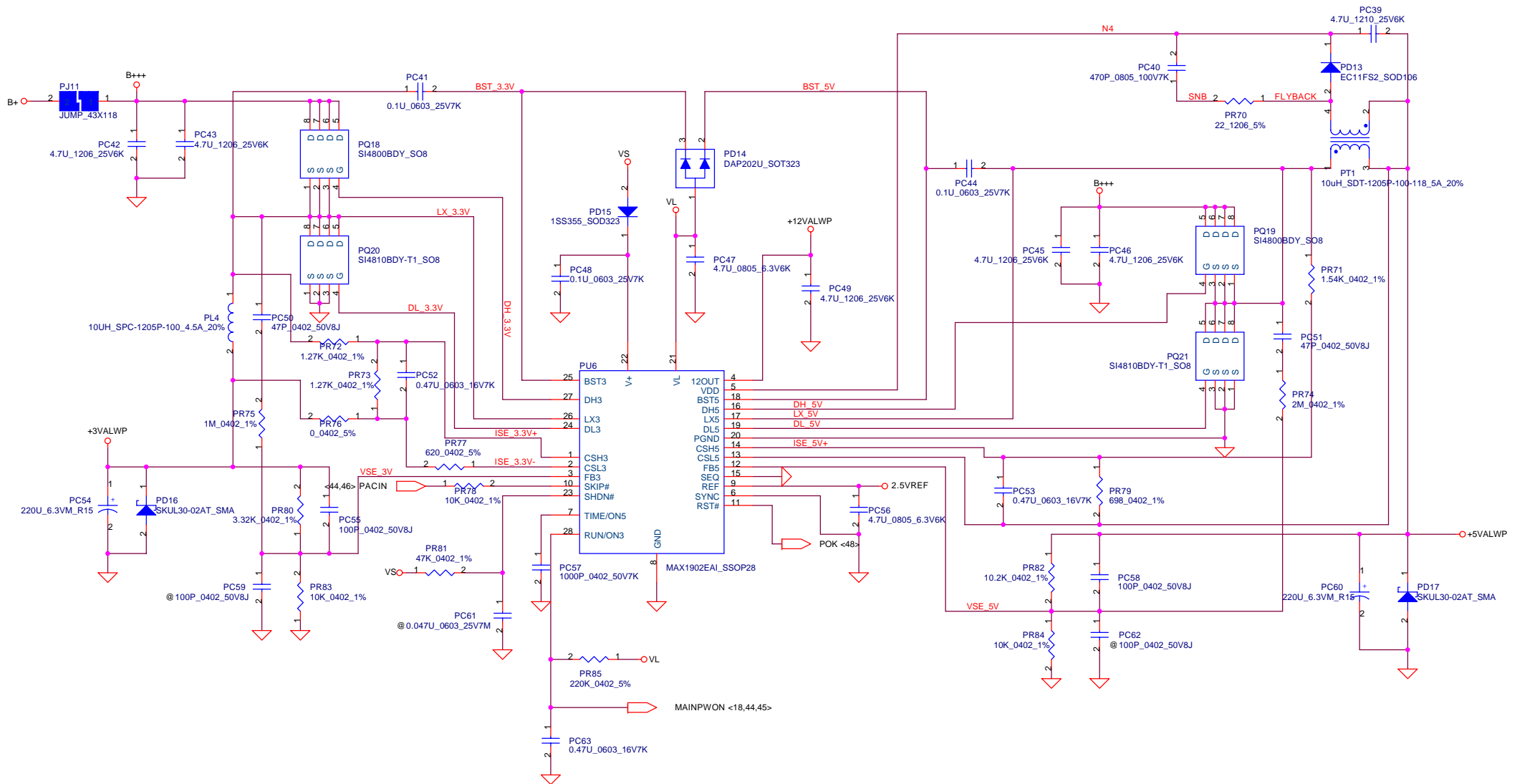
PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C



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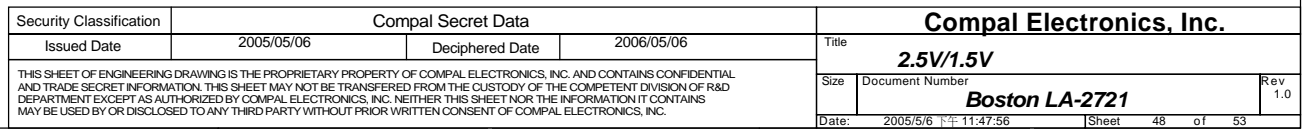
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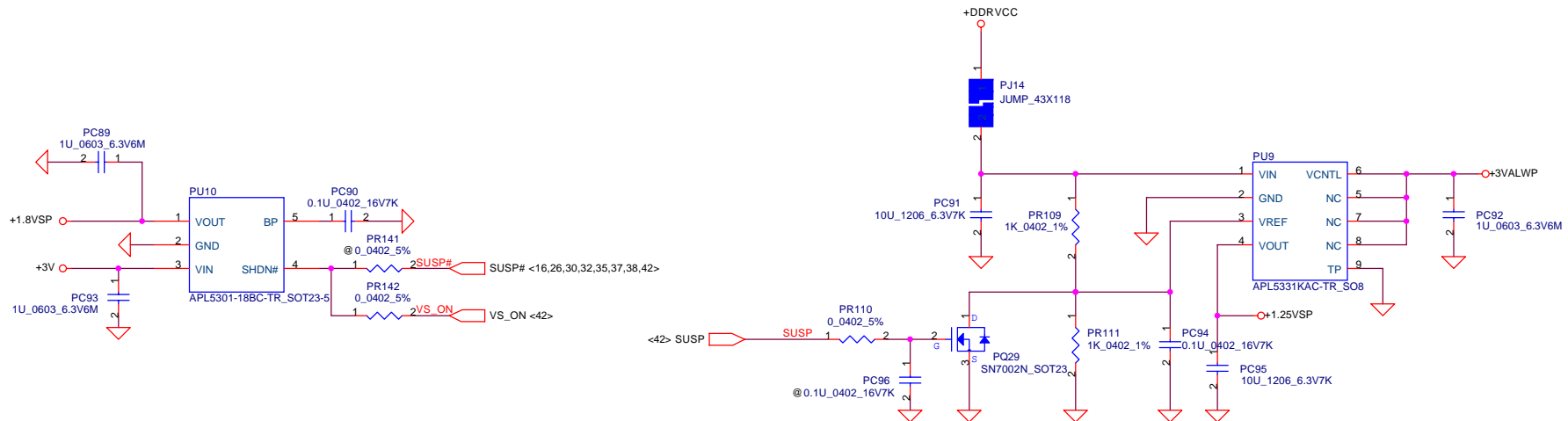
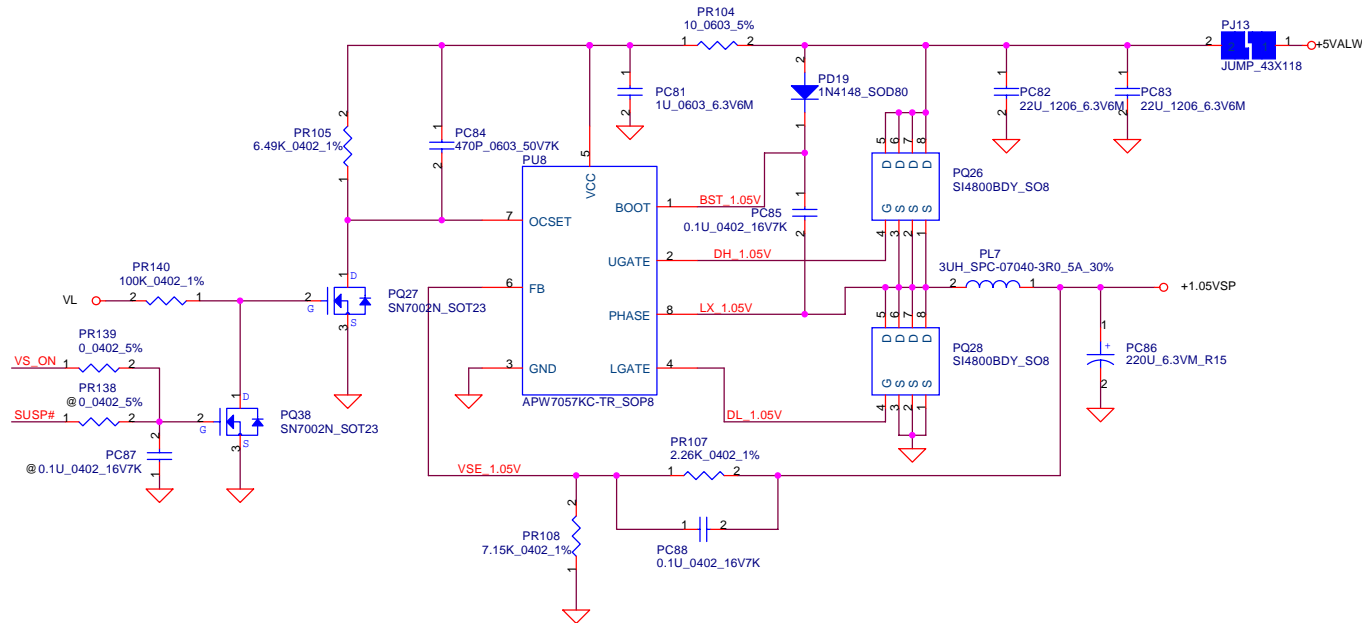




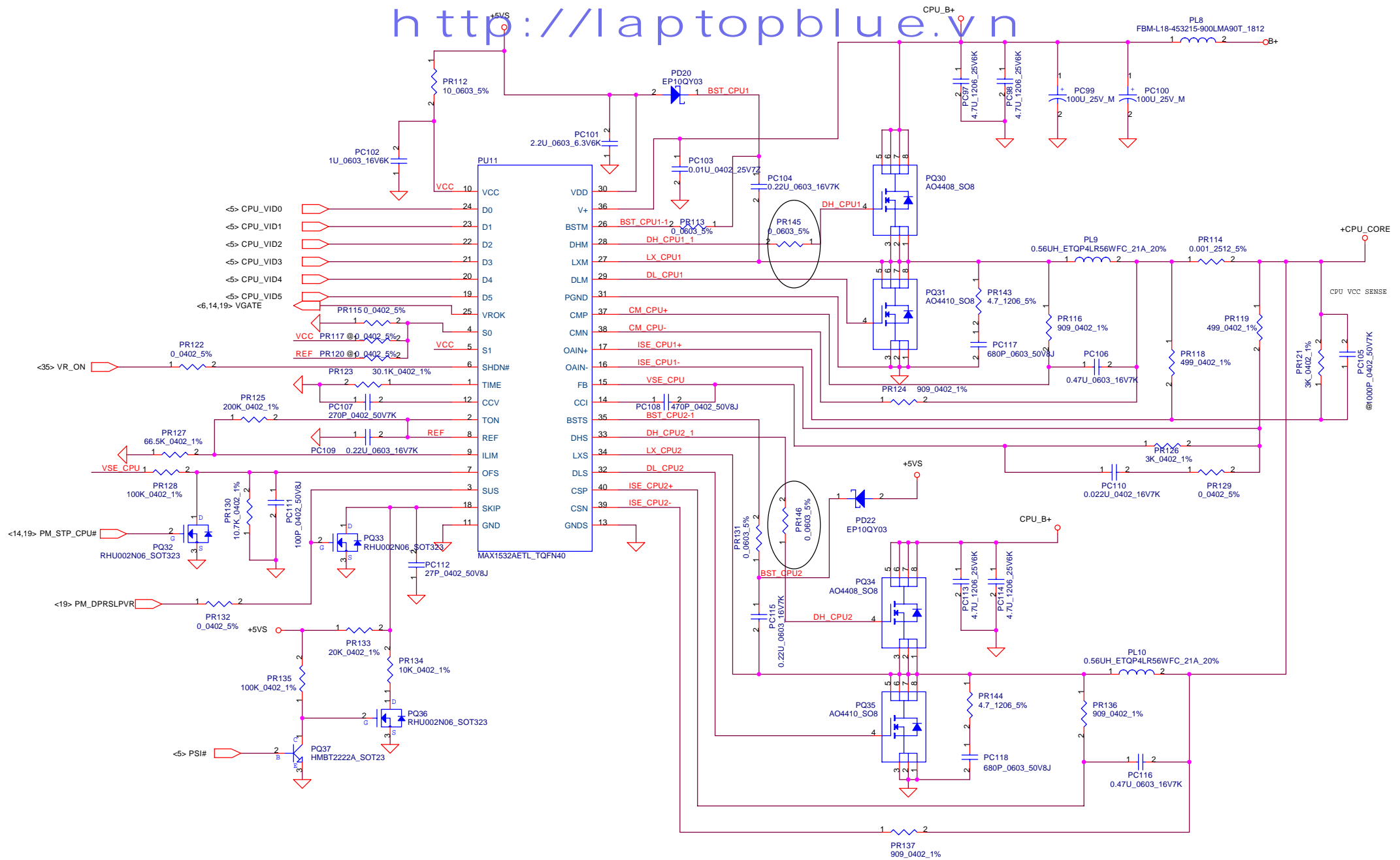
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2.5V





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ECU00 PIR List

http://laptopblue.vn

***** From Rev:0.1 to Rev:0.2 PIR List *****

1. Change R30 from 0603 package to 1206 package (Page9)
2. Add filter at CRT signal for EMI request (Page15)
3. Delete F1, D22 and change +CRT_VCC to +5VS (Page15)
4. Delete Software DJ circuit and change +5VCD to +5VS (Page21,22,32)
5. Chnage LAN_LINK and LAN_ACT signal to JP5 pin1,2 (Page28)
6. Add R588, R589, R590, R591 for co-existance function (Page29,36)
7. Add JP31 and R592~R597 for hardware EQ reserve (Page30)
8. Add SKU ID table (Page3,35)
9. Change JP3 and JP17 to 10pin (Page39)
10. Change U30 power from +3VALW to +CHGRTC (Page39)

***** From Rev:0.2 to Rev:0.3 PIR List *****

11. Reverse Q41, Q45 pin1, pin3 (Page28)
12. Non-stuff R586, R587 (Page39)
13. Change D27 to Amber LED (Page39)
14. Change U30 power to RTCVREF (Page39)
15. Non-stuff R268, R556 and Stuff R268, R557 (Page30)
16. Remove SATA 88SA8040 crystal reserve (Page21)
17. Change L1 to SM010012500 (Page9)
18. Add R602, C674 for EMI request (Page36)
19. Change ODD reset to PLT_RST# (Page22)
20. Connect Codec pin16, 17 to EC for EQ (Page30, 35)
21. Add D29 (Page41)
22. Add R604 and change R107 to 470ohm (Page35)
23. Change R568 to 3.3kohm (Page32)
24. Add R611 (Page15)

***** From Rev:0.2 to Rev:0.3 PIR List *****

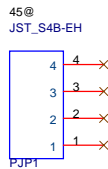
25. Replace JP2 (Page15)
26. Replace R358 for interfer (Page15)
27. Add three while area for ME.
28. .JP29 change from OCTEK_HDS-22TA1_44P_RV to OCTEK_HDS-22TA1_44P_RV-S.
29. JP30, update Mini PCI new Foot print form QTC to AMP to update outline.
30. U30. update new Foot print from A3212EEH_MLP6_5P to A3212EEH_MLP6_5P-S.
31. Change PCB PN to Rev1.0.
32. C146 的BOM Structure 7411@ 後有空格, delete.
33. R603 的BOM Structure MDC@ 後有空格, delete.
34. R199 的BOM Structure 7411@ 改爲 5IN1@
35. Change Q6 and Q46 from 2N7002 to SB501380009
36. Add C675 680P for H_NMI.
37. Reserve C676 180P for PCI_SERR#
38. Add C677 220P for H_FERR#
39. Reserve C678 ~ C686 180P for H_SMI#, H_INIT#, SERRIRQ, H_A20M#, H_INTR, H_IGNNE#, H_STPCLK#, H_PWRGOOD and H_CPUSLP#.
40. Add R615 ~ R617 00hm for EMI solution link DGND and RJ45_GND.
41. Change R542 from 22 Ohm to 33 Ohm.
42. R527 and C607 change from @ to mount for audio EMI.
43. Add L23 ~ L26 (SM070000H00) and Reserve R618 ~ R625 for EMI
44. Change U2 to SA411250200
45. Change C510 and C511 from 33P to 30P (SE071300J00)

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List) for Power Circuit

A vertical bar is divided into four segments labeled A, B, C, and D from bottom to top. An arrow points to the boundary between segments B and C.

A vertical bar is divided into four segments labeled A, B, C, and D from bottom to top. An arrow points to the boundary between segments B and C.



ZZZ
DA800001L10
--PCB ZKL LA-2721
REV1 M/B

DA800001L10

U4
SA0091500N0
--S IC A51 915GM-C1
BGA 1257P GMCH R3

R3GM@ SA0091500N0

U4
SA0000187A0
--S IC A51 910GML-C1
BGA 1257P GMCH R3

R3GML@SA0000187A0

U4
SA0091500M0
--S IC A51 915GM-C1
BGA 1257P GMCH R1

R1GM@ SA0091500M0

U4
SA000018790
--S IC A51 910GML-C1
BGA 1257P GMCH R1

R1GML@SA000018790

U4
SA0091501J0
--S IC 915PM-C1
BGA 1257P GMCH R1

R1PM@ SA0091501J0

U13
SA8280108B0
--S IC A51 FW82801FBM
SL7W6 B2 BGA 609P!

R1SB@ SA8280108B0

U12
SA000013200
--S IC PCI1510RGVF PBGA
253P PC CARD CTRL

1510@ SA000013200

U12
SA045100110
--S IC PCI4510RGVF PBGA
224P PCI-CARD BUS

4510@ SA045100110

U12
SA064110000
--S IC PCI6411ZHK PBGA-
288 PCI-CARD BUS

6411@ SA064110000

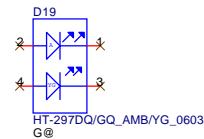
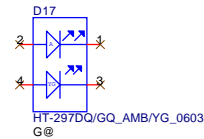
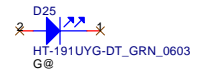
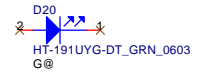
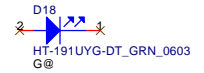
U36
SA880360000
--S IC88E88036 10/100
LAN CTRL

8036@ SA880360000

T1
SP050001X00
--TST1284B 10/100
LAN Transformer

8036@ SP050001X00

R445 2K 0402_1%
8036@



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