

Compal Confidential

Cougar

LA-6851P Schematics Document

Intel Pine View Processor/ Tiger point

2010-10-10

REV: 1.0

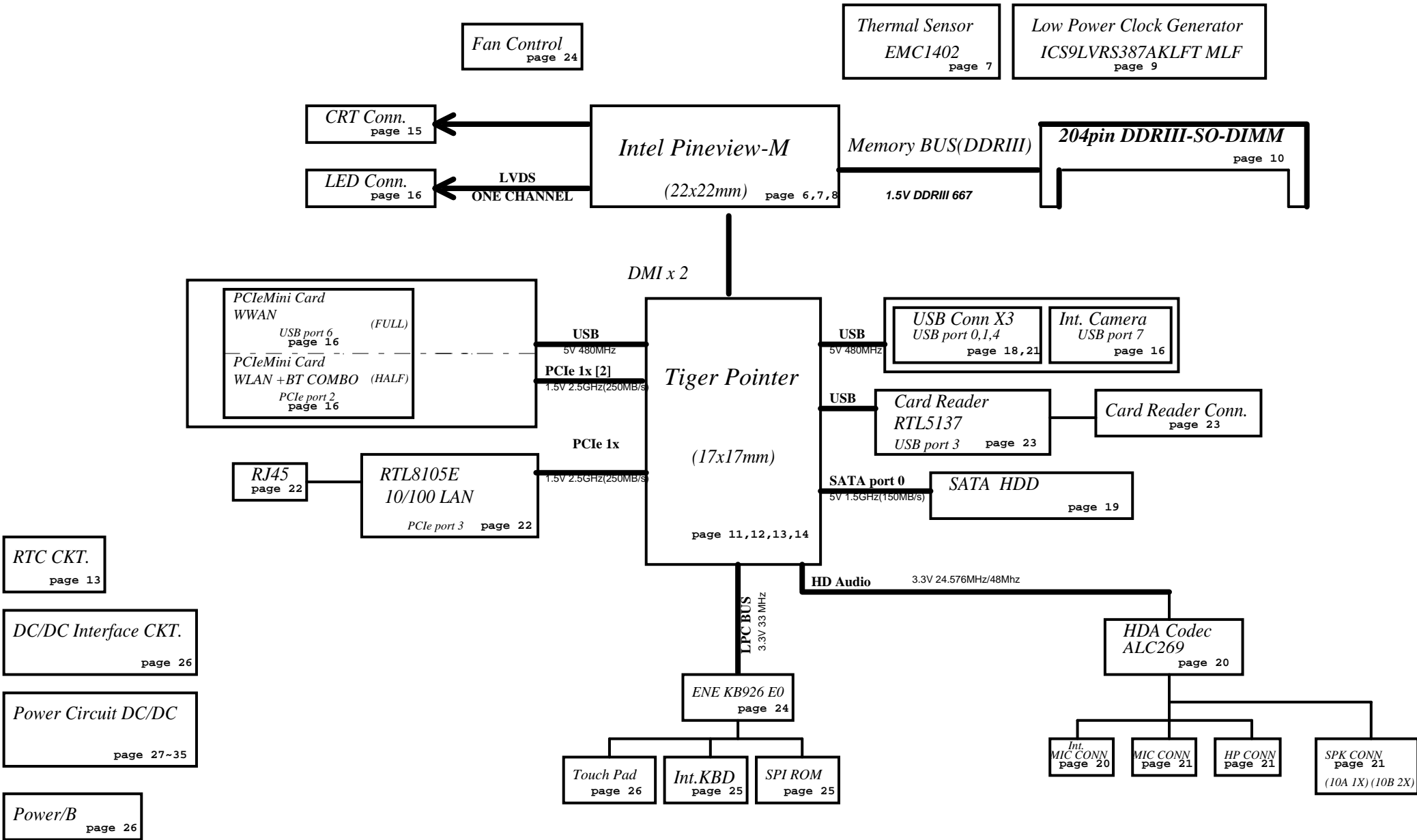
Toshiba Satellite NB500 NB505

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Model Name : PBU00
File Name : LA-6851P

http://laptopblue.vn



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.89VS	0.89VS GFX support voltage	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	VCCP switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	ON	OFF	OFF
+5VALW	5V always on power rail	ON	OFF	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

Function	Mini PCI-E SLOT				CAMERA & MIC		BLUE TOOTH		Clock gen	
description										
explain	Wi-Fi	WiMax	3GGPS	3G	CAMERA	MIC	BLUE TOOTH		Tpye	
BTO	WLAN@	WIMAX@	3GGPS@	3G@	CAM@	MIC@	BT@		low@	normal@

Function			
description			
explain			
BTO			

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 010X b

EC SM Bus2 address

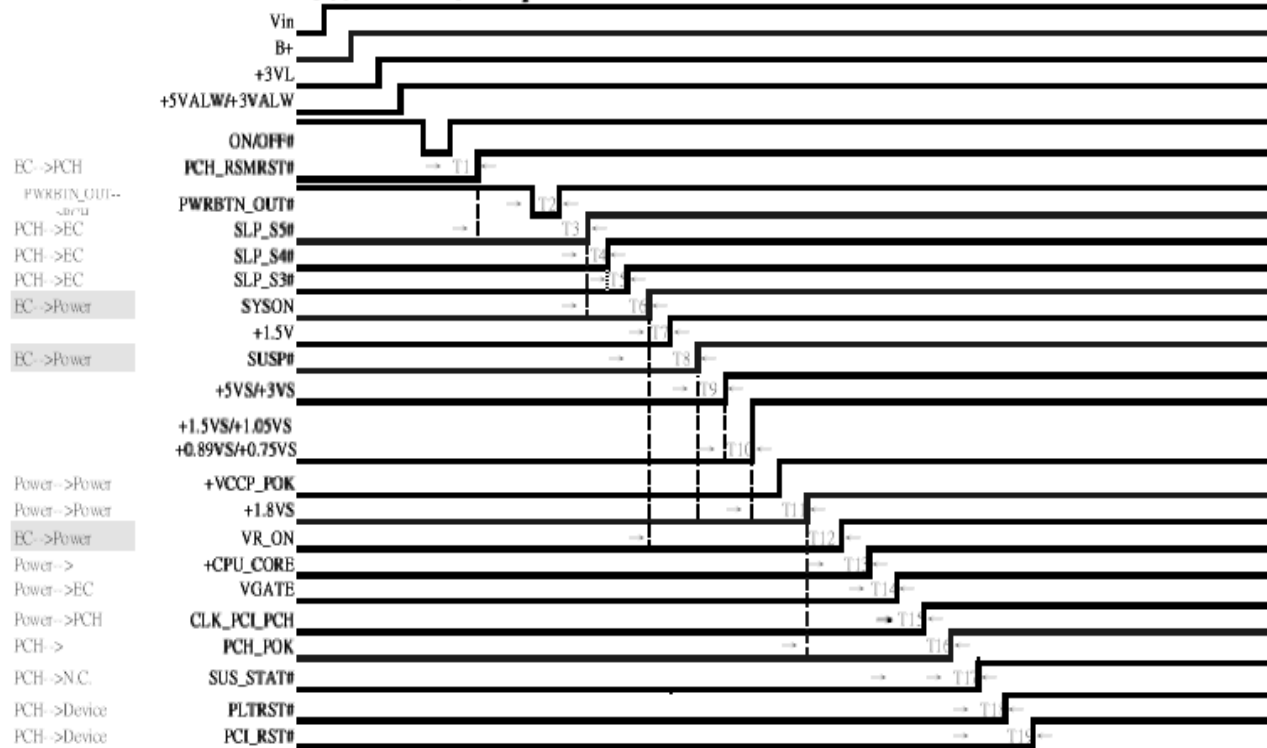
ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb
WWAN/WLAN	

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PBU00 Power ON sequence

Rev 07/2



Power-on Sequence

Time	Description	Expected
T1	Power Button active to PCH_RSMRST# inactive	> 105ms
T2	Power Button active to PBTN_OUT# inactive	< T1
T3	PCH_RSMRST# inactive to PM_SLP_S5# inactive	< 110ms
T4	PM_SLP_S5# inactive to PM_SLP_S4# inactive	28.992us ~ 64.088us
T5	PM_SLP_S4# inactive to PM_SLP_S3# inactive	28.992us ~ 64.088us
T6	PM_SLP_S3# inactive to SYSON active	>10ms
T7	SYSON active to +1.5V active	>0
T8	PM_SLP_S3# inactive to SUSP# inactive	>10ms
T9	SUSP# inactive to +5VS active	>0
T9	SUSP# inactive to +3VS active	>0
T10	SUSP# inactive to +1.5VS active	> 0
T10	SUSP# inactive to +0.89VS active	> 0
T10	SUSP# inactive to +1.05VS active	> 0
T10	SUSP# inactive to +0.75VS active	>0
T11	+1.05VS inactive to +1.8VS active	>0
T12	SUSP# inactive to VR_ON active	>10ms
T13	VR_ON active to +CPU_CORE active	>0
T14	+CPU_CORE active to VGATE	<10ms
T15	VGATE active to CLK_PCH_PCH stable	< 1.8ms
T16	+1.5VS power active to ICH_PWROK active	>99ms
T17	ICH_PWROK active to SUS_STAT# inactive	0.928ms ~ 1.218ms
T18	SUS_STAT# inactive to PLT_RST# inactive	57.984us ~ 96.132us
T23	SUS_STAT# inactive to PCL_RST# inactive	57.984us ~ 96.132us

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Cougar Power Map

Ipeak=6.97A, Imax=4.88A

DESIGN CURRENT 522mA

+3VALWP +-5%

** The SW just is reserved.
The power passes by jump or
0-ohm resistor.

UP6182CQAG

WOL_EN#

** P-CHANNEL
AO3413

DESIGN CURRENT 300mA

+3V_LAN

Ipeak=3.98A, Imax=2.8A

DESIGN CURRENT 3010mA

+5VALWP +-5%

SUSP

N-CHANNEL

SI4800BDY

DESIGN CURRENT 2286mA

+5VS

SUSP

N-CHANNEL

SI4800BDY

DESIGN CURRENT 5586mA

+3VS

ENVDD

P-CHANNEL
AO3413

DESIGN CURRENT 2000mA

+LCD_VDD

SUSP#

SY8033BDBC

DESIGN CURRENT 2640mA

+0.89VSP

SUSP#

SY8033BDBC

Ipeak=1.308A, Imax=4A

DESIGN CURRENT 3489mA

+1.05VSP +-5%

VR_ON

ADP3211AMNR2G

Imax=3.5A

DESIGN CURRENT 6000mA

+CPU_CORE

SYSON

G5603RU1U

Ipeak=19.6A, Imax=13.72A

DESIGN CURRENT 2000mA

+1.5VP +-5%

SUSP#

IRF8113PBF

DESIGN CURRENT 2112mA

+1.5VSP

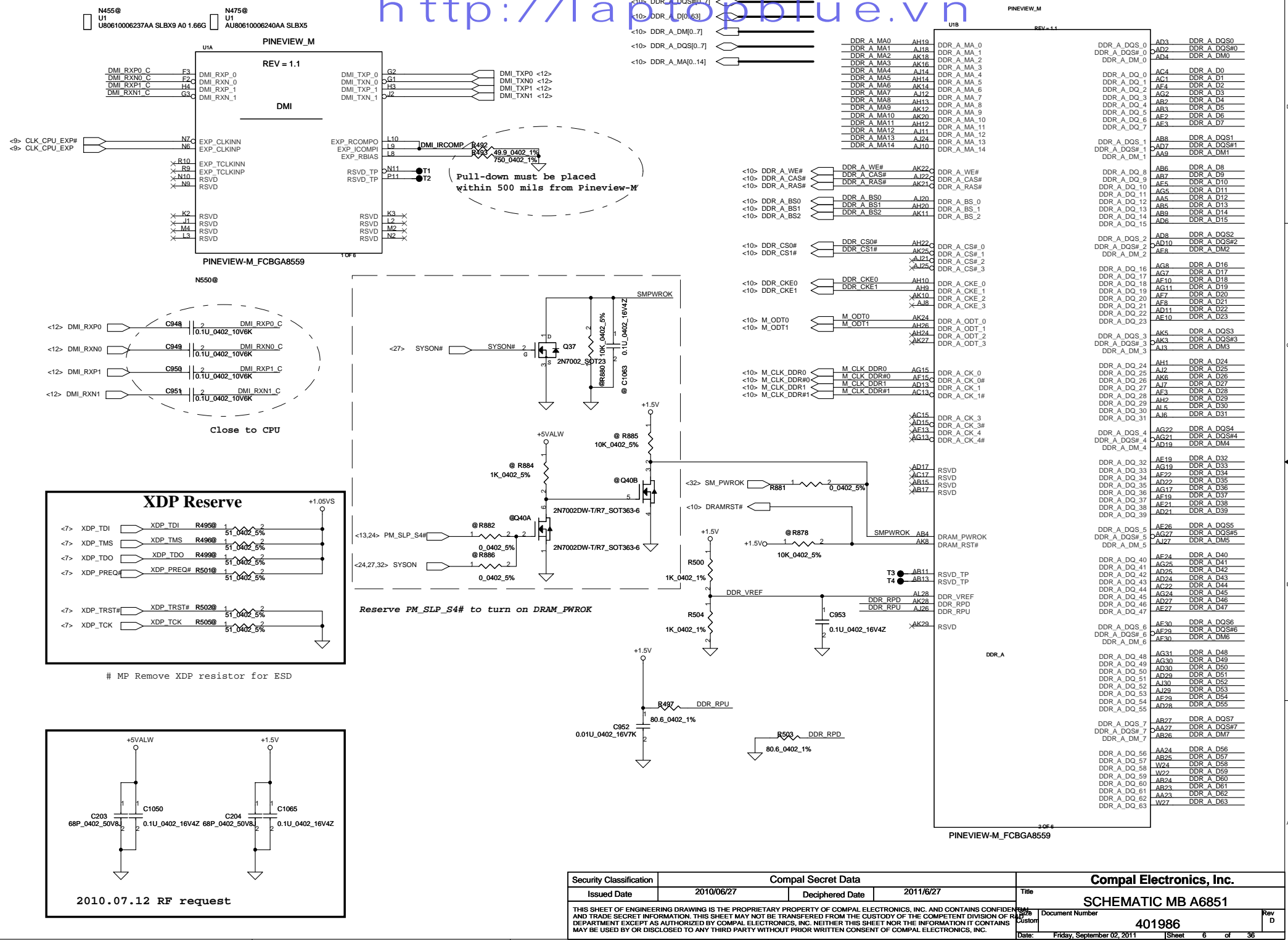
SUSP

UP7711U8

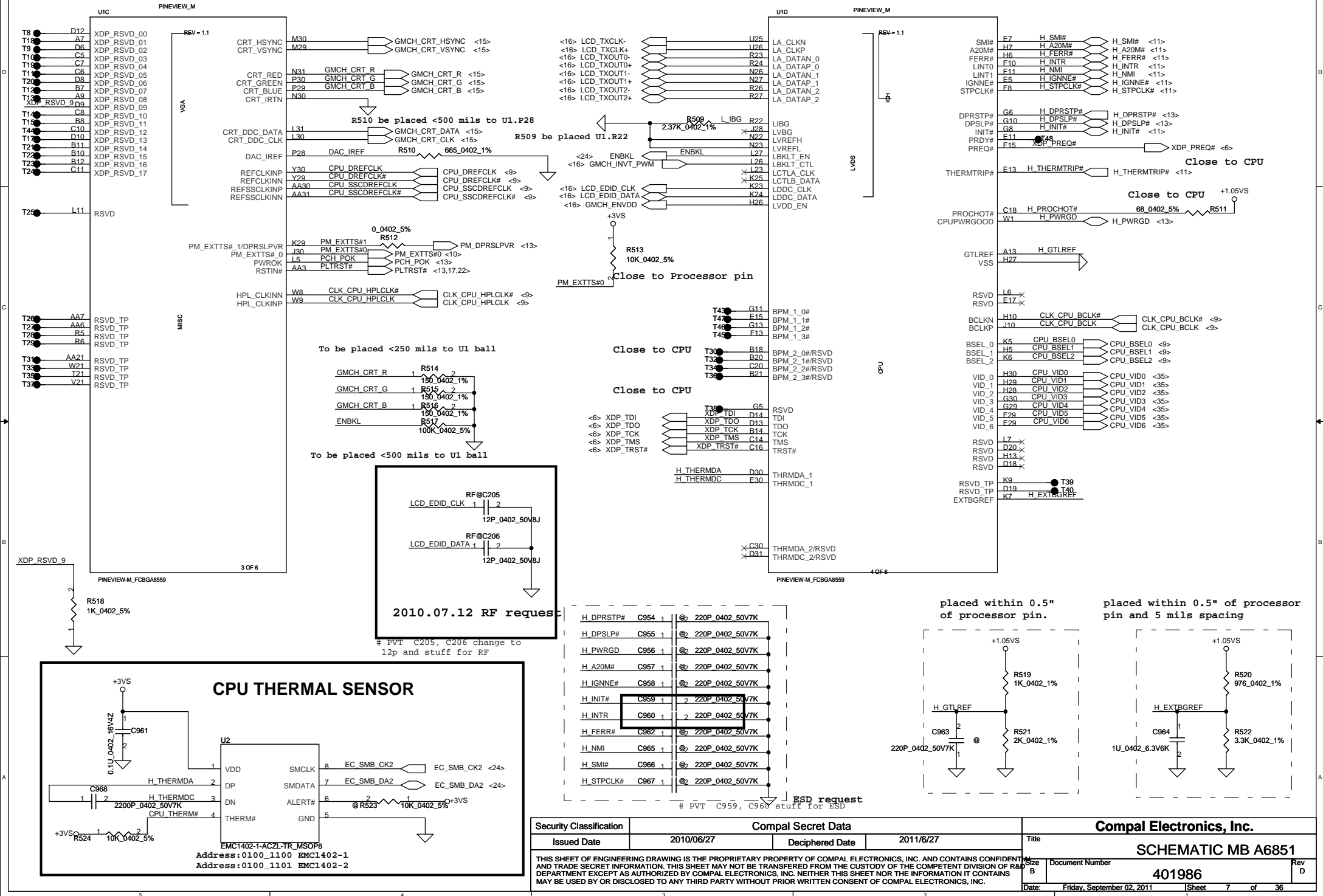
DESIGN CURRENT 500mA

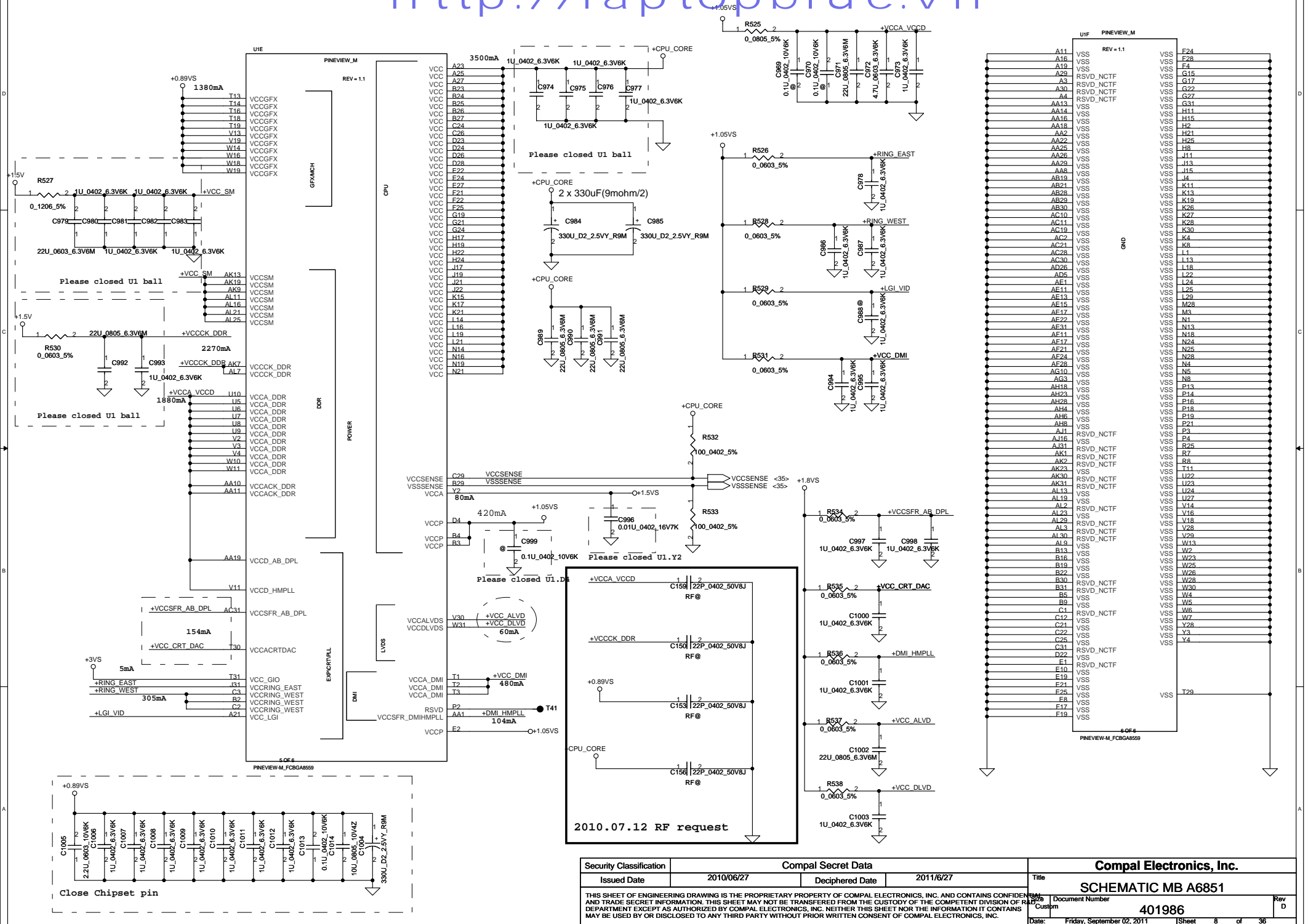
+0.75VSP

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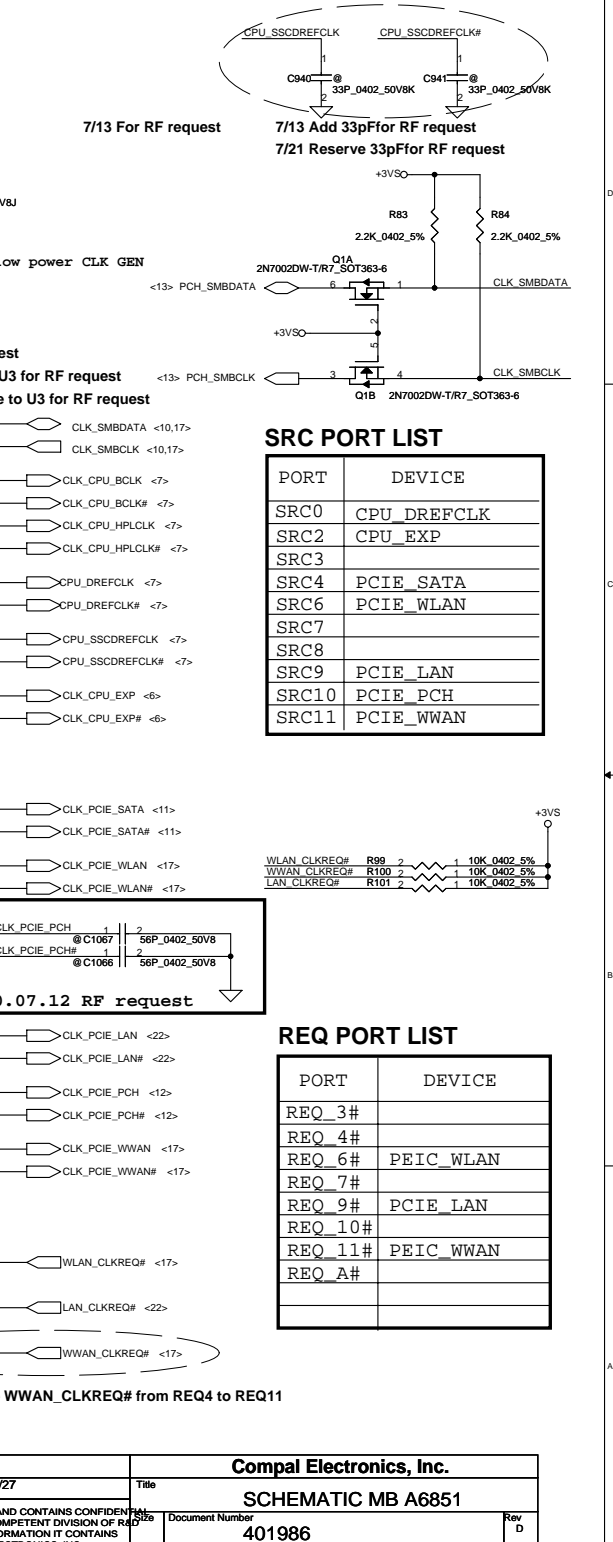
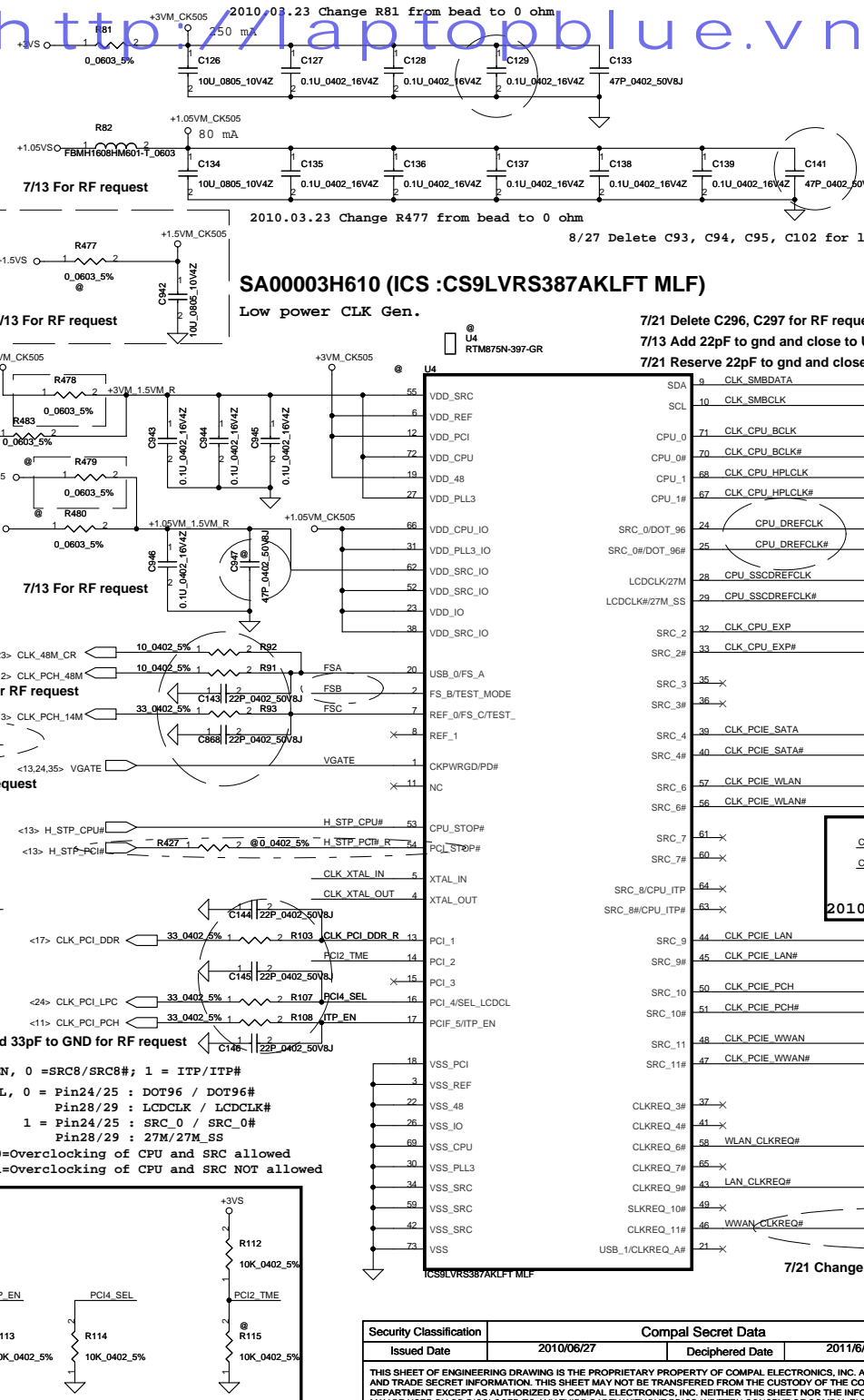
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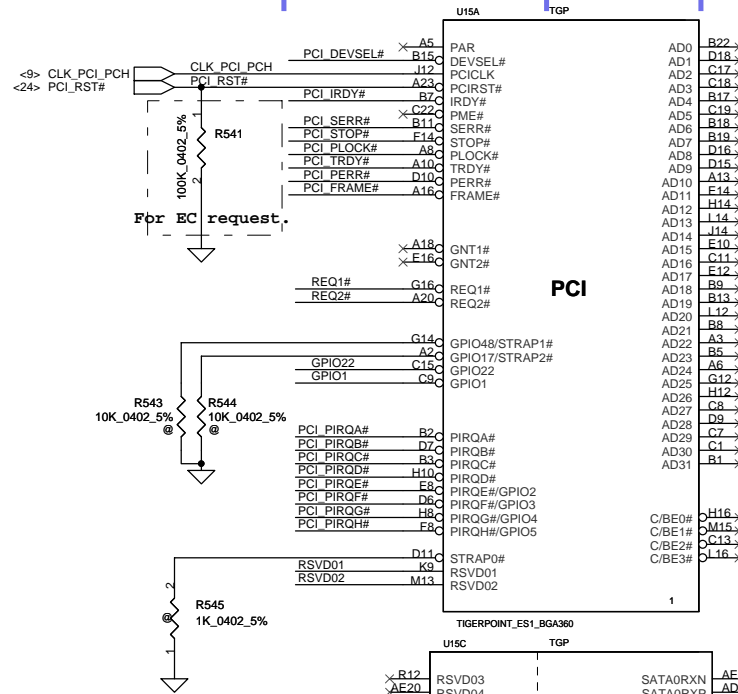
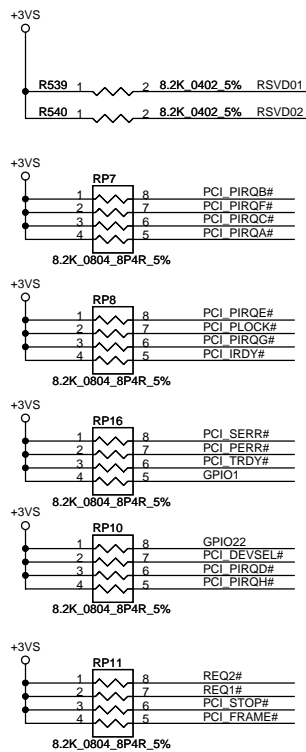




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	Normal Power	Low Power
R477	@	Stuff
R478	Stuff	@
R479	Stuff	@
R480	@	Stuff
R483	@	Stuff

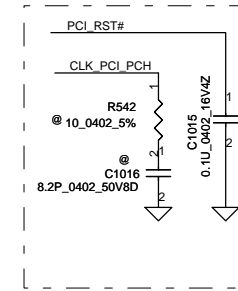
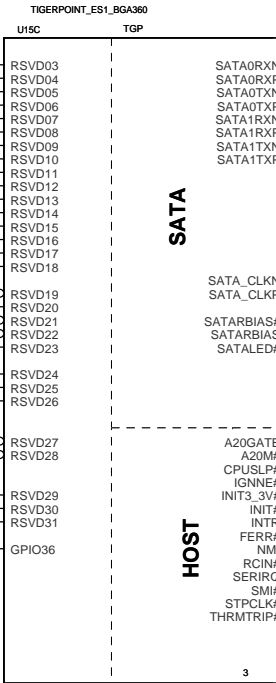




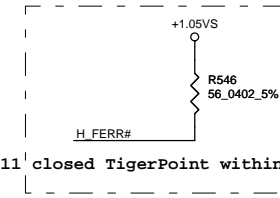
PCI

SATA

HOST

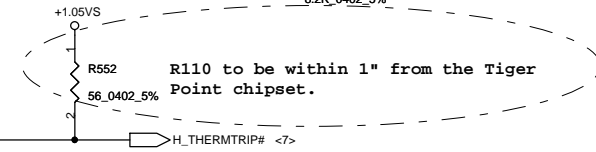
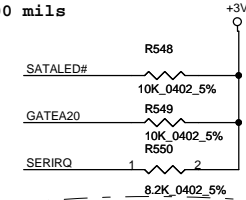


For EMI, close to TigerPoint



R111 closed TigerPoint within 1"

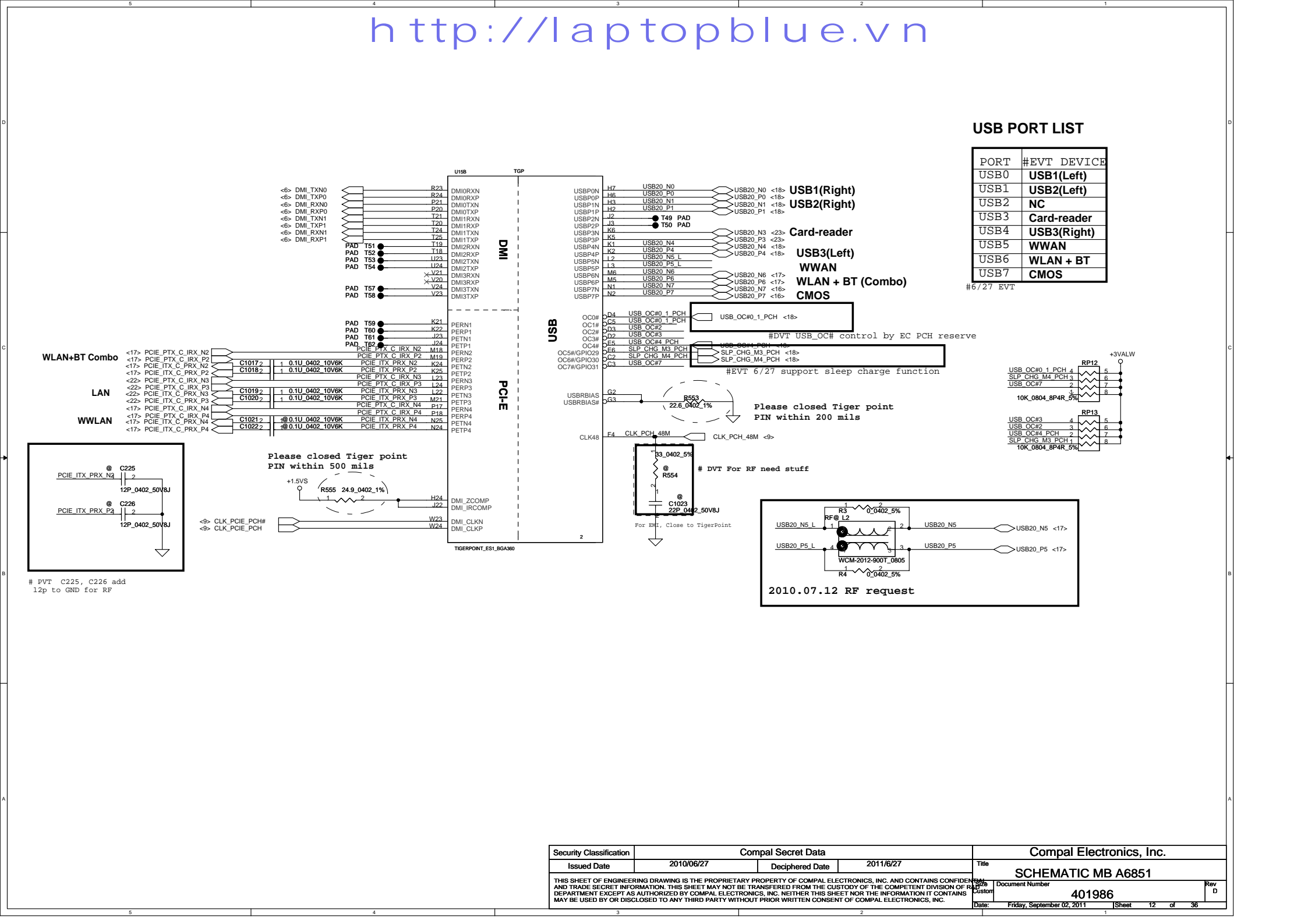
Please closed Tiger point PIN within 500 mils

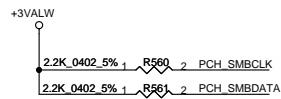


R110 to be within 1" from the Tiger Point chipset.

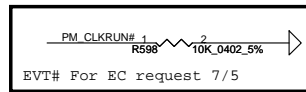
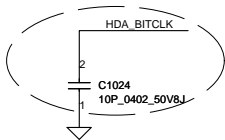
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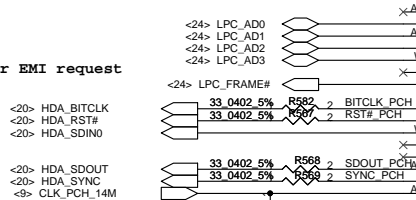
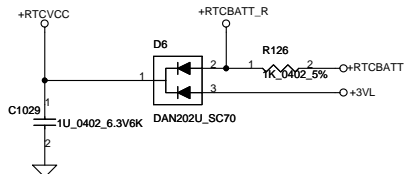
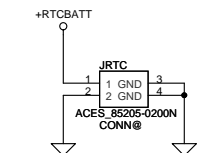
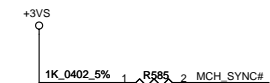
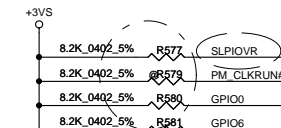
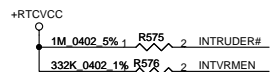
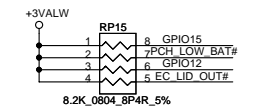
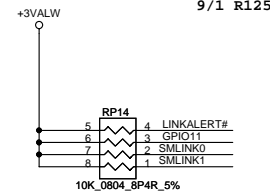


7/2 For EMI, Close to TigerPoint
9/1 C207 change to SE071100J80 for EMI request

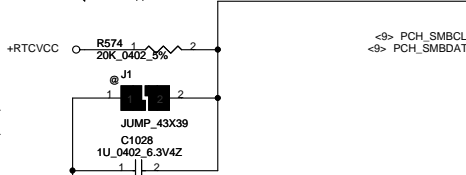
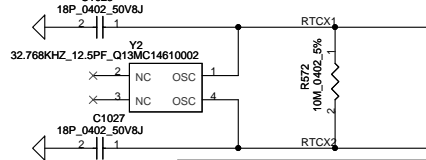
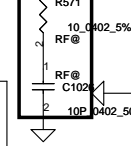


12/17 Add Pull high Resistor for GPIO14

9/1 R125 change to SM010027780 for EMI request

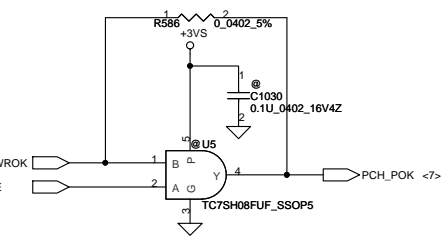
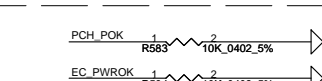
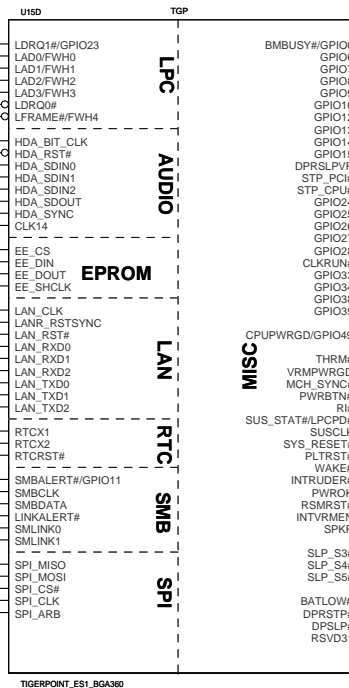


MP C1026 4.7P change to 10p for RF request

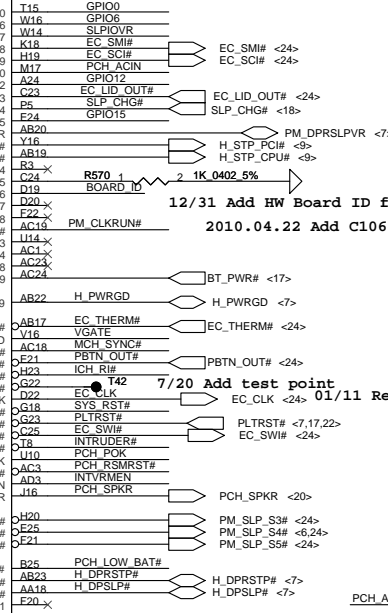


7/20 Add SLPIOV# pull up 8.2k to +3vs

9/23 Change RP17 to R256, R257, R258 for layout request

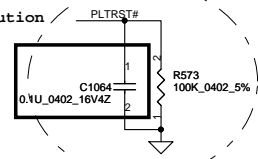


2010.03.22 Un-stuff U5 and C1030



12/31 Add HW Board ID function

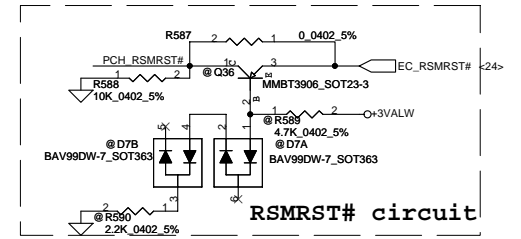
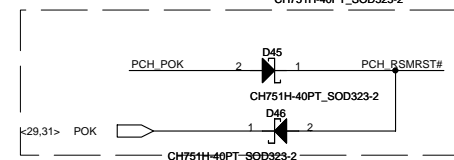
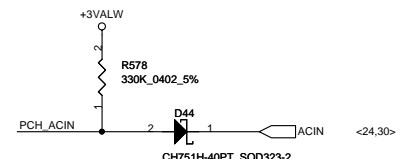
2010.04.22 Add C1064 for ESD solution



7/20 Add test point

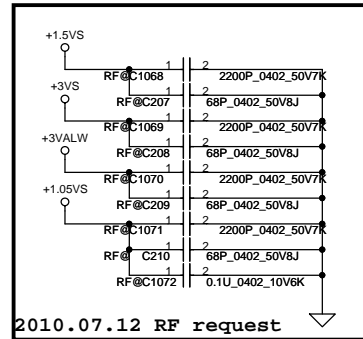
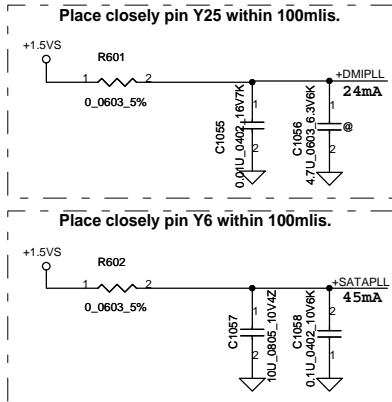
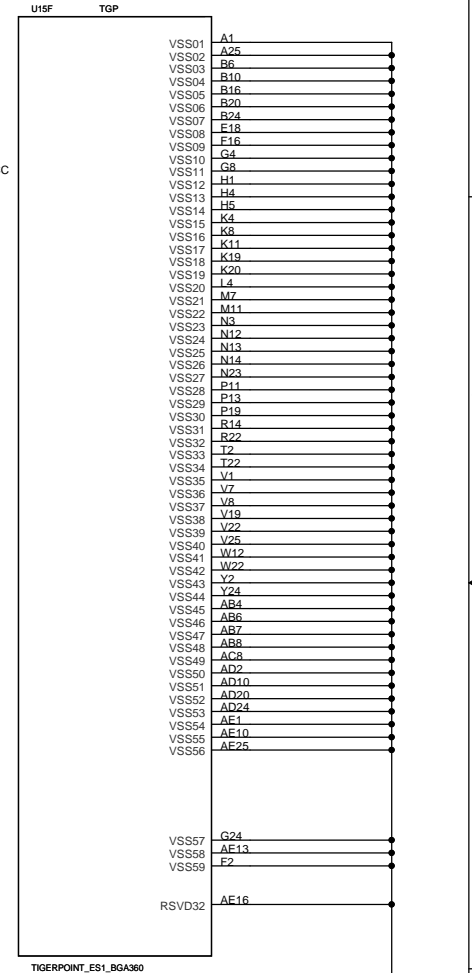
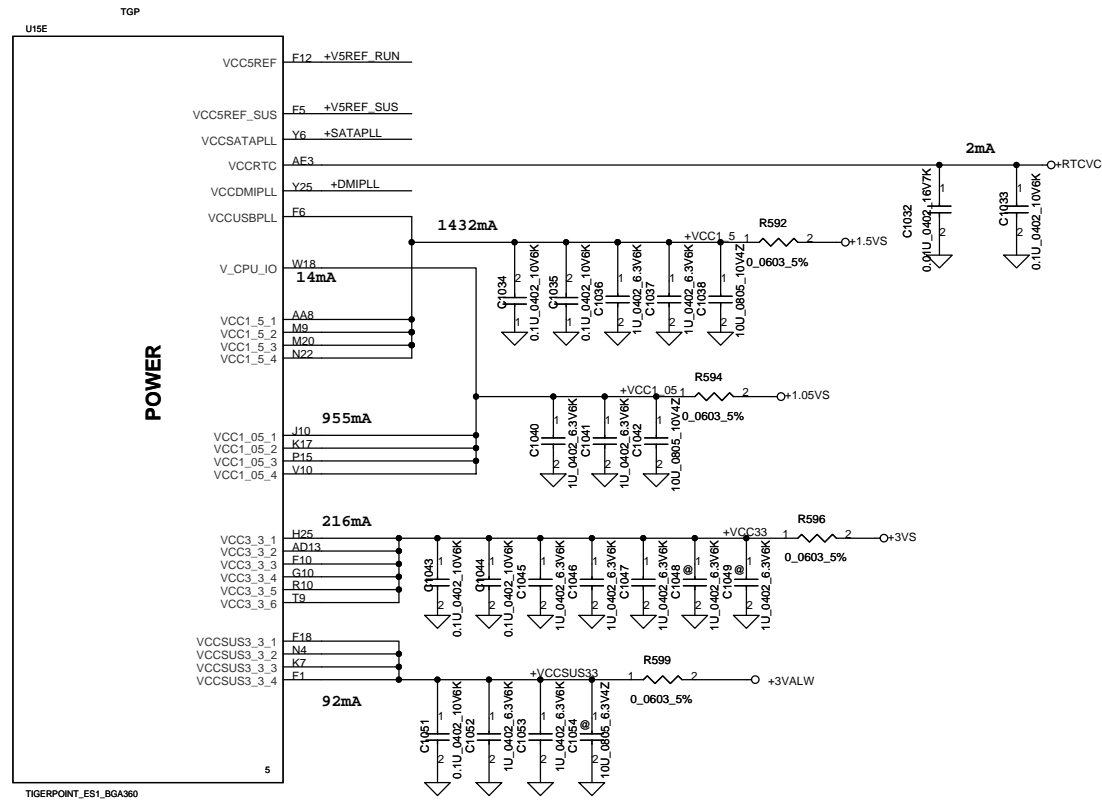
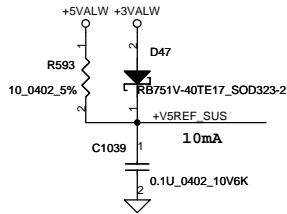
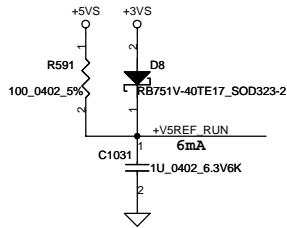
01/11 Reserve EC_CLK for KBC

8/24 Add R254 pull down for EC request



2010.03.22 Un-stuff RSMRST# circuit and use 0 ohm bypass

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CRT CONNECTOR

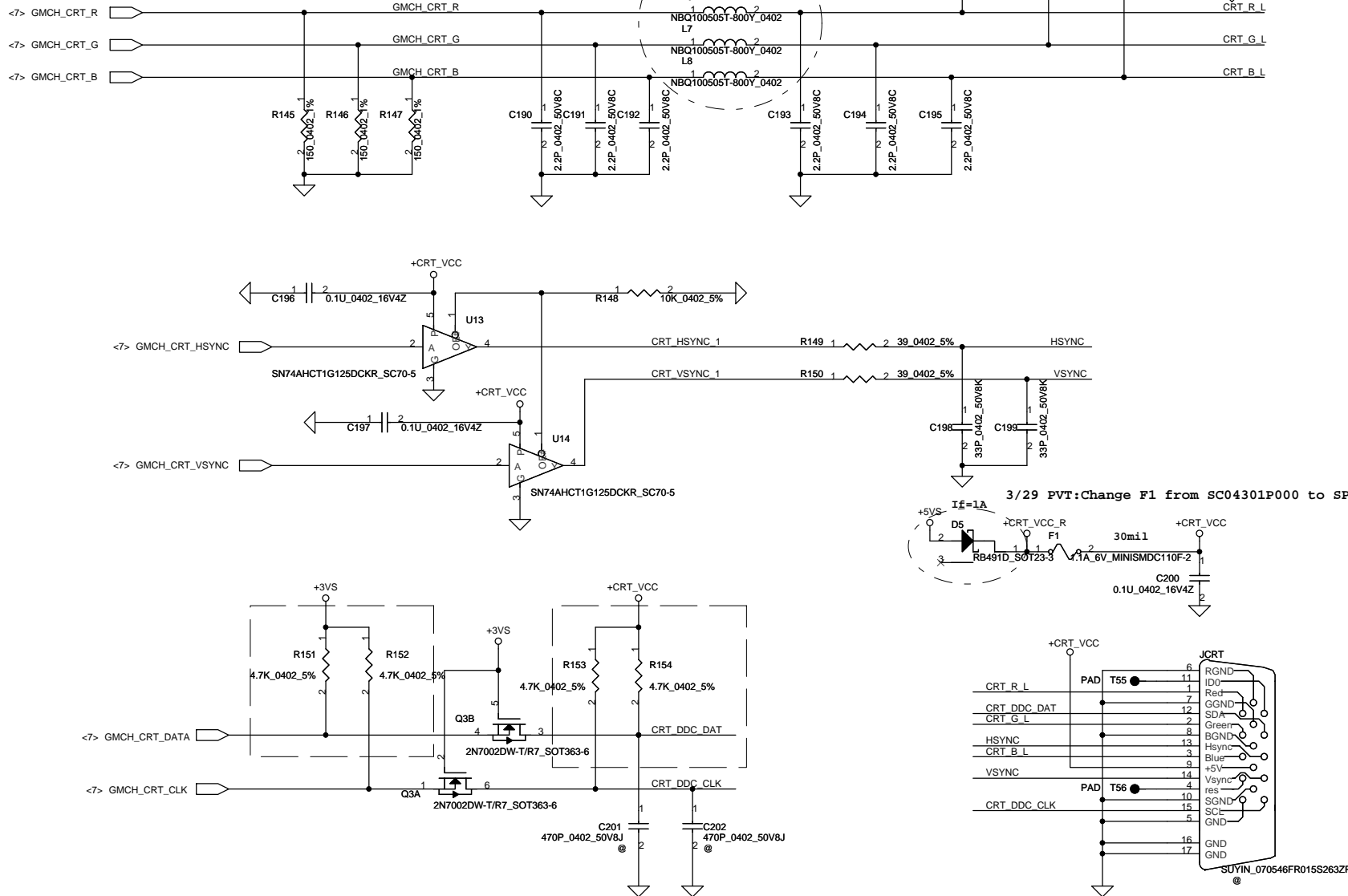
<http://laptopblue.vn>

Place closed to conn.

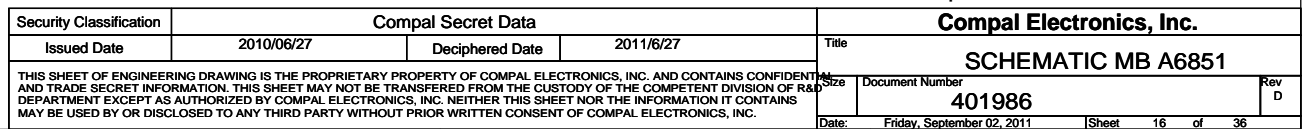
3/16 PVT: Change to high speed bead

2/16 DVT: Mount C504 for EMI request

Place closed to conn.

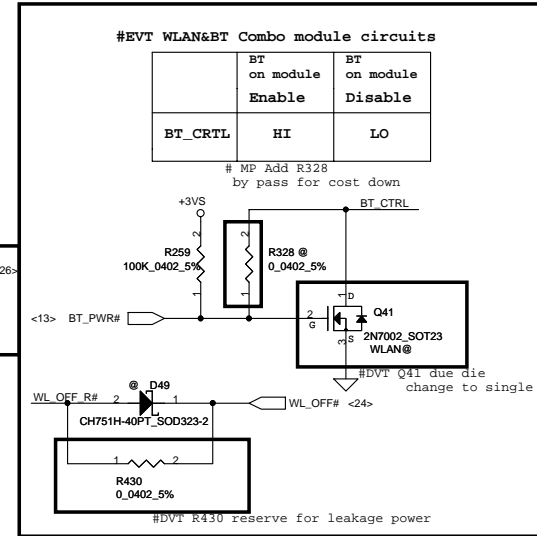
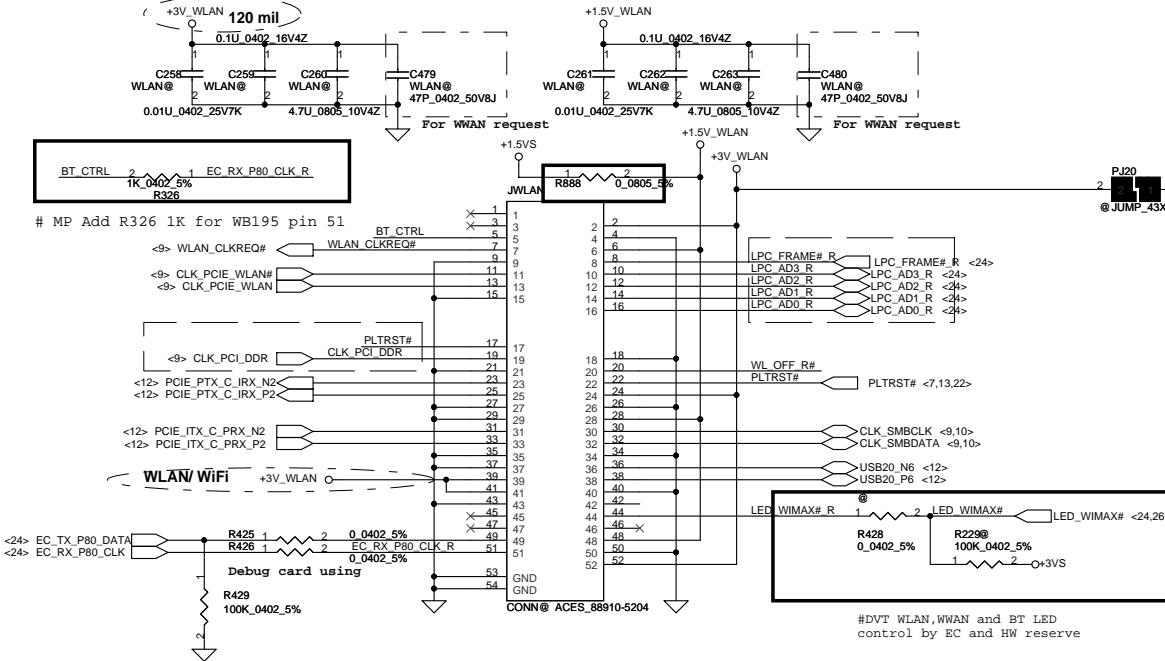


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Mini-Express Card for WLAN/WiMax

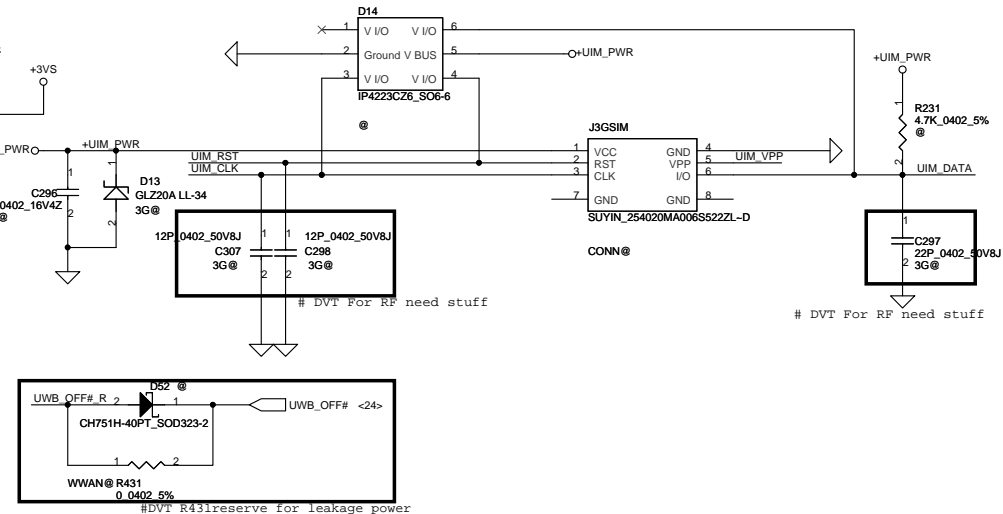
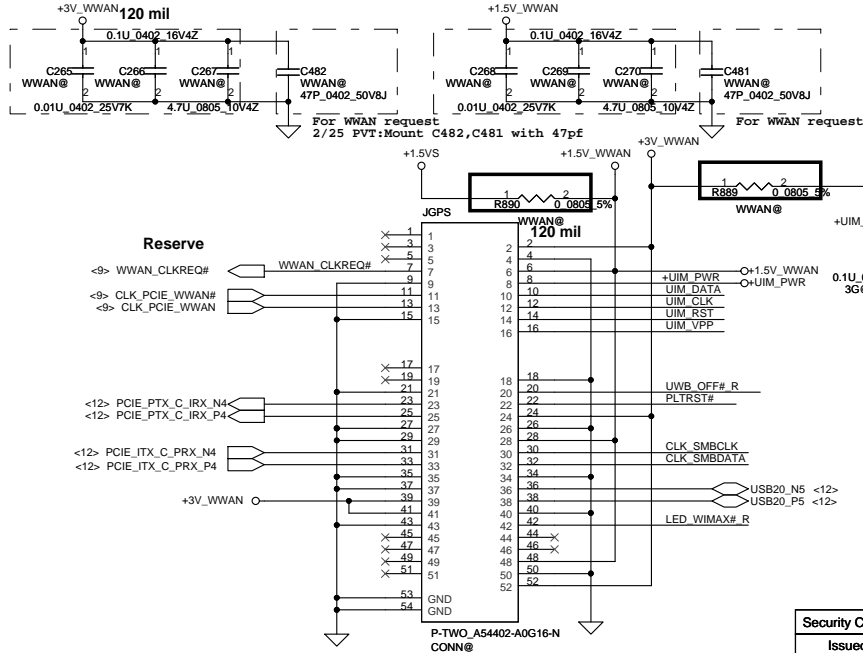
2/25 PVT:Mount C479,C480 with 47pf
3/16 PVT:Add BOM Config of C481,C482 to WLAN@



Mini-Express Card for 3G/GPS

3G current need to 2750mA

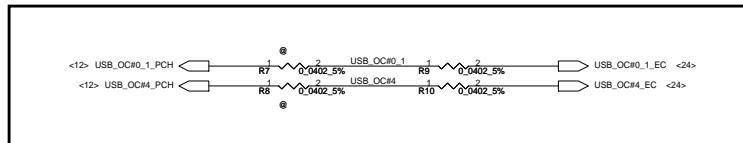
3/16 PVT:Add BOM Config of C481,C482 to 3GGPS@



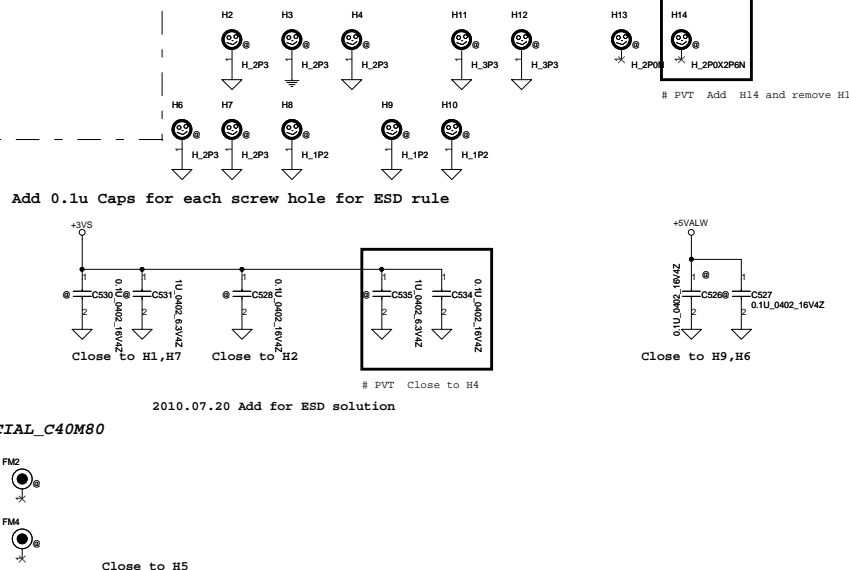
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h t t p : / / l a p t o p b l u e . u n i v . e d . u k

SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D



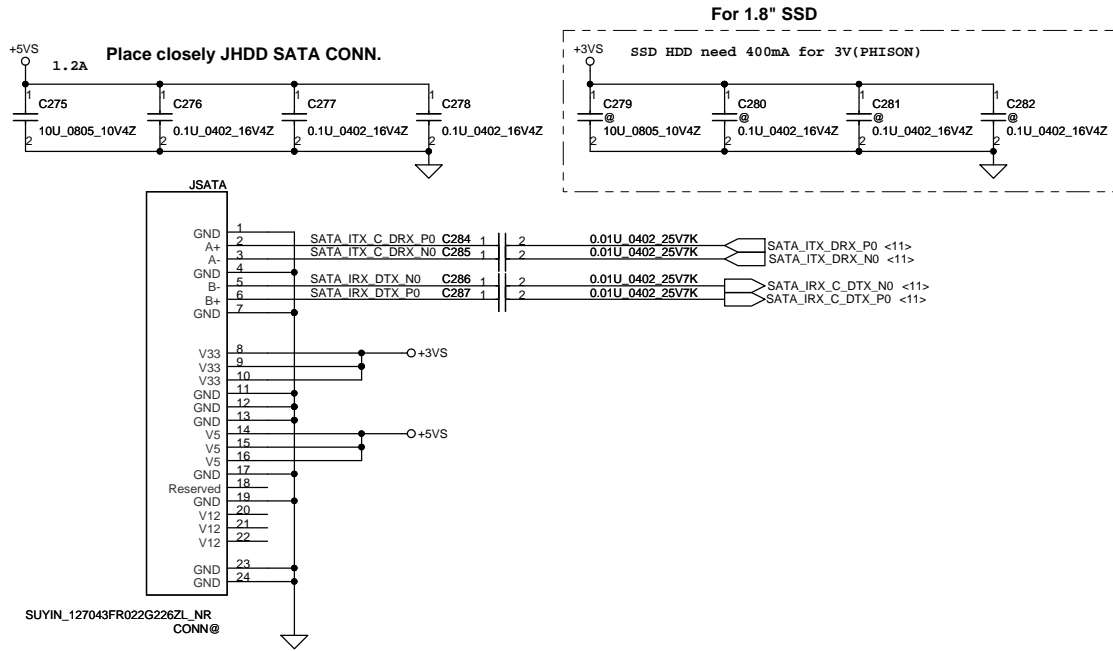
For EMI request 2/3 DVT: Change D38.D37 from PRT85V0U2X SOT143-4 to CM1293A-0480 SOT23-6 For EMI request



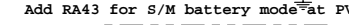
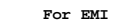
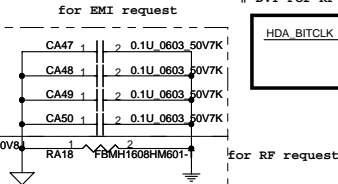
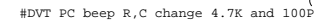
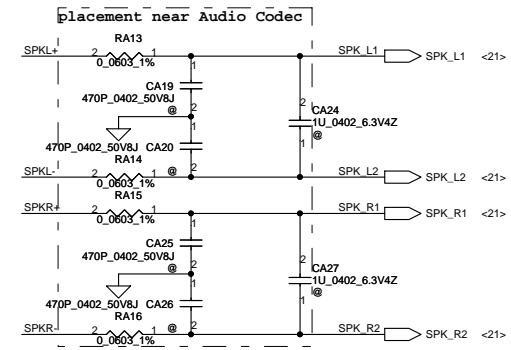
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SATA Conn.

http://laptopblue.vn

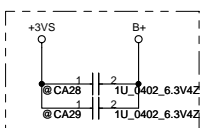


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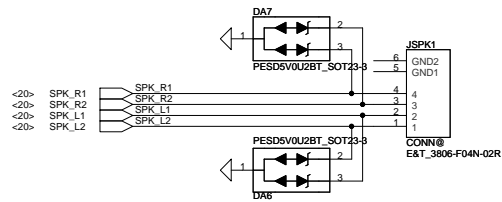


place close to chip

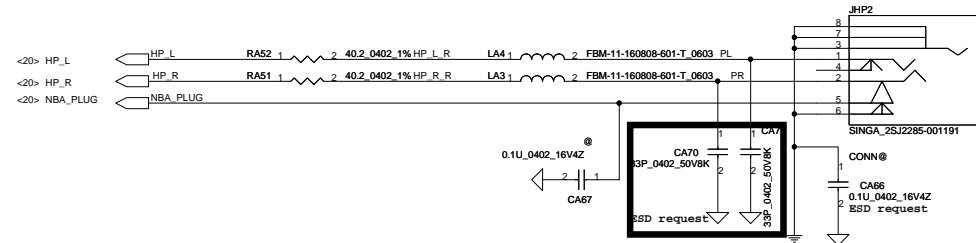
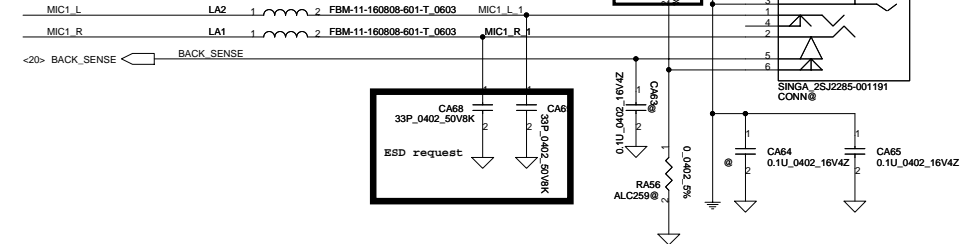
The diagram shows a horizontal line representing a sense line. On the left, it is labeled 'MIC_SENSE'. On the right, it is labeled 'SENSE_A'. Between these labels, there are two resistors. The first resistor is labeled 'RA10' and has a value of '20K_0402_1%'. The second resistor is labeled 'RA21' and has a value of '39.2K_0402_1%'. The 'RA10' resistor is connected to the 'MIC_SENSE' line. The 'RA21' resistor is connected to the 'SENSE_A' line. The 'RA21' resistor is also connected to a component labeled 'NBA_PLUG' with a pin number '<21>'. The 'RA21' resistor is connected to the 'SENSE_A' line via a vertical connection on the right side of the diagram.



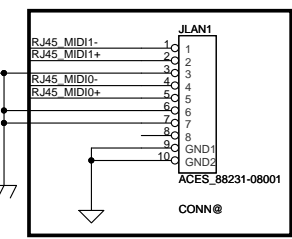
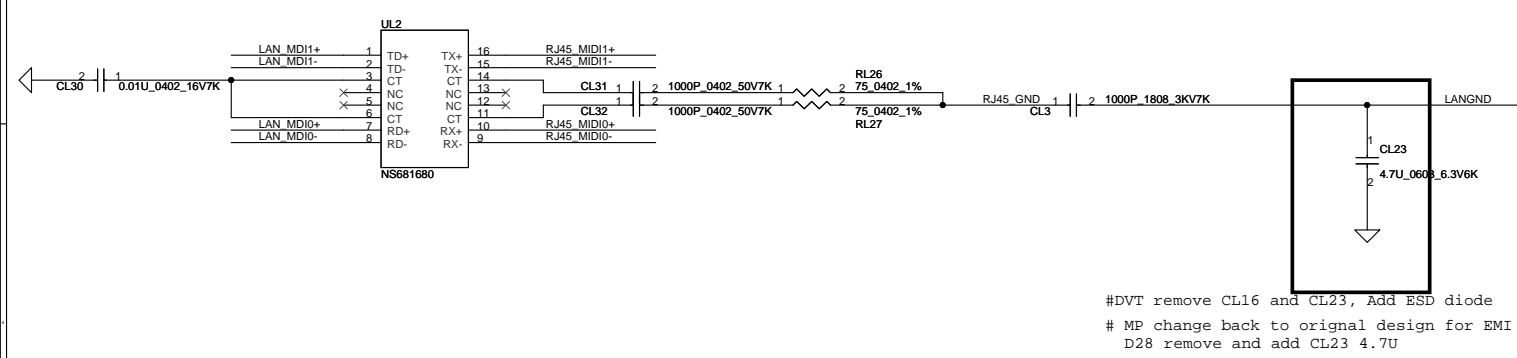
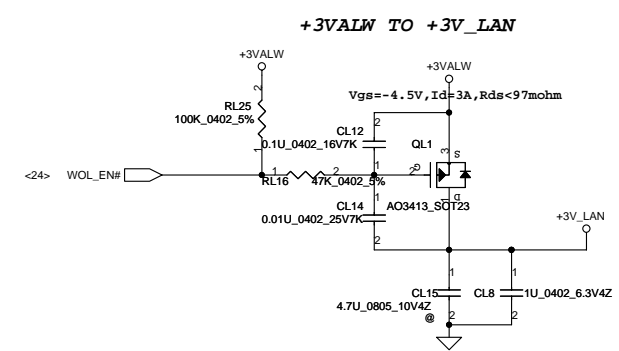
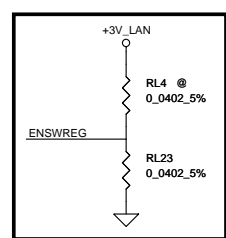
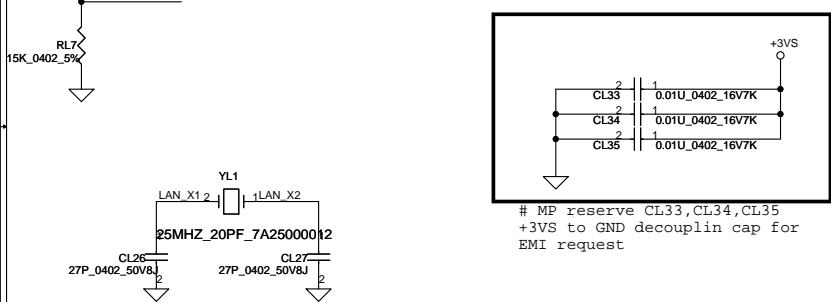
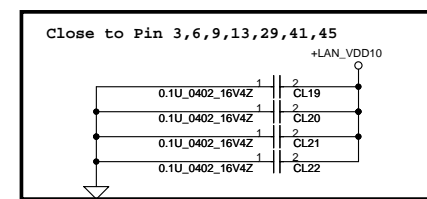
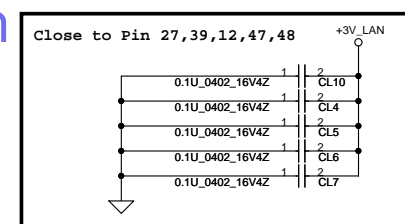
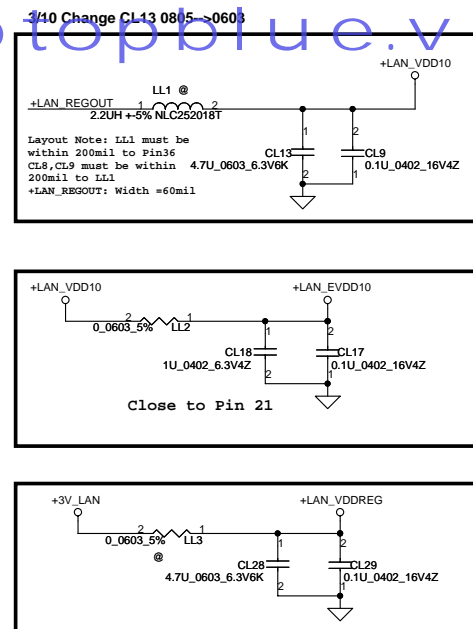
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MIC



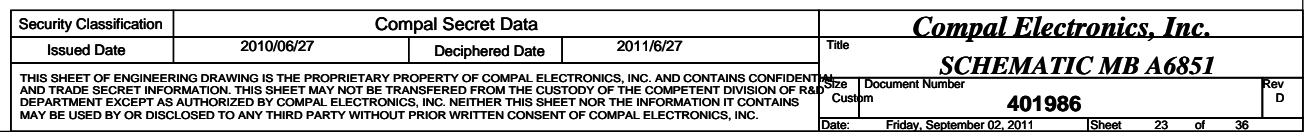
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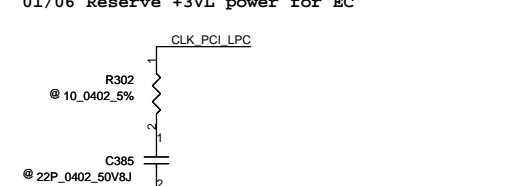
```
#DVT remove CL16 and CL23, Add ESD diode
# MP change back to original design for EMI
D28 remove and add CL23 4.7U
```

```
#DVT LAN connect pin definid change
# PVT Add pin 7 connect to LANGND
```

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01/06 Reserve +3VL power for EC



Place closely pin 109

R243

LID SW#

1 2

0.0402_5%

47K_0402_5%

+3VALW

+3VL

0.0402_5%

1 2

@

C525

0.1U_0402_16V4Z

1 2

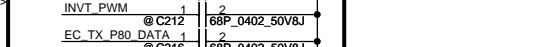
CLK_PCI_LPC

1 2

@ C211

68P_0402_50V8J

MP change LID# pull up to +3VL



EC RX P80 CLK 1	2	68P_0402_50V8J
@C216		
@C217		

2010.07.12 RF request

330K_0402_5%

+3V_EC

1 2

R307

ACIN_D

2 1

D21

CH751H-40PT_SOD323-2

ACIN <13,30>

Add D21 for AC-IN leakage issue

#DVT USB_OC# control by EC

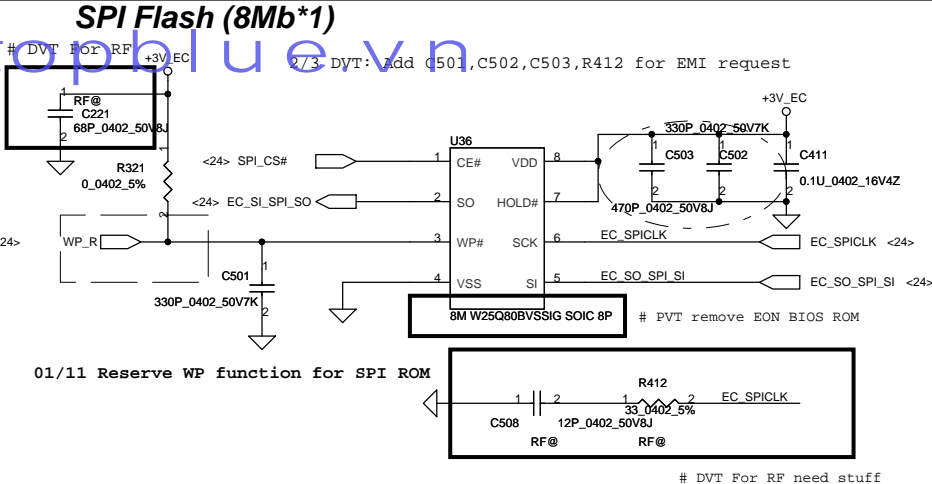
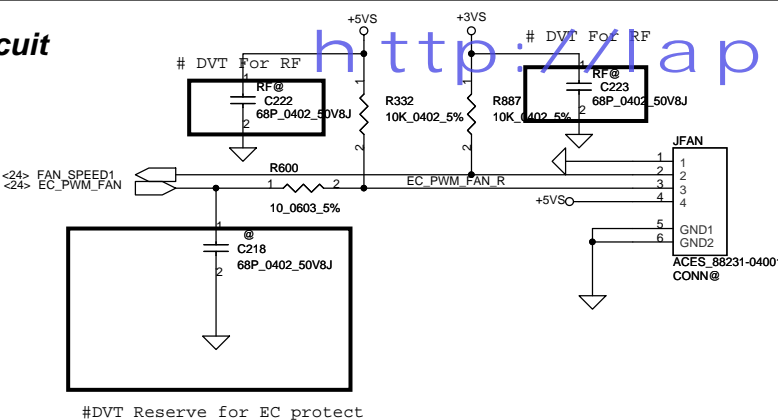
Change EAPD to NC

Diagram showing two resistors, R5 and R6, connected in series between +3VALW and USB_OC#0. R5 is labeled 10K_0402_5% and R6 is labeled 10K_0402_5%.

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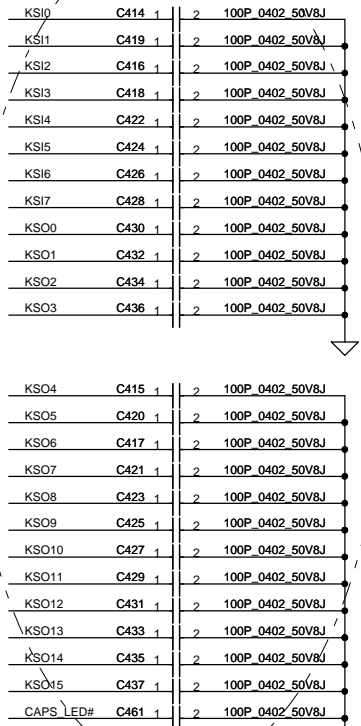
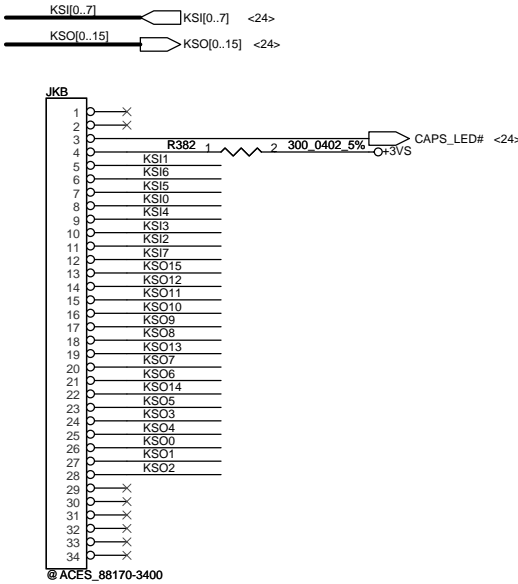
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FAN Control Circuit



LPC Debug Port

KEYBOARD
CONN.

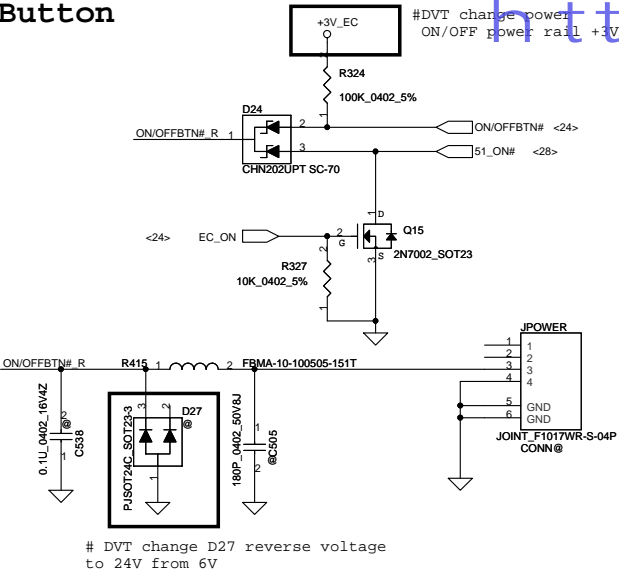


12/18 Follow KB Matrix the same to KSKAA

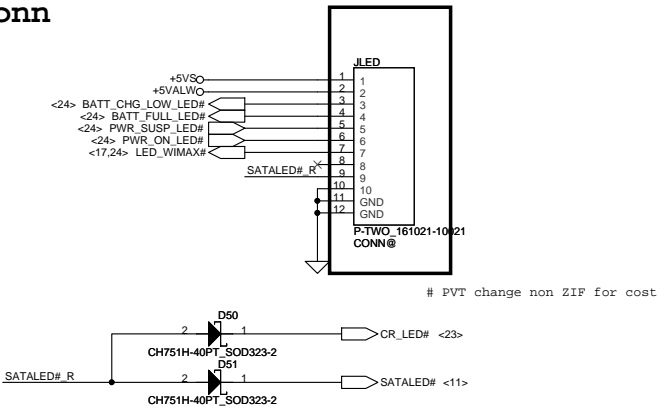
3/4 PVT:Mount C414~C437,C461 for EMI request

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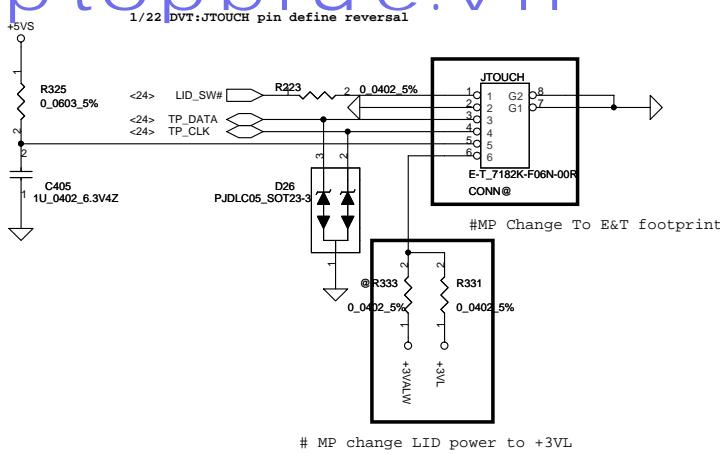
Power Button



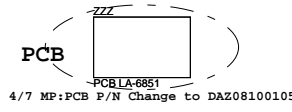
LED Conn



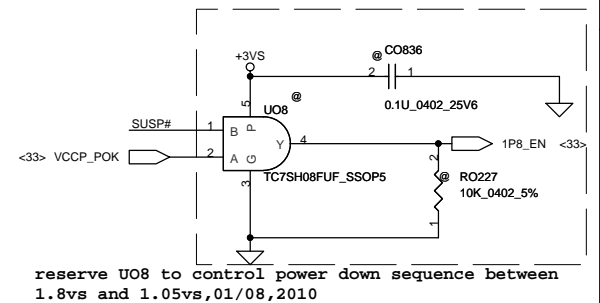
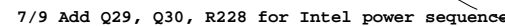
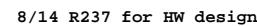
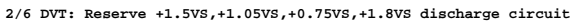
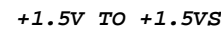
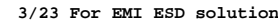
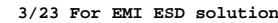
Touch/B Connector



ISPD



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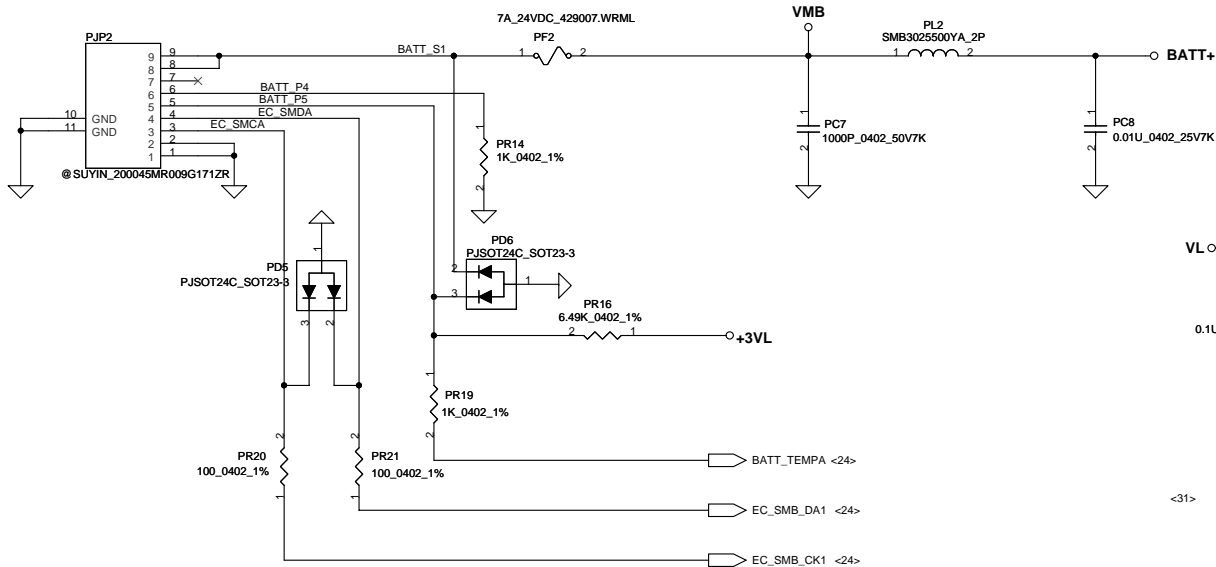


reserve U08 to control power down sequence between
1.8vs and 1.05vs,01/08,2010

8/31 Change Q20 from SB000002880 to SB00000DW00 for HW design

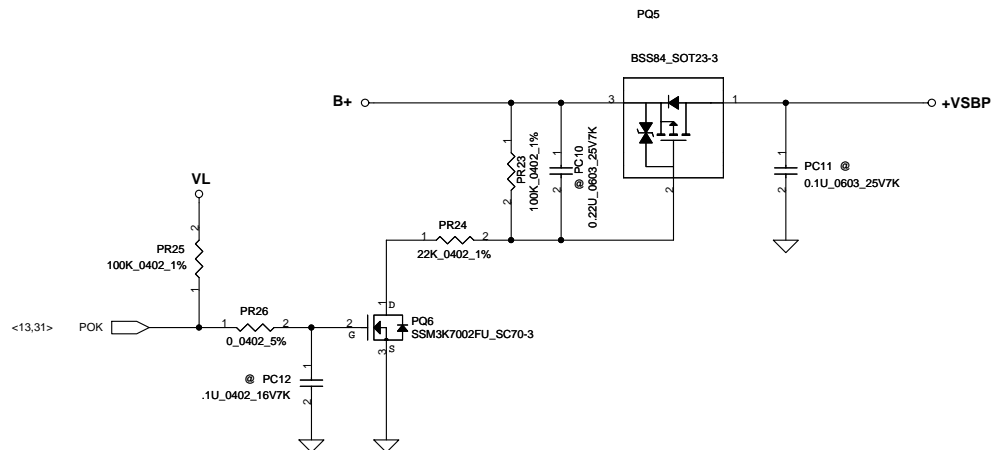
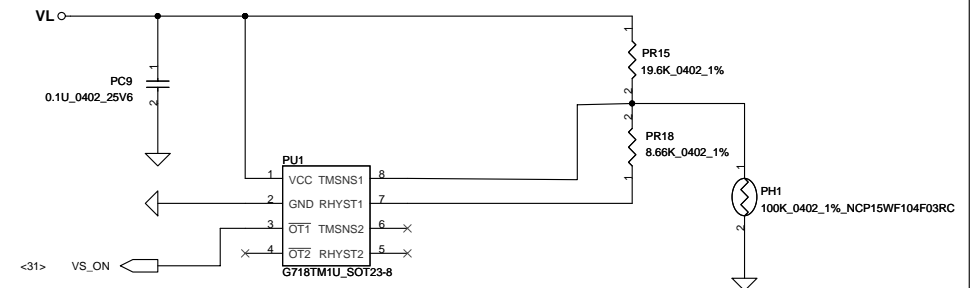
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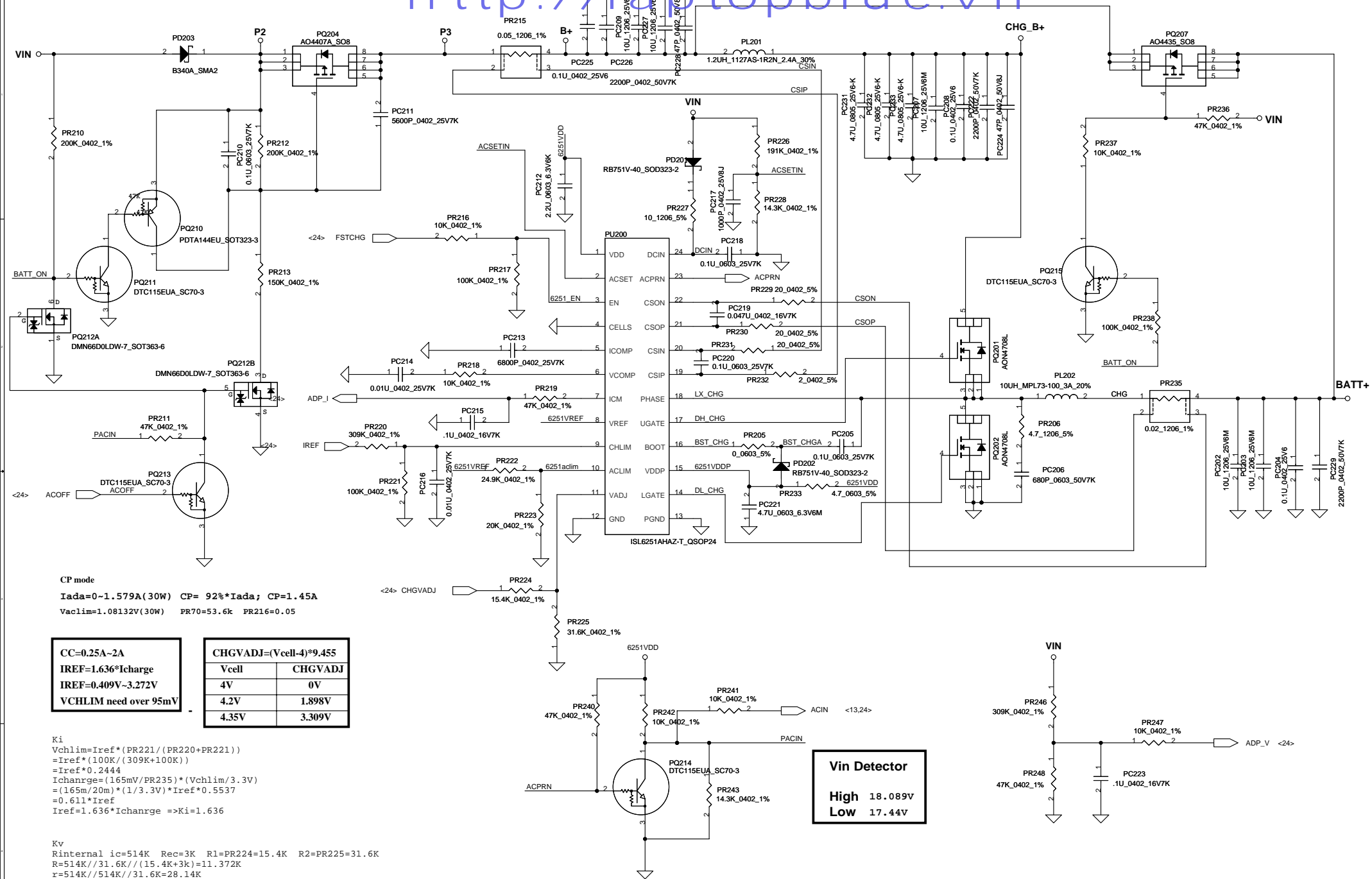


PH1 under CPU botten side :

CPU thermal protection at 95 degree C
Recovery at 56 degree C



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CP mode
 $I_{ada} = 0 \sim 1.579A (30W)$ CP= 92%* I_{ada} ; CP=1.45A
 $V_{aclim} = 1.08132V (30W)$ PR70=53.6k PR216=0.05

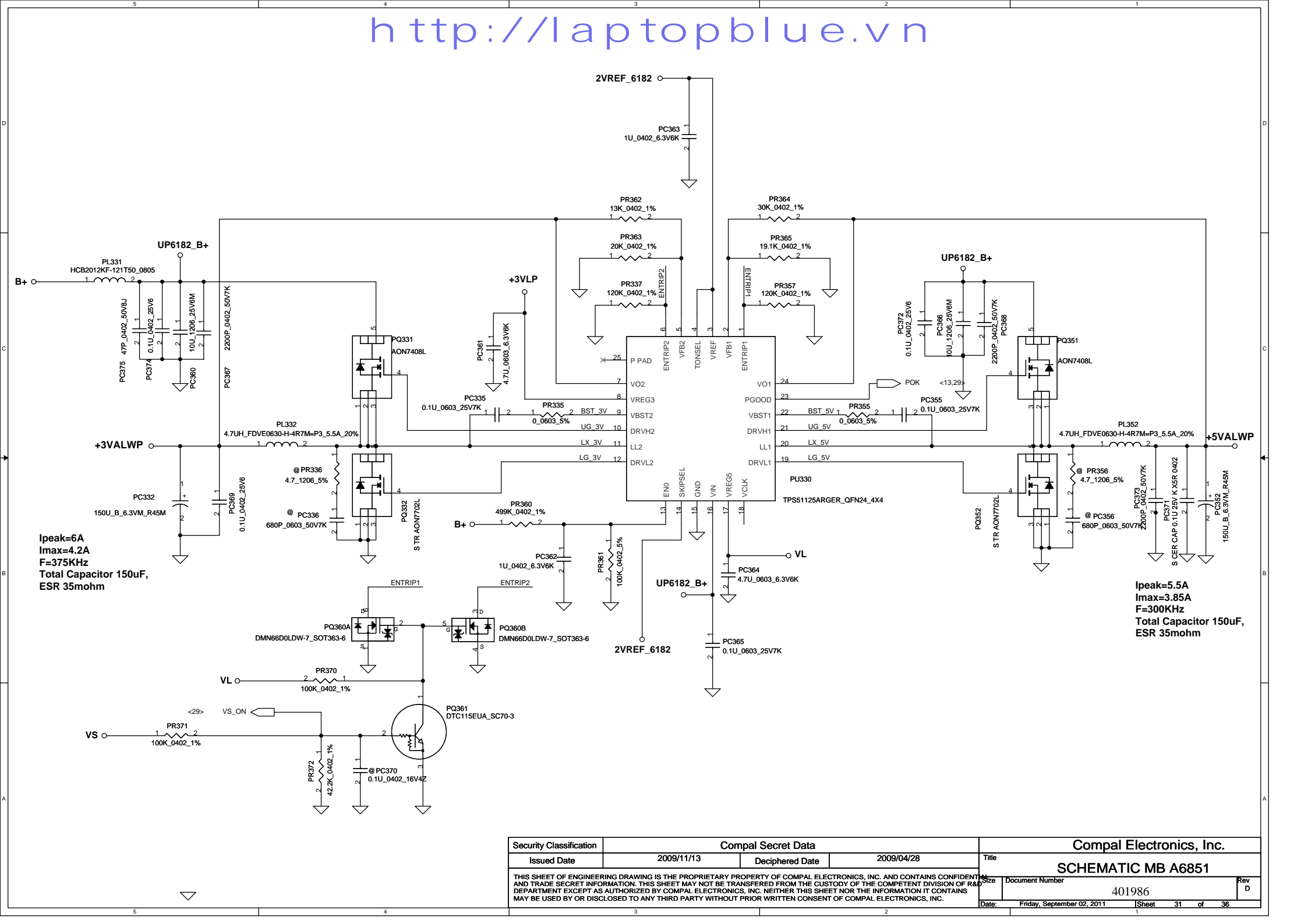
CC=0.25A~2A
 $I_{REF} = 1.636 * I_{charge}$
 $I_{REF} = 0.409V \sim 3.272V$
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.455	
Vcell	CHGVADJ
4V	0V
4.2V	1.898V
4.35V	3.309V

Ki
 $V_{chlim} = I_{ref} * (PR221 / (PR220 + PR221))$
 $= I_{ref} * (100K / (309K + 100K))$
 $= I_{ref} * 0.2444$
 $I_{charge} = (165mV / PR235) * (V_{chlim} / 3.3V)$
 $= (165m / 20m) * (1 / 3.3V) * I_{ref} * 0.5537$
 $= 0.611 * I_{ref}$
 $I_{ref} = 1.636 * I_{charge} \Rightarrow Ki = 1.636$

Kv
Internal ic=514K Rec=3K R1=PR224=15.4K R2=PR225=31.6K
 $R = 514K // 31.6K // (15.4K + 3K) = 11.372K$
 $r = 514K // 514K // 31.6K = 28.14K$
 $V_{cell} = 0.175 * V_{adj} + 3.99V$
 $4.2V = 0.175 * V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$
 $V_{adj} = V_{ref} * (R / (R + 514K)) + CALIBRATE * (r / (r + 514K))$
 $1.1483 = CALIBRATE * 0.6046 \Rightarrow CALIBRATE = 1.899$
 $1.899 = (4.2 - (V_{cell} + A * 0.175)) * Kv \Rightarrow Kv = (4.2 - (4.2 + A * 0.175)) * Kv$
 $A = V_{ref} * (R / (R + 514K)) = 0.052$
 $Kv = 9.455$

Vin Detector
High 18.089V
Low 17.44V



http://laptopblue.vn

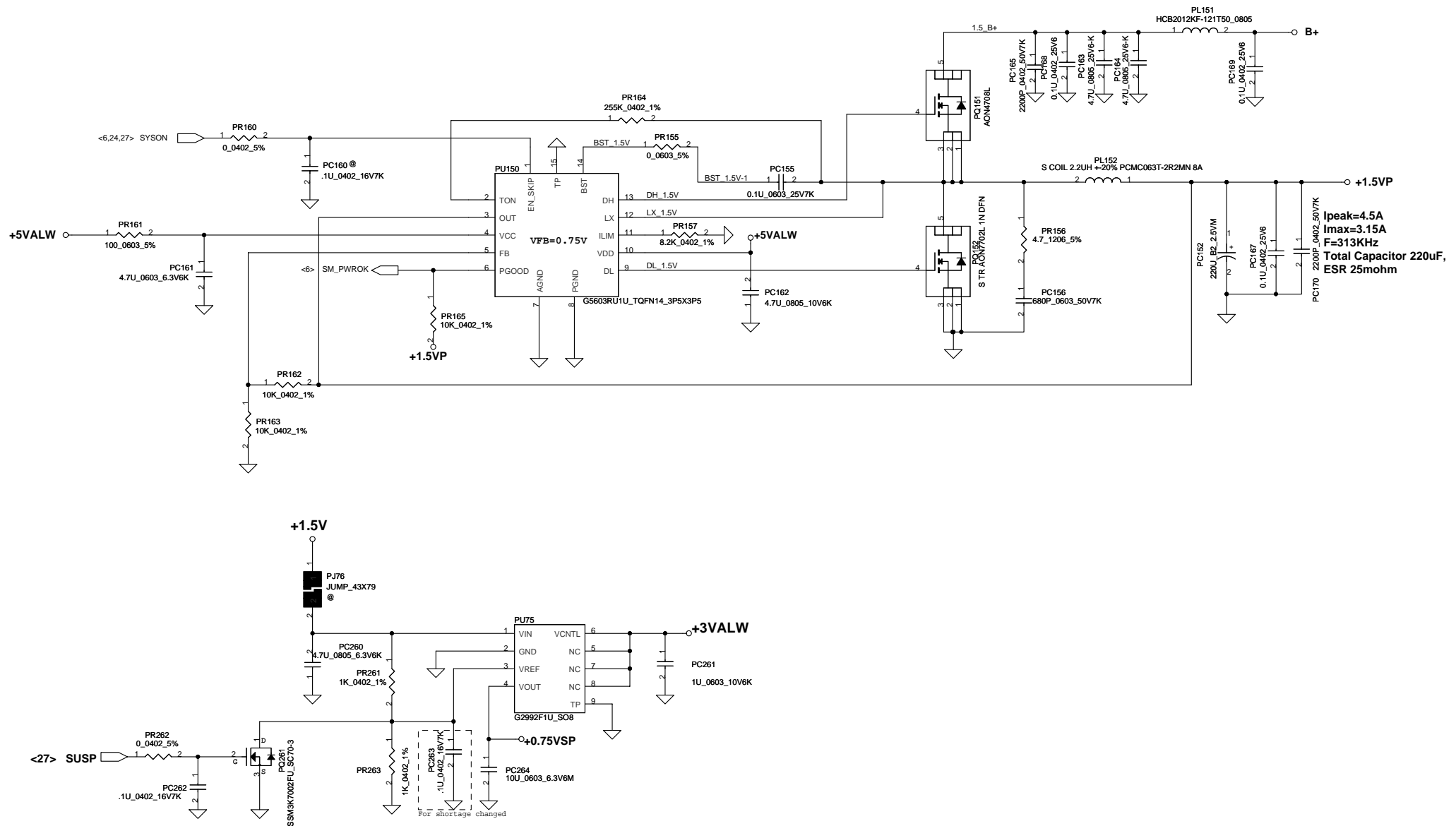
Specifications:

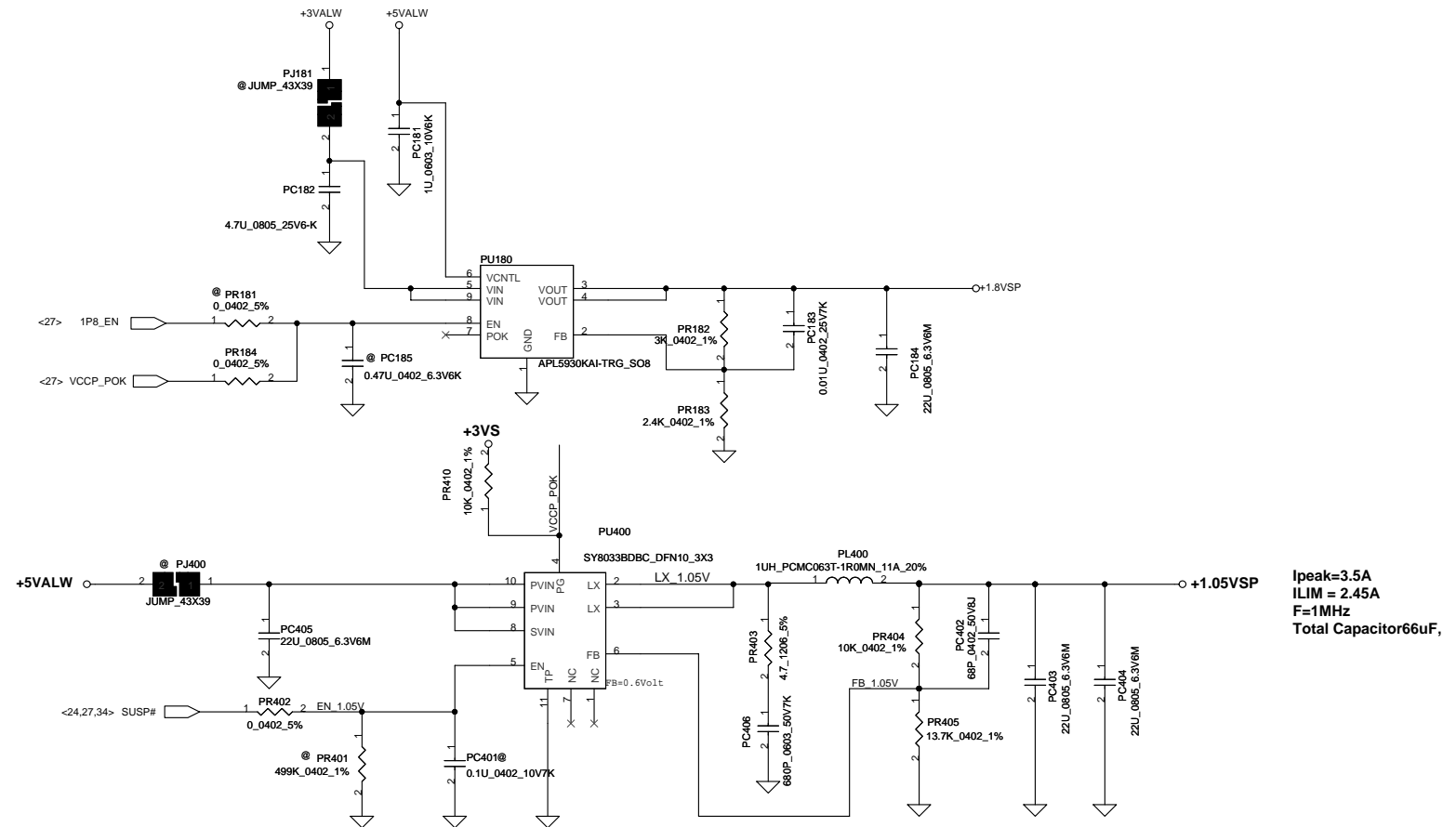
- I_{peak}=6A
- I_{max}=4.2A
- F=375KHz
- Total Capacitor 150uF, ESR 35mohm

Specifications:

- I_{peak}=5.5A
- I_{max}=3.85A
- F=300KHz
- Total Capacitor 150uF, ESR 35mohm

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
2010/8/23(DVT)	P32	+1.5VP/+0.75VSP	Change PU75 UP7711(SA00003XI00) -->G2992(SA00000VE80)	UPI had patent issue
2010/8/23(DVT)	P30	Charger	Change PU200 G5209(SA00003TK00) -->ISL6251(SA00001EP80)	G5209 had leakage issue
2010/8/23(DVT)	P31	+5VALWP/+3VALWP	Change PU330 UP6182(SA000043H00) -->TI51125A(SA000020C80)	UPI had patent issue
2010/8/23(DVT)	P30	Charger	add PR247(SD034100280) PC223(SE076104K80) PR246(SD034309380) PR248(SD034470280)	Support SA ECO unit
2010/8/23(DVT)	P35	CPU_CORE	Change PR526 174K (SD034174380) -->124K(SD034124380)	debug CPU load issue
2010/8/23(DVT)	All	snuber	Change PC273,PC274,PC275,PC403,PC404,PC405 22u(SE000008L80) -->PC273,PC274,PC275,PC403,PC404,PC405 22u(SE000000I10)	Chose the same material s
2010/8/23(DVT)	P30	Charger	Install PC222 PC224 0.1u (SE00000G880)	EMI commond
2010/8/23(DVT)	P30	Charger	Install PC227,PC209,PC207,PC208,PC204 10u (SE142106M80)	EMI commond
2010/8/23(DVT)	P35	CPU_CORE	Change PL500(SM01000BY00)-->(SM01000C000)	Chose the same material s
2010/8/23(DVT)	P31	+5VALWP/+3VALWP	Install PC371,PC369 0.1u (SE00000G880)	RF commond
2010/8/23(DVT)	P31	+5VALWP/+3VALWP	Install PC367 2200P(SE074222K80)	RF commond
2010/8/23(DVT)	P32	+1.5VP	Install PC165 2200P(SE074222K80)	RF commond
2010/8/23(DVT)	P32	+1.5VP	Install PC169,PC168,PC167 0.1u(SE00000G880)	RF commond
2010/8/23(DVT)	P35	CPU_CORE	add PC518 (SE071101J80)	debug CPU VR-ON issue
2010/9/21(PVT)	P30	Charger	Install PC225 PC208PC204 (0.1u) , PC226 PC222 PC229(2200P) Add PC208 add PC228 PC224 (47P),install snubber PR206,PC206	RF commond
2010/9/21(PVT)	P31	+5VALWP/+3VALWP	Add PC372 PC374(0.1u) , PC375(47P) PC371 (2200P)	RF commond
2010/9/21(PVT)	P32	+1.5VP	Add PC170(2200P) install snubber PR156 PC156	RF commond
2010/10/8(pre-MP)	p30	Charger	Change PL210 to 1.2u (SH00000B100)	EMI commond
2010/10/08(Pre-MP)	P31	+5VALWP/+3VALWP	Change PC332 & PC352 to ESR 45 m ohm	cost down plane
2010/10/08(Pre-MP)	p32	+1.5VP	Change PC152 to ESR 35 m ohm	cost down plane

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