

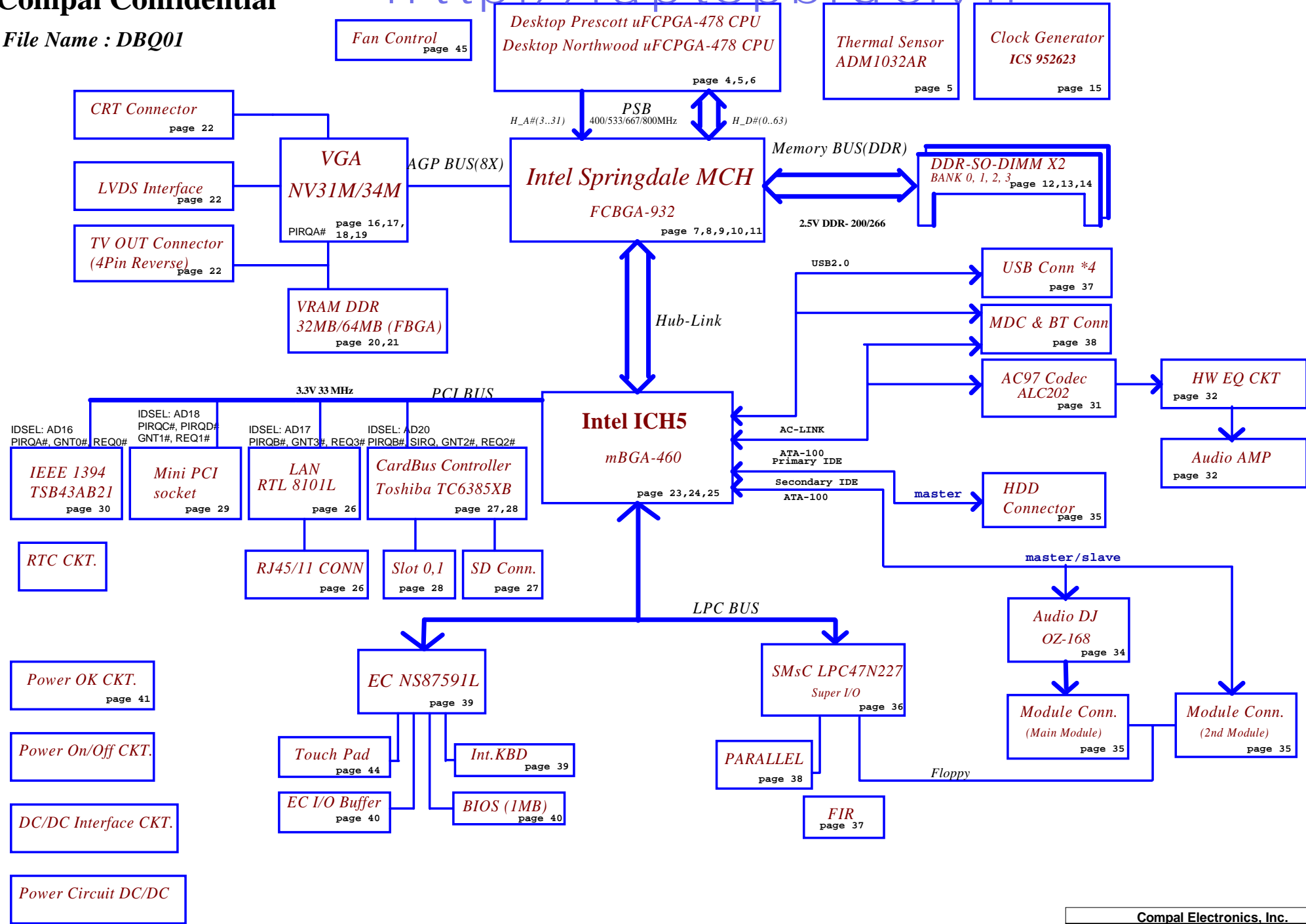
DBQ01 Rev0.1 Schematics Document

Intel Prescott uFCPGA-478 / P4 Northwood

with Springdale / ICH5 / nVIDIA NV34M/31M chipset

2003/07/01

Compal Electronics, Inc.			
Title			
Cover Sheet			
Size B	Document Number LA-2041		Rev 0.1
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_VID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VTT_GMCH	+1.225V (Prescott) / +1.45V (Northwood)	ON	OFF	OFF
+VGA_CORE	1.3V switched power rail for VGA chip	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X/8X	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
VGA			PIRQA
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
Mini-PCI	AD18	1/4	PIRQC/PIRQD
1394	AD16	0	PIRQA
SD	AD22		

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b	OZ168	0011 0100 b
(24C04)	1011 000Xb		

ICH5 SM Bus address

Device	Address
Clock Generator (ICS 952623)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 001Xb

http://laptopblue.vn

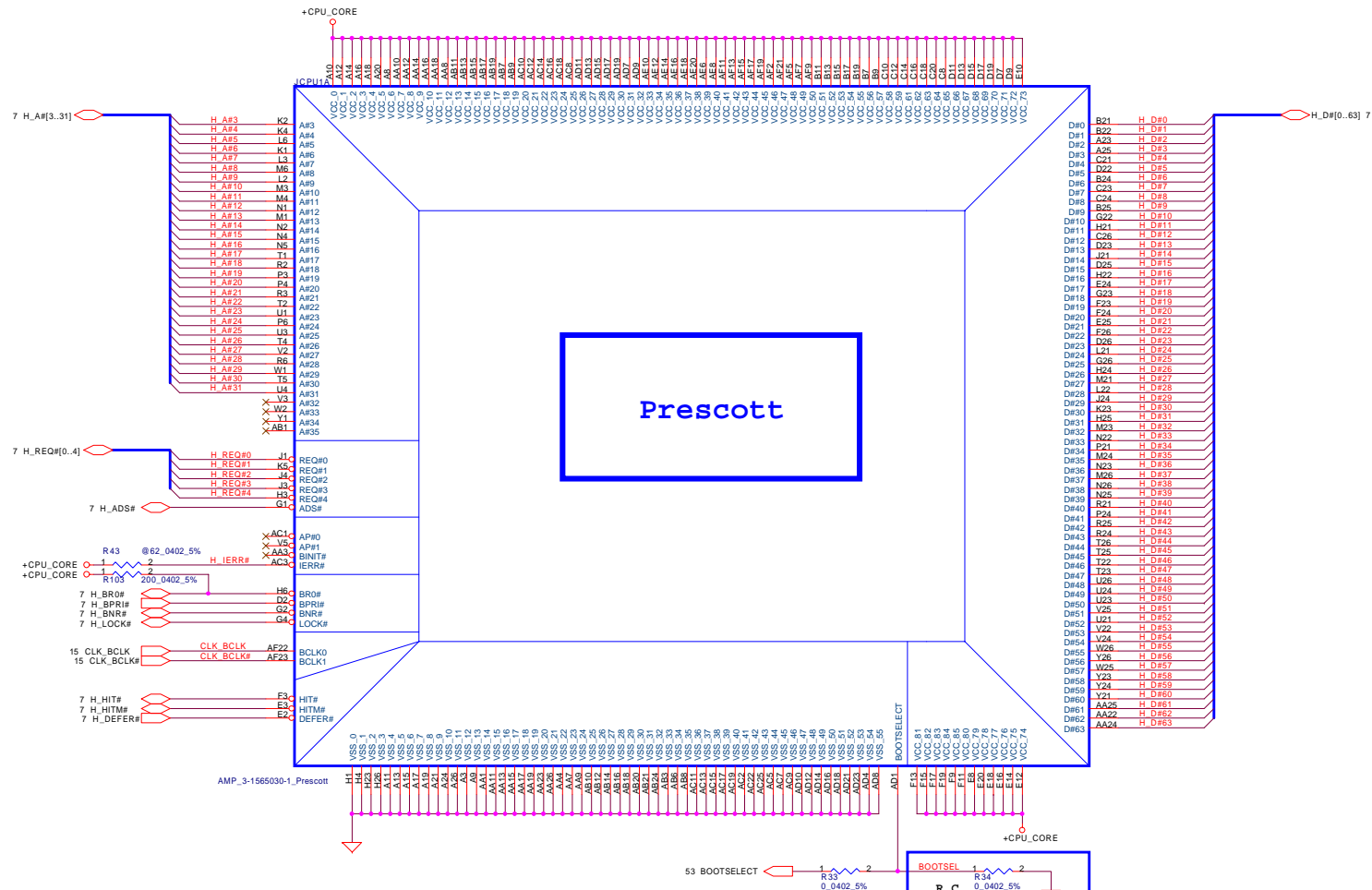
STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

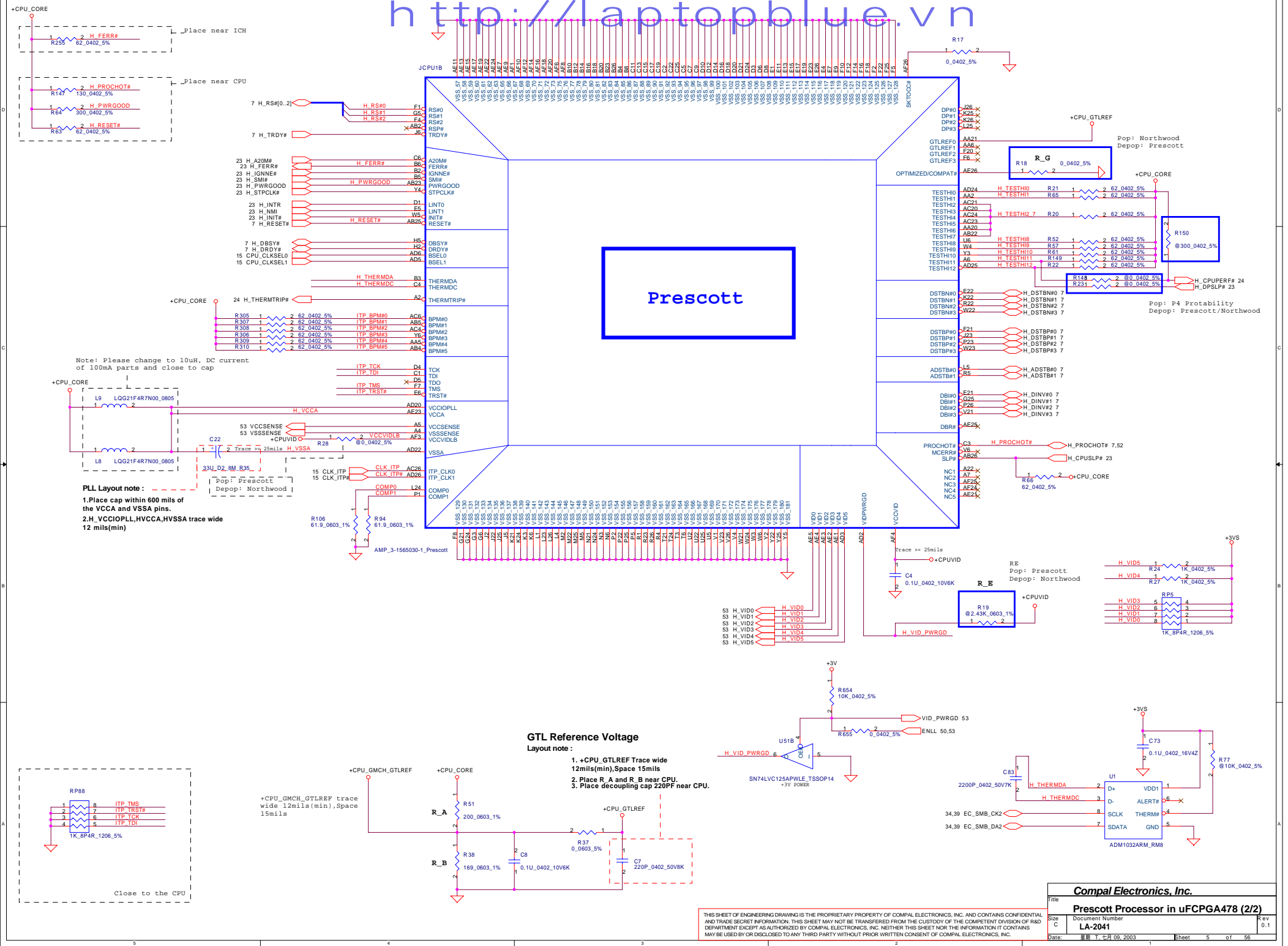
Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

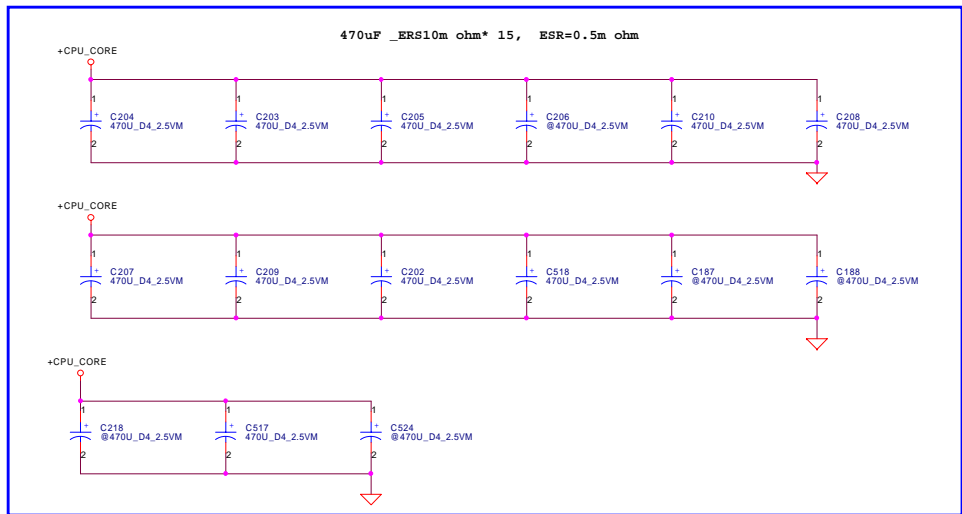
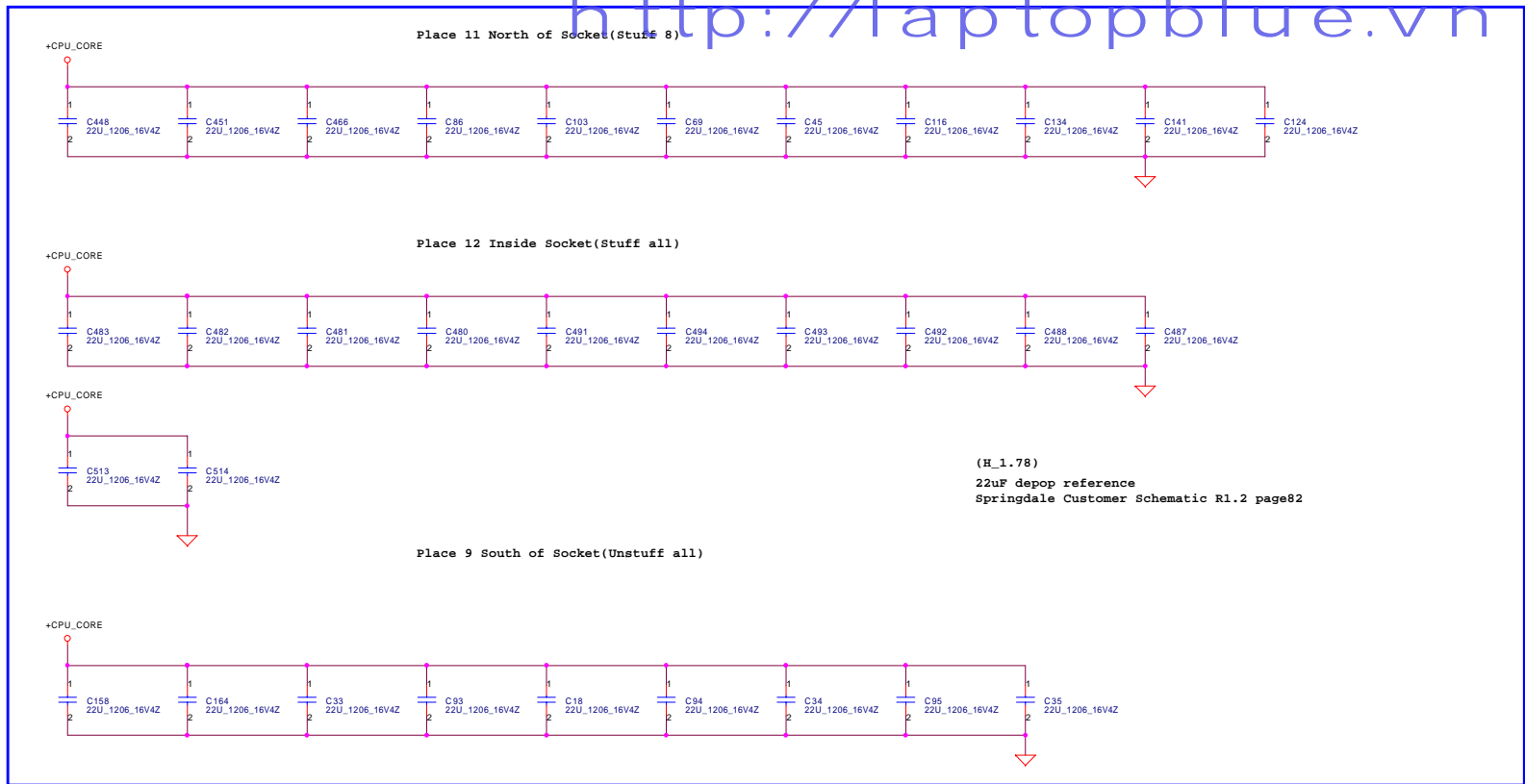
Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

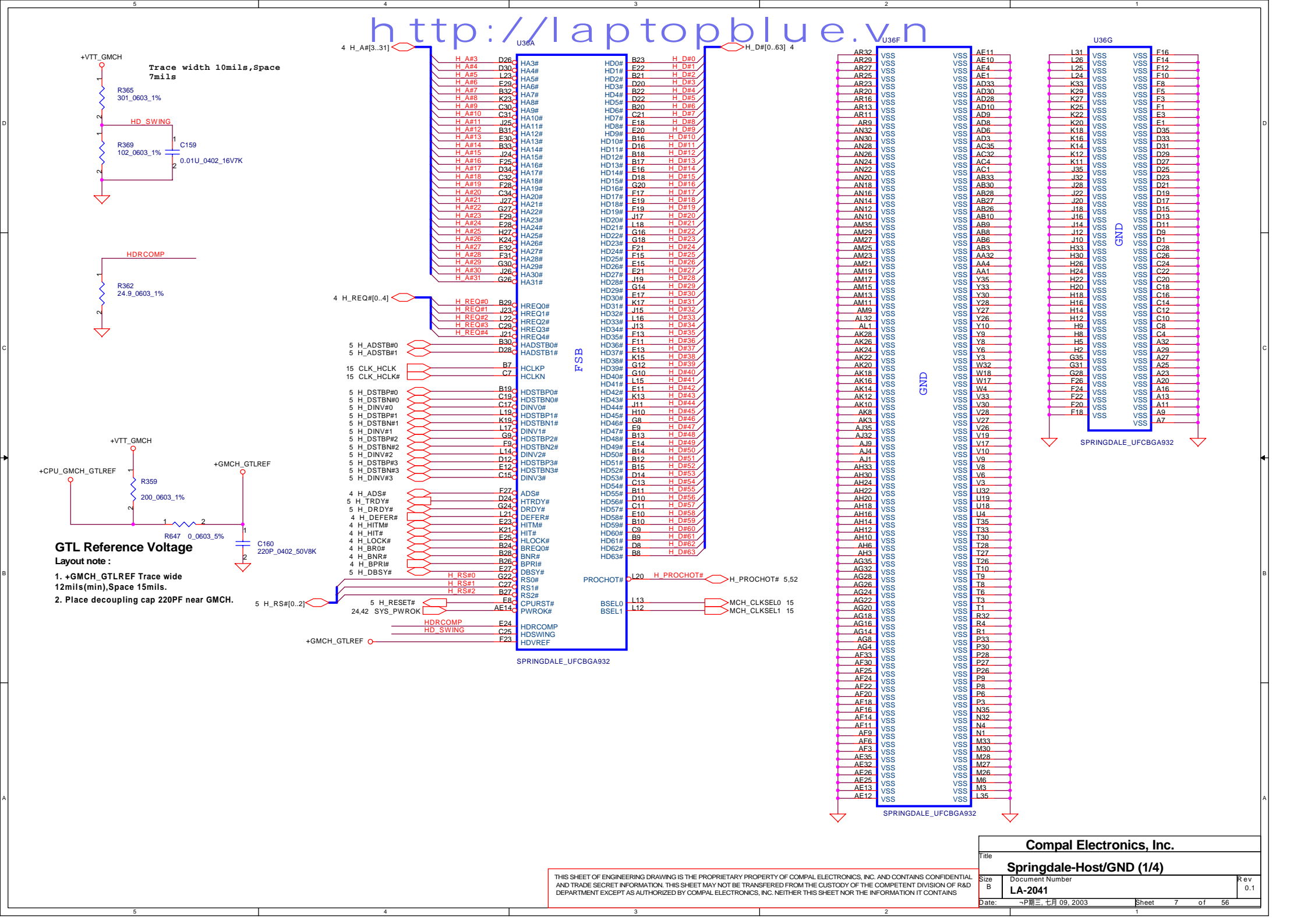
Compal Electronics, Inc.			
Title			
Notes			
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Reference Intel document						
Desktop P4 Spec.: 10988 P4 0.13u 512KB L2 EMTS Rev.2.0						
Desktop Prescott Spec.: 11910 Prescott EMTS Rev.0.5						
Pin number	Northwood Pin name	Comment	Prescott Pin name	Comment	Northwood	Prescott
B6	FERR#	Pull-up 62ohm to +VCC_CORE	FERR#/PBE#	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AA20	ITPCLKOUT0	Pull-up 62ohm to +VCC_CORE	TESTHI6	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AB22	ITPCLKOUT1	Pull-up 62ohm to +VCC_CORE	TESTHI7	Pull-up 62ohm to +VCC_CORE	Pop	Pop
AD2	NC	float	VIDPWRGD	Pull-up 8.2Kohm to +VCCVID	Depop	Pop
AD3	NC	float	VID5	Pull-up 1Kohm to +3VRUN & connect to PWRIC	Depop	Pop
AF3	NC	float	VCCVIDLB	Connect to +VCCVID	Depop	Pop
AD20	VCCA	Connect to CPU Filter	VCCIOPLL	Connect to CPU Filter		
AF23	VCCIOPLL	Connect to CPU Filter	VCCA	Connect to CPU Filter		
AD1	VSS	Connect to GND	BOOTSELECT	CPU determine	Pop	Depop
AE26	VSS	Connect to GND	OPTIMIZED/COMPAT#	float	Pop	Depop







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Trace width 10mils, Space 7mils

HD SWING

HDRCOMP

GTL Reference Voltage

Layout note :

- +GMCH_GTLREF Trace wide 12mils(min), Space 15mils.
- Place decoupling cap 220PF near GMCH.

COMPONENTS:

- R365 301_0603_1%
- R369 102_0603_1%
- C159 0.01U_0402_16V7K
- R362 24.9_0603_1%
- R359 200_0603_1%
- R647 0_0603_5%
- C160 220P_0402_50V8K

PIN CONNECTIONS:

- 4 H_A#[3..31]
- 4 H_D#[0..63]
- 4 H_REQ#[0..4]
- 5 H_ADSTB#0
- 5 H_ADSTB#1
- 15 CLK_HCLK
- 15 CLK_HCLK#
- 5 H_DSTBP#0
- 5 H_DSTBN#0
- 5 H_DINV#0
- 5 H_DSTBP#1
- 5 H_DSTBN#1
- 5 H_DINV#1
- 5 H_DSTBP#2
- 5 H_DINV#2
- 5 H_DSTBP#3
- 5 H_DINV#3
- 4 H_ADS#
- 5 H_TRDY#
- 5 H_DRDY#
- 4 H_DEFER#
- 4 H_HITM#
- 4 H_HIT#
- 4 H_LOCK#
- 4 H_BR0#
- 4 H_BNR#
- 4 H_BPR#
- 5 H_DBSY#
- 5 H_RS#[0..2]
- 5 H_RESET#
- 24.42 SYS_PWROK
- +GMCH_GTLREF
- +GMCH_GTLREF

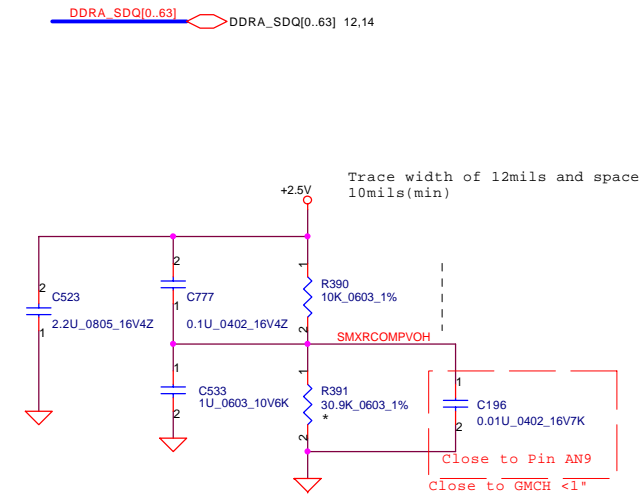
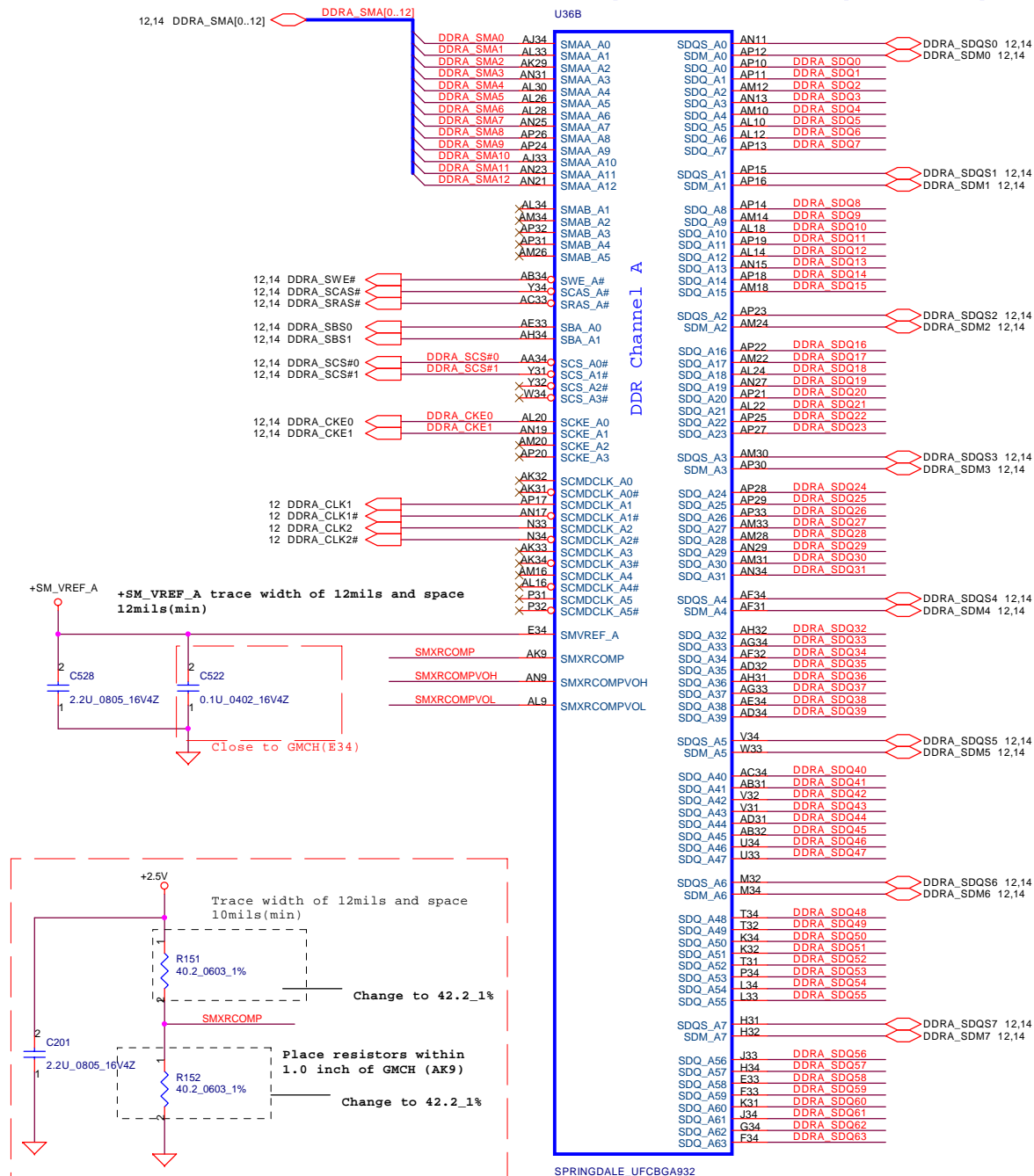
SPRINGDALE_UFCBGA932

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Springdale-Host/GND (1/4)

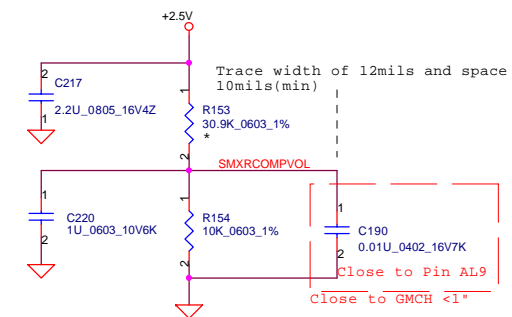
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* Change to 31.12R

Follow Intel design guide
R1.11(12474) page124,125



13,14 DDRB_SMA[0..12] **DDR8 SMA[0..12]** U36C

DDR8 SMA0 AG31
DDR8 SMA1 AJ31
DDR8 SMA2 AD27
DDR8 SMA3 AE24
DDR8 SMA4 AK27
DDR8 SMA5 AG25
DDR8 SMA6 AL25
DDR8 SMA7 AF21
DDR8 SMA8 AL23
DDR8 SMA9 AJ22
DDR8 SMA10 AF29
DDR8 SMA11 AL21
DDR8 SMA12 AJ20

AE27
AD26
AL29
AL27
AE23

13,14 DDRB_SWE# W27
13,14 DDRB_SCAS# W31
13,14 DDRB_SRAS# W26

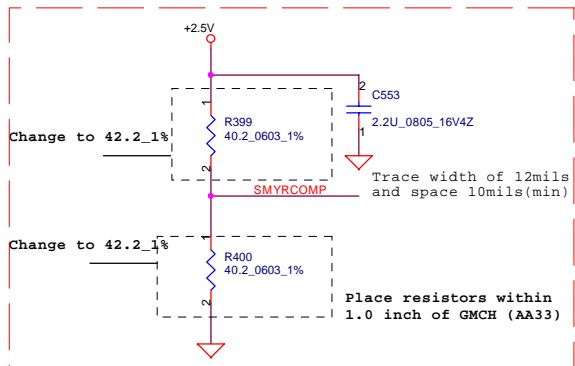
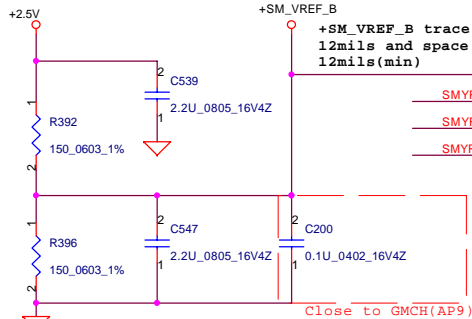
13,14 DDRB_SBS0 Y25
13,14 DDRB_SBS1 AA25

13,14 DDRB_SCS#0 U26
13,14 DDRB_SCS#1 T29
W25
W25

13,14 DDRB_CKE0 AK19
13,14 DDRB_CKE1 AK19

13 DDRB_CLK1 AG29
13 DDRB_CLK1# AG30
13 DDRB_CLK2 AF17
13 DDRB_CLK2# AG17

SM_VREF_B and SM_VREF_A
are connected inside GMCH.



DDR Channel B

SDQS_B0 AF15
SDM_B0 AG11
SDQ_B0 AJ10
SDQ_B1 AE15
SDQ_B2 AE16
SDQ_B3 AL11
SDQ_B4 AE16
SDQ_B5 AL8
SDQ_B6 AF12
SDQ_B7 AK11
SDQ_B8 AG12
SDQ_B9 AG12
SDQ_B10 AF12
SDQ_B11 AK11
SDQ_B12 AG12
SDQ_B13 AF12
SDQ_B14 AK11
SDQ_B15 AG12

SDQS_B1 AG13
SDM_B1 AG15

SDQ_B8 AE17
SDQ_B9 AL13
SDQ_B10 AK17
SDQ_B11 AL17
SDQ_B12 AK13
SDQ_B13 AJ14
SDQ_B14 AJ16
SDQ_B15 AJ18

SDQS_B2 AG21
SDM_B2 AE21

SDQ_B16 AE19
SDQ_B17 AE20
SDQ_B18 AG23
SDQ_B19 AK23
SDQ_B20 AL19
SDQ_B21 AK21
SDQ_B22 AJ24
SDQ_B23 AE22

SDQS_B3 AH27
SDM_B3 AJ28

SDQ_B24 AK25
SDQ_B25 AH26
SDQ_B26 AG27
SDQ_B27 AF27
SDQ_B28 AJ26
SDQ_B29 AJ27
SDQ_B30 AD25
SDQ_B31 AF28

SDQS_B4 AD29
SDM_B4 AC31

SDQ_B32 AE30
SDQ_B33 AC27
SDQ_B34 AC30
SDQ_B35 Y29
SDQ_B36 AE31
SDQ_B37 AE29
SDQ_B38 AA26
SDQ_B39 AA27

SDQS_B5 U30
SDM_B5 U31

SDQ_B40 AA30
SDQ_B41 W30
SDQ_B42 U27
SDQ_B43 T25
SDQ_B44 AA31
SDQ_B45 V29
SDQ_B46 U25
SDQ_B47 R27

SDQS_B6 L27
SDM_B6 M29

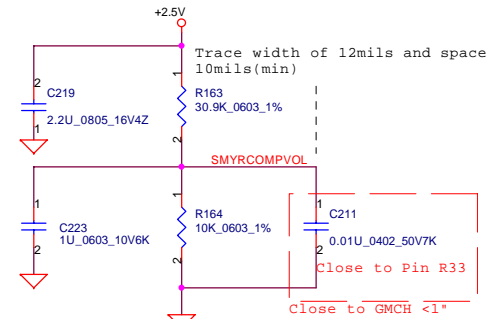
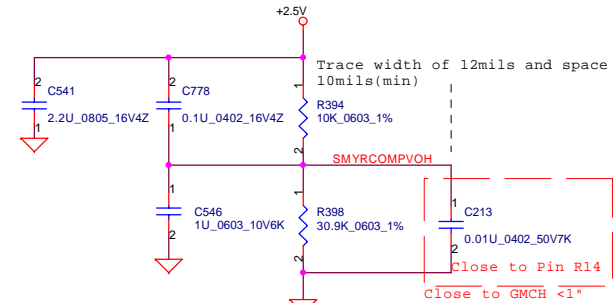
SDQ_B48 P29
SDQ_B49 R30
SDQ_B50 K28
SDQ_B51 L30
SDQ_B52 R31
SDQ_B53 R26
SDQ_B54 P25
SDQ_B55 L32

SDQS_B7 J30
SDM_B7 J31

SDQ_B56 K30
SDQ_B57 H29
SDQ_B58 F32
SDQ_B59 G33
SDQ_B60 N25
SDQ_B61 M25
SDQ_B62 J29
SDQ_B63 G32

SPRINGDALE_UFCBGA932

DDR8 SDQ[0..63] 13,14



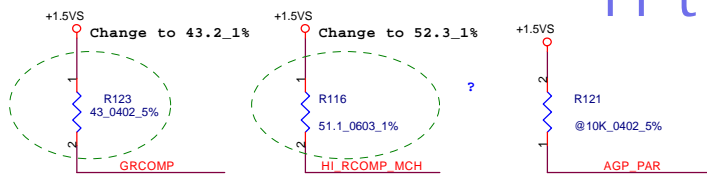
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Springdale-DDR Interface-B(3/5)

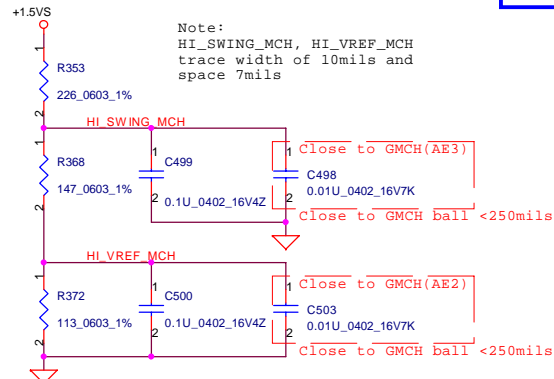
Size B Document Number LA-2041 Rev 0.1

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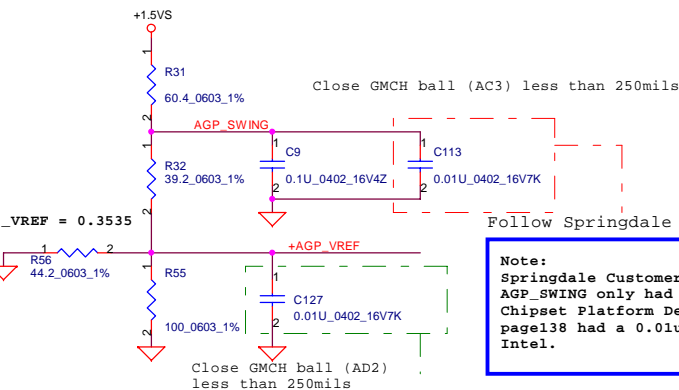
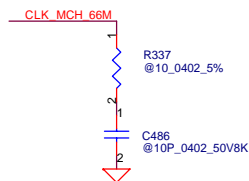
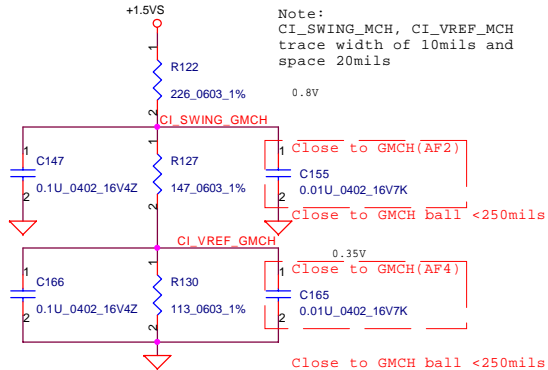
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```
1: External AGP
0: Internal Graphics
```

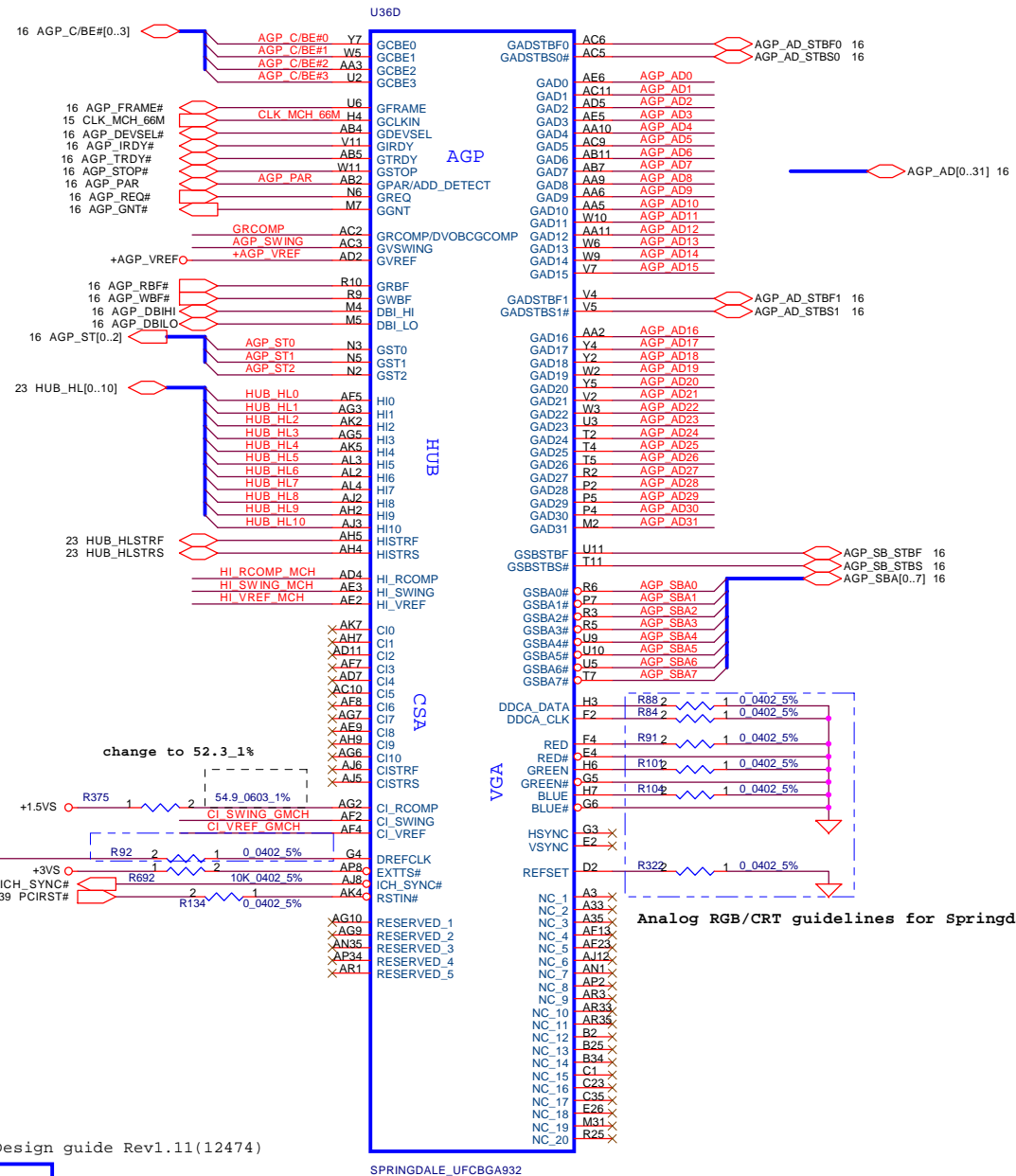


Note:
CI_SWING_MCH, CI_VREF_MCH
trace width of 10mils and
space 20mils



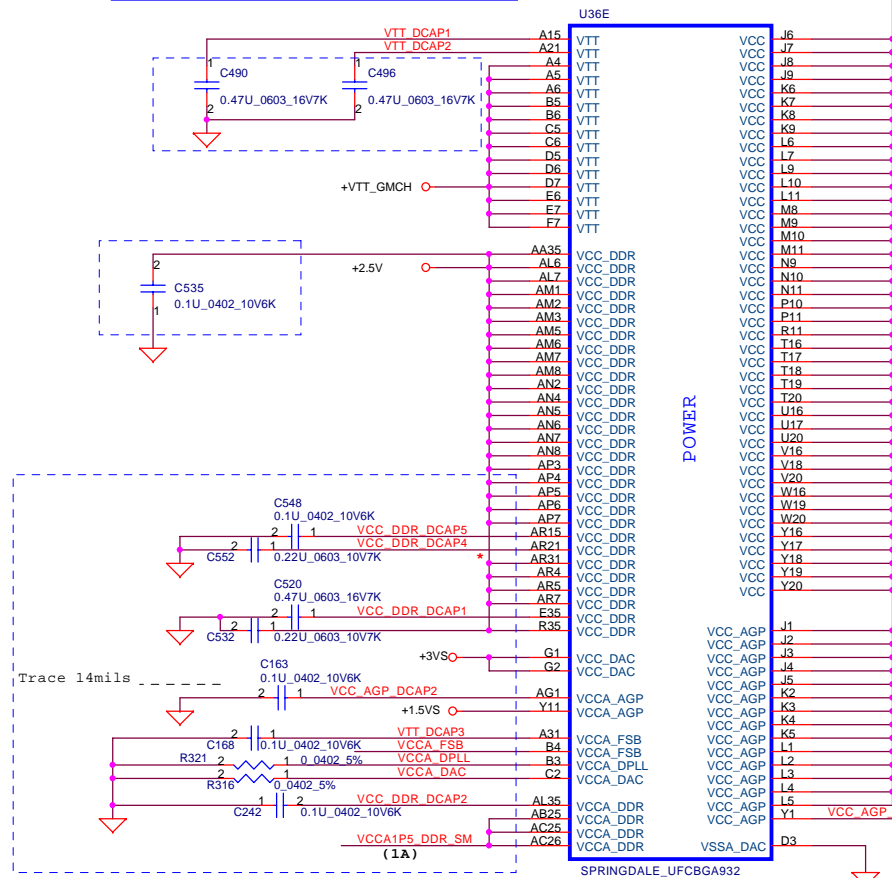
Follow Springdale Chipset Platform Design guide Rev1.11(12474)

Note:
Springdale Customer Schematic R1.2 page18
AGP_SWING only had 0.1u cap ; But Springdale
Chipset Platform Design guide Rev1.11(12474)
page138 had a 0.01uf cap. need confirm with
Intel.



Analog RGB/CRT guidelines for Springdale-P

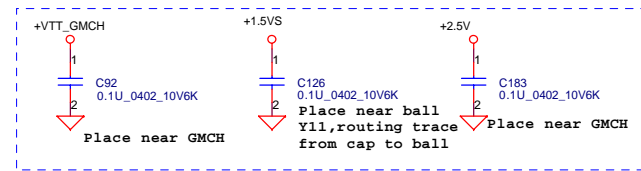
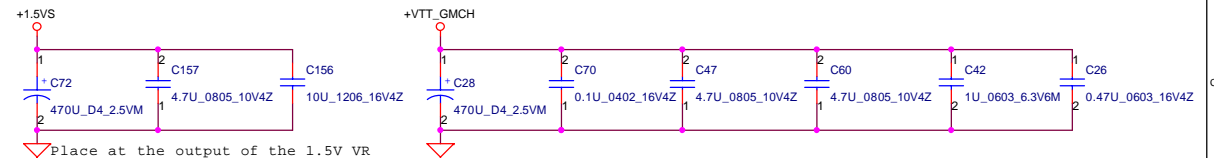
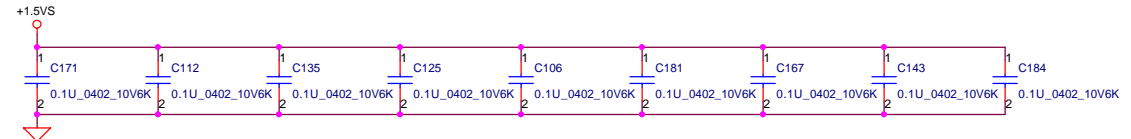
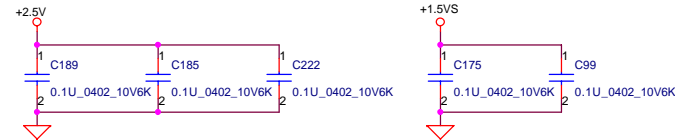
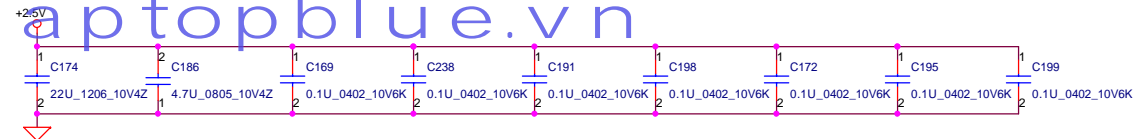
Note:
Placed less than 100 mils from ball
Route to GMCH ball without via



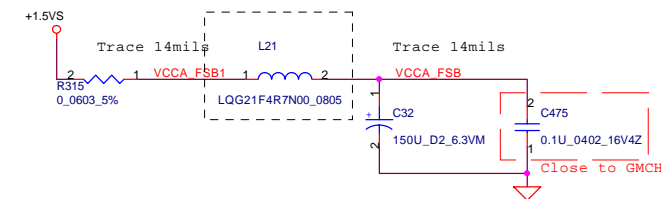
Note:
Placed less than 100 mils from ball
Route to GMCH ball without via

Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)page246,248

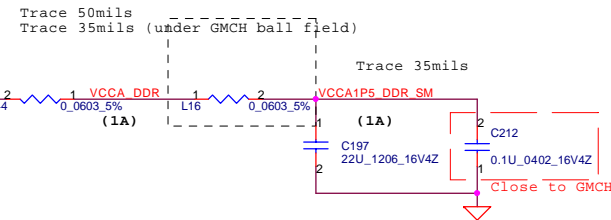
Decoupling Reference Document:
Springdale Customer Schematic R1.2 page84



Note: Please change to 0.82uH, DC current of 30mA parts and close to cap



Note: Please change to 1uH(0.54uH-D-IN), DC current of 1000mA parts and close to cap



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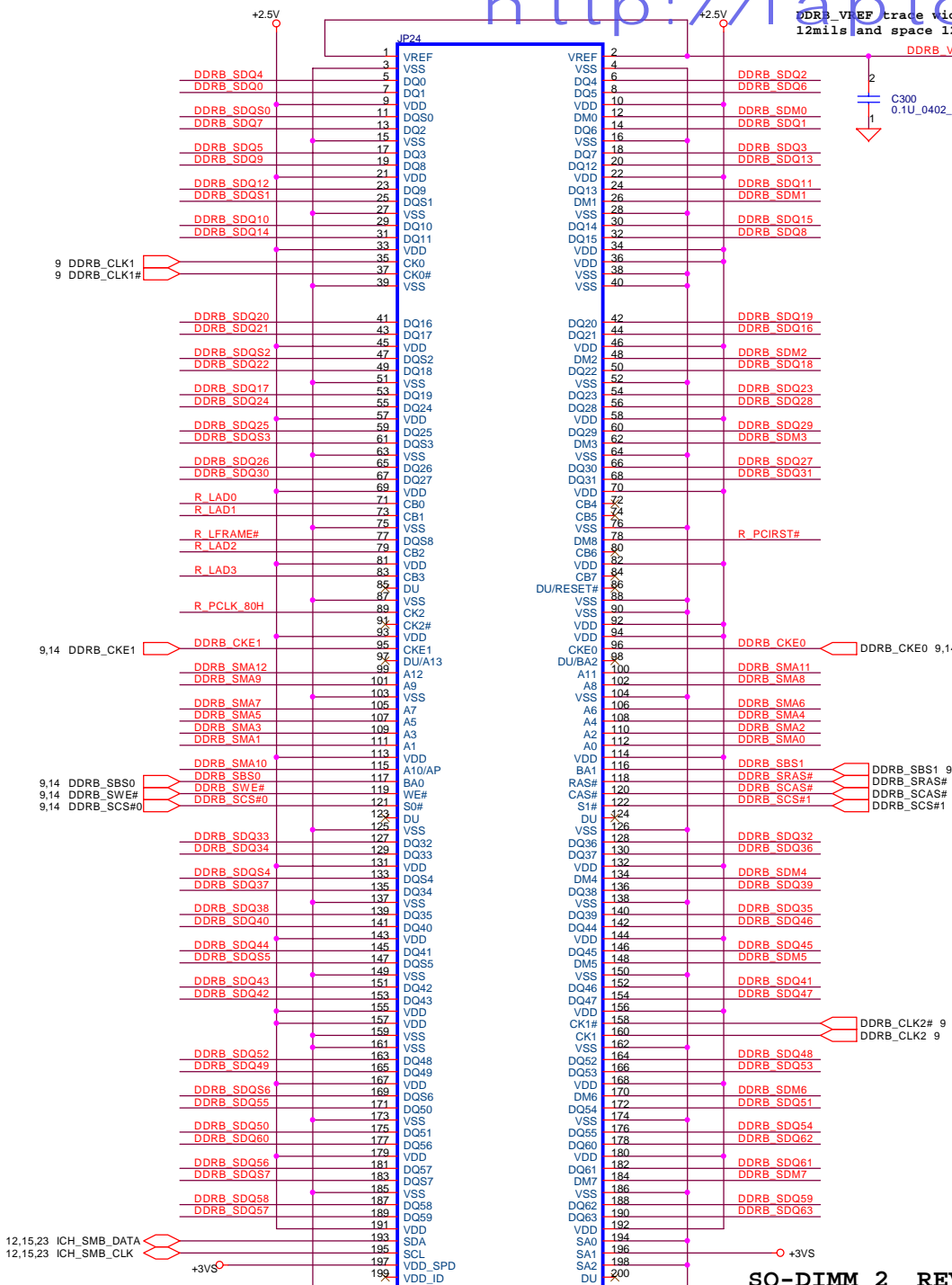
Springdale-Decoupling (5/5)

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A

DDR VREF trace width of 12mils and space 12mils(min)



KLINK_5746-3-111

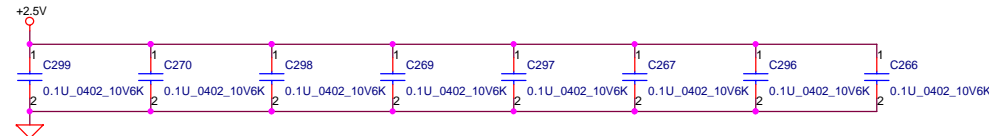
H= 9.2mm

SO-DIMM 2 REVERSE

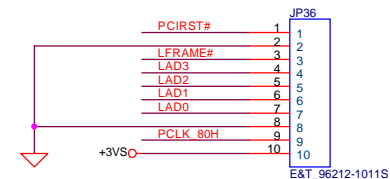
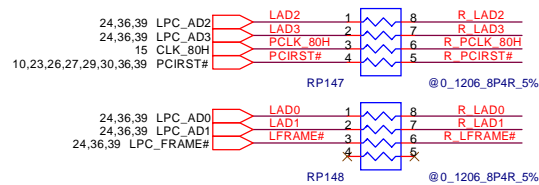
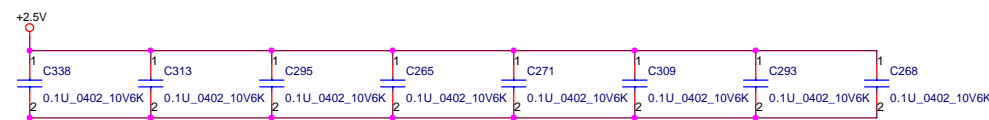
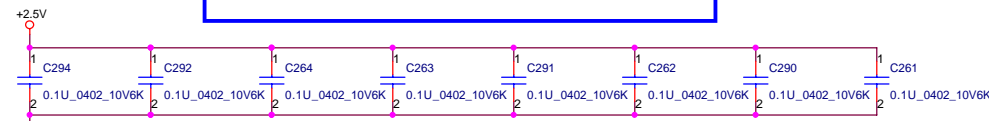
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- 9,14 DDRB_SDQ[0..63] \rightarrow DDRB_SDQ[0..63]
- 9,14 DDRB_SDQS[0..7] \rightarrow DDRB_SDQS[0..7]
- 9,14 DDRB_SMA[0..12] \rightarrow DDRB_SMA[0..12]
- 9,14 DDRB_SDM[0..7] \rightarrow DDRB_SDM[0..7]

System Memory Decoupling caps



Decoupling Reference Document:
Springdale Customer Schematic R1.2 page26
each Channel(two DIMMs) requirement 0.1uF*24

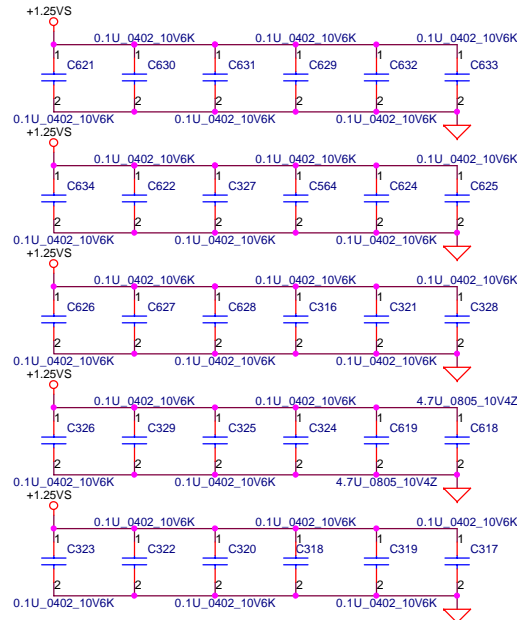


DEBUG PORT

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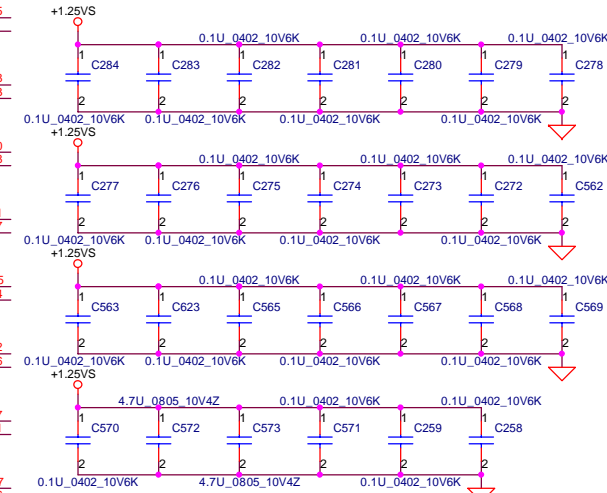
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Size		Document Number		Rev
		LA-2041		0.1
Date:		~P 星期三, 七月 09, 2003	Sheet	13 of 56

Decoupling caps (Channel B DIMM1) Termination resistors



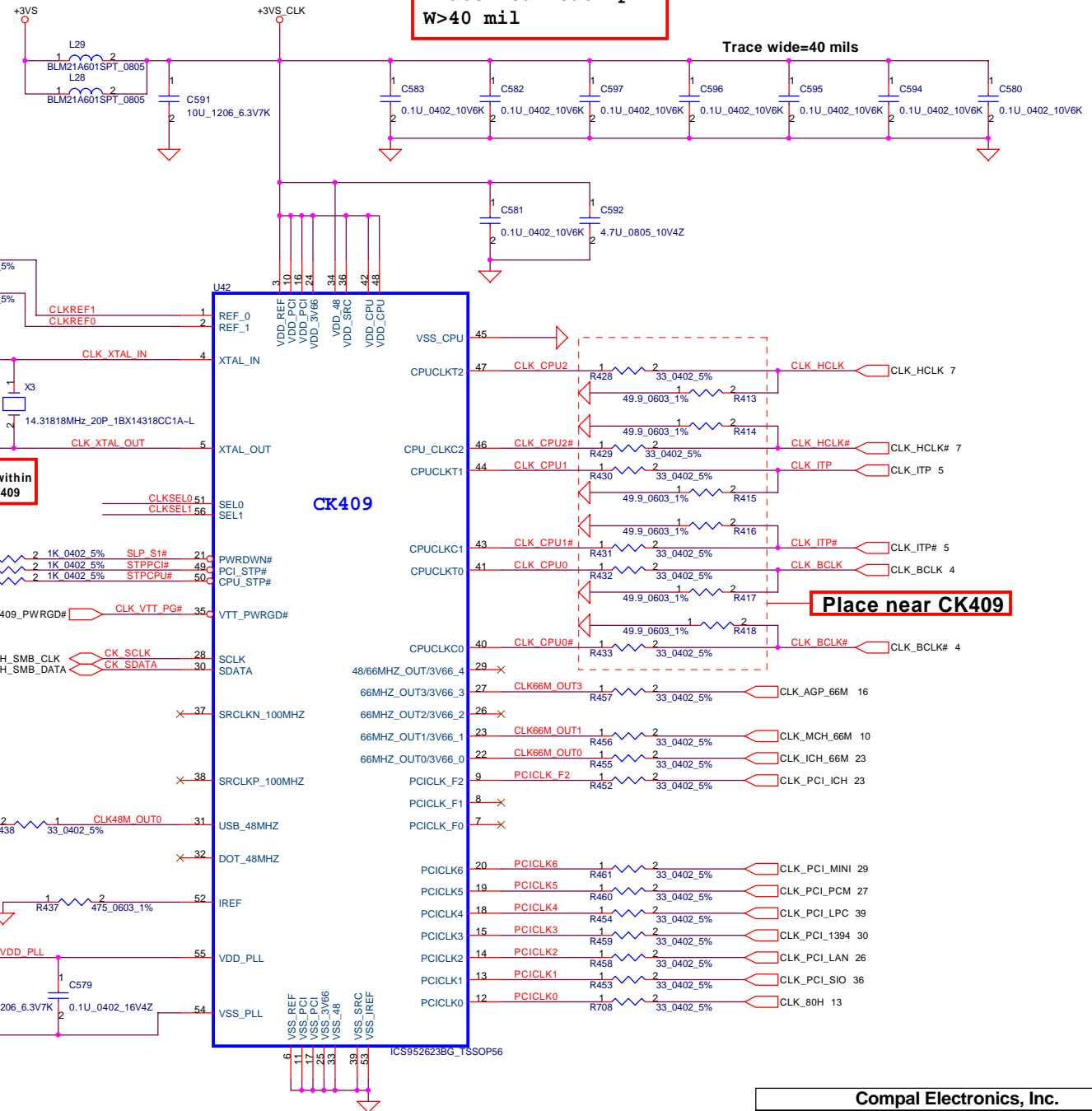
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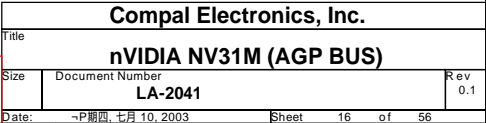
Channel B (DIM1) Termination resistors & Decoupling caps



Title			
DDR Termination Resistors			
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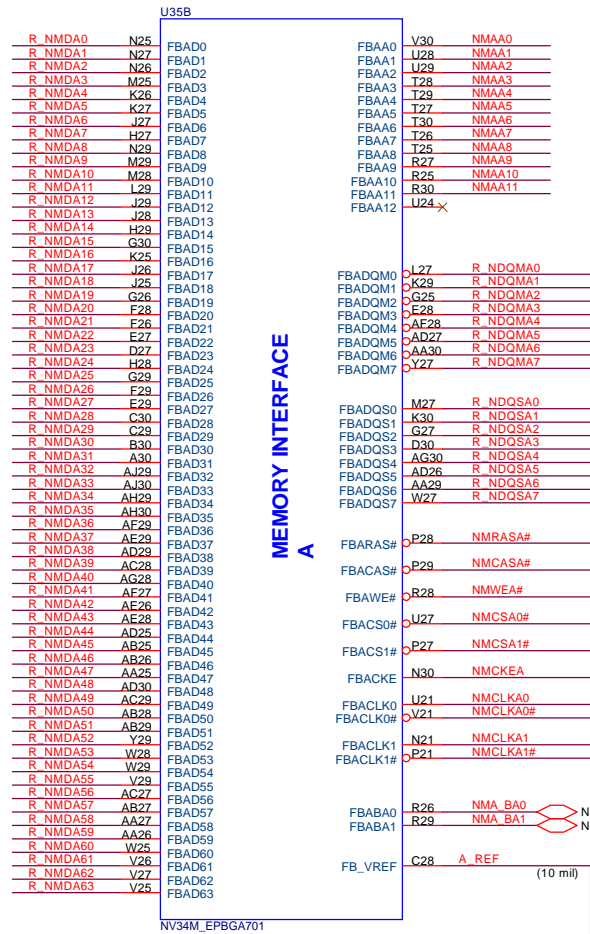
SEL0	SEL1	CPU	3V66[0..3]	REF0	REF1	SRC	USB/Dot
0	0	100	66	14.3	14.3	100/200	48
0	MID	REF	REF	REF	REF	REF	REF
0	1	200	66	14.3	14.3	100/200	48
1	0	133	66	14.3	14.3	100/200	48
1	1	166	66	14.3	14.3	100/200	48
1	MID	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z





20 R_NDQMA[0..7] R_NDQMA[0..7]
20 R_NDQSA[0..7] R_NDQSA[0..7]
20 NMAA[0..11] NMAA[0..11]
20 R_NMDA[0..63] R_NMDA[0..63]

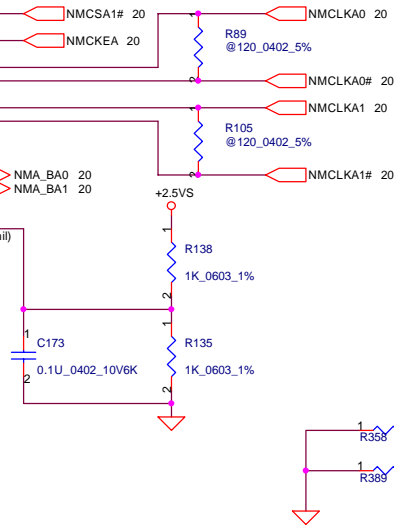
21 R_NDQMB[0..7] R_NDQMB[0..7]
21 R_NDQSB[0..7] R_NDQSB[0..7]
21 NMAB[0..11] NMAB[0..11]
21 R_NMDB[0..63] R_NMDB[0..63]

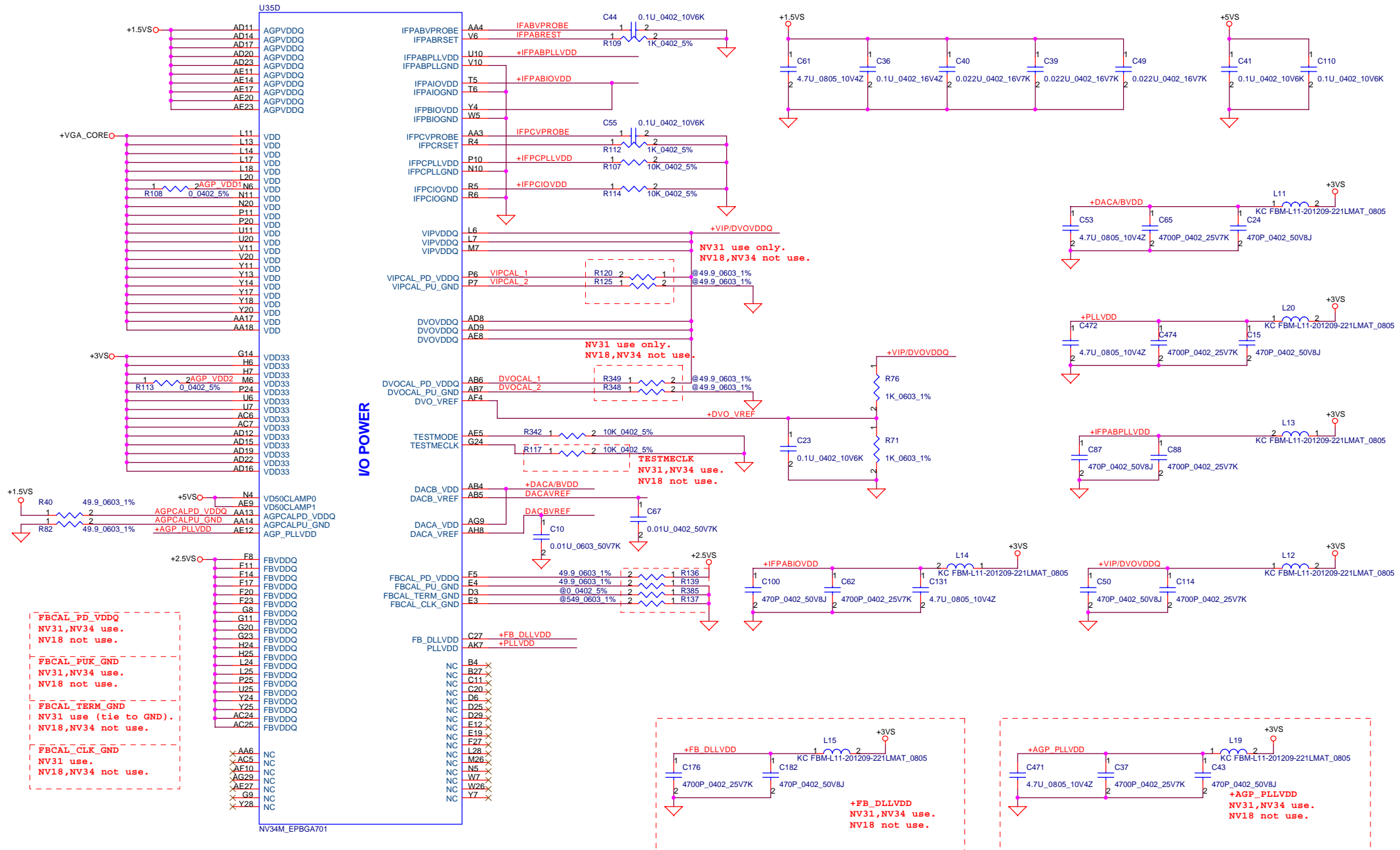


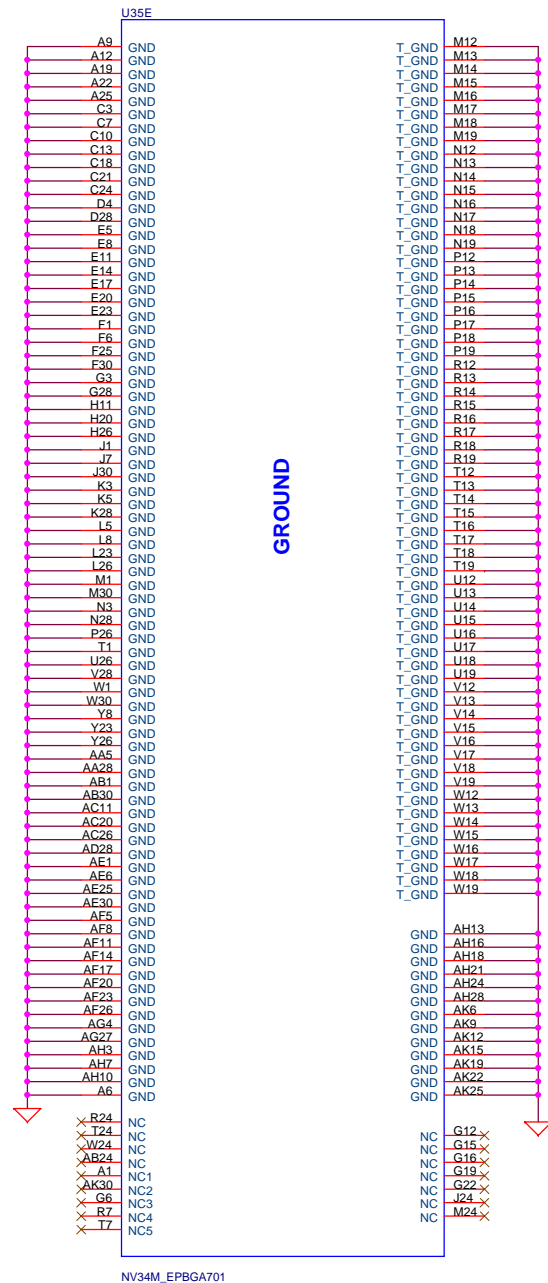
MEMORY INTERFACE A

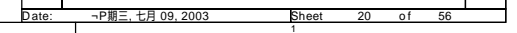


MEMORY INTERFACE B









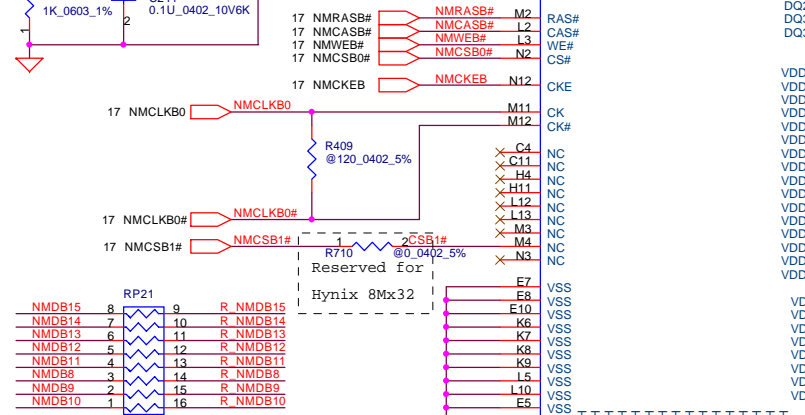
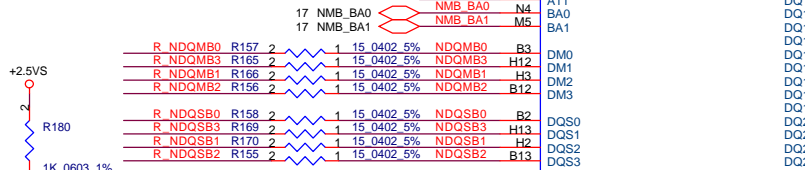
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17_R_NDQSB[0..7] R_NDQSB[0..7]
17_NMAB[0..11] R_NMAB[0..11]
17_R_NMDB[0..63] R_NMDB[0..63]

RP16
1 16 R_NMDB0
2 15 R_NMDB2
3 14 R_NMDB1
4 13 R_NMDB3
5 12 R_NMDB4
6 11 R_NMDB5
7 10 R_NMDB6
8 9 R_NMDB7

22_16P8R_1206_5%

RP20
1 16 R_NMDB31
2 15 R_NMDB30
3 14 R_NMDB29
4 13 R_NMDB28
5 12 R_NMDB27
6 11 R_NMDB26
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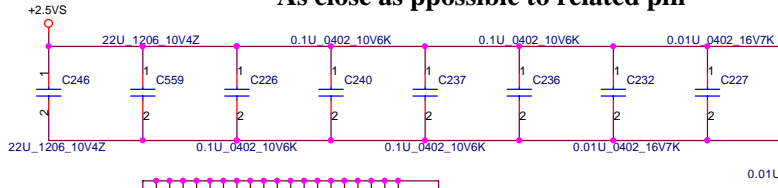


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1 8 R_NMDB15
2 7 R_NMDB14
3 6 R_NMDB13
4 5 R_NMDB12
5 4 R_NMDB11
6 3 R_NMDB10
7 2 R_NMDB9
8 1 R_NMDB8

22_16P8R_1206_5%

RP15
1 16 R_NMDB16
2 15 R_NMDB17
3 14 R_NMDB18
4 13 R_NMDB19
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22_16P8R_1206_5%

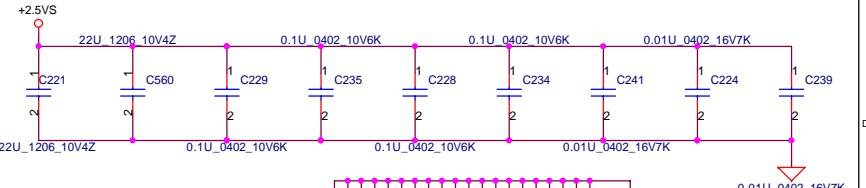
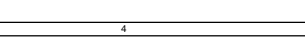
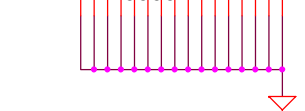
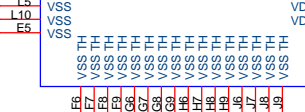
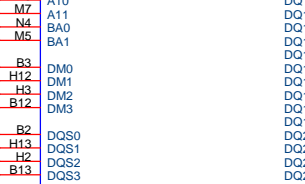


RP18
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2 15 R_NMDB41
3 14 R_NMDB42
4 13 R_NMDB43
5 12 R_NMDB44
6 11 R_NMDB45
7 10 R_NMDB46
8 9 R_NMDB47

22_16P8R_1206_5%

RP22
1 8 R_NMDB55
2 7 R_NMDB54
3 6 R_NMDB53
4 5 R_NMDB52
5 4 R_NMDB51
6 3 R_NMDB50
7 2 R_NMDB49
8 1 R_NMDB48

22_16P8R_1206_5%

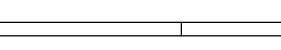
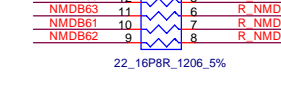
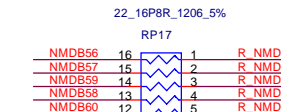
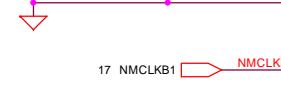
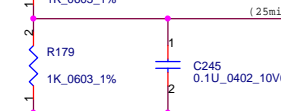
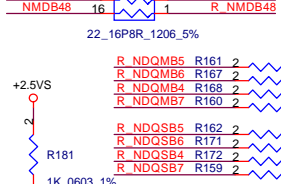


RP18
1 16 R_NMDB40
2 15 R_NMDB41
3 14 R_NMDB42
4 13 R_NMDB43
5 12 R_NMDB44
6 11 R_NMDB45
7 10 R_NMDB46
8 9 R_NMDB47

22_16P8R_1206_5%

RP22
1 8 R_NMDB55
2 7 R_NMDB54
3 6 R_NMDB53
4 5 R_NMDB52
5 4 R_NMDB51
6 3 R_NMDB50
7 2 R_NMDB49
8 1 R_NMDB48

22_16P8R_1206_5%

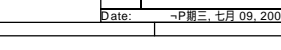
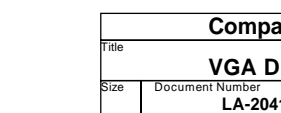
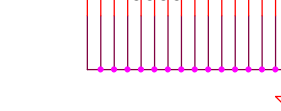
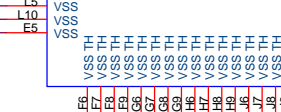


RP18
1 16 R_NMDB40
2 15 R_NMDB41
3 14 R_NMDB42
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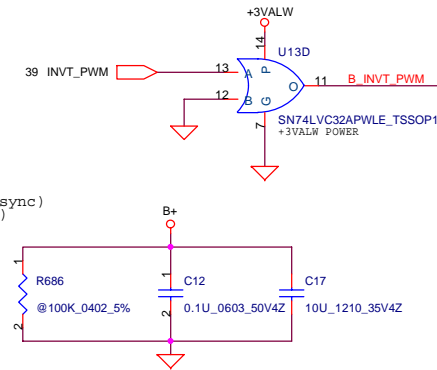
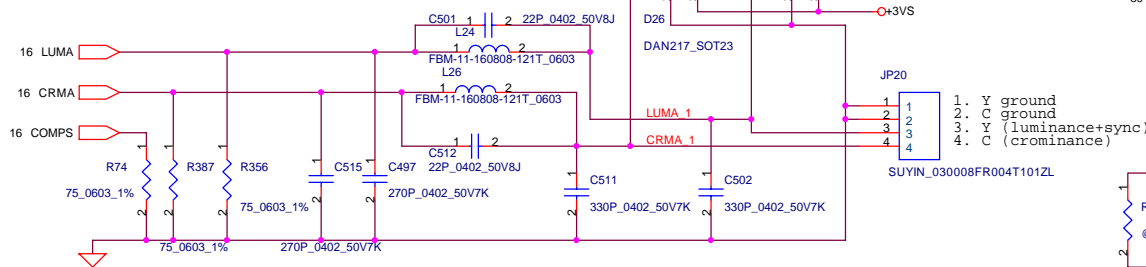
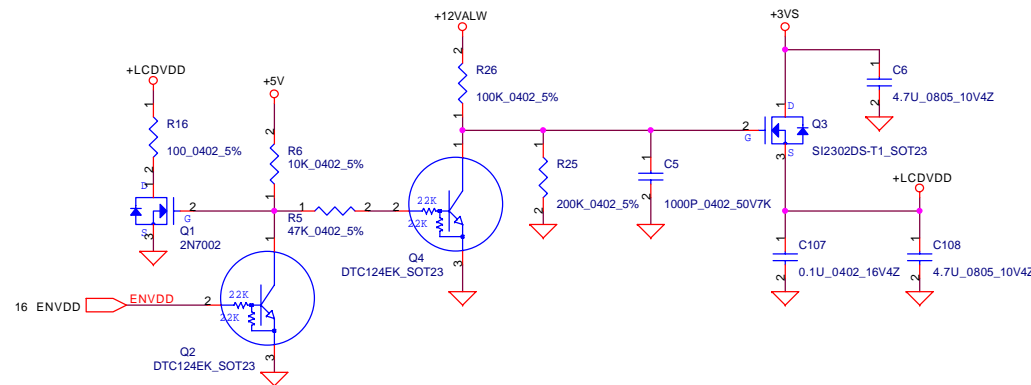
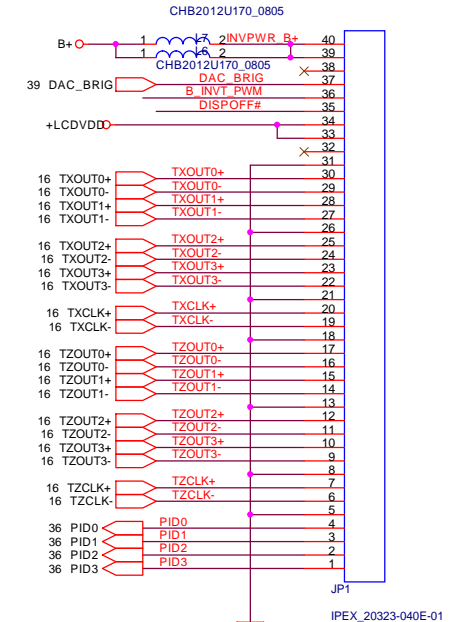
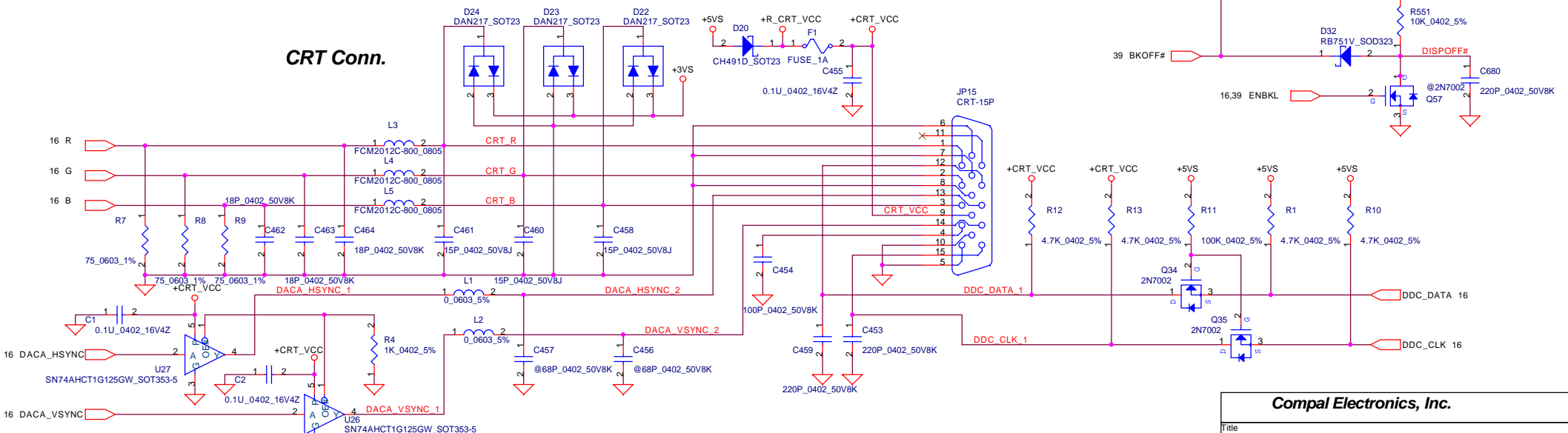
22_16P8R_1206_5%

RP22
1 8 R_NMDB55
2 7 R_NMDB54
3 6 R_NMDB53
4 5 R_NMDB52
5 4 R_NMDB51
6 3 R_NMDB50
7 2 R_NMDB49
8 1 R_NMDB48

22_16P8R_1206_5%



CRT, TV-OUT & LVDS CONNECTOR

TV-OUT Conn.**LVDS Conn.****CRT Conn.**

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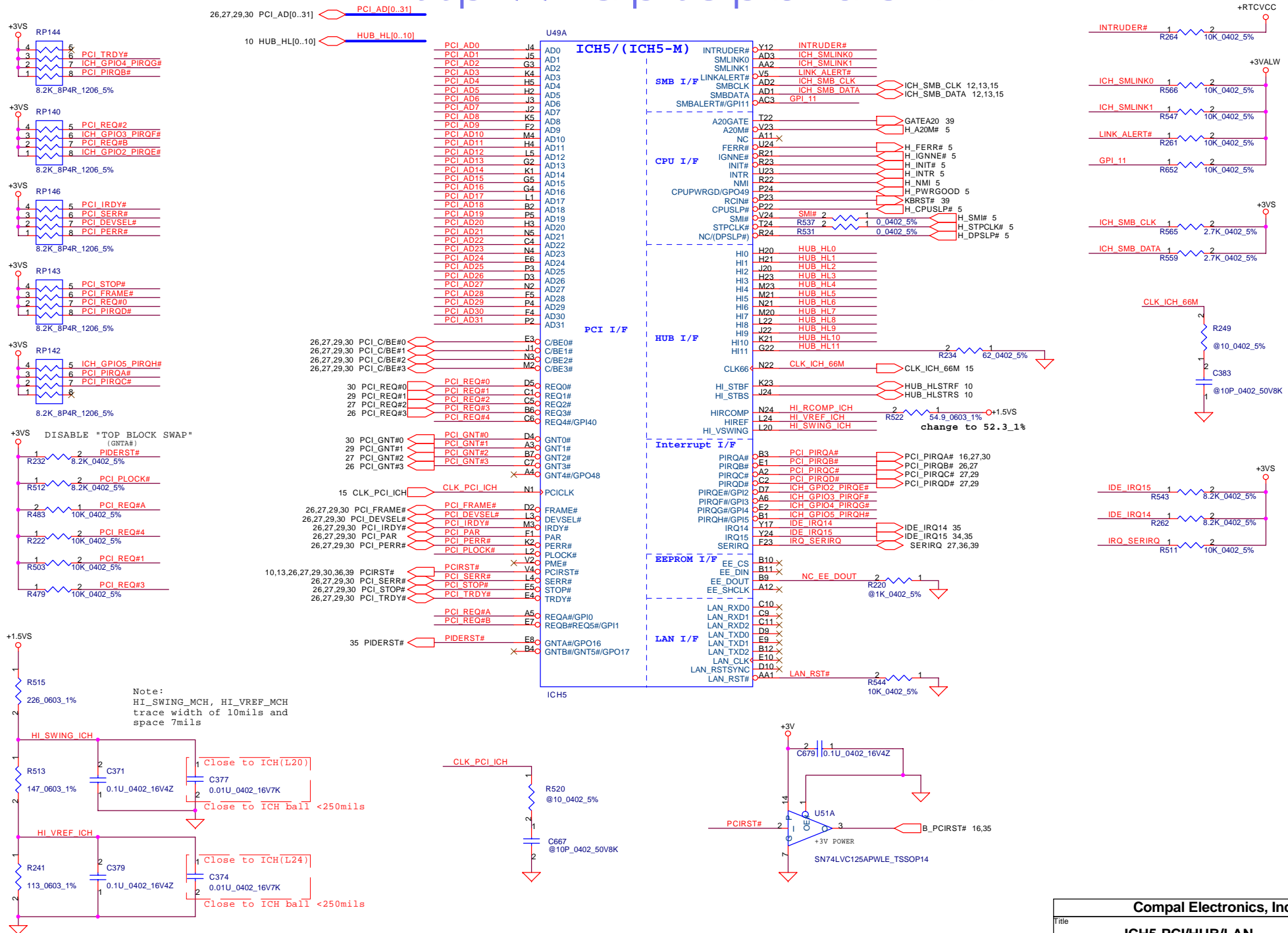
CRT,TV-OUT & LVDS Connector

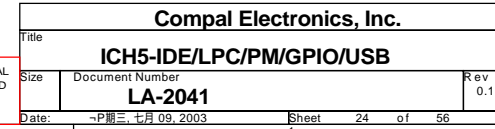
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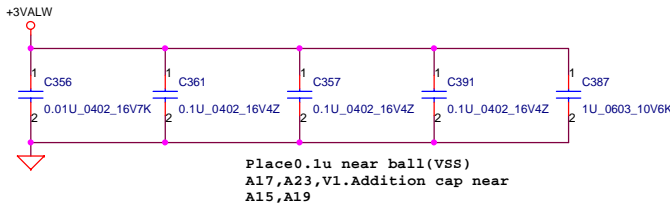
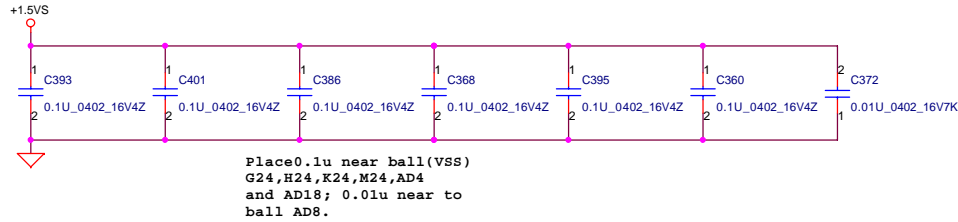
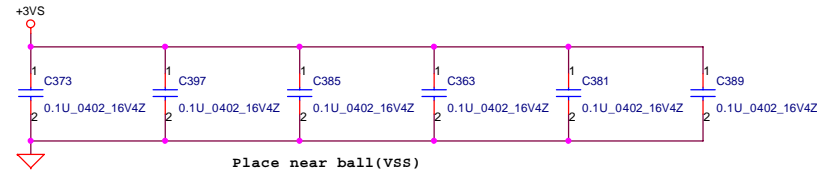
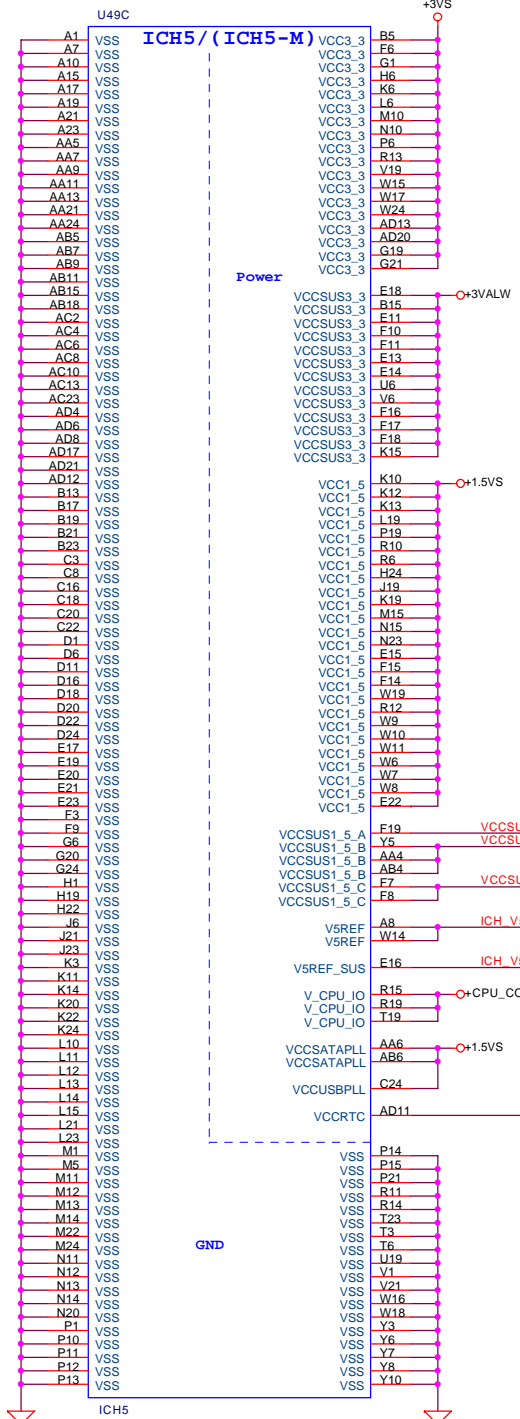
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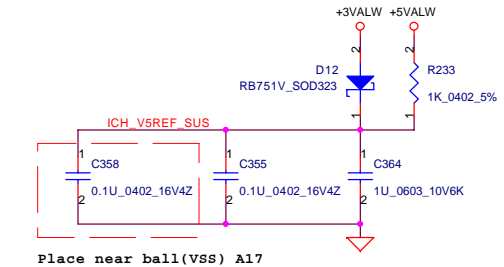
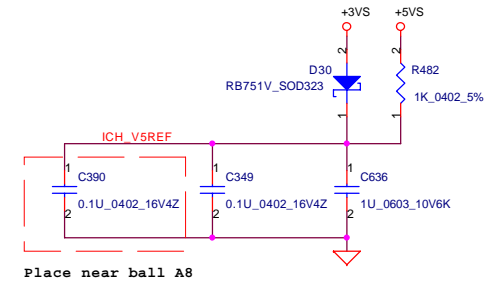
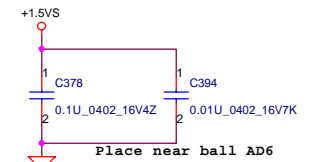
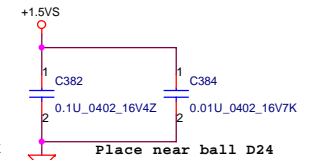
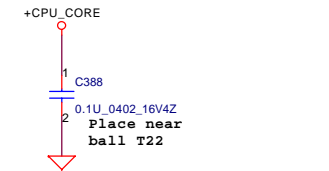
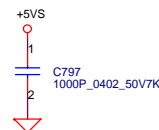
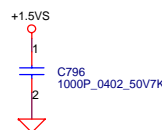
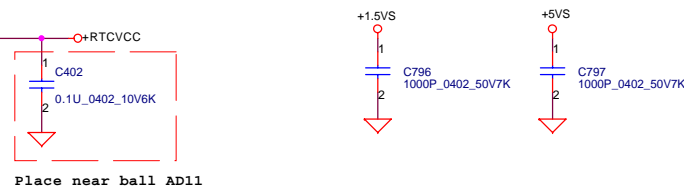
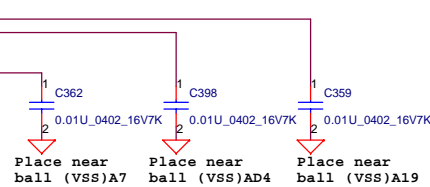
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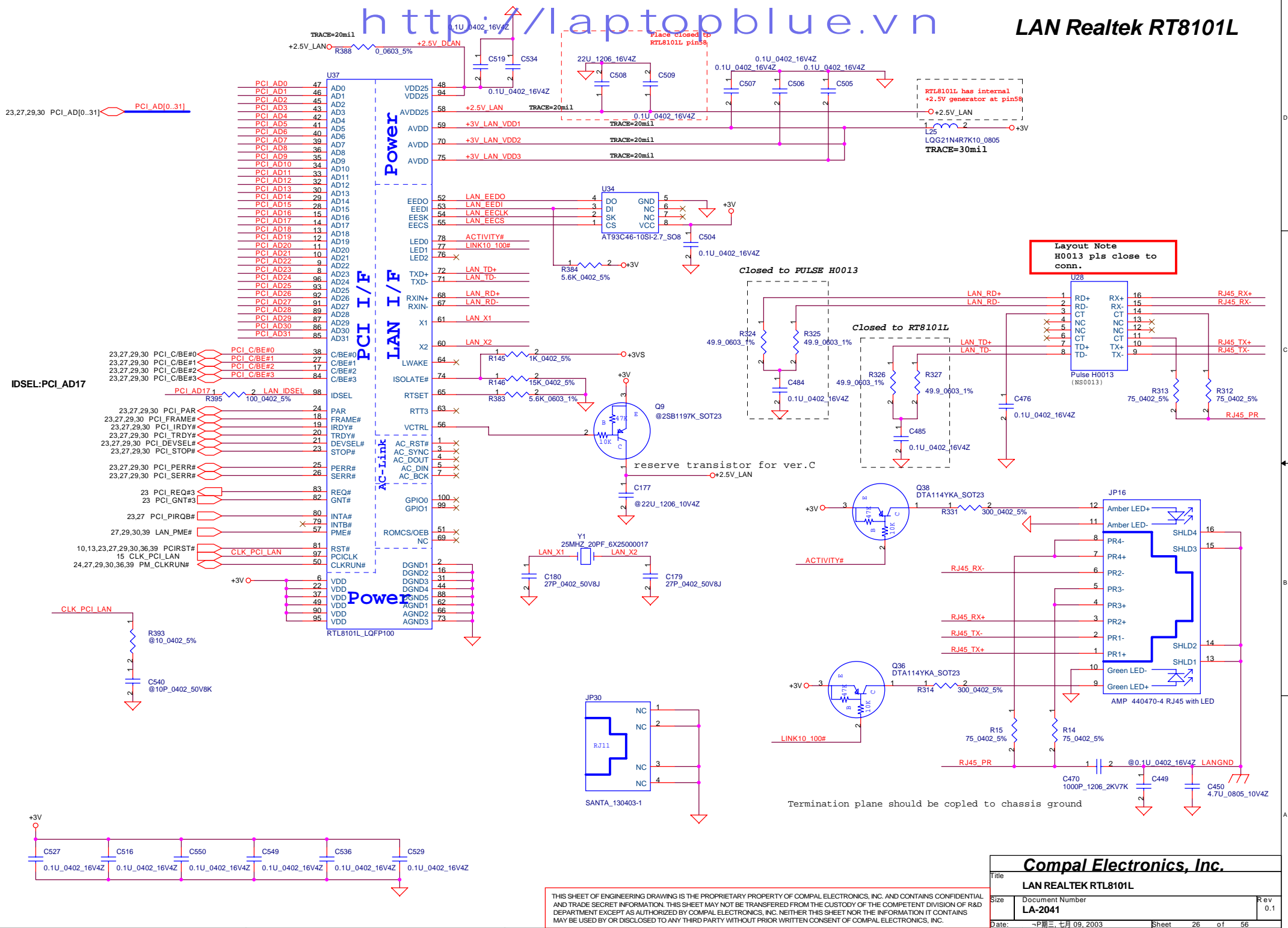




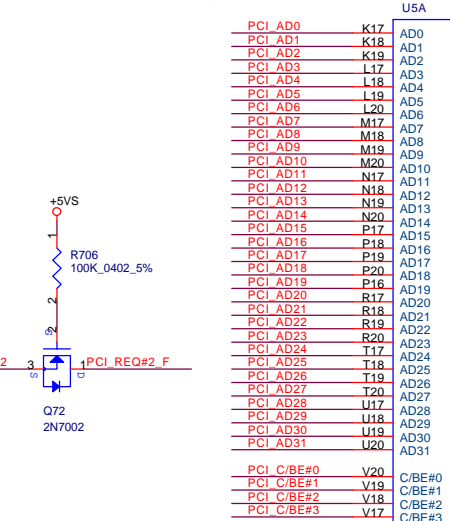


Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)page278

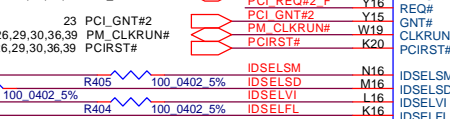




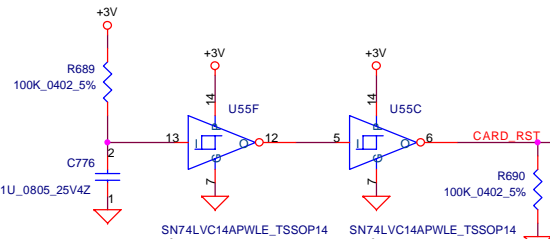
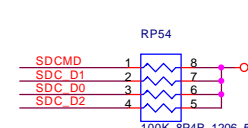
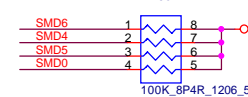
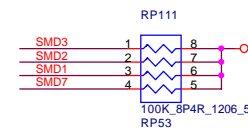
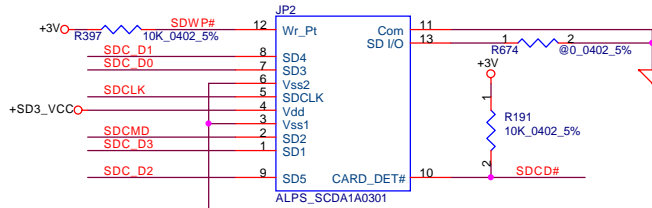
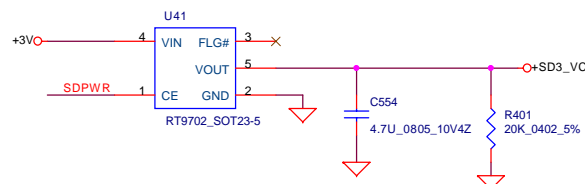
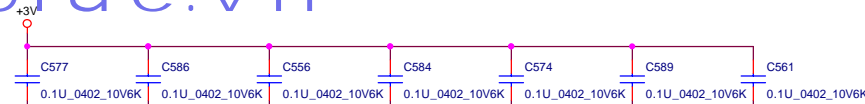
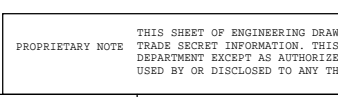
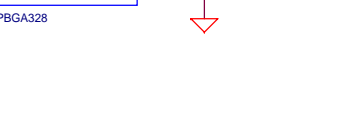
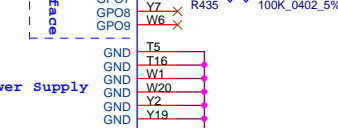
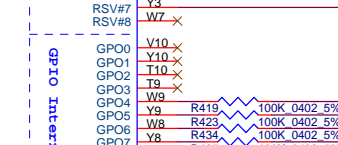
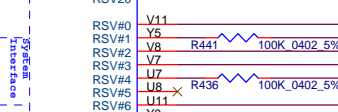
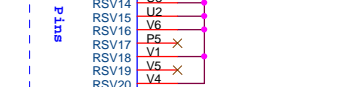
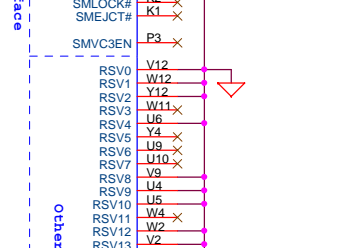
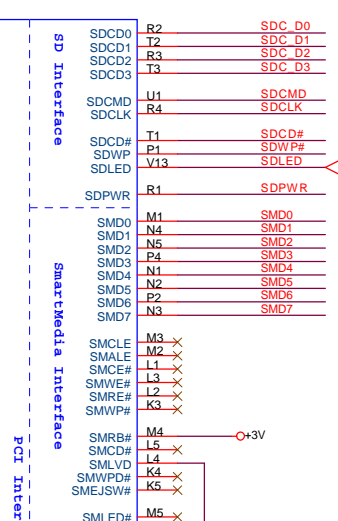
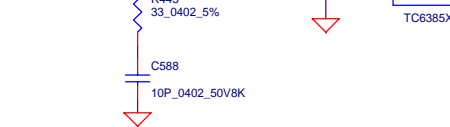
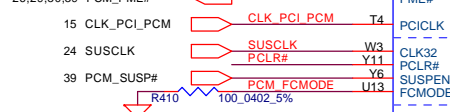
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23,26,29,30 PCI_C/BE#[3..0]



23,26,29,30 PCI_PAR
23,26,29,30 PCI_PERR#
23,26,29,30 PCI_SERR#
23,26,29,30 PCI_FRAME#
23,26,29,30 PCI_IRDY#
23,26,29,30 PCI_TRDY#
23,26,29,30 PCI_STOP#
23,26,29,30 PCI_DEVSEL#
23 PCI_GNT#2
24,26,29,30,36,39 PM_CLKRUN#
10,13,23,26,29,30,36,39 PCIRST#



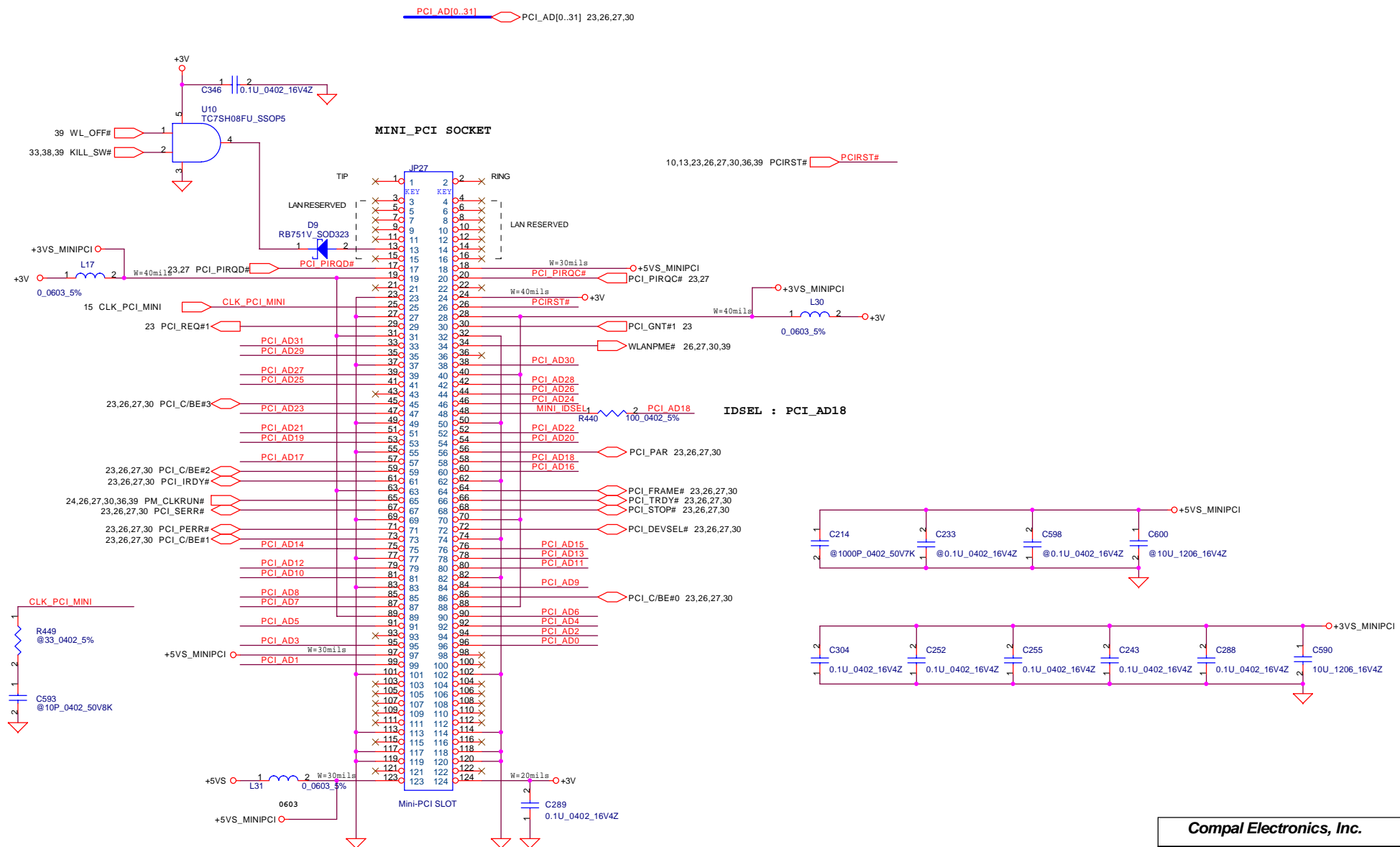
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16,23,30 PCI_PIRQA#
23,26 PCI_PIRQB#
23,29 PCI_PIRQC#
23,29 PCI_PIRQD#
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15 CLK_PCI_PCM
24 SUSCLK
39 PCM_SUSP#



Compal Electronics, Inc.

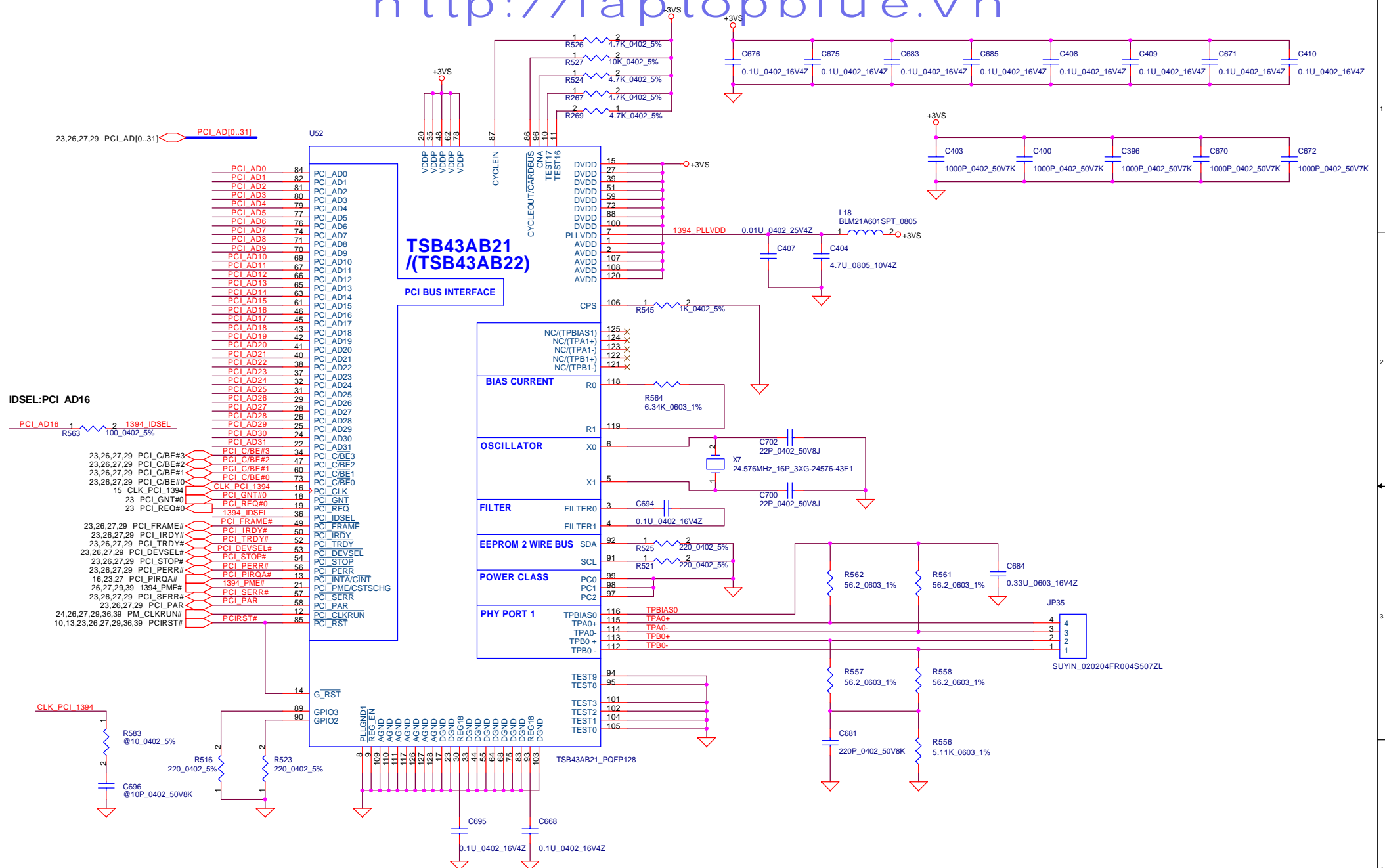
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CARDBUS & SD CONN (1/2)			
Size	Document Number		Rev
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Date	~P期三, 七月 09, 2003		Sheet 27 of 56

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h t t p : / / l a p t o p b l u e . v n



Compal Electronics, Inc.

Title

1394 Interface

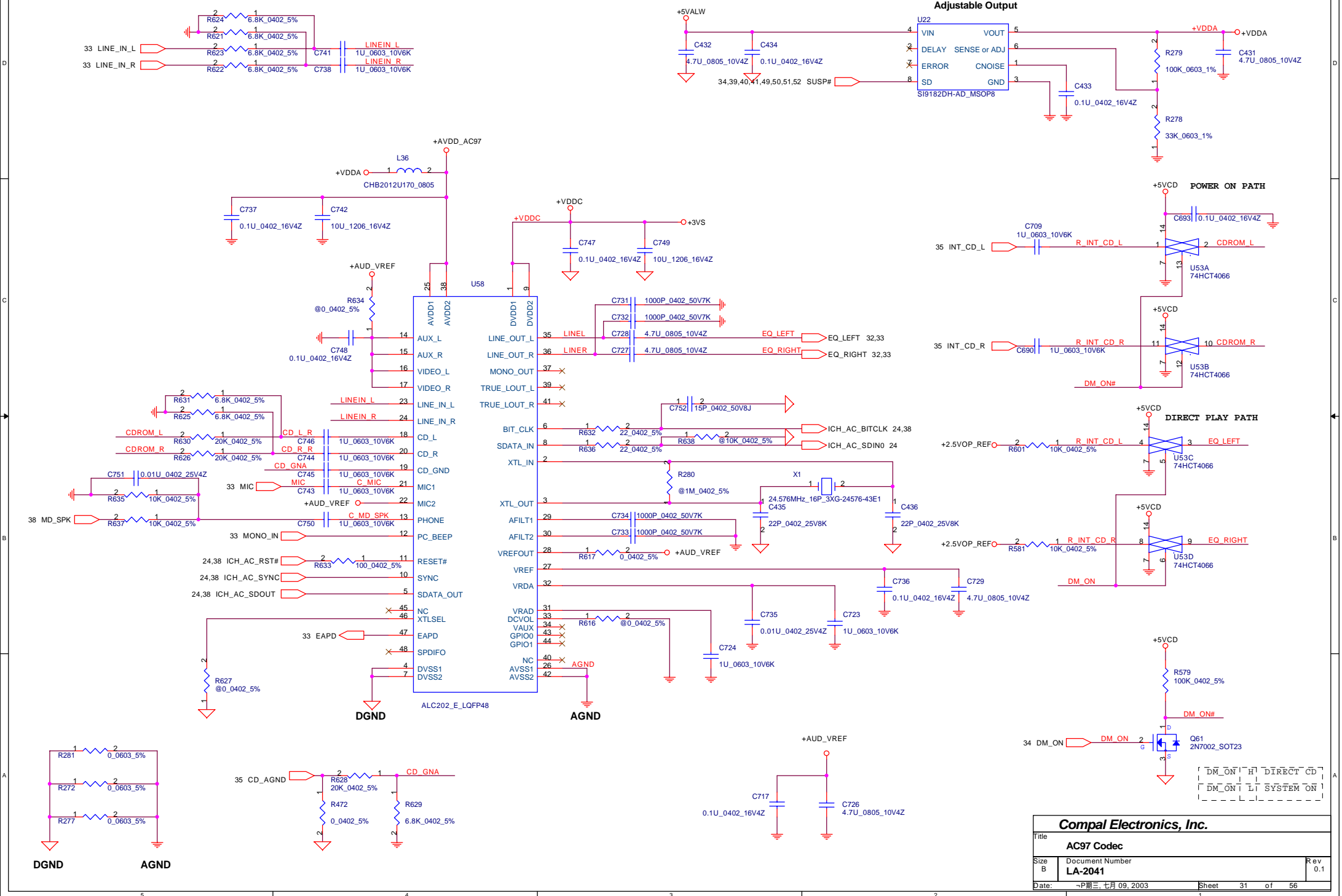
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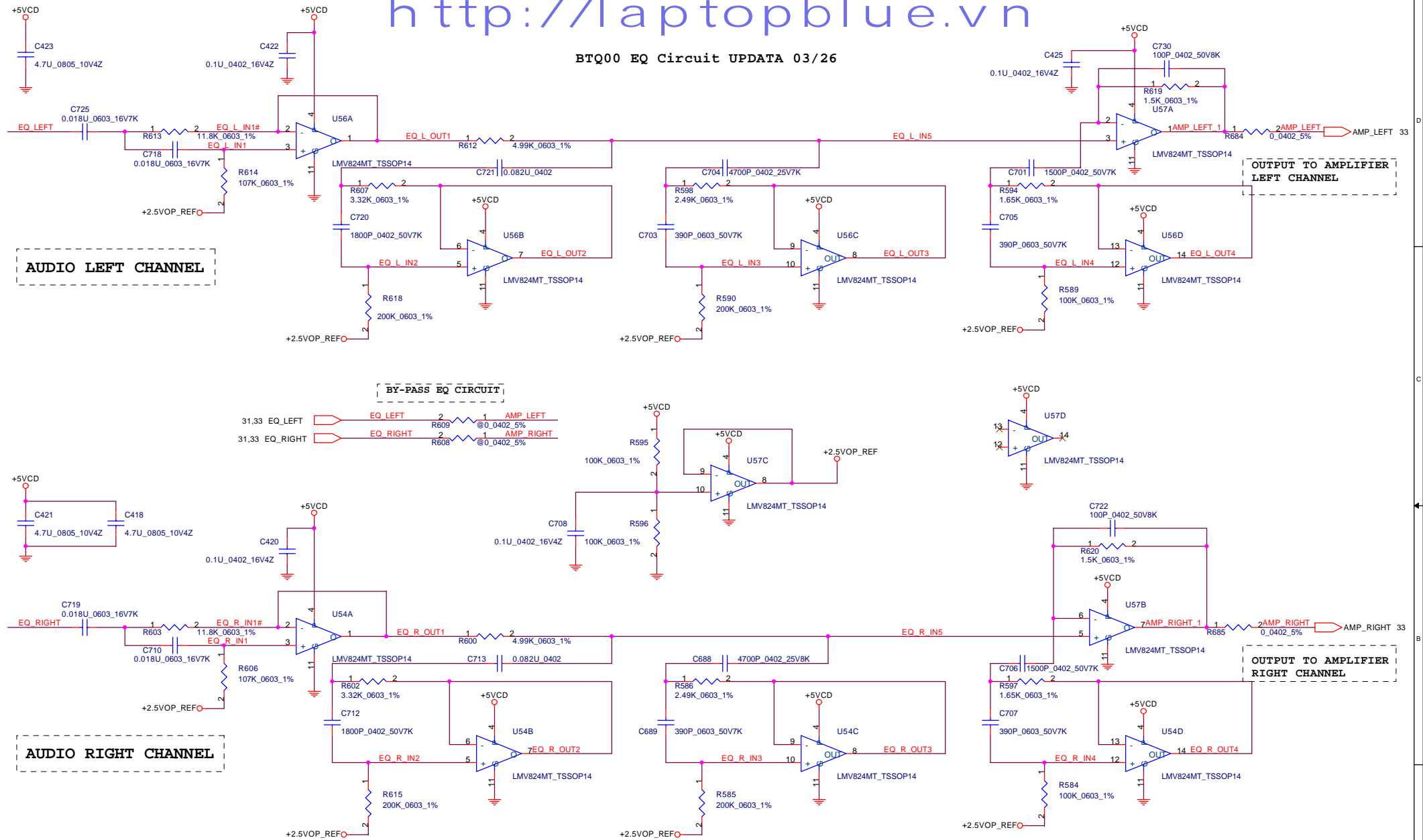
Sheet 30 of 56



Compal Electronics, Inc.

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Size	Document Number	Rev	
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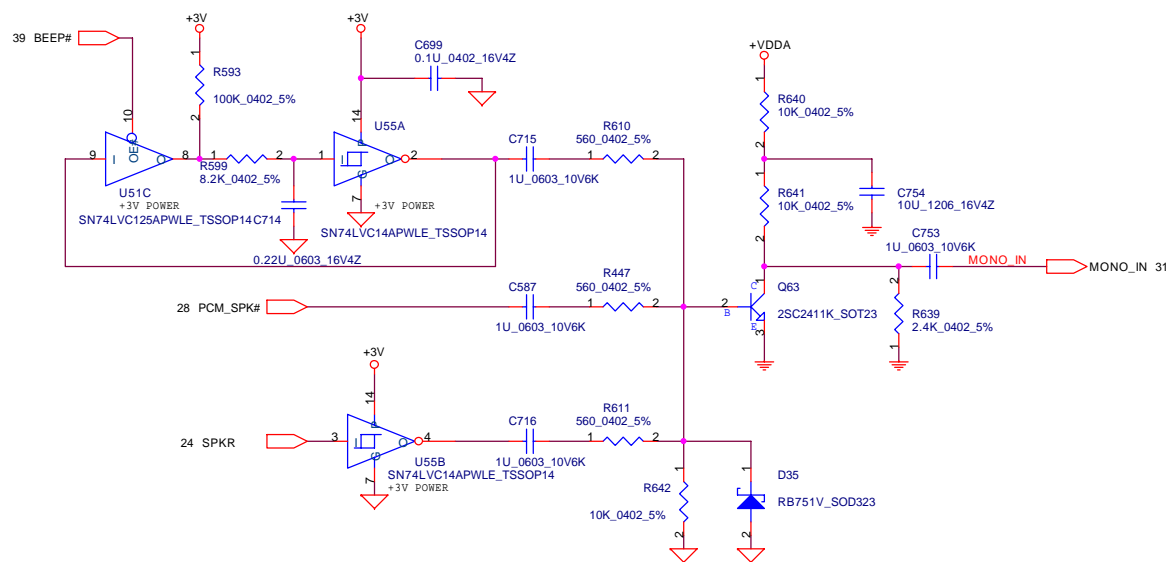
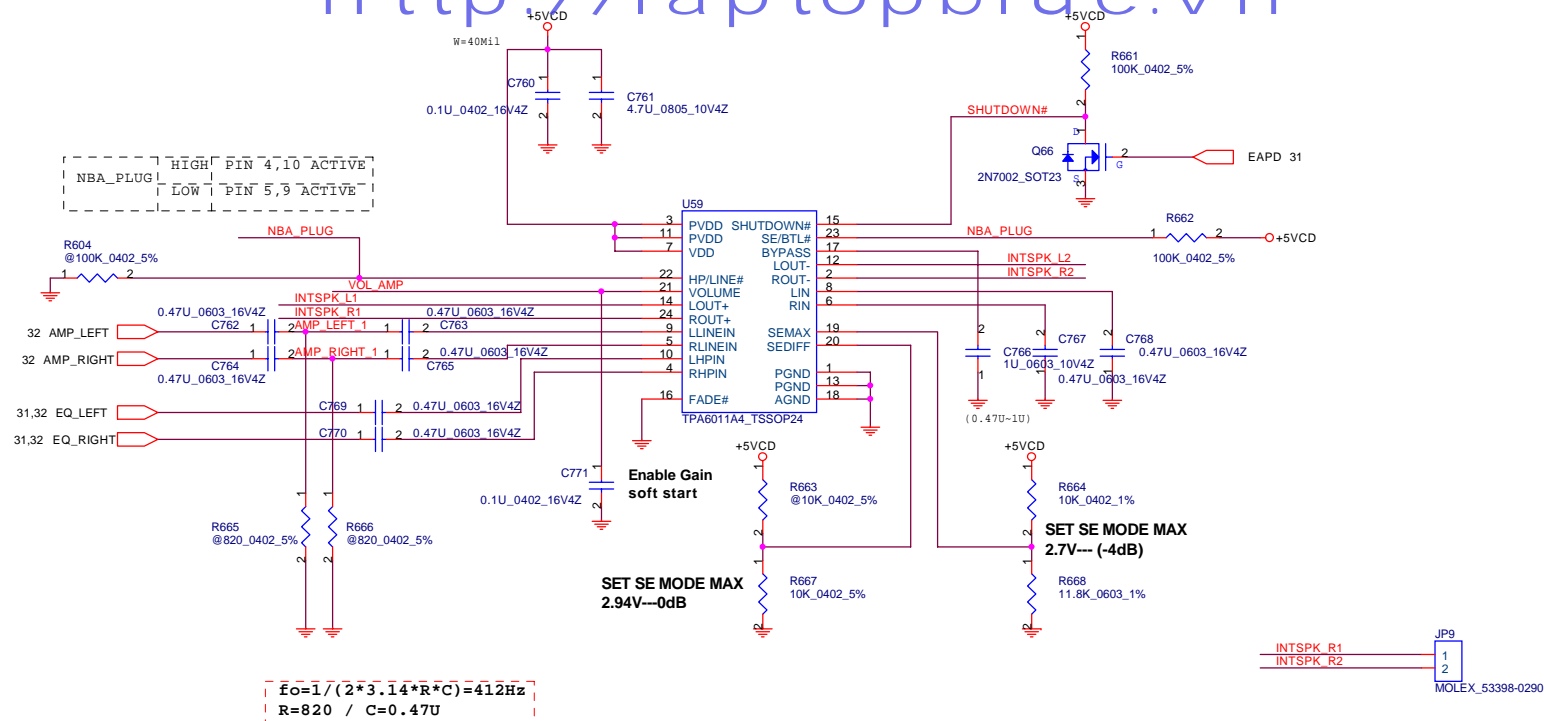
BTQ00 EQ Circuit UPDATA 03/26



Compal Electronics, Inc.

Title			HAREWARE EQ
Size	Document Number	Rev	
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Date:	~P 星期三, 七月 09, 2003	Sheet	32 of 56

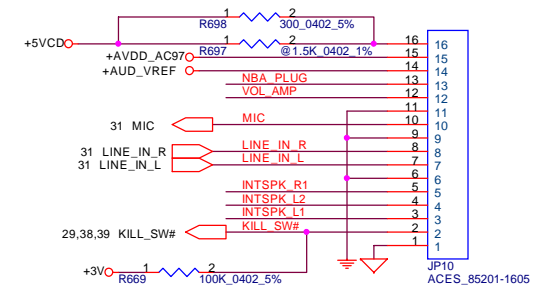
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AUDIO Board Conn.

R697(1.5K)-----10dB

R698(300)-----14dB



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Compal Electronics, Inc.

Title	AMP & Audio Jack
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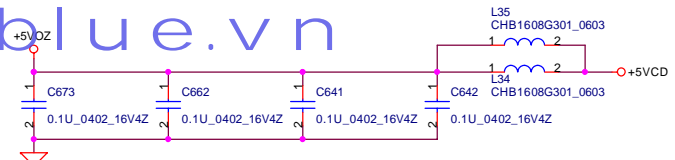
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Date: 7月09日, 星期三

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0.1	

35 CDD[0..15] \leftarrow CDD[0..15]



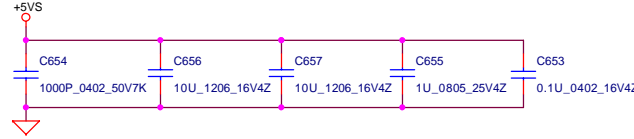
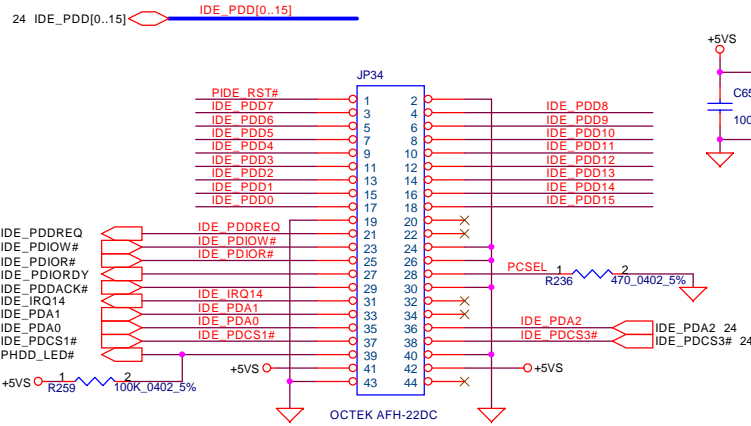
Compal Electronics, Inc.

Title		OZ-168 CD_PLAY	
Size	Document Number	Rev	
B	LA-2041	0.1	
Date:	~P 星期三, 七月 09, 2003	Sheet	34 of 56

HDD CONNECTOR

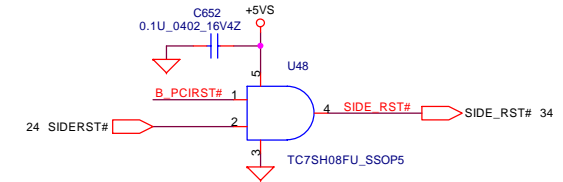
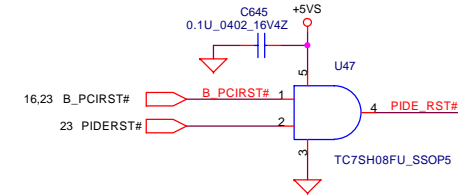
http://laptopblue.vn

IDE,CD-ROM Module CONN.

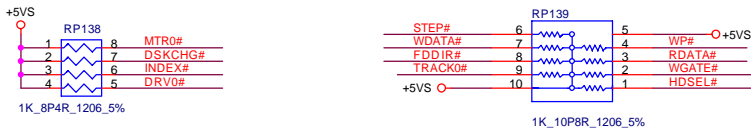
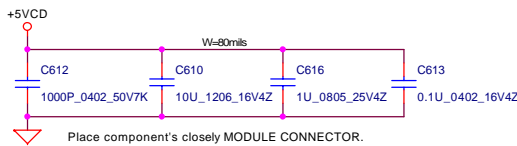
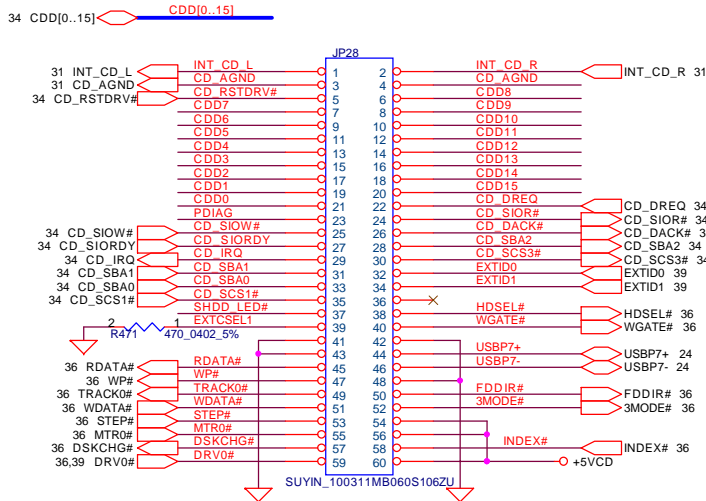


EXTID1	EXTID0	Module
0	0	CDROM
0	1	FDD
1	0	HDD
1	1	TV Tuner/No Module

EXTID3	EXTID2	Module
0	0	CDROM
0	1	FDD
1	0	HDD
1	1	TV Tuner/No Module

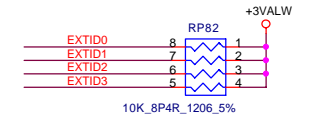
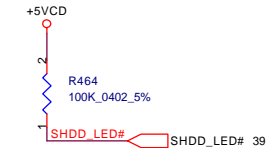
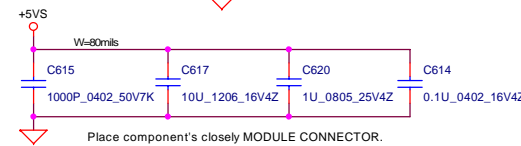
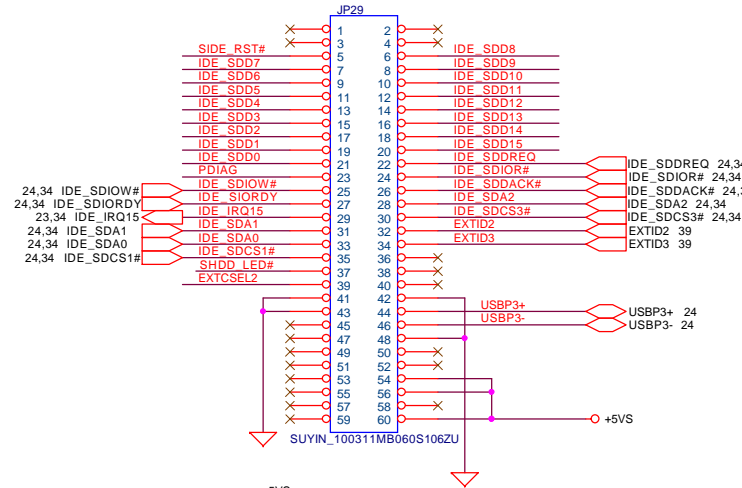


Main Module Conn. (Master)



2nd Module Conn. (Slave)

24,34 IDE_SDD[0..15] IDE_SDD[0..15]



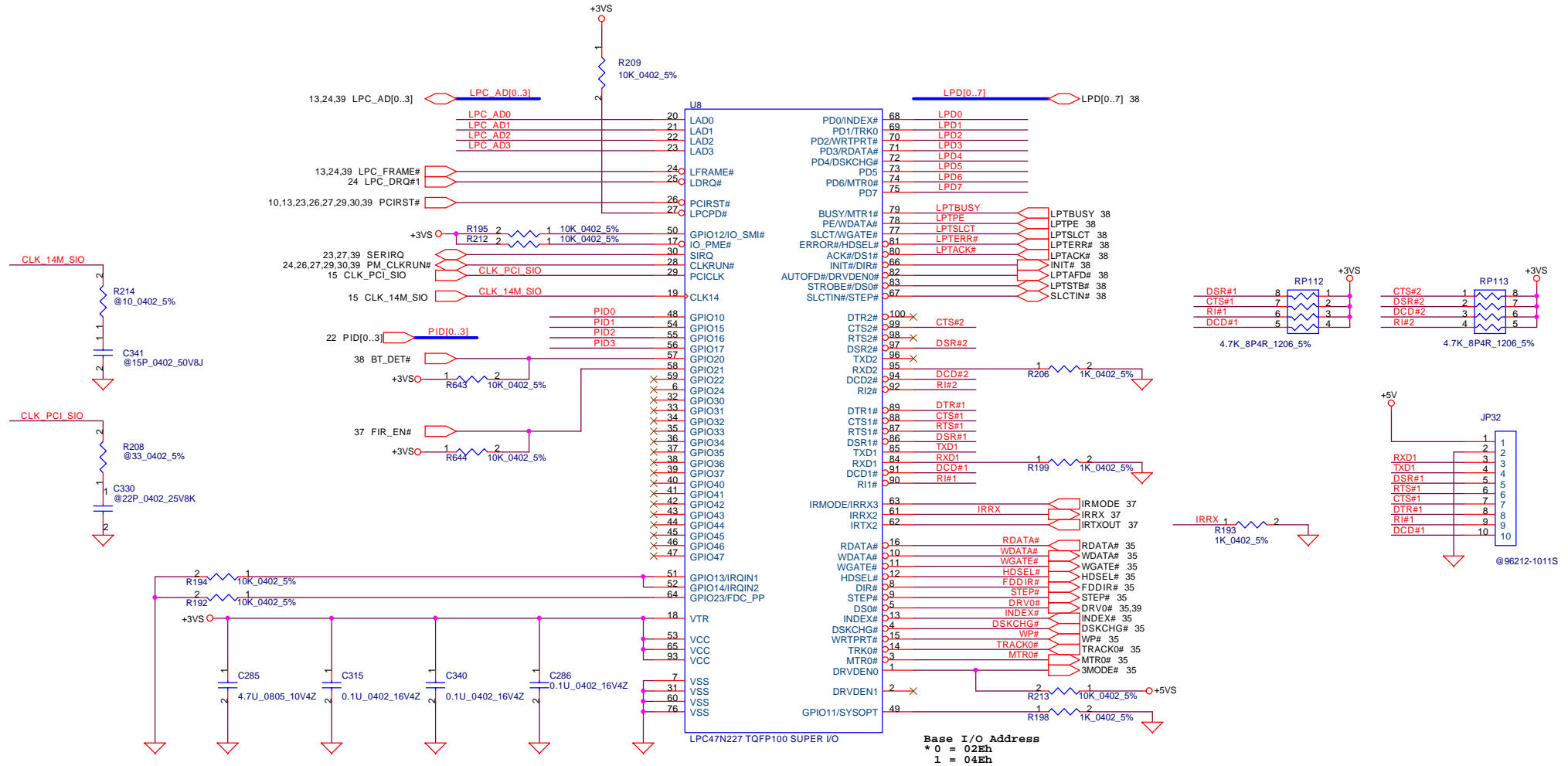
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IDE/FDD MODULE CONN.

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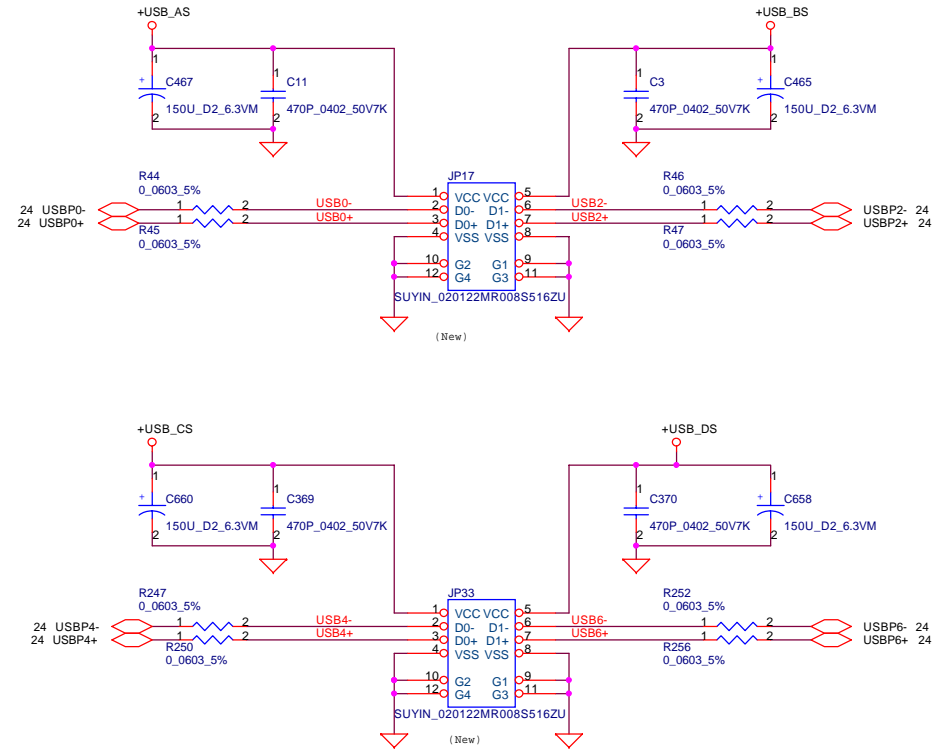
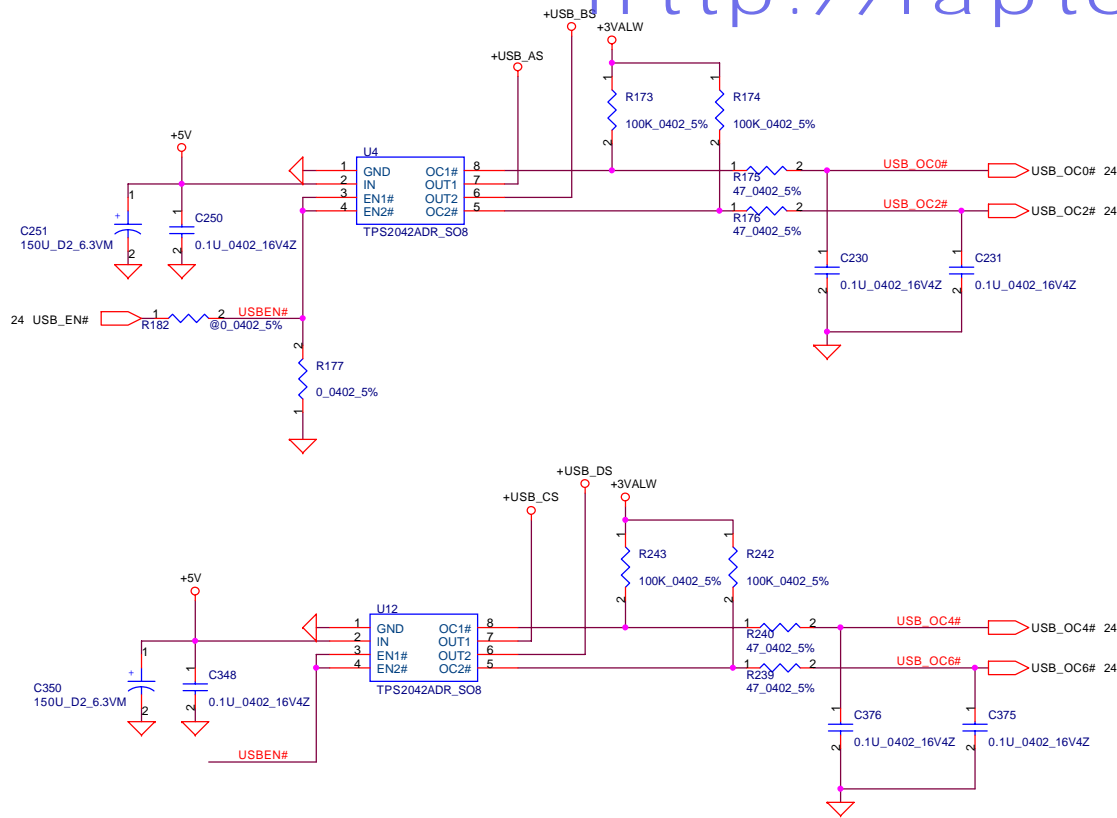
SUPER I/O SMC FDC47N227



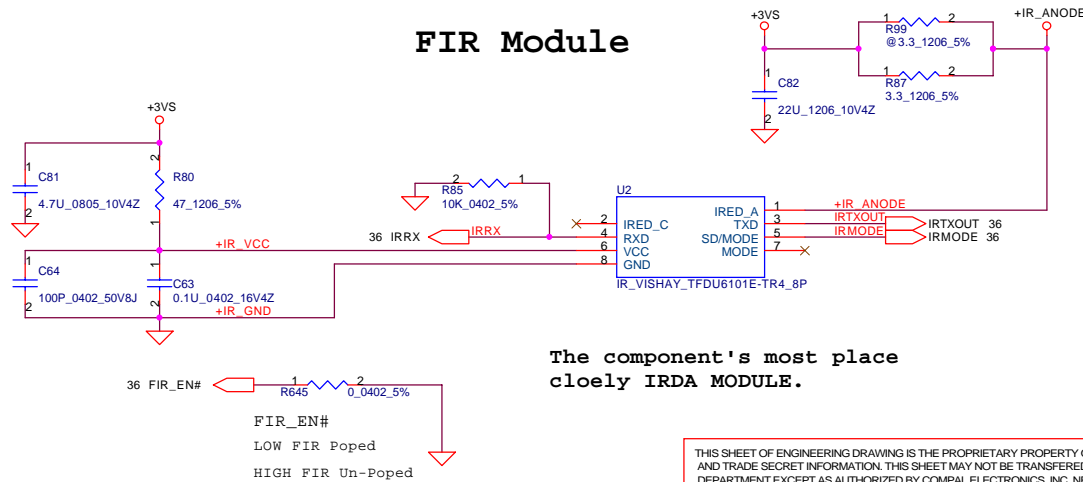
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Title		SUPER I/O	
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FIR Module



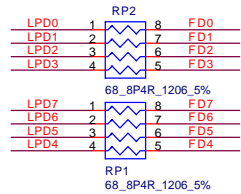
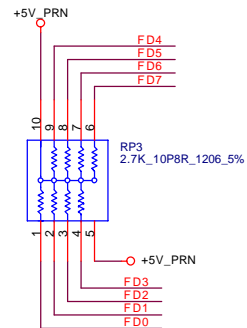
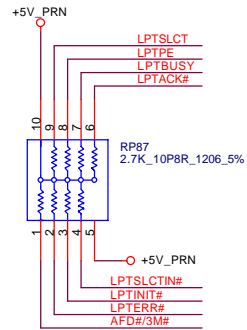
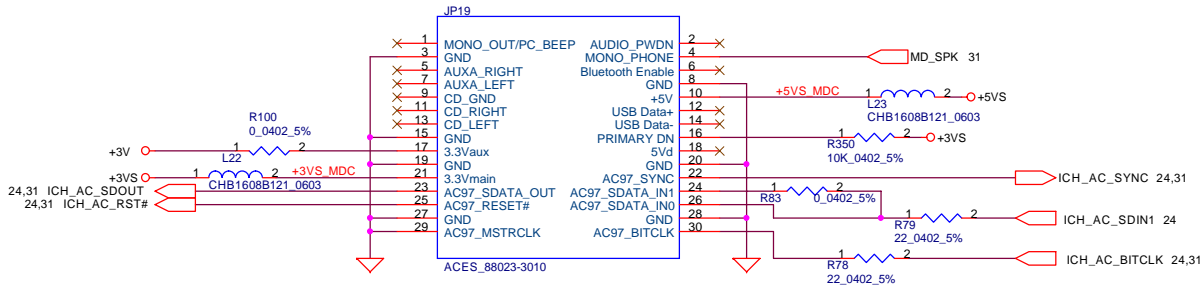
The component's most place
cloely IRDA MODULE.

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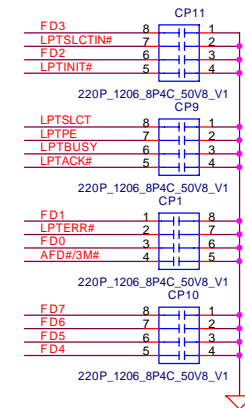
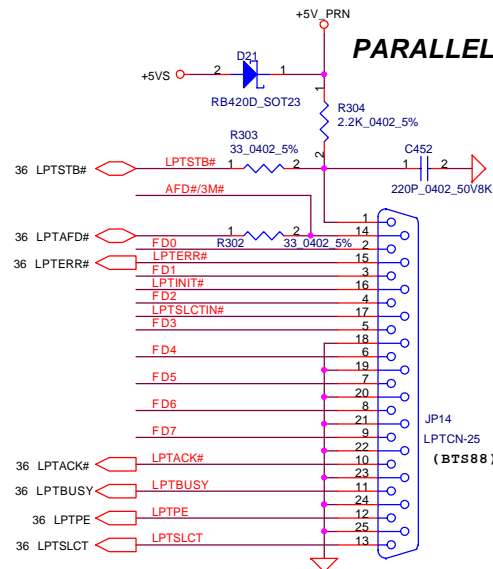
Compal Electronics, Inc.

Title			
USB Conn.			
Size B	Document Number	Rev	
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MDC CONN.



PARALLEL PORT



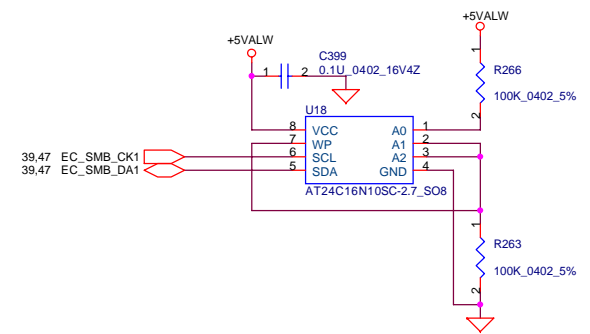
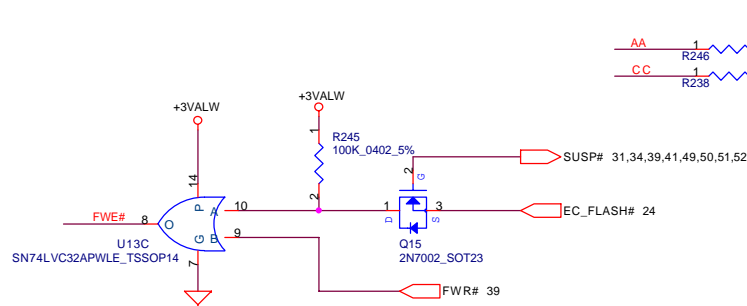
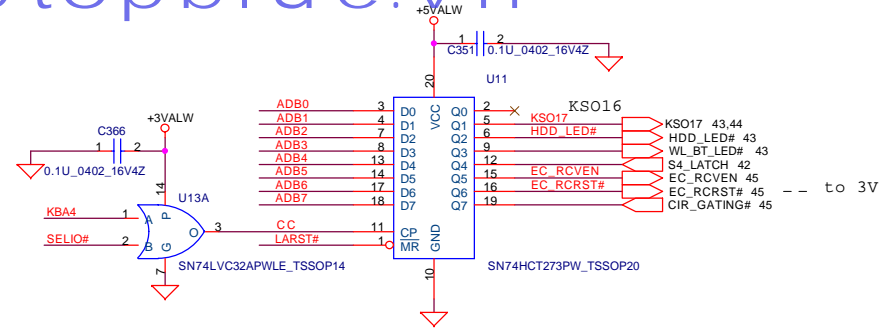
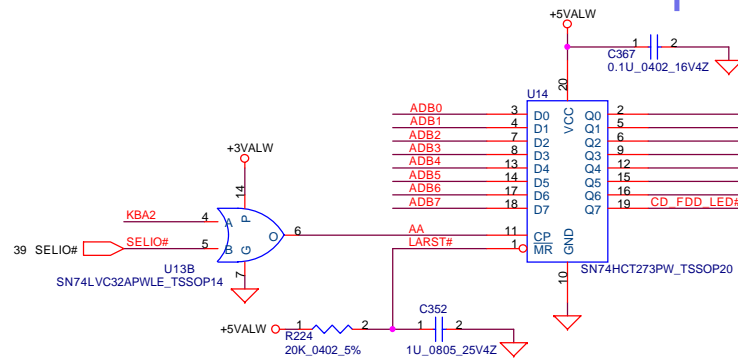
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PARALLEL/MDC PORT

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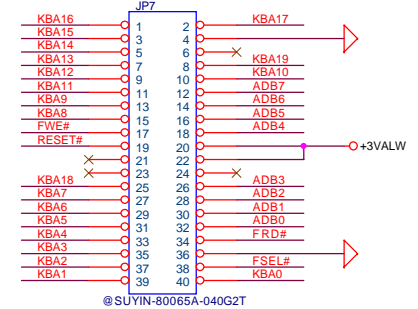
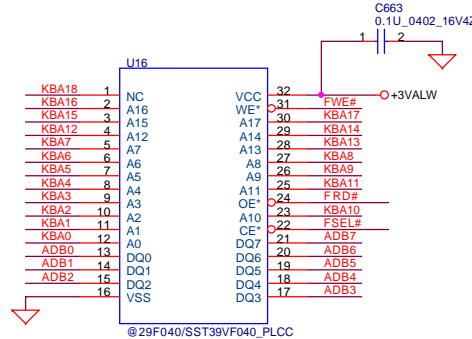
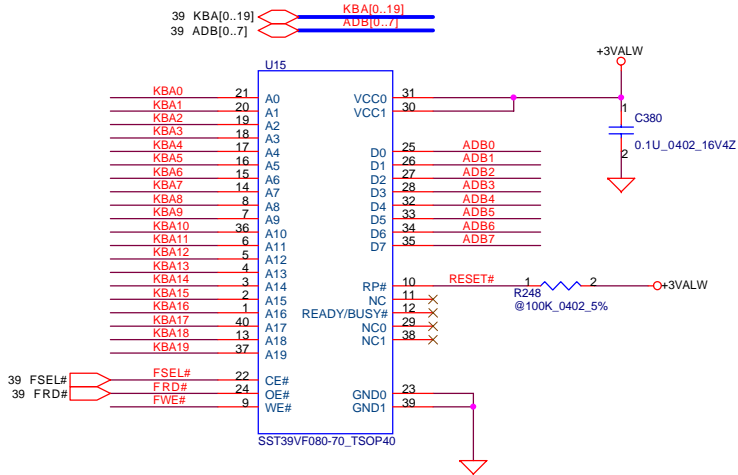




1MB Flash ROM

512KB Flash ROM

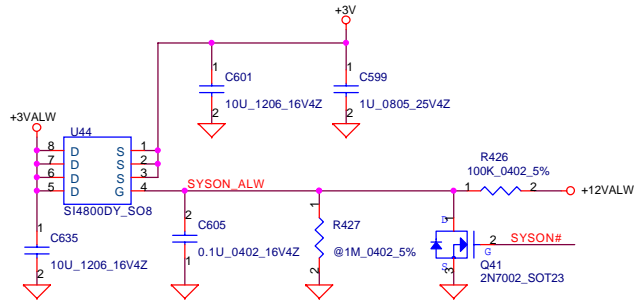
Flash ROM Socket Conn.



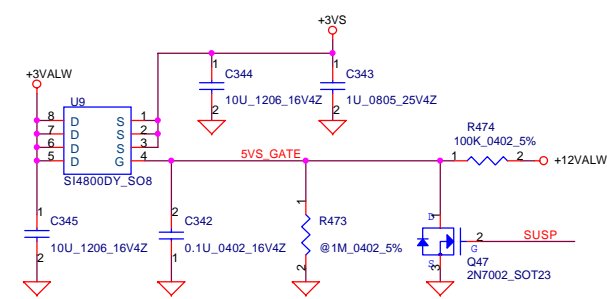
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Compal Electronics, Inc.			
Title			
BIOS & EXT. I/O PORT			
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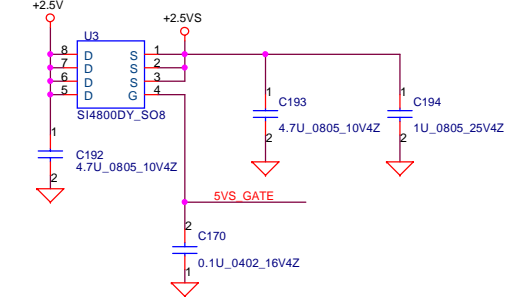
+3VALW TO +3V



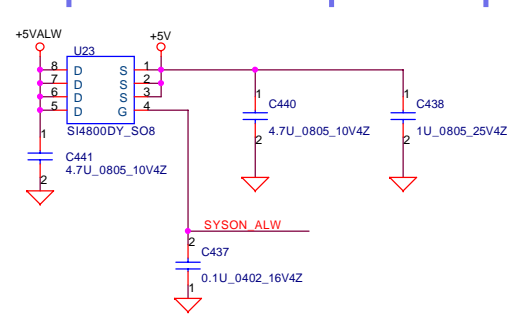
+3VALW TO +3VS



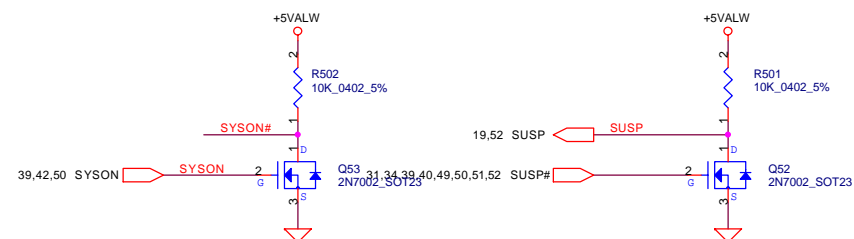
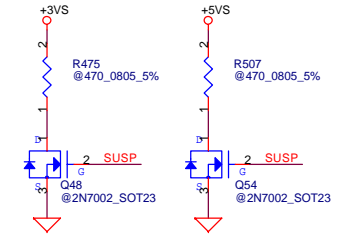
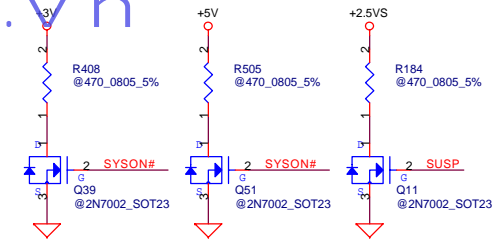
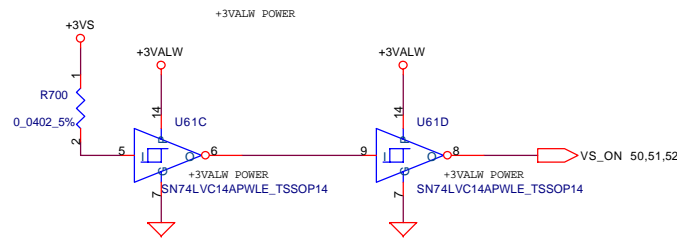
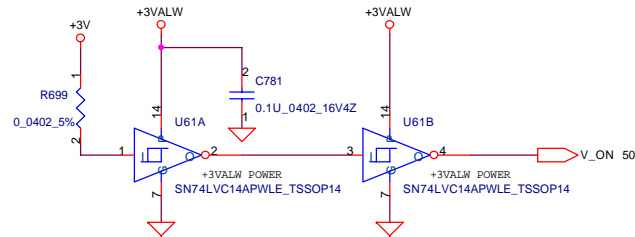
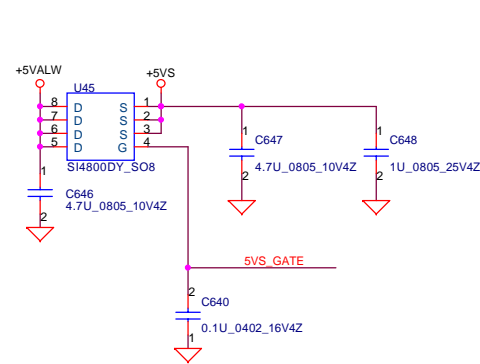
+2.5V TO +2.5VS



+5VALW TO +5V



+5VALW TO +5VS



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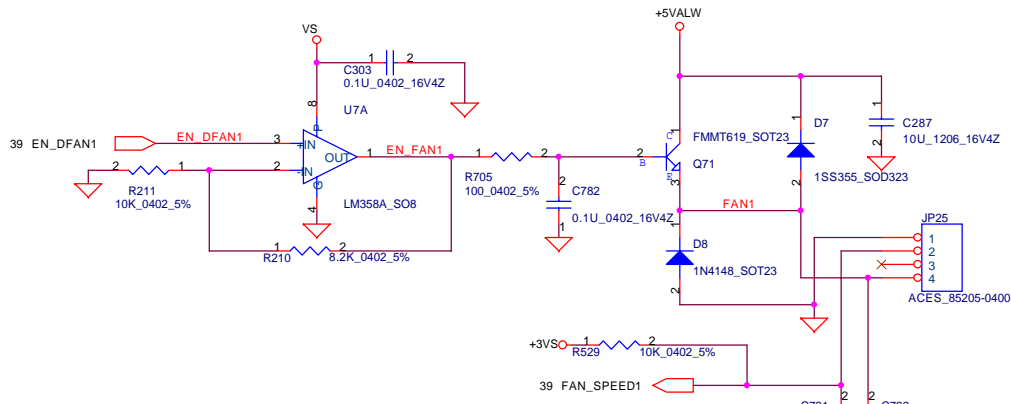
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Document Number LA-2041

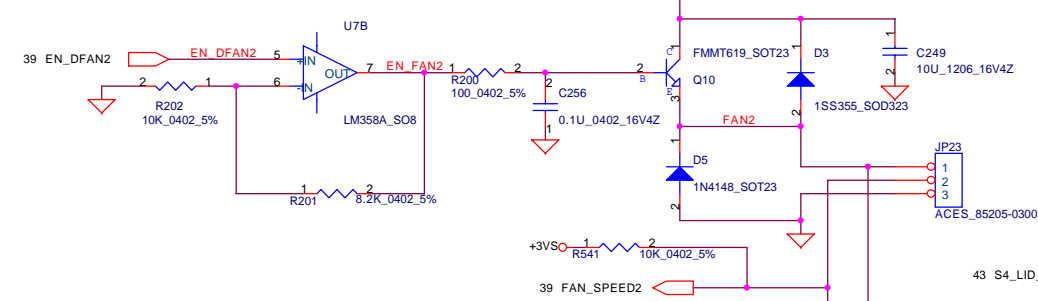
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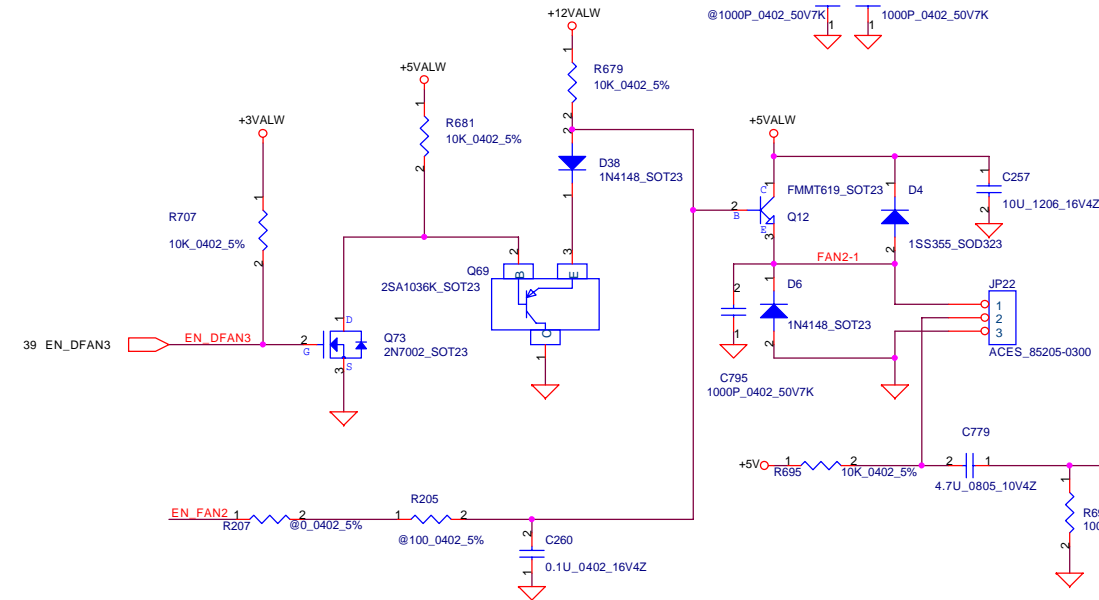
FAN CONN. 1



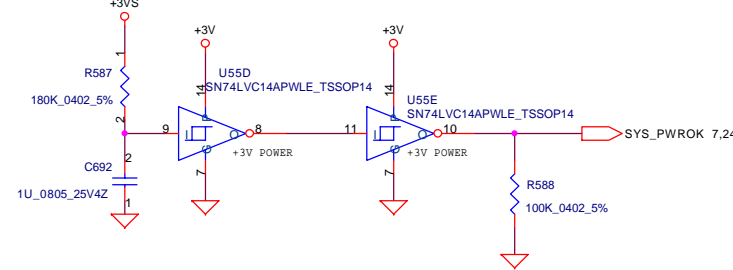
FAN CONN. 2



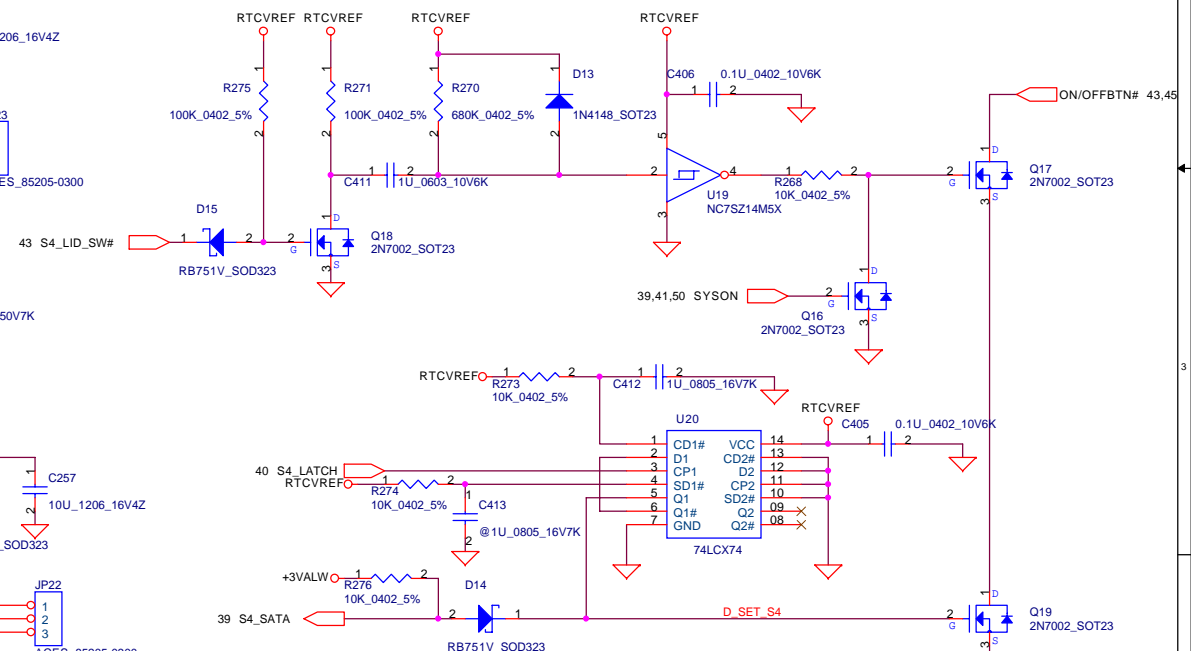
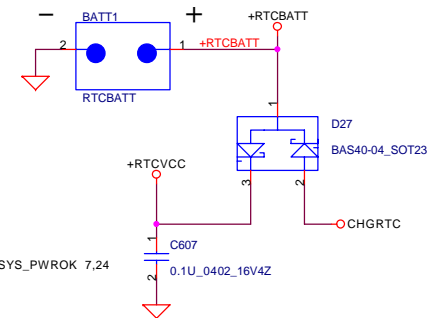
FAN CONN. 3



Power ON Circuit



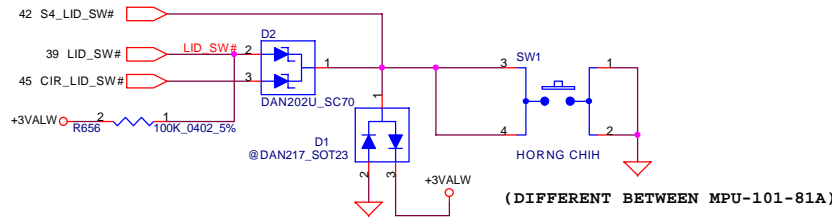
RTC Battery



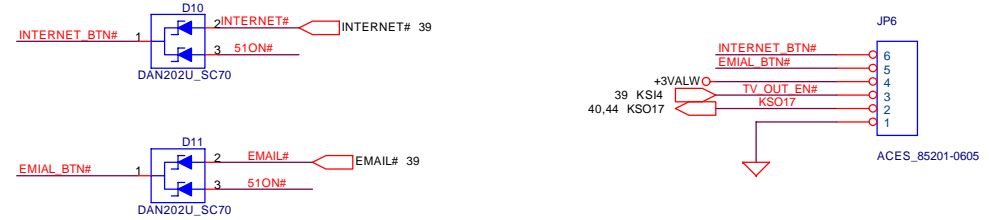
Compal Electronics, Inc.

Title		
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Size	Document Number	Rev
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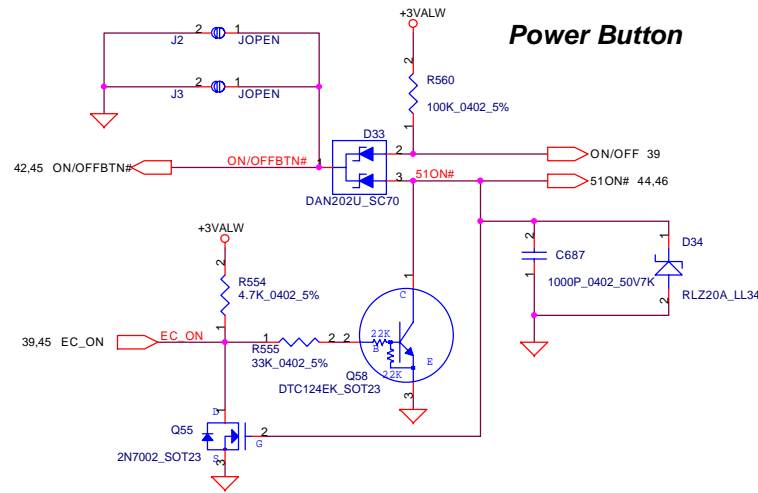
LID Switch



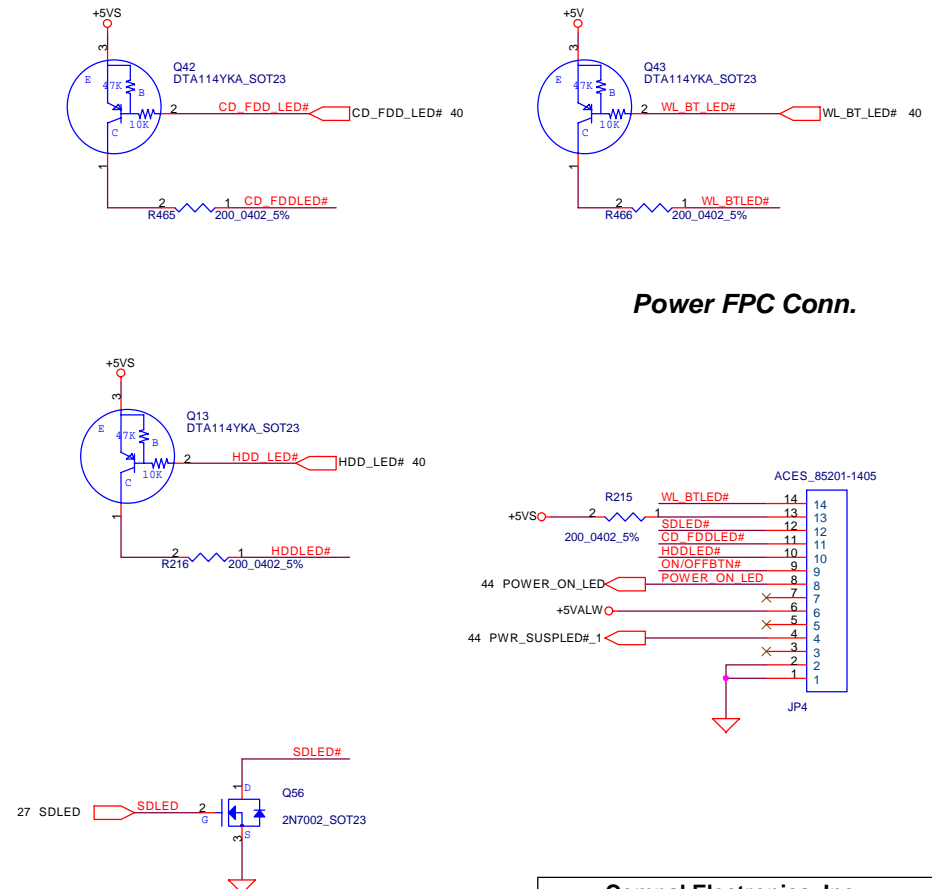
Button FPC Conn.



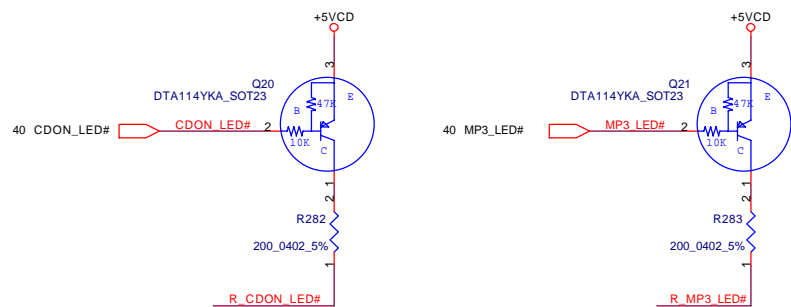
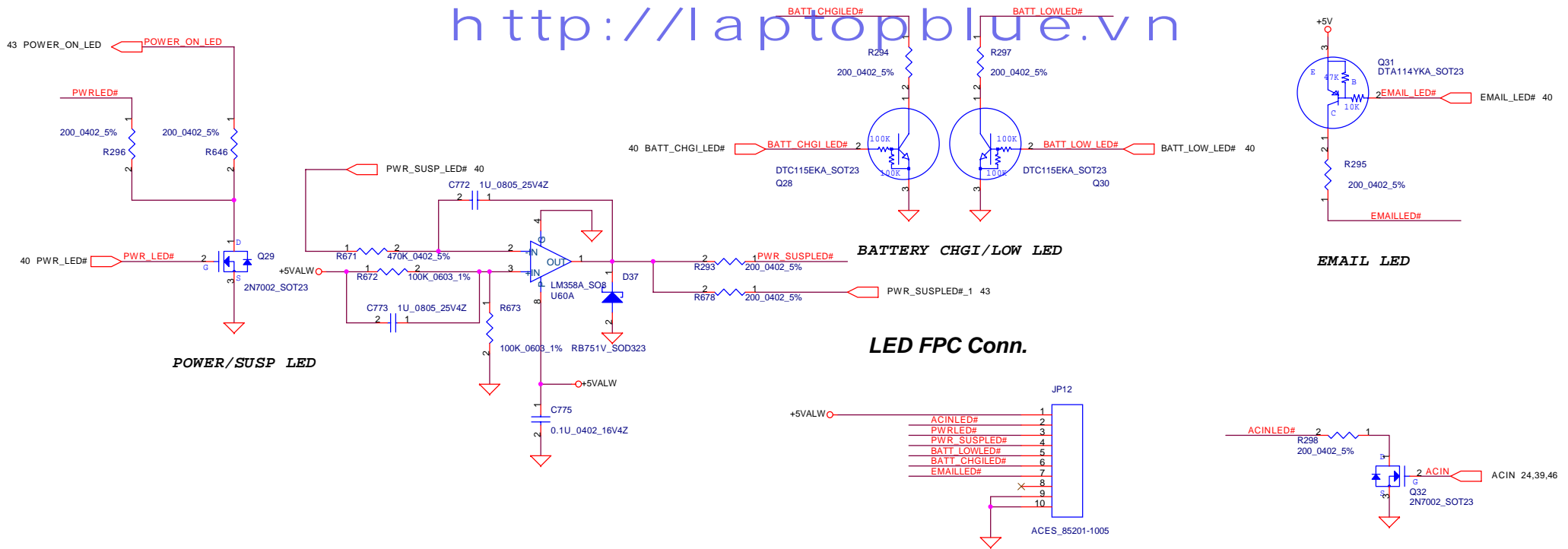
Power Button



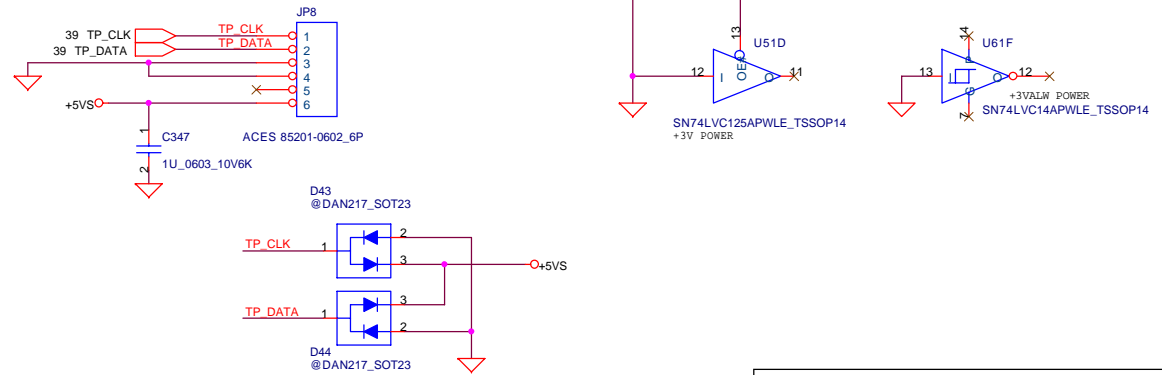
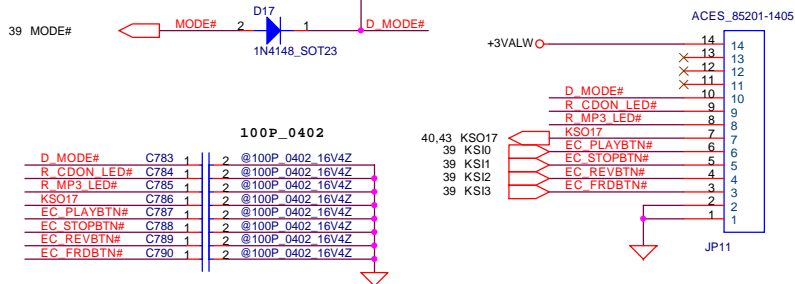
Power FPC Conn.



h t t p : / / l a p t o p b l u e . v n



Touch Pad Connector

**CDPLAY Board Conn.**

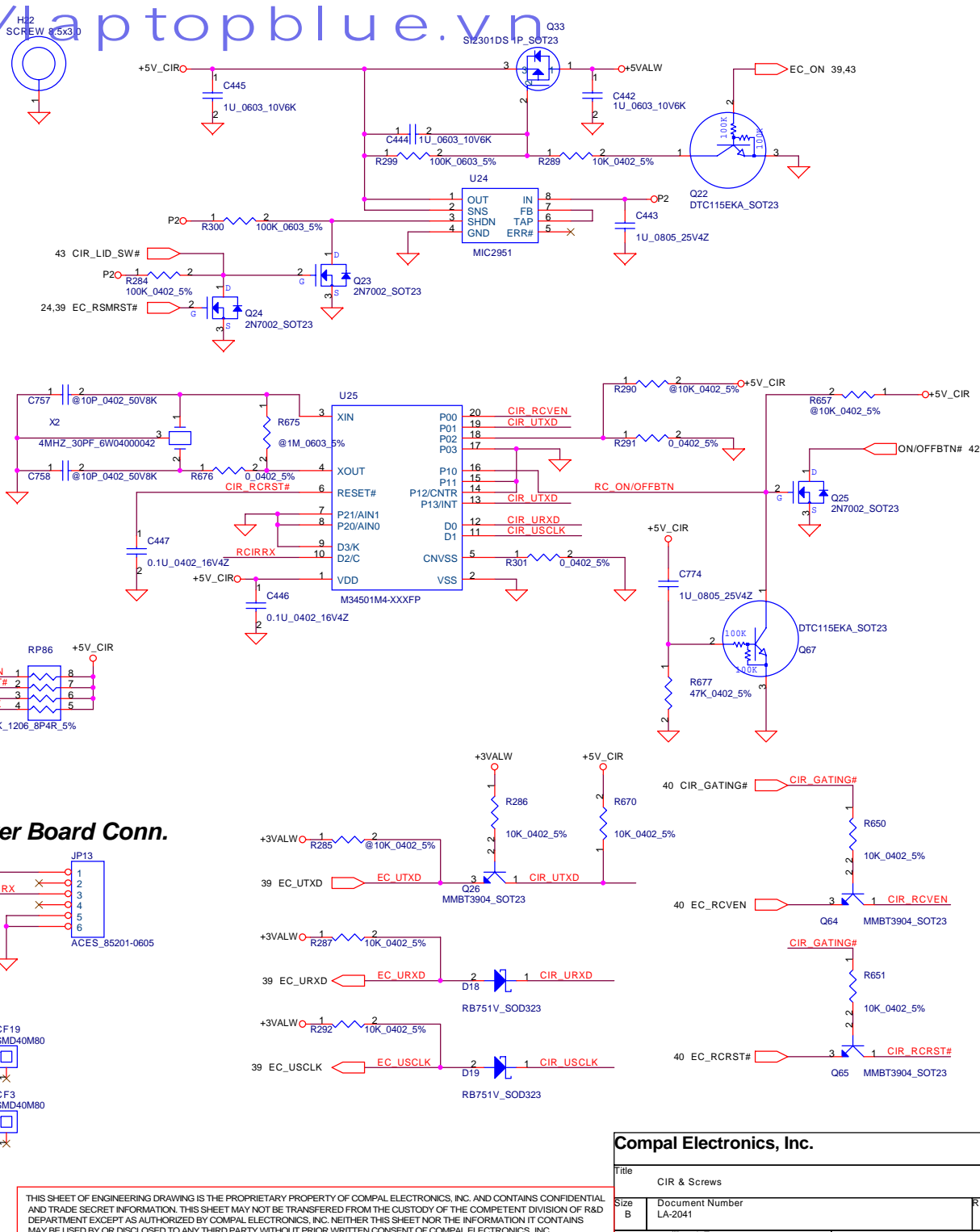
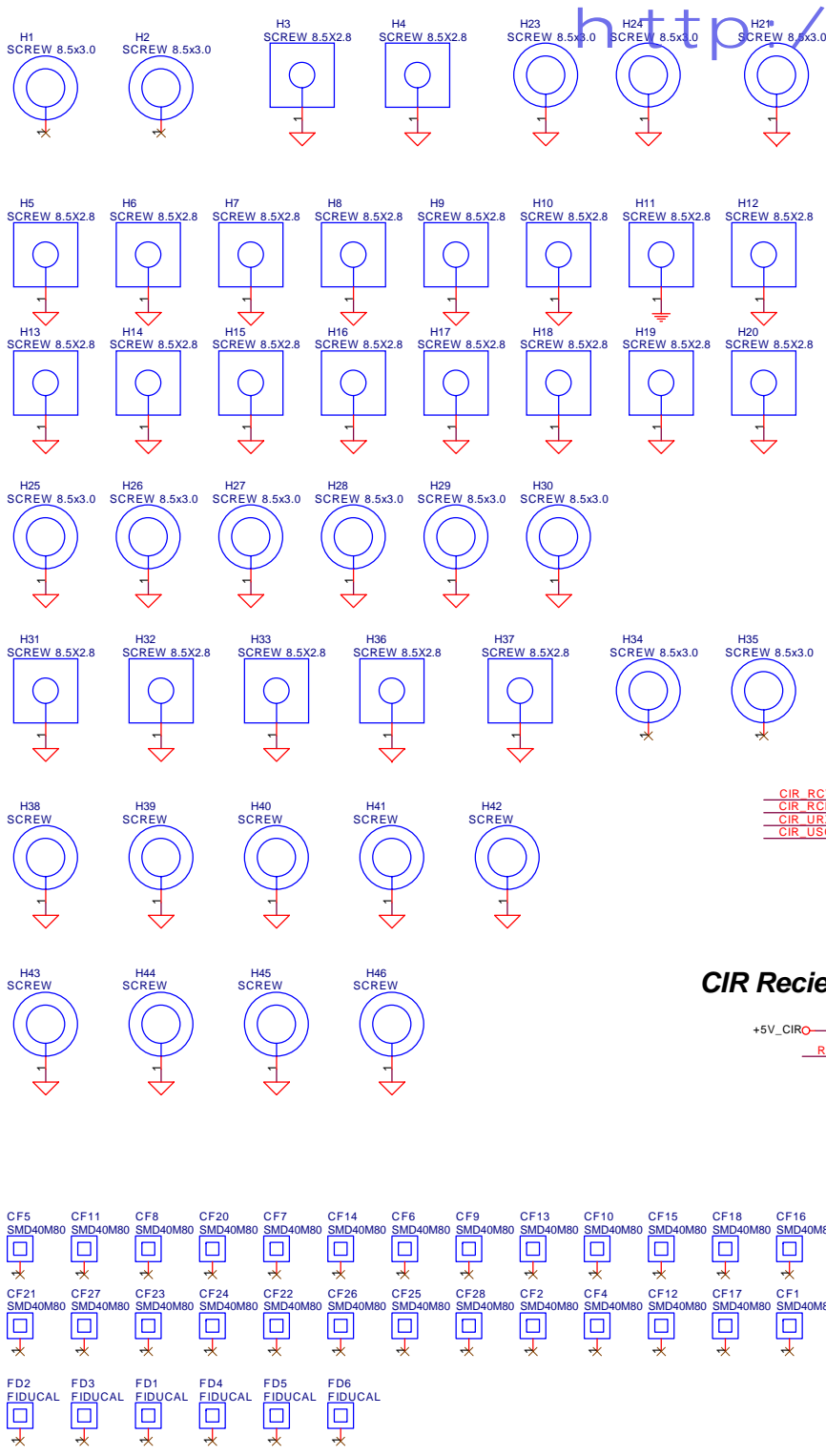
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Switchs & Connectors

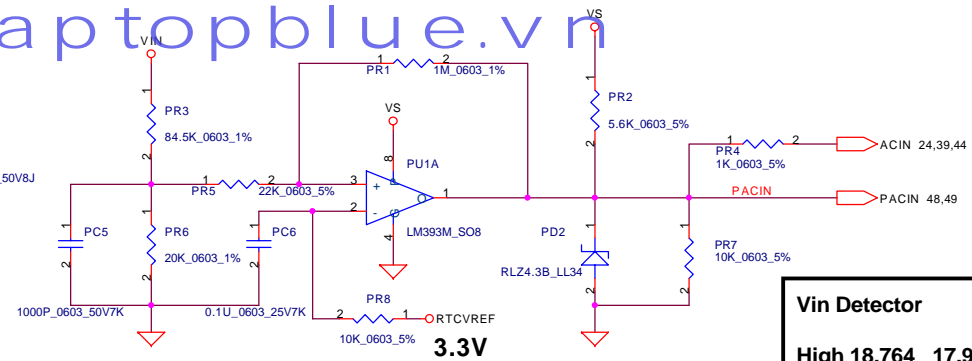
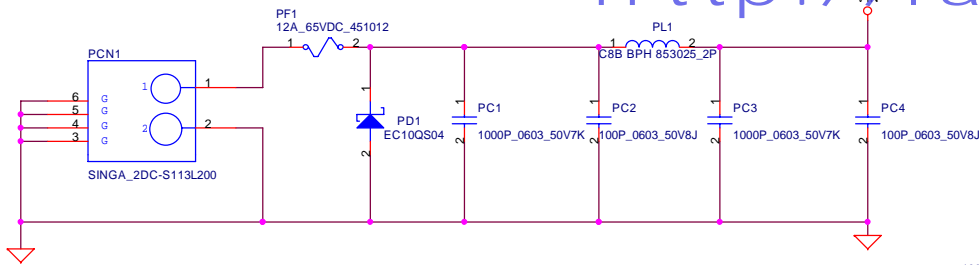
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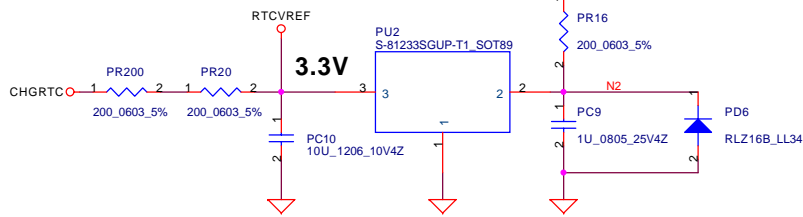
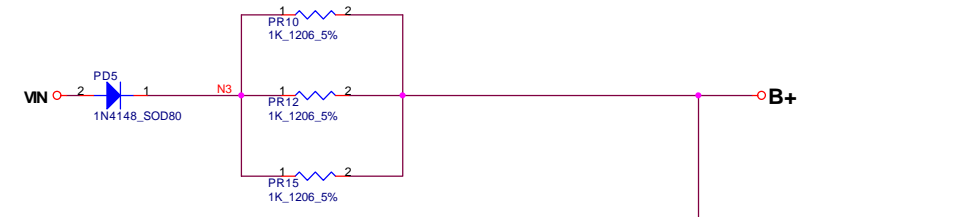
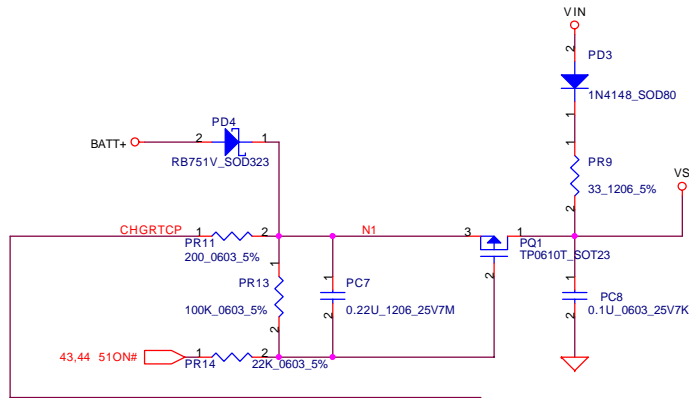
Compal Electronics, Inc.		
Title CIR & Screws		
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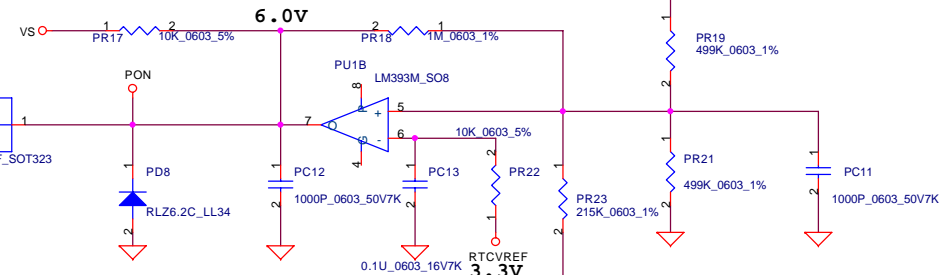


Vin Detector

High 18.764 17.901 17.063
Low 17.745 16.903 16.038

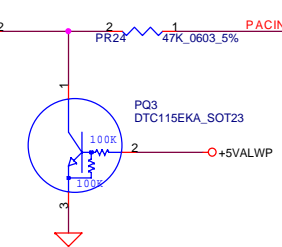
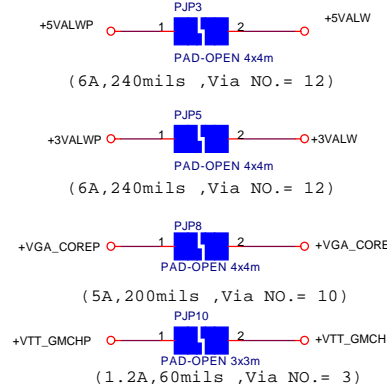
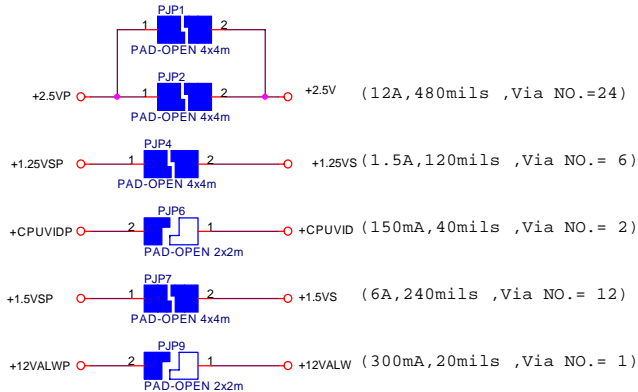


47.49 MAINPWON
48 ACON



Precharge detector

15.34 15.90 16.48
13.13 13.71 14.20



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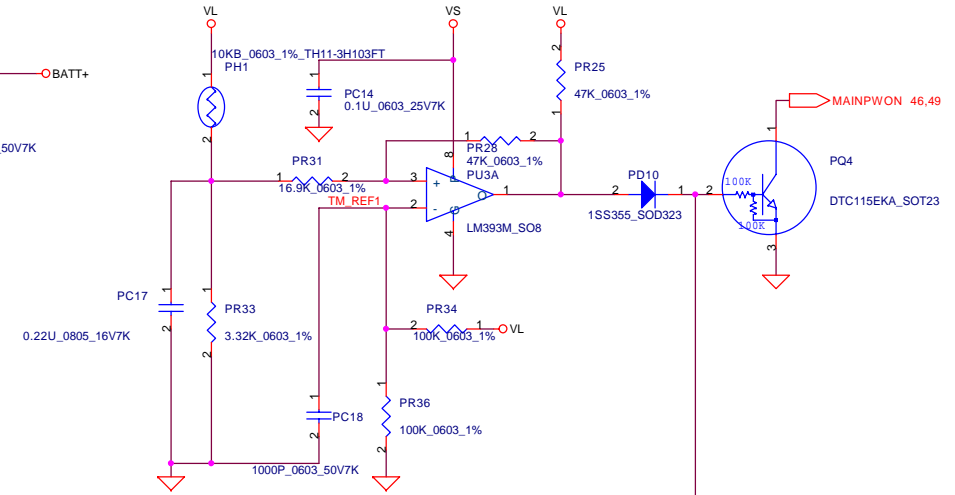
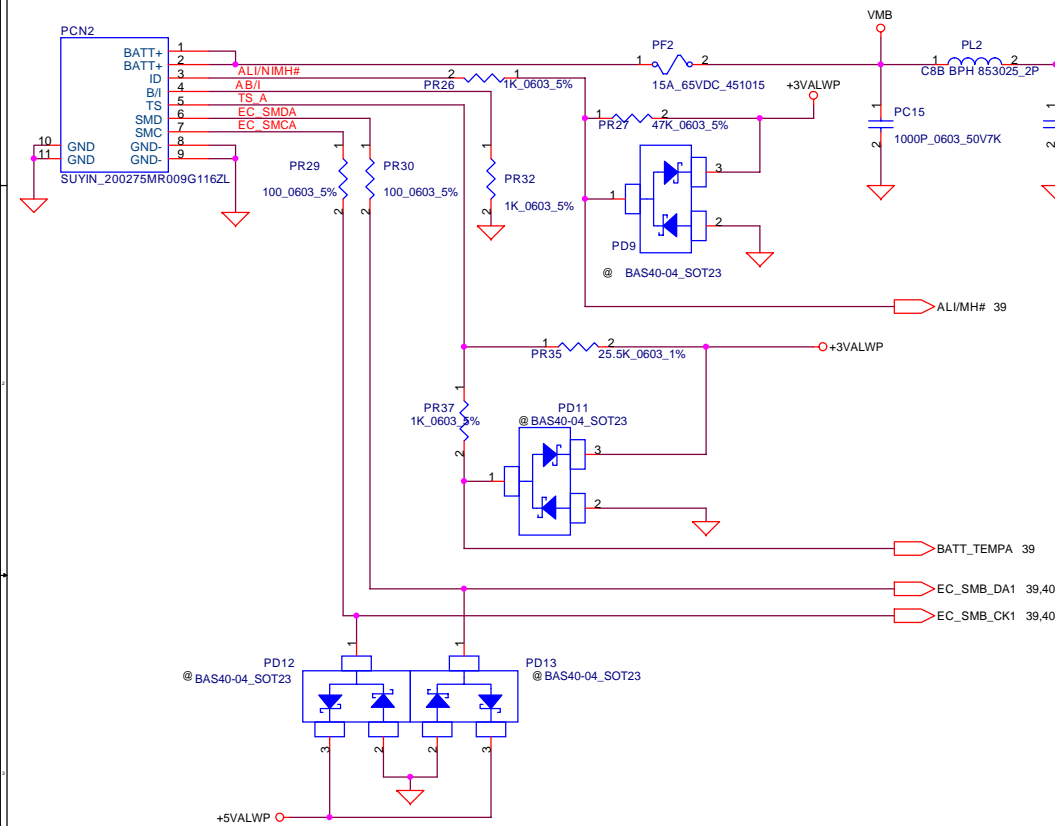
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DCIN & DETECTOR		
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PH1 under CPU botten side :

CPU thermal protection at 84 degree C

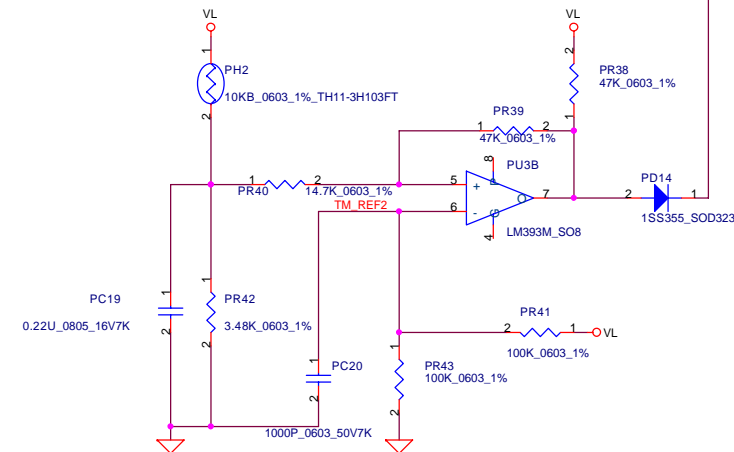
Recovery at 45 degree C

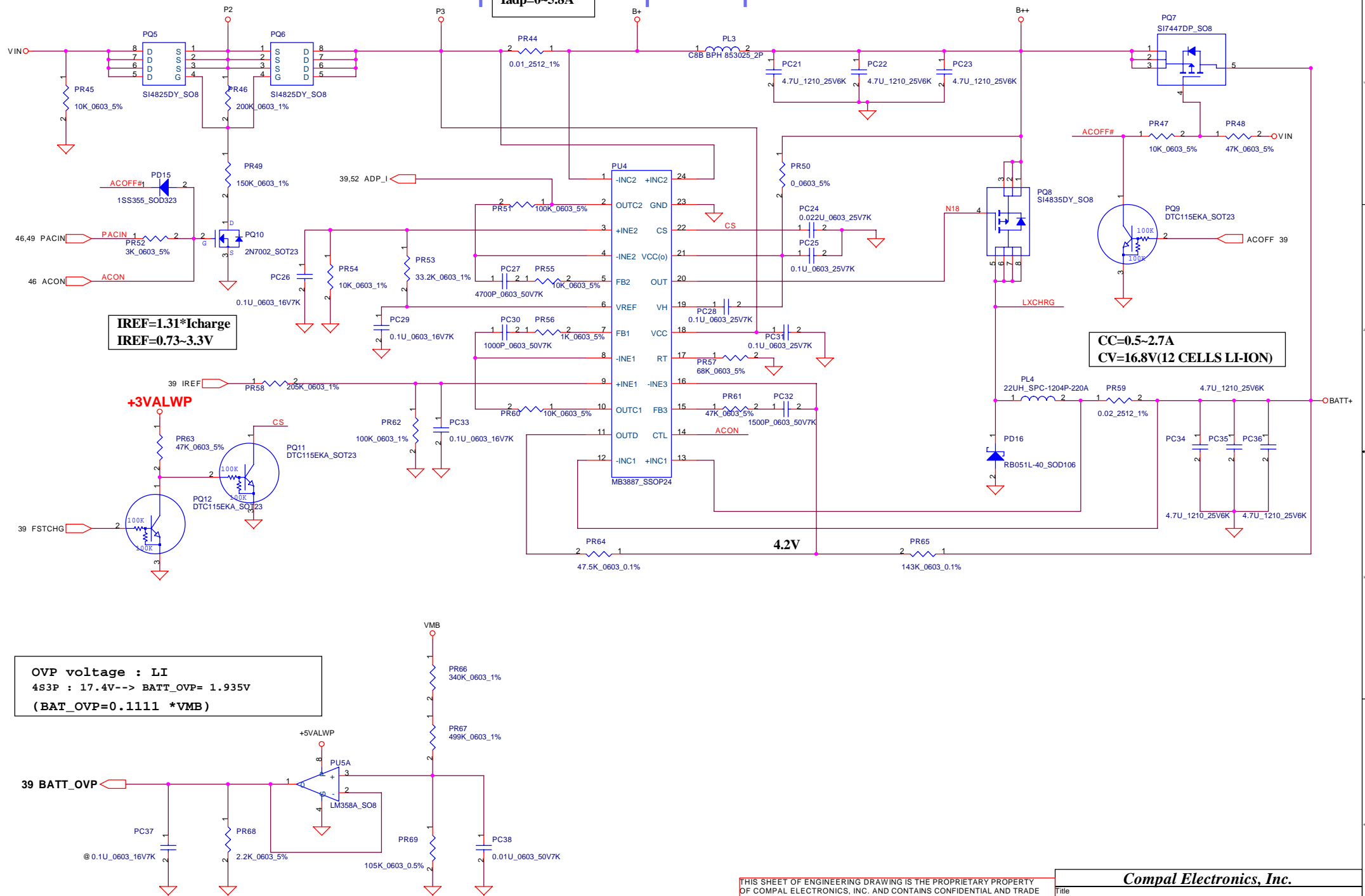


PH2 near main Battery CONN :

BAT. thermal protection at 79 degree C

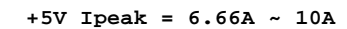
Recovery at 45 degree C

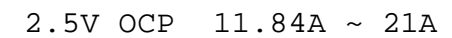




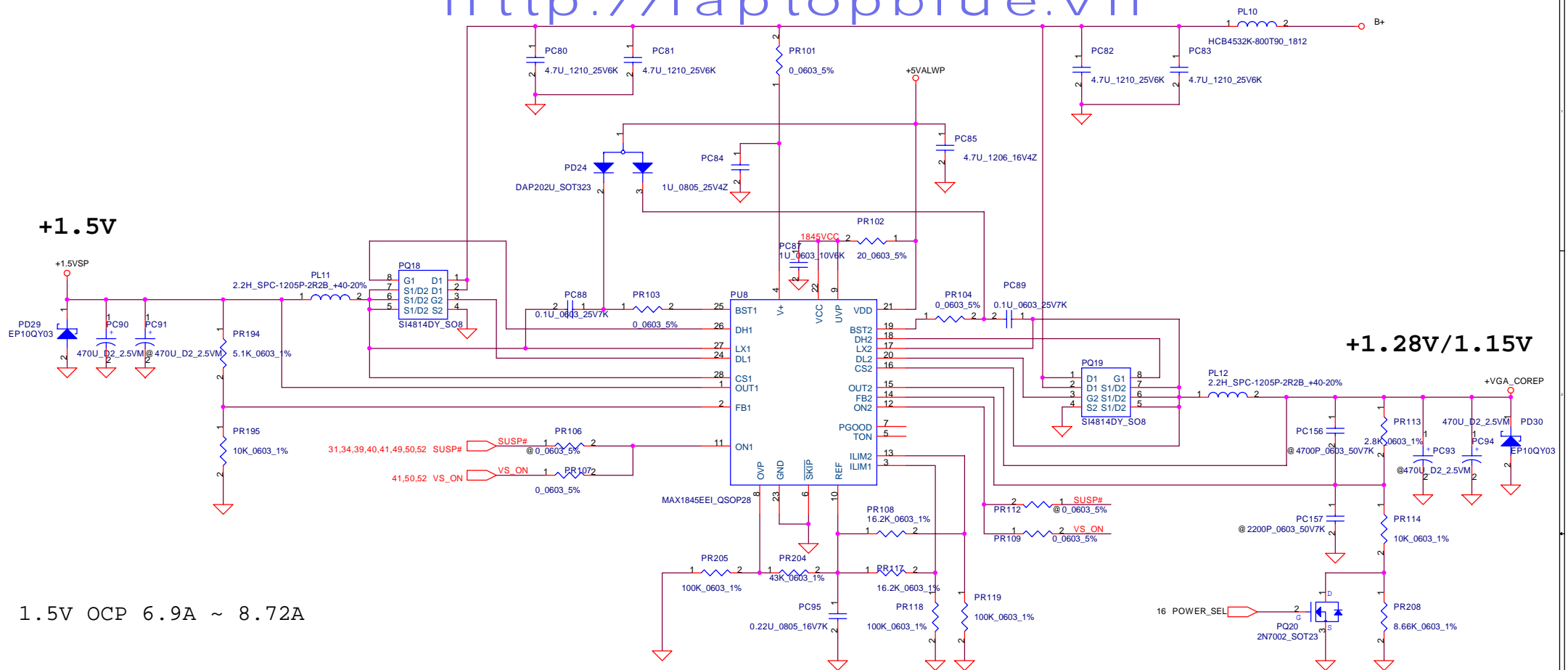
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GMCH_SEL=1 NORTHWOOD VTT_GMCH=1.45V OCP 1.98A ~ 3.78A



1.5V OCP 6.9A ~ 8.72A

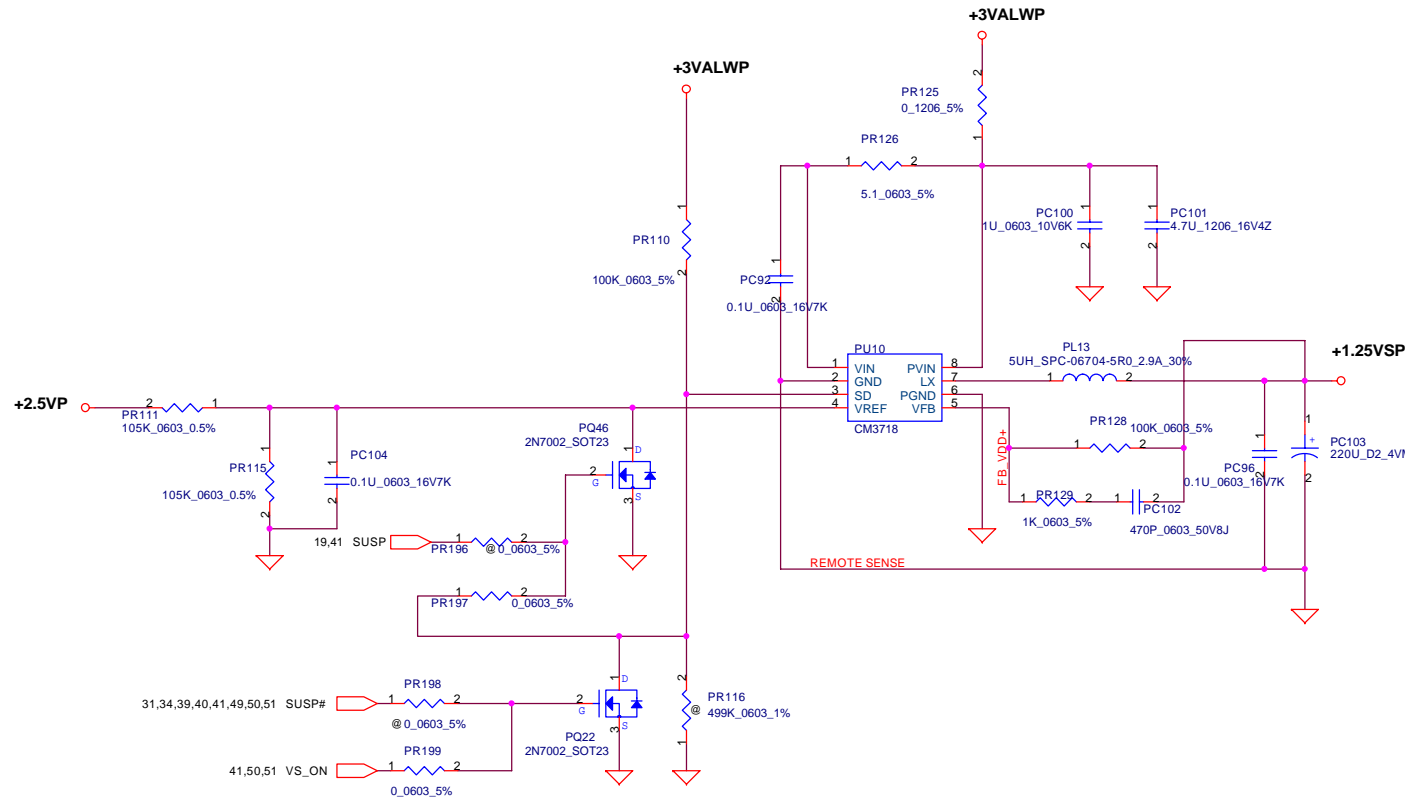
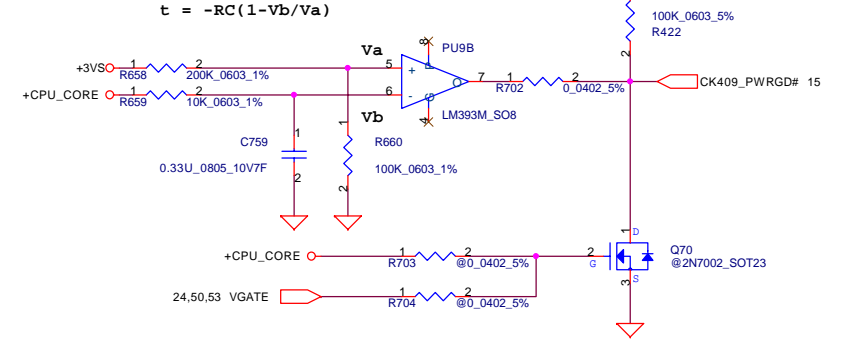
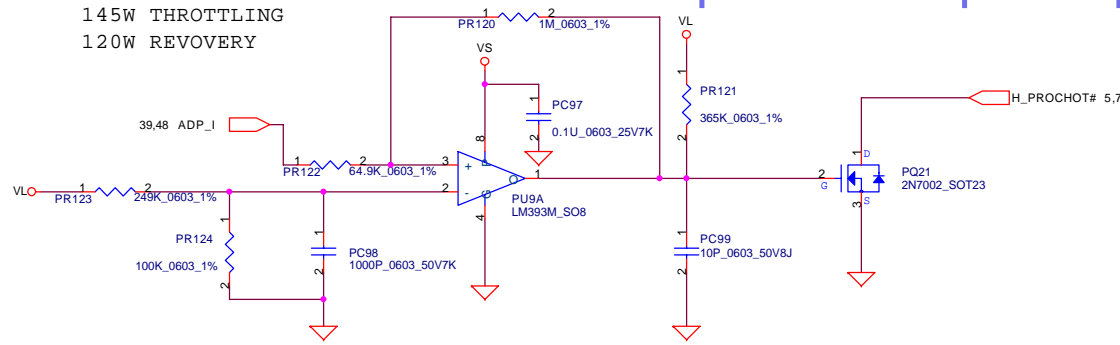
NV34M Ultra			
POWER_SEL=1	VOUT=1.28V	OCP 7.1A ~ 8.9A	PR113=2.8K_0603_1%
POWER_SEL=0	VOUT=1.15V	OCP 6.85A ~ 8.7A	PR208=8.66K_0603_1%

NV31			
POWER_SEL=1	VOUT=1.27V	OCP 7.1A ~ 8.9A	PR113=2.7K_0603_1%
POWER_SEL=0	VOUT=1V	OCP 6.85A ~ 8.7A	Unpop PR208

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145W THROTTLING
120W RECOVERY

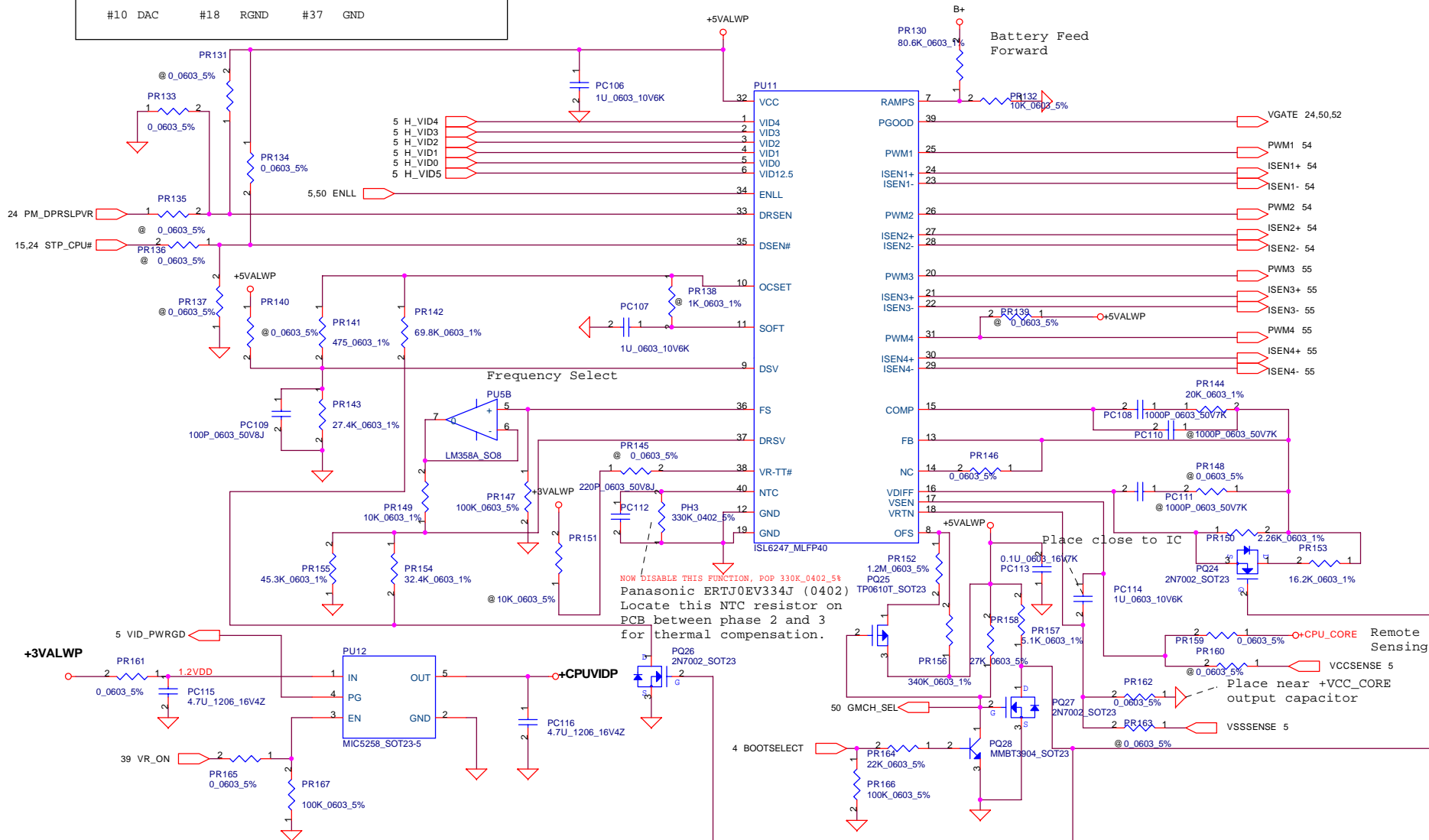


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Compal Electronics, Inc.			
Title			
DDR_1.25V/CLOCK THROTTLING			
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Different Pin Definition for ISL6561 in EU9

#7	GND	#11	REF	#33	EN	#38	OVP
#9	TCOMP	#14	IDROOP	#35	GND	#40	GND
#10	DAC	#18	RGND	#37	GND		



1. When mode control signal is high/ low, the VR will operate to Northwood/ Prescott load line.
2. VID5(12.5) should be pulled high, when the VR operates to Northwood load line.

BOOTSELECT=1 PRESCOTT

BOOTSELECT=0 NORTHWOOD

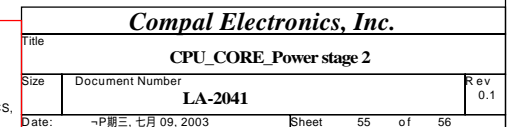
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Title			
CPU_CORE_Controller			
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Compal Electronics, Inc.			
Title			
CPU_CORE_Power stage 1			
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DBQ01 PIR LIST

http://laptopblue.vn

***** Rev0.1 PIR List *****

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