LongBeach 100

LA-2451 REV 0.4 Schematic

Desktop LGA-775 Package

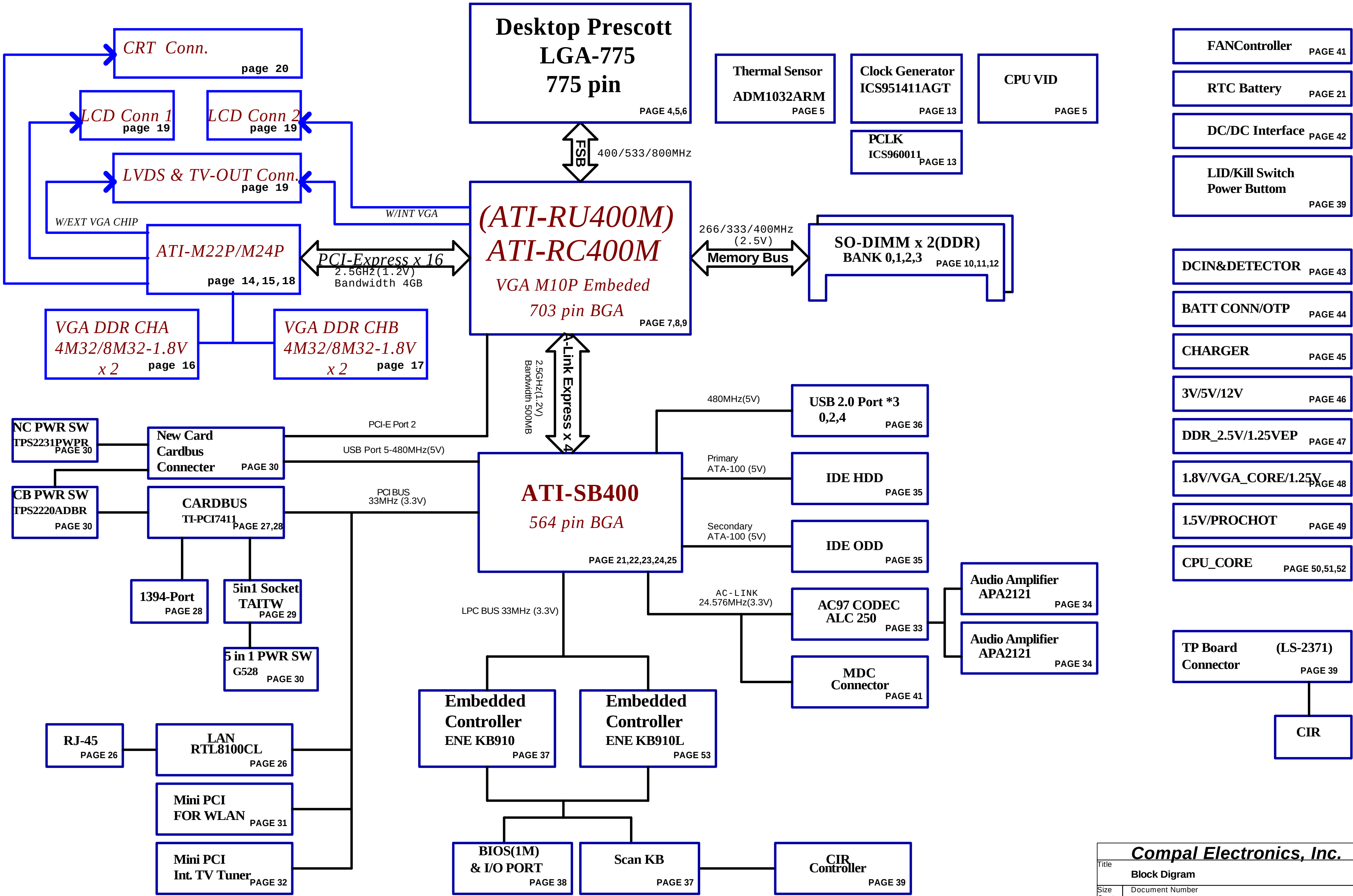
RXC400M(RU400M)+SB400+ATI M22P/M24P(64/128MB VRAM)

2004-11-08<A>

Compal Electronics, Inc.
Title: Cover Page
Size: Custom | Document Number | Rev 0.1
Date: 星期一, 十一月 08, 2004 | Sheet 1 of 53

EAQ11 LA-2451

FUNCTION BLOCK DIAGRAM



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Title: Block Digram

Size: Custom | Document Number | Rev: 0.1

Date: 星期六, 十一月 06, 2004 | Sheet 2 of 53

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VGA_CORE	1.0V/1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.2VS	1.2VS for PCI-Express	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 8X	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(PCI7411)	AD20	2	PIRQE/PIRQF/PIRQG/PIRQH
LAN	AD22	1	PIRQG/PIRQC
Mini-PCI(WLAN)	AD18	3	PIRQF:PIRQG/PIRQC:PIRQD
Mini-PCI(TV-Tuner)	AD23	4	PIRQH:PIRQE/PIRQD:PIRQA

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

EC SM Bus1 address

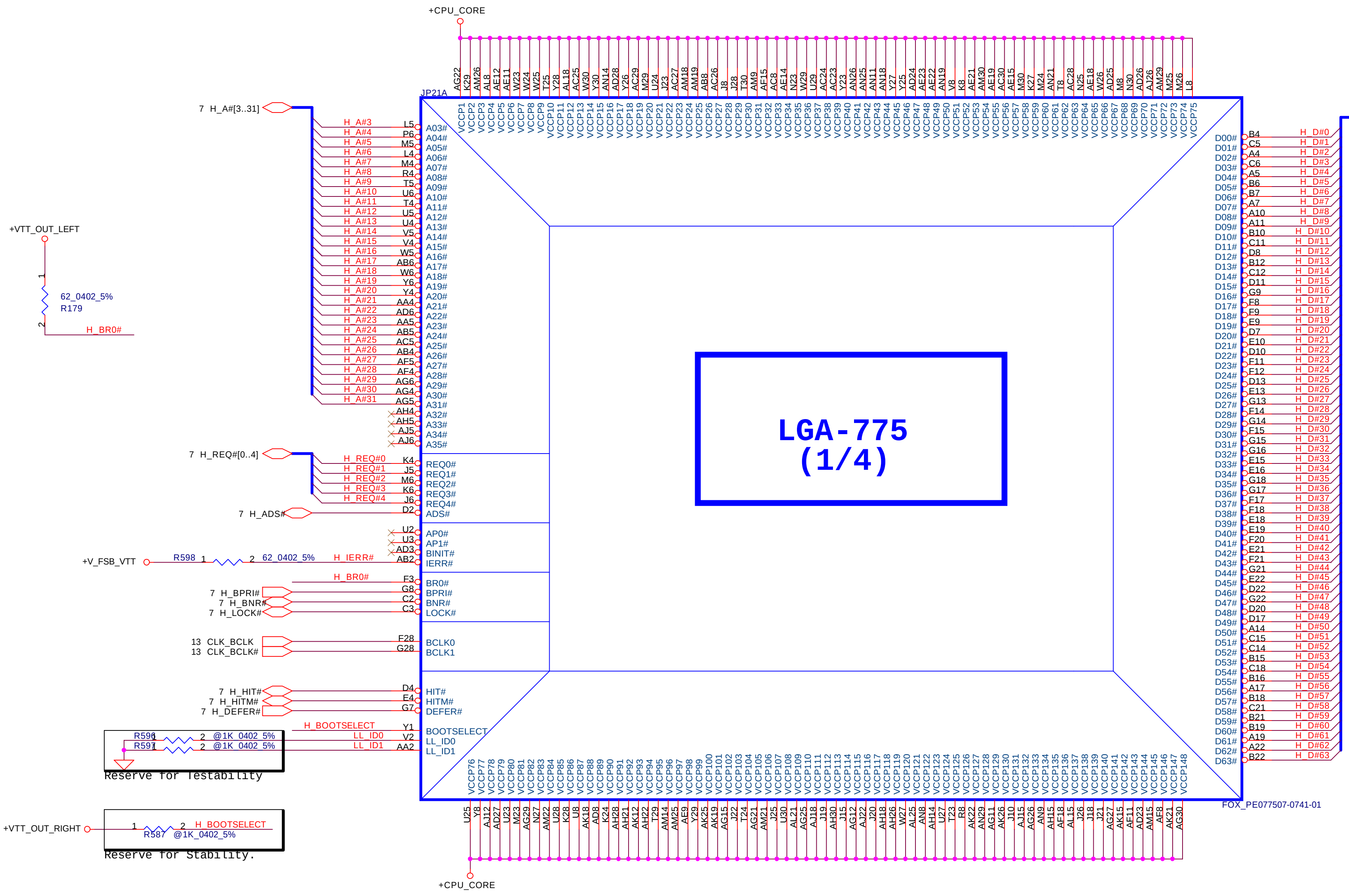
Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
(24C04)	1011 000Xb

EC SM Bus2 address

Device	Address
ADM1032	1001 110X b
ICS960011	1101 110X b

SB400 SM Bus address

Device	Address
Clock Generator (ICS951411BGLFT)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 001Xb



In Intel CPU datasheet:
LL_ID[1:0], VTT_SEL, GTLREF_SEL and VID_SELECT are signals that
are implement on the processor package.
That is they are either connected directly to Vss or open lands.

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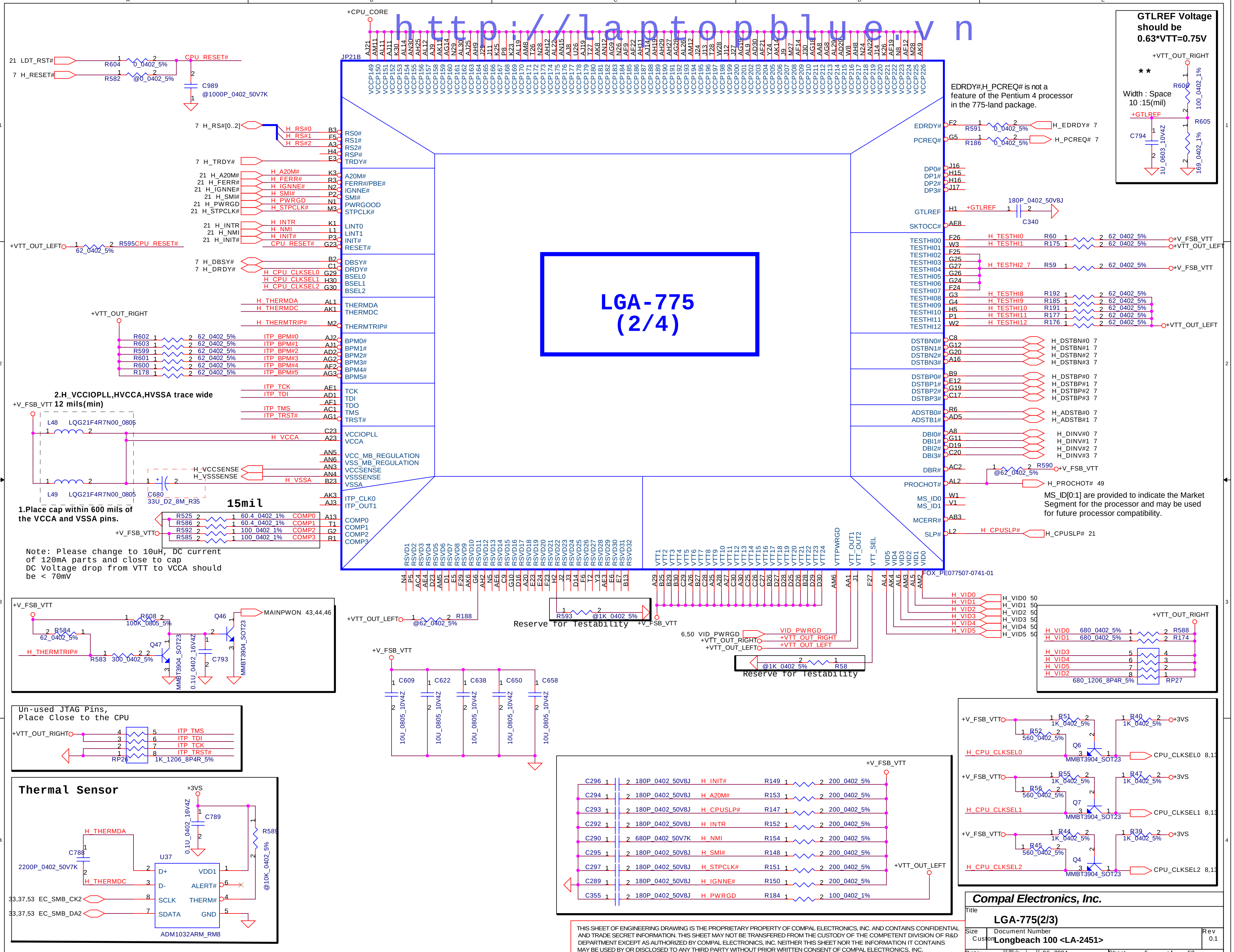
Title: LGA-775(1/3)		
Size: Custom	Document Number: Longbeach 100 <LA-2451>	Rev: 0.1
Date: 星期六, 十一月 06, 2004	Sheet 4 of 53	



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Title: LGA-775(2/3)

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Date: 星期六, 十一月 06, 2004 | Sheet 5 of 53

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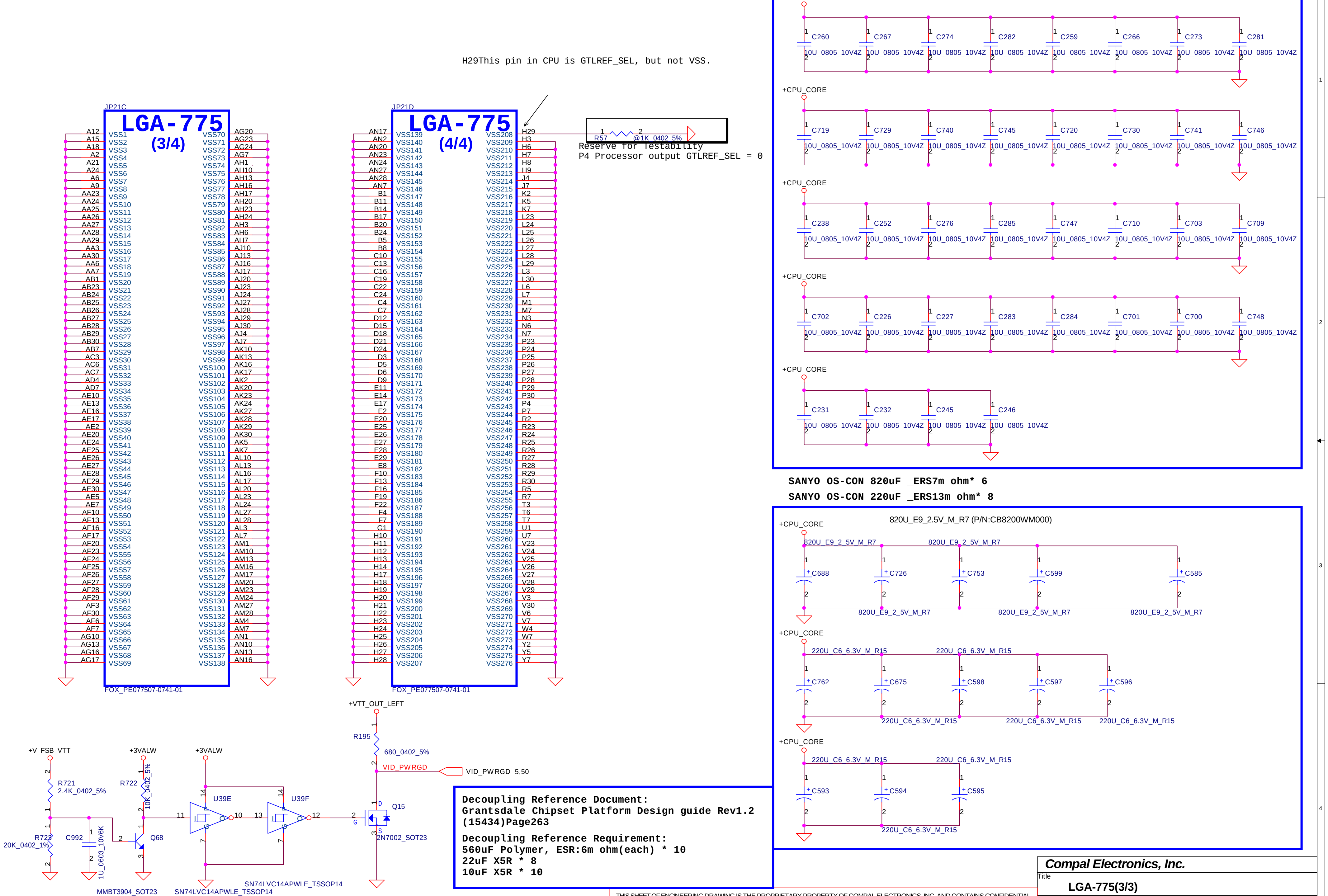

Decoupling Reference Document:
Grantsdale Chipset Platform Design guide Rev1.2
(15434)Page263

Decoupling Reference Requirement:
560uF Polymer, ESR:6m ohm(each) * 10
22uF X5R * 8
10uF X5R * 10

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Title	LGA-775(3/3)
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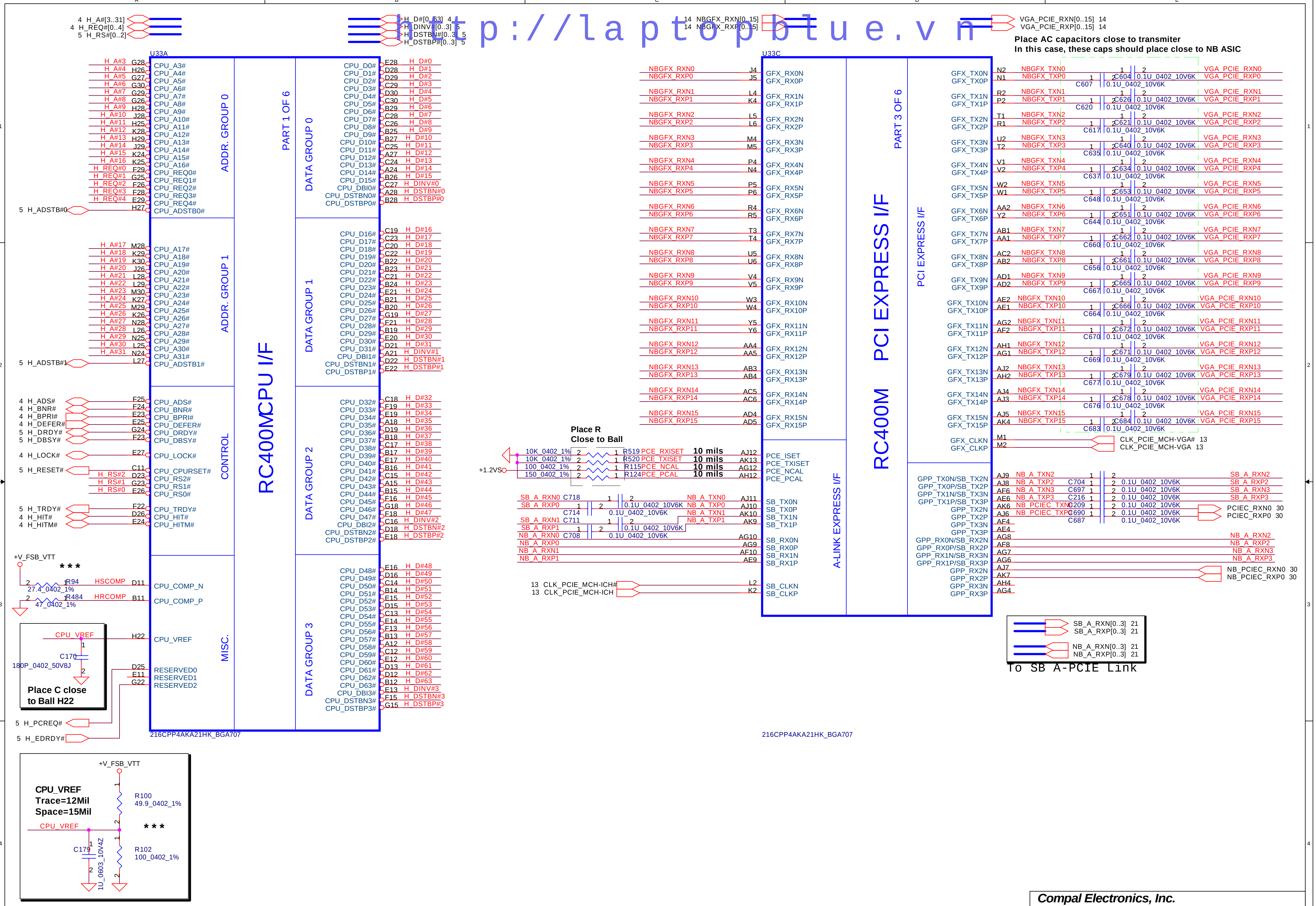
Rev	0.1
Date: 星期六, 十一月 06, 2004	Sheet 6 of 53



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Title: RC400M-FSB,PCIE,A-PCIE(1/3)

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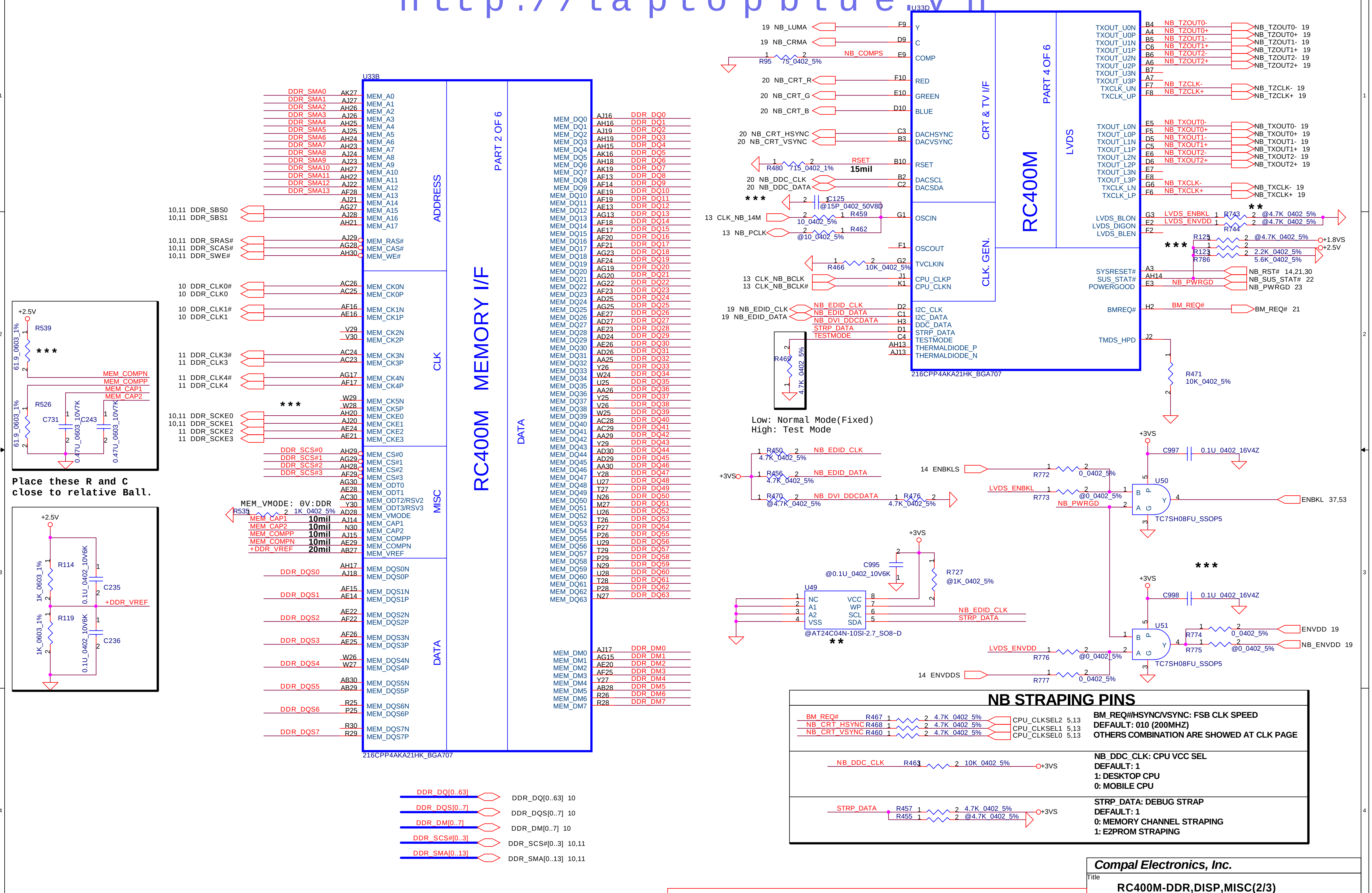
Date: 星期六, 十一月 06, 2004 | Sheet 7 of 53



NB STRAPING PINS

BM_REQ# R467 4.7K_0402_5% CPU_CLKSEL2 5,13; NB_CRT_HSYNC R468 4.7K_0402_5% CPU_CLKSEL1 5,13; NB_CRT_VSYNC R460 4.7K_0402_5% CPU_CLKSEL0 5,13	**BM_REQ#/HSYNC/VSYNC: FSB CLK SPEED** **DEFAULT: 010 (200MHZ)** **OTHERS COMBINATION ARE SHOWED AT CLK PAGE**
NB_DDC_CLK R463 10K_0402_5% +3VS	**NB_DDC_CLK: CPU VCC SEL** **DEFAULT: 1** **1: DESKTOP CPU** **0: MOBILE CPU**
STRP_DATA R457 4.7K_0402_5% +3VS; R455 @4.7K_0402_5%	**STRP_DATA: DEBUG STRAP** **DEFAULT: 1** **0: MEMORY CHANNEL STRAPING** **1: E2PROM STRAPING**

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Title	RC400M-DDR,DISP,MISC(2/3)
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Document Number	Longbeach 100 <LA-2451>
Rev	0.1
Date:	星期六, 十一月 06, 2004
Sheet	8 of 53

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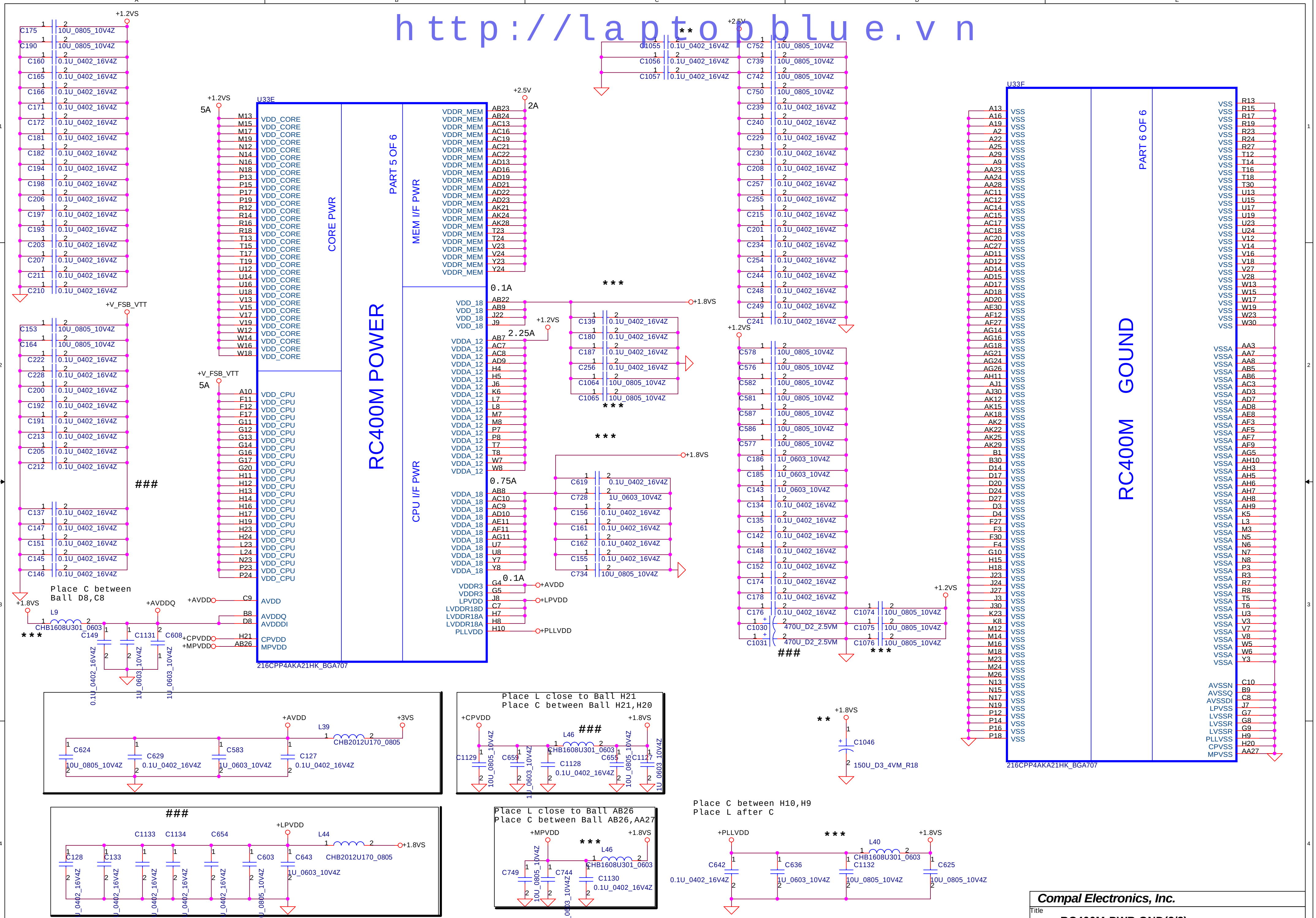

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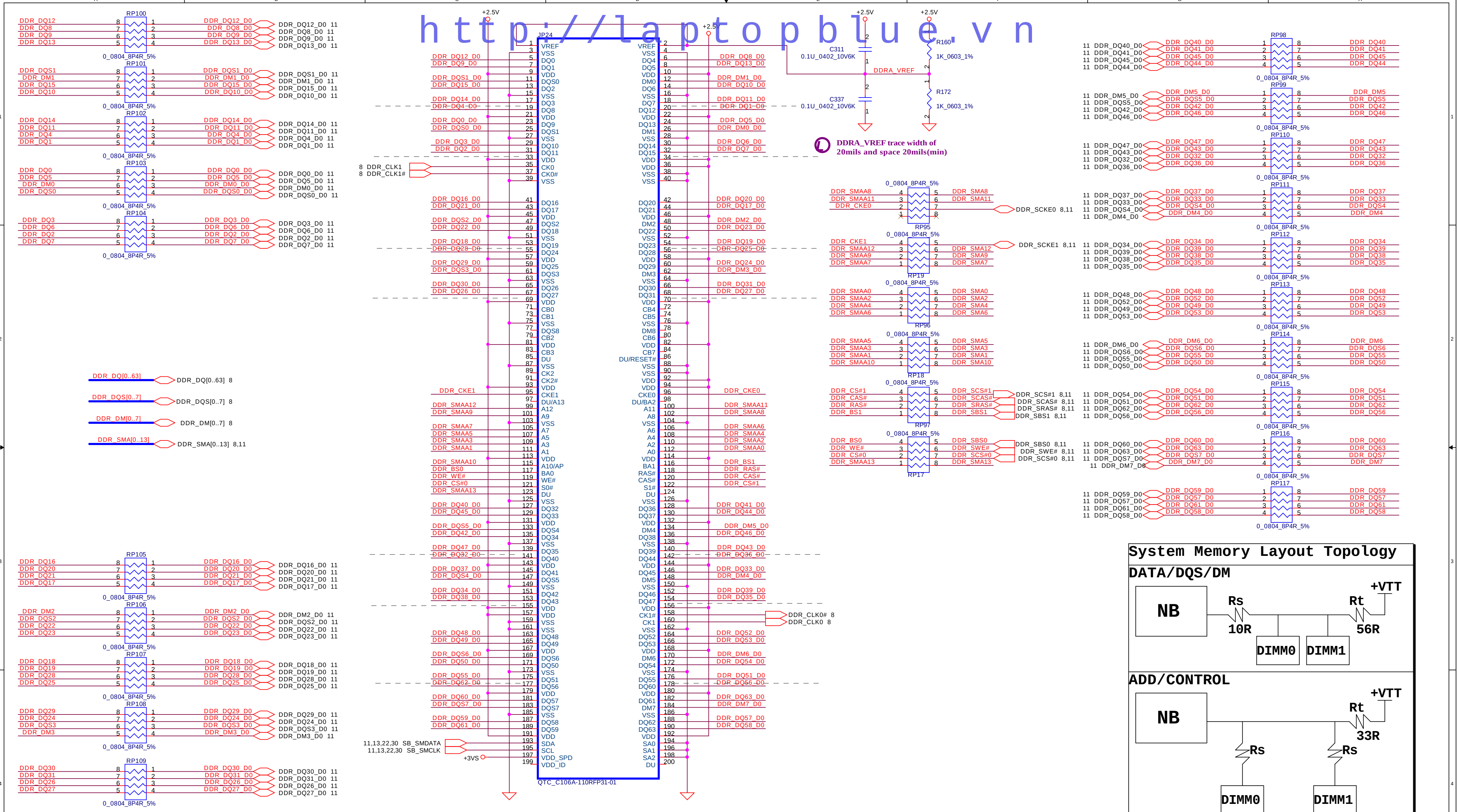
Title	RC400M-PWR,GND(3/3)	
Size: Custom	Document Number: Longbeach 100 <LA-2451>	Rev: 0.1
Date: 星期六, 十一月 06, 2004	Sheet 9 of 53	



Layout note
Place Add/Command resisotrs
Close to Pin, max L = 300 mils

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Title: DDR-SODIMM SLOT0		
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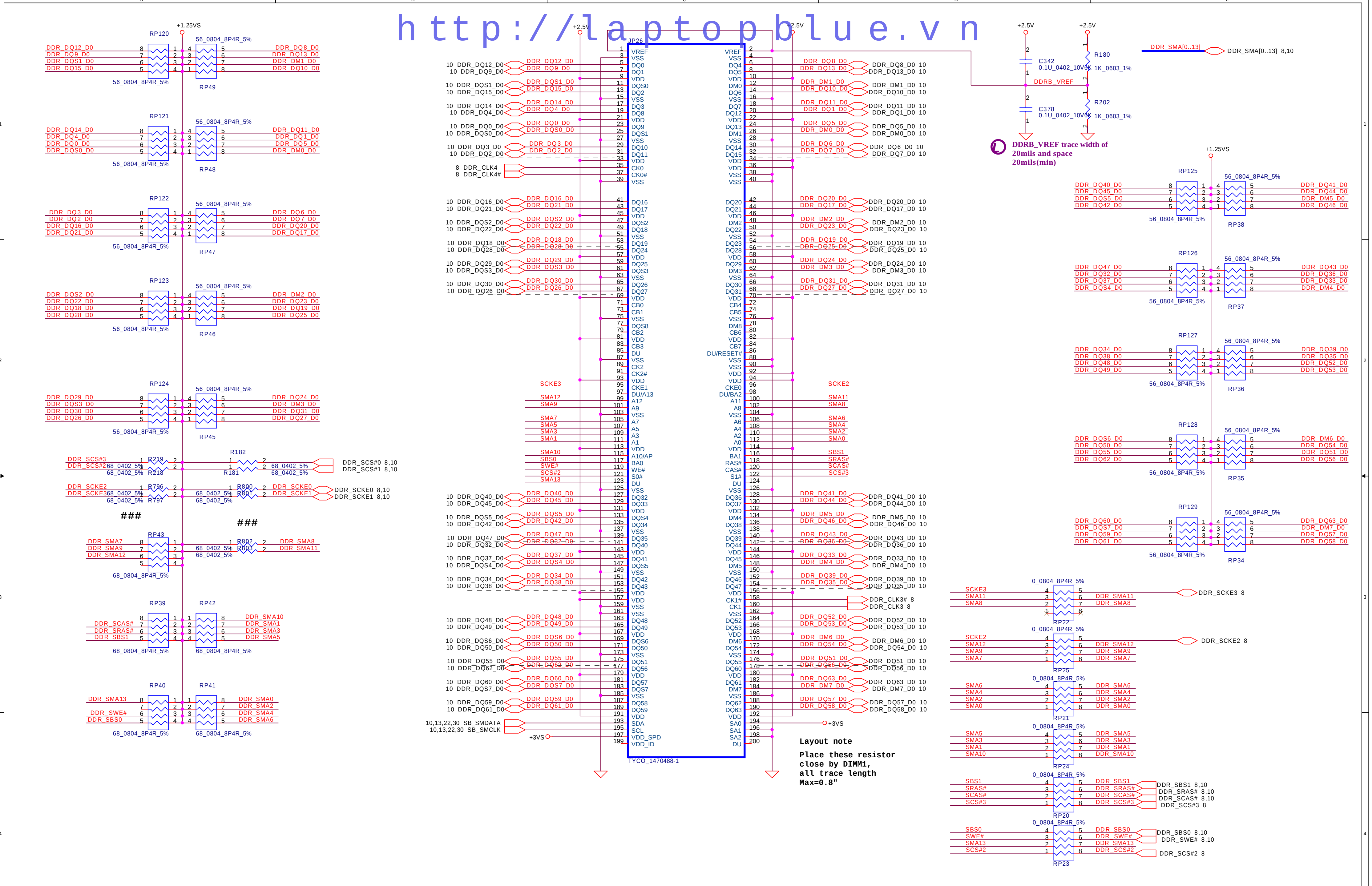
Date: 星期六, 十一月 06, 2004	Sheet 10 of 53	



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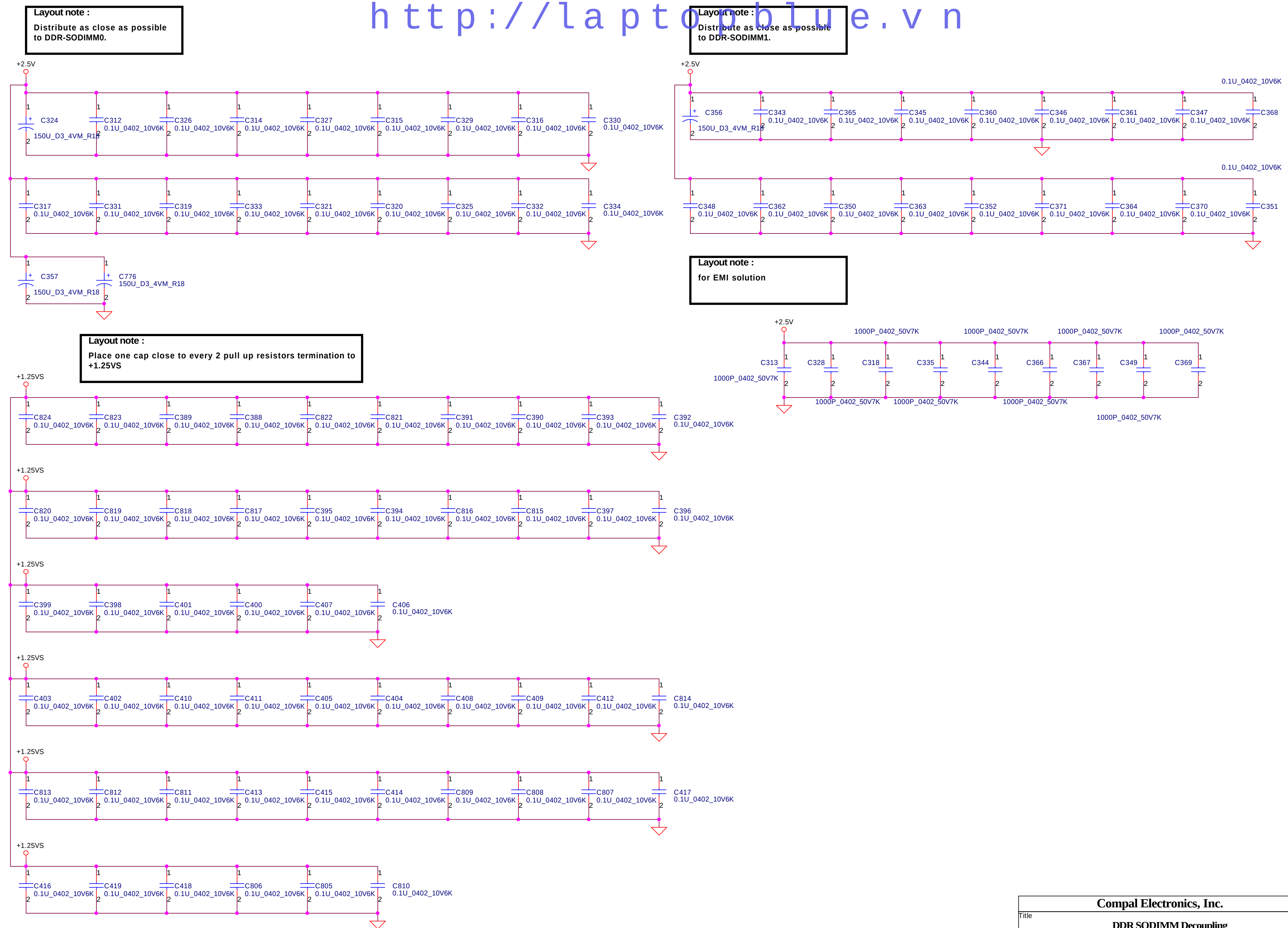
Title: DDR-SODIMM SLOT1

Size | Document Number: Longbeach 100 <LA-2451> | Rev 0.1

Date: 星期六, 一月 06, 2004 | Sheet 11 of 53



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Title	DDR SODIMM Decoupling	
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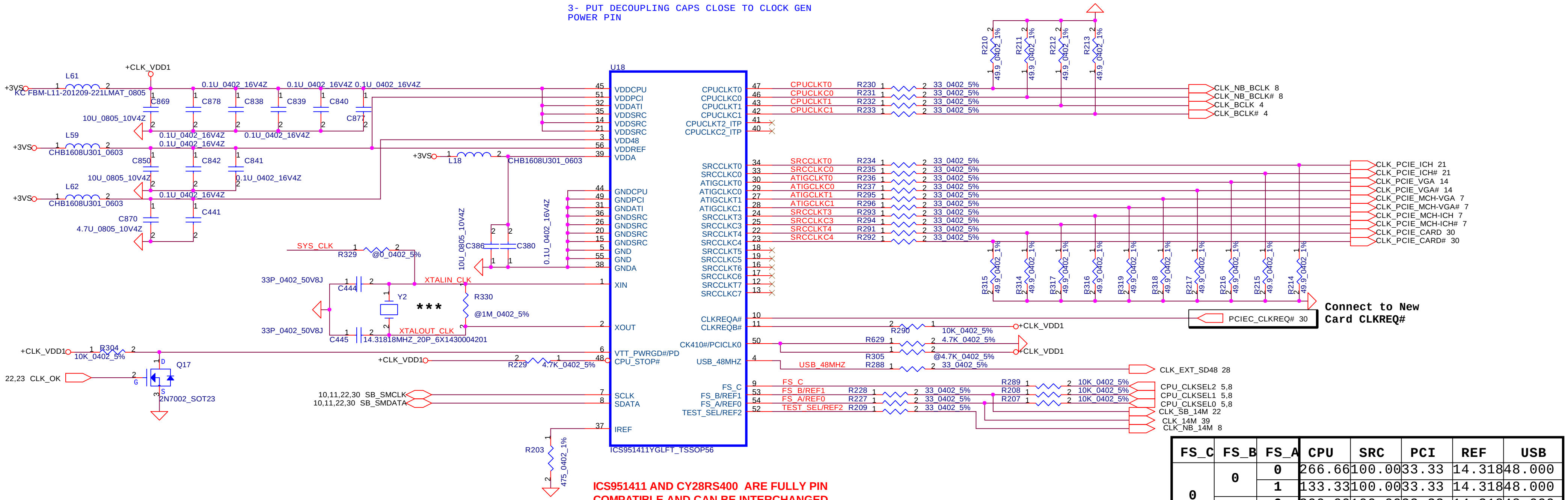
Date: 星期六, 十一月 06, 2004	Sheet 12 of 53	

Clock Generator

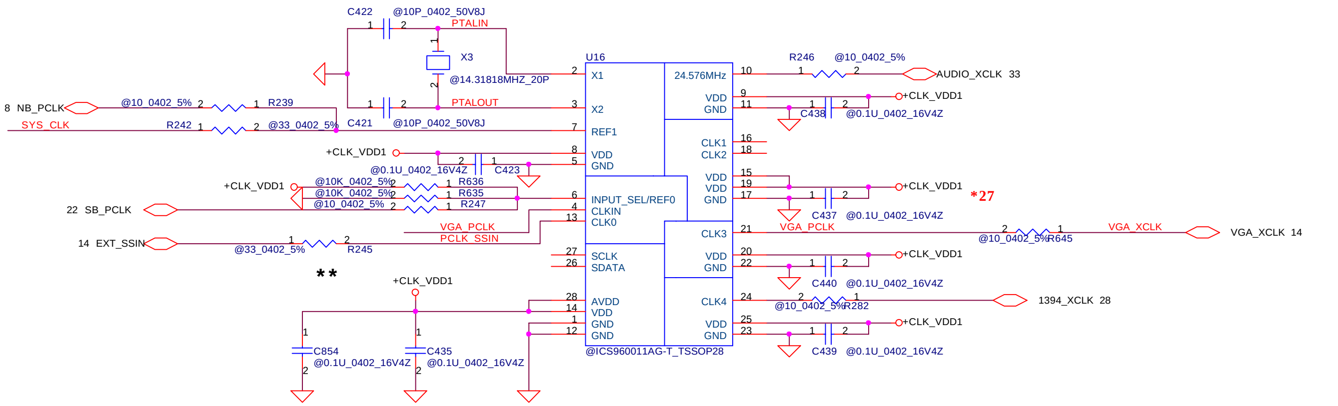
1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLOCK GEN AS POSSIBLE
2- ROUTE ALL CPUCLK/#, NBCLK/#, ITPCLK/# AND SCR/# ,AS DIFFERENT PAIR RULE
3- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



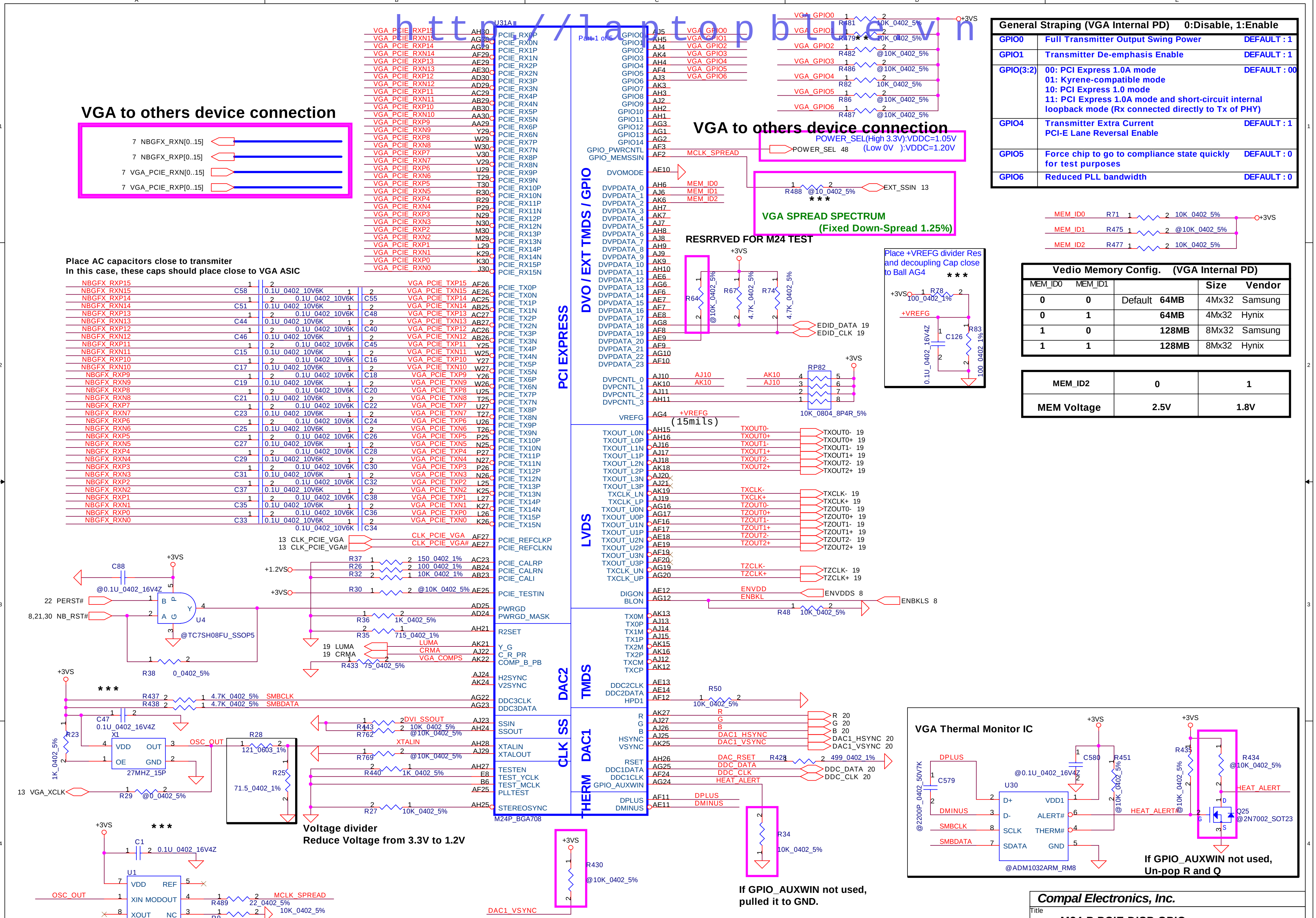
ICS951411 AND CY28RS400 ARE FULLY PIN COMPATIBLE AND CAN BE INTERCHANGED WITHOUT ANY HARDWARE MODIFICATION.

FS_C	FS_B	FS_A	CPU	SRC	PCI	REF	USB
0	0	0	266.66	100.00	33.33	14.318	48.000
		1	133.33	100.00	33.33	14.318	48.000
	1	0	200.00	100.00	33.33	14.318	48.000
		1	166.66	100.00	33.33	14.318	48.000
1	0	1	100.00	100.00	33.33	14.318	48.000
	1	0	400.00	100.00	33.33	14.318	48.000
		1	RESERVED			14.318	48.000

CLOCK OF IC



Compal Electronics, Inc.	
Title	CLOCK GENERATOR ICS951411
Size: Custom	Document Number: Longbeach 100 <LA-2451>
Rev	0.1
Date:	星期六, 十一月 06, 2004
Sheet	13 of 53



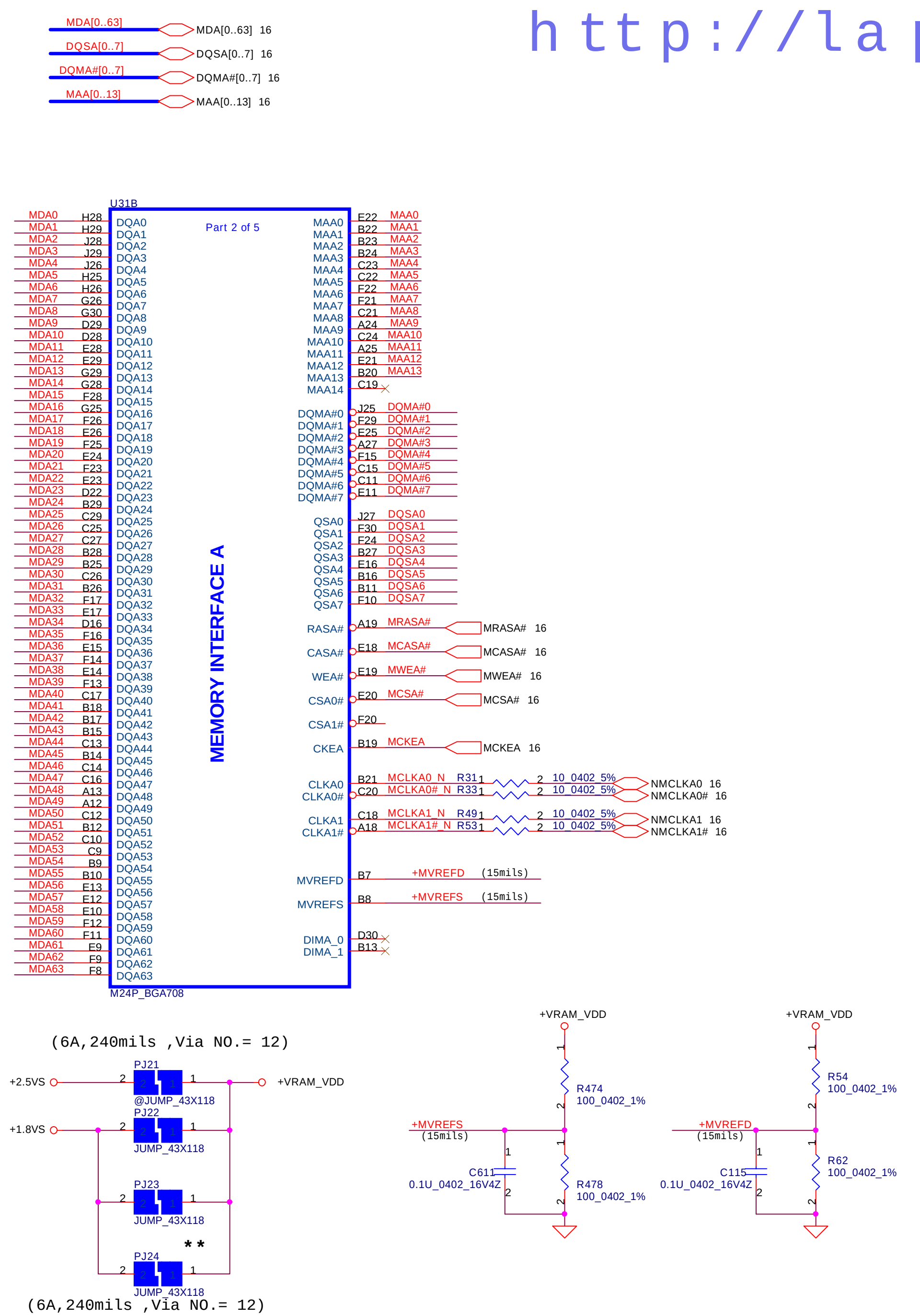
General Straping (VGA Internal PD) 0:Disable, 1:Enable

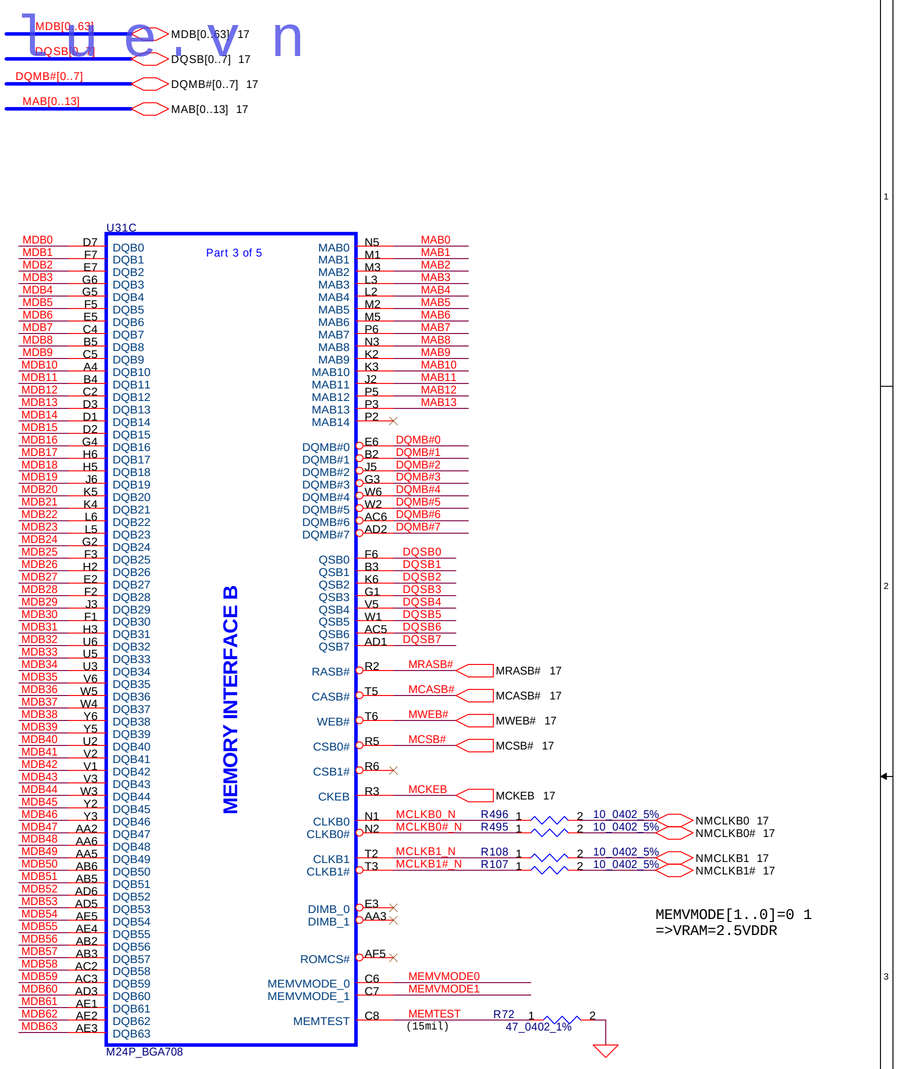
GPIO0	Full Transmitter Output Swing Power	DEFAULT : 1
GPIO1	Transmitter De-emphasis Enable	DEFAULT : 1
GPIO(3:2)	00: PCI Express 1.0A mode 01: Kyrene-compatible mode 10: PCI Express 1.0 mode 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	DEFAULT : 00
GPIO4	Transmitter Extra Current PCI-E Lane Reversal Enable	DEFAULT : 1
GPIO5	Force chip to go to compliance state quickly for testing purposes	DEFAULT : 0
GPIO6	Reduced PLL bandwidth	DEFAULT : 0

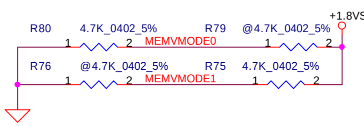
Vedio Memory Config. (VGA Internal PD)

MEM_ID0	MEM_ID1		Size	Vendor
0	0	Default	64MB	4Mx32 Samsung
0	1		64MB	4Mx32 Hynix
1	0		128MB	8Mx32 Samsung
1	1		128MB	8Mx32 Hynix

MEM_ID2	0	1
MEM Voltage	2.5V	1.8V







	R79	R75	R80	R76
M24(2.5V VRAM)	POP	UNPOP	UNPOP	POP
M24(1.8V VRAM)	UNPOP	POP	POP	UNPOP
M26(1.8V VRAM)	UNPOP	UNPOP	UNPOP	UNPOP

For Uni-directional signals, series resistors should be placed close to the VGA ASIC.
Such as MDQMB[0..7] ,MBA[0..13],MRASB#,MCASB#, MWEB#,MCSB#[0..1]

For Bi-directional signals, series resistors should be placed close to the memory.
Such as MDB[0..63] and MDQSB[0..7]

For Uni-directional signals, series resistors should be placed close to the VGA ASIC.
Such as MDQMA[0..7] ,MAA[0..13],MRASA#,MCASA#, MWEA#,MCSA#[0..1]

For Bi-directional signals, series resistors should be placed close to the memory.
Such as MDA[0..63] and MDQSA[0..7]

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Title: M24-P VRAM INTERFACE

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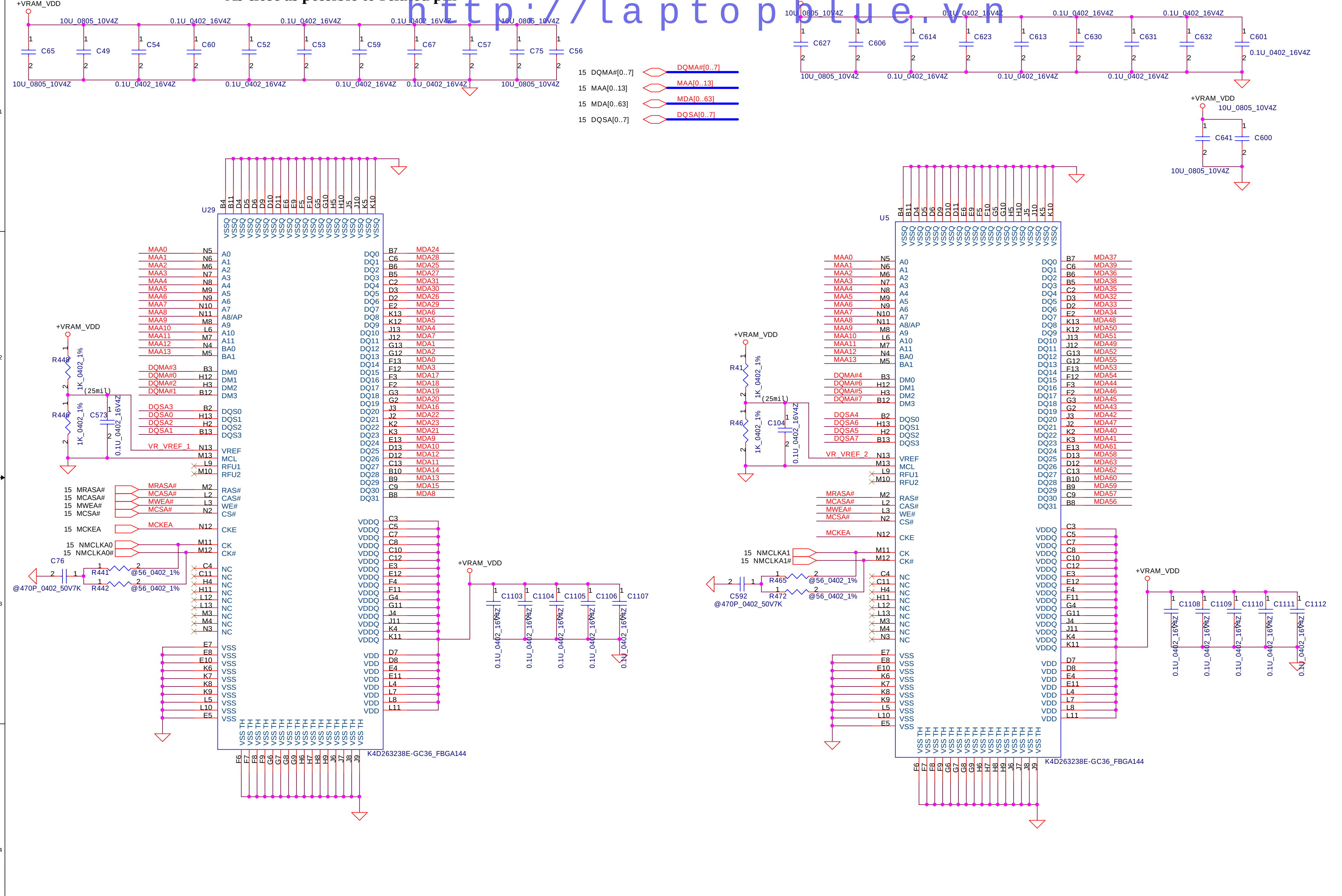
Date: 星期六, 十一月 06, 2004 | Sheet 15 of 53

As close as possible to related pin



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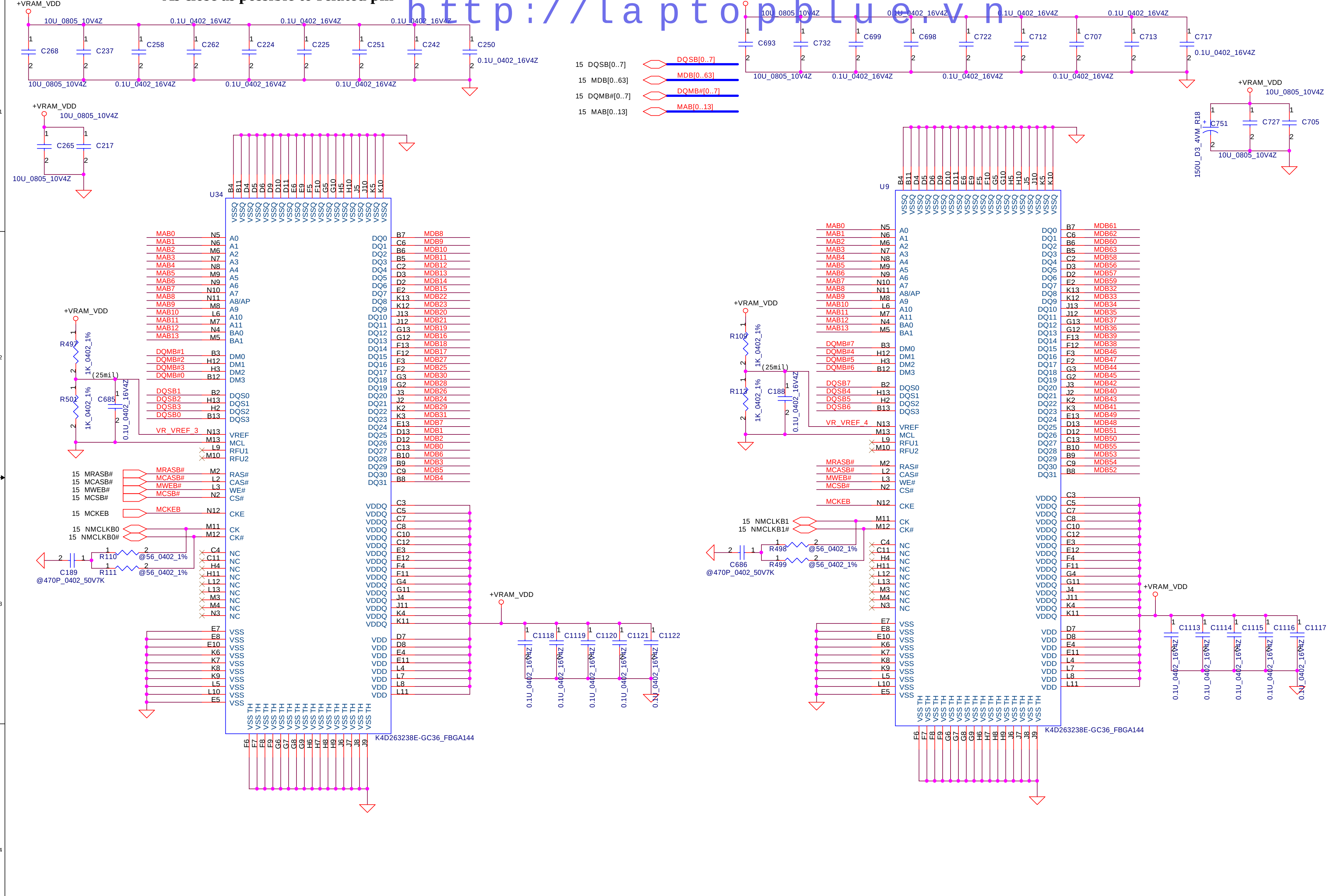
Title	VRAM DDR CHANNEL A
Size: Custom	Document Number: Longbeach 100 <LA-2451>
Rev	0.1
Date:	星期六, 十一月 06, 2004
Sheet	16 of 53

As close as possible to related pin



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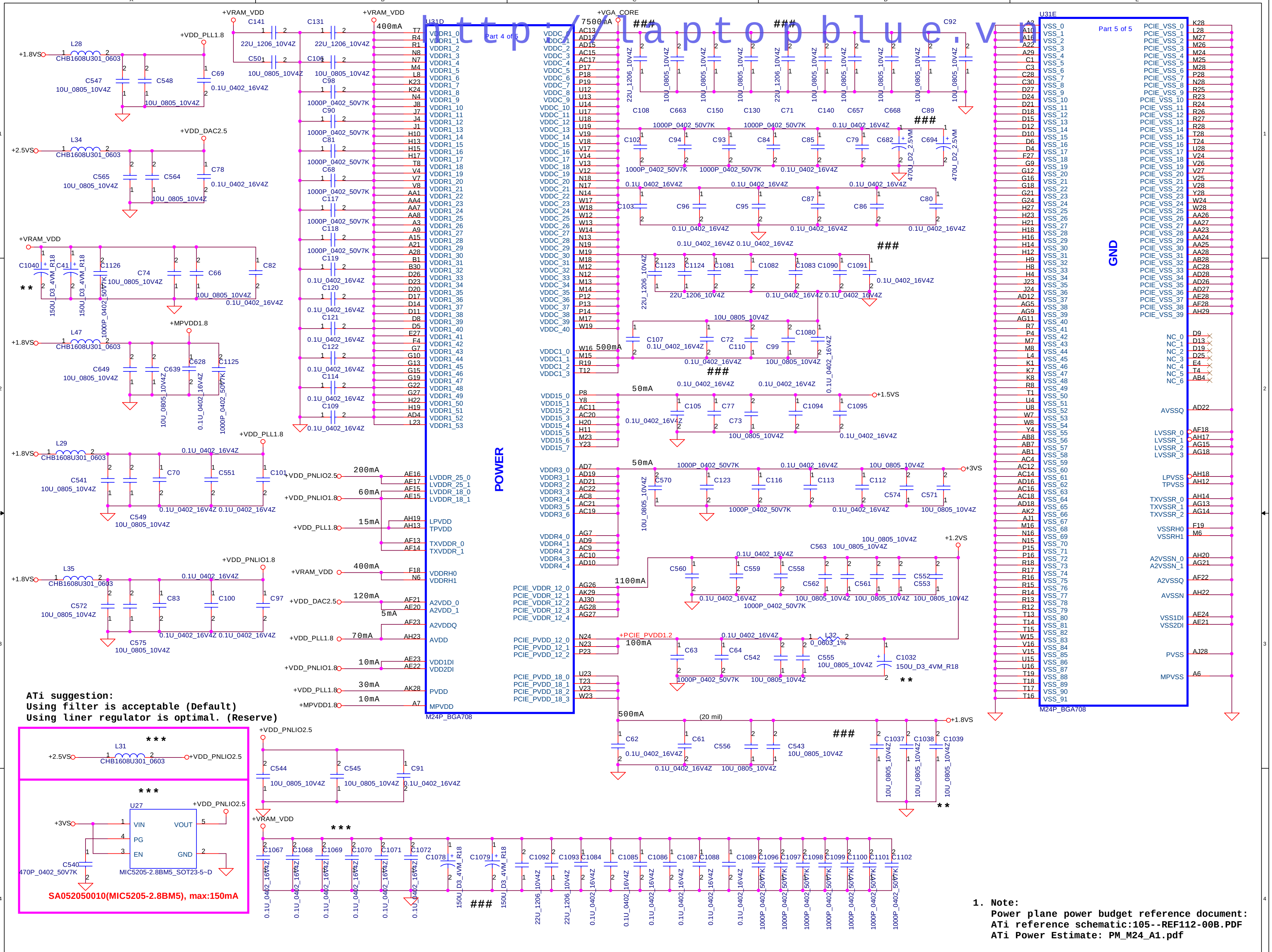
Title	VRAM DDR CHANNEL B	
Size: Custom	Document Number: Longbeach 100 <LA-2451>	Rev 0.1
Date: 星期六, 十一月 06, 2004	Sheet 17 of 53	



ATi suggestion:
Using filter is acceptable (Default)
Using liner regulator is optimal. (Reserve)

1. Note:
Power plane power budget reference document:
ATi reference schematic:105--REF112-00B.PDF
ATi Power Estimate: PM_M24_A1.pdf

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Title	M24-P POWER
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Rev	0.1
Date:	星期六, 十一月 06, 2004
Sheet	18 of 53

TV-OUT CONNECTOR

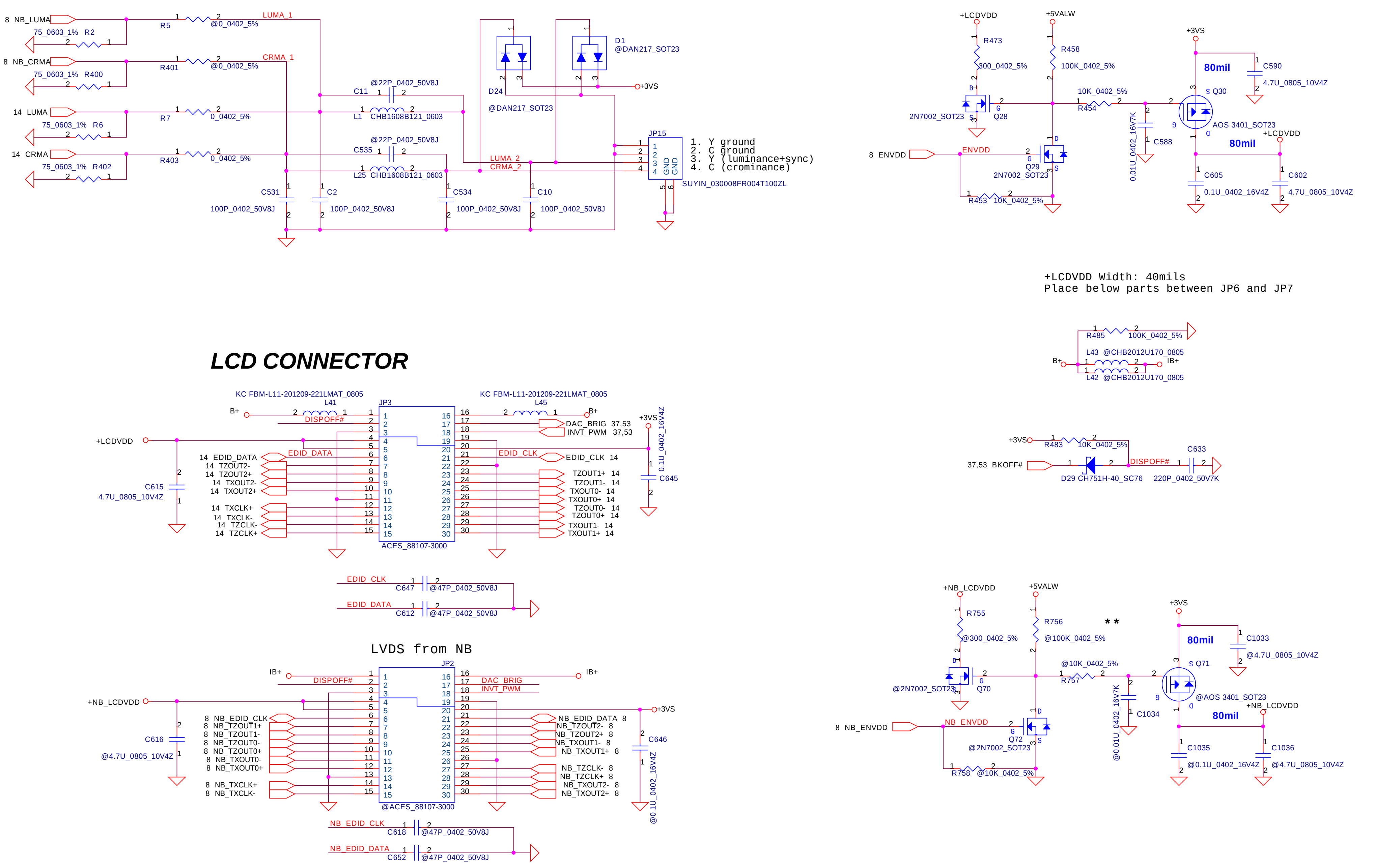
Reduce LUMA_1 and CRMA_1 length
As short as possible

PANEL +LCDVDD CTRL CKT

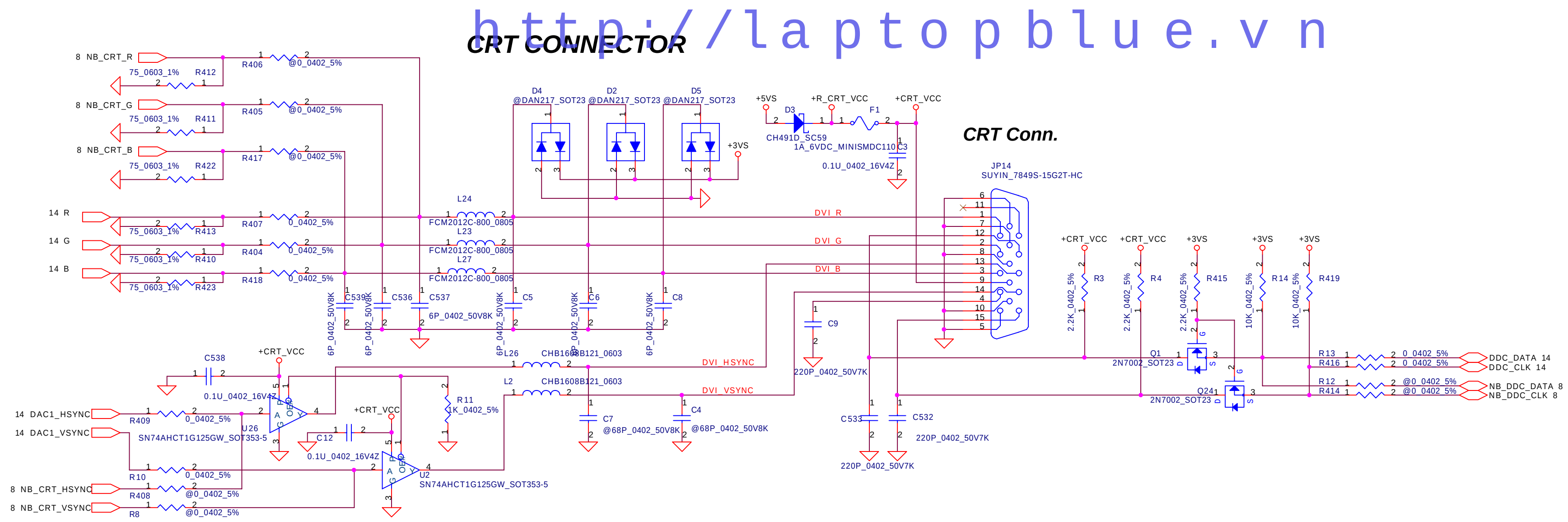
+LCDVDD Width: 40mils
Place below parts between JP6 and JP7

LCD CONNECTOR

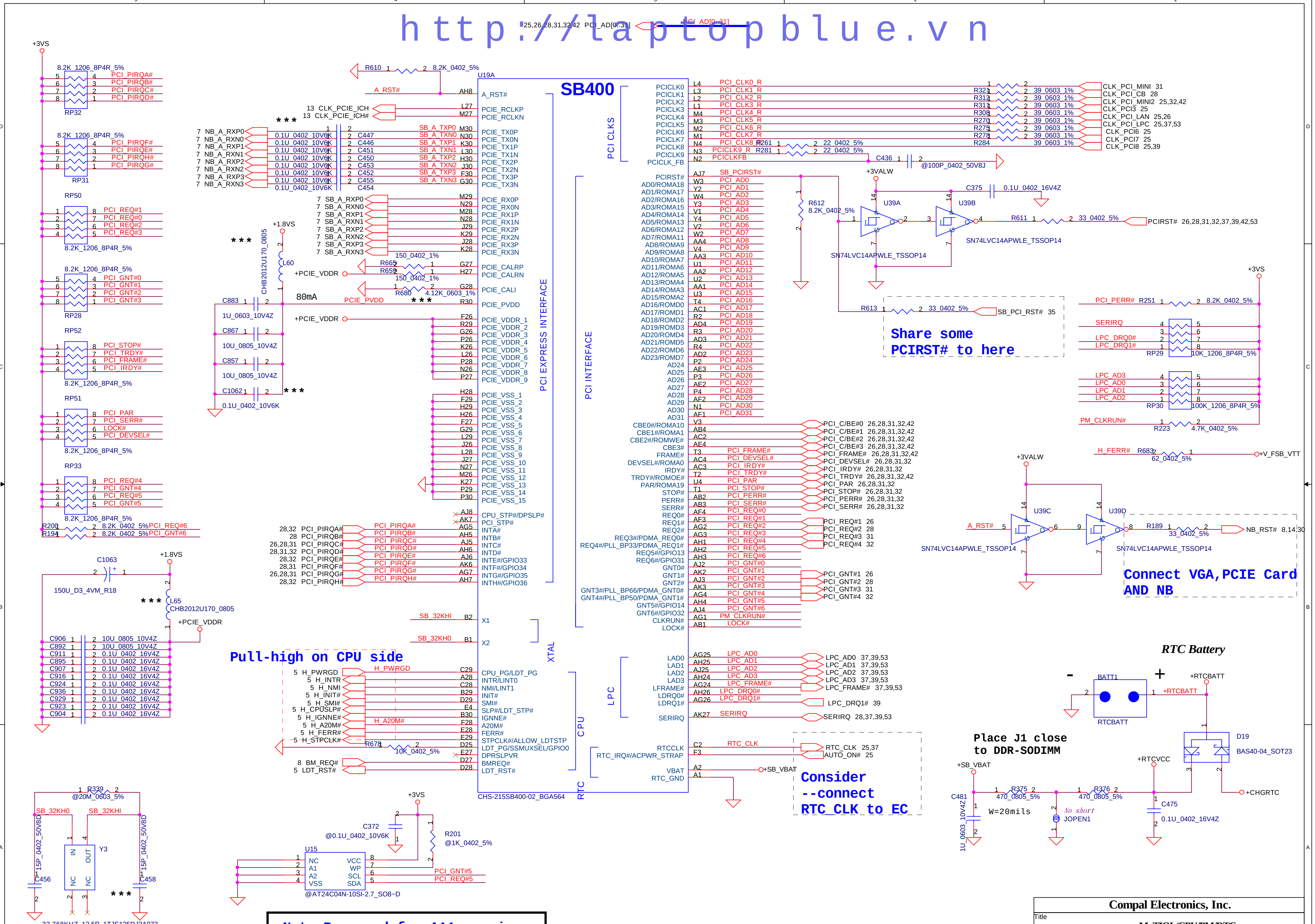
LVDS from NB



Compal Electronics, Inc.		
Title: CRT,TV-OUT,LVDS		
Size: Custom	Document Number: Longbeach 100 <LA-2451>	Rev: 0.1
Date: 星期六, 十一月 06, 2004	Sheet 19 of 53	



Compal Electronics, Inc.		
Title: CRT,DVI/SII1362		
Size: C	Document Number: Longbeach 100 <LA-2451>	Rev: 0.1
Date: 星期 ? 十一月 06, 2004	Sheet 20 of 53	



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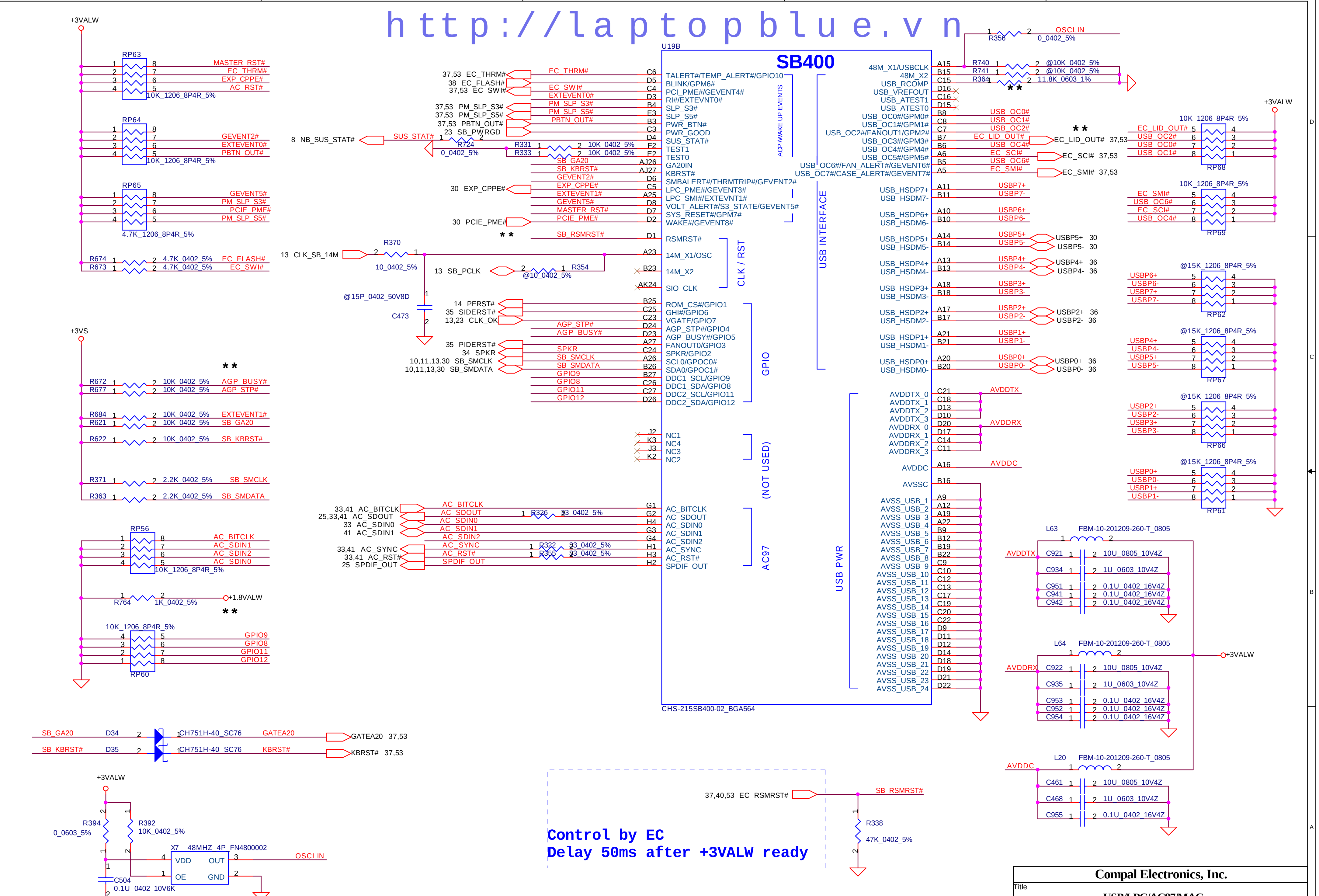
Title	MuTIOL/CPU/PM/RTC
Size	Document Number: Longbeach 100 <LA-2451>
Rev	0.1
Date: 星期六, 十一 ?06, 2004	Sheet 21 of 53



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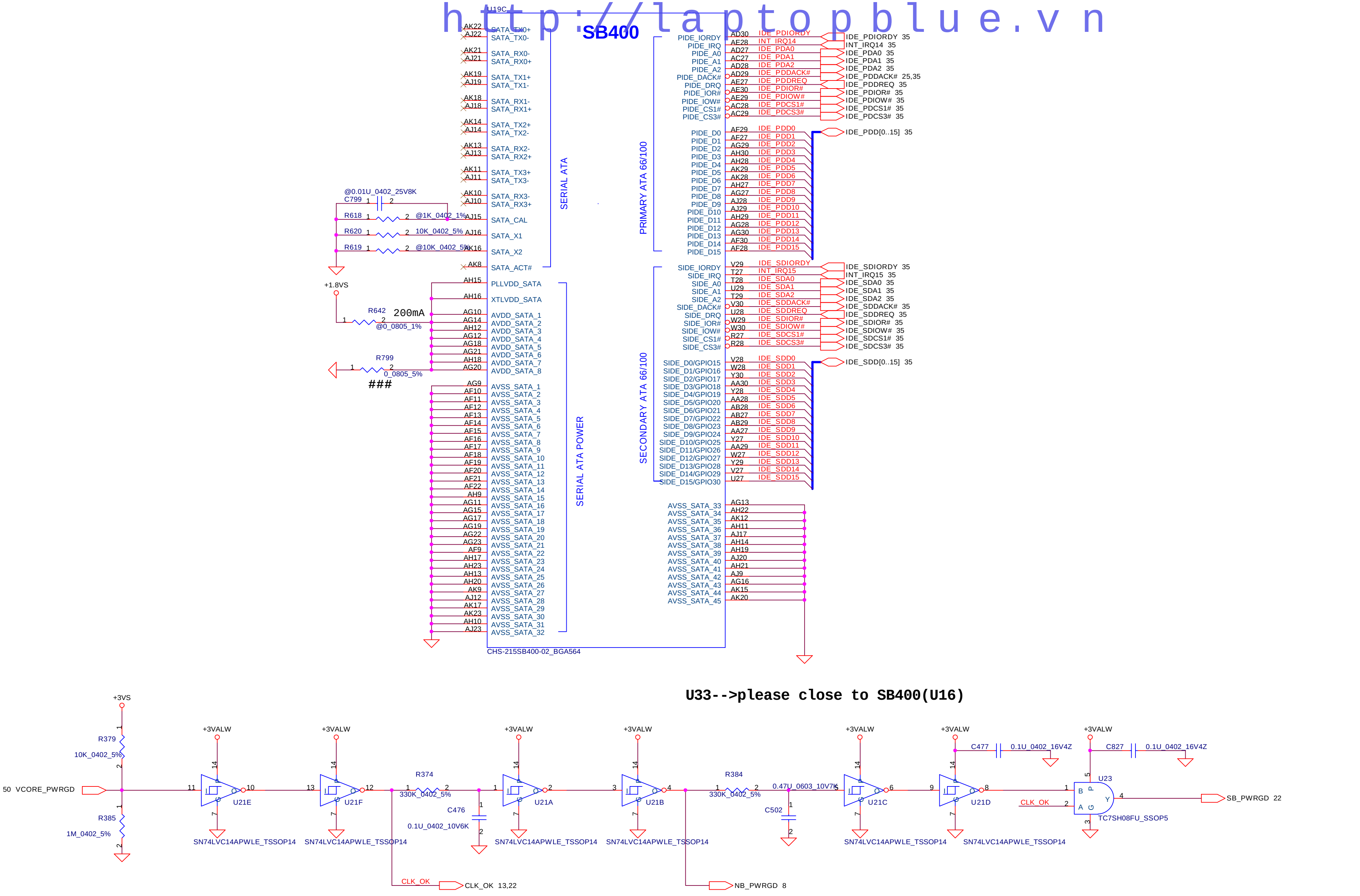
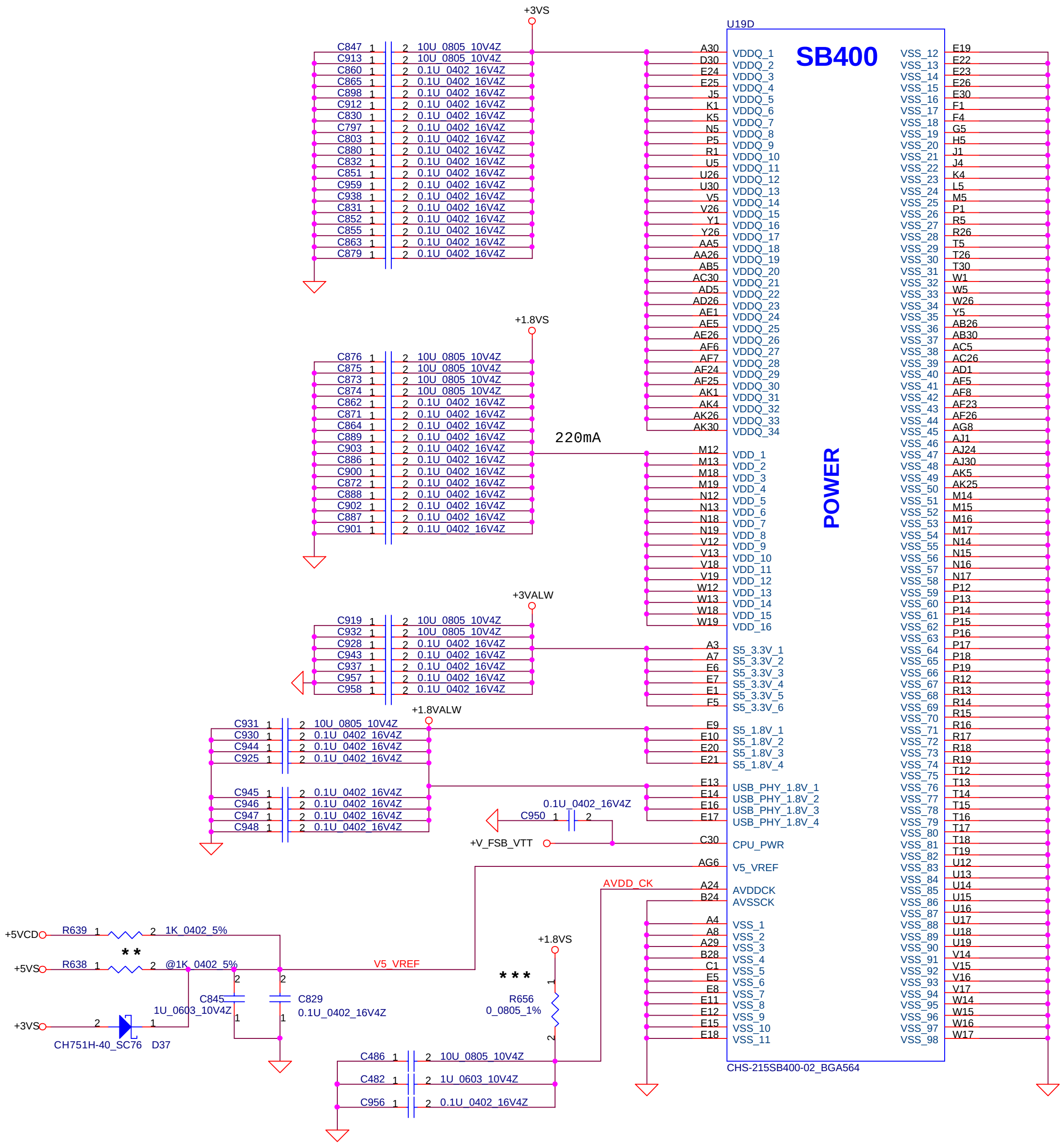
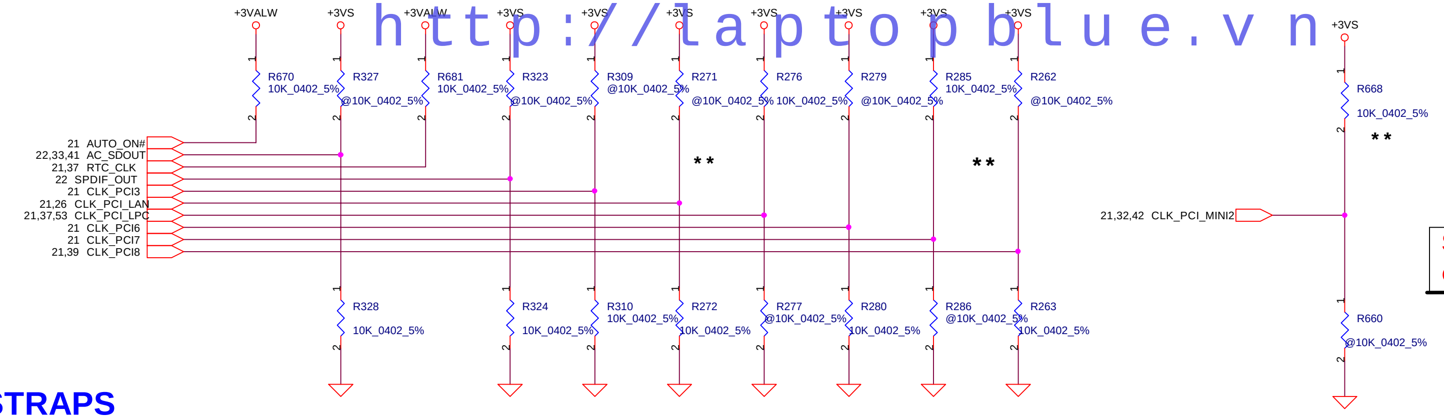
Title: USB/LPC/AC97/MAC		
Size	Document Number: Longbeach 100 <LA-2451>	Rev 0.1
Date: ¬P期六, 十一月 06, 2004	Sheet 22 of 53	



Compal Electronics, Inc.		
Title: IDE/SATA		
Size: Custom	Document Number: Longbeach 100 <LA-2451>	Rev: 0.1
Date: 星期六, 十一月 06, 2004	Sheet 23 of 53	



Compal Electronics, Inc.		
Title: **Power/GND**		
Size	Document Number: **Longbeach 100 <LA-2451>**	Rev 0.1
Date: 星期六, 十一 ?06, 2004	Sheet 24 of 53	

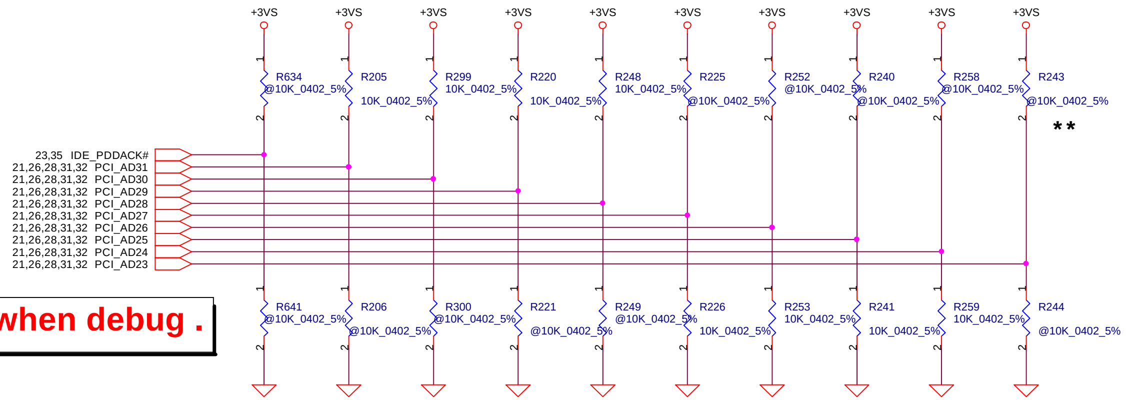


Selects type of 48MHz clock pad

REQUIRED STRAPS

ACPWRON

	AUTO_ON#	AC97_SDOUT	RTC_CLK	SPDIF_OUT	CLK_PCI3	CLK_PCI_LAN	CLK_PCI_LPC	PCI_CLK6	PCI_CLK7 PCI_CLK8	CLK_PCI_MINI2
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	USB PHY PWRDOWN DISABLE	Internal PLL	14MHz OSC MODE DEFAULT	CPU I/F = K8	ROM TYPE H,H = PCI ROM H,L = LPC ROM I L,H = LPC ROM II L,L = FWH ROM	Clock input buffer DEFAULT
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	USB PHY PWRDOWN ENABLE DEFAULT	External Clock DEFAULT	14MHz XTAL MODE	CPU I/F = P4 DEFAULT		Crytsal Pad

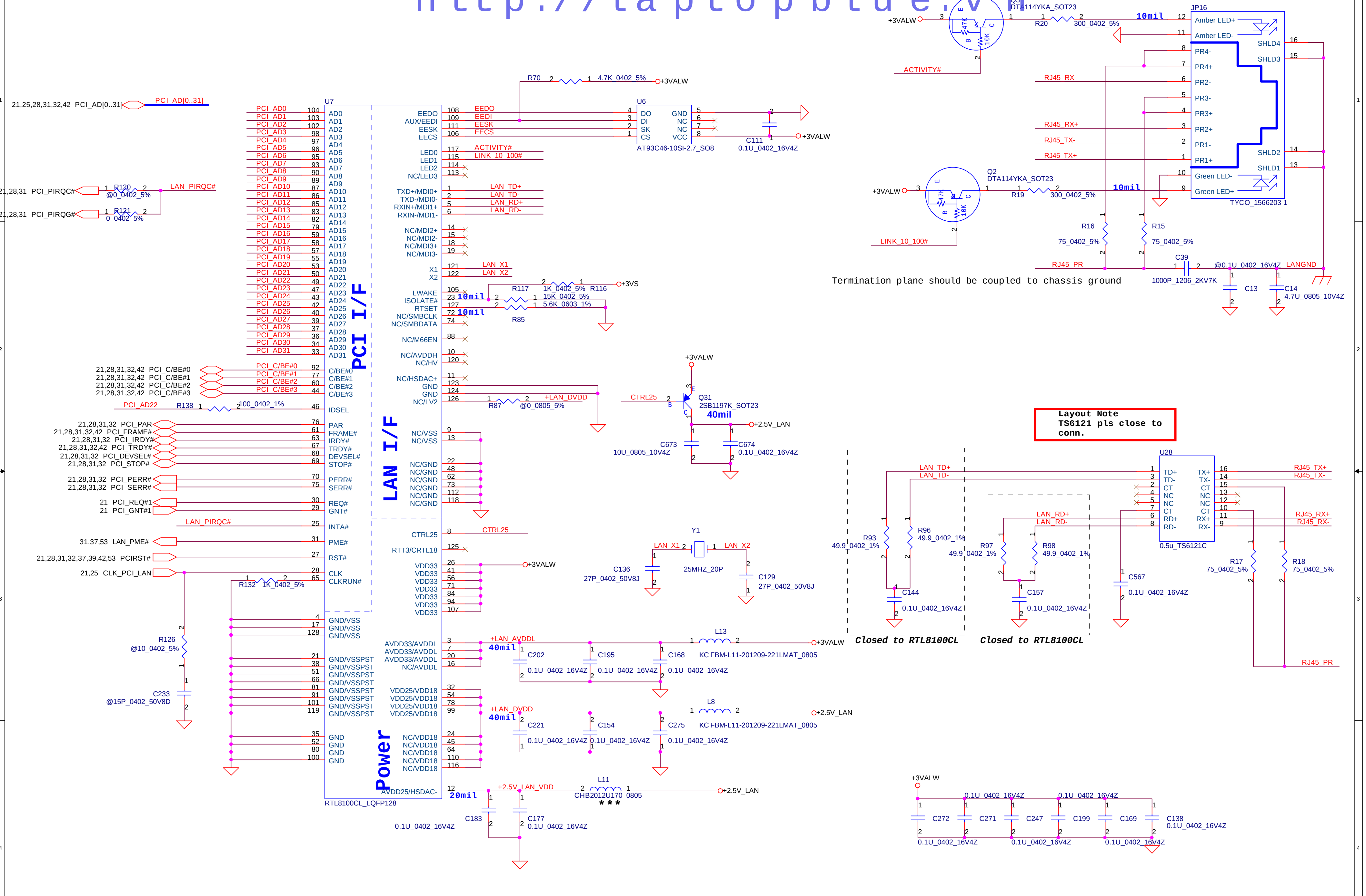


Pop R634 when debug .

DEBUG STRAPS

	IDE_PDDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24
PULL HIGH	USE LONG RESET DEFAULT	PLL CHARGE PUMP CTRL BIT 1 HI DEFAULT	PLL CHARGE PUMP CTRL BIT 0 HI DEFAULT	PLL VCO CTRL BIT 1 HI DEFAULT	PLL VCO CTRL BIT 0 HI DEFAULT	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS
PULL LOW	USE SHORT RESET	PLL CHARGE PUMP CTRL BIT 1 LO	PLL CHARGE PUMP CTRL BIT 0 LO	PLL VCO CTRL BIT 1 LO	PLL VCO CTRL BIT 0 LO	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT

Compal Electronics, Inc.
Title: Hardware Trap
Size | Document Number: Longbeach 100 <LA-2451> | Rev 0.1
Date: 星期六, 十一 ?06, 2004 | Sheet 25 of 53



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Title: **Ethernet RTL8100CL**

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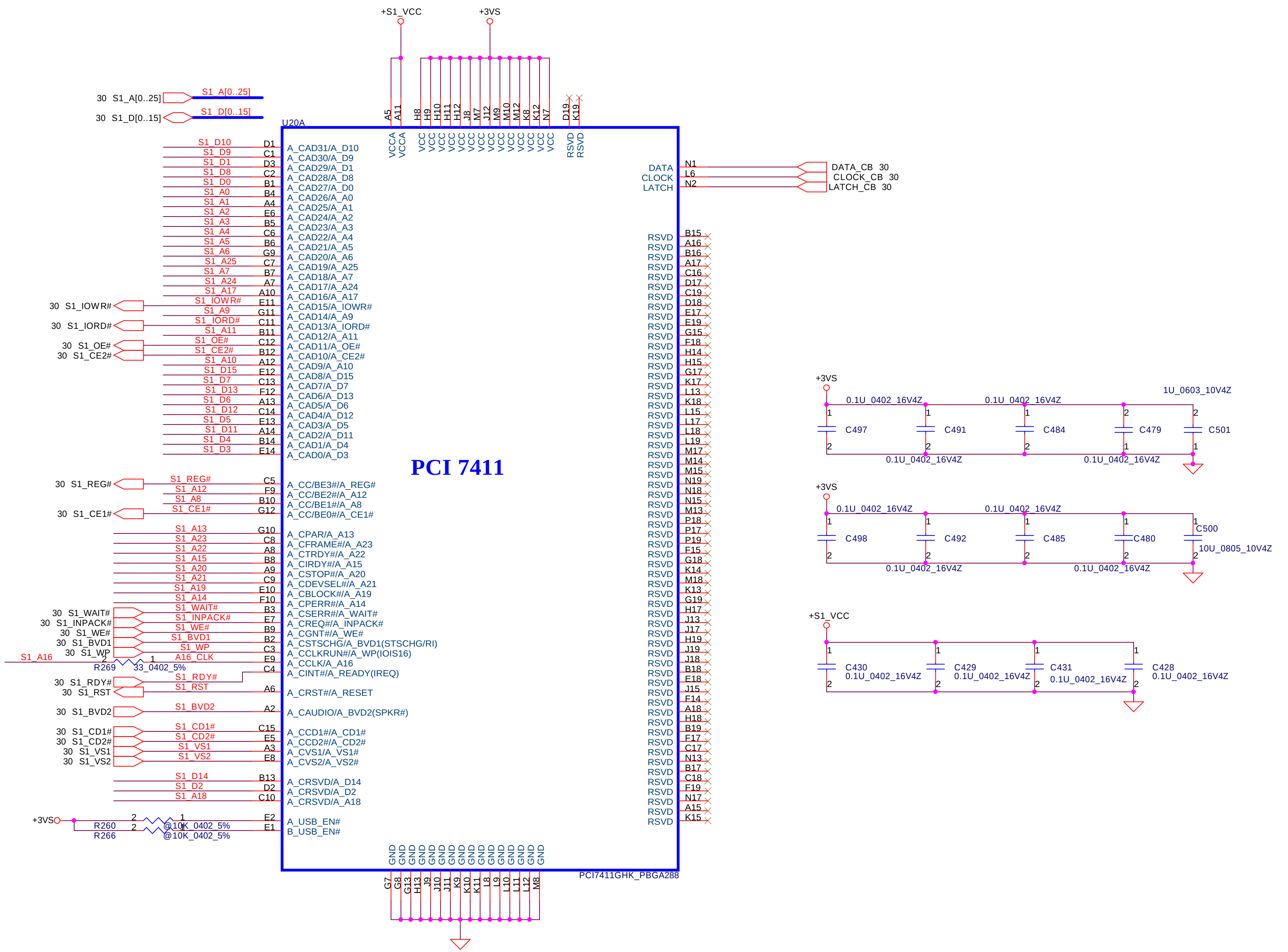
		0.1

Date: 星期六, 十一 ?06, 2004 | Sheet 26 of 53



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Size: Custom	Document Number: Longbeach 100 <LA-2451>		Rev: 0.1
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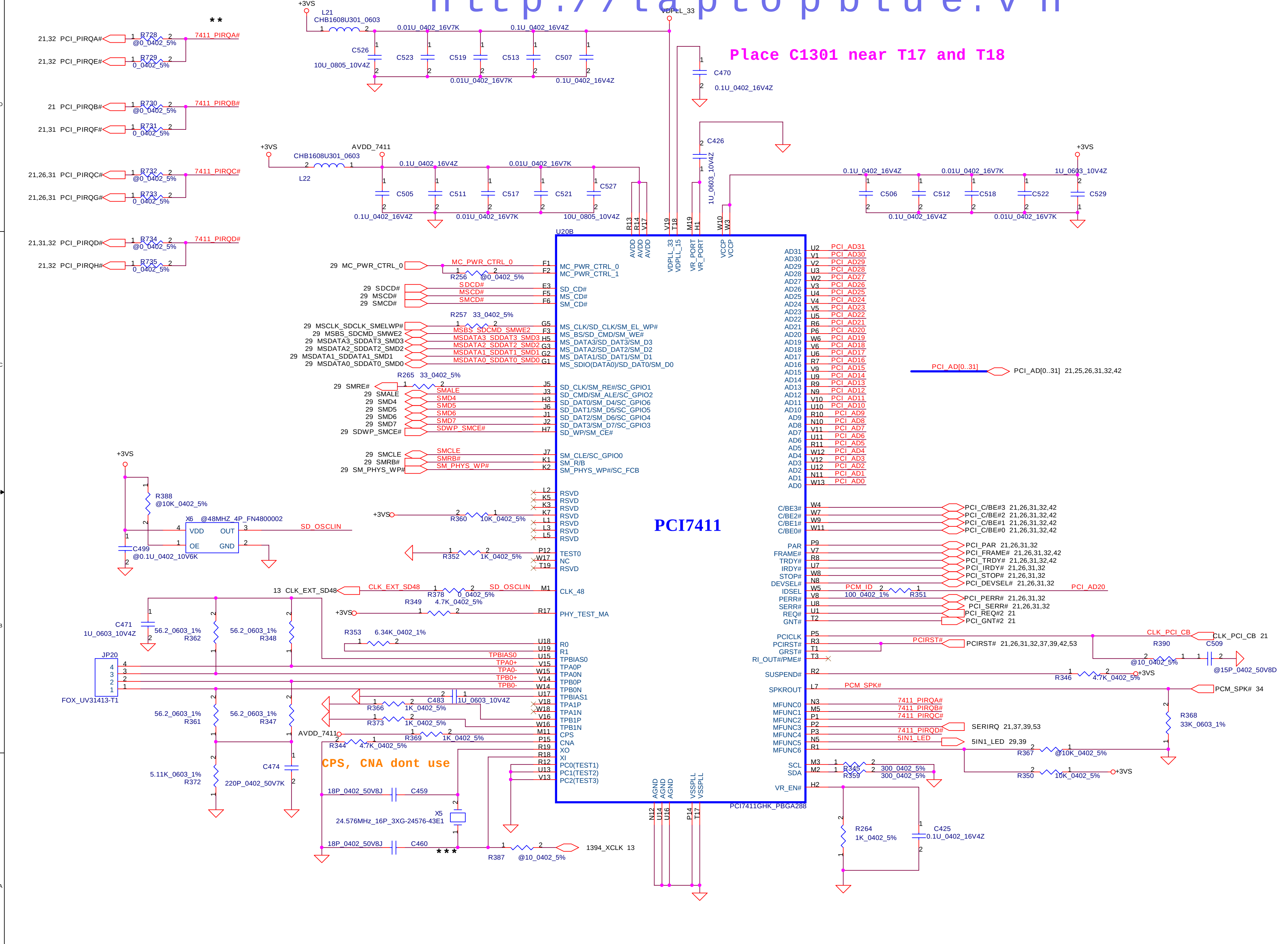

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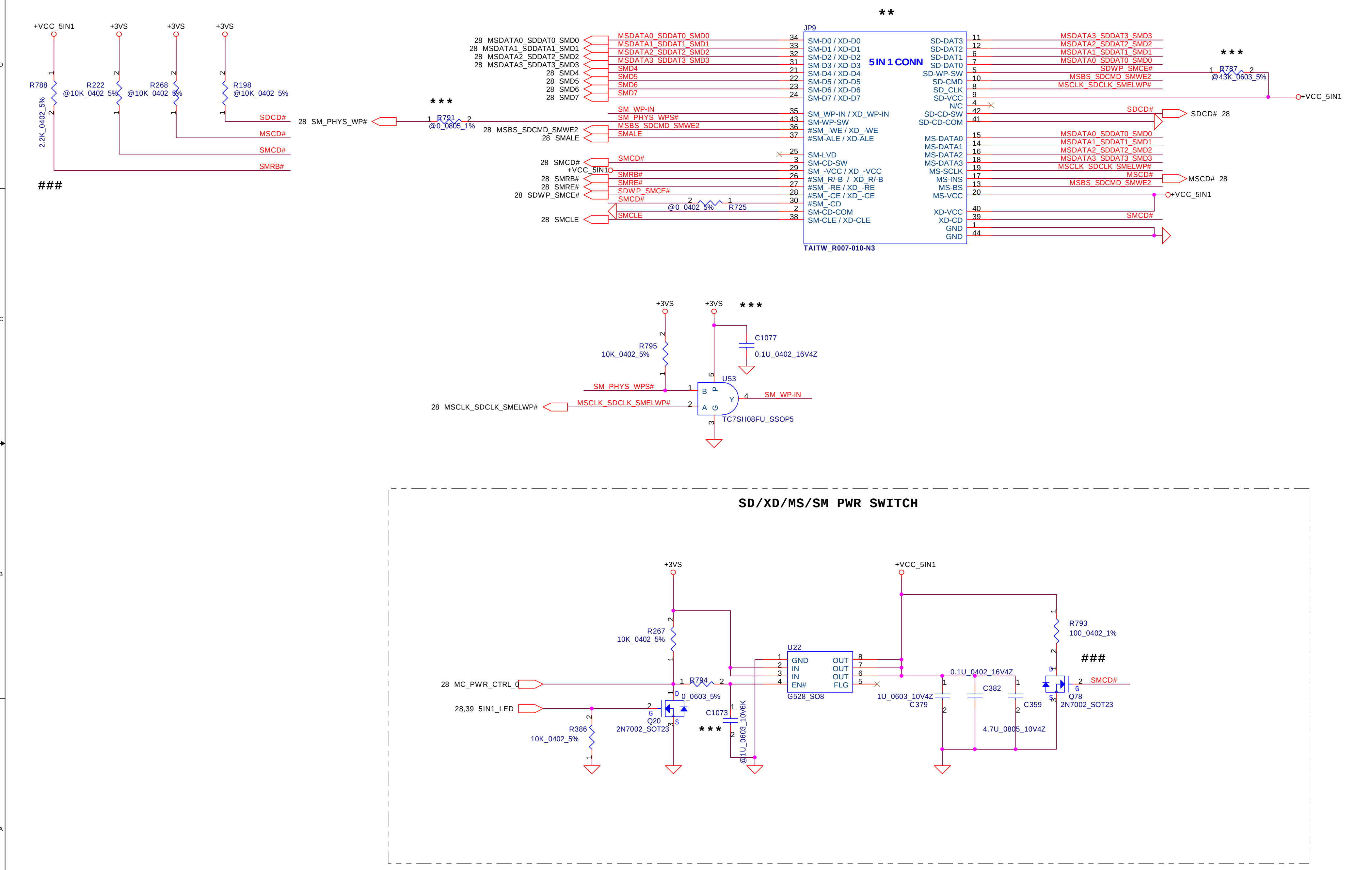
Title	PCI7411-2	
Size Custom	Document Number Longbeach 100 <LA-2451>	Rev 0.1
Date: 星期六, 十一月 06, 2004	Sheet 28 of 53	



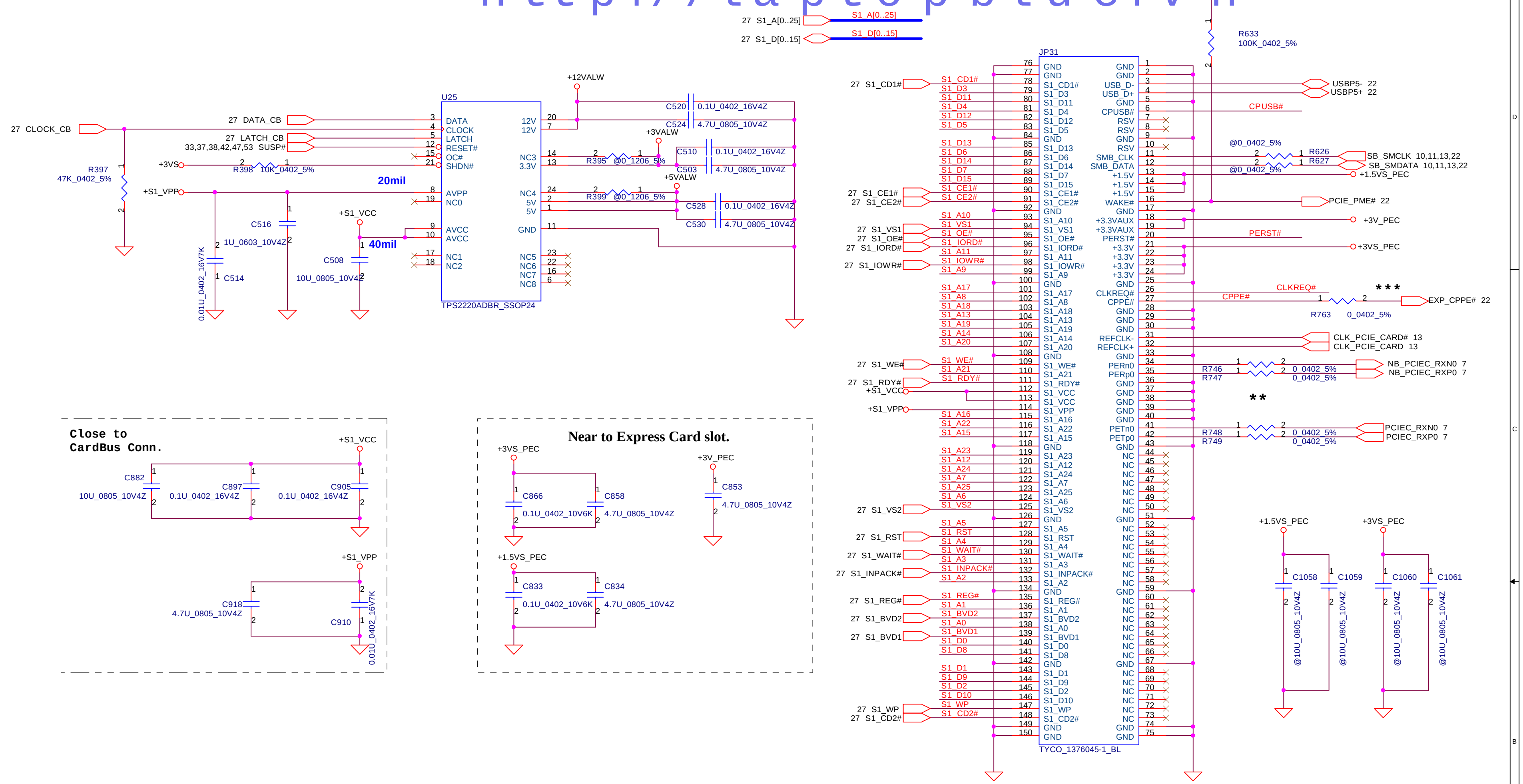
Title: CardBus & PCI-E Socket ,5IN 1 CON

Size: Custom | Document Number | Rev 0.1

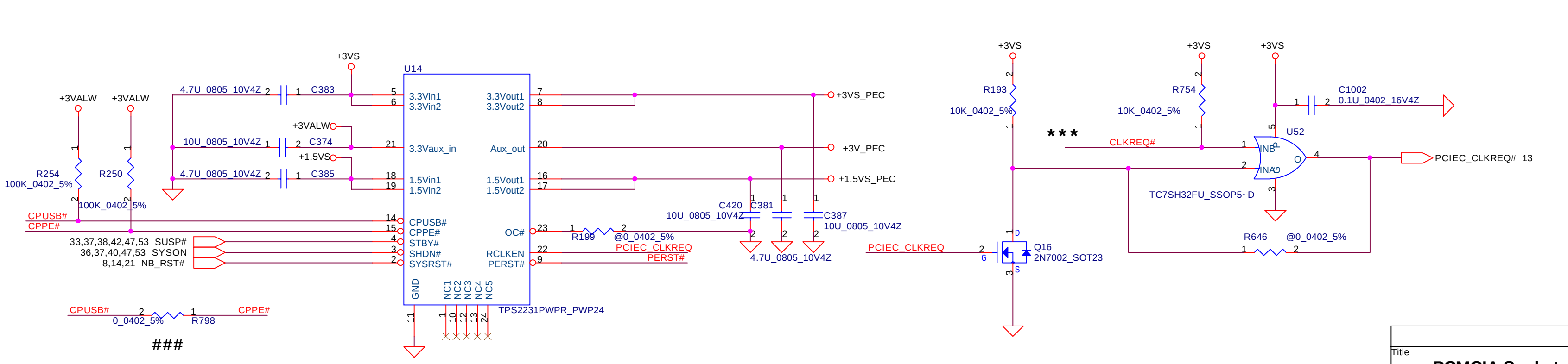
Date: 星期六, 十一月 06, 2004

Power Switch for PCMCIA

CardBus & PCI-E Socket

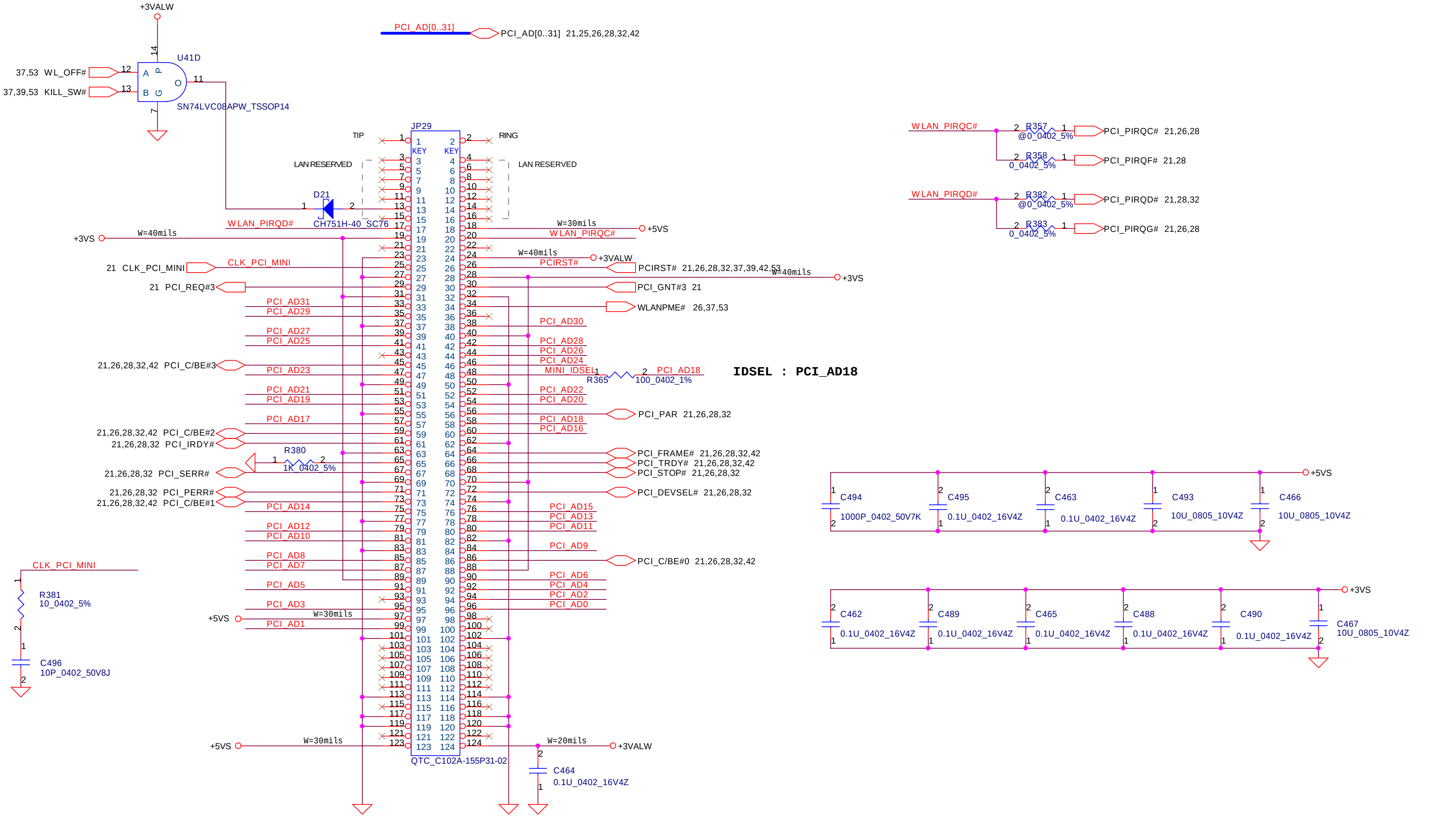


Power Switch for PCI-E



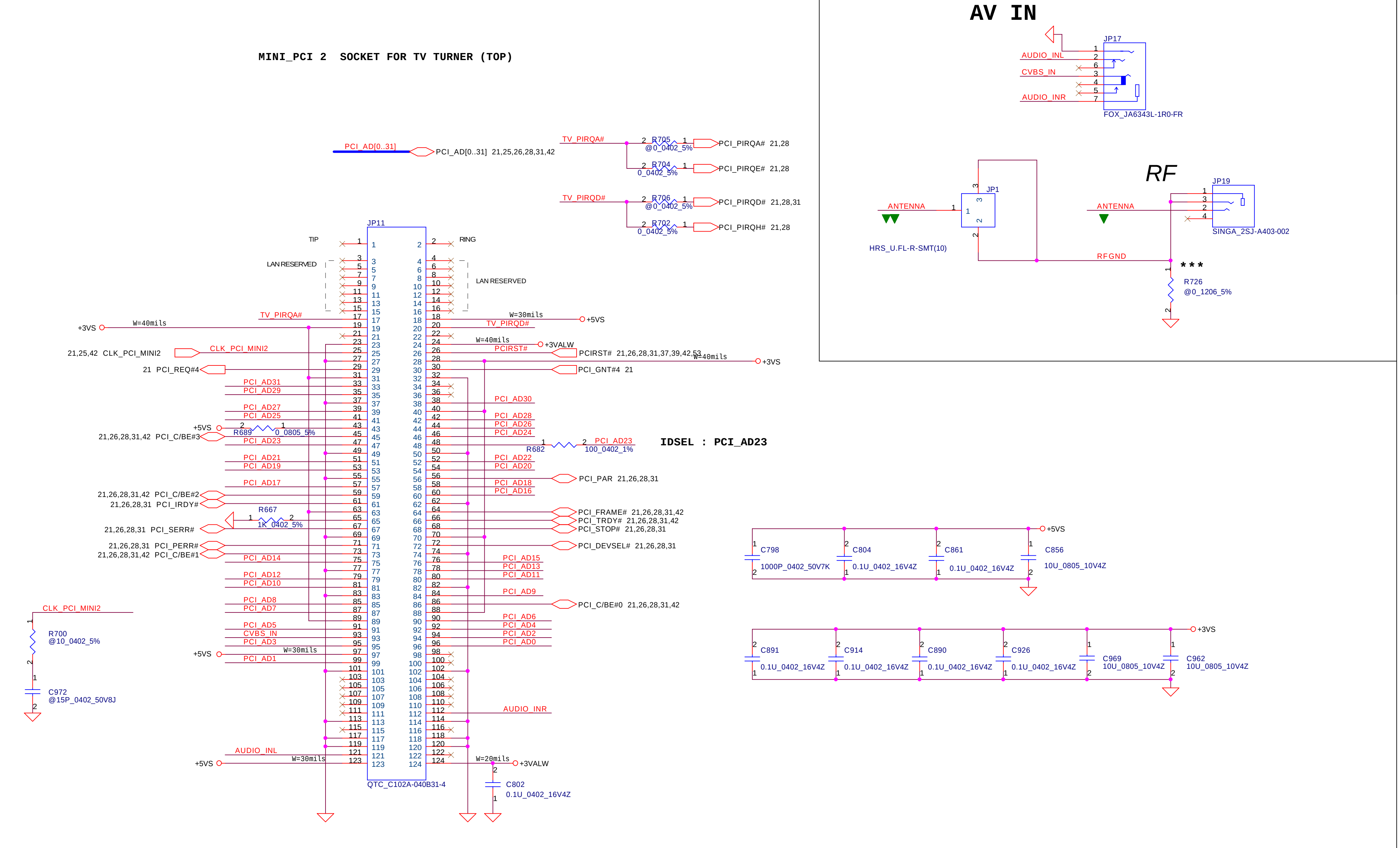
Title	PCMCIA Socket	
Size Custom	Document Number Longbeach 100 <LA-2451>	Rev 0.1
Date: 星期六, 十一月 06, 2004	Sheet 30 of 53	

MINI_PCI 1 SOCKET FOR WLAN (BOTTOM)



Compal Electronics, Inc.		
Title	MINI_PCI-WLAN	
Size Custom	Document Number Longbeach 100 <LA-2451>	Rev 0.1
Date: 星期六, 十一月 06, 2004	Sheet 31 of 53	

TV-Tuner

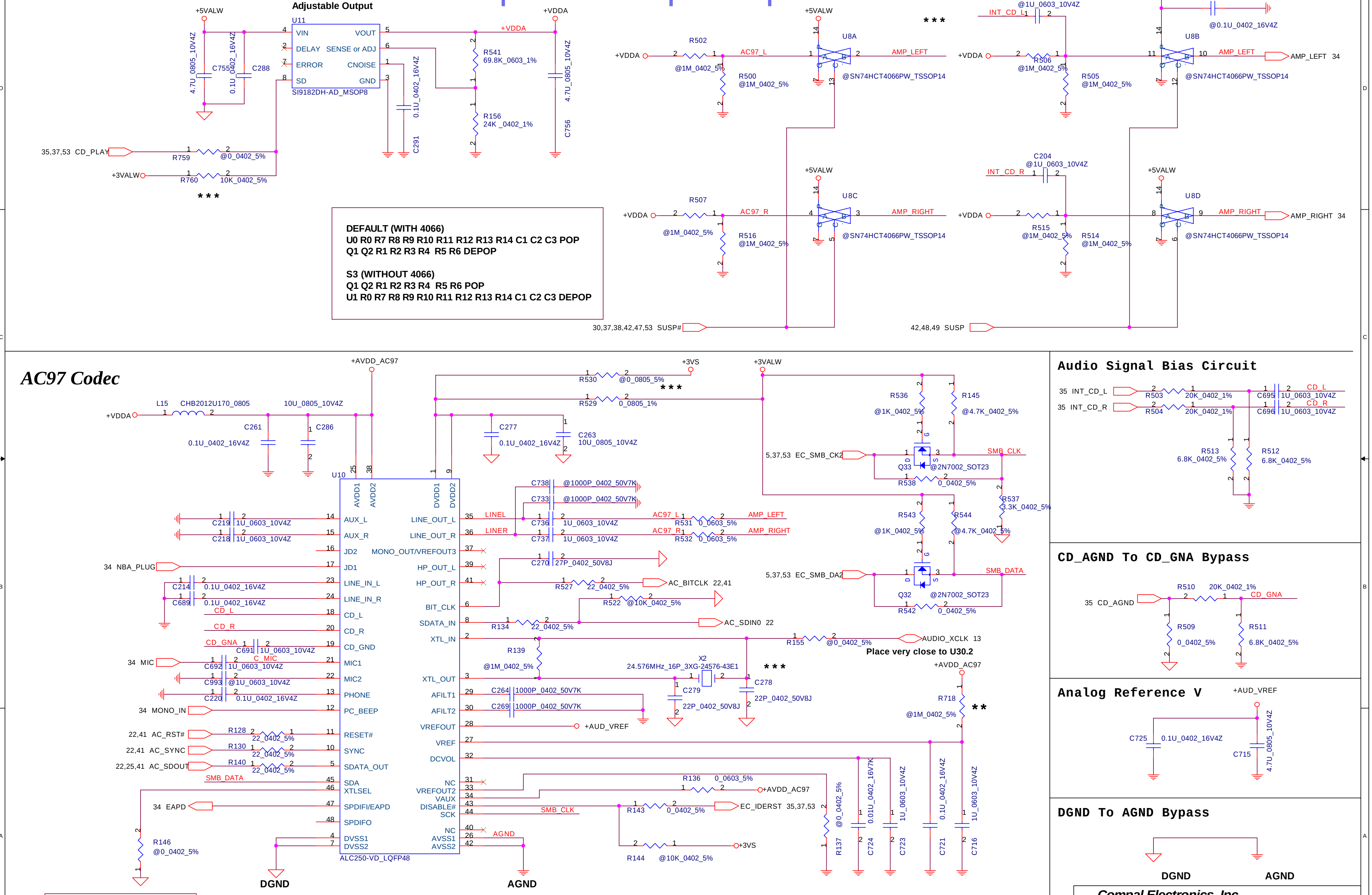


Compal Electronics, Inc.

Title: MINI_PCI-TV Tuner

Size: Custom | Document Number: Longbeach 100 <LA-2451> | Rev 0.1

Date: 星期六, 十一月 06, 2004 | Sheet 32 of 53

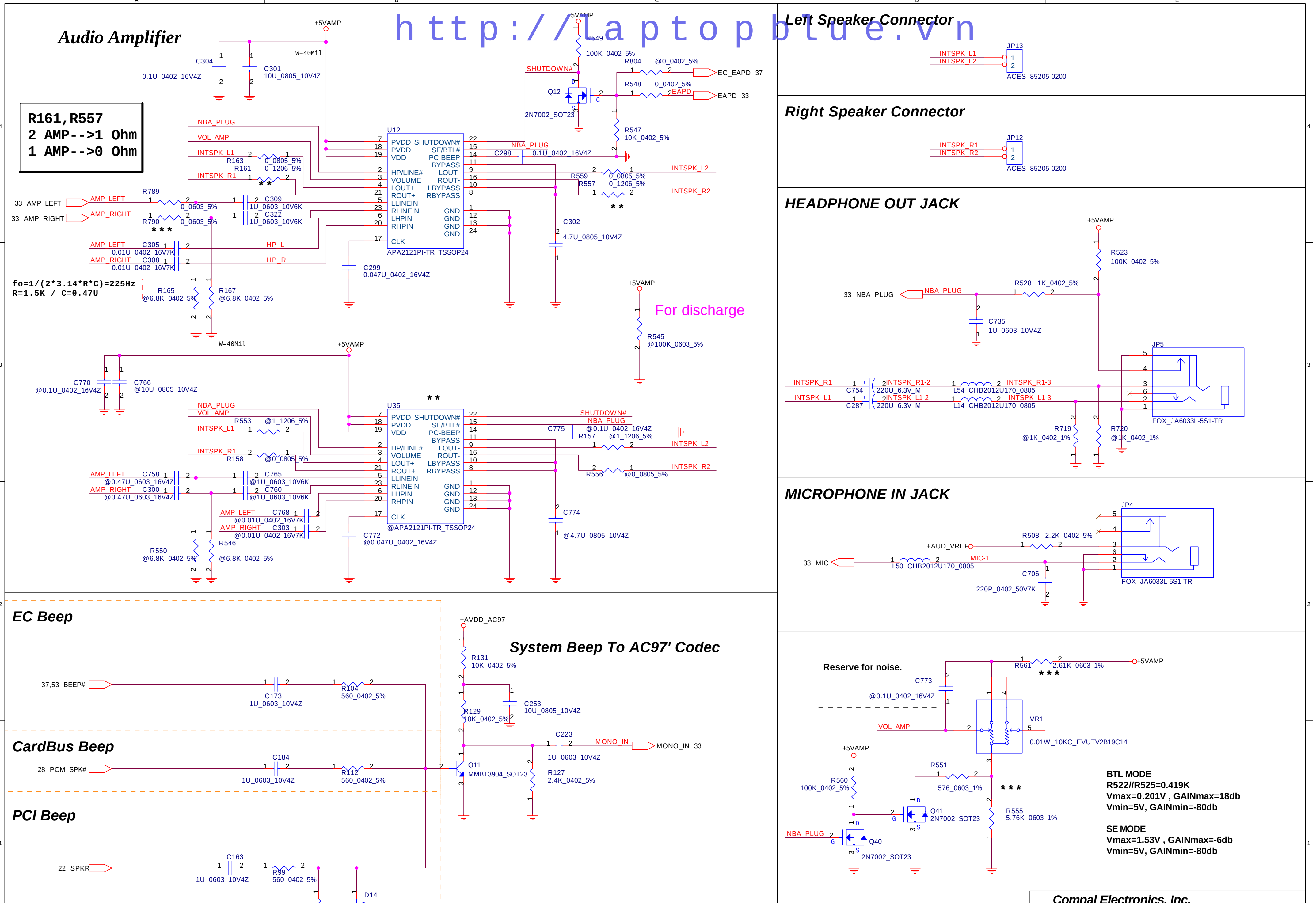


DEFAULT (WITH 4066)
U0 R0 R7 R8 R9 R10 R11 R12 R13 R14 C1 C2 C3 POP
Q1 Q2 R1 R2 R3 R4 R5 R6 DEPOP

S3 (WITHOUT 4066)
Q1 Q2 R1 R2 R3 R4 R5 R6 POP
U1 R0 R7 R8 R9 R10 R11 R12 R13 R14 C1 C2 C3 DEPOP

WITH 14.318MHz : Rxxx POP
WITH 24.576MHz : Rxxx DEPOP

Compal Electronics, Inc.		
Title	AC97 Codec	
Size: Custom	Document Number: Longbeach 100 <LA-2451>	Rev: 0.1
Date: 星期六, 十一月 06, 2004	Sheet 33 of 53	



PROPRIETARY NOTE

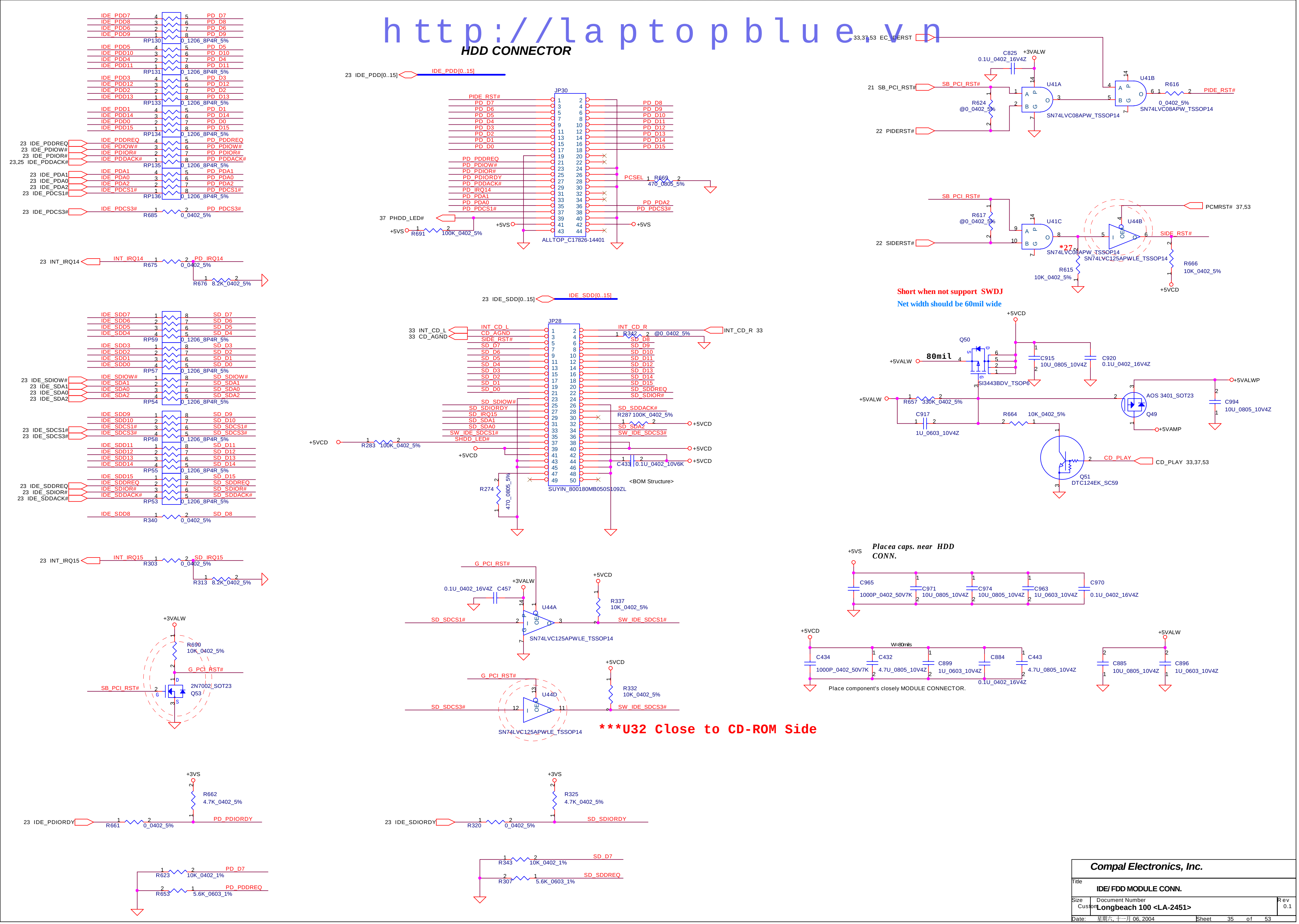
Compal Electronics, Inc.

Title: AMP & Audio Jack

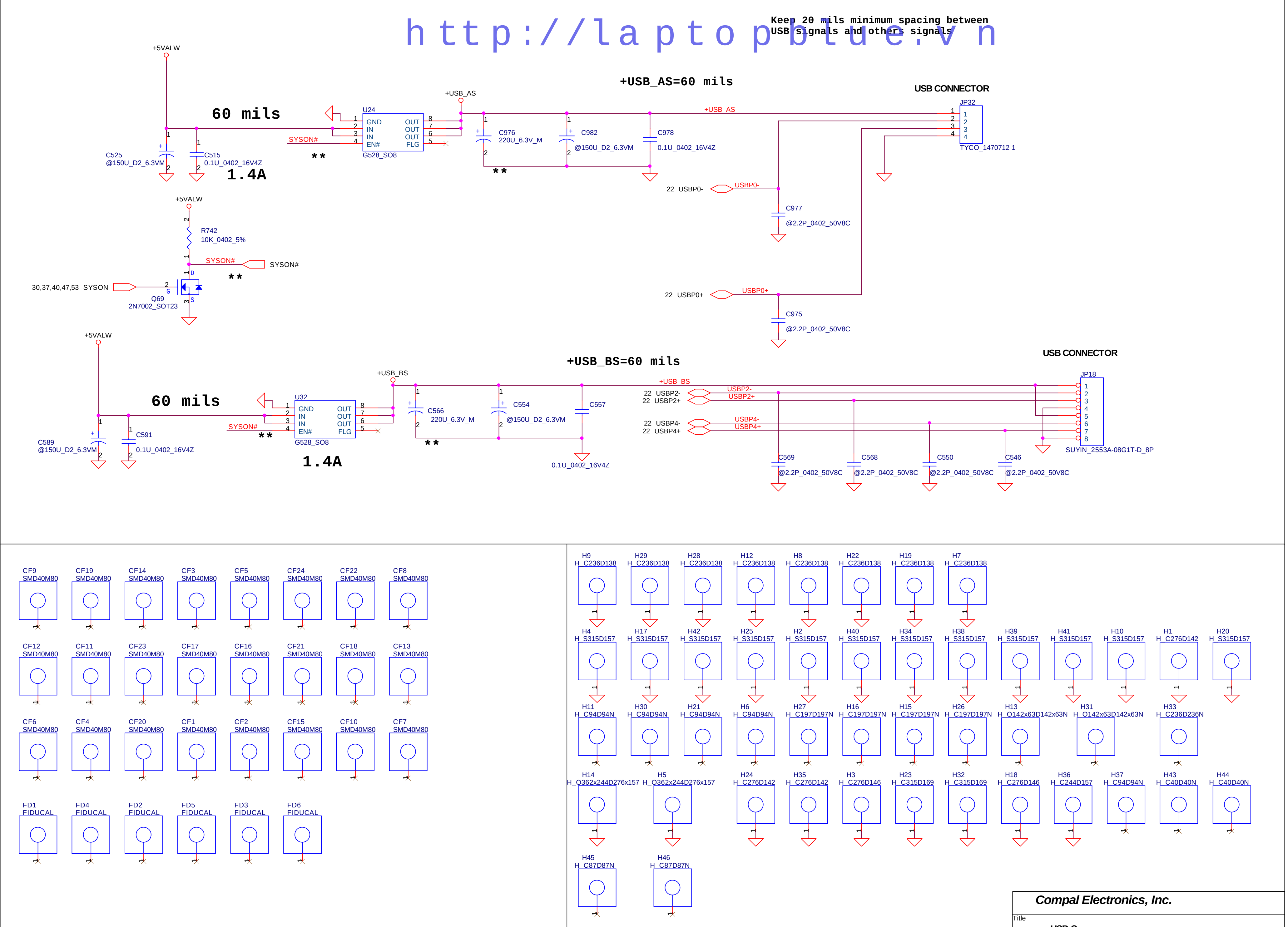
Size: Custom | Document Number: Longbeach 100 <LA-2451> | Rev: 0.1

Date: 星期六, 十一月 06, 2004 | Sheet 34 of 53

HDD CONNECTOR



Compal Electronics, Inc.			
Title	IDE/ FDD MODULE CONN.		
Size: Custom	Document Number: Longbeach 100 <LA-2451>		Rev: 0.1
Date: 星期六, 十一月 06, 2004	Sheet 35 of 53		

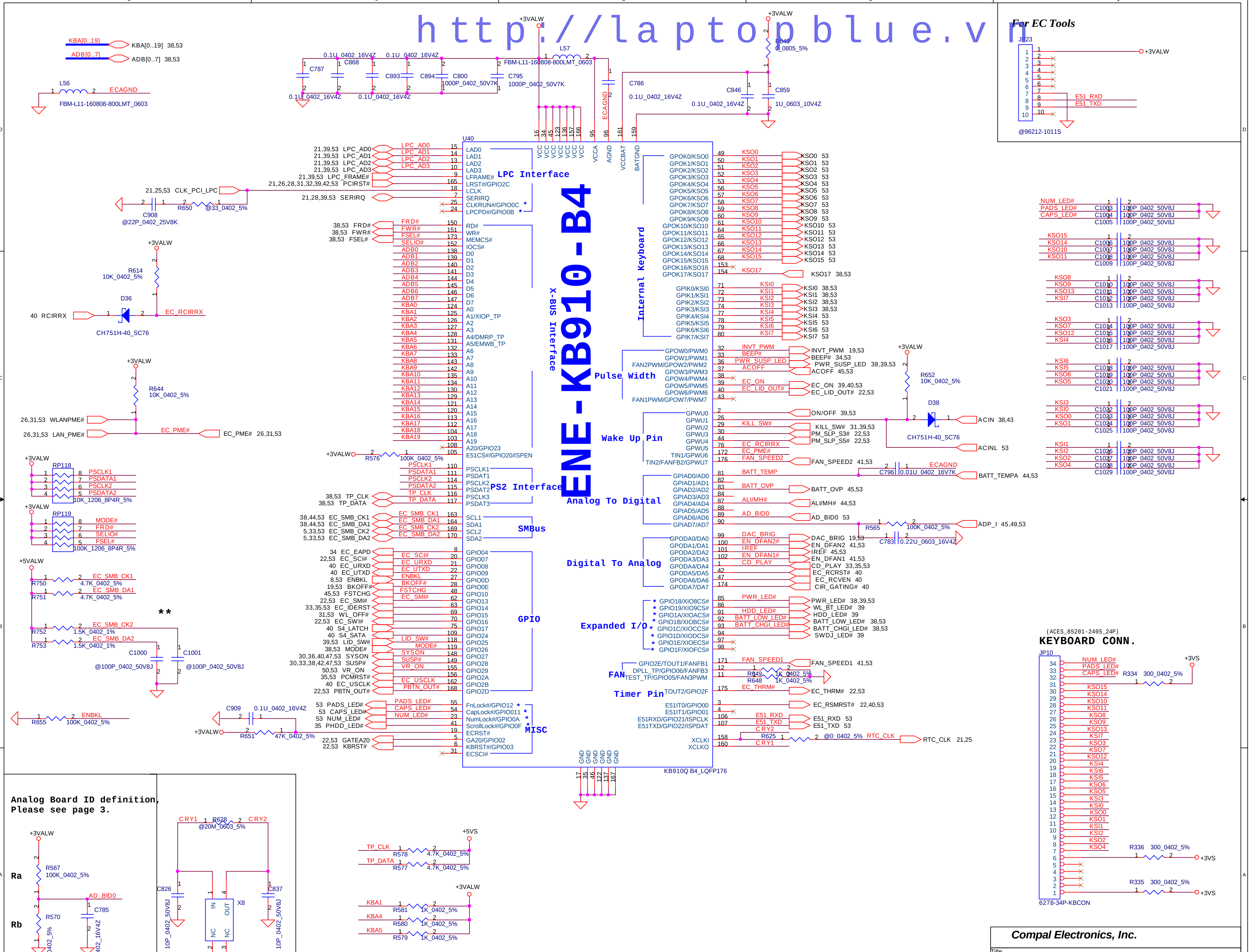


Compal Electronics, Inc.

Title: USB Conn.

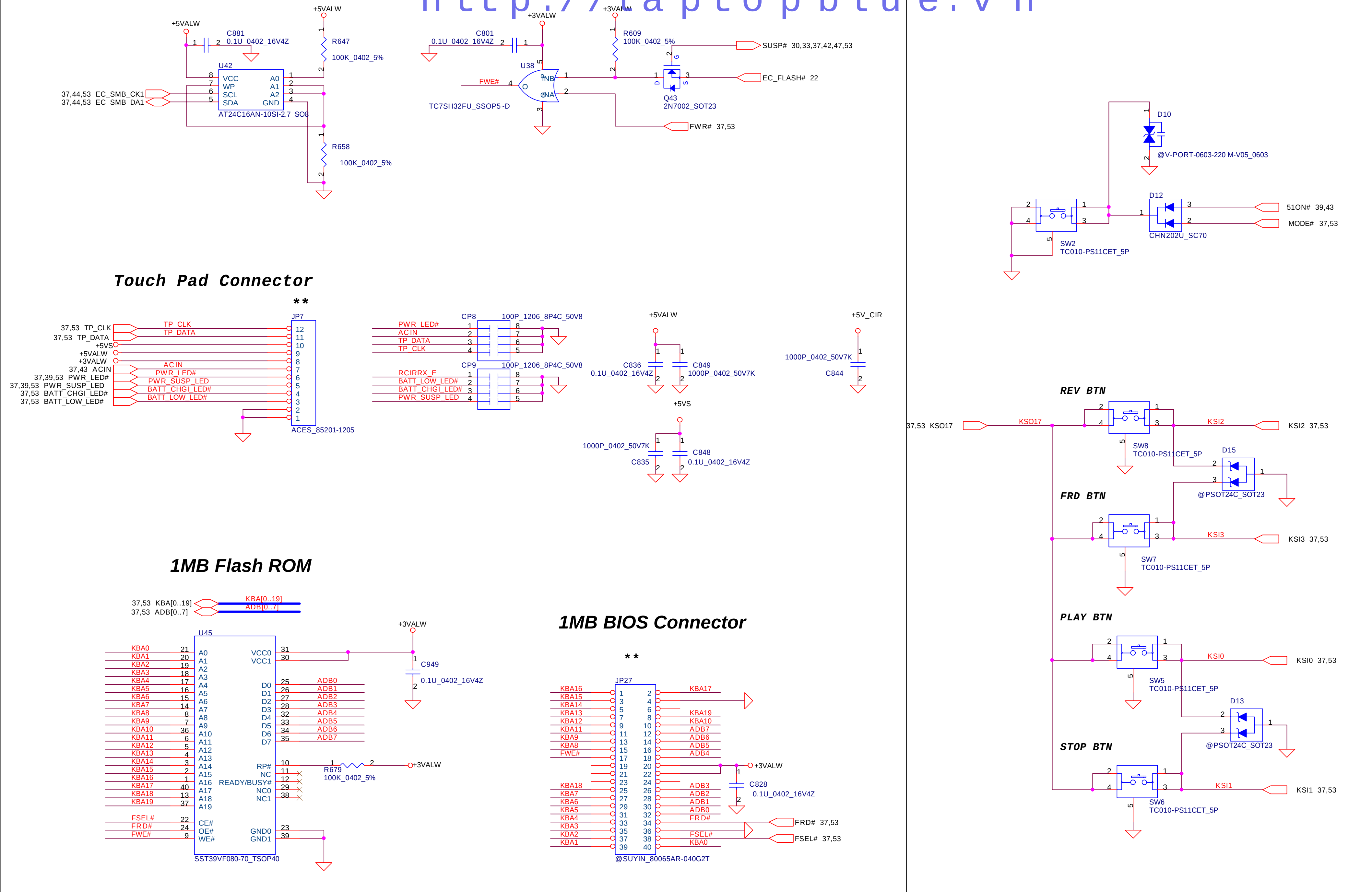
Size: Custom | Document Number: Longbeach 100 <LA-2451> | Rev 0.1

Date: 星期六, 十一 ?06, 2004 |

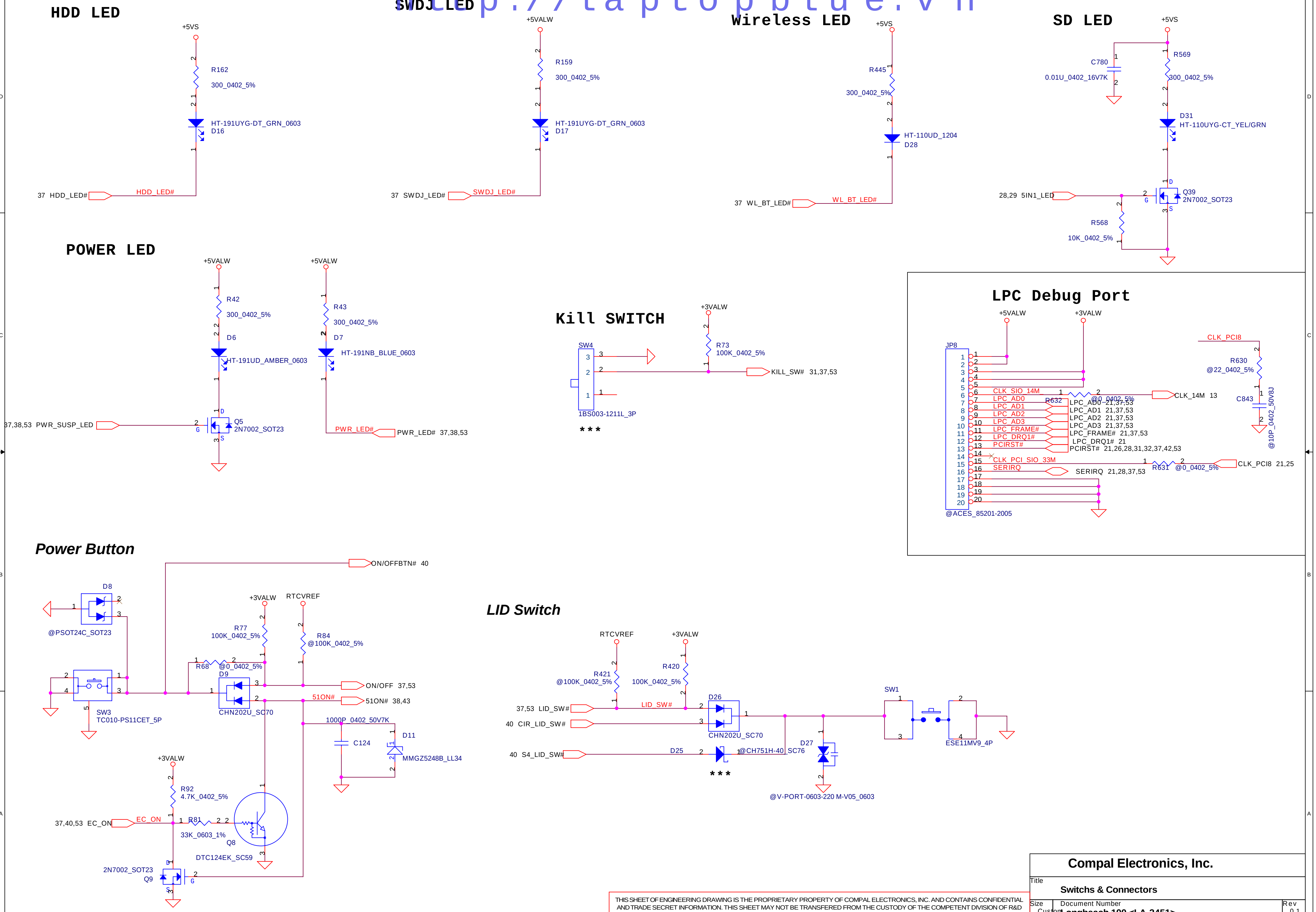


Compal Electronics, Inc.

Title	ENE-KB910	
Size: Custom	Document Number: Longbeach 100 <LA-2451>	Rev: 0.1
Date: 星期六, 十一月 06, 2004	Sheet 37 of 53	

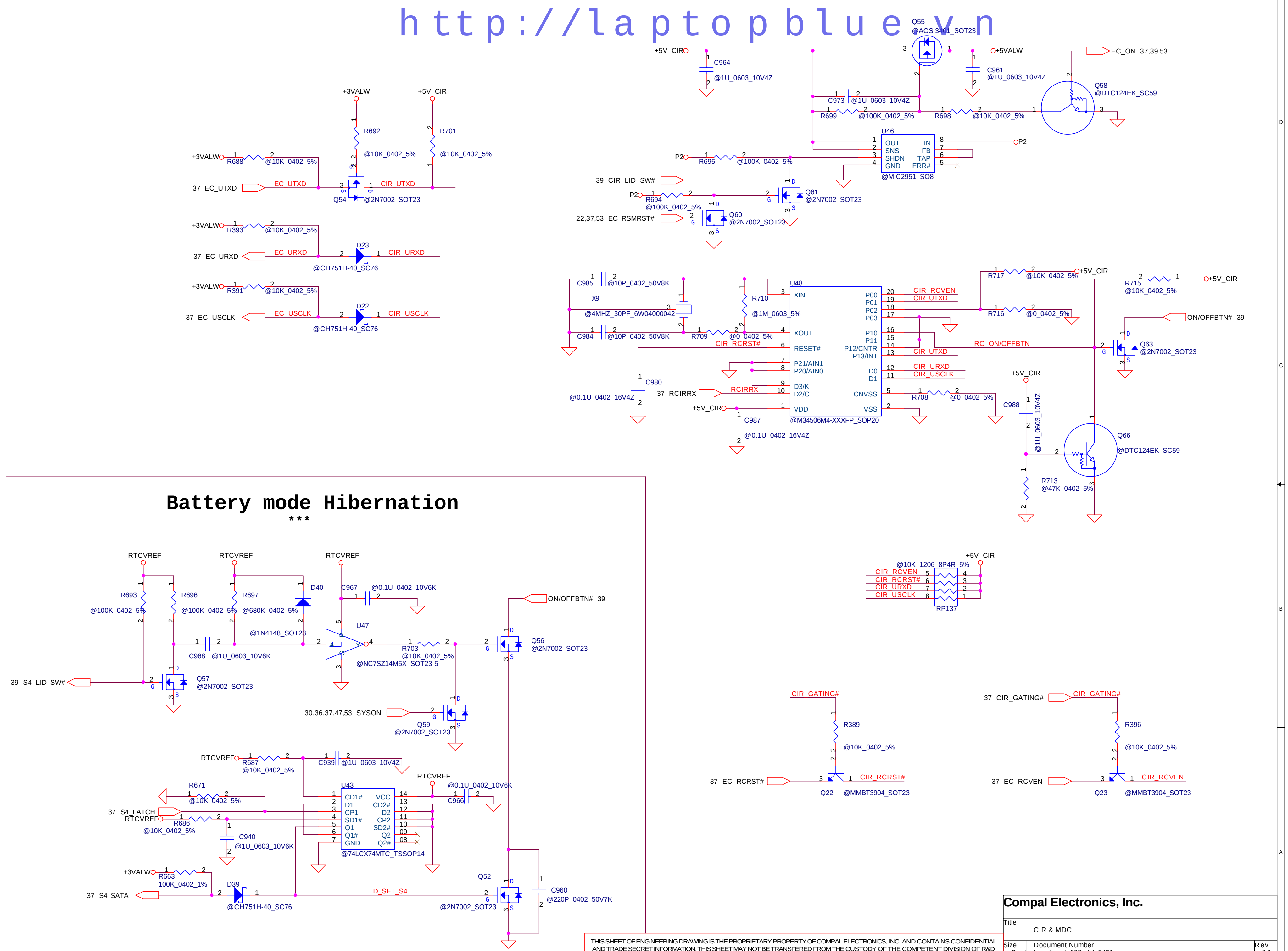


Compal Electronics, Inc.		
Title: BIOS & EXT. I/O PORT		
Size: Custom	Document Number: Longbeach 100 <LA-2451>	Rev: 0.1
Date: 星期六, 十一月 06, 2004	Sheet 38 of 53	

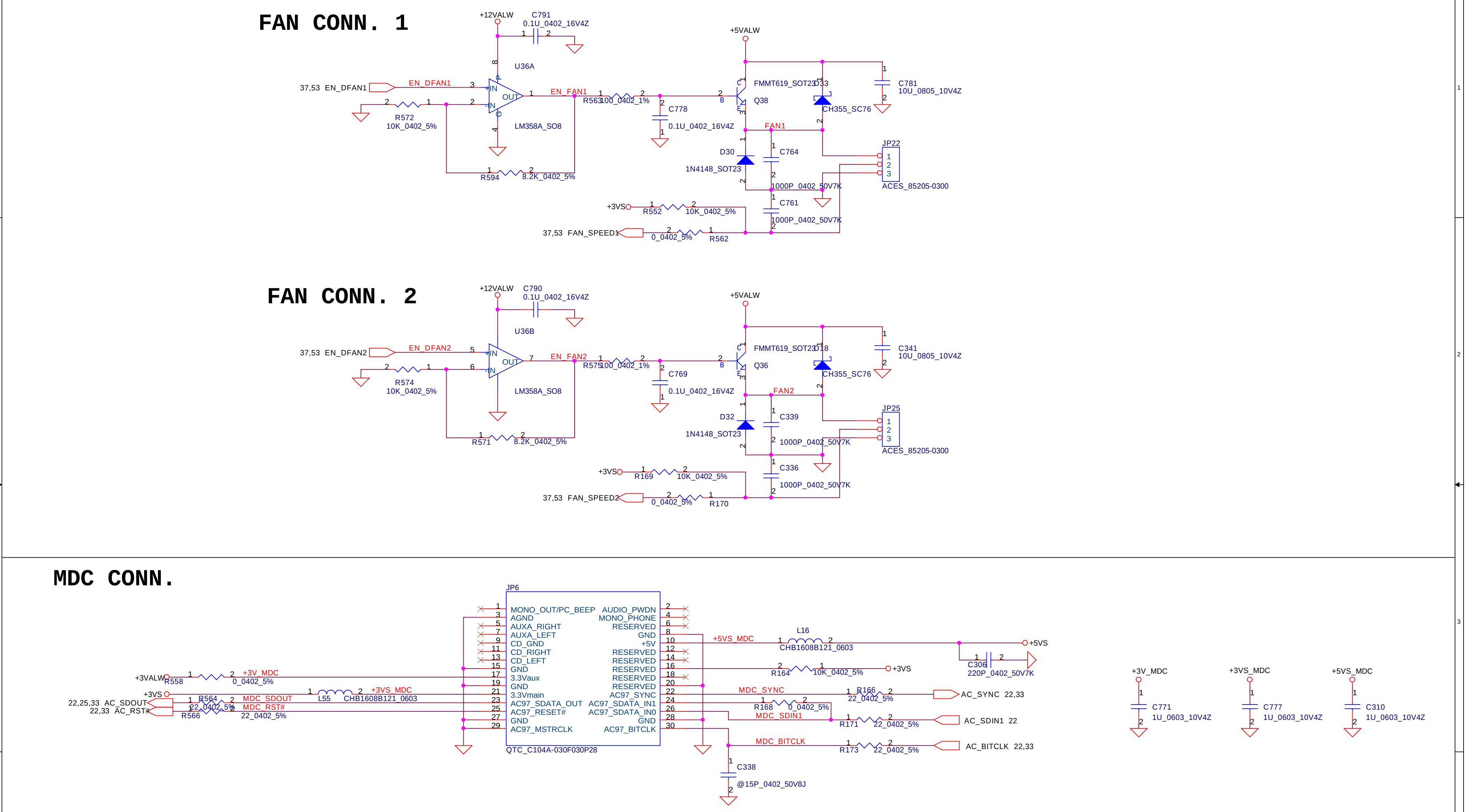


Compal Electronics, Inc.

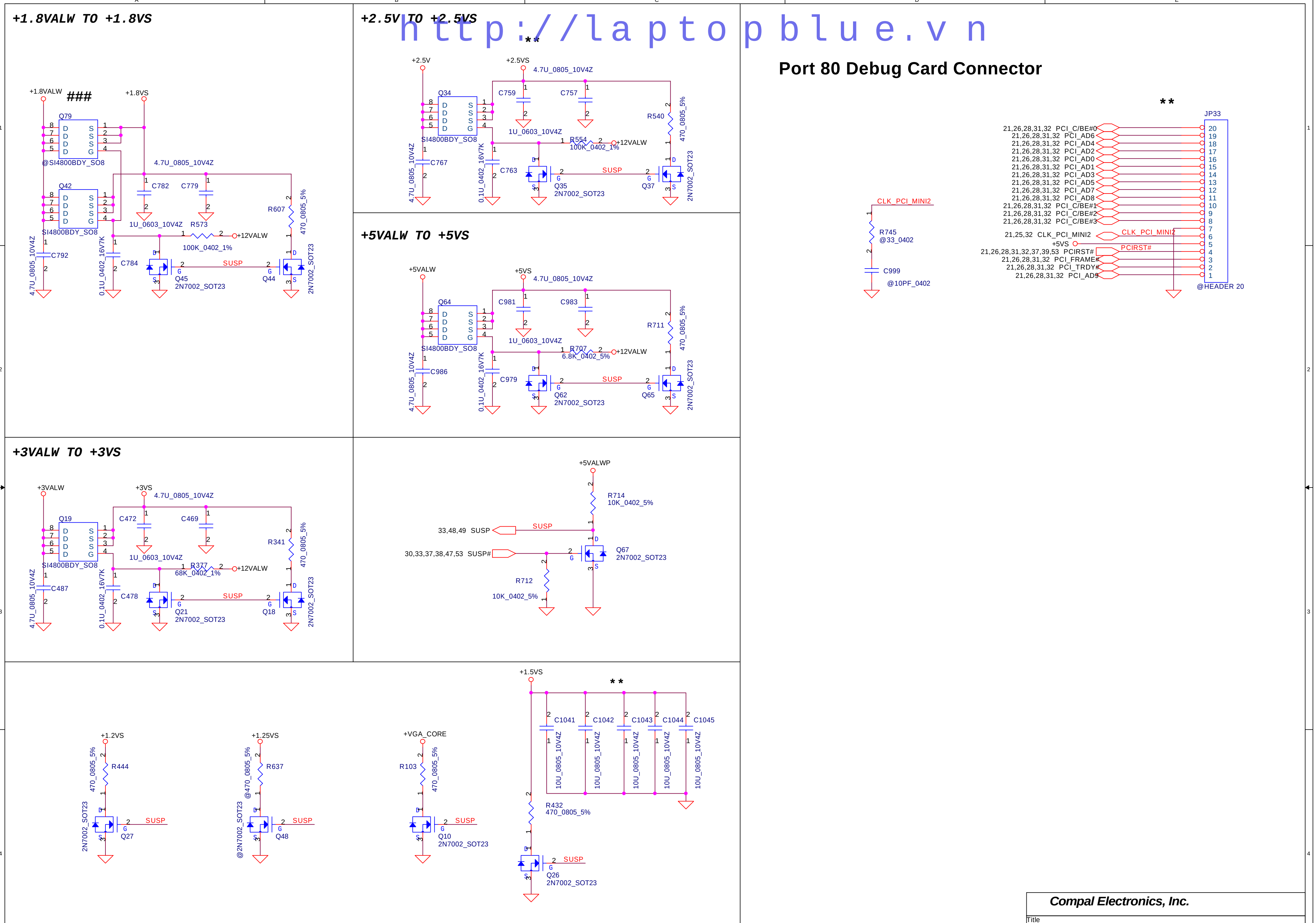
Title	Switchs & Connectors
Size: Custom	Document Number: Longbeach 100 <LA-2451>
Rev	0.1
Date: 星期六, 十一月 06, 2004	Sheet 39 of 53



Compal Electronics, Inc.		
Title	CIR & MDC	
Size Custom	Document Number Longbeach 100 <LA-2451>	Rev 0.1
Date: 星期六, 十一月 06, 2004	Sheet 40 of 53	



Compal Electronics, Inc.		
Title: FAN & MDC		
Size	Document Number: Longbeach 100 <LA-2451>	Rev 0.1
Date: 星期六, 十一月 06, 2004	Sheet 41 of 53	



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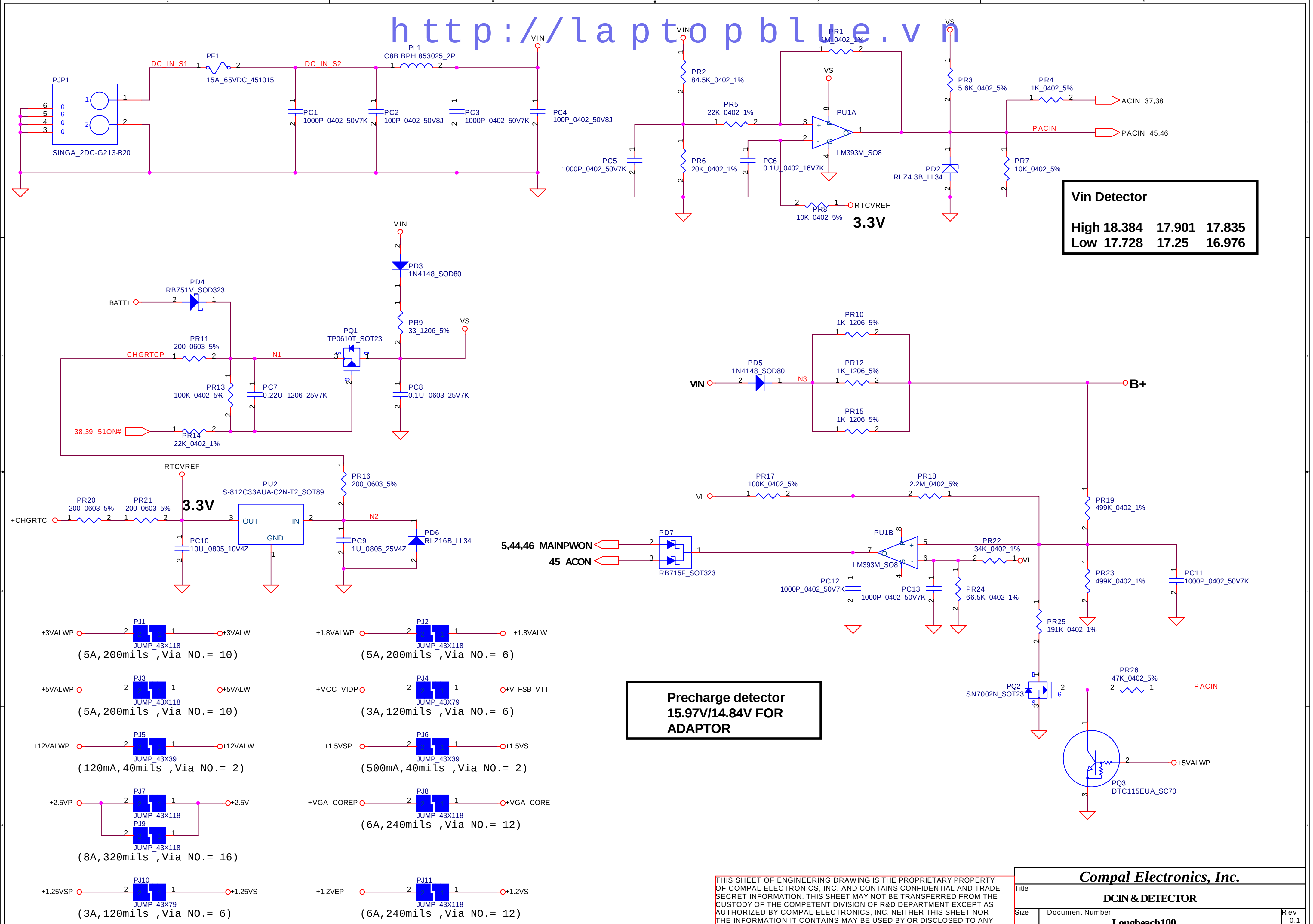
Compal Electronics, Inc.

Title: POWER CONTROL CKT

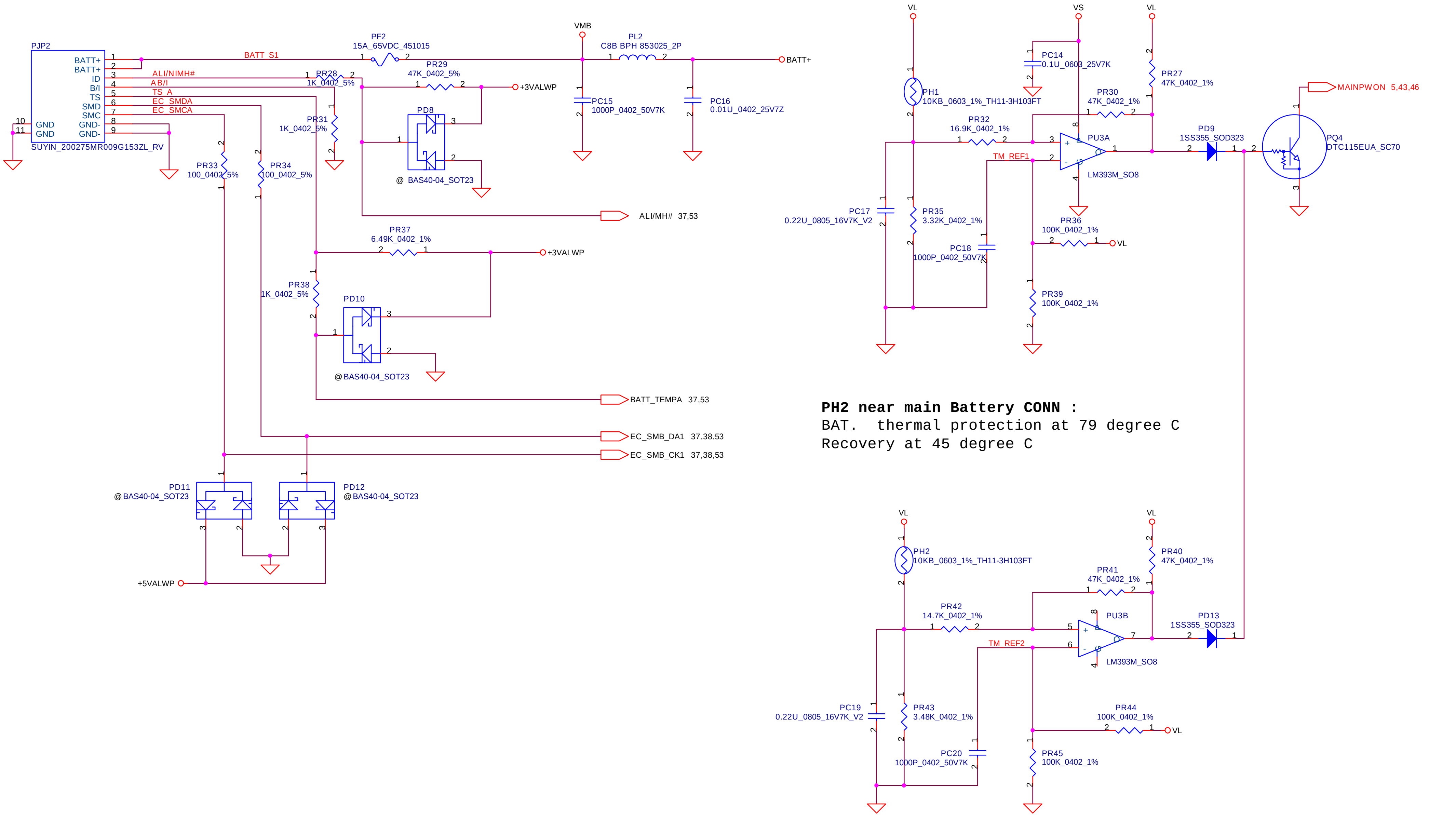
Size: Custom | Document Number: Longbeach 100 <LA-2451> | Rev: 0.1

Date: 星期六, 十一月 06, 2004 | Sheet 42 of 53



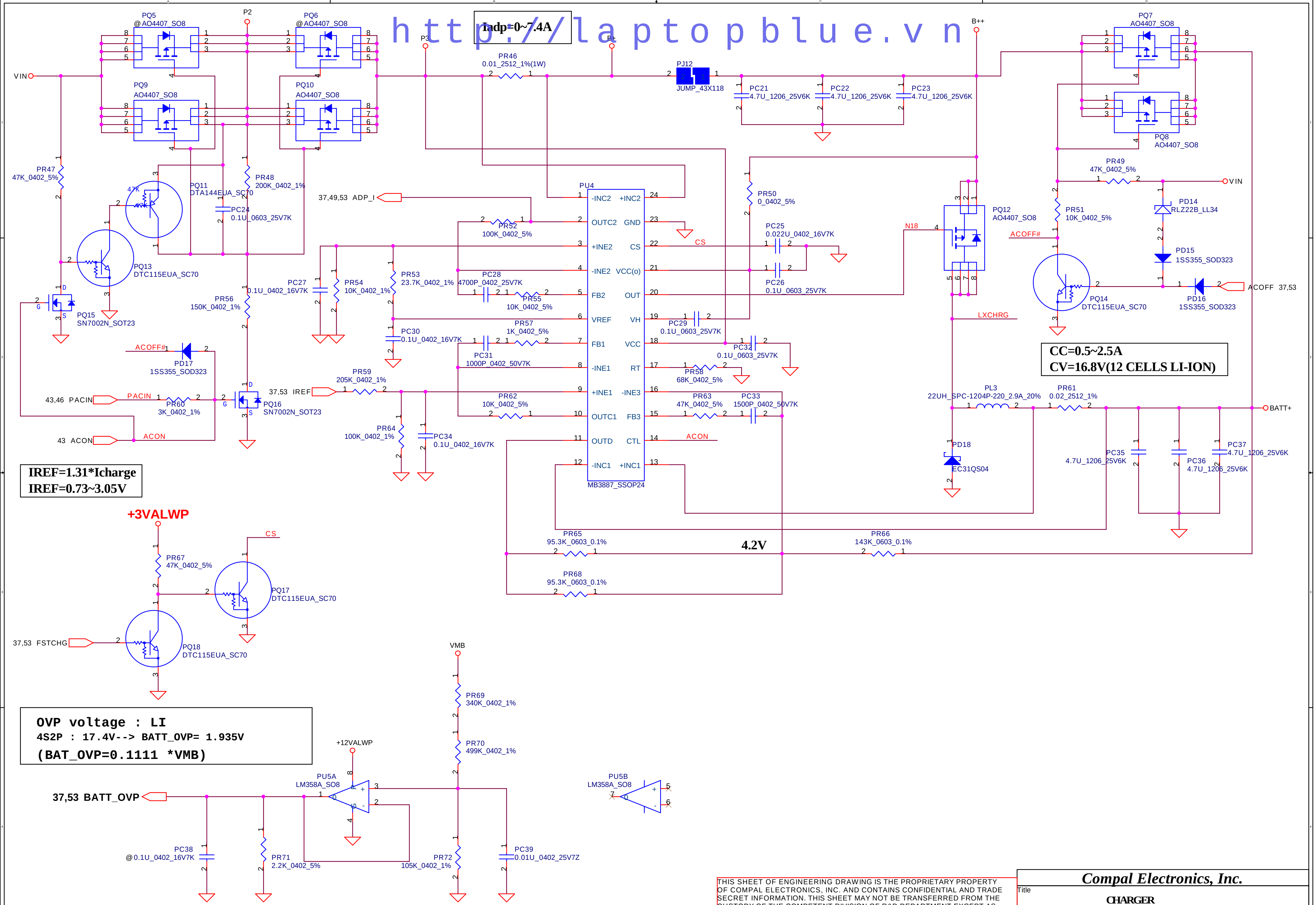
Compal Electronics, Inc.		
Title	DCIN & DETECTOR	
Size	Document Number: Longbeach100	Rev 0.1
Date: ¬P期六, 十一月 06, 2004	Sheet 43 of 53	

PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C

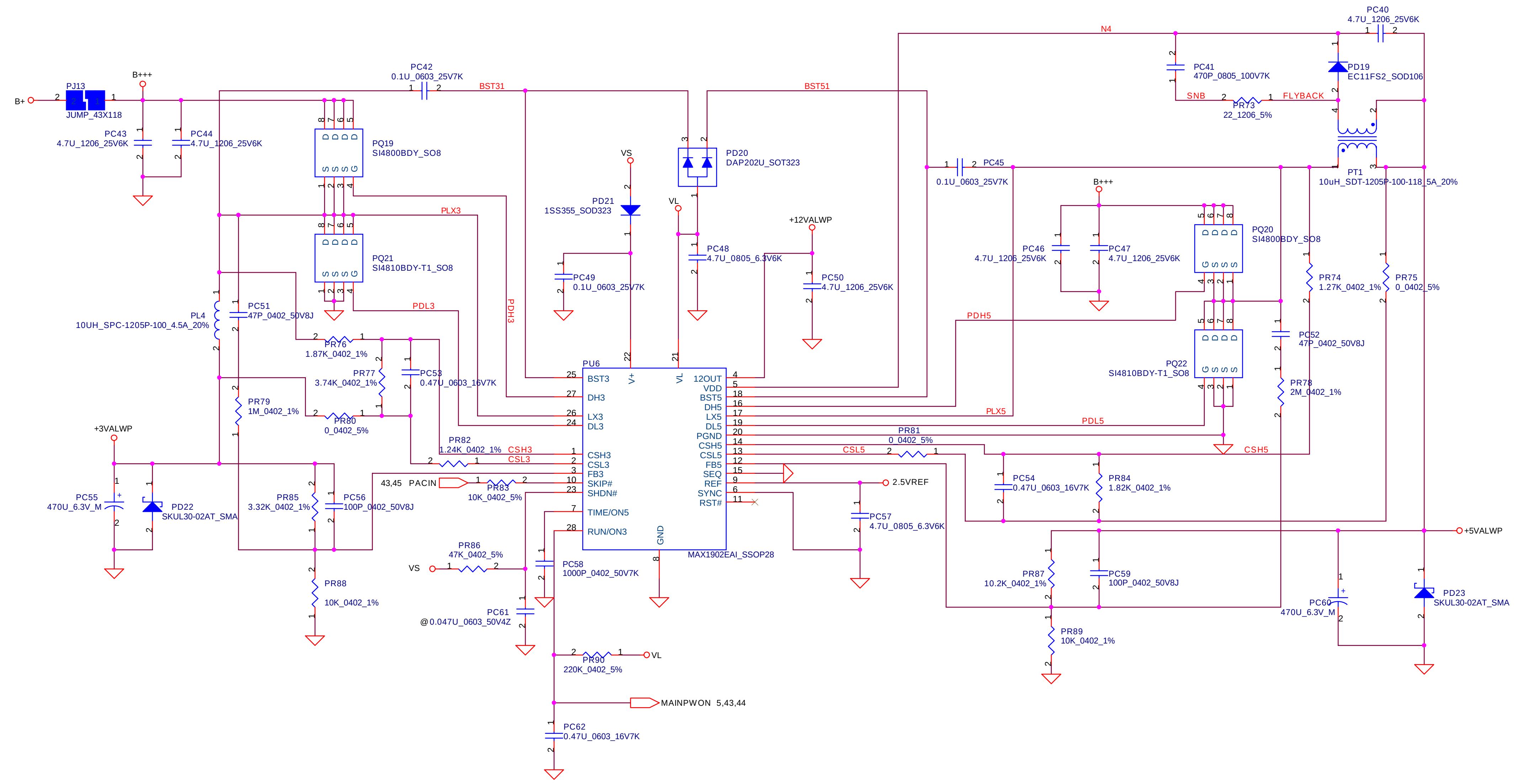


PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C

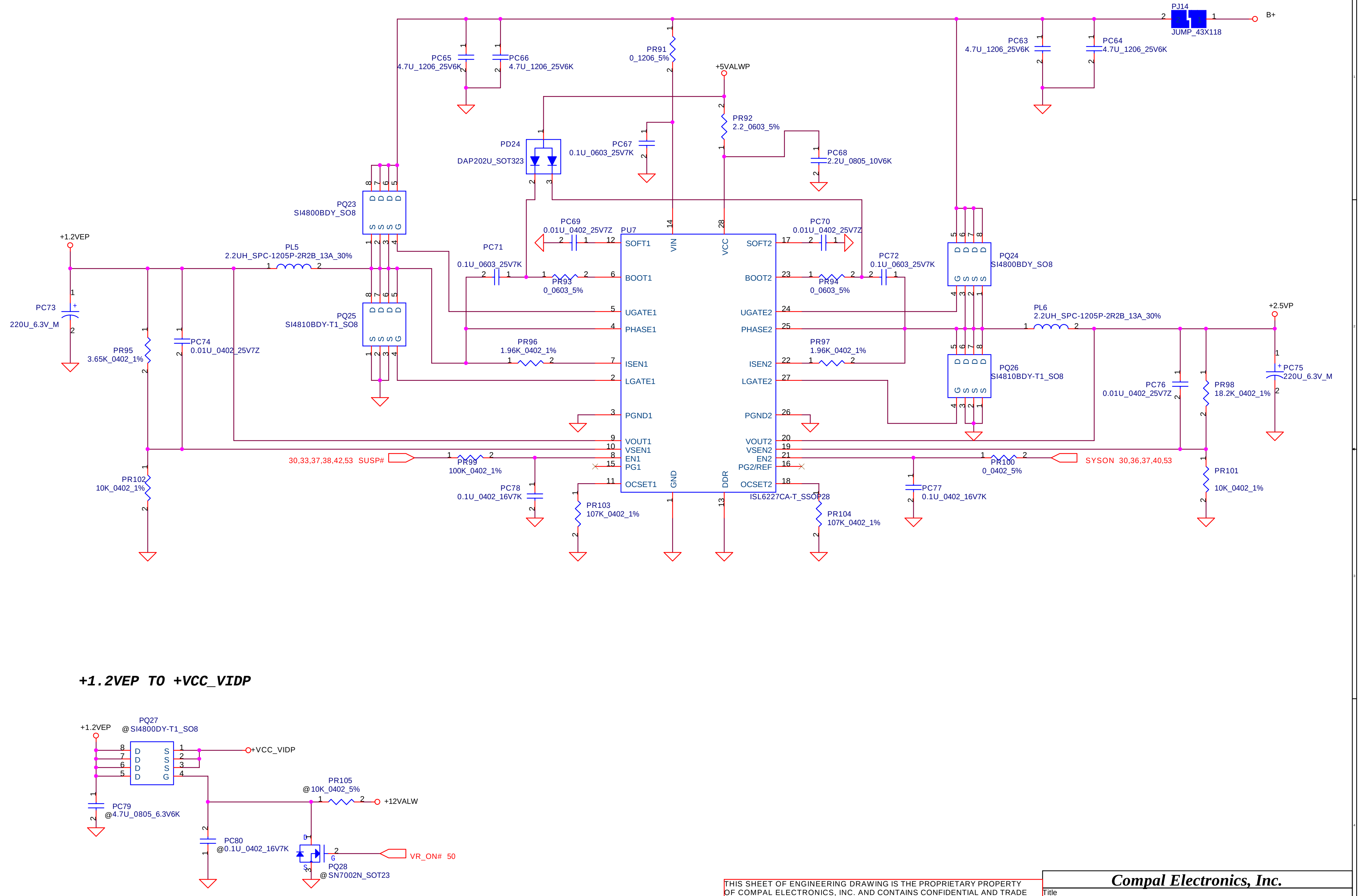
Compal Electronics, Inc.	
Title	BATTERY CONN / OTP
Size	Document Number: Longbeach100 — Rev 0.1
Date: ¬P期六, 十一月 06, 2004	Sheet 44 of 53



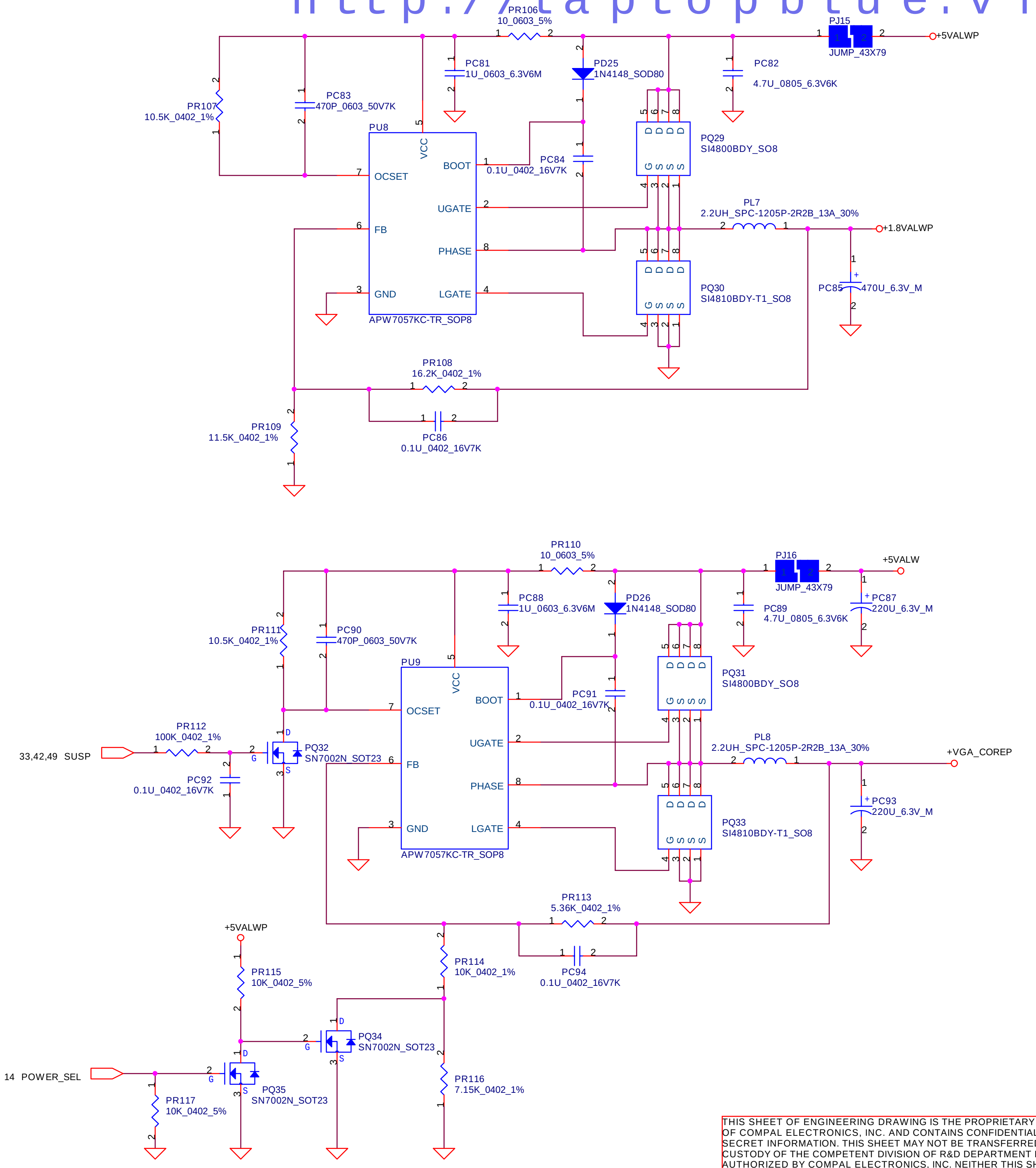
Compal Electronics, Inc.		
Title	CHARGER	
Size	Document Number: Longbeach100	Rev 0.1
Date: ¬P期六, 十一月 06, 2004	Sheet 45 of 53	



Compal Electronics, Inc.		
Title: 3V/5V/12V		
Size	Document Number: Longbeach100	Rev 0.1
Date: ¬P朋六, 十一月 06, 2004	Sheet 46 of 53	



Compal Electronics, Inc.			
Title	DDR_2.5V/1.2VEP		
Size	Document Number: Longbeach100		Rev 0.1
Date: ¬P期六, 十一月 06, 2004	Sheet 47	of 53	



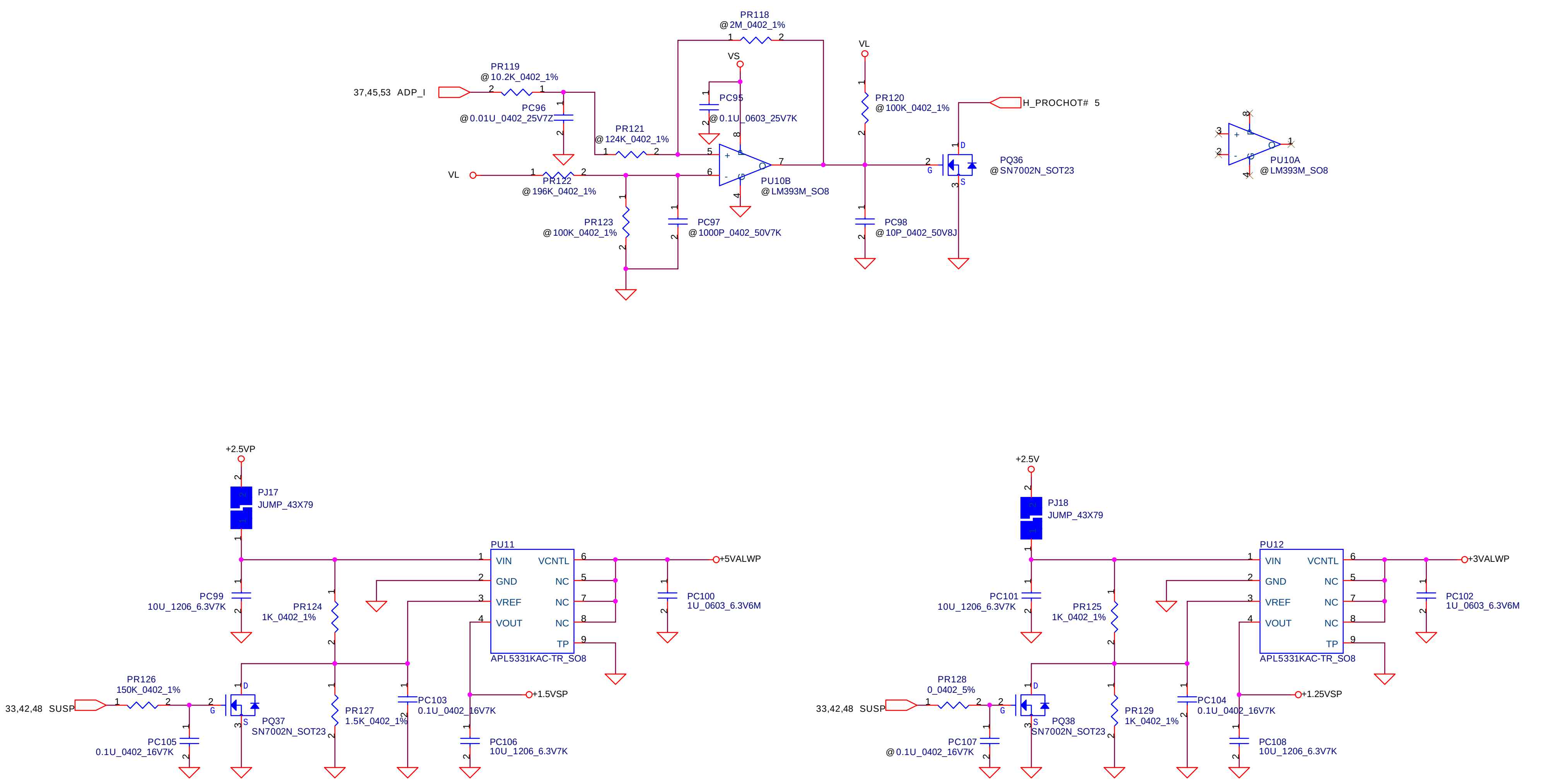
	M24/1.2V	M22/1.15V
PR113	5.36K	3.92K
PR114	10K	8.87K
PR116	7.15K	6.81K

Compal Electronics, Inc.

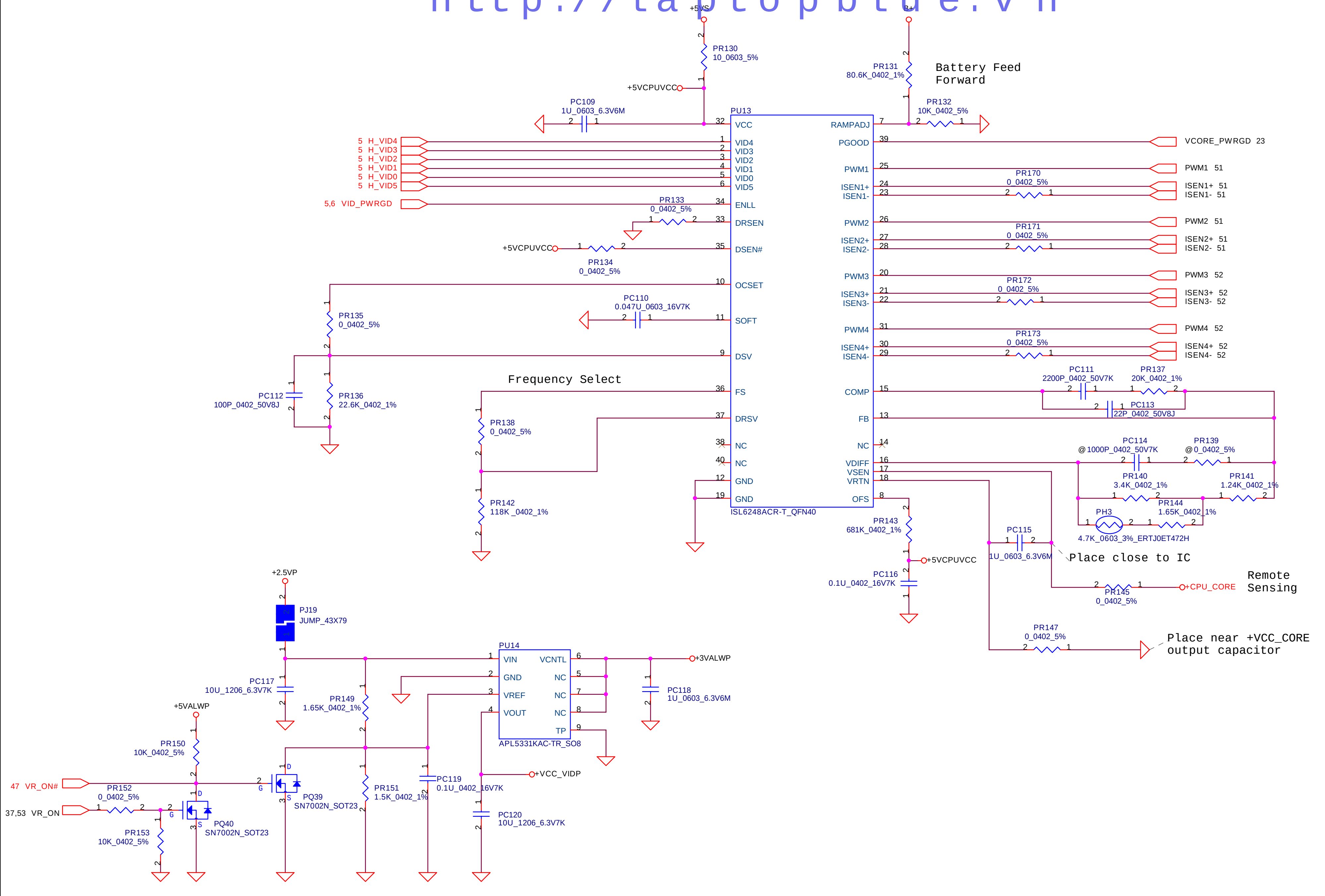
Title: 1.8V/VGA

Size | Document Number: Longbeach100 | Rev 0.1

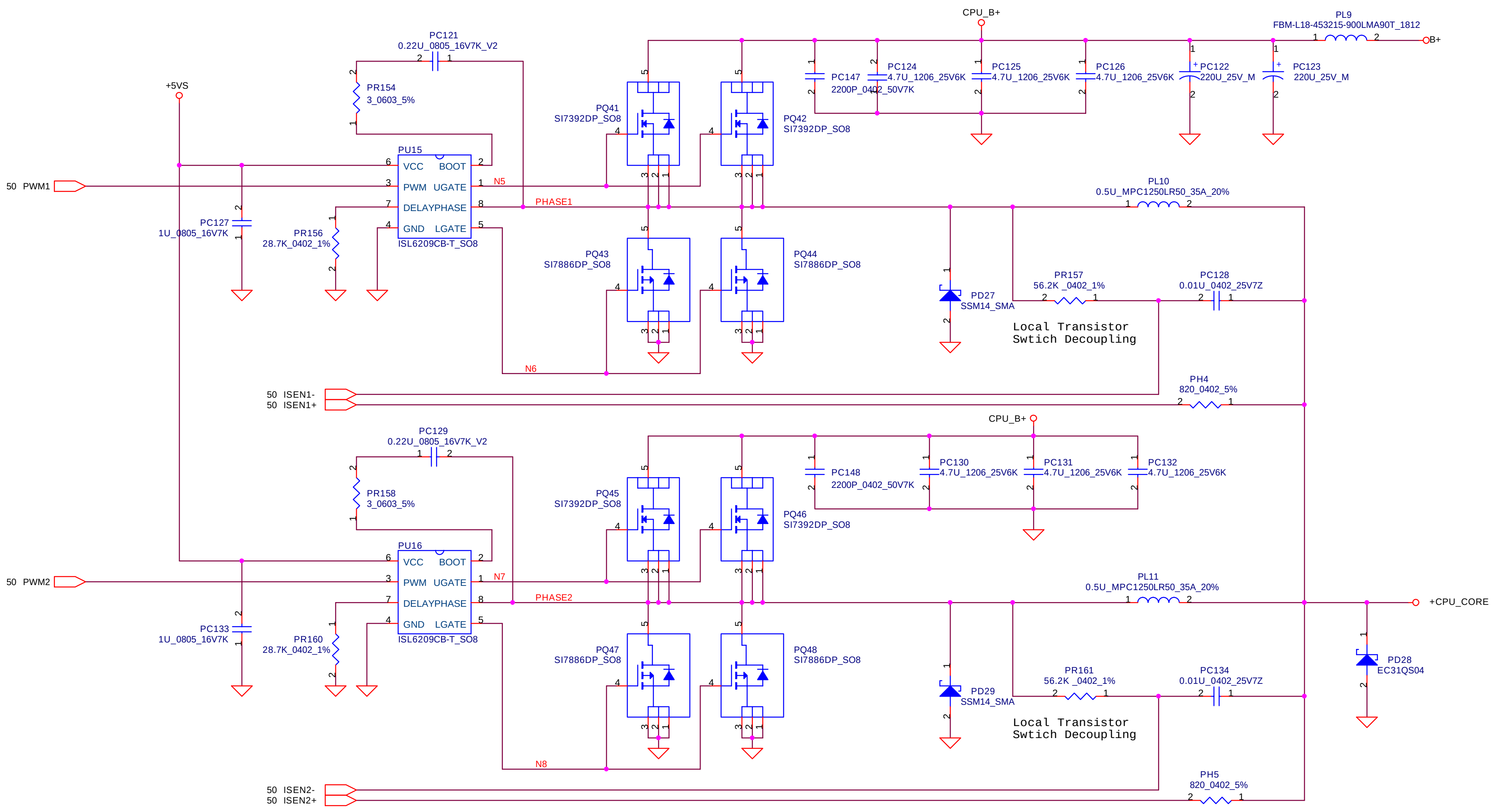
Date: ¬P期六, 十一月 06, 2004 |



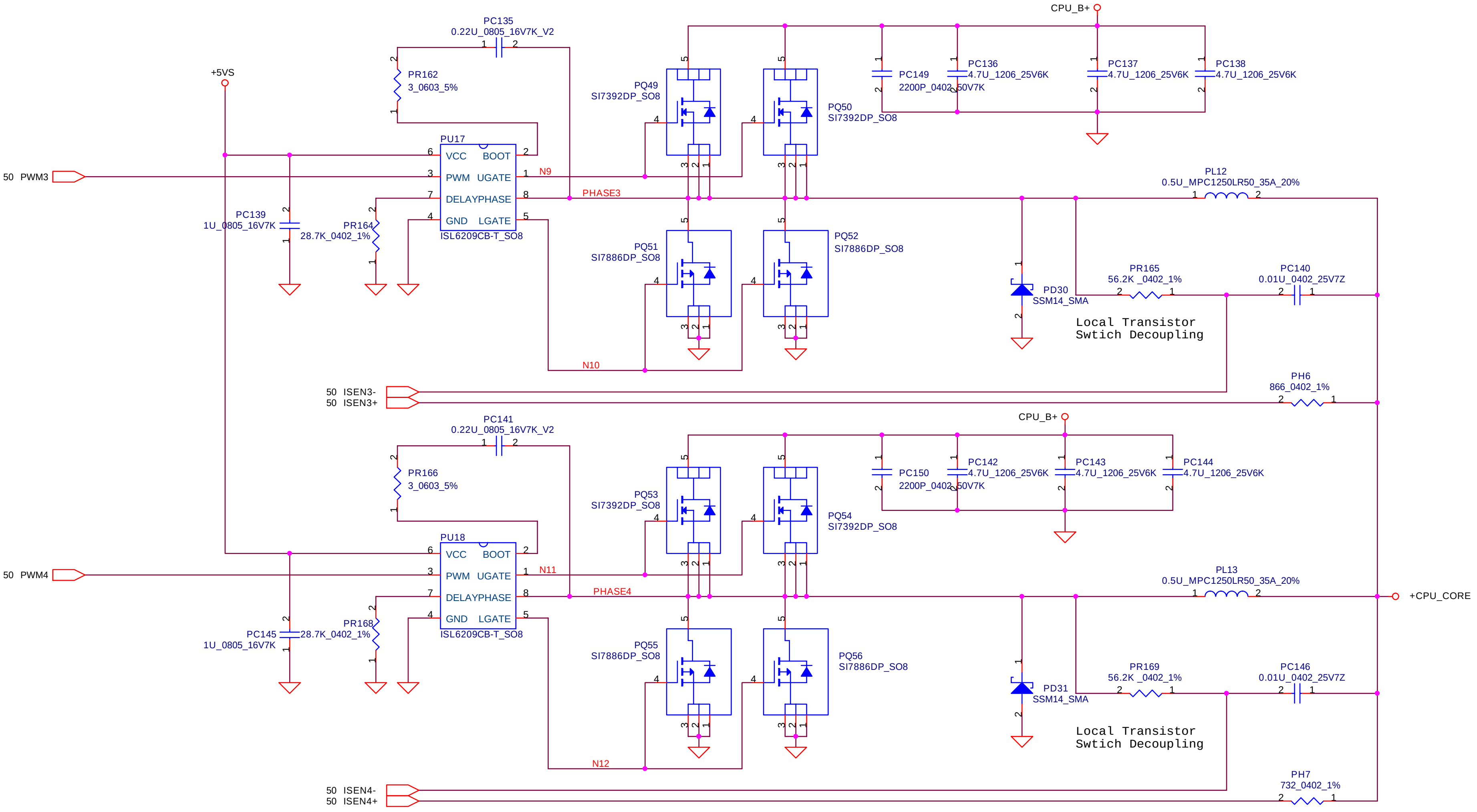
Compal Electronics, Inc.	
Title	1.5V/1.25V/PROCHOT
Size / Document Number	Longbeach100
Rev	0.1
Date:	¬P期六, 十一月 06, 2004
Sheet	49 of 53



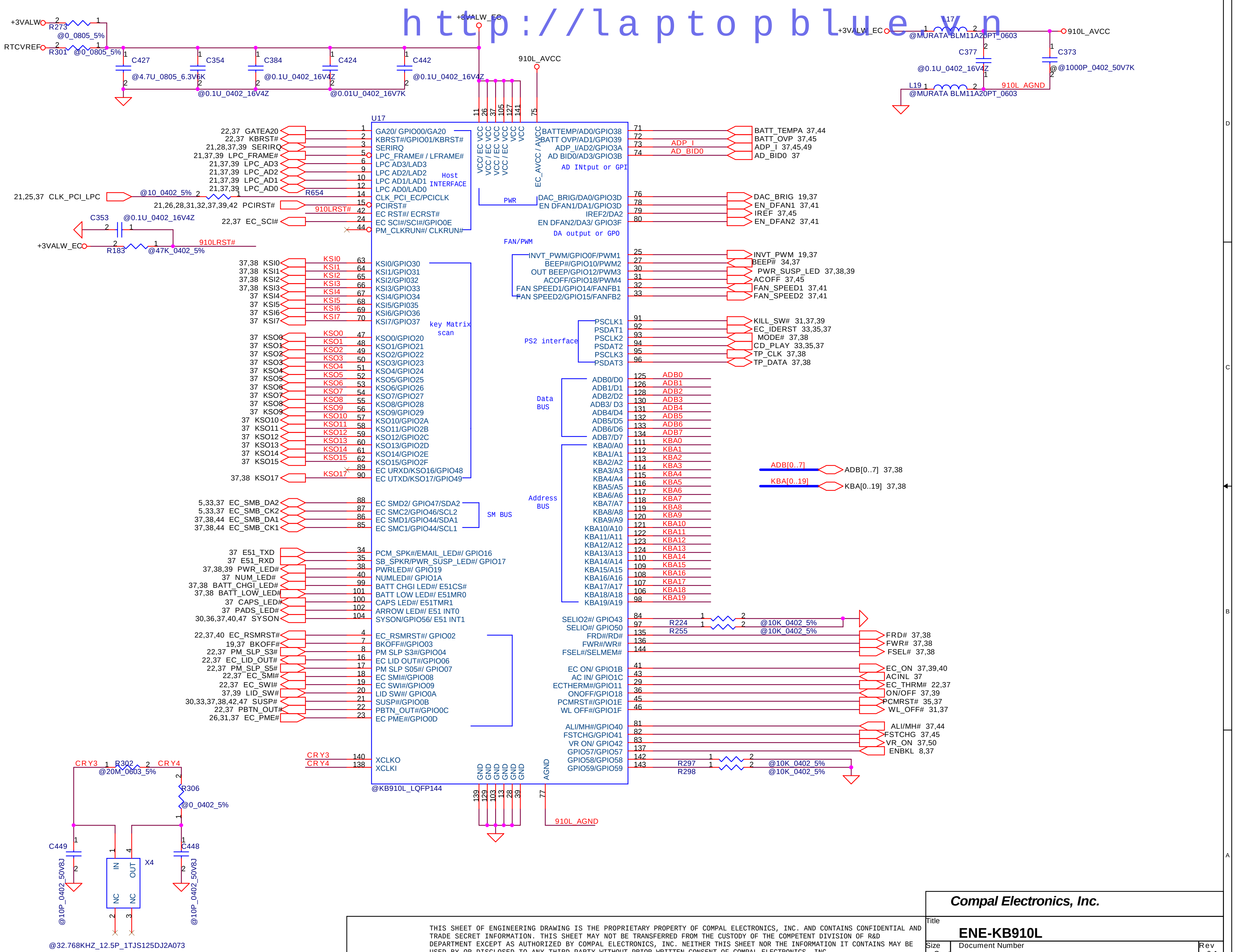
Compal Electronics, Inc.			
Title	CPU_CORE (1)		
Size	Document Number: Longbeach100		Rev 0.1
Date: ¬P期六, 十一月 06, 2004	Sheet 50 of 53		



Compal Electronics, Inc.		
Title: CPU_CORE (1)		
Size	Document Number: Longbeach100	Rev: 0.1
Date: ¬P期六, 十一月 06, 2004	Sheet 51 of 53	



Compal Electronics, Inc.		
Title: CPU_CORE (2)		
Size	Document Number: Longbeach100	Rev 0.1
Date: ¬P期六, 十一月 06, 2004	Sheet 52 of 53	



Compal Electronics, Inc.

Title	ENE-KB910L	
Size: Custom	Document Number: Longbeach 100 <LA-2451>	Rev: 0.1
Date: 星期六, 十一月 06, 2004	Sheet 53 of 53	