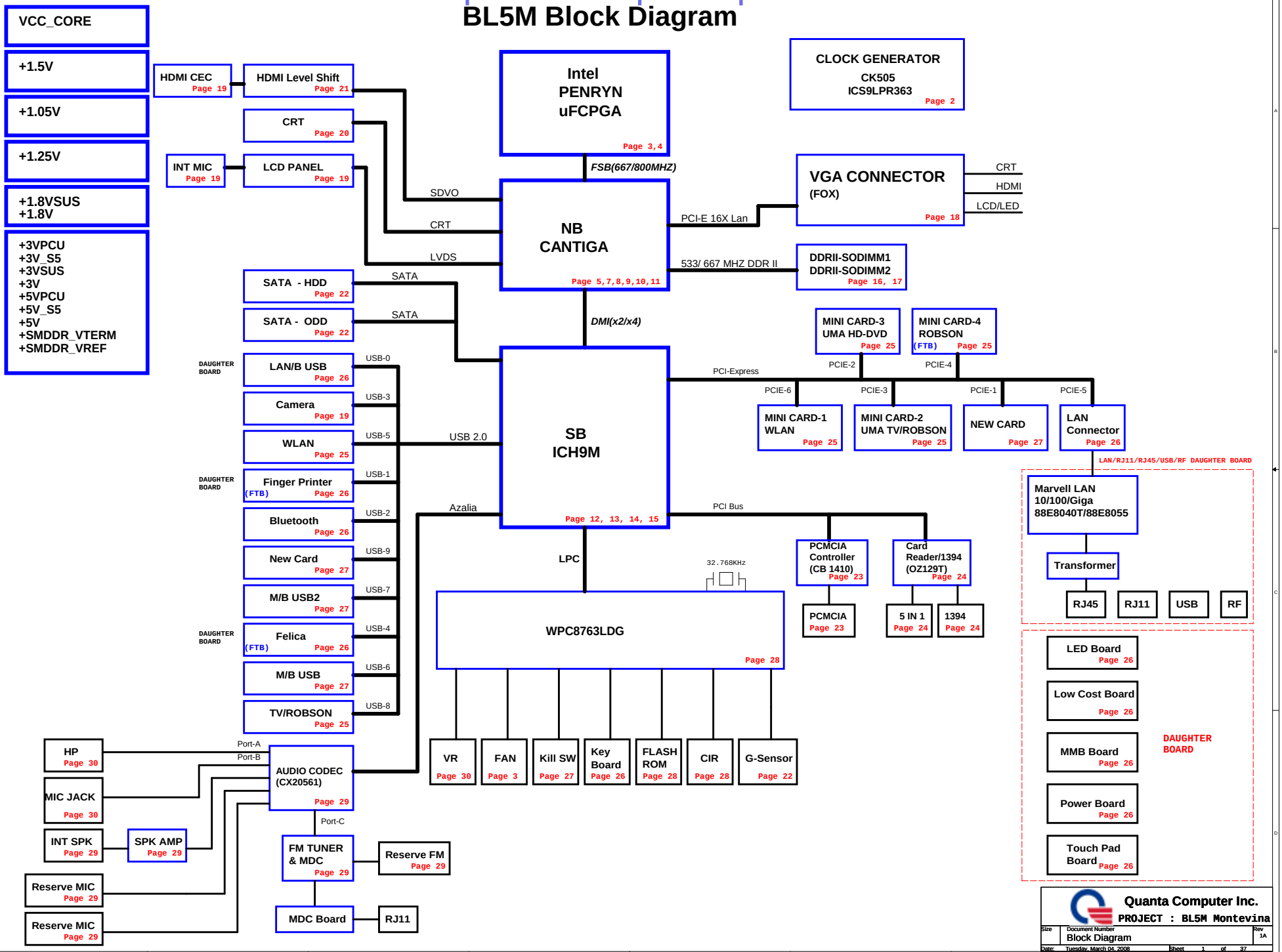
BL5M Block Diagram



Clock Generator

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA

11/01 Modify

CK505 — ICS9LPRS365BGLFT

<MAIN>:ICS9LPRS365BGLFT QCI:ALPRS365K13
<SECOND>:SLG8SP512TTR: QCI:AL8SP512K05

10/30 Change Value and need change PN

	ICS9LPRS365 (ALPRS365K13)	RTM875T-606 (AL000875K06)	PULL HIGH	PULL DOWN
Pin 4	PCI2/TME	PCI2/TME internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 5	PCI-3	PCI-3/SRC5_EN internal PD	PIN37/38 IS SRC5	PIN37/38 IS PCI_STOP/CPU_STOP (default)
Pin 6	PCI-4/27M_SEL	PCI-4/27M_SEL internal PD	PIN 17/18 IS 27MHz	PIN 17/18 IS SRC/DOT (default)
Pin 7	PCIF-5/ITP_EN	PCIF-5/ITP_EN internal PD	PIN 46/47 IS CPUITP	PIN 46/47 IS SRC8 (default)

To SB
To CPU
To NB
To MINI3
To NB
To New Card
To MINI2
To WLAN
To LAN
To SB
To SB
To NB
To NB
To VGA Card

FREQ. SEL TABLE

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Clock Gen I2C

11/01 Del C3195

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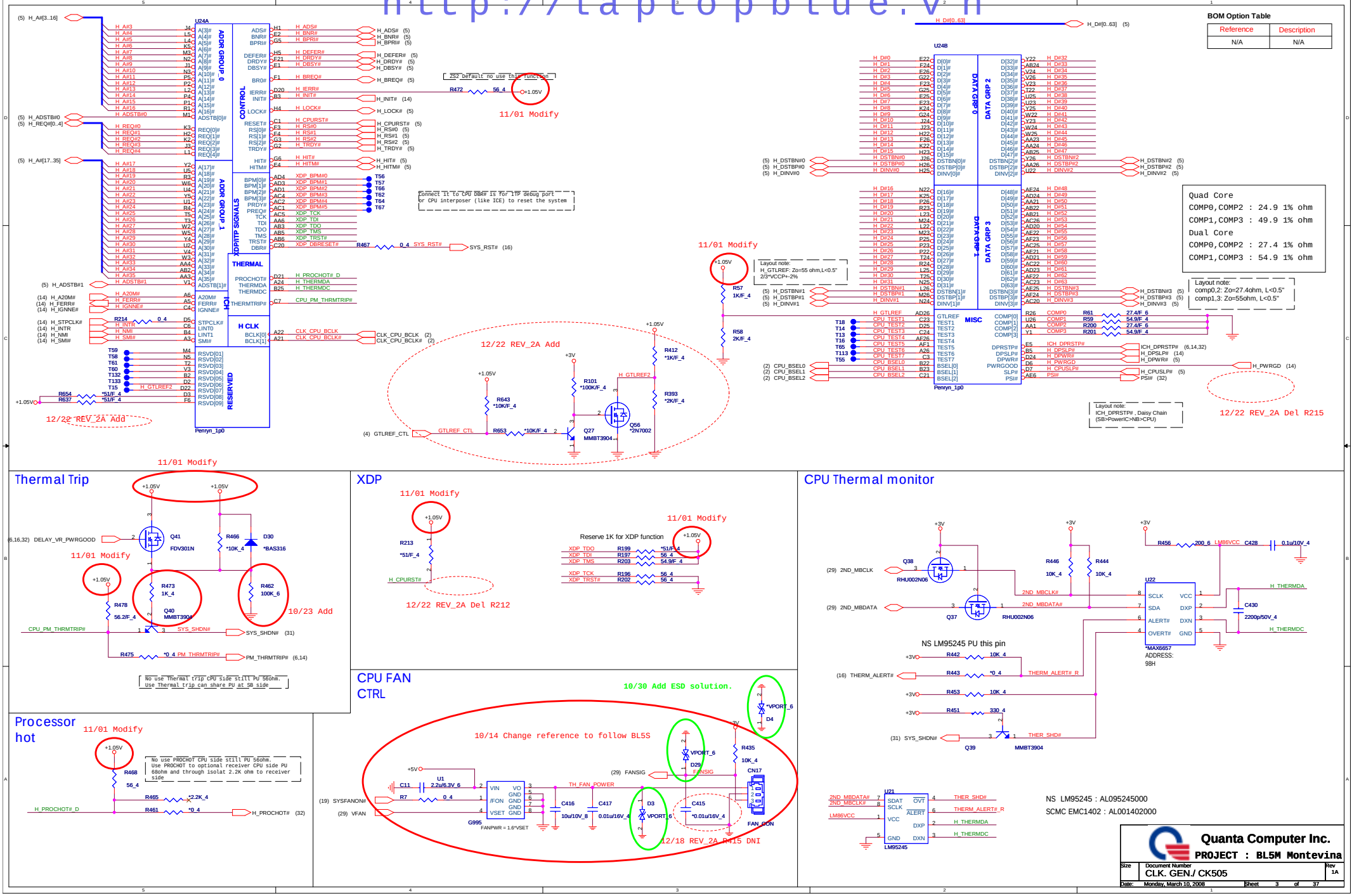
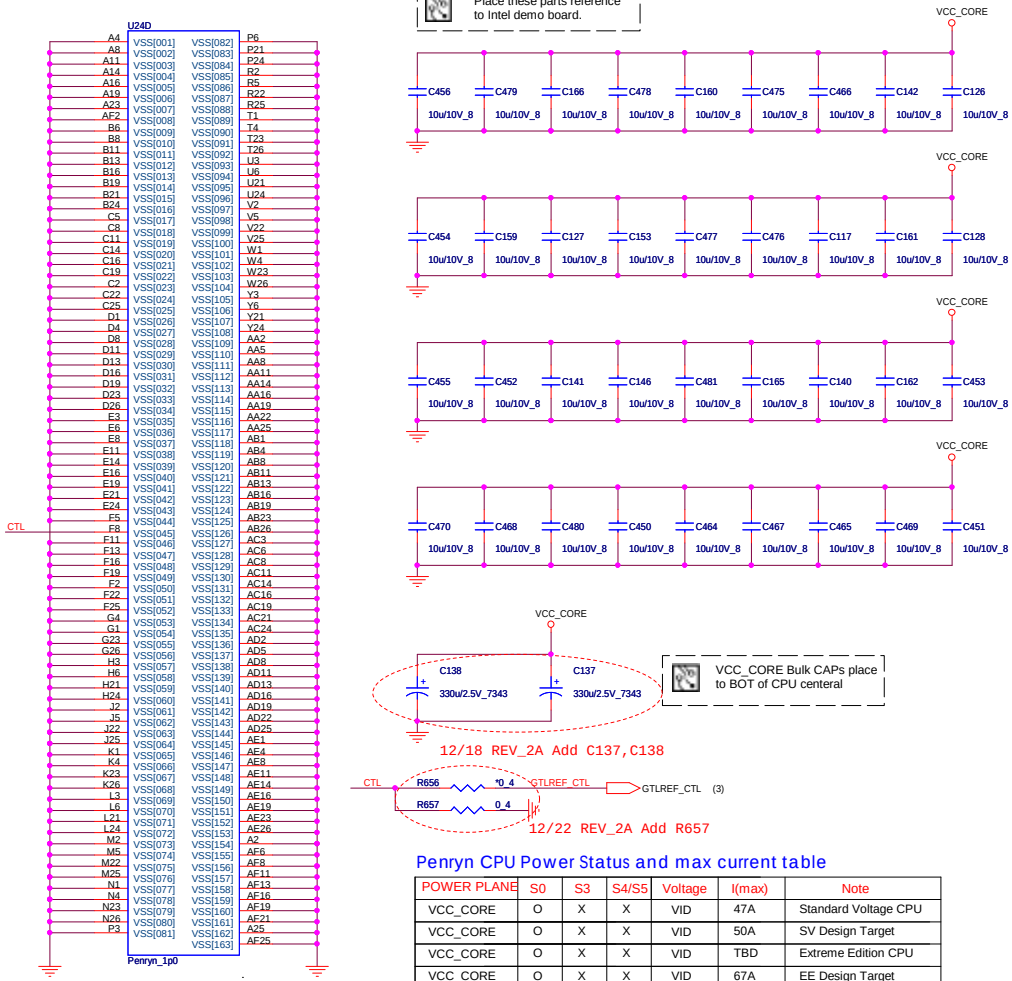


BOM Option Table

Reference	Description
N/A	N/A

Need NC 20PCS 10u before A1 BOM released(A0 all stuff)

Place these parts reference to Intel demo board.



VCC_CORE Bulk CAPs place to BOT of CPU centeral

12/18 REV_2A Add C137,C138

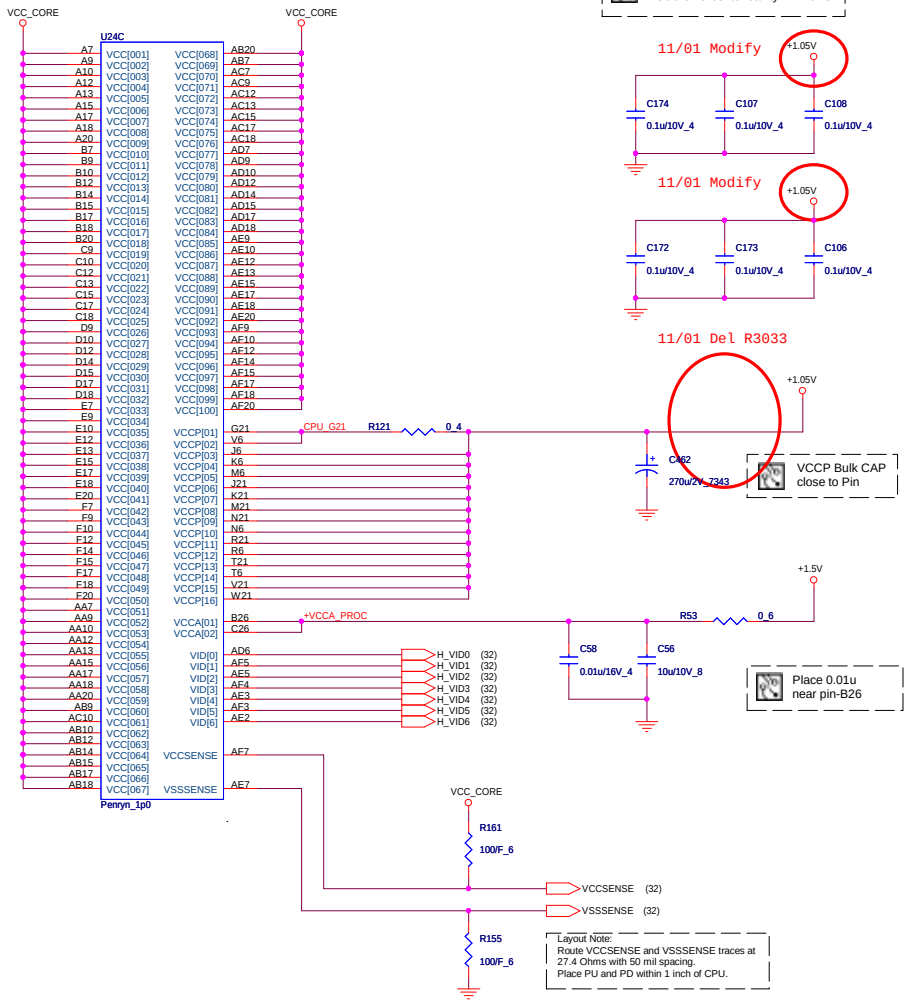
12/22 REV_2A Add R657

Penryn CPU Power Status and max current table

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC_CORE	O	X	X	VID	47A	Standard Voltage CPU
VCC_CORE	O	X	X	VID	50A	SV Design Target
VCC_CORE	O	X	X	VID	TBD	Extreme Edition CPU
VCC_CORE	O	X	X	VID	67A	EE Design Target
VCCA	O	X	X	+1.5V	130mA	
VCCP	O	X	X	+1.05V	4.5A	Before VCC Stable
VCCP	O	X	X	+1.05V	2.5A	After VCC Stable

(See Penryn EMTS Rev:1.0 Table7,8 for voltage and current)

(See Penryn EMTS Rev:1.0 Table-3 for VID table)



Layout Note:
Inside CPU center cavity in 2 rows

11/01 Modify

11/01 Modify

11/01 Del R3033

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.

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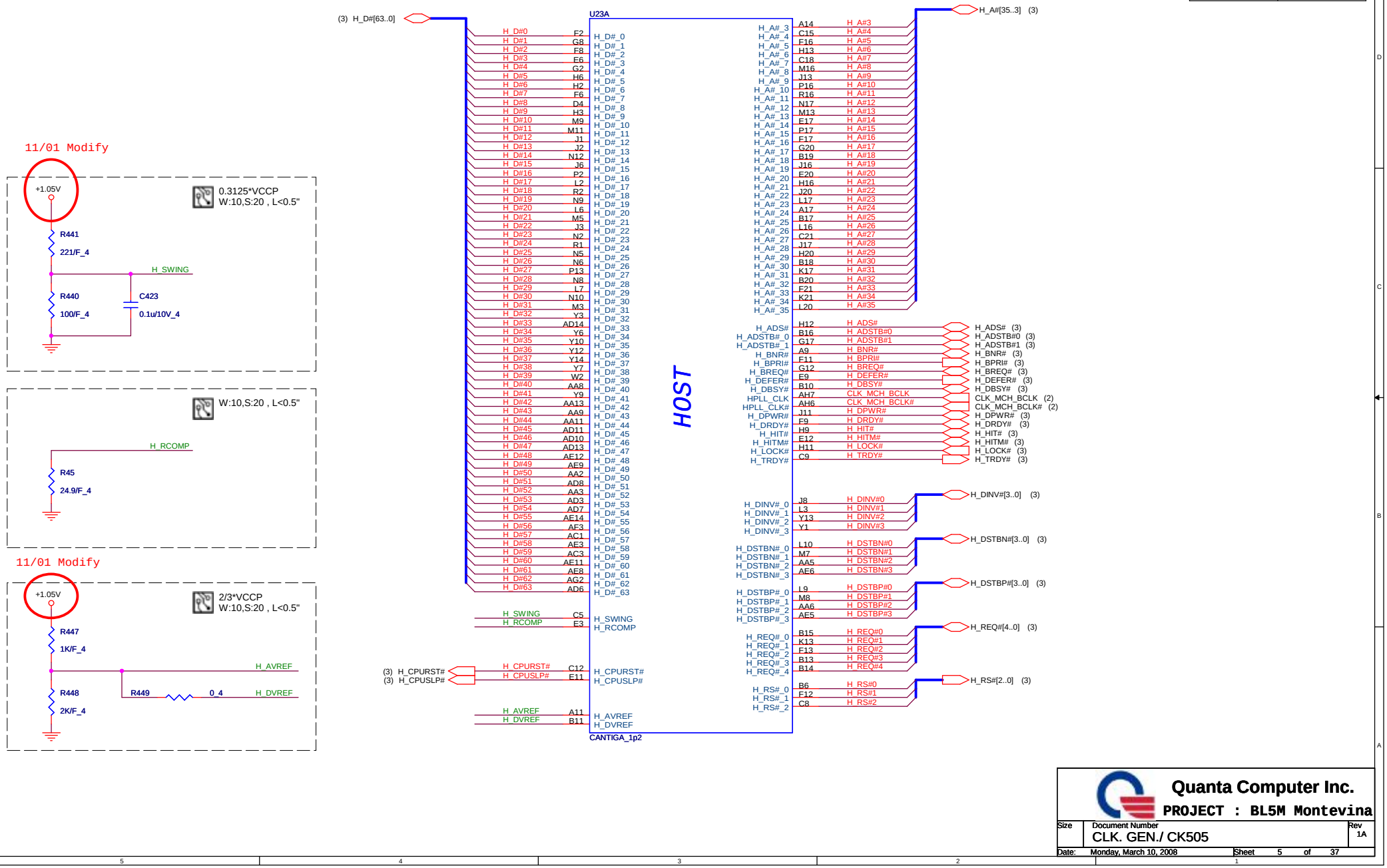
BOM Option Table

Reference	Description
N/A	N/A



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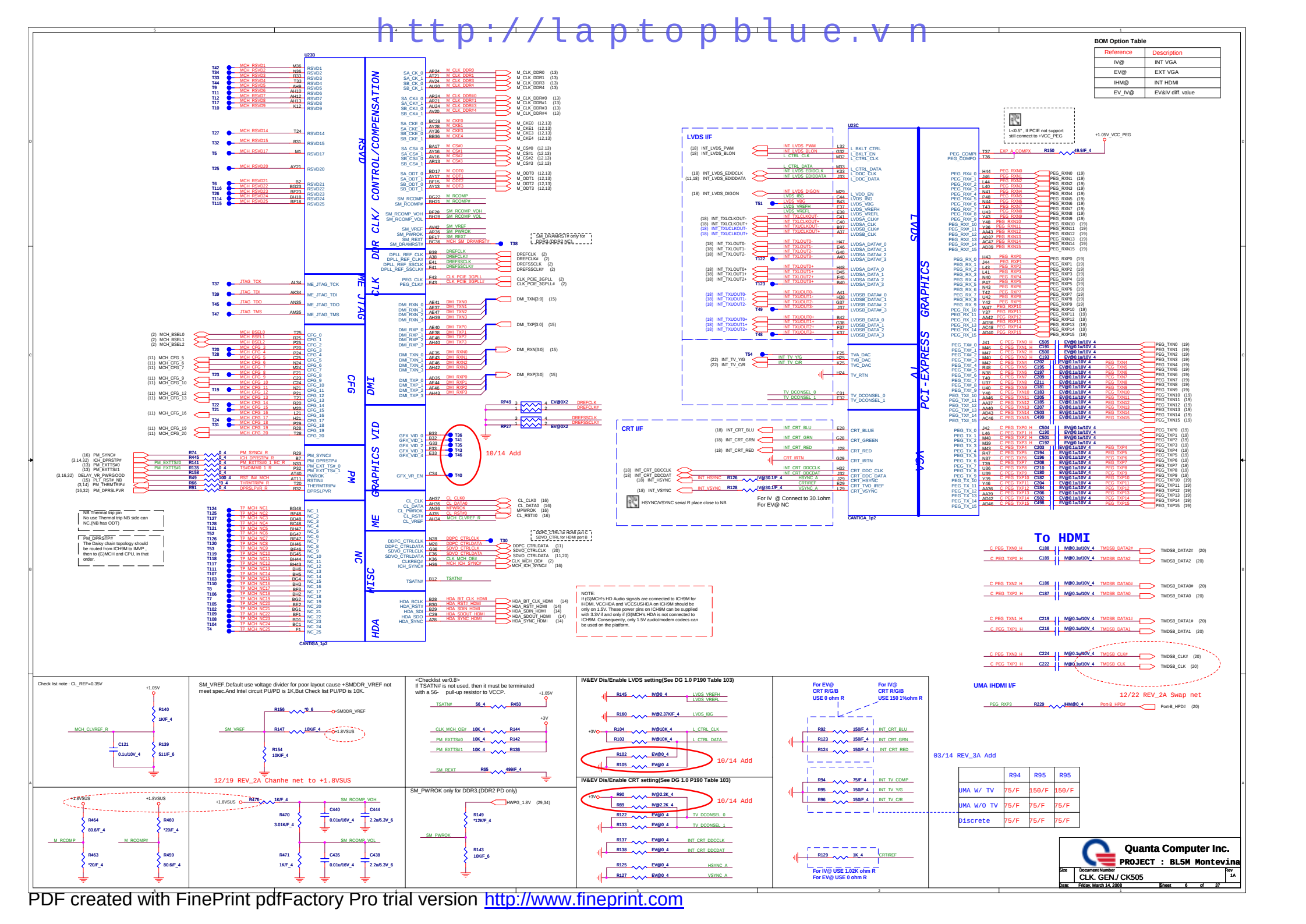
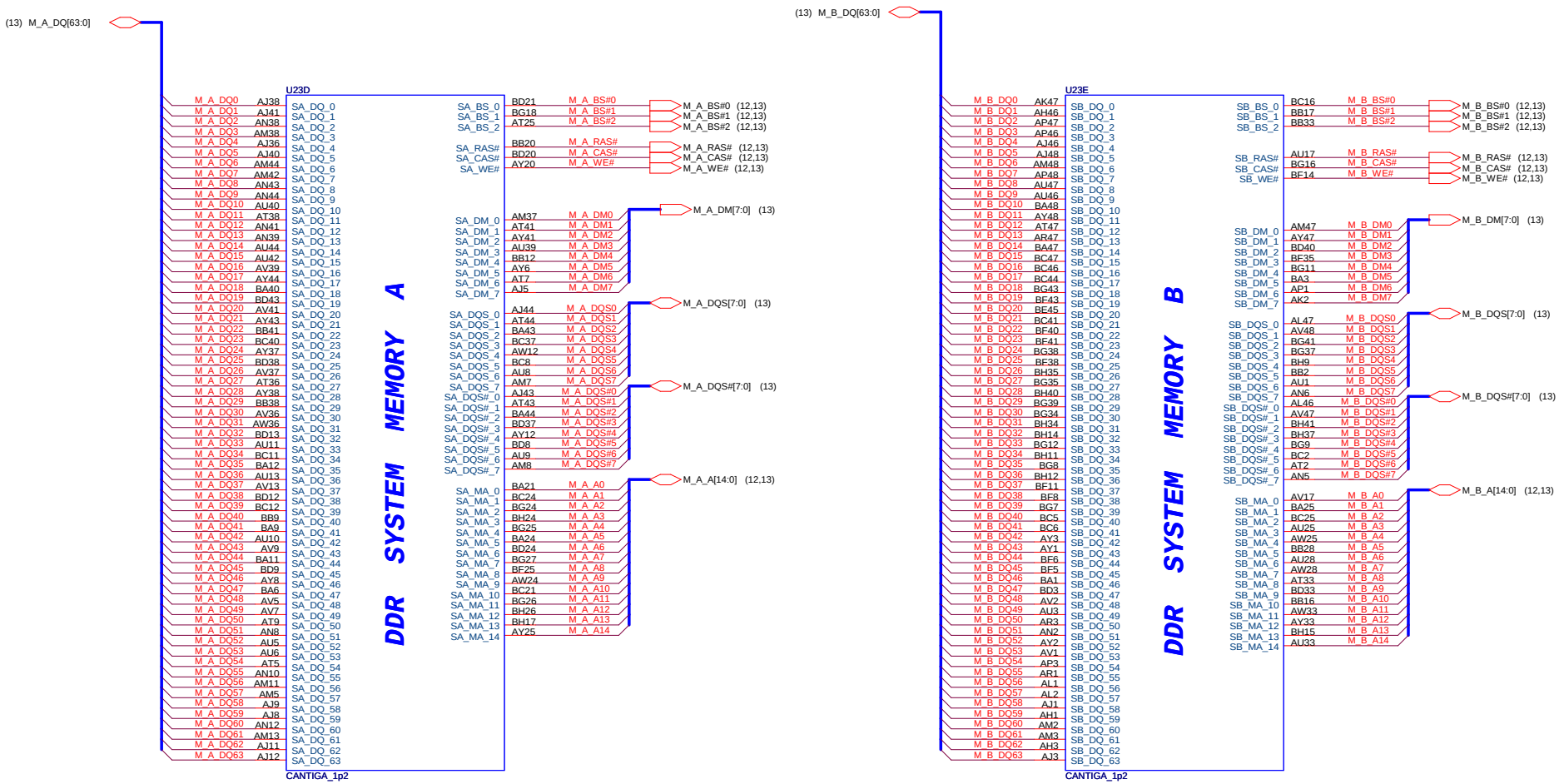


BOM Option Table

Reference	Description
N/A	N/A



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PROJECT : BL5M Montevina

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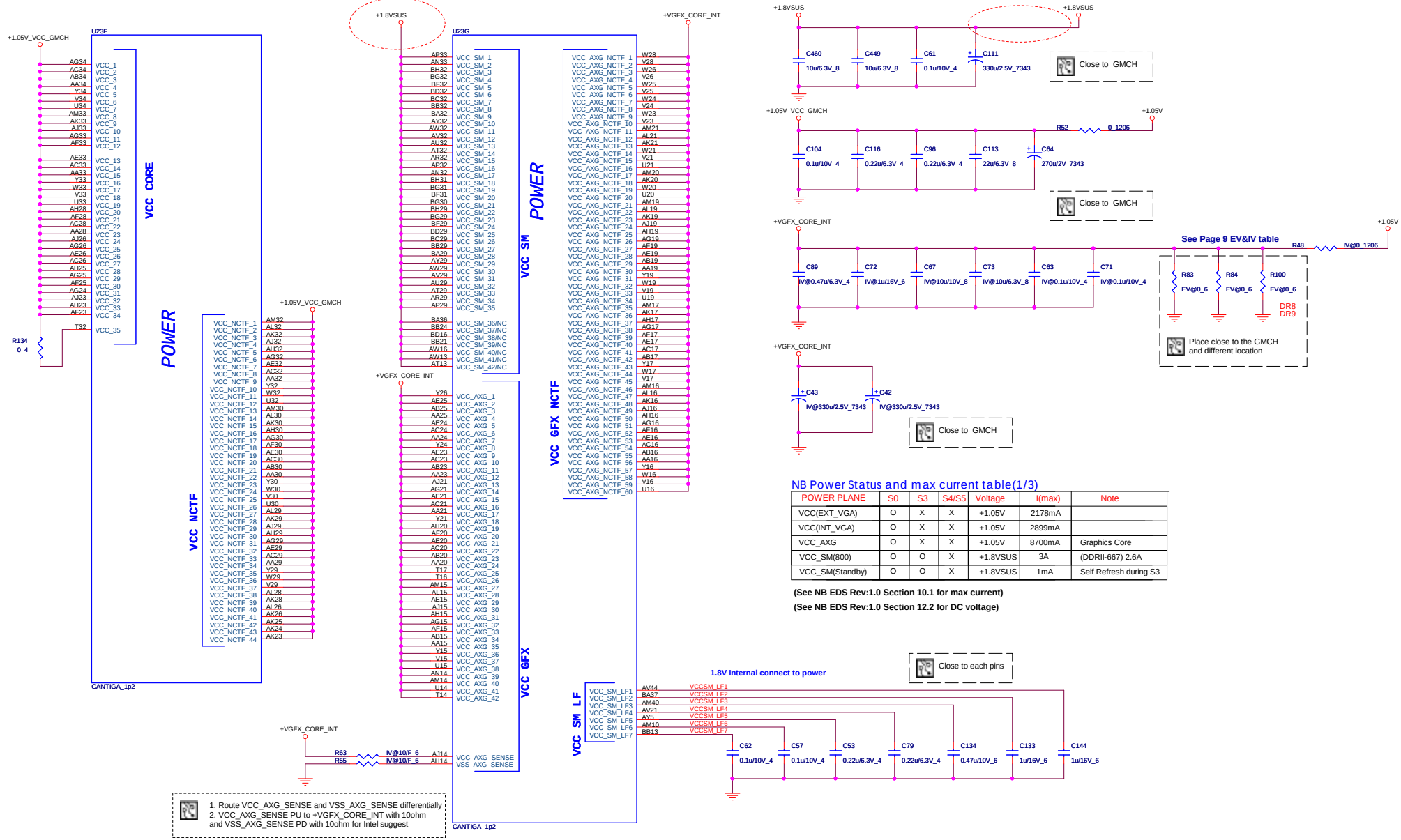
BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA

12/19 REV_2A Chanhe net to +1.8VSUS

12/19 REV_2A Del R101



NB Power Status and max current table(1/3)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AXG	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(800)	O	O	X	+1.8VSUS	3A	(DDRII-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

(See NB EDS Rev:1.0 Section 10.1 for max current)

(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

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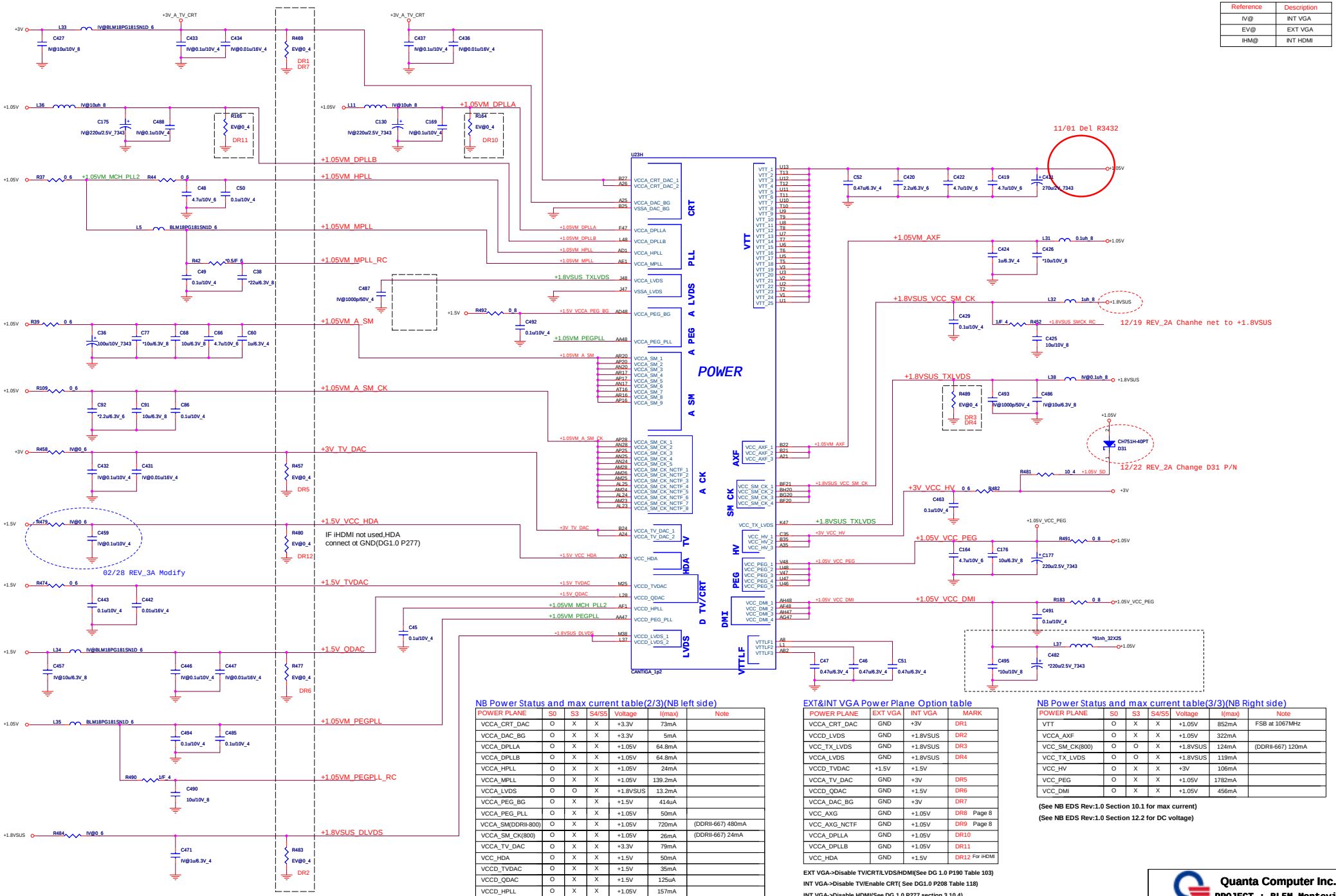

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT HDMI

NB Power Status and max current table(2/3)(NB left side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCCA_CRT_DAC	O	X	X	+3.3V	73mA	
VCCA_DAC_BG	O	X	X	+3.3V	5mA	
VCCA_DPLLA	O	X	X	+1.05V	64.8mA	
VCCA_DPLLB	O	X	X	+1.05V	64.8mA	
VCCA_HPLL	O	X	X	+1.05V	24mA	
VCCA_MPLL	O	X	X	+1.05V	139.2mA	
VCCA_LVDS	O	O	X	+1.8VSUS	13.2mA	
VCCA_PEG_BG	O	X	X	+1.5V	414uA	
VCCA_PEG_PLL	O	X	X	+1.05V	50mA	
VCCA_SM(DDRII-800)	O	X	X	+1.05V	720mA	(DDRII-667) 480mA
VCCA_SM_CK(800)	O	X	X	+1.05V	26mA	(DDRII-667) 24mA
VCCA_TV_DAC	O	X	X	+3.3V	79mA	
VCC_HDA	O	X	X	+1.5V	50mA	
VCCD_TVDAC	O	X	X	+1.5V	35mA	
VCCD_QDAC	O	X	X	+1.5V	125uA	
VCCD_HPLL	O	X	X	+1.05V	157mA	
VCCD_PEG_PLL	O	X	X	+1.05V	50mA	
VCCD_LVDS	O	O	X	+1.8VSUS	60mA	

EXT&INT VGA Power Plane Option table

POWER PLANE	EXT VGA	INT VGA	MARK
VCCA_CRT_DAC	GND	+3V	DR1
VCCD_LVDS	GND	+1.8VSUS	DR2
VCC_TX_LVDS	GND	+1.8VSUS	DR3
VCCA_LVDS	GND	+1.8VSUS	DR4
VCCD_TVDAC	+1.5V	+1.5V	
VCCA_TV_DAC	GND	+3V	DR5
VCCD_QDAC	GND	+1.5V	DR6
VCCA_DAC_BG	GND	+3V	DR7
VCC_AXG	GND	+1.05V	DR8 Page 8
VCC_AXG_NCTF	GND	+1.05V	DR9 Page 8
VCCA_DPLLA	GND	+1.05V	DR10
VCCA_DPLLB	GND	+1.05V	DR11
VCC_HDA	GND	+1.5V	DR12 For iHDMI

EXT VGA->Disable TV/CRT/LVDS/HDMI(See DG 1.0 P190 Table 103)
INT VGA->Disable TV/Enable CRT(See DG1.0 P208 Table 118)
INT VGA->Disable HDMI(See DG 1.0 P277 section 3.10.4)

NB Power Status and max current table(3/3)(NB Right side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VTT	O	X	X	+1.05V	852mA	FSB at 1067MHz
VCCA_AXF	O	X	X	+1.05V	322mA	
VCC_SM_CK(800)	O	O	X	+1.8VSUS	124mA	(DDRII-667) 120mA
VCC_TX_LVDS	O	O	X	+1.8VSUS	119mA	
VCC_HV	O	X	X	+3V	106mA	
VCC_PEG	O	X	X	+1.05V	1782mA	
VCC_DMI	O	X	X	+1.05V	456mA	

(See NB EDS Rev:1.0 Section 10.1 for max current)
(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

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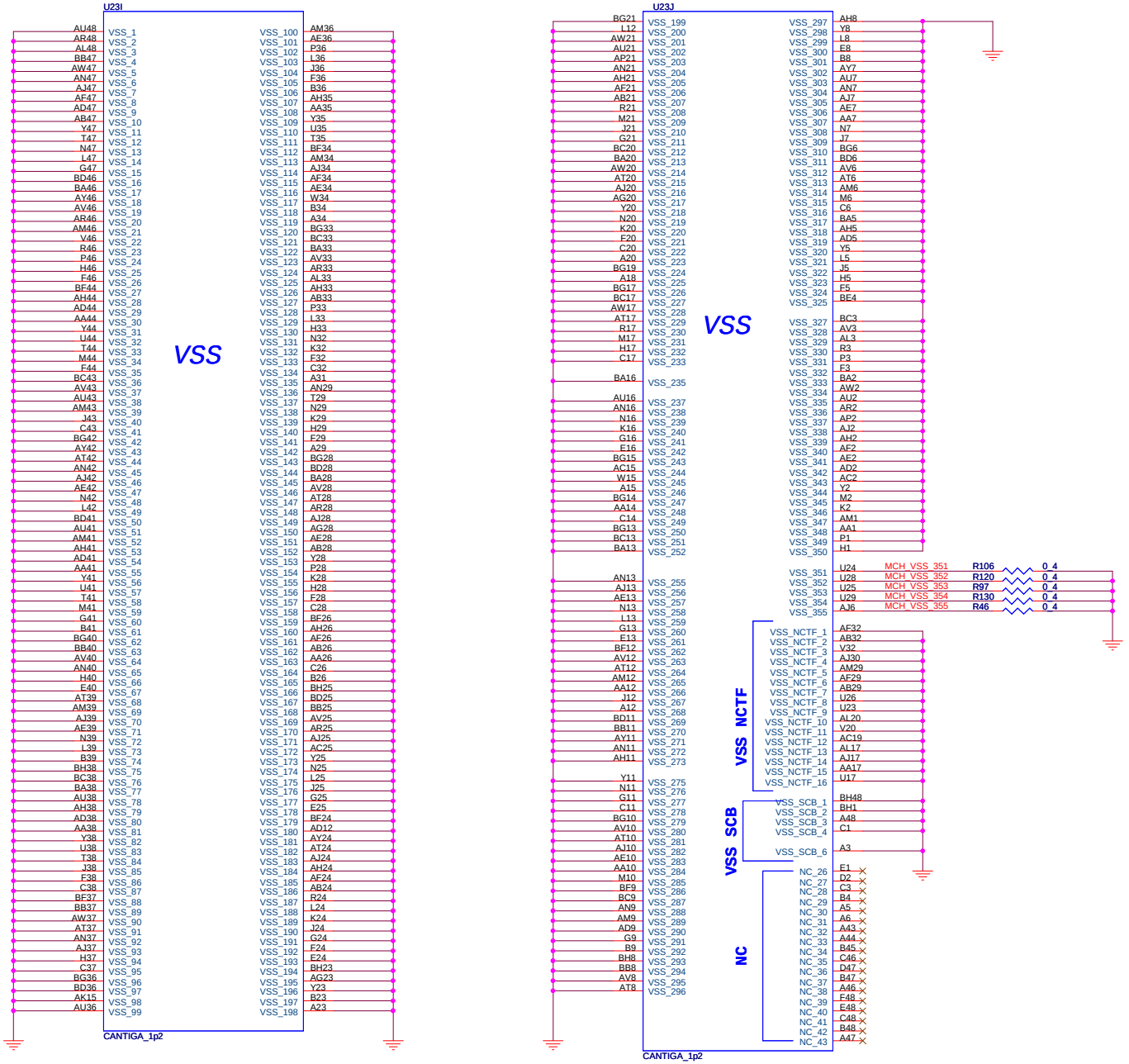
BOM Option Table

Reference	Description
N/A	N/A



Quanta Computer Inc.

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North Bridge Strap Pin Configuration Table

(See DG 1.0 P295 Table 184)
(See NB EDS 1.0 P187 Table 74)

BOM Option Table

Reference	Description
N/A	N/A

Pin Name	Strap description	Configuration	PU<4.02K> PD <2.21K>	Note
CFG[2:0]	FSB Frequency Select	[000]= FSB 1066MHz [010] = FSB 800MHz [011] = FSB 667MHz	See Page 2 FSB selection table	
CFG[4:3]	Reserved			
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)	(6) MCH_CFG_5 — R93 *4.02K/F_4	
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)	(6) MCH_CFG_6 — R99 *10K/F_4	
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)	(6) MCH_CFG_7 — R98 *4.02K/F_4	
CFG8	Reserved			
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)	(6) MCH_CFG_9 — R454 *4.02K/F_4	
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)	(6) MCH_CFG_10 — R455 *4.02K/F_4	
CFG11	Reserved			
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)	(6) MCH_CFG_12 — R76 *4.02K/F_4	
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)	(6) MCH_CFG_13 — R77 *4.02K/F_4	
CFG[15:14]	Reserved			
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)	(6) MCH_CFG_16 — R75 *4.02K/F_4	
CFG[18:17]	Reserved			
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed	(6) MCH_CFG_19 — R72 *4.02K/F_4 — +3V	
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port	(6) MCH_CFG_20 — R73 *4.02K/F_4 — +3V	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI/DP Device Present(Default) 1 = SDVO/HDMI/DP Device present	(6,20) SDVO_CTRLDATA — R146 *2.2K/F_4 — +3V	
L_DDC_DATA	Local Flat Panel(LFP) Present	0 = LFP Disable(Default) 1 = LFP Card Present;PCIE disable	(6,18) INT_LVDS_EDIDDATA — R166 *2.2K/F_4 — +3V	
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present	(6) DDPC_CTRLDATA — R71 *2.2K/F_4 — +3V	

Enable iTPM Table

PAGE	Net Name	PU & PD	NOTE
11	MCH_CFG_6	PD 10K to GND	NB Strap pin
13	SPI_MOSI	PU 20K to +3V_S5	SB Strap pin
14	CLGPIO5	PU 10K to +3V_S5	SB Strap pin

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DDR2 Dual channel A/B PU

M_A_A[13..0] M_A_A[13..0] (7,13)
M_B_A[13..0] M_B_A[13..0] (7,13)

DDRII A CHANNEL

+SMDDR_VTERM

C83 C131 C90 C168 C125 C150 C85 C94 C135 C156 C84 C157 C87
0.1u/10V_4

DDRII B CHANNEL

+SMDDR_VTERM

C167 C143 C88 C102 C93 C152 C163 C171 C124 C101 C147 C158 C122
0.1u/10V_4

M_A_A3 M_A_A1 RP17 56X2 +SMDDR_VTERM
M_A_A9 M_A_A8 RP22 56X2
M_A_A2 M_A_A4 RP20 56X2
(6,13) M_CKE1 M_A_A6 RP29 56X2
(7,13) M_A_BS#2 M_A_A5 RP25 56X2
M_A_A12 RP30 56X2
(6,13) M_CKE0
M_A_A0 RP15 56X2
(7,13) M_A_BS#1

M_B_A10 RP14 56X2 +SMDDR_VTERM
(7,13) M_B_BS#0
M_B_A3 M_B_A5 RP19 56X2
(7,13) M_B_BS#1 M_B_A0 RP13 56X2
M_B_A7 M_B_A11 RP21 56X2
M_B_A8 M_B_A1 RP24 56X2
M_B_A4 M_B_A2 RP18 56X2
(7,13) M_B_BS#2 M_B_A12 RP26 56X2

(7,13) M_A_A14 R151 56_4
(7,13) M_B_A14 R148 56_4 +SMDDR_VTERM

M_A_A7 M_A_A11 RP23 56X2 +SMDDR_VTERM
M_B_A9 RP31 56X2
(6,13) M_CKE3
(6,13) M_ODT1 (6,13) M_CS#1 RP6 56X2
RP7 56X2
(6,13) M_ODT3 (6,13) M_CS#3
(7,13) M_A_BS#0 M_A_A10 RP16 56X2
(7,13) M_A_WE# (7,13) M_A_CAS# RP12 56X2
(6,13) M_CS#0 (7,13) M_A_RAS# RP11 56X2
(7,13) M_B_WE# (7,13) M_B_CAS# RP10 56X2
(6,13) M_CKE4 M_B_A6 RP28 56X2
(6,13) M_ODT2 (7,13) M_B_RAS# RP9 56X2
M_A_A13 RP5 56X2
(6,13) M_ODT0
(6,13) M_CS#2 M_B_A13 RP8 56X2

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	DDR RES. ARRAY	1A

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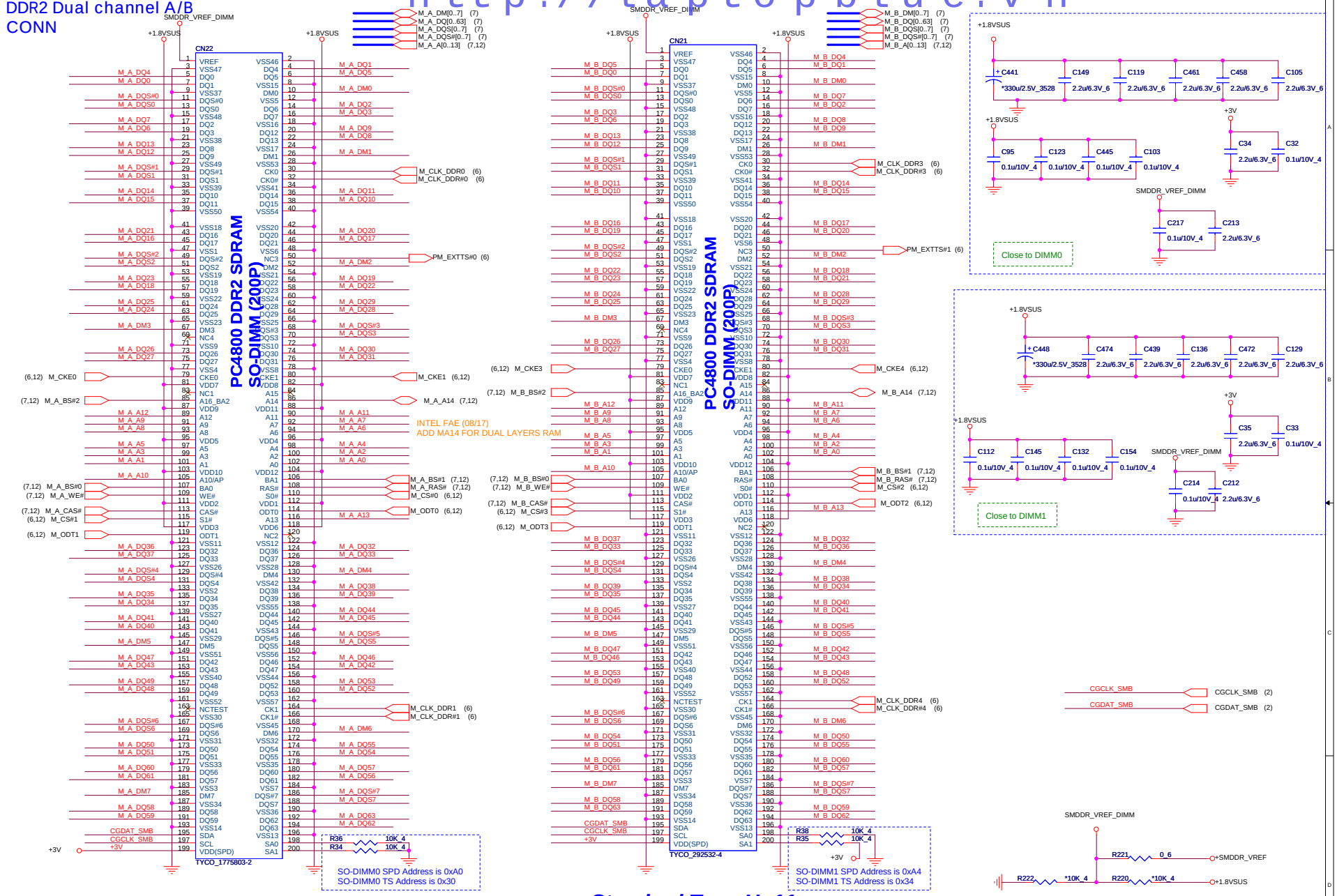
DDR2 Dual channel A/B CONN



Standard Type H: 6.5mm

CLOCK 0,1
CKE 0,1

Standard Type H: 11mm

CLOCK 3,4
CKE 2,3

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RTC CRYSTAL

RESET JUMP

An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided.

(DG 1.0 Table-292)

Internal VRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05.

24.9 Ohm pull up to 1.5V for GLAN_COMPI/O is required, no matter intel LAN is used or not.

LDRQ0/1# : Internal PU

Layout note: DPRSTP# , Daisy Chain (SB>Power>NB>CPU)

BOM Option Table

Reference	Description
IHM@	INT HDMI

U35A

ICH9M REV 1.0

SATA_RBIAS_PN<0.5" Avoid routing next to clock/high speed signals

Layout note: PU R needs to placed within 2" of ICH9-M, series R must be placed within 2"of PU R w/o stub.

02/14 REV_3A Swap SATA chennal

12/18 REV_2A Swap SATA chennal

SATA I/F

To 2'nd SATA HDD

To 1'st SATA HDD

To SATA ODD

To E-SATA

HD Audio I/F(CODEC& iHDMI)

10/14 Add

RTC BATTERY

02/12 REV_3A Change R528,R529,R532 value

South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT: 0/0 RSVD; 0/1 Enter XOR Chain; 1/0 Normal opration(Default); 1/1 Set PCIE port config bit 1	(16) ICH_TP3 — ICH_TP3 R264 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R R582 *1K_4 +3V_HDA_IO_ICH PU +1.5V

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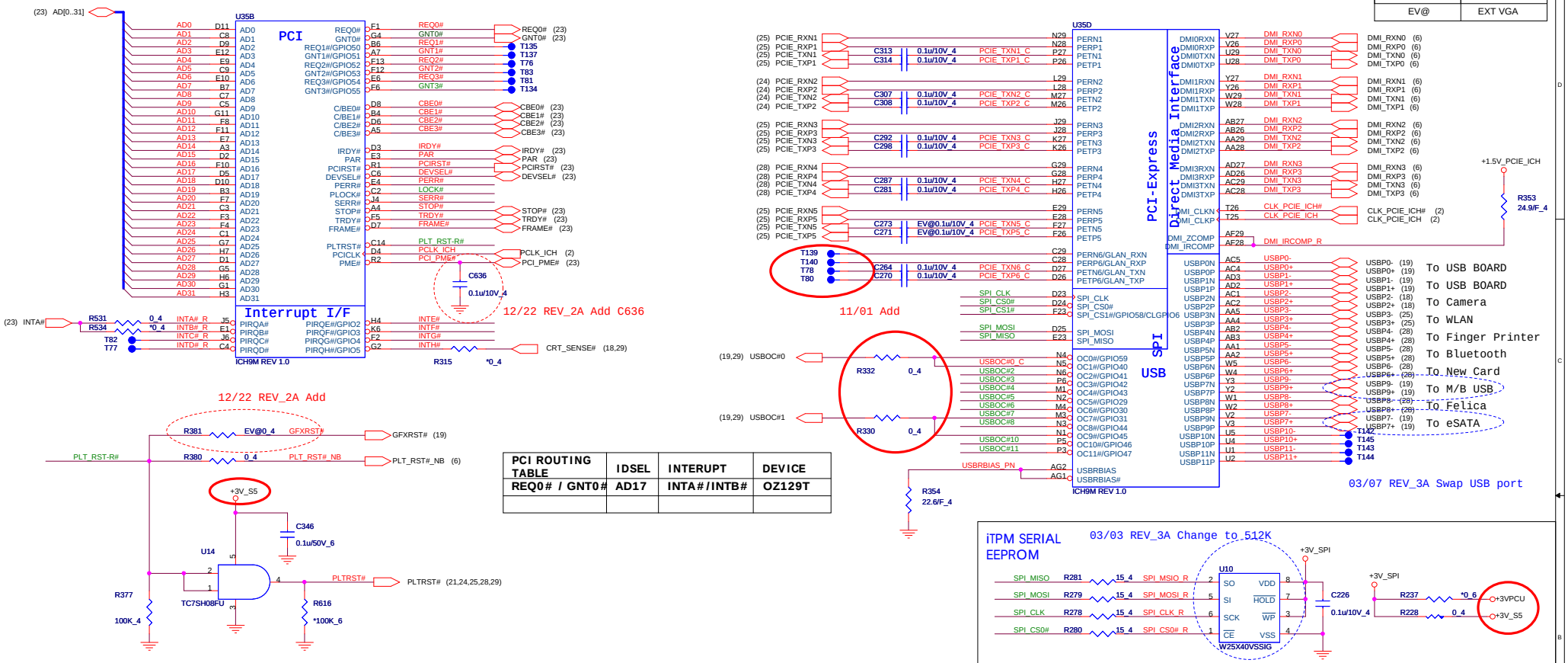
PCI/PCI-E/USB/DMI/SPI

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA



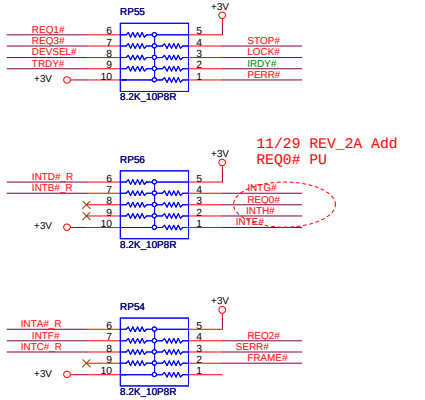
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#/INTB#	OZ129T

South Bridge Strap Pin (2/3)

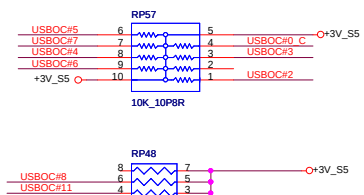
Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R511 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	Enable iTPM SPI_MOSI R295 *20K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK		GNT0# R304 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# R314 *1K_4

PCI_GNT#0	SPI_CS#1	Boot Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

PCI PULL-UP



USBOC# PULL-UP



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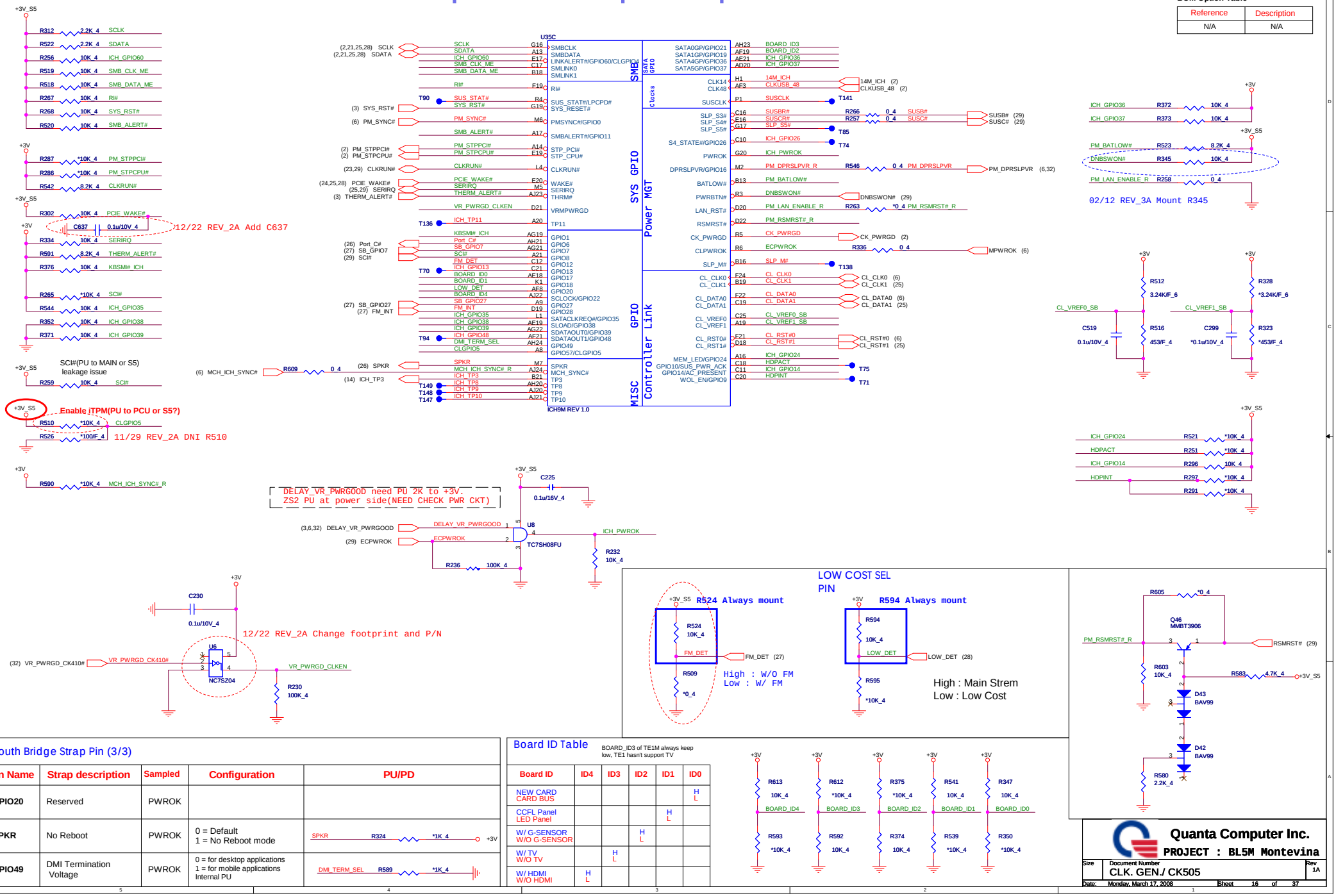


South Bridge Strap Pin (3/3)

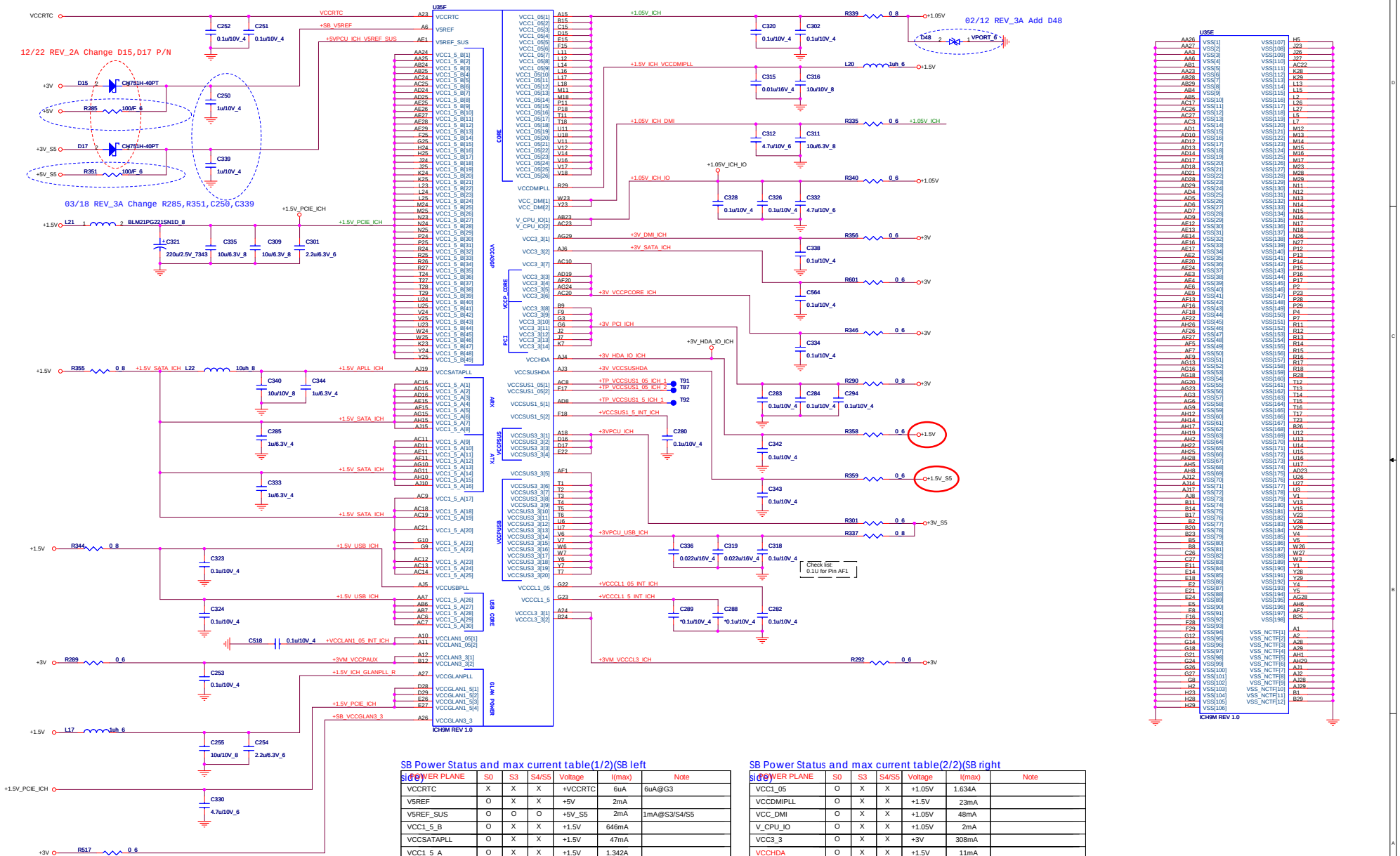
Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	SPKR R324 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R589 *1K_4

Board ID Table

BOARD_ID3 of TE1M always keep low, TE1 hasn't support TV

Board ID	ID4	ID3	ID2	ID1	ID0
NEW CARD CARD BUS					H L
CCFL Panel LED Panel				H L	
W/ G-SENSOR W/O G-SENSOR			H L		
W/ TV W/O TV		H L			
W/ HDMI W/O HDMI	H L				

Quanta Computer Inc.
PROJECT : BL5M Montevina
Size | Document Number: CLK. GEN./ CK505 | Rev: 1A
Date: Monday, March 17, 2008 | Sheet 16 of 37



BOM Option Table

Reference	Description
N/A	N/A

SB Power Status and max current table(1/2)(SB left side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCCRTC	X	X	X	+VCCRTC	6uA	6uA@G3
V5REF	O	X	X	+5V	2mA	
V5REF_SUS	O	O	O	+5V_S5	2mA	1mA@S3/S4/S5
VCC1_5_B	O	X	X	+1.5V	646mA	
VCCSATAPLL	O	X	X	+1.5V	47mA	
VCC1_5_A	O	X	X	+1.5V	1.342A	
VCCUSBPLL	O	X	X	+1.5V	11mA	
VCCLAN1_05	O	X	X	+1.05V	X	Powered by Vcc1_05 in S0
VCCLAN3_3	O	X	X	+3V	19mA	Tied to +3V,not +3VSUS
VCCGLANPLL	O	X	X	+1.5V	23mA	
VCCGLAN1_5	O	X	X	+1.5V	80mA	
VCCGLAN3_3	O	X	X	+3V	1mA	

SB Power Status and max current table(2/2)(SB right side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC1_05	O	X	X	+1.05V	1.634A	
VCCDMIPLL	O	X	X	+1.5V	23mA	
VCC_DMI	O	X	X	+1.05V	48mA	
V_CPU_IO	O	X	X	+1.05V	2mA	
VCC3_3	O	X	X	+3V	308mA	
VCCHDA	O	X	X	+1.5V	11mA	
VCCSUSHDA	O	O	O	+1.5V_S5	11mA	1mA@S3/S4/S5
VCCSUS1_05	O	O	O	+1.05V	X	Powered by Vcc1_05 in S0
VCCSUS1_5	O	O	O	+1.5V	X	Powered by Vcc1_5_A in S0
VCCSUS3_3	O	O	O	+3VSUS	212mA	52mA@S3/S4/S5
VCCCL1_05	O	X	X	+1.05V	X	Powered by Vcc1_05 in S0
VCCCL1_5	O	X	X	+1.5V	X	Powered by Vcc1_5_A in S0
VCCCL3_3	O	X	X	+3V	19mA	Tied to +3V,not +3VSUS

Note:VCCSUS1_05 , VCCSUS1_5 are powered by VccSus3_3 in S3/S4/S5

Quanta Computer Inc.
PROJECT : BL5M Montevina
Size: Document Number: CLK. GEN./ CK505 Rev: 1A
Date: Tuesday, March 18, 2008 Sheet 17 of 37

CRT PORT

BOM Option Table	
Reference	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT HDMI
EV_IV@	EV&IV diff. value

03/08 REV_3A Chage L2,L3,L4 P/N to CX8BA470003

03/08 REV_3A Chage C8,C6,C4,C3,C5,C7 P/N to CH-686T0B07

H=1.75mm

03/07 REV_3A Del RP1

HALL SENSOR

02/12 REV_3A Reserve DISPON to EC

10/30 Change Value

02/12 REV_3A Add D49

12/18 REV_2A Del D28,R412
12/18 REV_2A Add Q53,Q54,R652

CAMERA MODULE

02/12 REV_3A Add C640 for EMI

LCD PANEL MODULE

10/23 Add

12/18 REV_2A Add C628

02/12 REV_3A Mount C14 for EMI

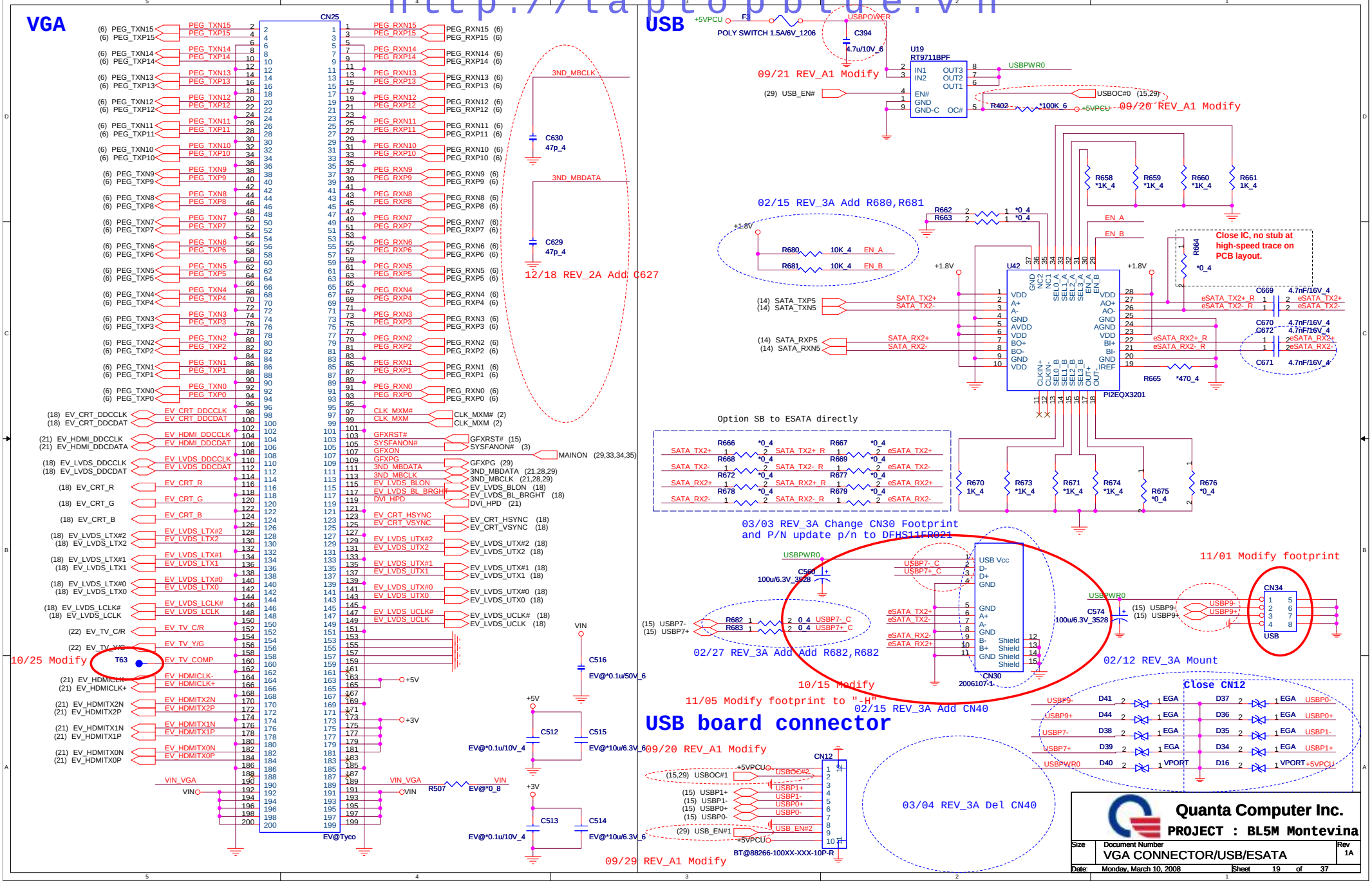
8/14 Modify Pin Define

12/18 REV_2A Add

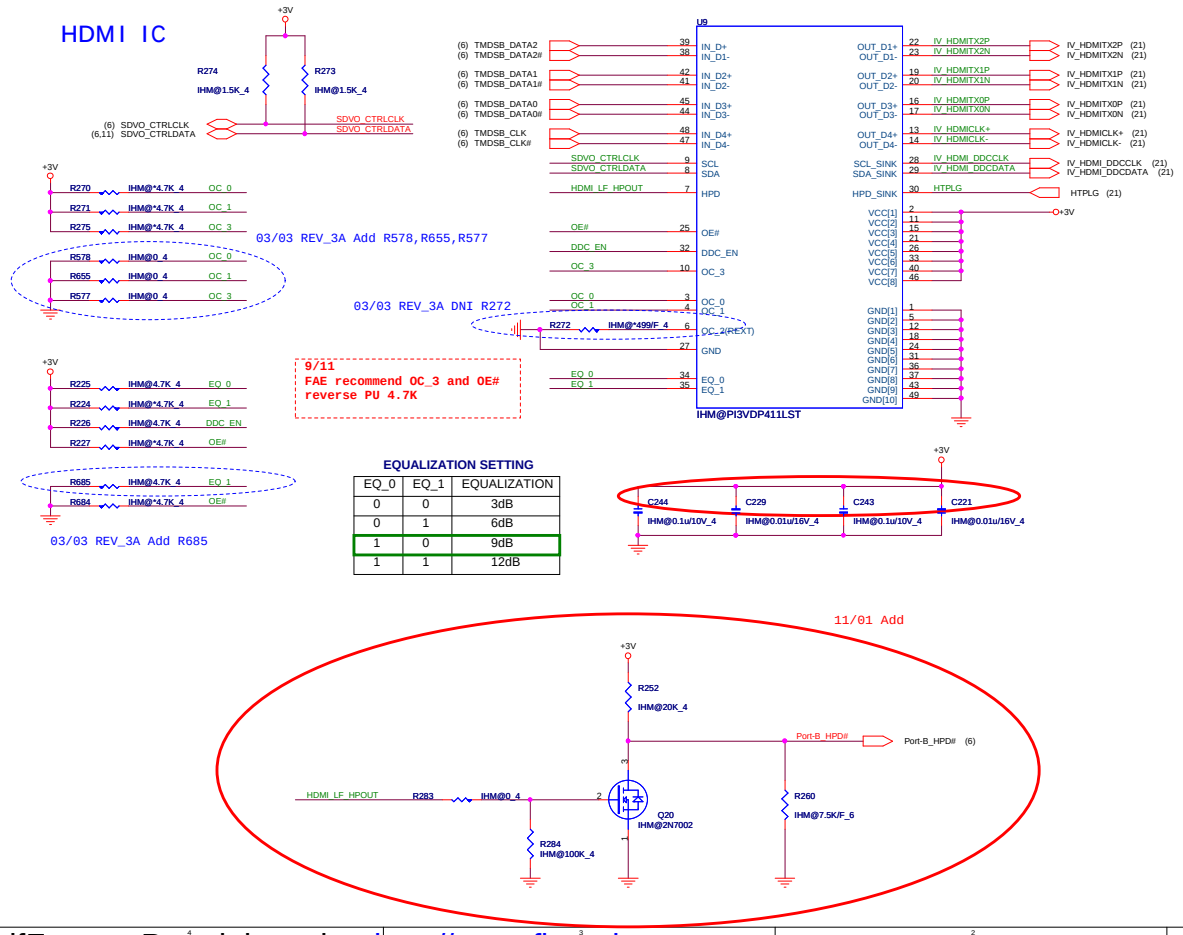
Quanta Computer Inc.
PROJECT : BL5M Montevina

Size	Document Number	Rev
	LCD/CRT/LID/CAMERA	1A

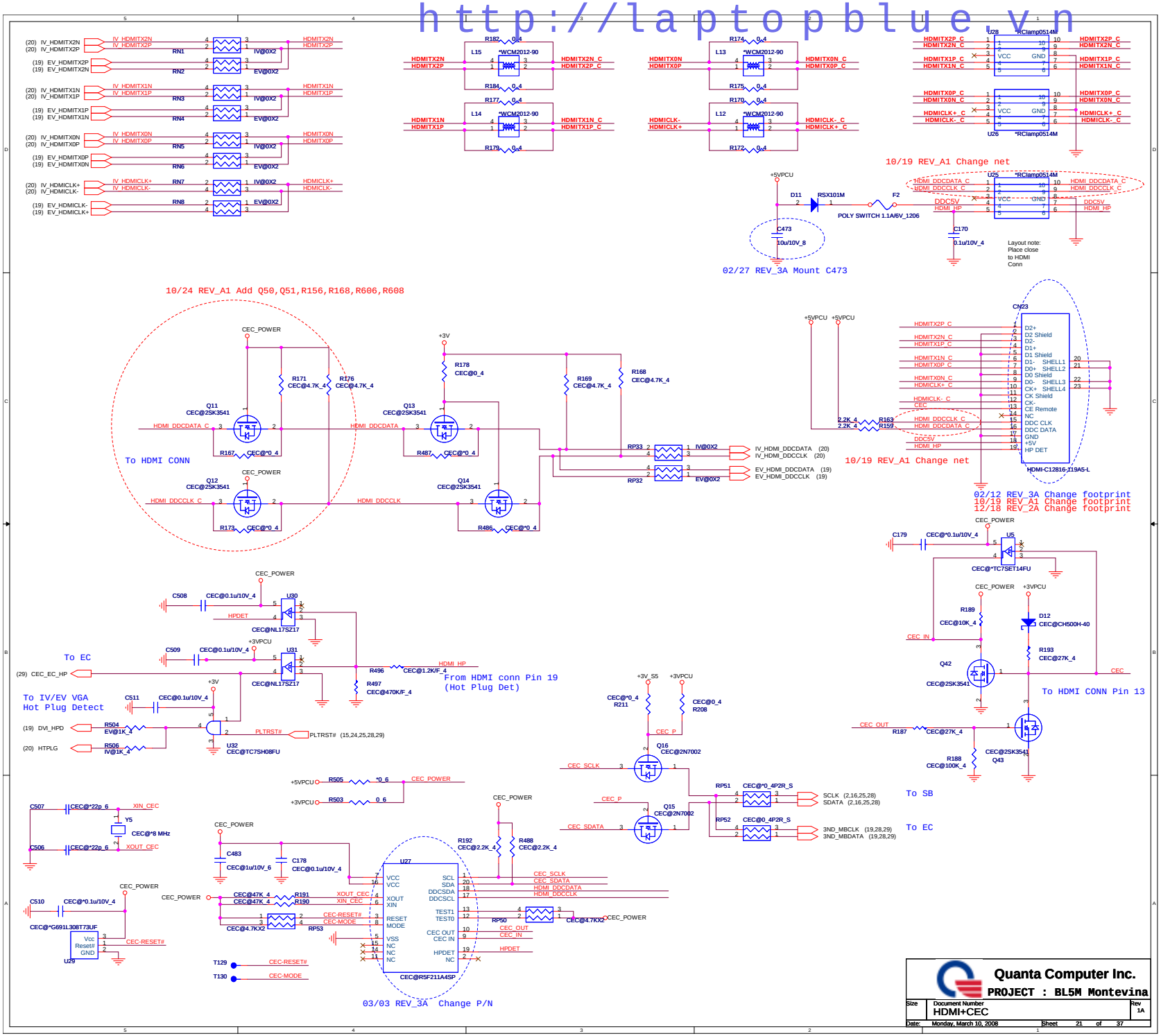
Date: Monday, March 10, 2008 Sheet 18 of 37



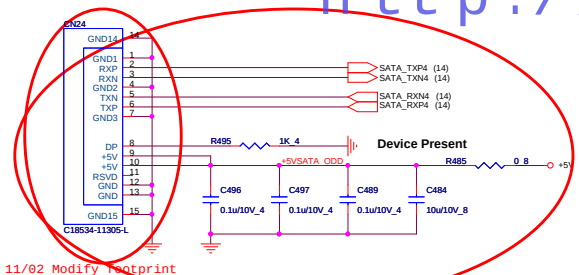
Only For UMA



Quanta Computer Inc.
PROJECT : BL5M Montevina
Size | Document Number: PI3VDP411LST(HDMI) | Rev 1A
Date: Monday, March 17, 2008 | Sheet 20 of 37

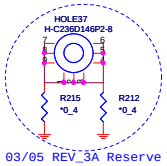


SATA ODD



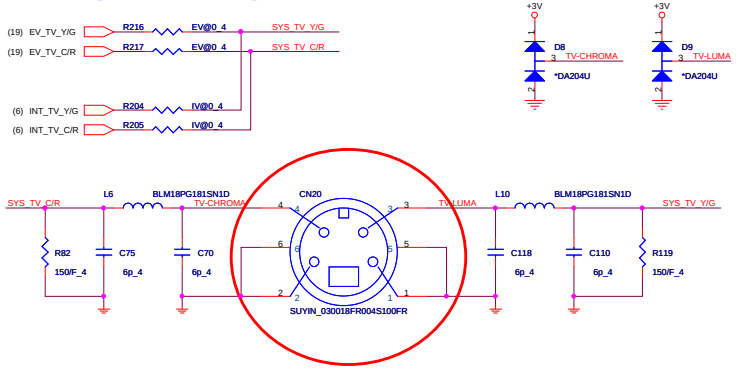
11/02 Modify footprint

10/15 Add



03/05 REV_3A Reserve R215,R212 fro EMI

TVOUT



10/25 Modify
11/01 Modify Footprint

CPU SINK

VGA SINK

MB SINK

10/23 REV_A1 Modify footprint
10/26 REV_A1 Modify footprint

02/12 REV_3A Modify HOLE32 to AGND
09/27 REV_A1 Modify Footprint

12/18 REV_2A Modify
10/26 REV_A1 Del HOLE34 for EXP

MINI-1 SINK

MODEM

02/12 REV_3A Change footprint

MINI-2 SINK

10/20 REV_A1 Add
10/22 REV_A1 Modify

LED / WLAN SW

02/12 REV_3A change LED4,LED3 footprint and P/N

10/26 REV_A1 Add

03/10 REV_3A Add

10/30 Copy from BL5S

12/18 REV_2A Add

11/05 Add

W-LAN&BT LED

Mainstream --> Orange
Low Cost --> Orange

WiMAX LED

10/25 Modify
03/07 REV_3A Mount R649

02/27 REV_3A Mount D24,D47

02/12 REV_3A Change R415,R414 value

10/25 Modify
12/18 REV_2A Change LED type

Mainstream --> White
Low Cost --> N/A

09/20 REV_A1 Add HOLE32,HOLE33 for ESATA

09/20 REV_A1 Add HOLE30,HOLE31 for ESATA

2'nd SATA HDD

02/12 REV_3A Add for ESD

02/12 REV_3A Change footprint

SATA HDD

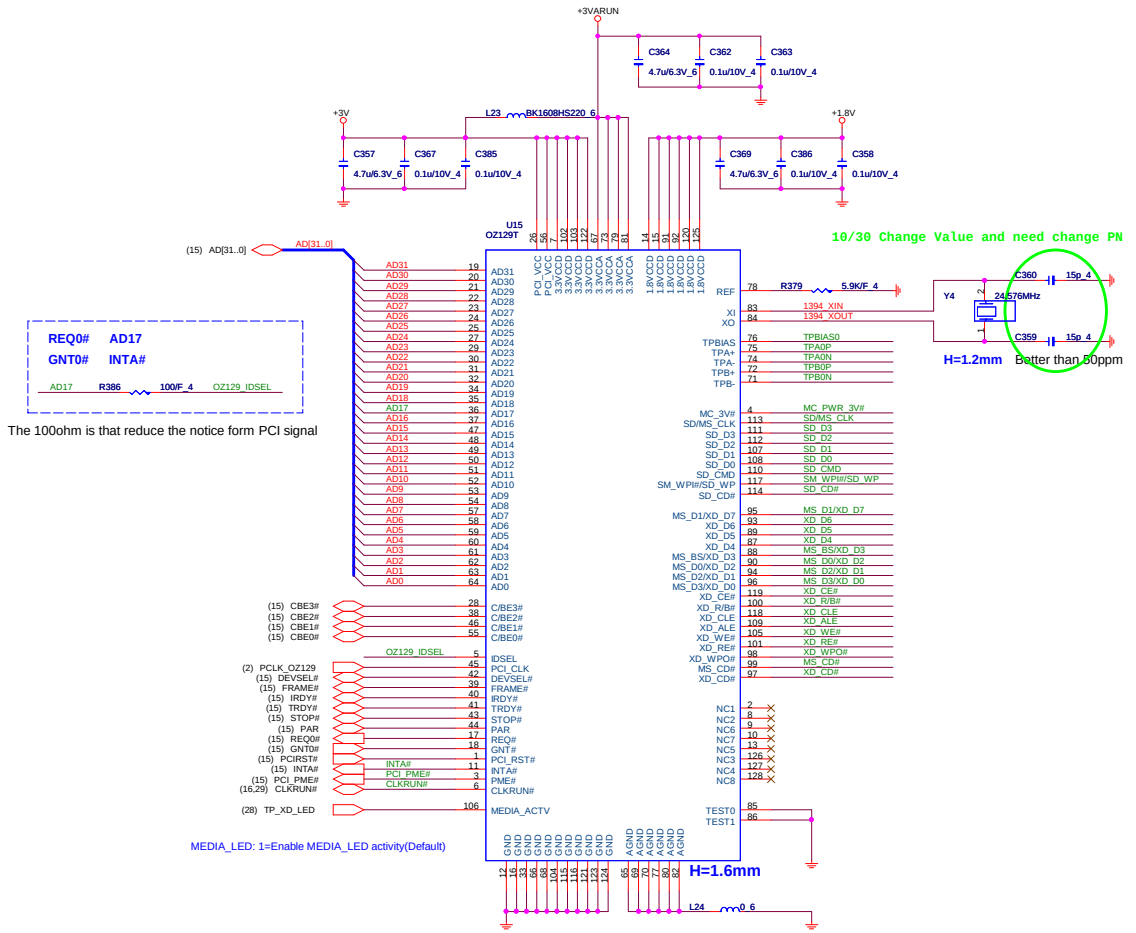
03/09 REV_3A Del

12/18 REV_2A Change P/N

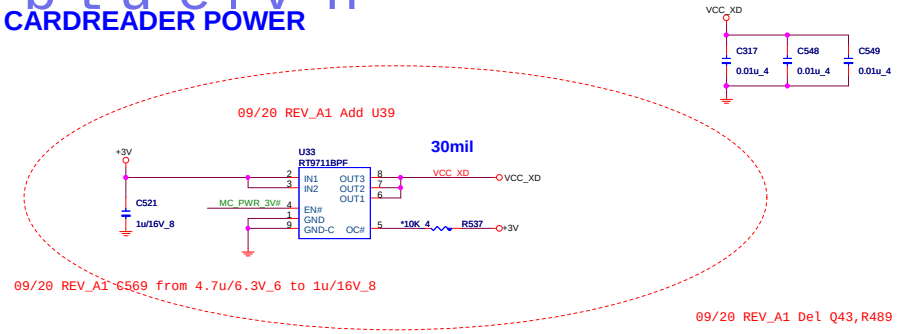
02/12 REV_3A Change footprint

Quanta Computer Inc.
PROJECT : BL5M Montevina

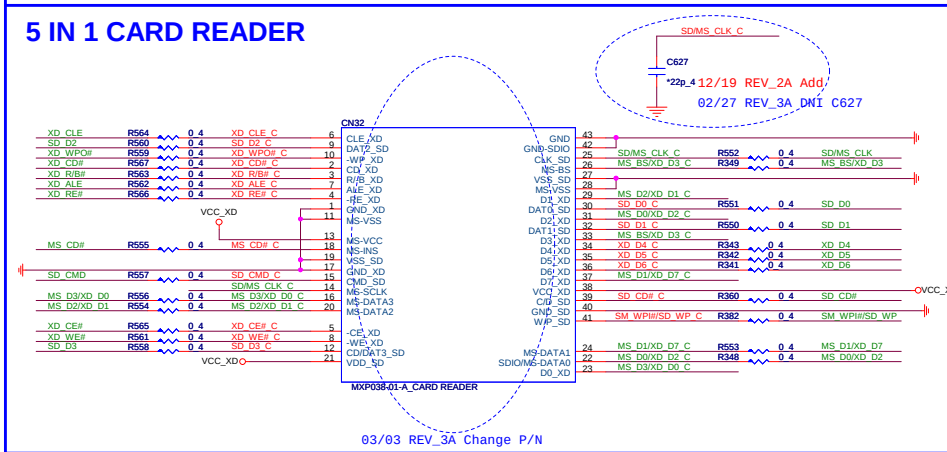
Size	Document Number	Rev
	PATA/ODD/TV/LED	1A
Date: Monday, March 10, 2008	Sheet 22 of 37	



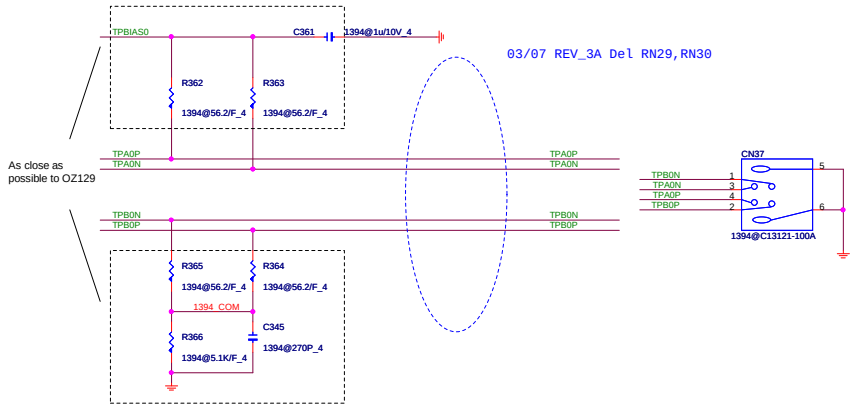
CARDREADER POWER



5 IN 1 CARD READER



1394



Quanta Computer Inc.
PROJECT : BL5M Montevina

Size	Document Number	Rev
	OZ129T (Card Reader/1394)	1A

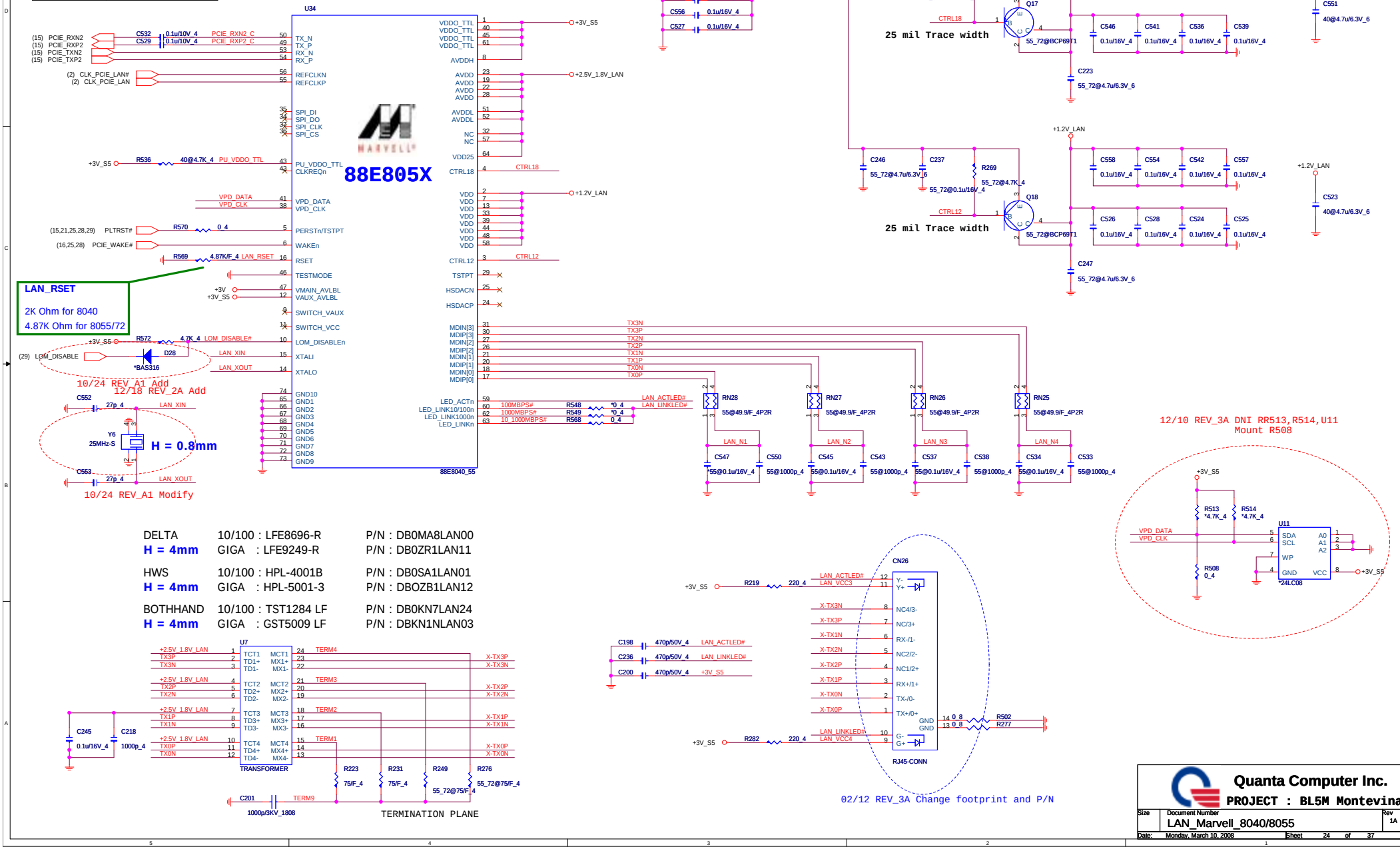
Date: Monday, March 10, 2008 Sheet 23 of 37

LAN_MARVELL_88E8040/88E8055

BOM Option Table

Reference	Description
40@	10/100 : 88E8040
55@	GIGA : 88E8055
55_72@	GIGA : 88E8072

10/100 : 88E8040 P/N : AL008040001
GIGA : 88E8055 P/N : AJ080550000
GIGA : 88E8072 P/N : AL008072000



DELTA 10/100 : LFE8696-R P/N : DB0MA8LAN00
H = 4mm GIGA : LFE9249-R P/N : DB0ZR1LAN11

HWS 10/100 : HPL-4001B P/N : DB0SA1LAN01
H = 4mm GIGA : HPL-5001-3 P/N : DBOZB1LAN12

BOTHHAND 10/100 : TST1284 LF P/N : DB0KN7LAN24
H = 4mm GIGA : GST5009 LF P/N : DBKN1NLAN03

Quanta Computer Inc.	
PROJECT : BL5M Montevina	
Size	Document Number: LAN_Marvell_8040/8055 — Rev: 1A
Date: Monday, March 10, 2008	Sheet 24 of 37

Mini PCI-E Card WLAN

MINI-Card I

09/28 REV_A1 Modify

03/14 REV_3A DNI

12/04 REV_2A Change to +3V_S5

12/04 REV_2A Change to +3V_S5

12/04 REV_2A Mount R24

10/30 Modify Wimax LED net.

12/13 REV_2A Add

03/03 REV_3A Add

To BT

09/28 REV_A1 Modify

12/04 REV_2A Change to +3V_S5

MINI-Card II

09/20 REV_A1 Modify

12/23 REV_2A Change P/N

EMI

12/20 REV_2A Add PAD

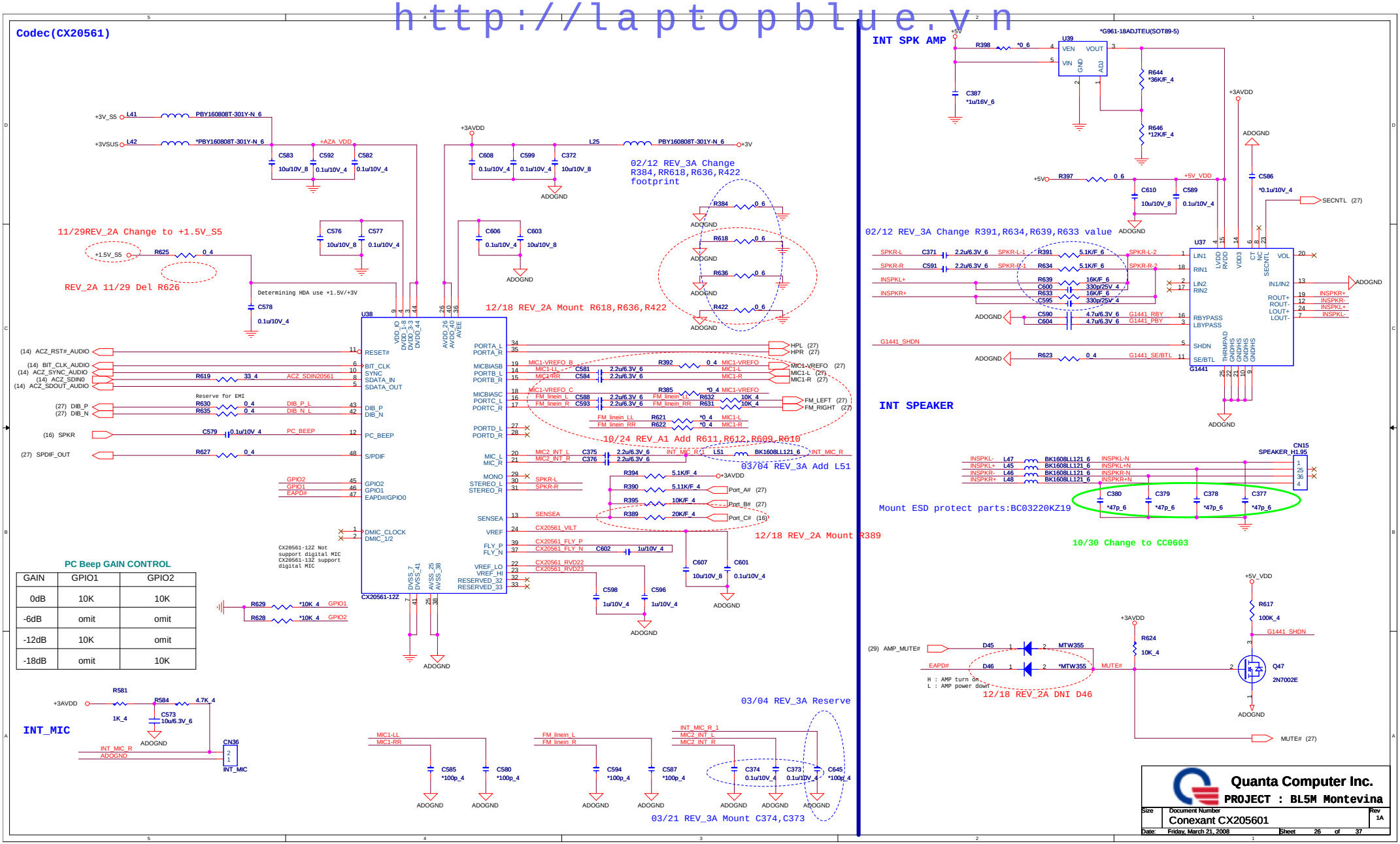
12/18 REV_2A Add C620~C626

12/18 REV_2A Add C618

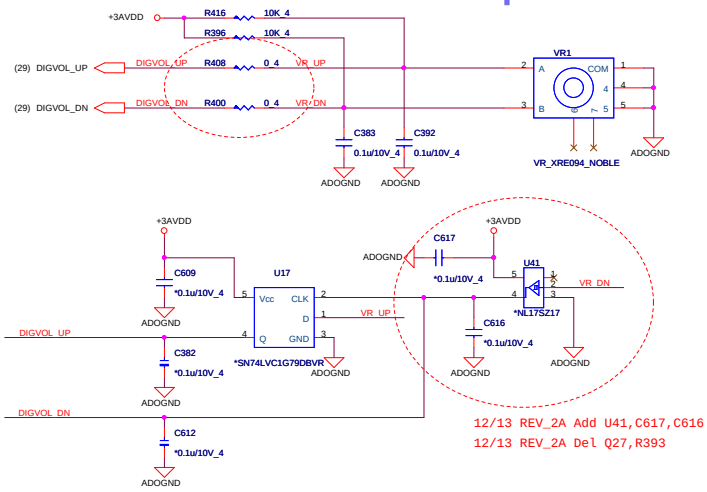
MINI-Card III

H= 8mm

Quanta Computer Inc.
PROJECT : BL5M Montevina
Size: Document Number: MINI PCIE/HOLE Rev: 1A
Date: Friday, March 14, 2008 Sheet 25 of 37

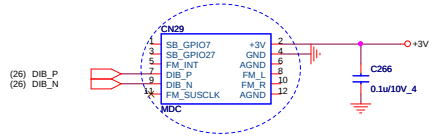


VR



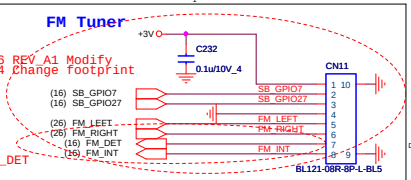
MDC

02/12 REV_3A Change footprint



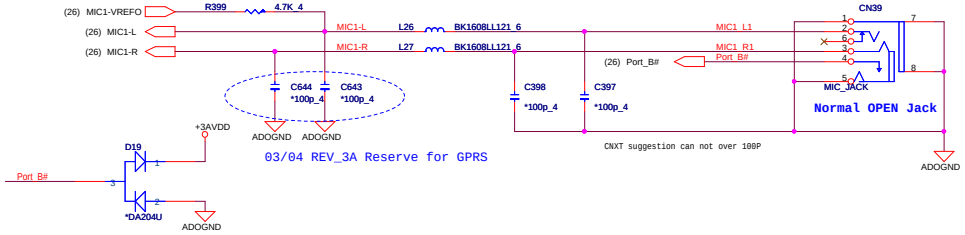
FM Tuner

09/26 REV_A1 Modify
10/24 Change footprint



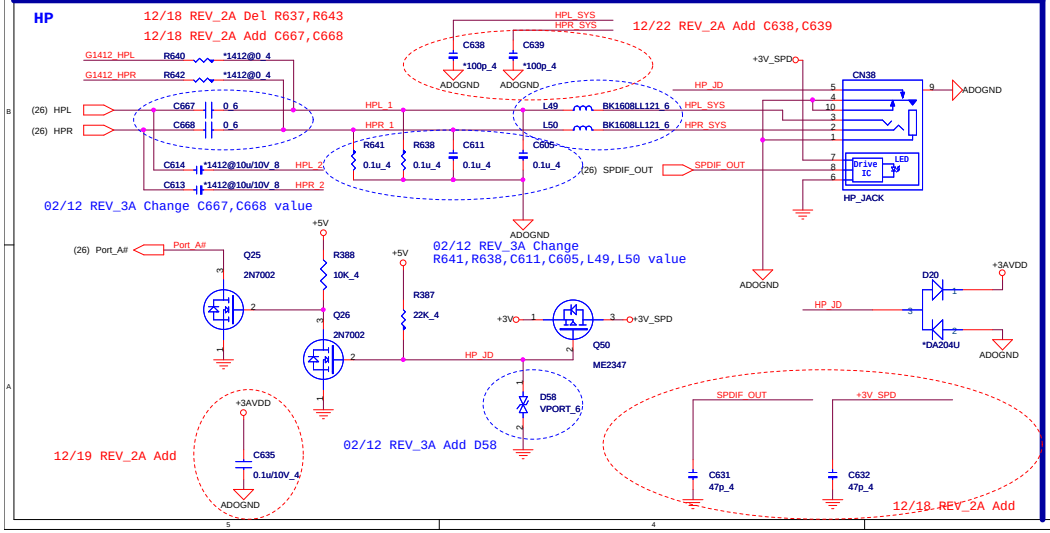
11/05 Add FM_DET

SYSTEM MIC

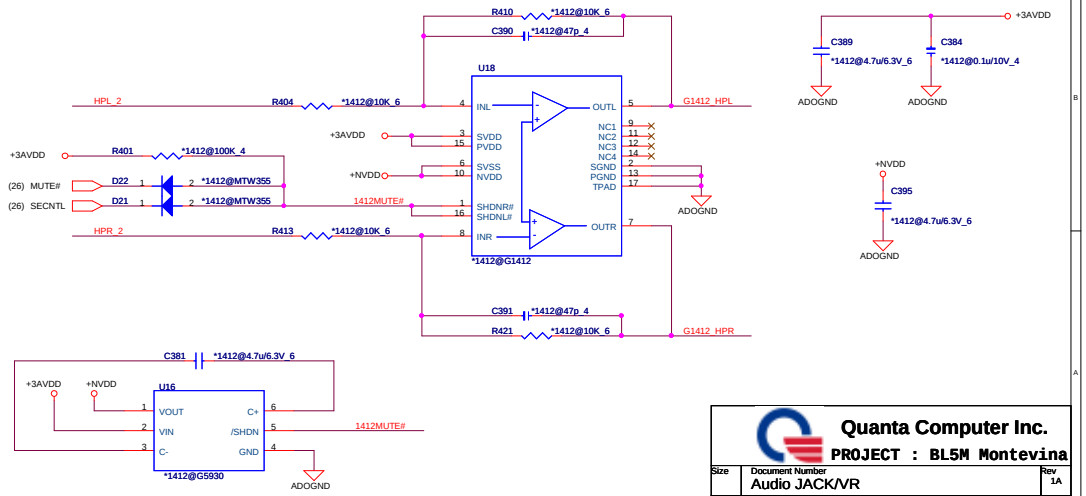


HP

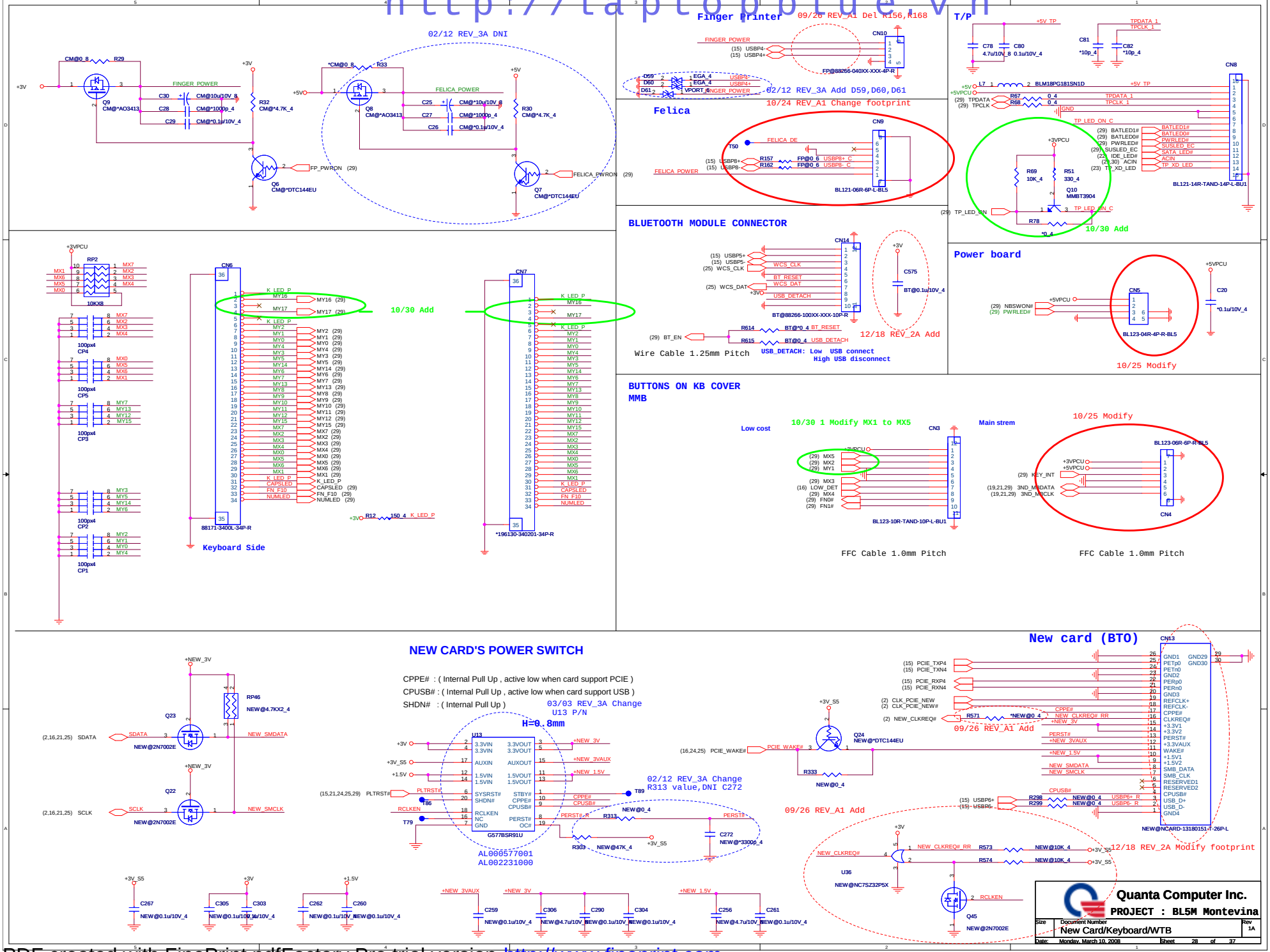
12/18 REV_2A Del R637,R643
12/18 REV_2A Add C667,C668



HP Amplifier



Quanta Computer Inc.
PROJECT : BL5M Montevina
Size
Document Number
Audio JACK/VR
Rev 1A
Date: Monday, March 10, 2008
Sheet 27 of 37



Page 29 copy from BL5S

SMBUS Table

SMBUS	Devices
1	Battery
2	CPU Thermal Sensor 3D Sensor EC EEPROM
3	VGA Board Thermal Sensor Touch Sensor

SM BUS PU

I/O Base Address

BADDR1-0	I/O Address	
	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

12/18 REV_2A R54 DNI,R56 mount

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID

H=1.75mm

24LC08BT-I

ADDRESS: A0H

SPI FLASH

H=2.16mm

W25X80VSSIG

INTERNAL KEYBOARD STRIP SET

CIR (Copy from PB2A)

Only for 8769/775C

10/19 REV_A1 Change footprint
10/21 REV_A1 Change pin define

10/26 REV_A1 Add R64,R73,R176

09/20 REV_A1 Modify

09/29 REV_A1 Modify

02/12 REV_3A Add to control MMB LED

10/22 REV_A1 Modify

10/24 REV_A1 Add

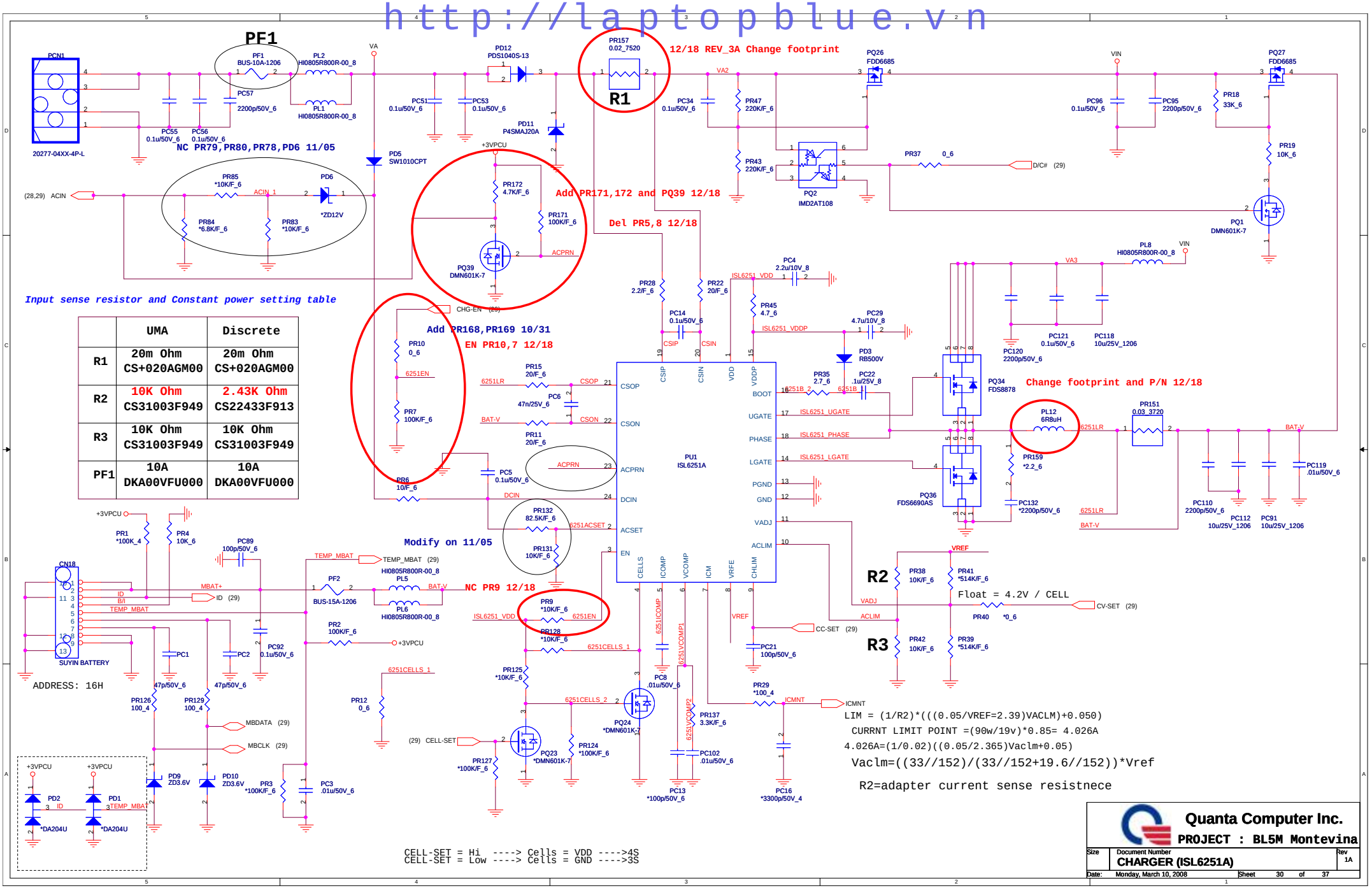
10/26 REV_A1 Modify

03/03 REV_3A Add WMAX_P net

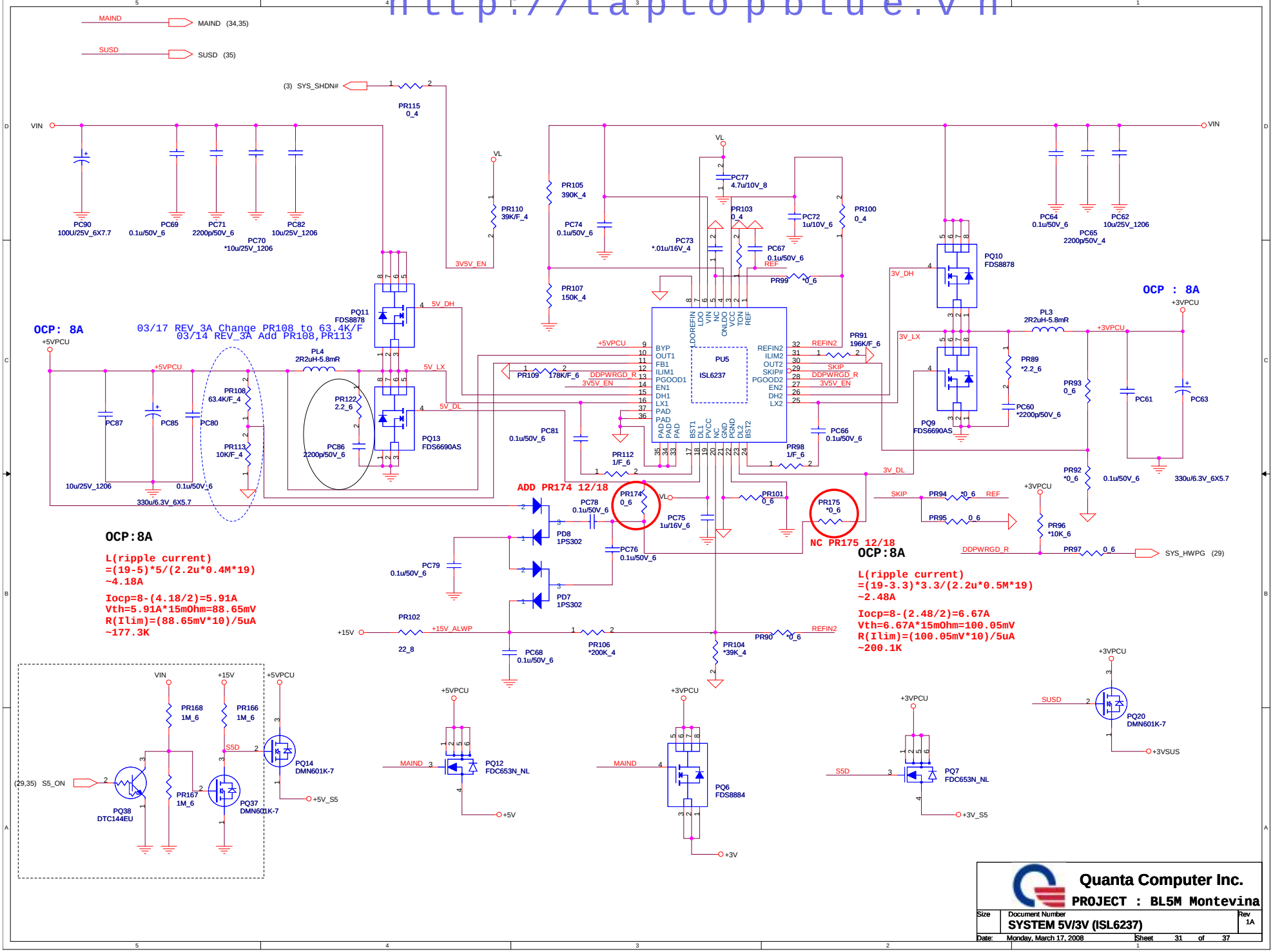
11/05 Add

11/01 Del D12

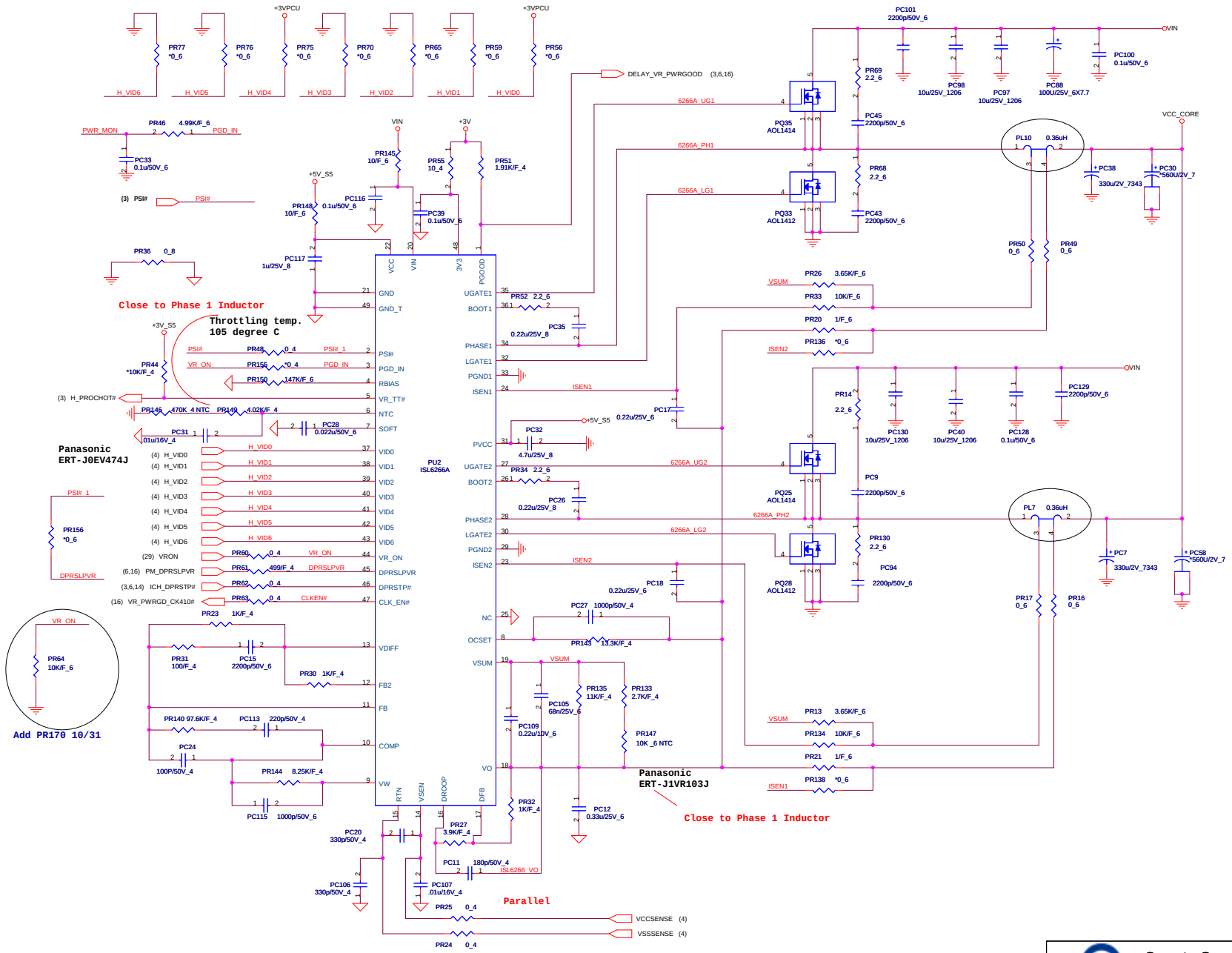
Quanta Computer Inc.	
PROJECT : BL5M Montevina	
Size	Document Number: EC-WPCE775C — Rev: 1A
Date: Monday, March 10, 2008	Sheet 29 of 37



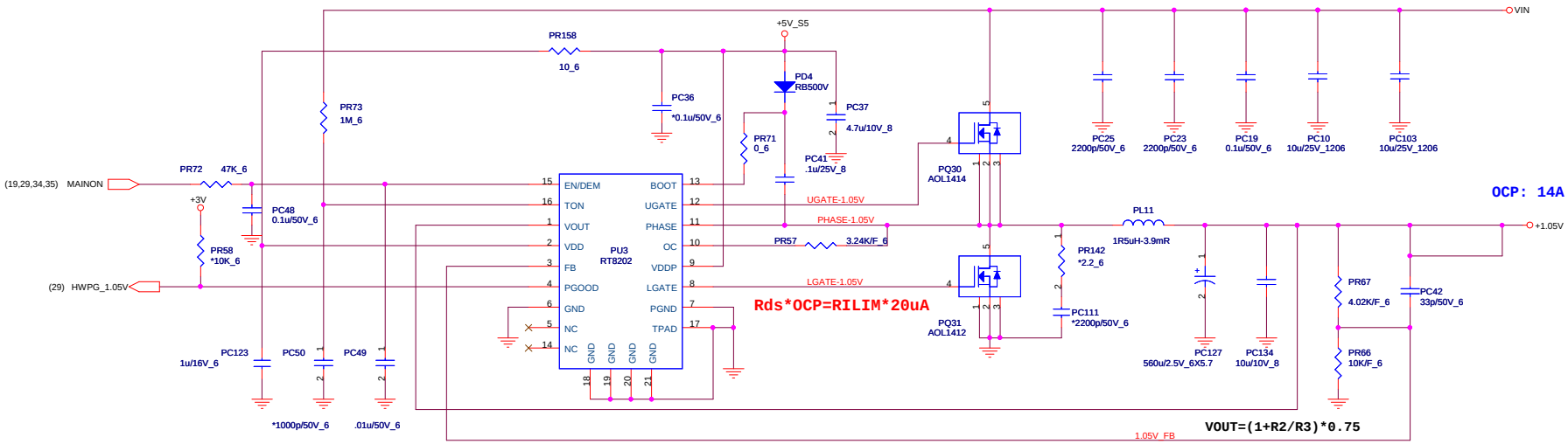
	UMA	Discrete
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	10K Ohm CS31003F949	2.43K Ohm CS22433F913
R3	10K Ohm CS31003F949	10K Ohm CS31003F949
PF1	10A DKA00VFU000	10A DKA00VFU000



Quanta Computer Inc.		
PROJECT : BL5M Montevina		
Size	Document Number: SYSTEM 5V/3V (ISL6237)	Rev 1A
Date: Monday, March 17, 2008	Sheet 31 of 37	



Quanta Computer Inc.		
PROJECT : BL5M Montevina		
Size	Document Number: CPU CORE(ISL6266A)	Rev: 1A
Date: Monday, March 10, 2008	Sheet 32 of 37	

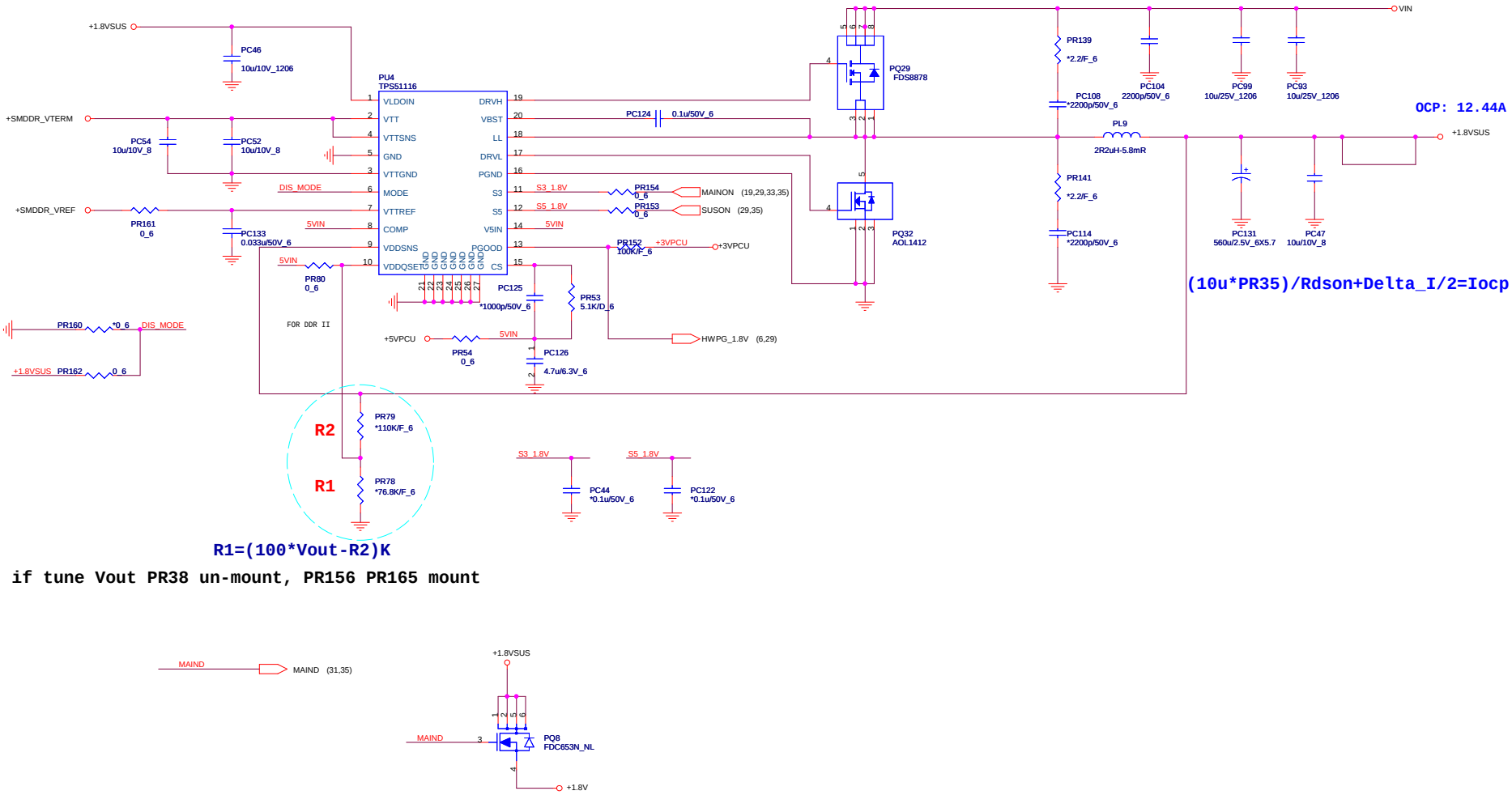


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

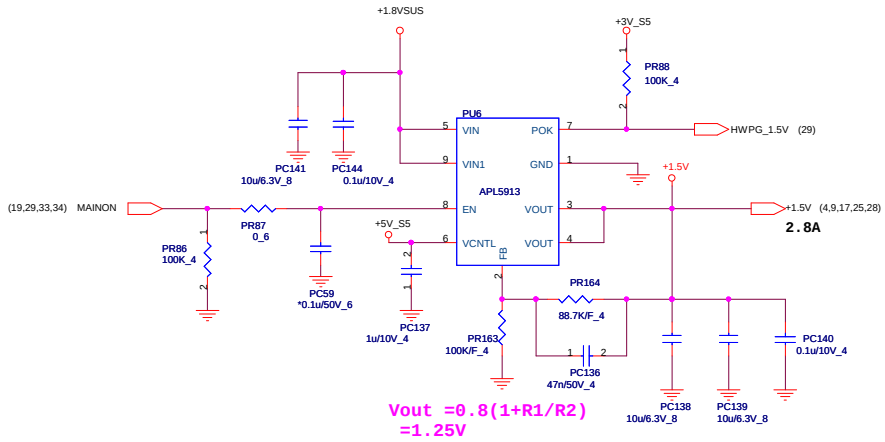
AOL1412 Rds=4.6mOhm
14A OCP --- OC=3.22K

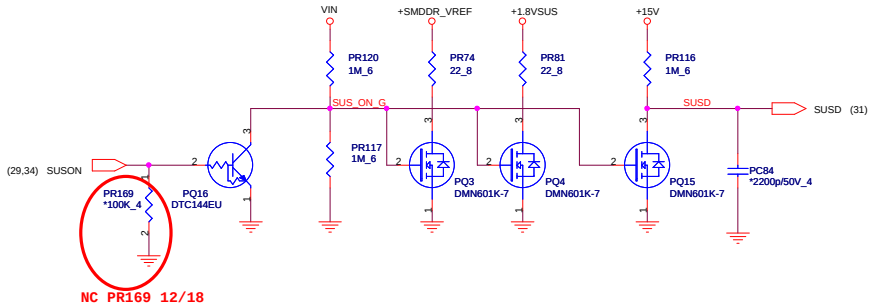
Quanta Computer Inc.		
PROJECT : BL5M Montevina		
Size	Document Number: VTT 1.05V (RT8202)	Rev: 1A
Date: Monday, March 10, 2008	Sheet 33 of 37	

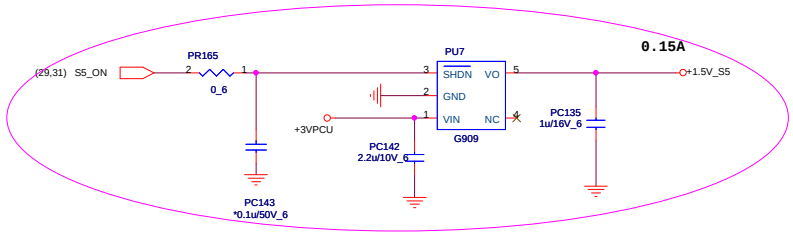


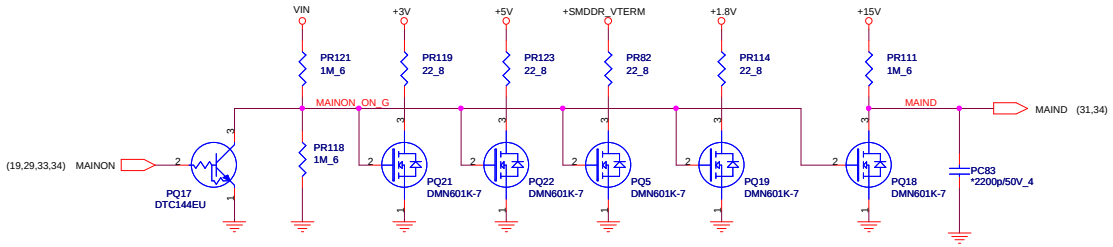
Quanta Computer Inc.
PROJECT : BL5M Montevina

Size	Document Number	Rev
	DDR 1.8V(TPS51116)	1A
Date: Monday, March 10, 2008	Sheet 34 of 37	









Quanta Computer Inc.
PROJECT : BL5M Montevina

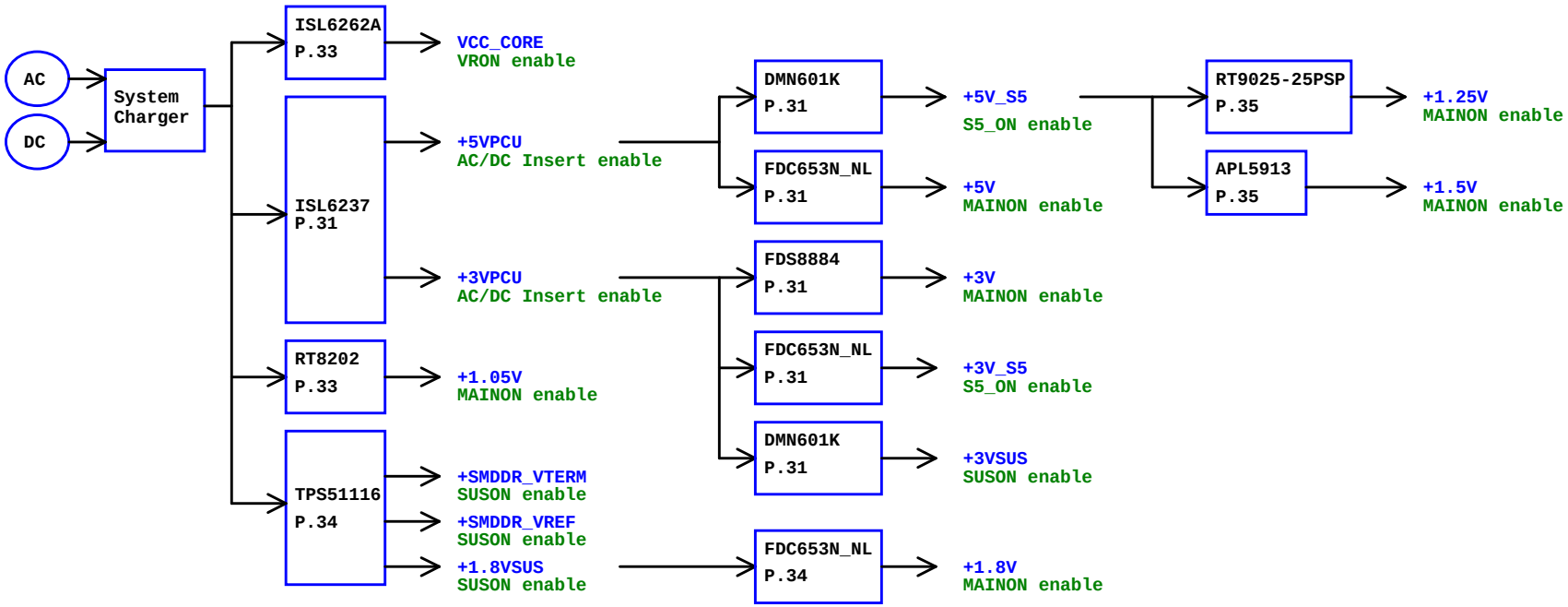
Size	Document Number	Rev
	Discharge (1.25V/1.5V)	1A
Date: Monday, March 10, 2008	Sheet 35 of 37	

Model	REV	DATE	CHANGE LIST	NOTE
BL5S	00	20070824	FIRST RELEASED : 20070824	
	1A	20070914	FIRST RELEASED : E200709-2519	

Quanta Computer Inc.
PROJECT : BL5M Montevina

Size	Document Number	Rev
	Change List	1A

Date: Tuesday, March 04, 2008 Sheet 36 of 37



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.8VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T) Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	HDMI, Cardreader (OZ129T)
+1.25V	CLK, GMCH, ICH8M

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