

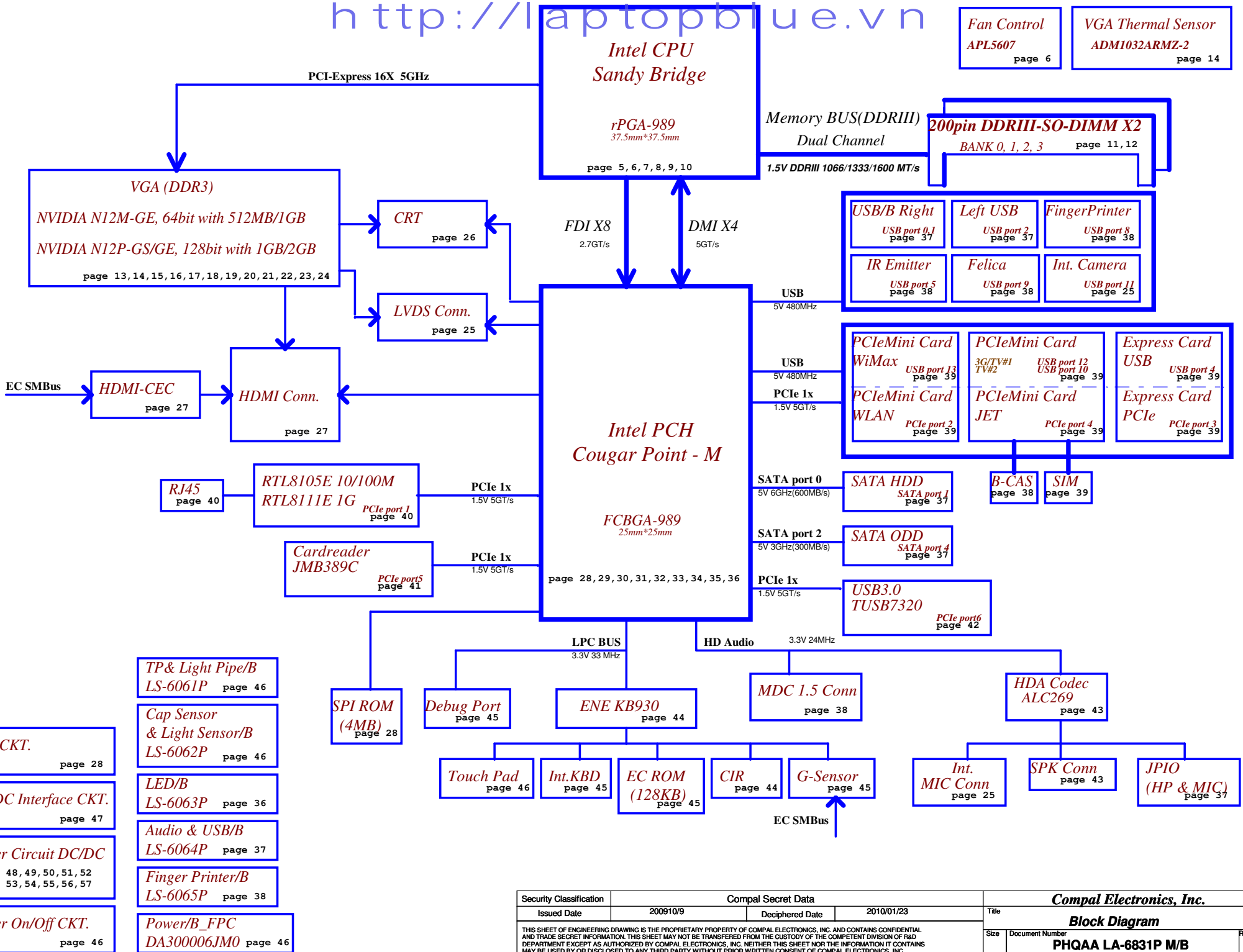
PHQAA

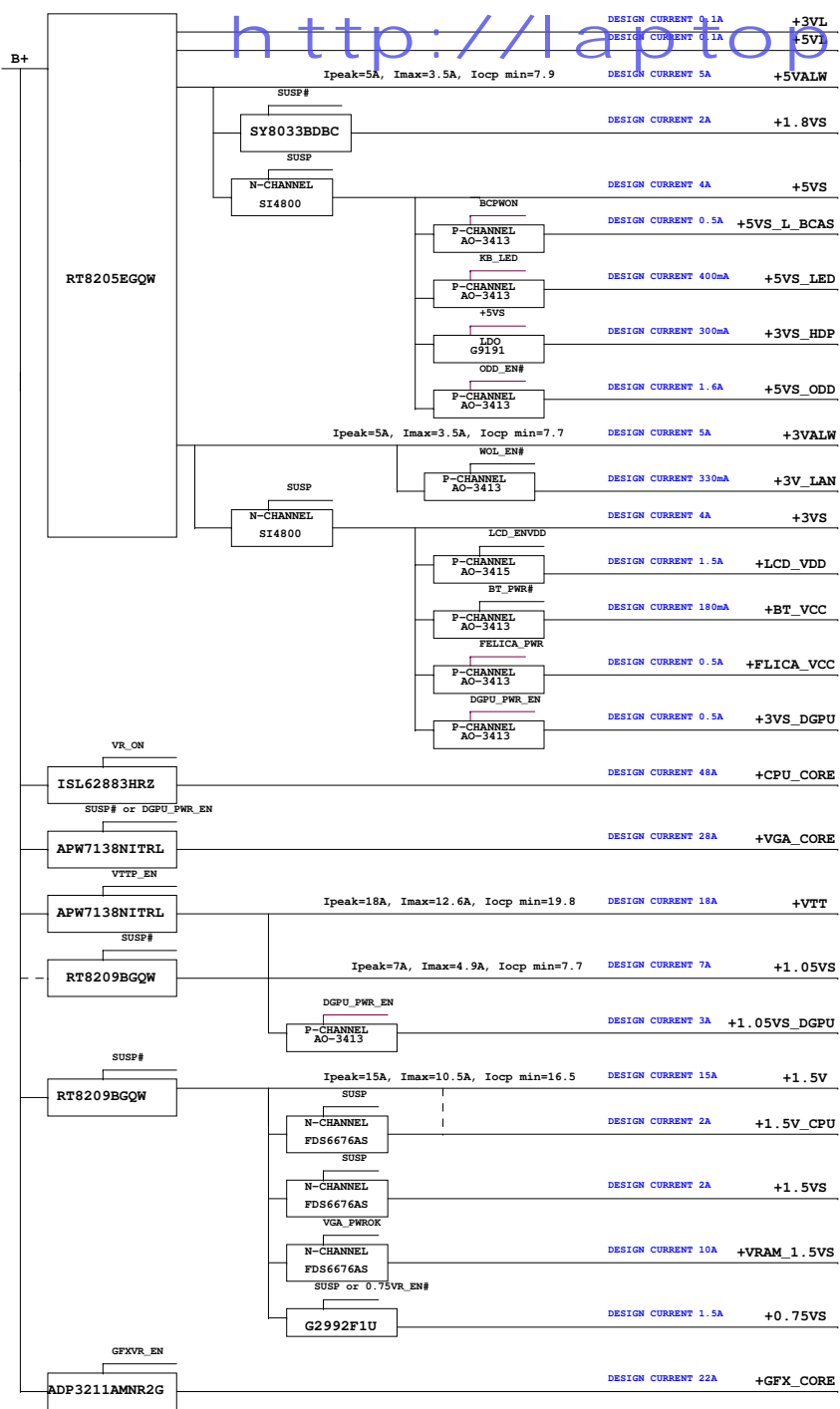
Marseille 10R/10RG

LA-6831P REV 0.1 Schematic

Intel Processor (Sandy Bridge) / PCH (Cougar Point)
2010-07-05 Rev 0.1

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b
Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9A H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	Light Sensor	52 H	0101 0010 b

Platform	SKU	CPU	PCH	VGA
Calpella	UMA(OPT@)	Arrandale	HM55@/HM57@	N/A
	Discrete (DIS@)	Clarksfield/Arrandale	HM55@/HM57@/PM55@	N11P@/N11M@
	Optimus (OPT@)	Arrandale	HM55@/HM57@	N11P@/N11M@

BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	MDC@	CIR@	KBL@

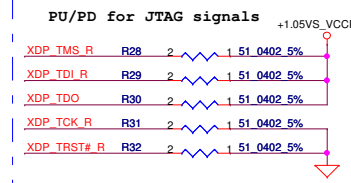
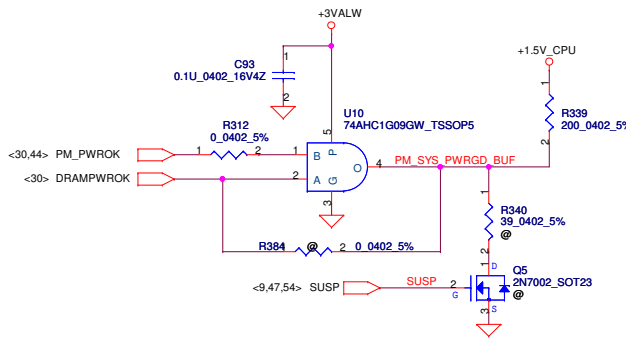
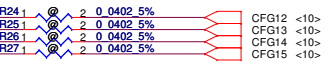
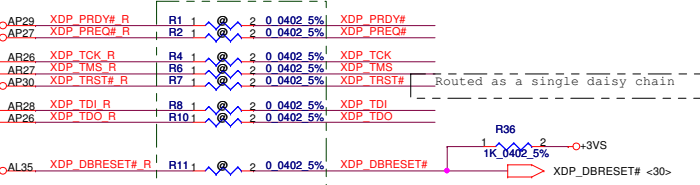
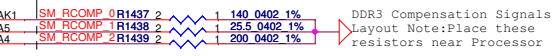
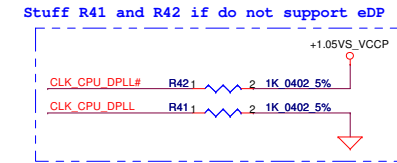
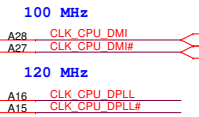
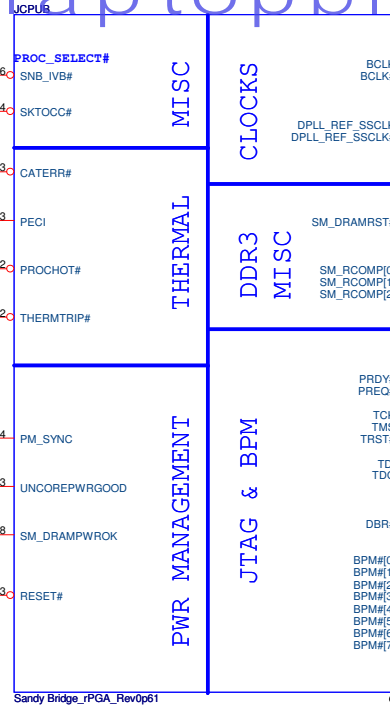
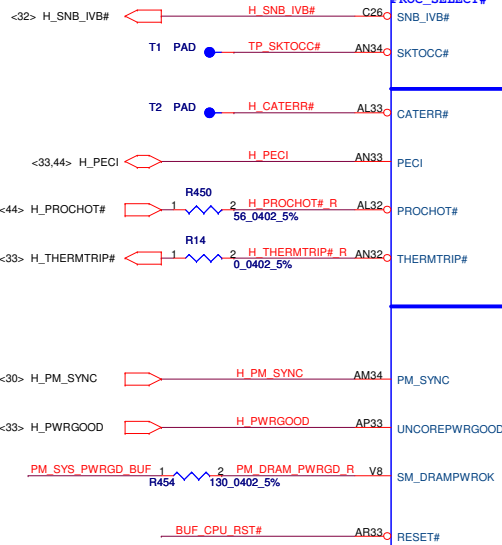
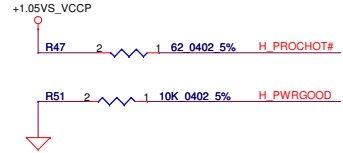
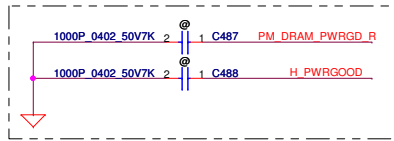
Function	Felica	BLUE TOOTH	G-SENSOR	SKU		LVDS		Camera & Mic	
description	Felica	BLUE TOOTH	G-SENSOR	SKU		3D Panel		Camera & Mic	
explain	Felica	BLUE TOOTH	G-SENSOR	Discrete	Optimus	Discrete		Optimus	Camera & Mic
BTO	FELICA@	BT@	GSENSOR@	DIS@	OPT@	3D@	NO3D@	OPTFH@	CAM@

Function	S3 Power Saving		GPU					
description	S3 Power Saving		N11P & N11E			N11M		
explain	No Power Saving	Power Saving	VRAM	N11P	N11E	N11M-GE1	N11M-GE2	N11M-OP1
BTO	NOPS@	PS@	8PCS@	N11P@	N11E@	N11MGE1@	N11MGE2@	N11MOP@

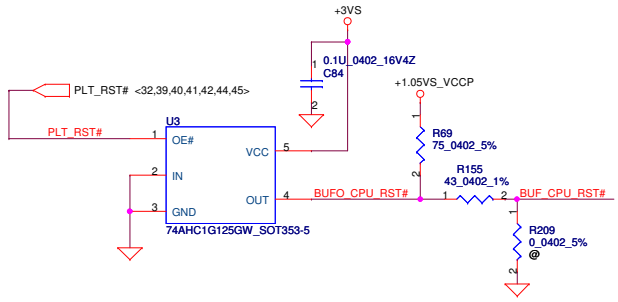
Function	Card reader		New Card
description	JMB385C/389C		New Card
explain	JMB385C	JMB389C	New Card
BTO	JMB385@	JMB389@	NEW@

STATE	SIGNAL		
	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

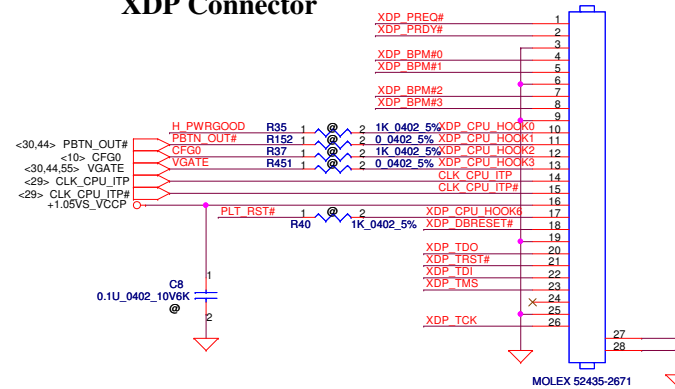
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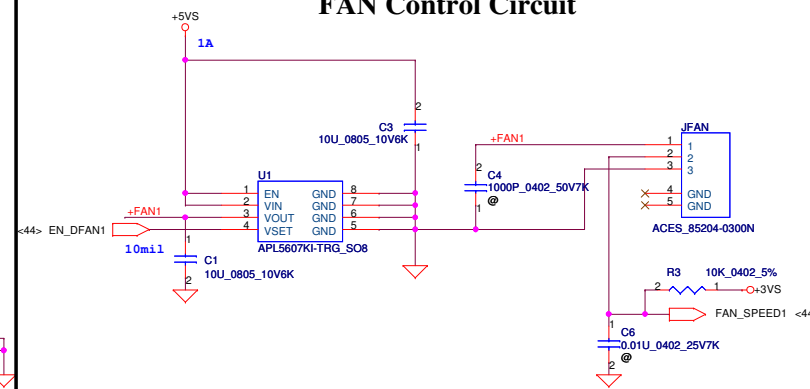
Buffered Reset to CPU



XDP Connector

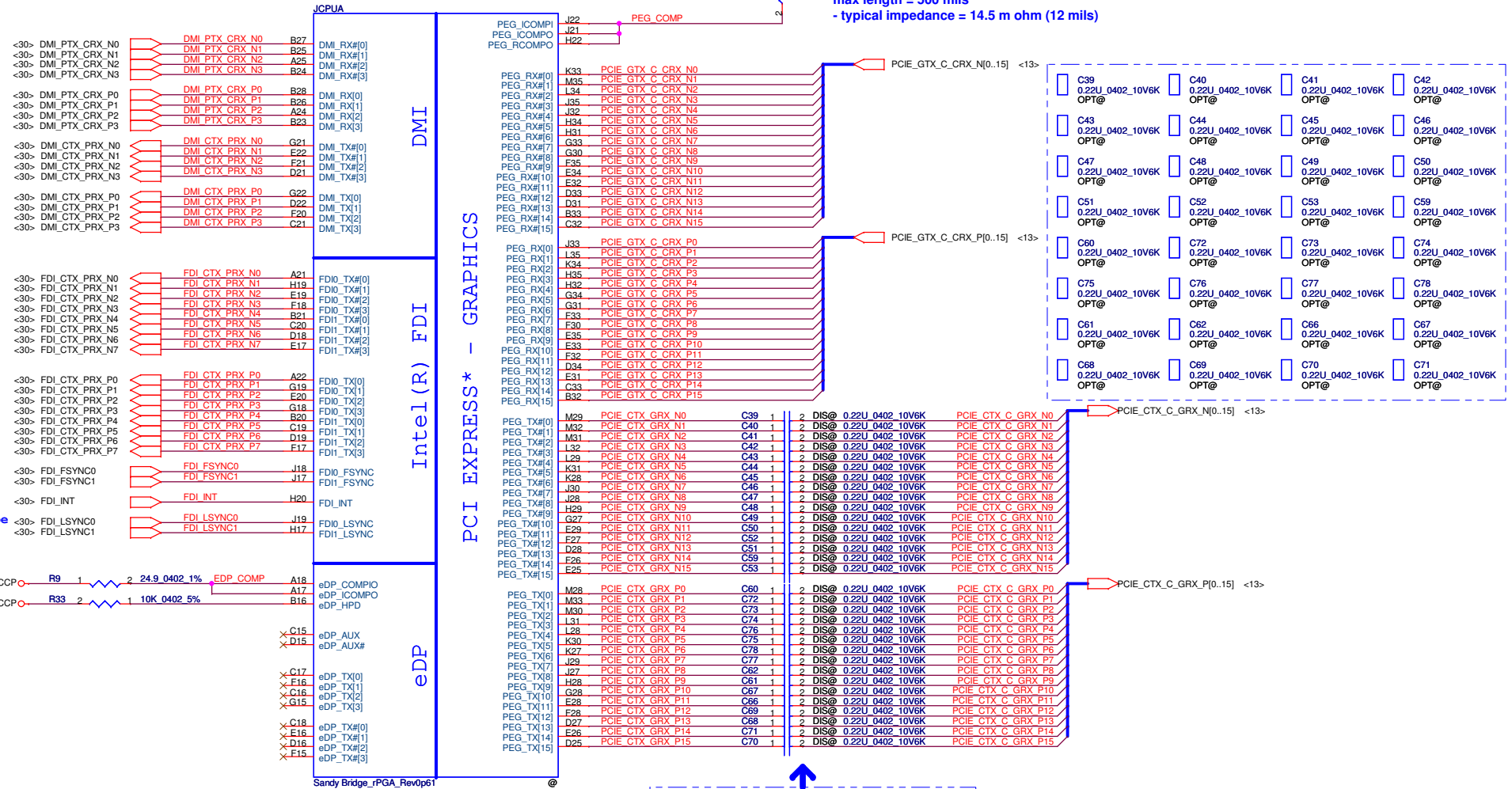


FAN Control Circuit



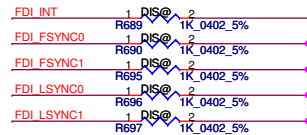
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PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)



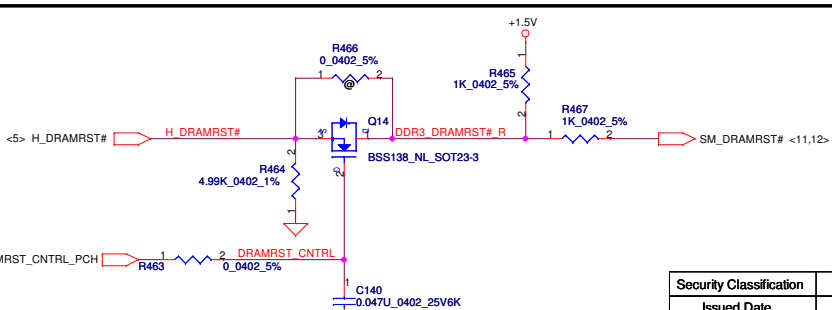
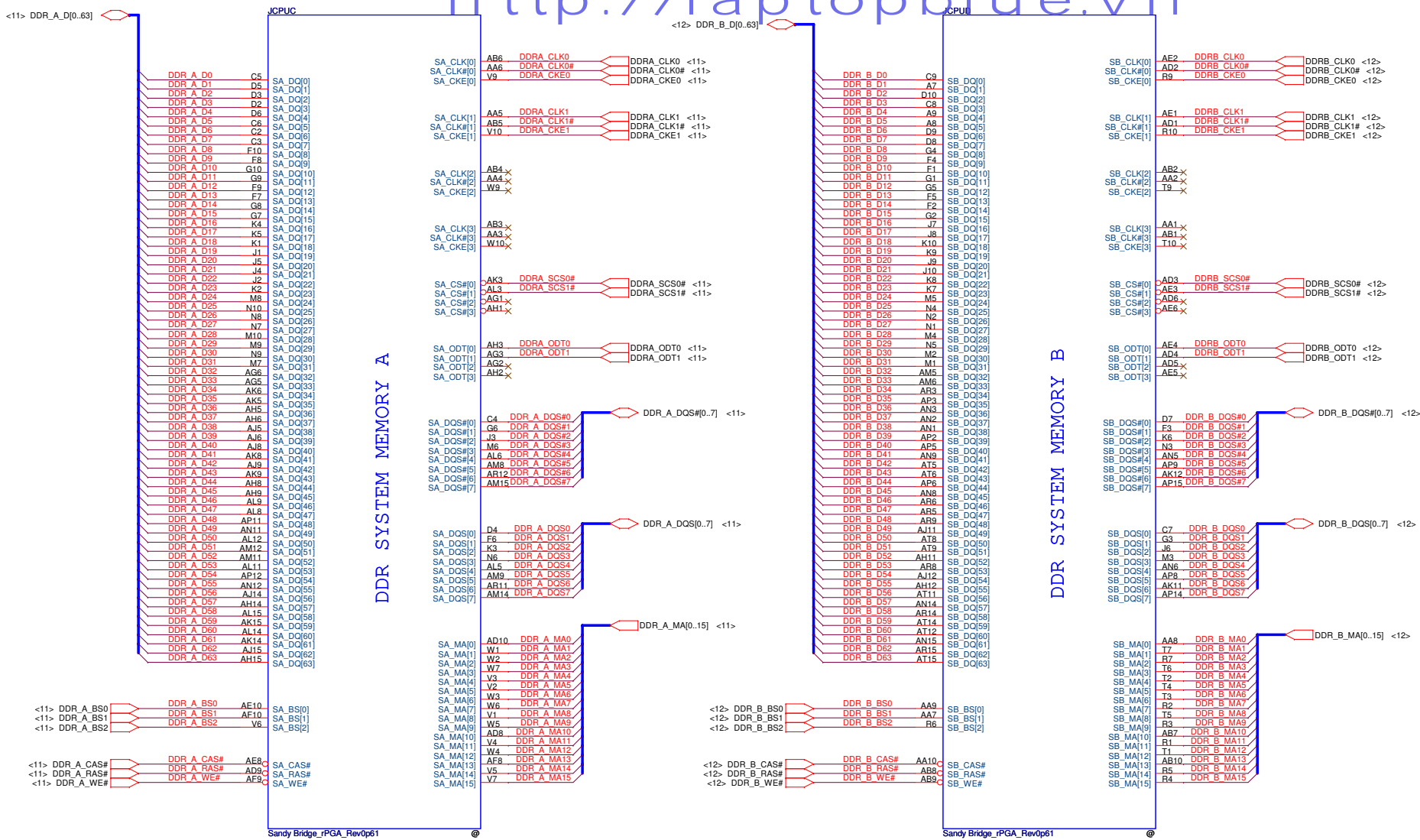
eDP_COMP signals should be shorted near balls and routed with typical impedance <25m ohm

Close to CPU

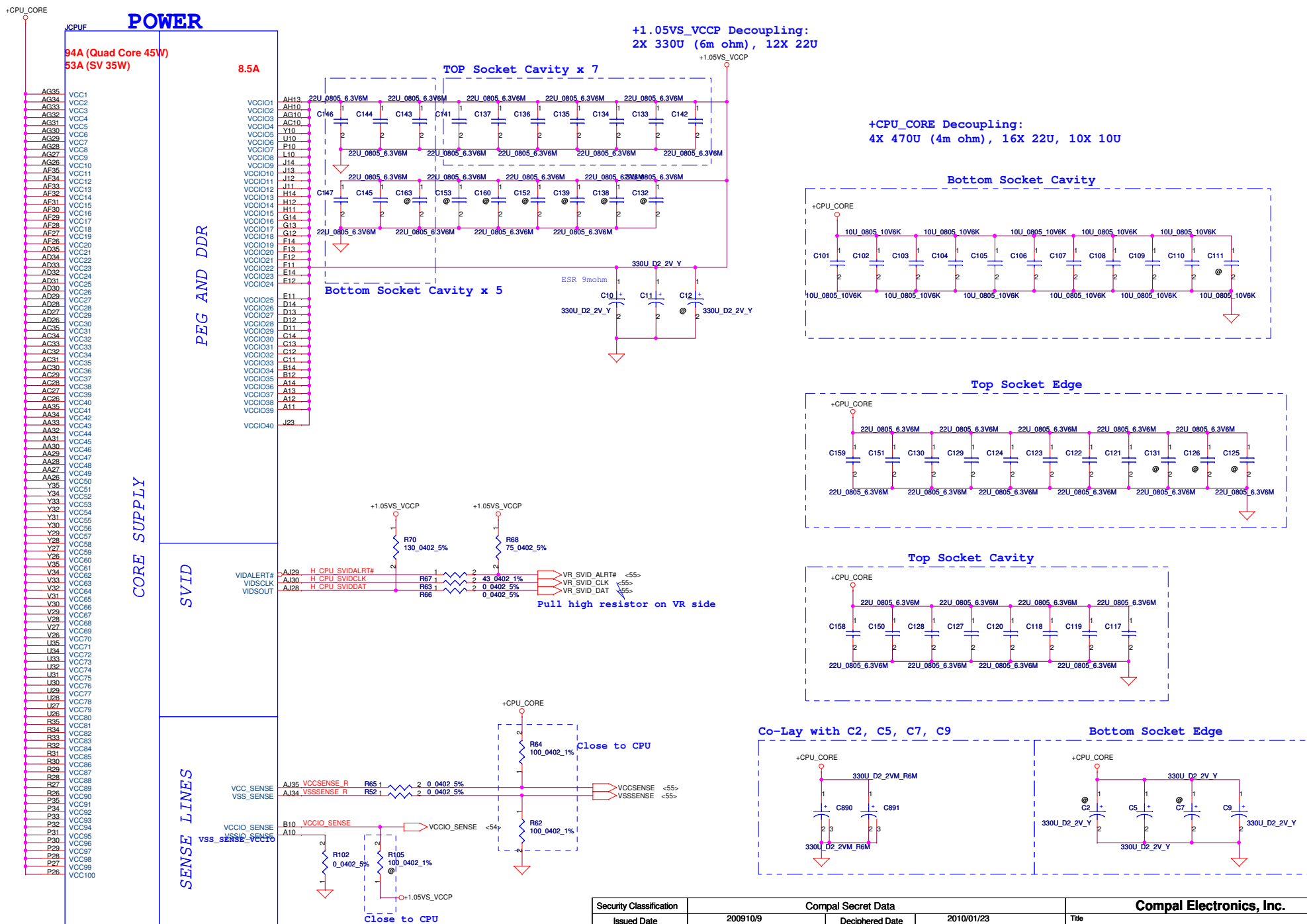


Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

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Flow		0.1			



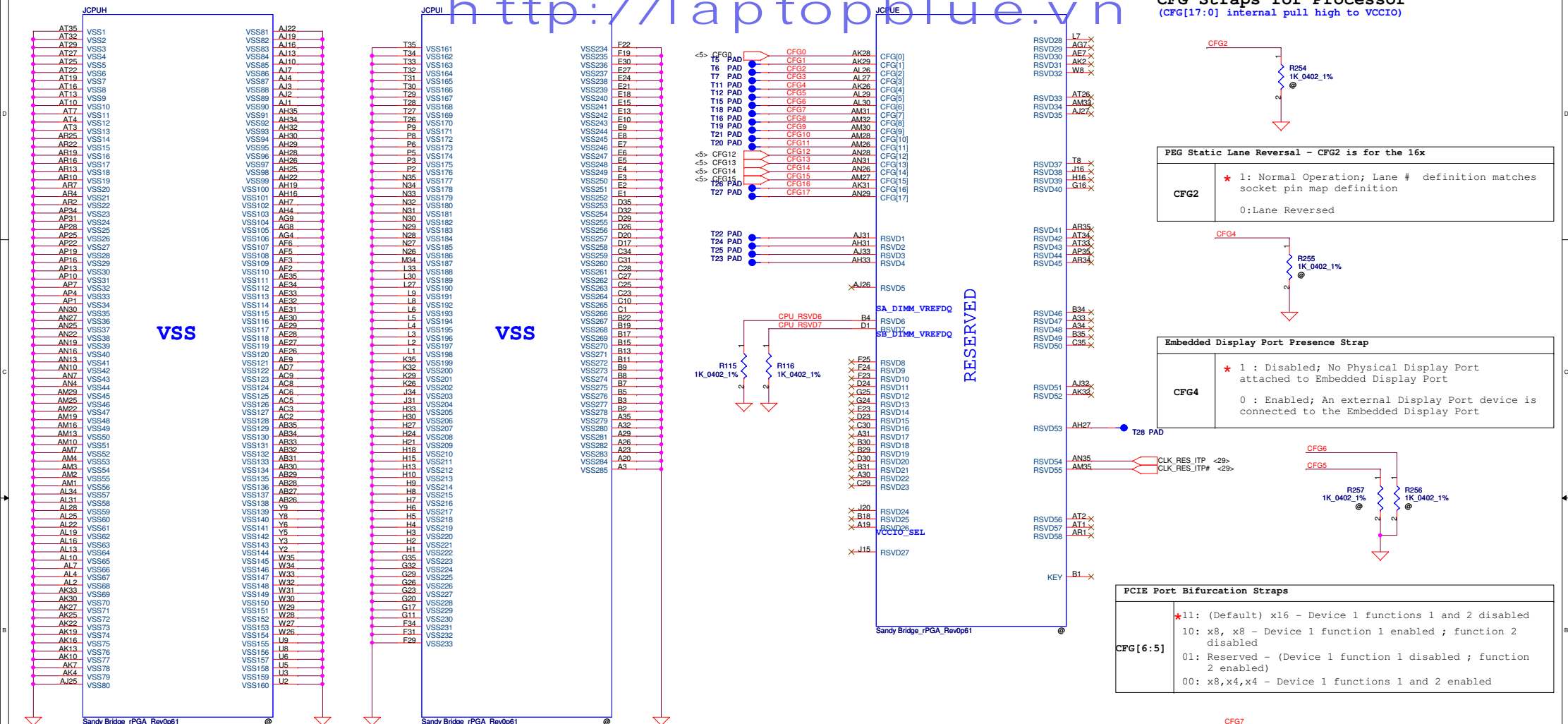
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MISC

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CFG Straps for Processor

(CFG[17:0] internal pull high to VCCIO)



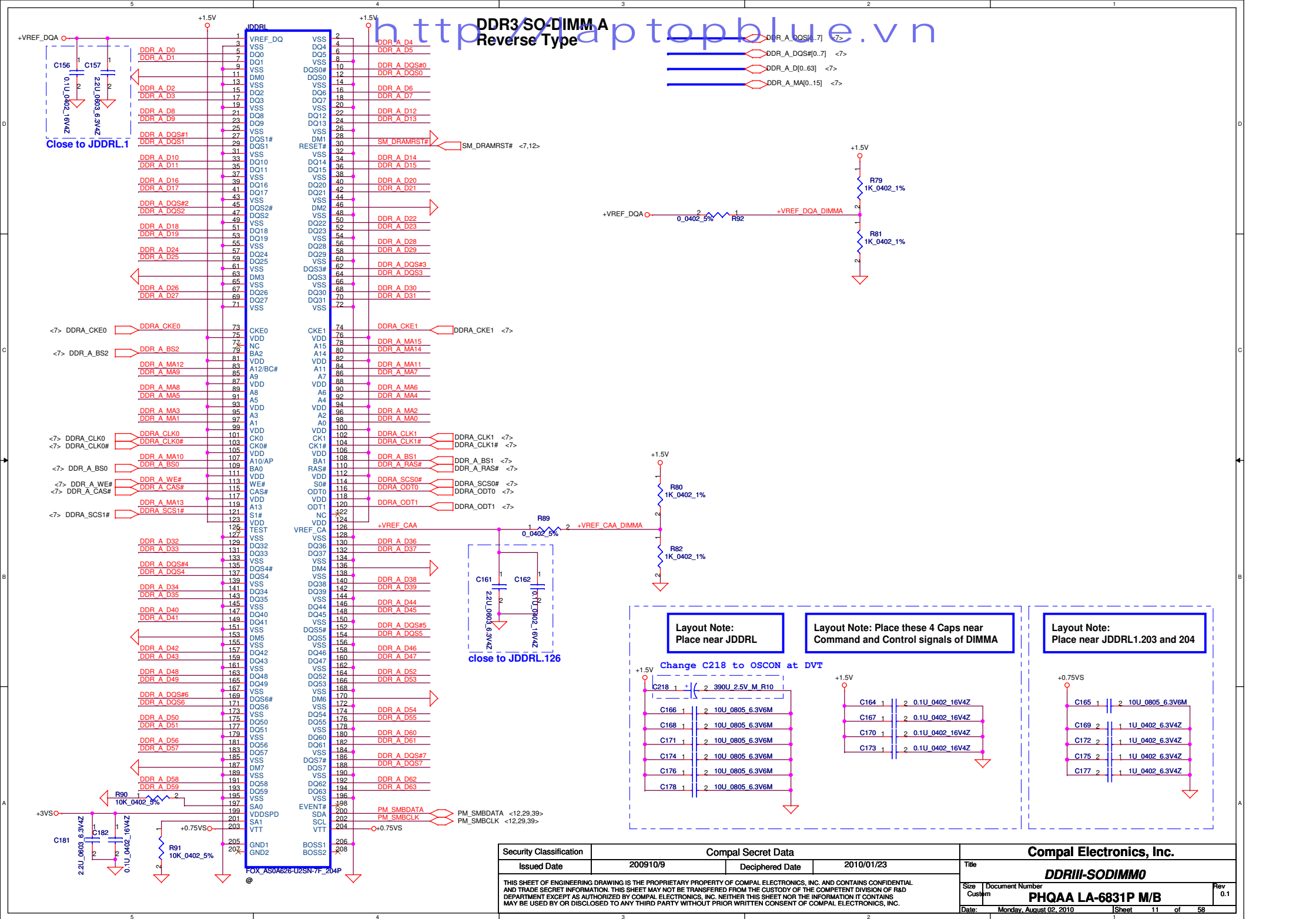
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	★ 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

Embedded Display Port Presence Strap	
CFG4	★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

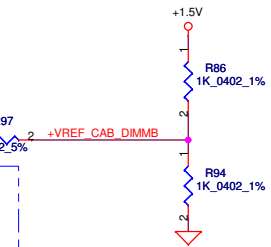
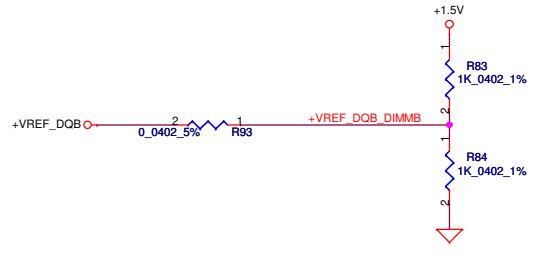
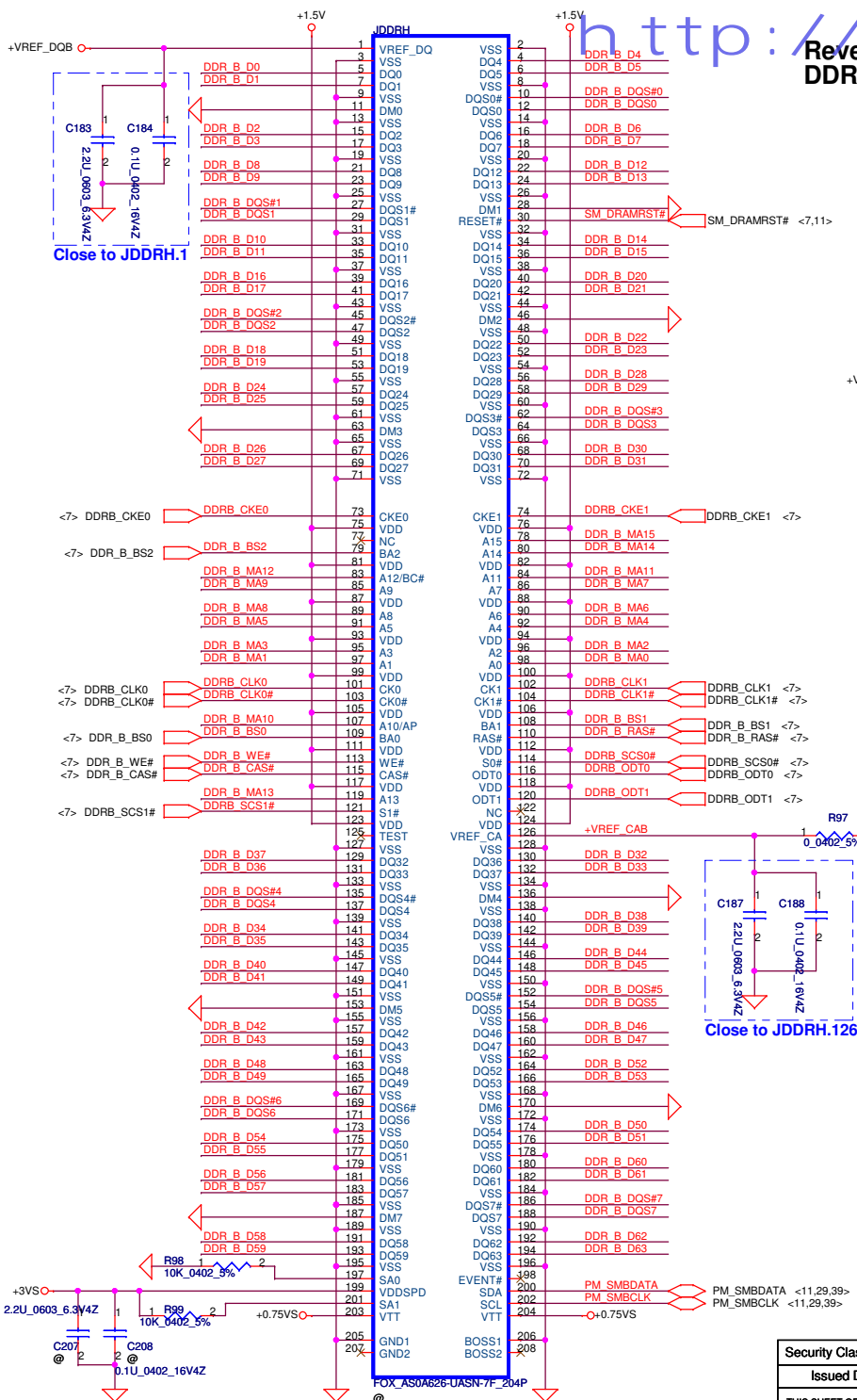
PCIe Port Bifurcation Straps	
CFG[6:5]	★ 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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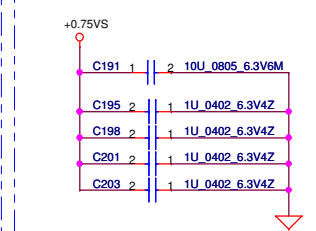
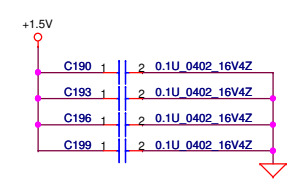
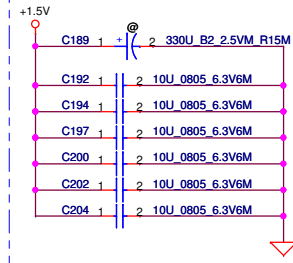
Reverse Type
DDR3 SO-DIMM B



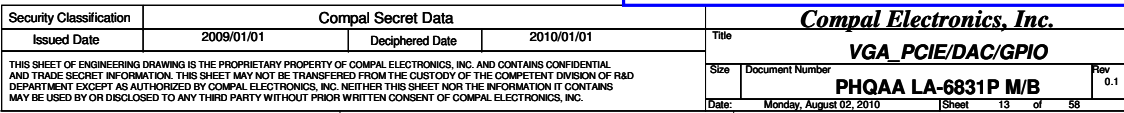
Layout Note:
Place near JDDR.H

Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB

Layout Note:
Place near JDDR.H.203 and 204



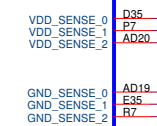
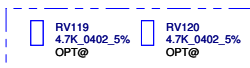
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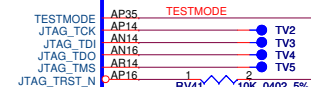
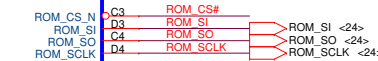


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eDP    <25> VGA_eDP_AUX
       <25> VGA_eDP_AUX-

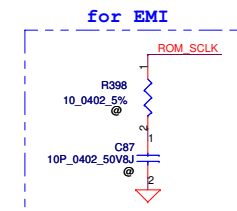
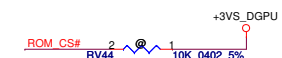
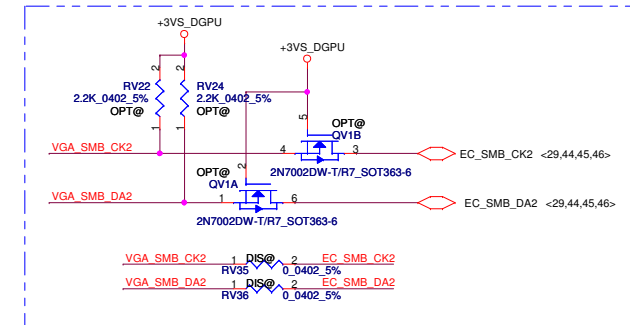
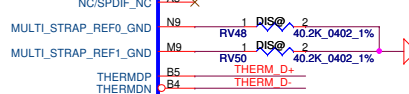
HDMI   <27> VGA_HDMI_CLK
       <27> VGA_HDMI_DAT.
```



TEST

**SERIAL**

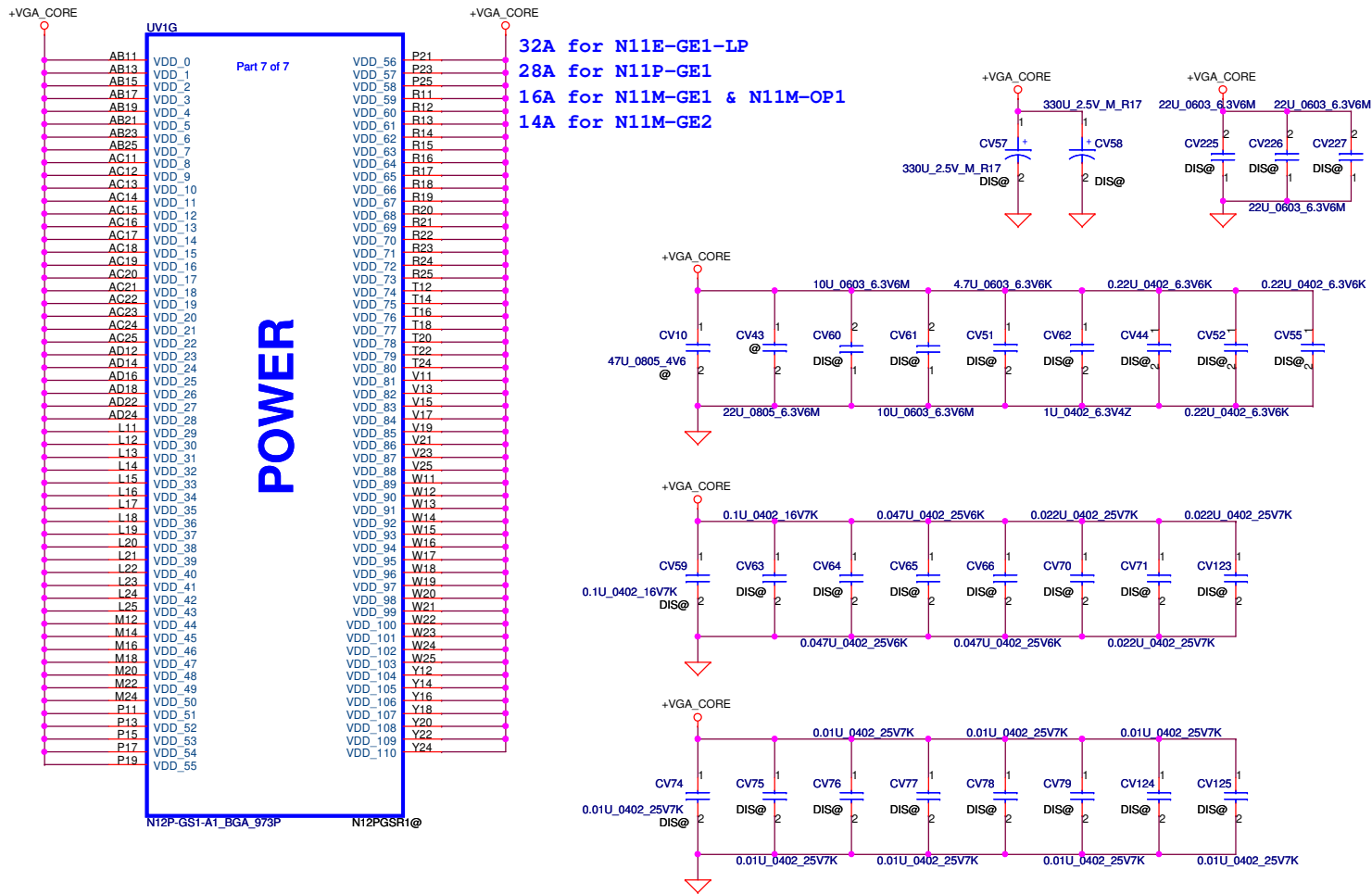
GENERAL



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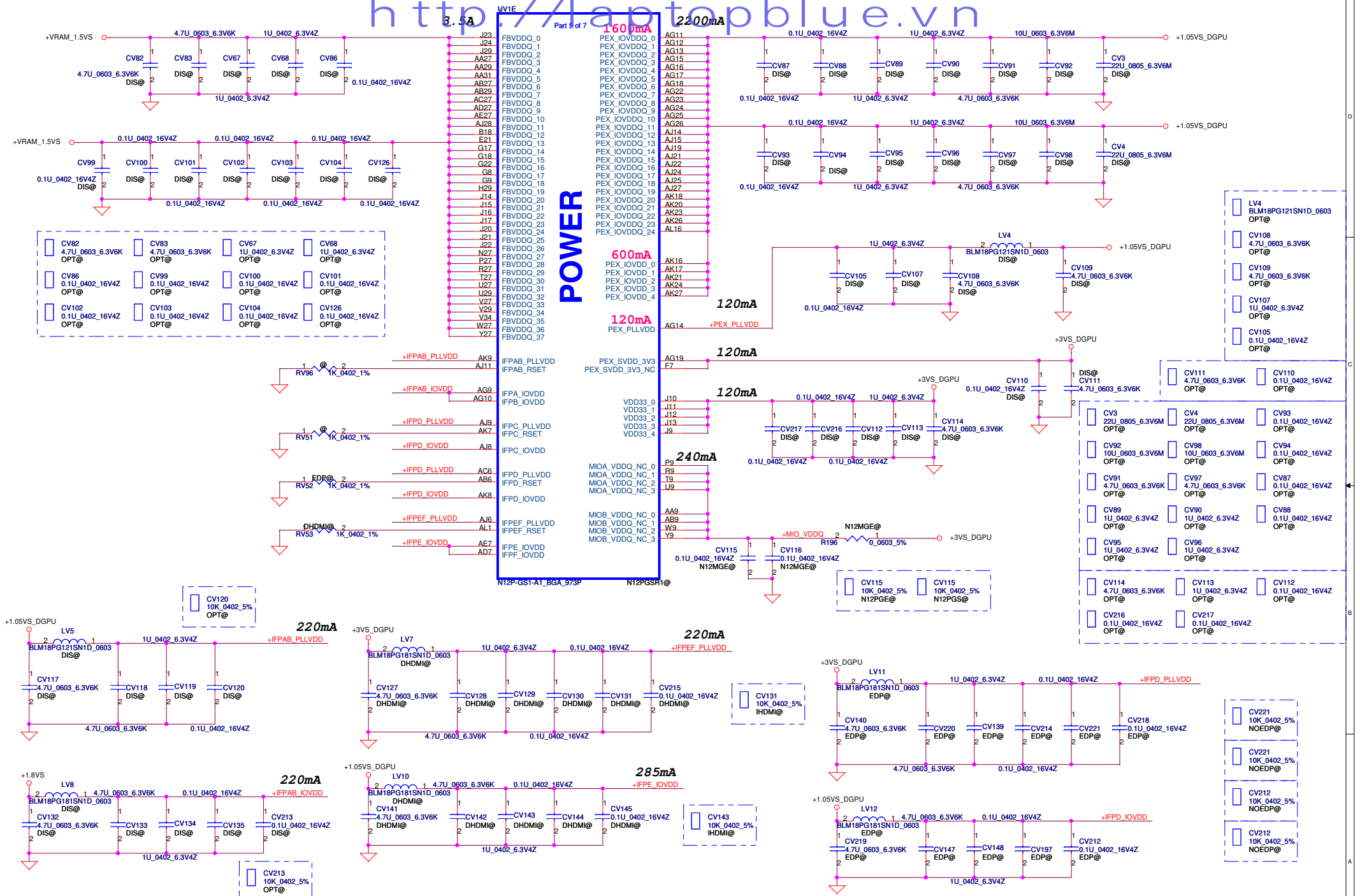
N12M-GE Performance Mode				N12P-GS Performance Mode			
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE	Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	606	790	1.00 V	P0	TBD	TBD	TBD
P8	TBD	TBD	TBD	P8	TBD	TBD	TBD
P12	TBD	TBD	TBD	P12	TBD	TBD	TBD

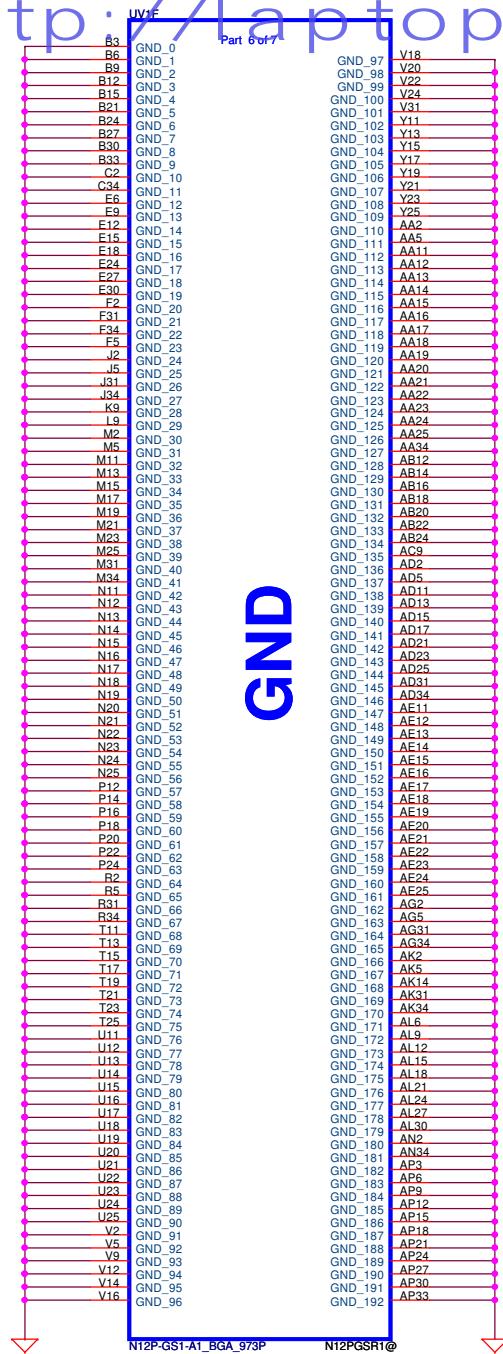
N12P-GE Performance Mode			
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD



CV225 22U_0603_6.3V6M OPT@	CV227 22U_0603_6.3V6M OPT@
CV226 22U_0603_6.3V6M OPT@	CV228 22U_0603_6.3V6M OPT@
CV57 330U_2.5V_M_R17 OPT@	CV58 330U_2.5V_M_R17 OPT@
CV10 47U_0805_4V6 OPT@	CV43 22U_0603_6.3V6M OPT@
CV60 10U_0603_6.3V6M OPT@	CV61 10U_0603_6.3V6M OPT@
CV51 47U_0603_6.3V6K OPT@	CV62 1U_0402_6.3V4Z OPT@
CV44 0.22U_0402_6.3V6K OPT@	CV52 0.22U_0402_6.3V6K OPT@
CV55 0.22U_0402_6.3V6K OPT@	CV59 0.1U_0402_16V7K OPT@
CV63 0.1U_0402_16V7K OPT@	CV64 0.047U_0402_25V6K OPT@
CV85 0.047U_0402_25V6K OPT@	CV66 0.047U_0402_25V6K OPT@
CV70 0.022U_0402_25V7K OPT@	CV71 0.022U_0402_25V7K OPT@
CV123 0.022U_0402_25V7K OPT@	CV74 0.01U_0402_25V7K OPT@
CV75 0.01U_0402_25V7K OPT@	CV76 0.01U_0402_25V7K OPT@
CV77 0.01U_0402_25V7K OPT@	CV78 0.01U_0402_25V7K OPT@
CV79 0.01U_0402_25V7K OPT@	CV124 0.01U_0402_25V7K OPT@
CV125 0.01U_0402_25V7K OPT@	

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						Size		Document Number		Rev	
						PHQAA LA-6831P M/B		0.1			
						Date:		Monday, August 02, 2010		Sheet 15 of 58	
3				2		1					

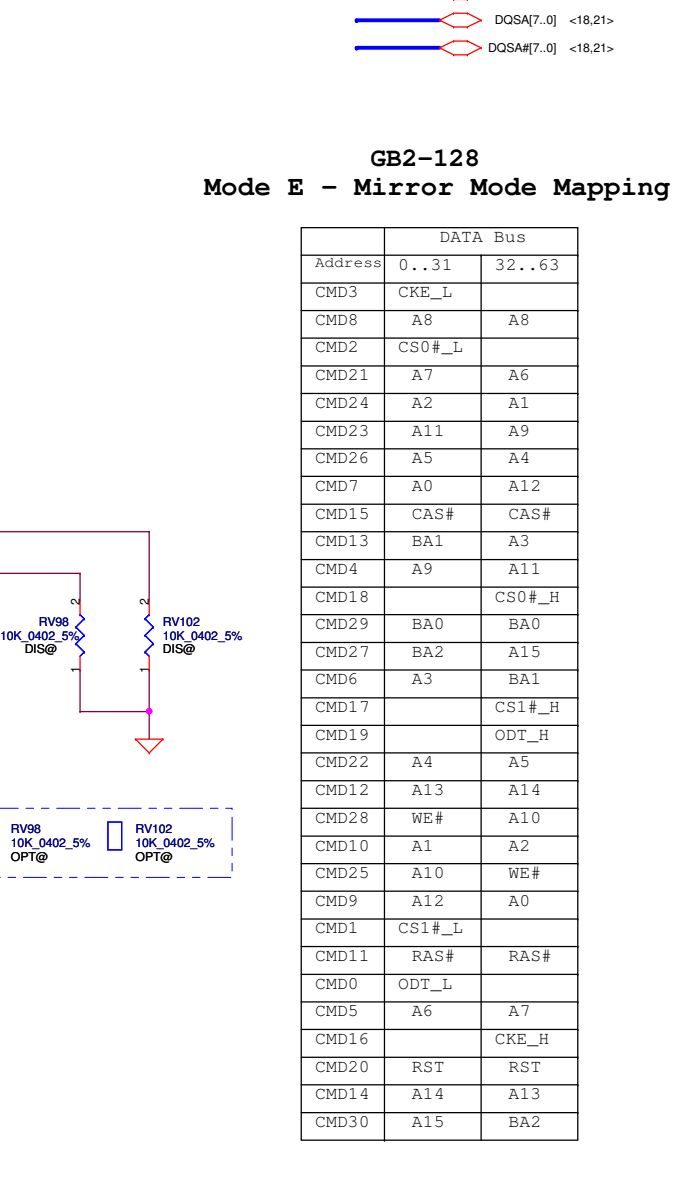
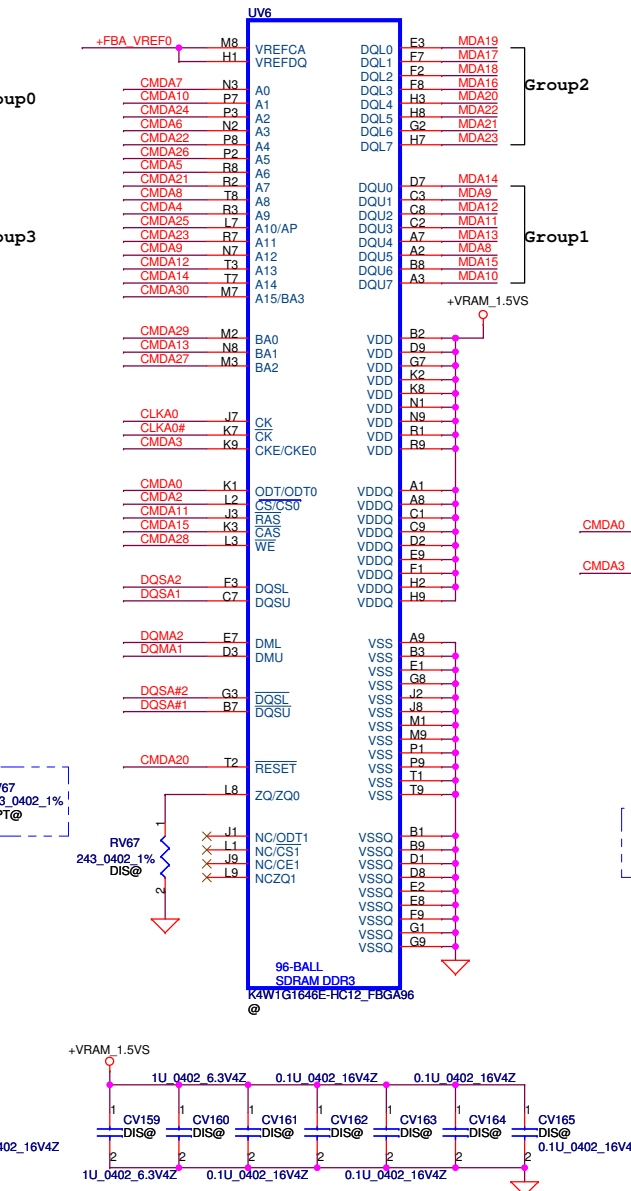
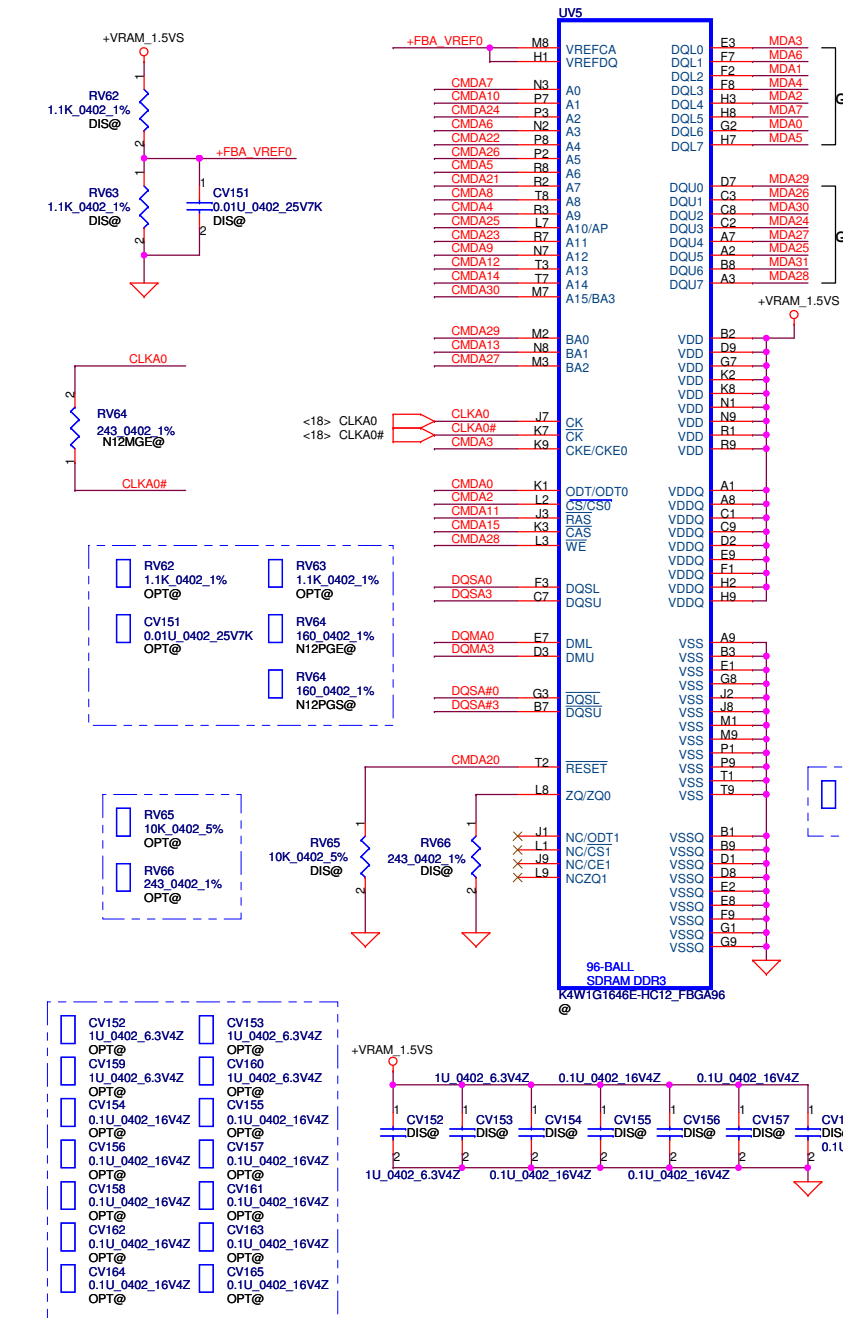




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				PHQAA LA-6831P M/B	
				Date:	Monday, August 02, 2010
				Sheet	17 of 58

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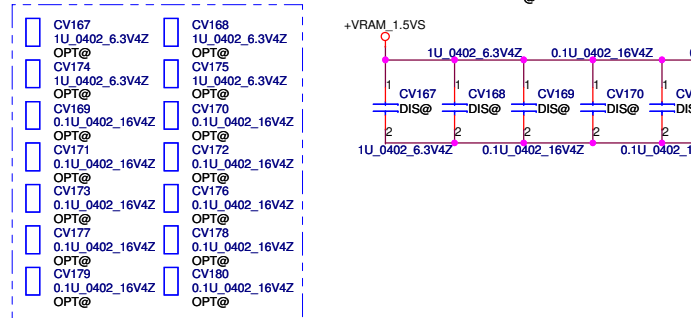
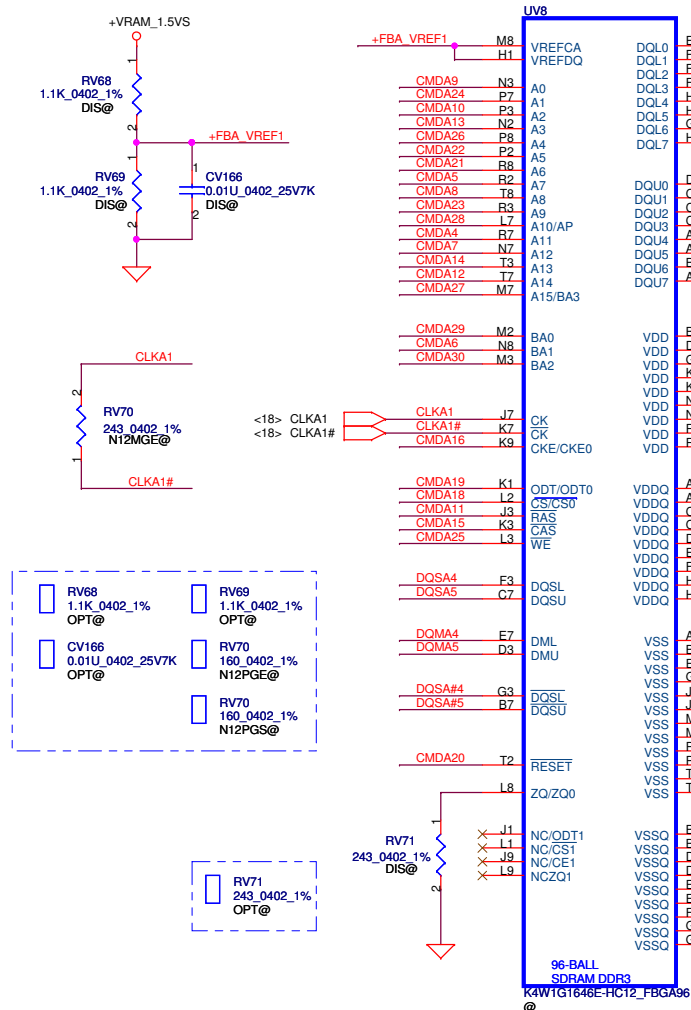
Memory Partition A - Lower 32 bits



GB2-128
Mode E - Mirror Mode Mapping

DATA Bus	
Address	0..31 32..63
CMD3	CKE_L
CMD8	A8
CMD2	CS0#_L
CMD21	A7
CMD24	A2
CMD23	A11
CMD26	A5
CMD7	A0
CMD15	CAS#
CMD13	BA1
CMD4	A9
CMD18	CS0#_H
CMD29	BA0
CMD27	BA2
CMD6	A3
CMD17	CS1#_H
CMD19	ODT_H
CMD22	A4
CMD12	A13
CMD28	WE#
CMD10	A1
CMD25	A10
CMD9	A12
CMD1	CS1#_L
CMD11	RAS#
CMD0	ODT_L
CMD5	A6
CMD16	CKE_H
CMD20	RST
CMD14	A14
CMD30	A15

Memory Partition A - Upper 32:bits



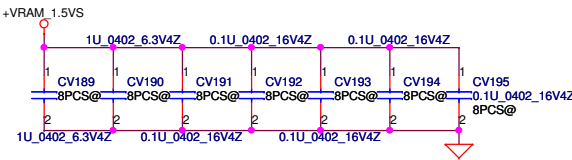
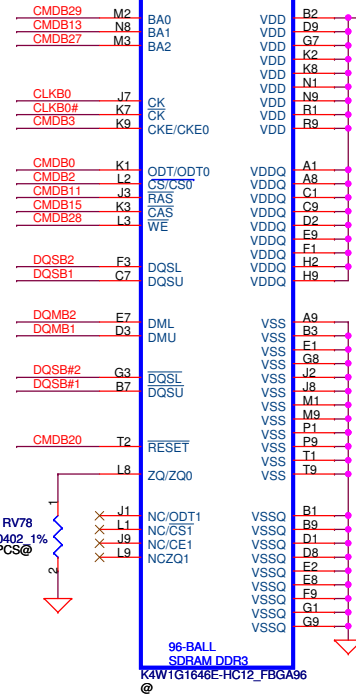
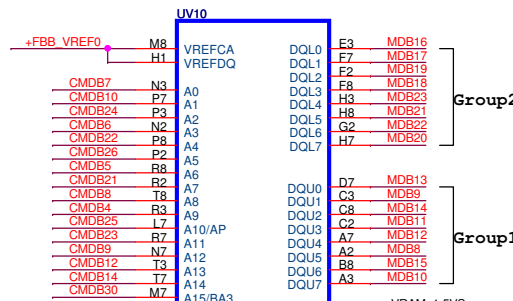
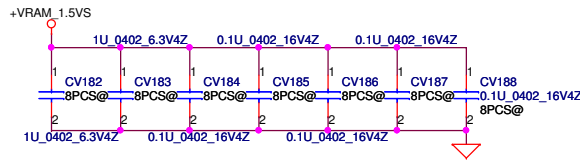
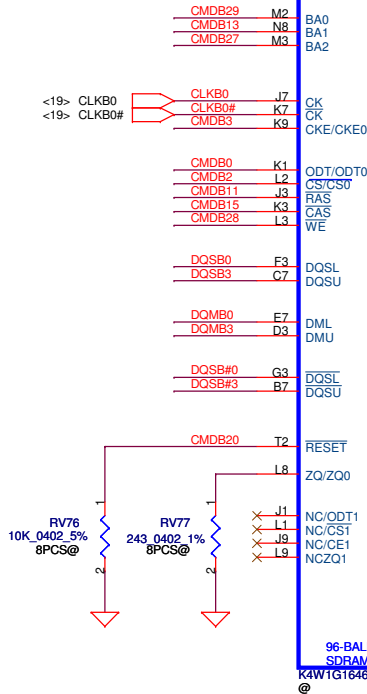
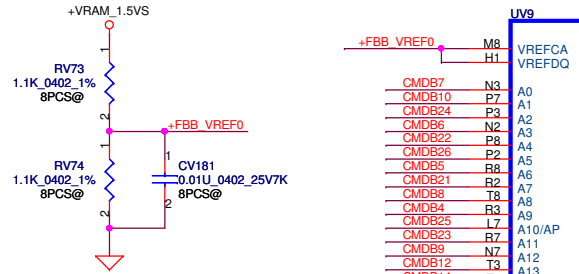
GB2-128 Mode E - Mirror Mode Mapping

Address		DATA Bus	
0..31		32..63	
CMD3	CKE_L		
CMD8	A8	A8	
CMD2	CS0#_L		
CMD21	A7	A6	
CMD24	A2	A1	
CMD23	A11	A9	
CMD26	A5	A4	
CMD7	A0	A12	
CMD15	CAS#	CAS#	
CMD13	BA1	A3	
CMD4	A9	A11	
CMD18		CS0#_H	
CMD29	BA0	BA0	
CMD27	BA2	A15	
CMD6	A3	BA1	
CMD17		CS1#_H	
CMD19		ODT_H	
CMD22	A4	A5	
CMD12	A13	A14	
CMD28	WE#	A10	
CMD10	A1	A2	
CMD25	A10	WE#	
CMD9	A12	A0	
CMD1	CS1#_L		
CMD11	RAS#	RAS#	
CMD0	ODT_L		
CMD5	A6	A7	
CMD16		CKE_H	
CMD20	RST	RST	
CMD14	A14	A13	
CMD30	A15	BA2	

Security Classification		Compal Secret Data		Title	
Issued Date	2009/01/01	Deciphered Date	2010/01/01	VGA_VRAM_A Upper	
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				PHQAA LA-6831P M/B	
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Memory Partition C - Lower 32 bits

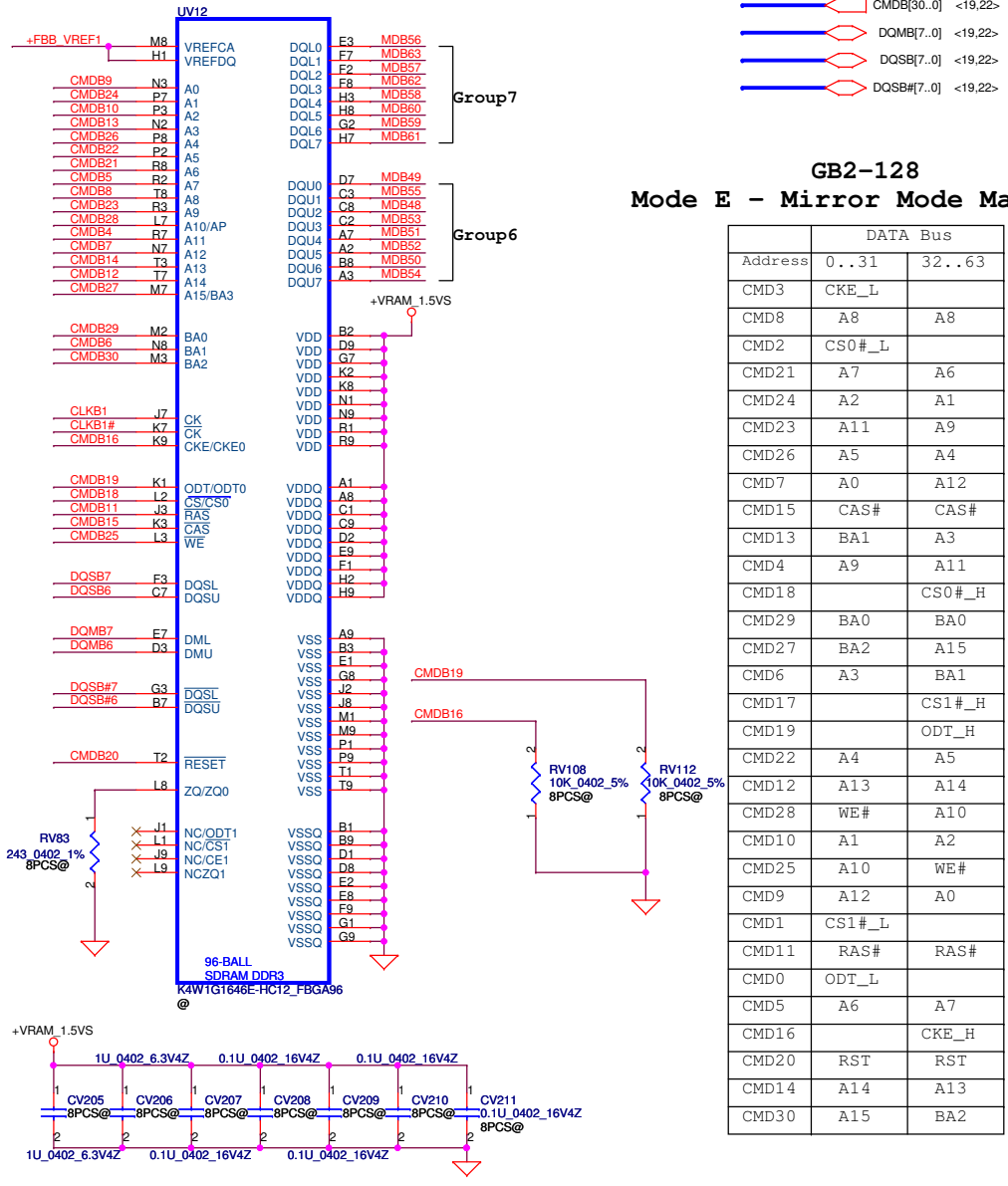
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GB2-128 Mode E - Mirror Mode Mapping

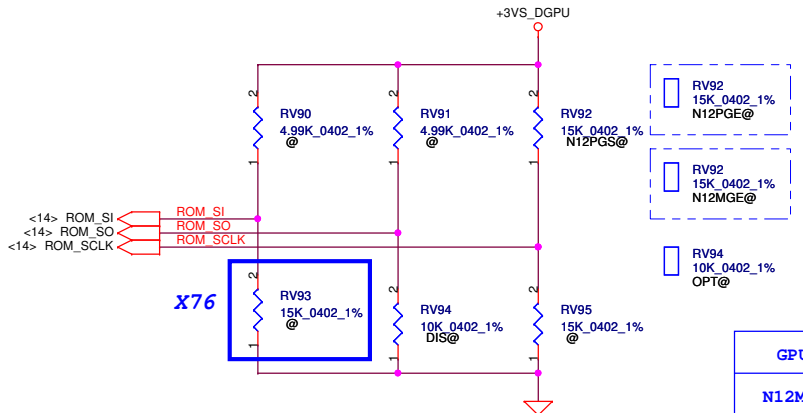
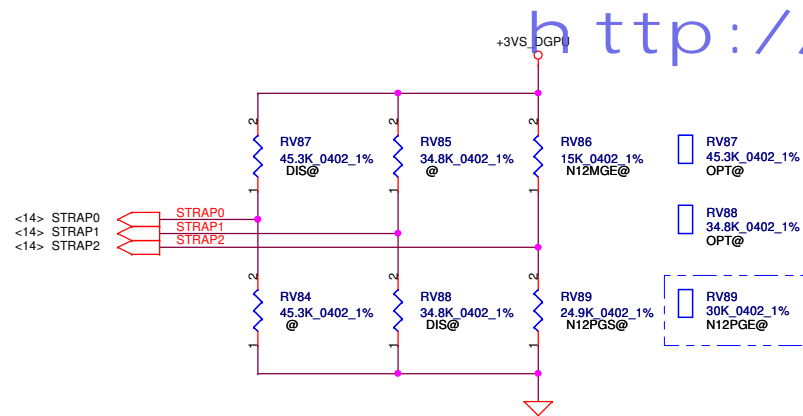
DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Inner 32 bits



	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2009/01/01	Deciphered Date	2010/01/01	VGA_VRAM_C Upper			
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Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SCLK	STRAP2
N12M-GE	0x0A7A	Pull up 15K	Pull up 15K
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GE	0x0DF5	Pull up 15K	Pull down 30K

Hynix H5TQ1G63BFR-12C SA000032400	512M	0010	PD 15K
	1G	0010	PD 15K
Samsung K4W1G1646E-HC12 SA000035700	512M	0011	PD 20K
	1G	0011	PD 20K

SD034150280

SD034200280

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User [3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

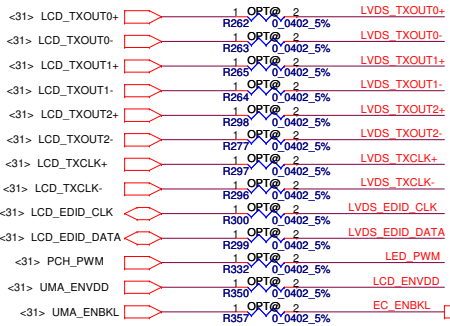
SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

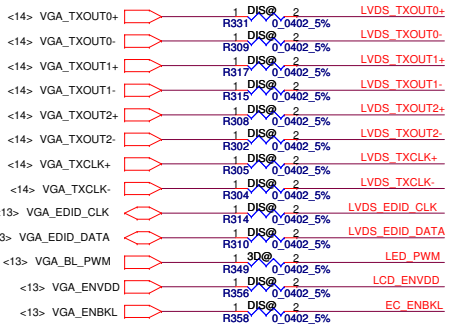
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				Date	Monday, August 02, 2010
				Sheet	24 of 58

OPTIMUS



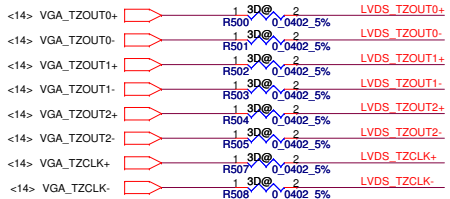
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DISCRETE



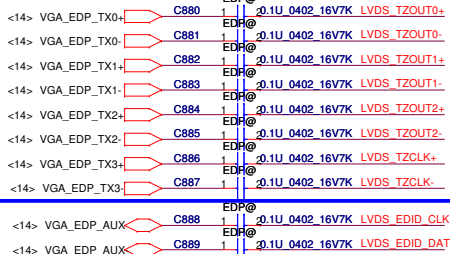
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DISCRETE for Full-HD and 3D LVDS Panel



Close to LVDS1 Connector

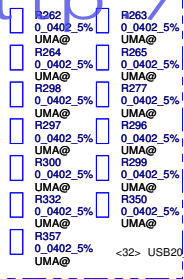
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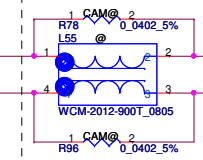
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Close to LVDS Connector

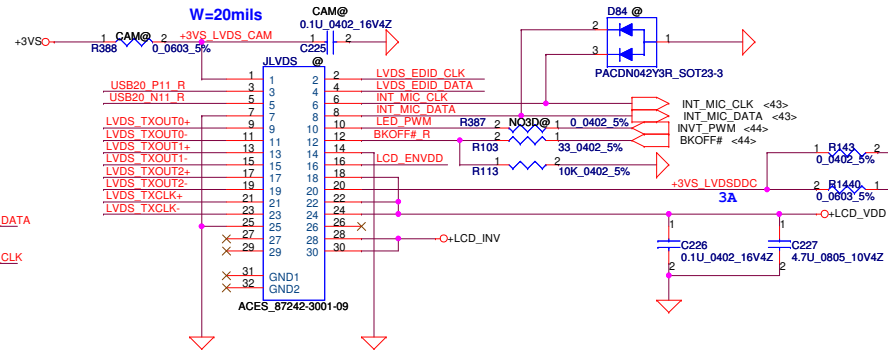
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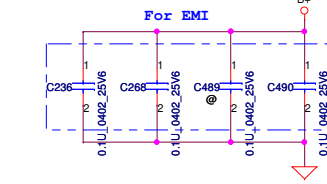
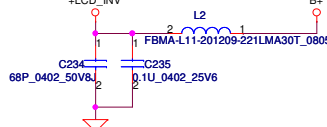
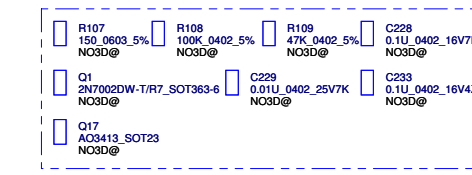
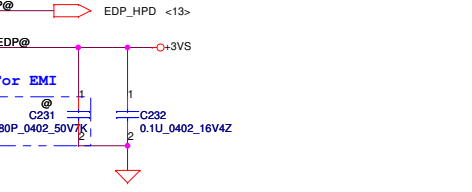
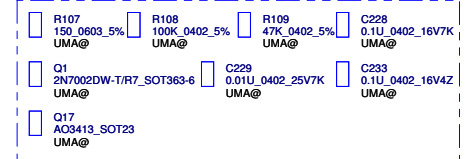
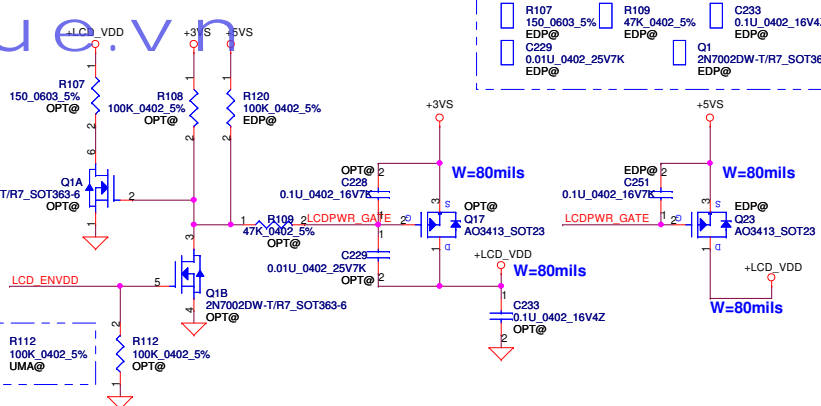
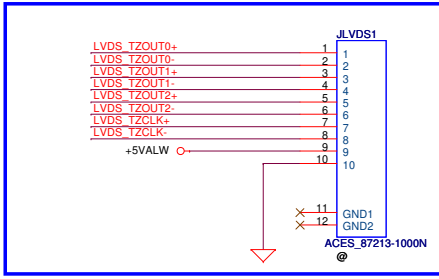
Reserve for EMI request



LCD/PANEL BD. Conn.

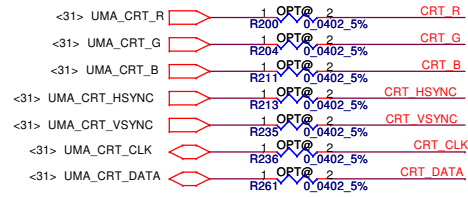


For 3D Panel

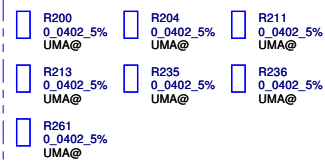


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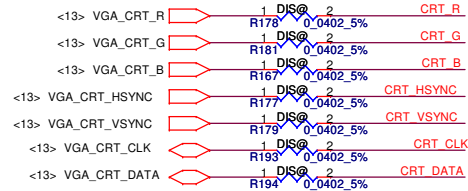
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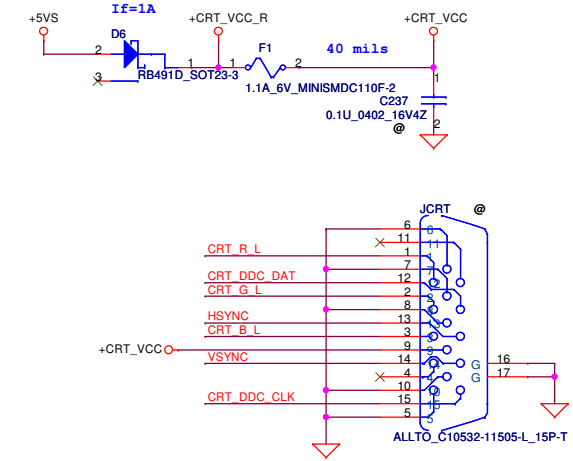
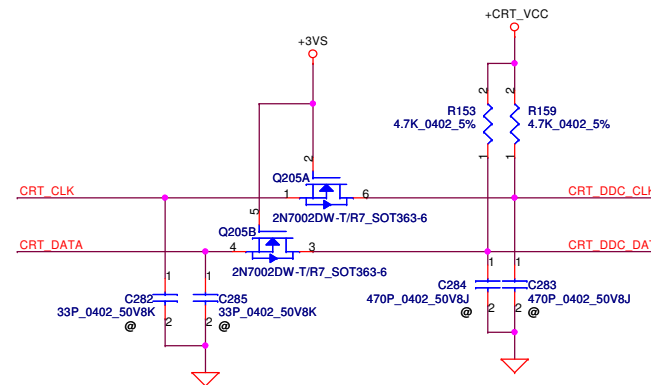
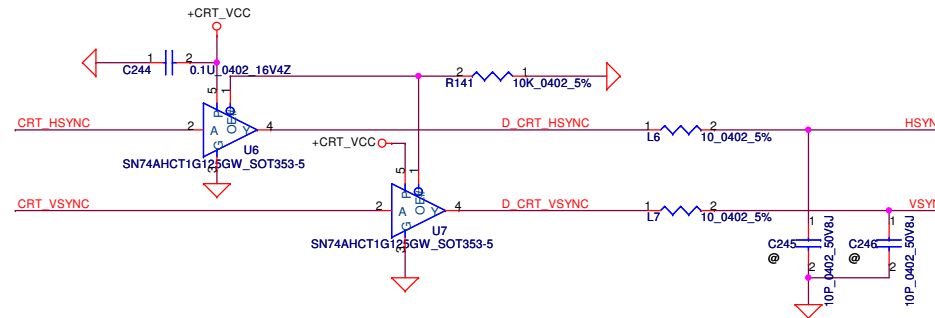
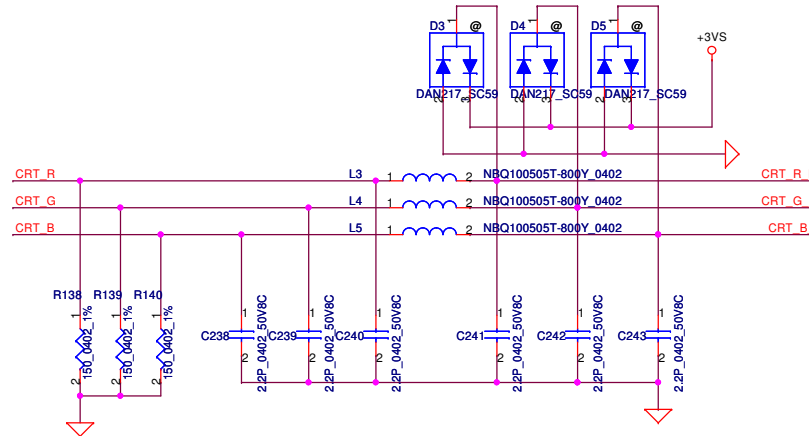
Close to CRT Connector



DISCRETE

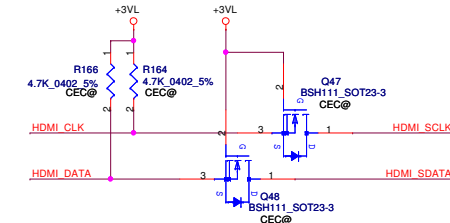
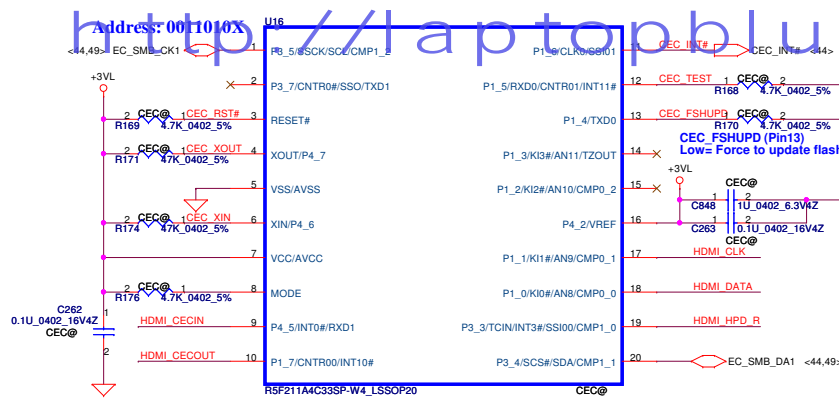
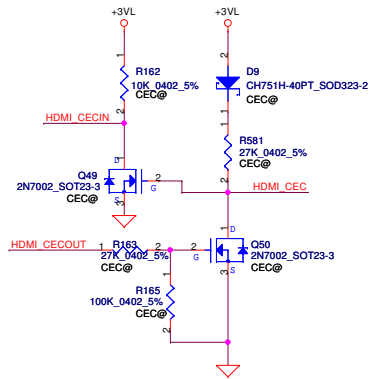


Close to CRT Connector

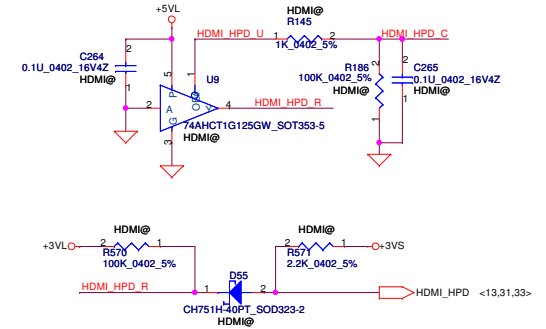
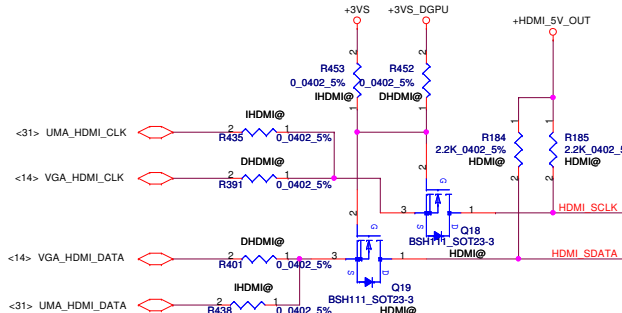
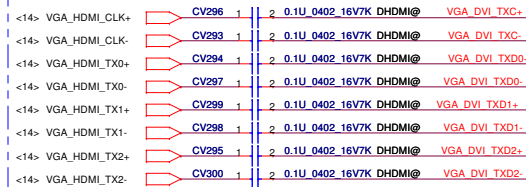


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Issued Date	200910/9	Deciphered Date	2010/01/23	Title	
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Size		Document Number		Rev	
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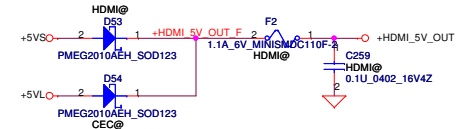
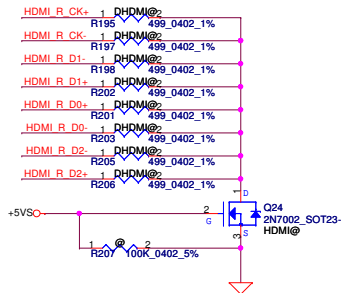
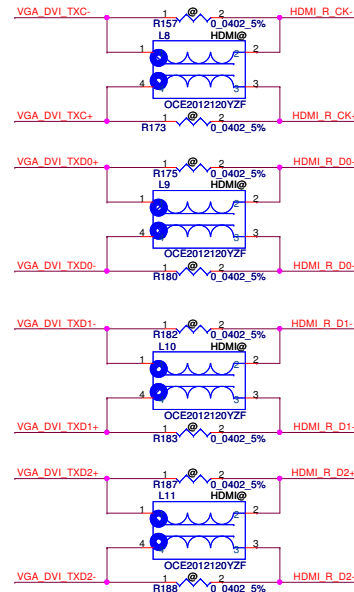
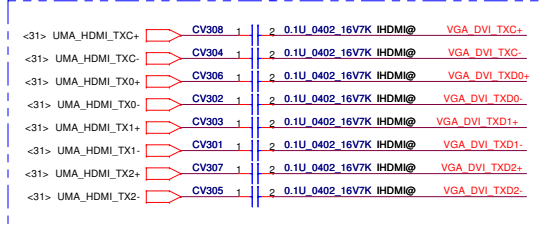
HDMI CEC Controller



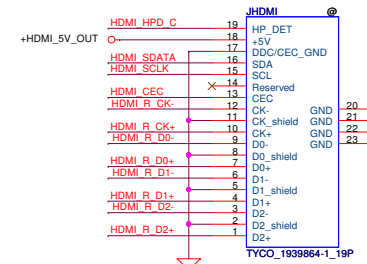
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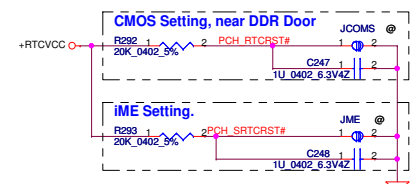
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HDMI Connector

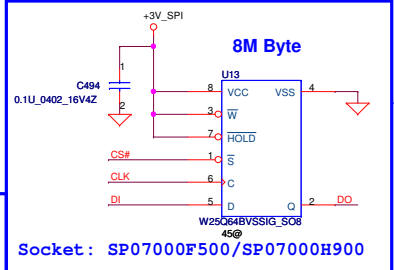
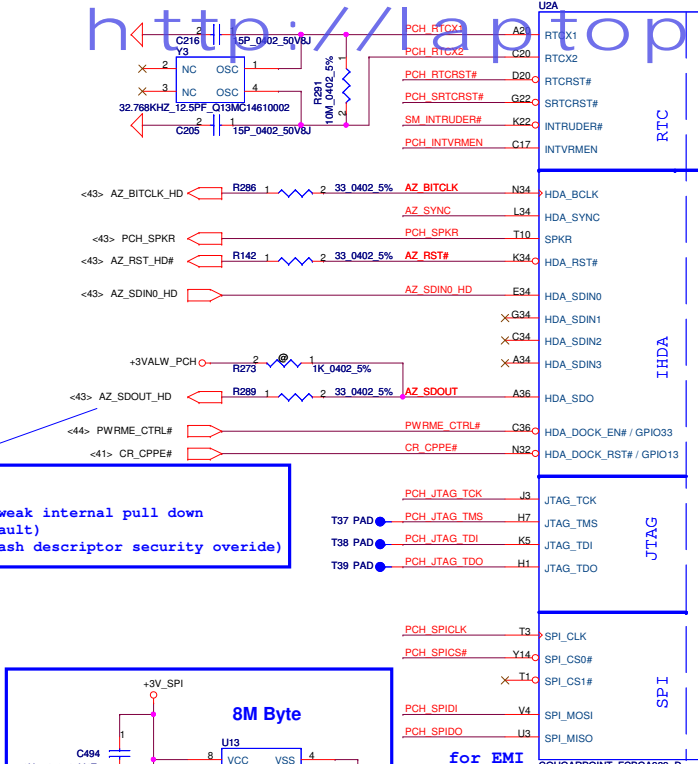
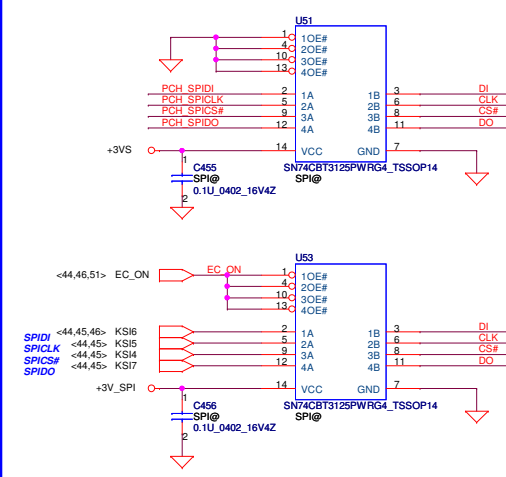
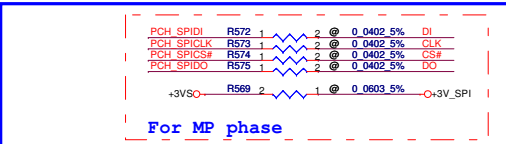
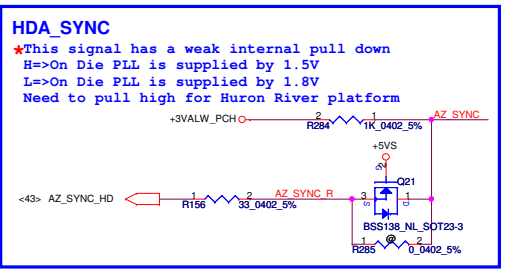
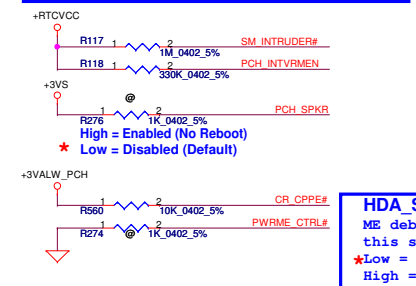


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2009/10/9		2010/01/23		HDMI Conn./CEC	
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		PHQAA LA-6831P M/B		Rev	
		Date: Monday, August 02, 2010		Sheet 27 of 58	

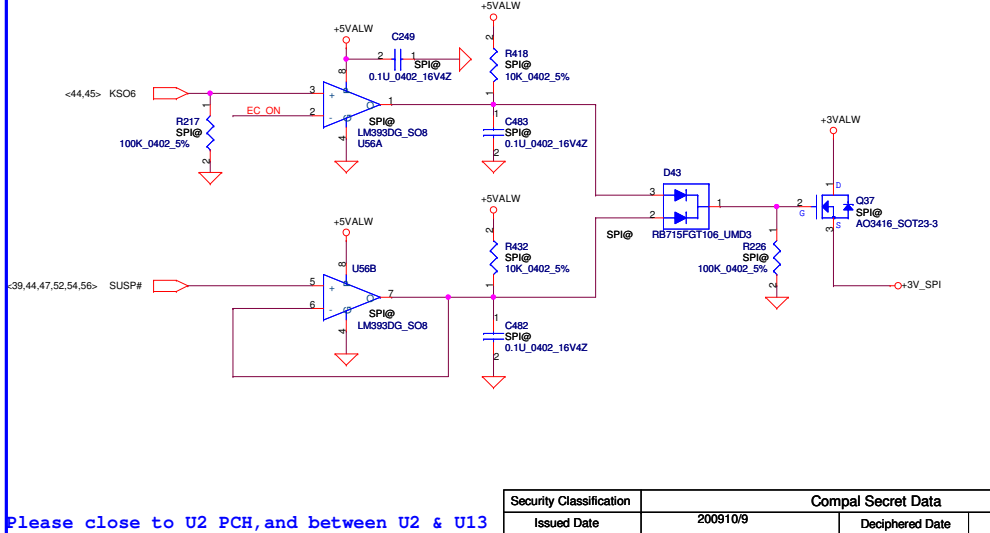


Integrated SUS 1.05V VRM Enable

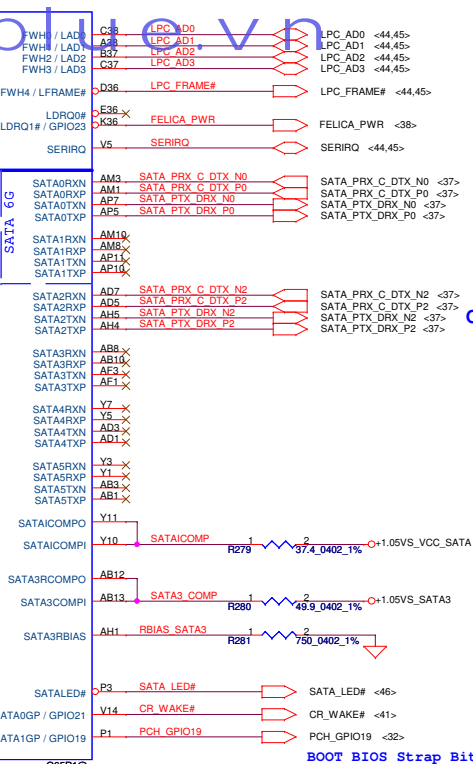
High - Enable Internal VRs
(must be always pulled high)



Please close to U2 PCH



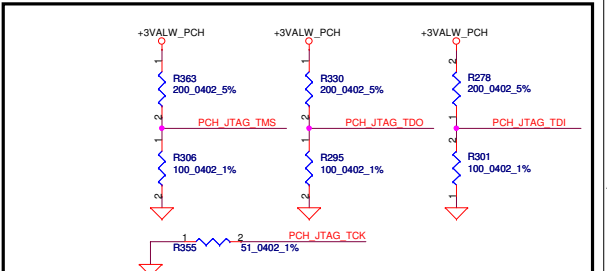
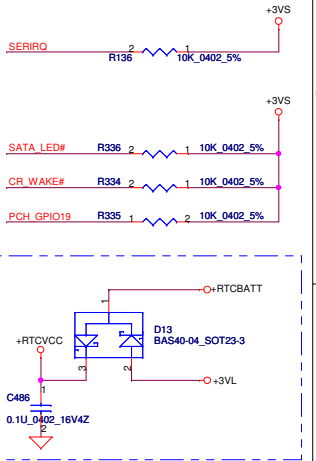
Please close to U2 PCH, and between U2 & U13



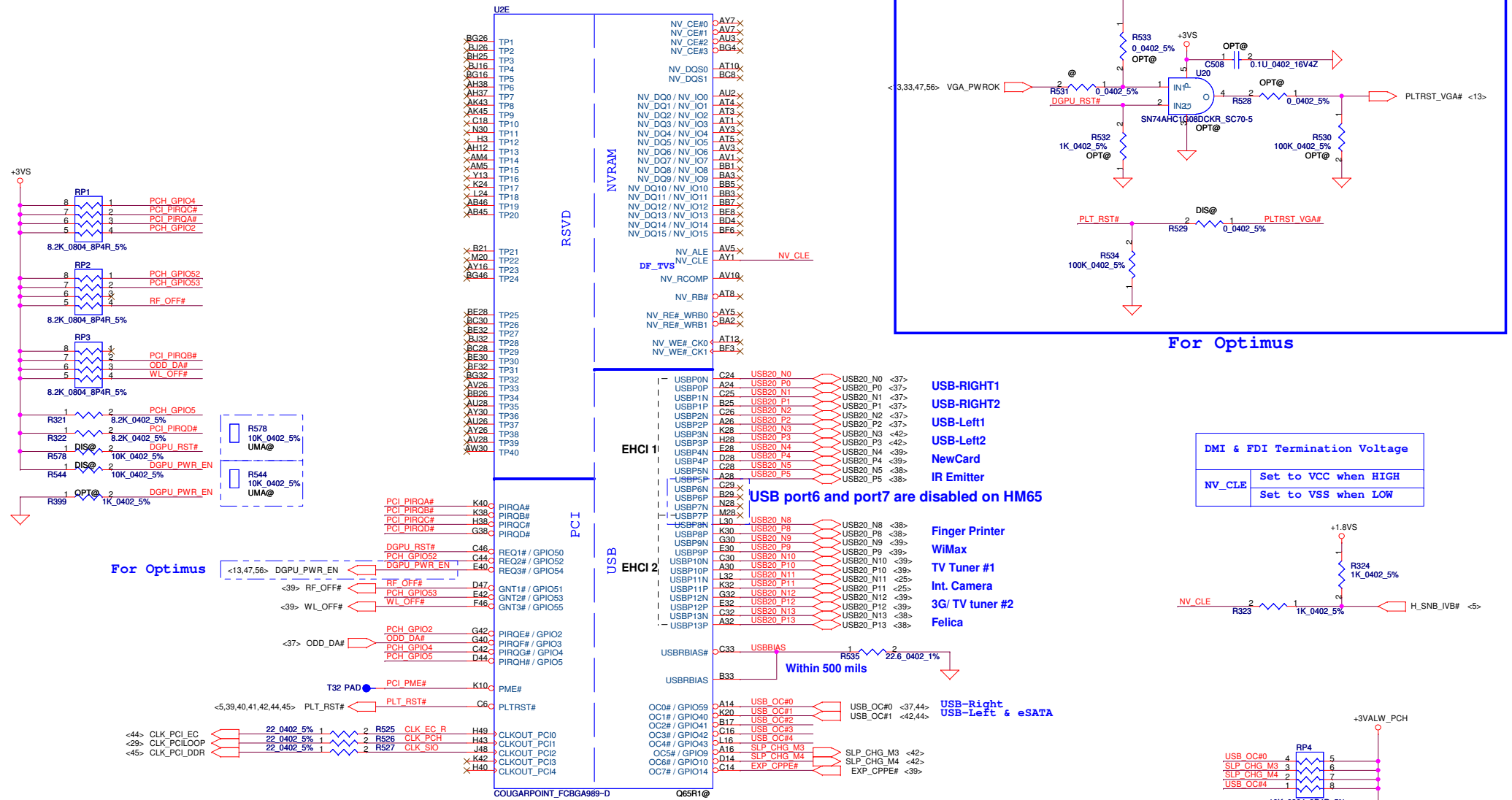
HDD

ODD

BOOT BIOS Strap Bit 0



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Size Custom		Document Number PHQAA LA-6831P M/B	Rev 0.1
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For Optimus

<13,47,56> DGPU_PWR_EN

<39> RF_OFF#

<39> WL_OFF#

<37> ODD_DA#

<5,39,40,41,42,44,45> PLT_RST#

<44> CLK_PCI_EC
<29> CLK_PCI_ODP
<45> CLK_PCI_DDR

Boot BIOS Strap

RF_OFF#	PCH_GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

A16 Swap Override Strap

WL_OFF#	Low= A16 swap override Enable High= A16 swap override Disable
---------	--

Security Classification

Issued Date

200910/9

Compal Secret Data

Deciphered Date

2010/01/23

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PCH_PCI/USB/NAND

Size

Document Number

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0.1

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DMI & FDI Termination Voltage

NV_CLE	Set to VCC when HIGH Set to VSS when LOW
--------	---

USB port6 and port7 are disabled on HM65

Finger Fingerprint

WiMax

TV Tuner #1

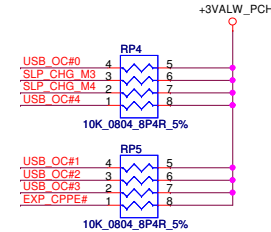
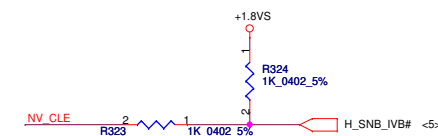
Int. Camera

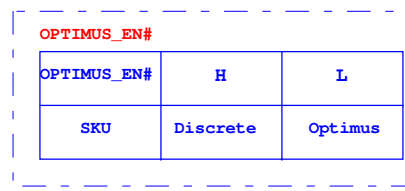
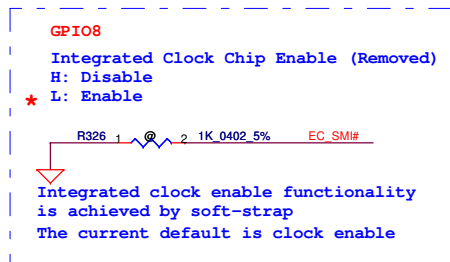
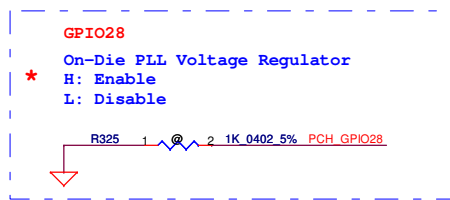
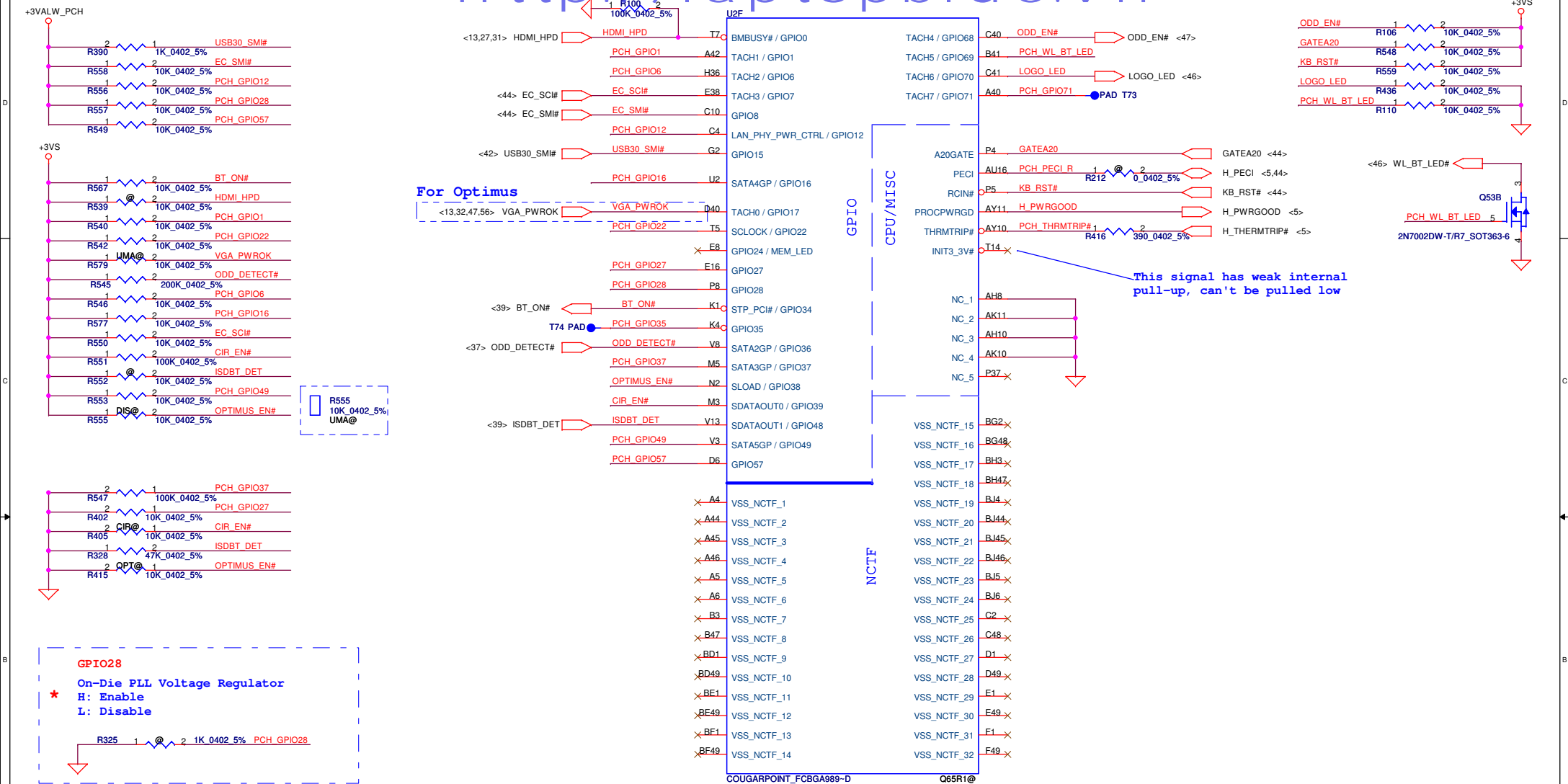
3G/ TV tuner #2

Felica

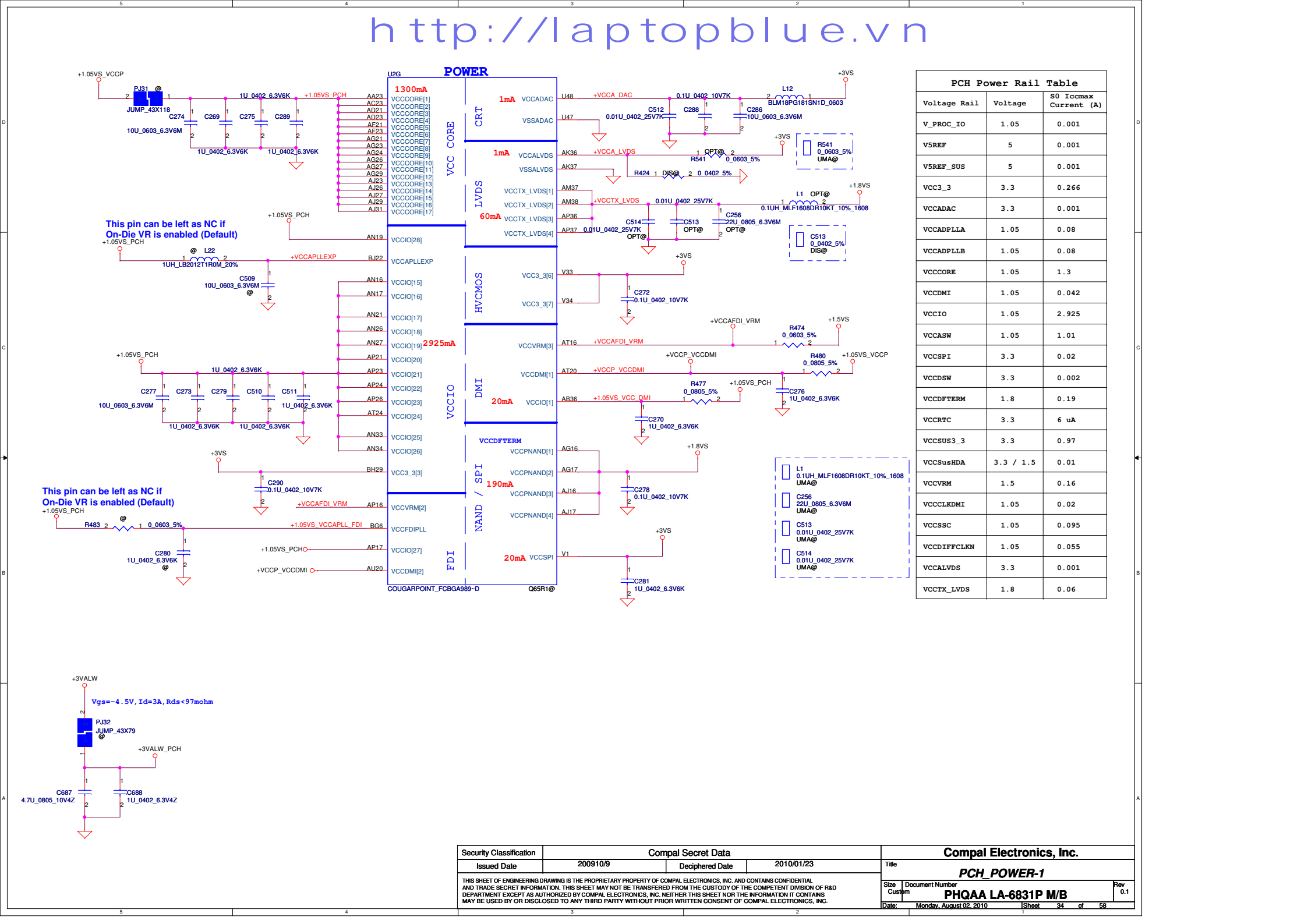
USB-Right
USB-Left & eSATA

Within 500 mils





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POWER

PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCADAC	3.3	0.001
VCCADPILLA	1.05	0.08
VCCADPLL	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTERM	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCTX_LVDS	1.8	0.06

This pin can be left as NC if On-Die VR is enabled (Default)

This pin can be left as NC if On-Die VR is enabled (Default)

Security Classification

Compal Secret Data

Compal Electronics, Inc.

PCH_POWER-1

PHQAA LA-6831P M/B

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POWER

PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCADAC	3.3	0.001
VCCADPILLA	1.05	0.08
VCCADPLL	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTERM	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3 / 1.5	0.97
VCCSUSHDA	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCTX_LVDS	1.8	0.06

This pin can be left as NC if On-Die VR is enabled (Default)

This pin can be left as NC if On-Die VR is enabled (Default)

Security Classification

Compal Secret Data

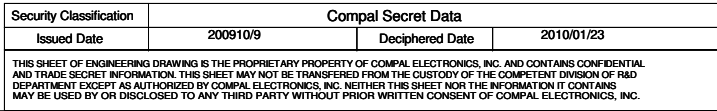
Compal Electronics, Inc.

PCH_POWER-1

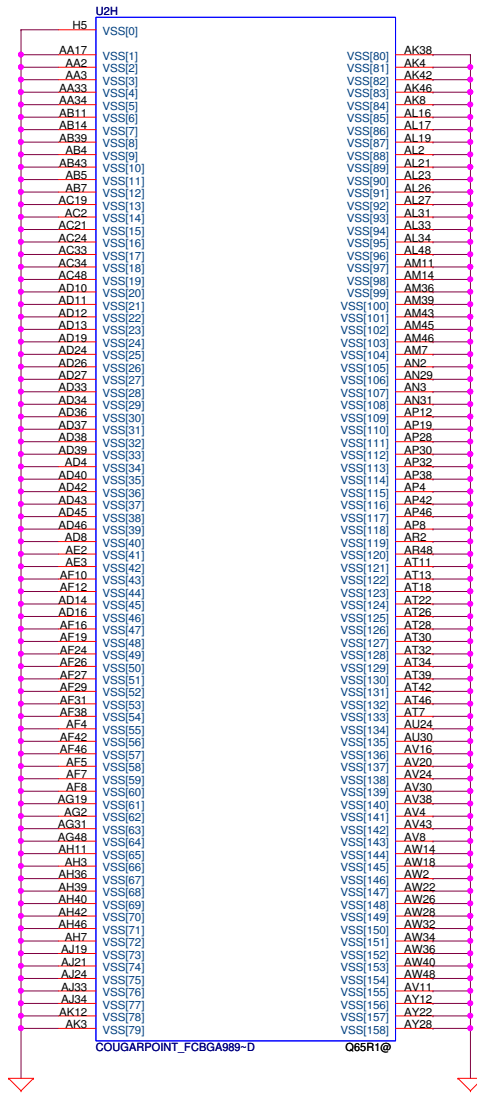
PHQAA LA-6831P M/B

Date: Monday, August 02, 2010 **Sheet:** 34 of 58

This pin can be left as NC if -
On-Die VR is enabled (Default)

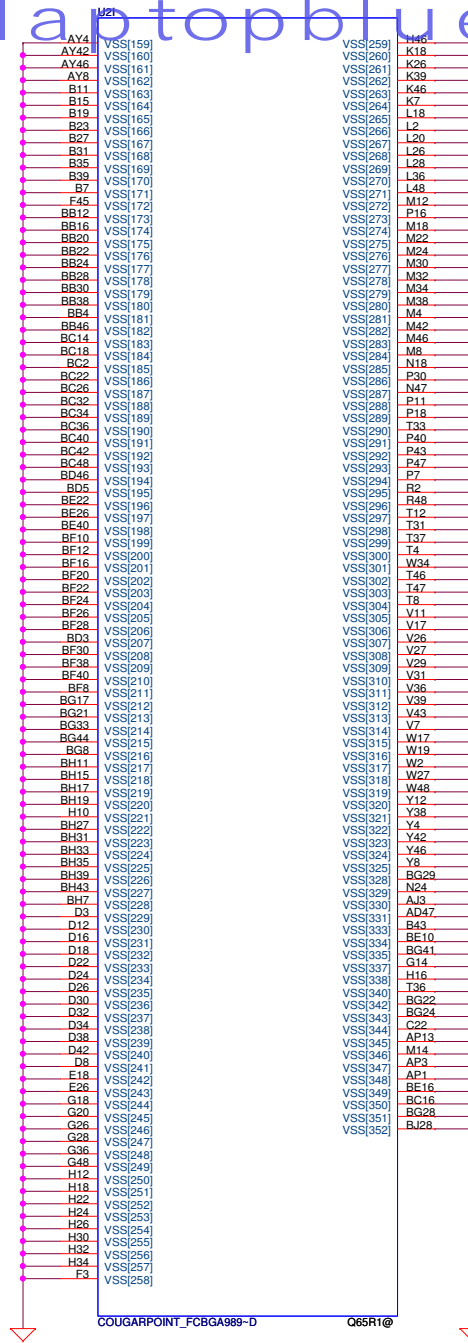


Compal Electronics, Inc.			
Title			
PCH_POWER-2			
Size	Document Number		Rev
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COUGARPOINT_FCBGA989-D

Q65R1@

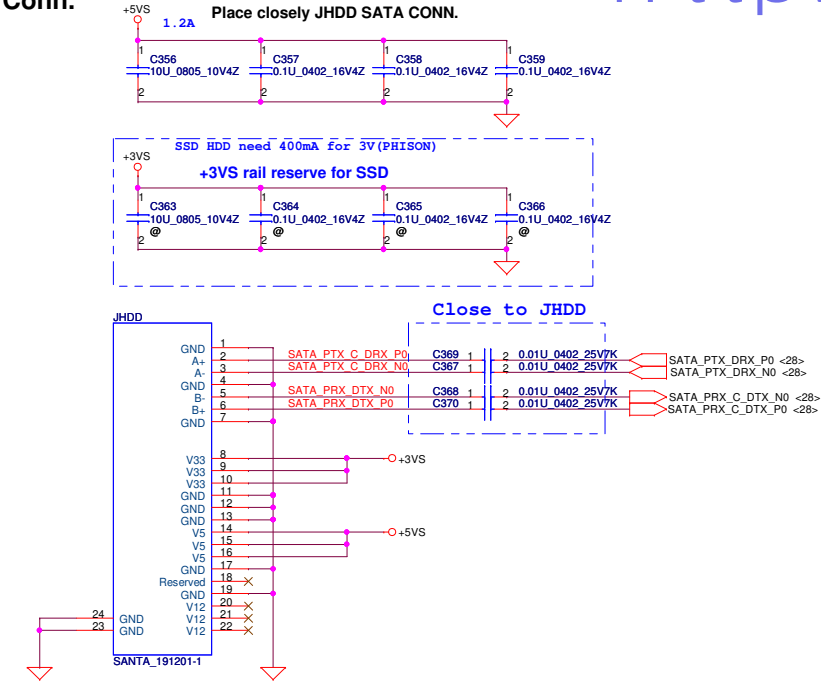


COUGARPOINT_FCBGA989-D

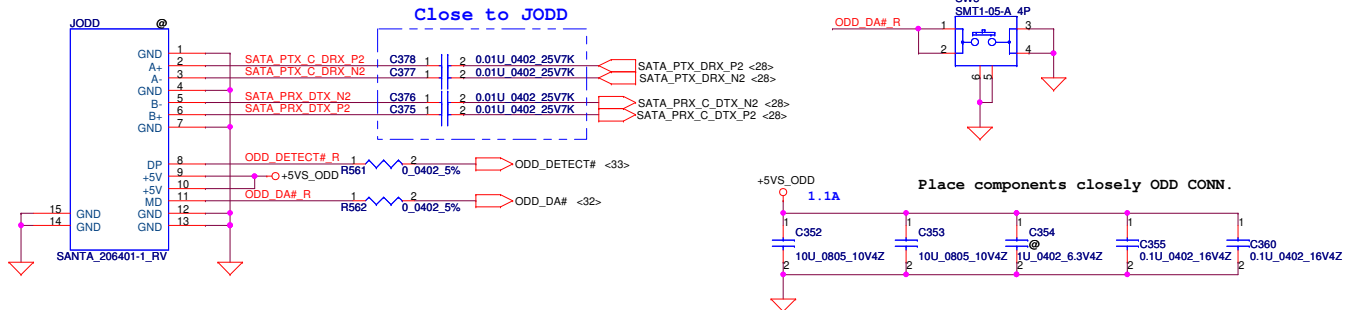
Q65R1@

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Size		Document Number		Rev	
Custom		PHQAA LA-6831P M/B		0.1	
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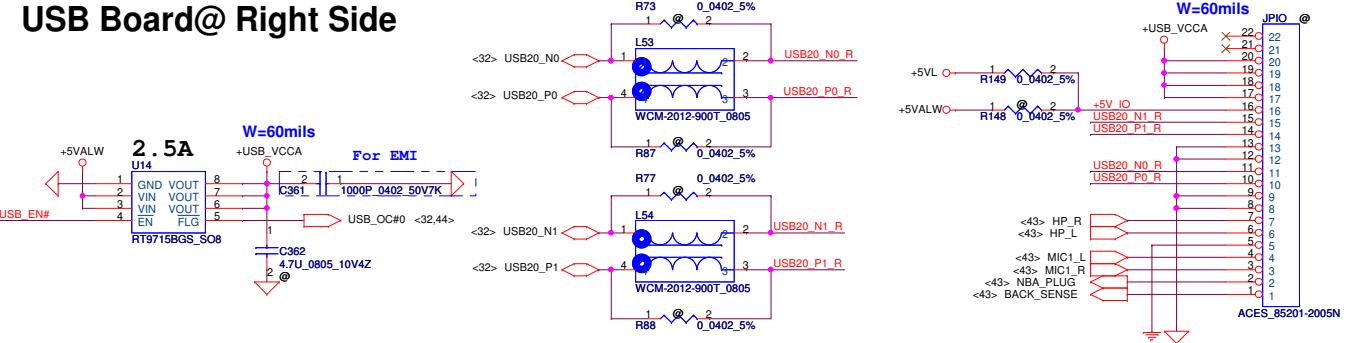
SATA HDD Conn.



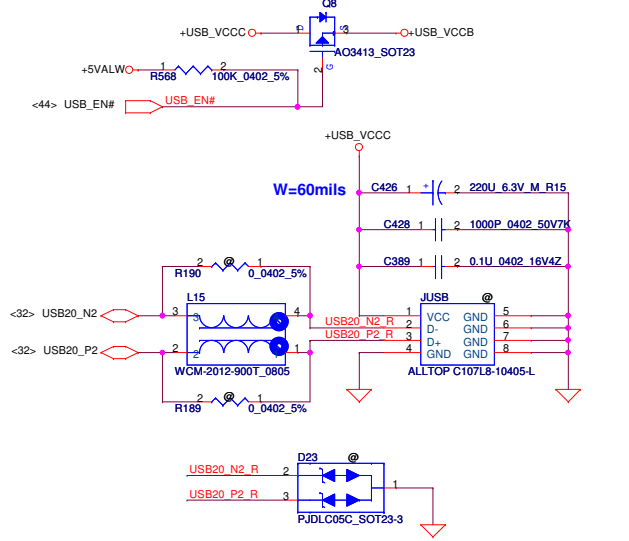
SATA ODD Conn



USB Board@ Right Side

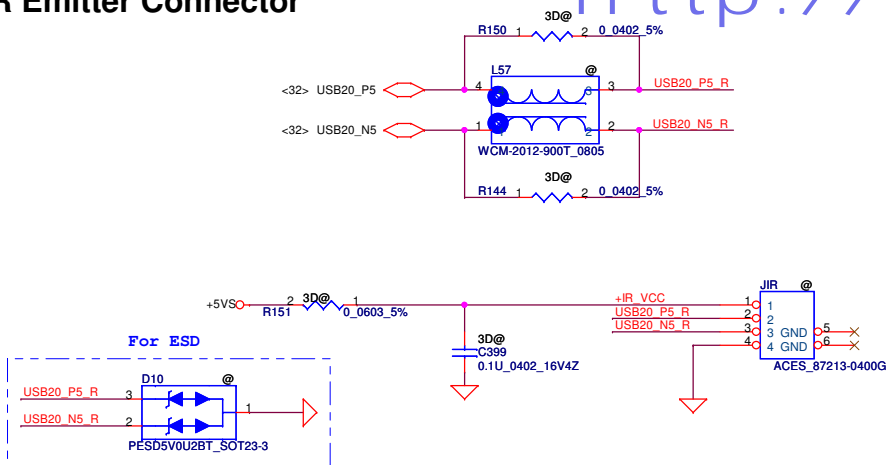


USB Board@ Left Side



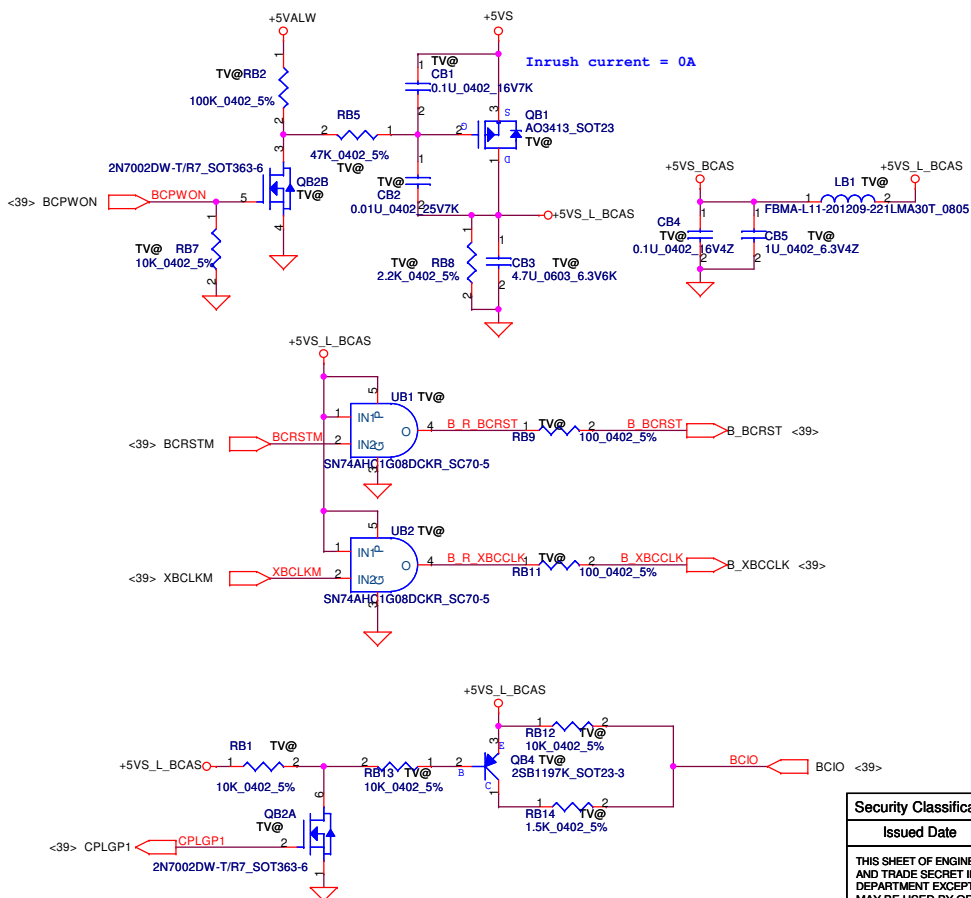
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Issued Date	200910/9	Deciphered Date	2010/01/23	SATA-HDD/ODD/USB	
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				Rev	0.1

IR Emitter Connector

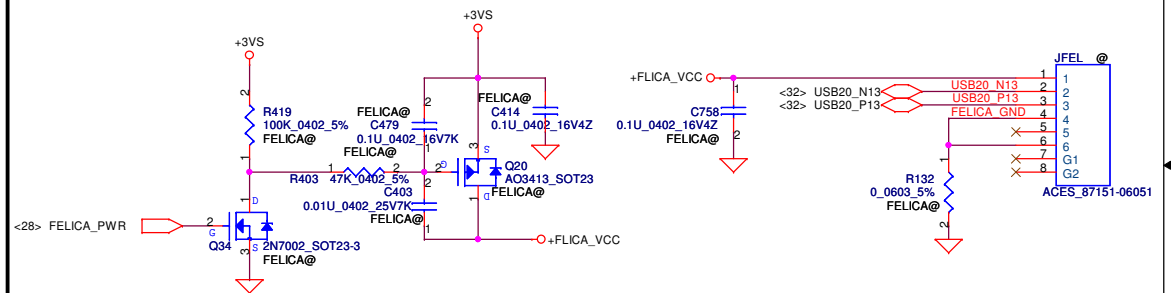


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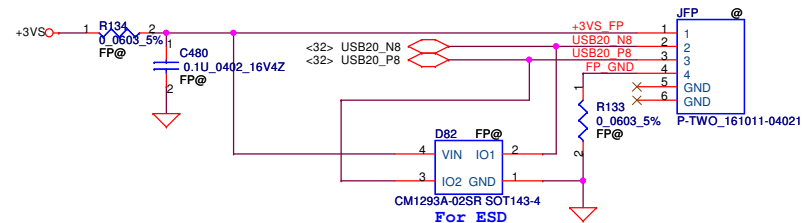
B-CAS Circuit



Felica

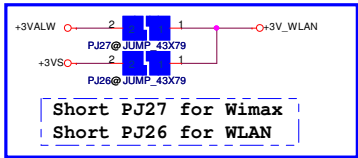


Finger printer



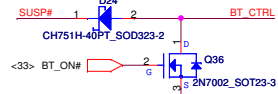
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						Size		Document Number		Rev	
								PHQAA LA-6831P M/B		0.1	
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Slot 1 Half PCIe Mini Card-WLAN/ WiMax



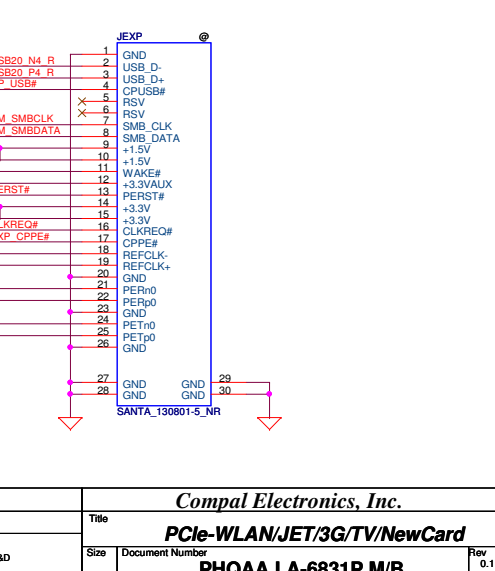
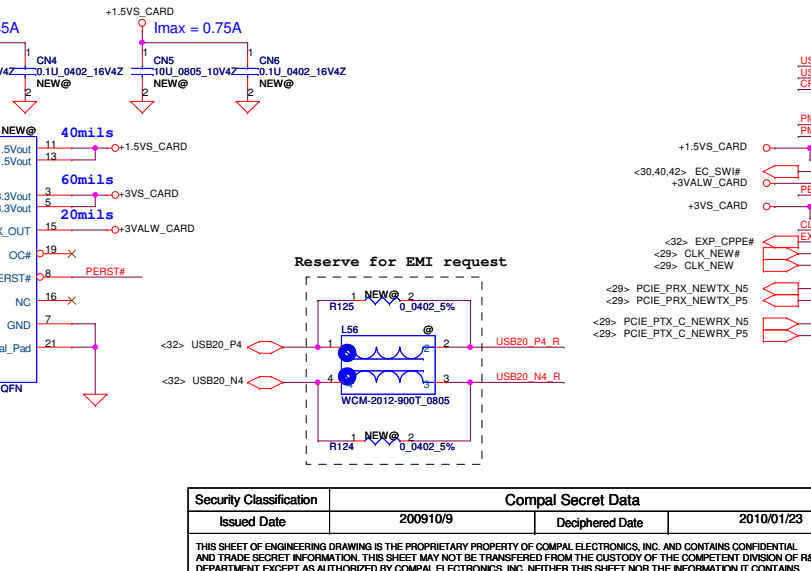
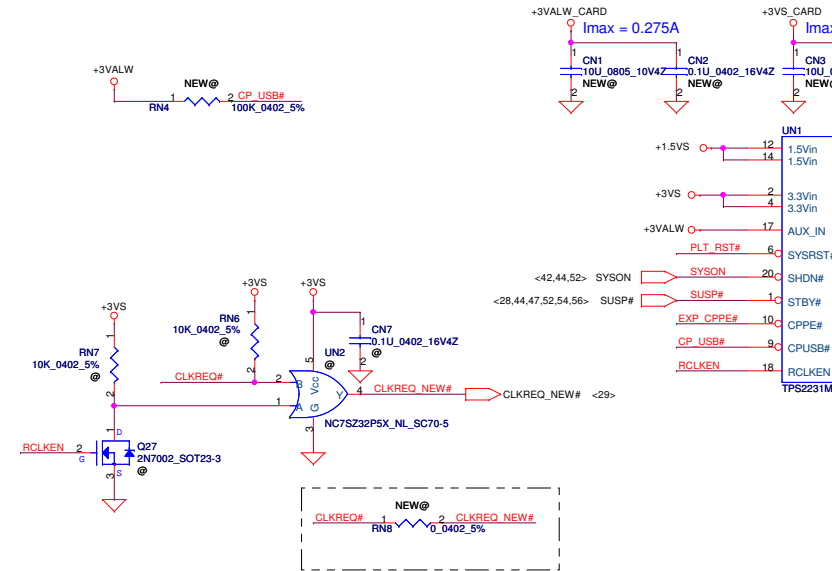
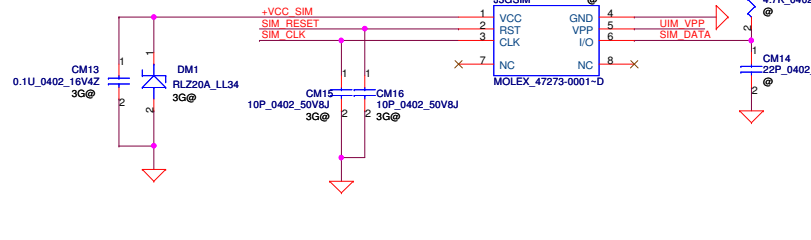
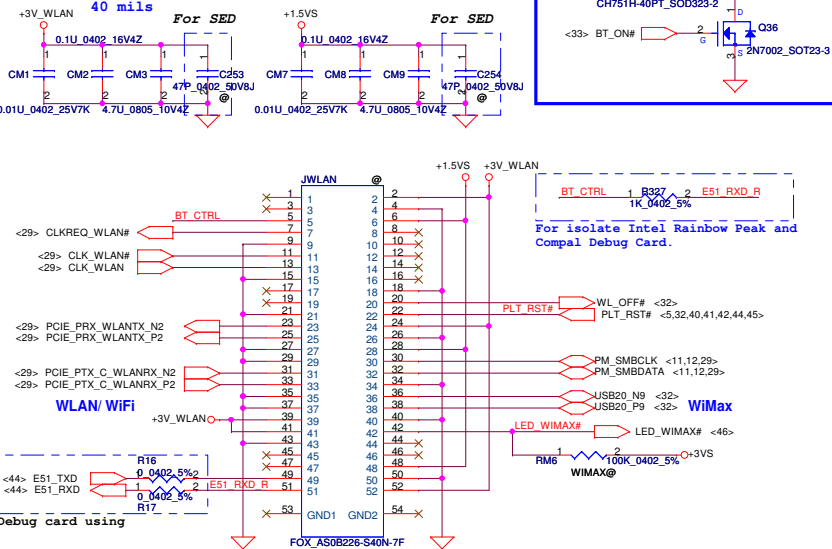
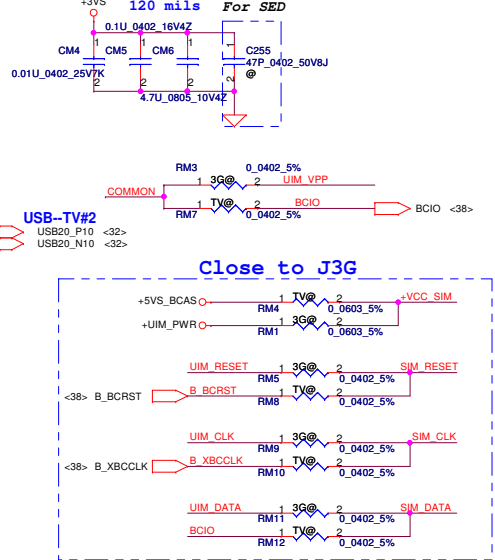
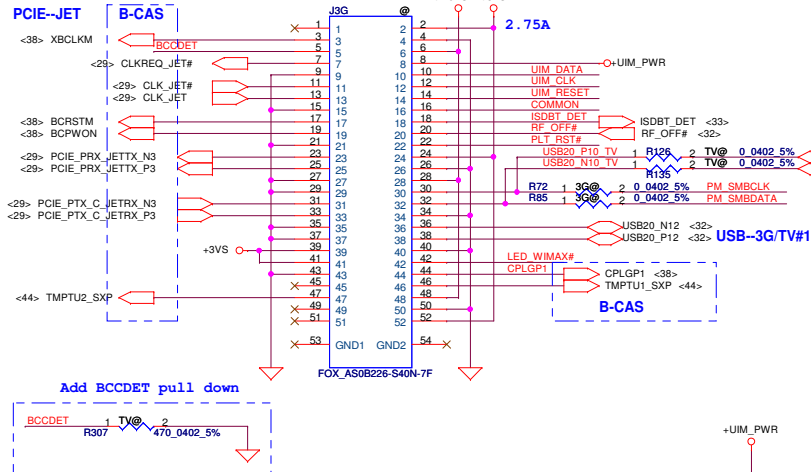
WLAN&BT Combo module circuits		
	BT on module	BT on module
	Enable	Disable
BT_CTRL#	H	L
BT_ON#	L	H

**If +3V_WLAN is +3VS, please remove D24

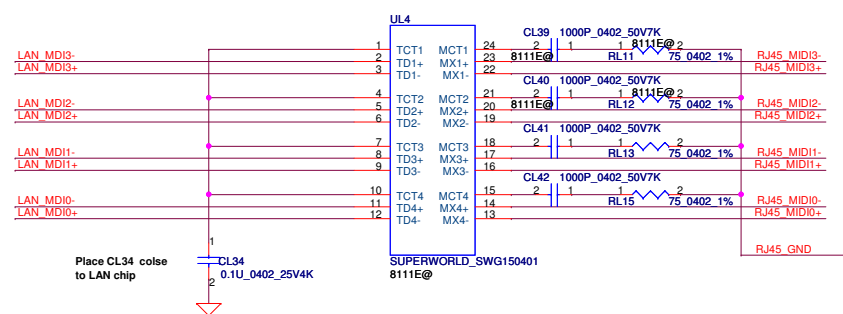
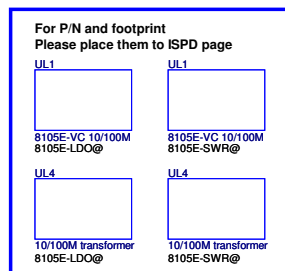
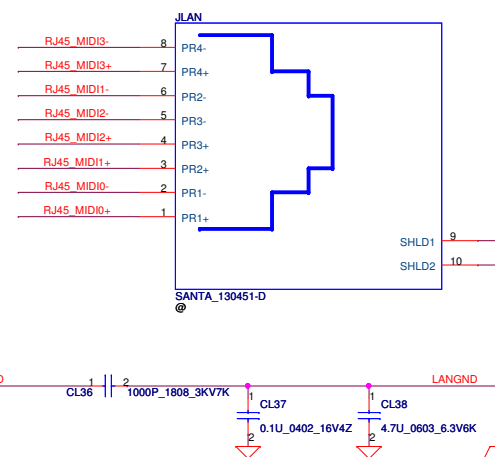
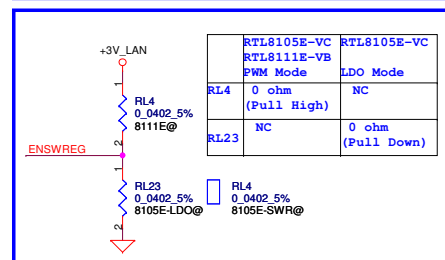
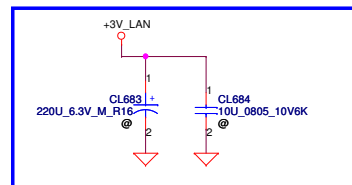
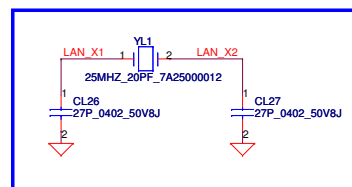
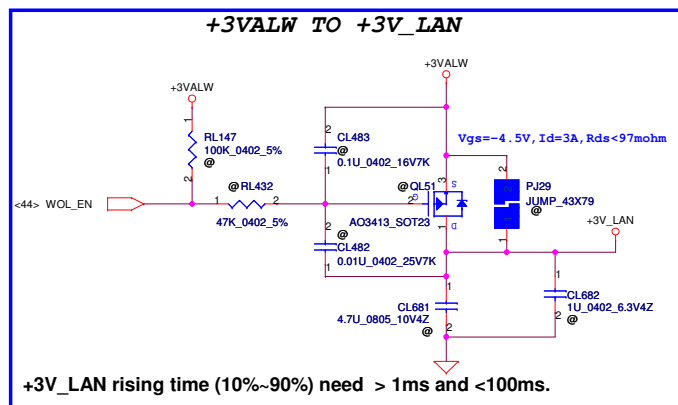
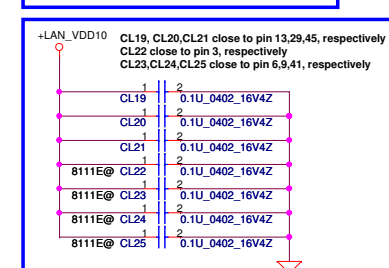
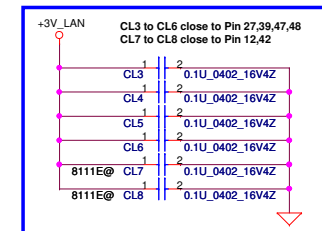
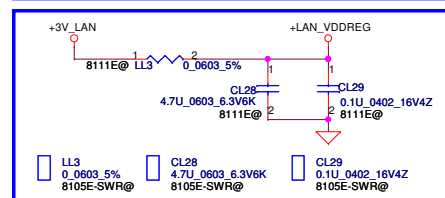
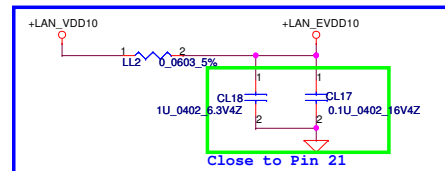
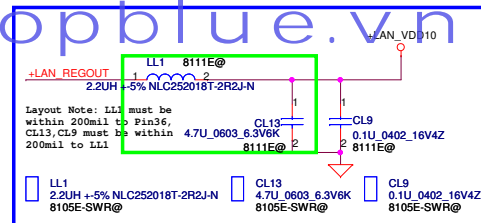
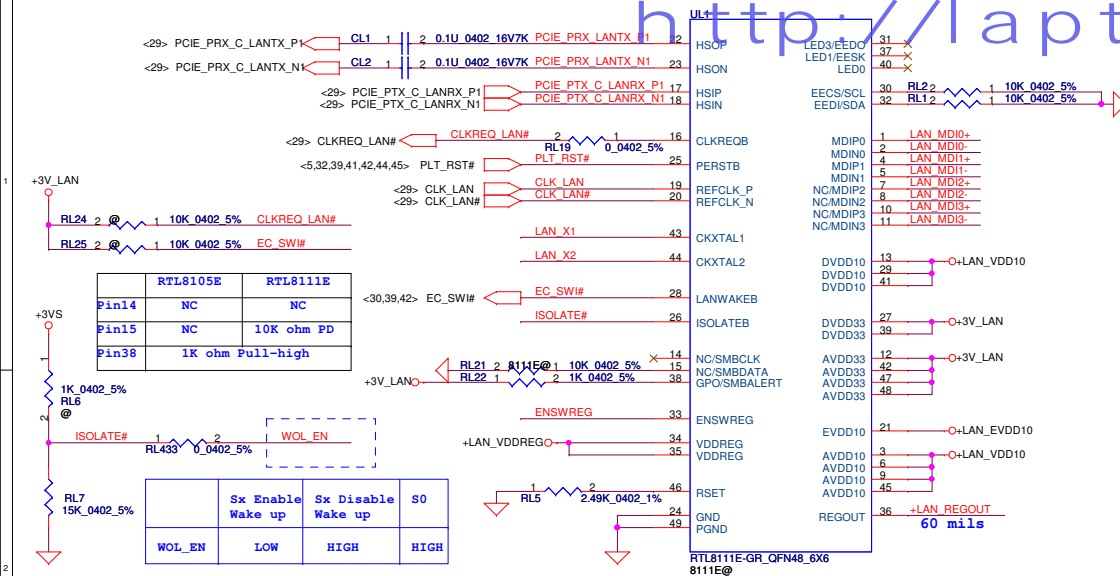


For isolate Intel Rainbow Peak and Compal Debug Card.

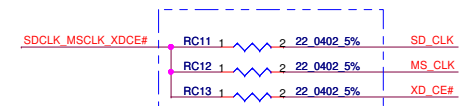
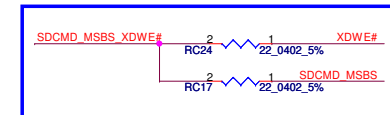
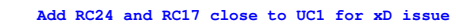
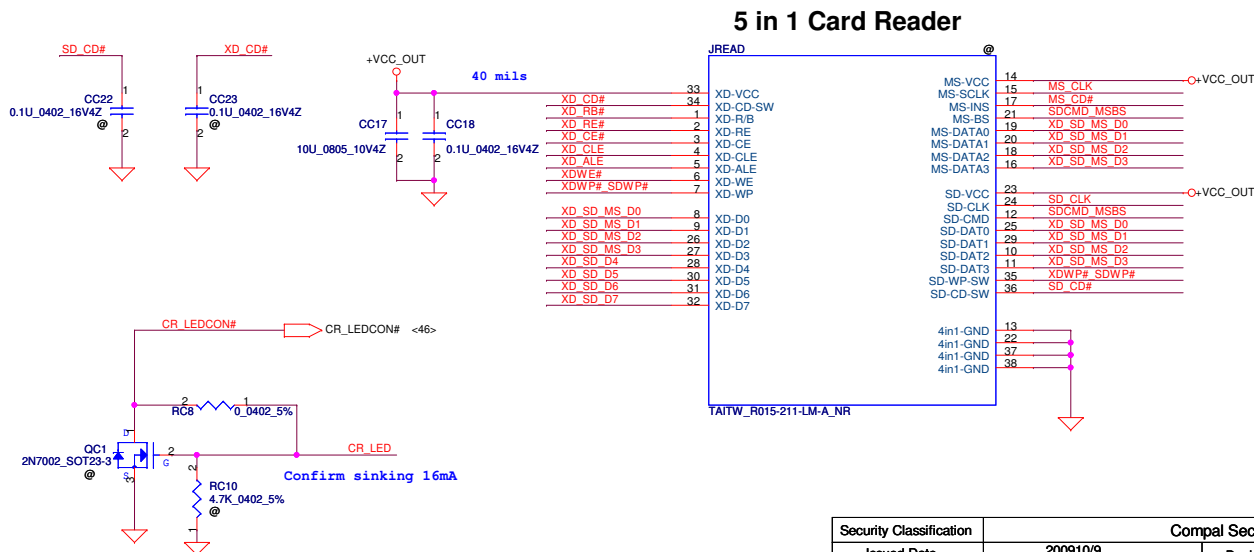
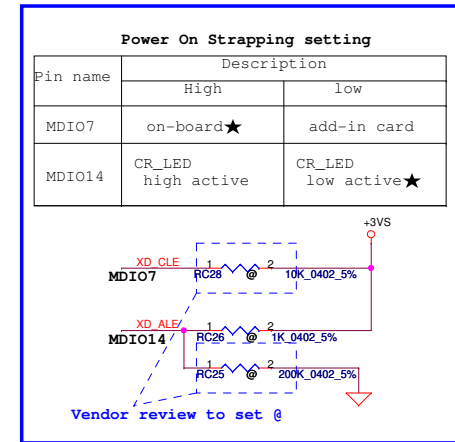
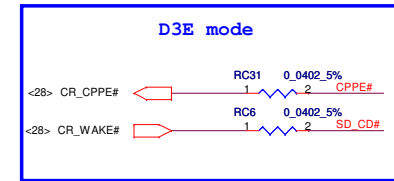
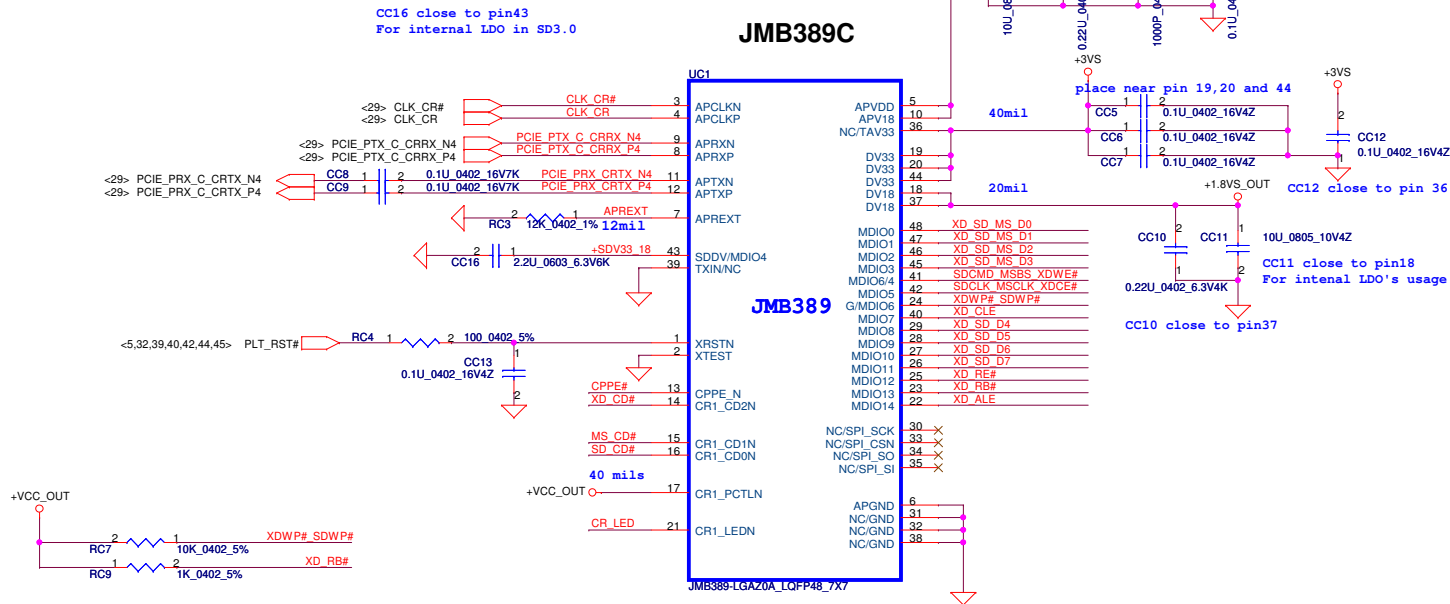
Slot 2 Full PCIe Mini Card- 3G/ TV Tuner
Half PCIe Mini Card- JET



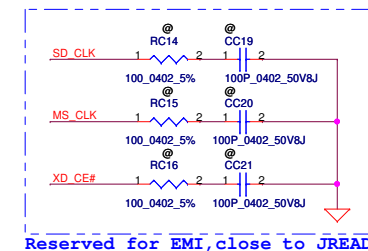
Security Classification		Compal Secret Data		Title	
Issued Date	2009/10/9	Deciphered Date	2010/01/23	PCIE-WLAN/JET/3G/TV/NewCard	
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				PHQAA LA-6831P M/B	
				Date	Monday, August 02, 2010
				Sheet	39 of 58

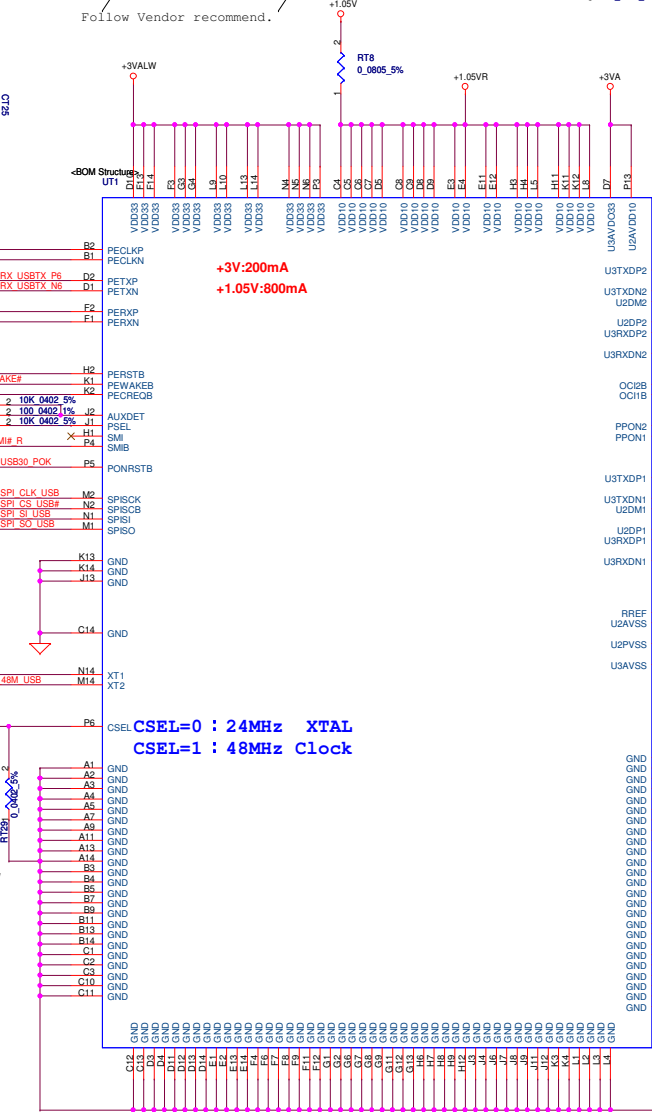
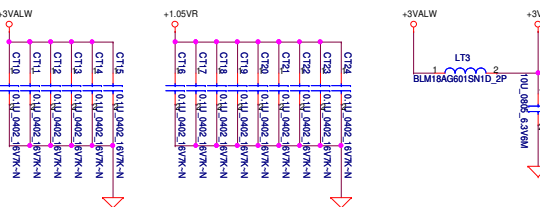
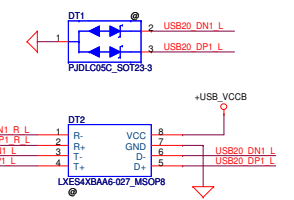
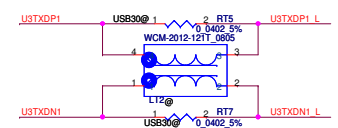
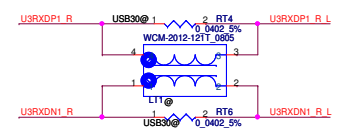
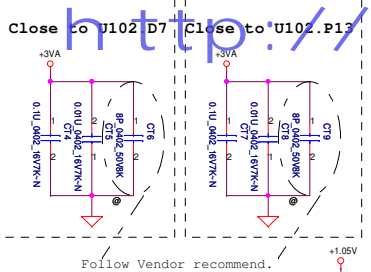
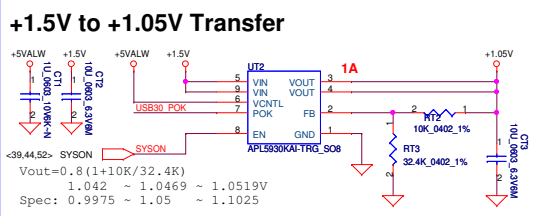


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Issued Date	2009/10/05	Deciphered Date	2010/01/23	Title	
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				Customer	0.1
				Document Number PHQAA LA-6831P M/B	
Date: Monday, August 02, 2010		Sheet 40 of 58			



Reserved for EMI, close to UC1.42



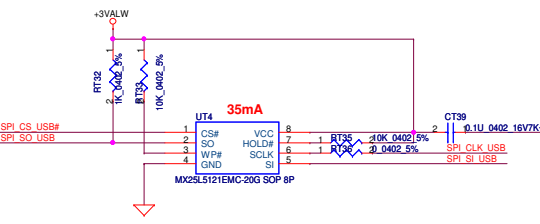


USB Sleep & Charge Auto-Mode

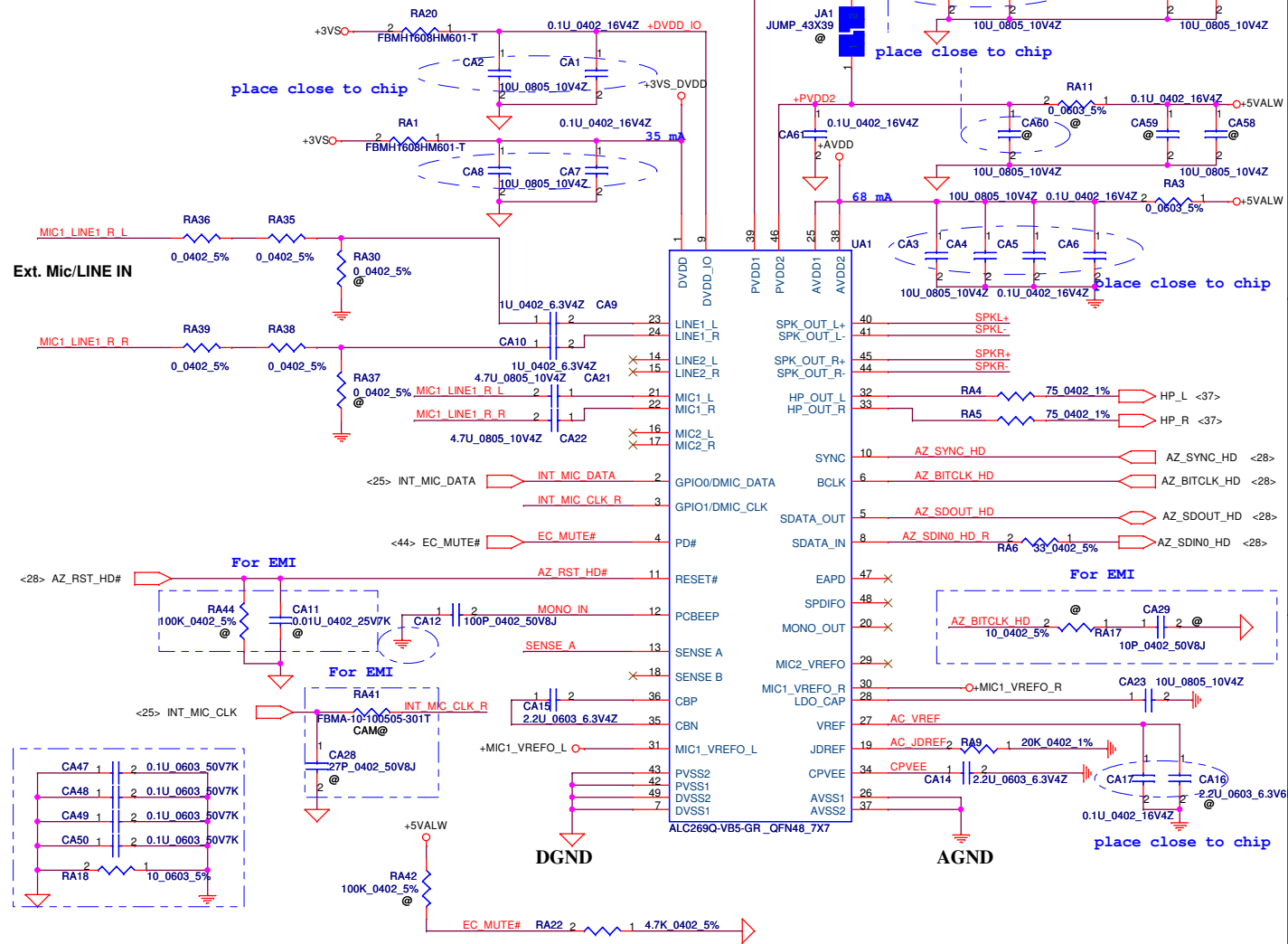
07/08/2010
Need EC to set these signals to high active
SLP_CHG, USB_CHG_EN

SLP_CHG_M4	SLP_CHG_M3	SLP_CHG	Mode
0	0	X(1)	Dedicated Charging Port, Auto-detect
0	1	X(1)	Dedicated Charging Port, BC Specification 1.1 Only (Mode 3)
1	0	X(1)	Dedicated Charging Port, Apple Only (Mode 4)
1	1	0	Standard Downstream Port, USB 2.0 Mode
1	1	1	Charging Downstream Port, BC Specification 1.1

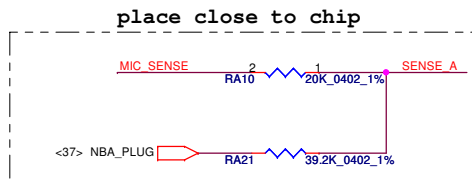
Place as close as possible to U102.2P13 and U102.2P14



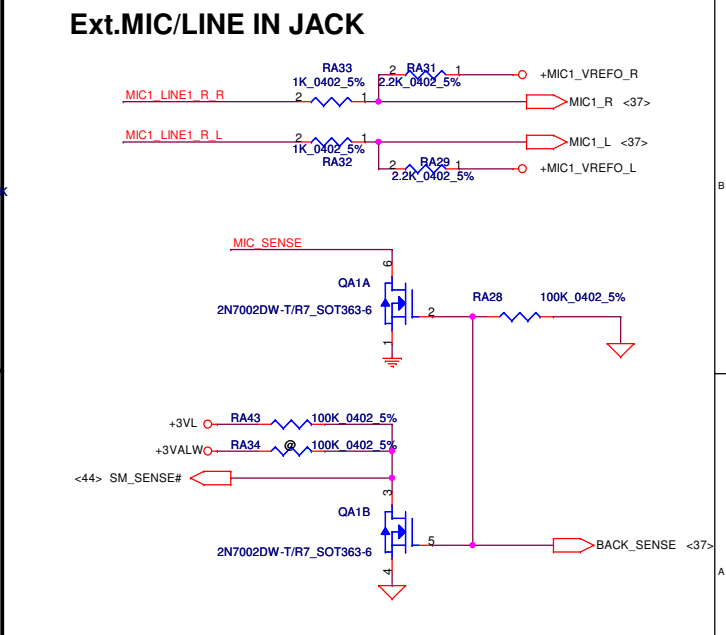
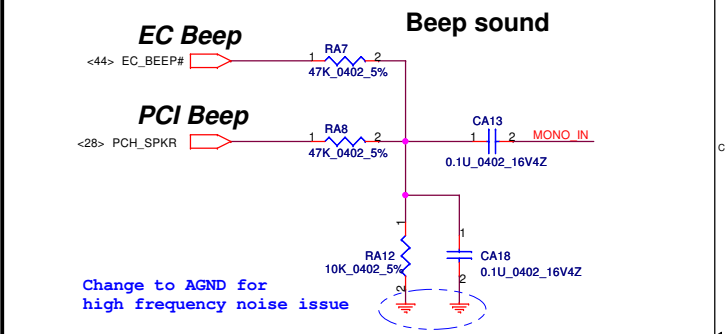
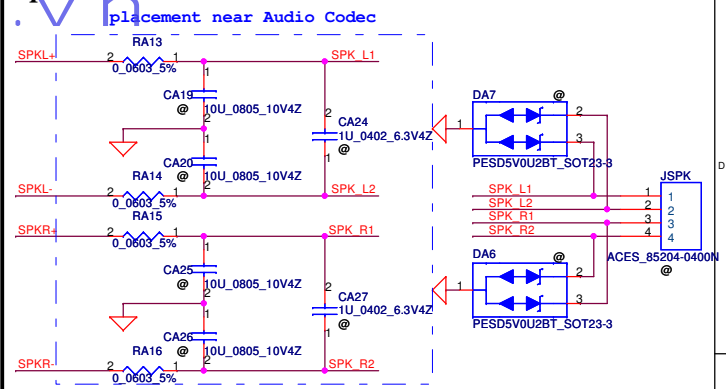
http://laptopblue.vn



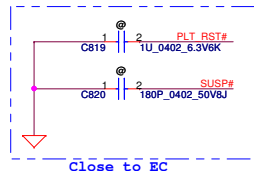
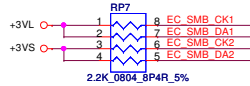
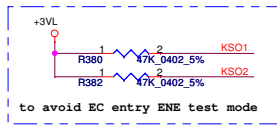
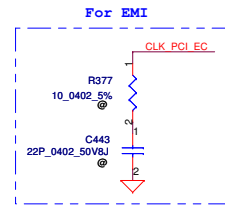
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



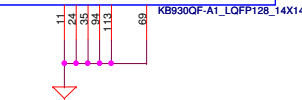
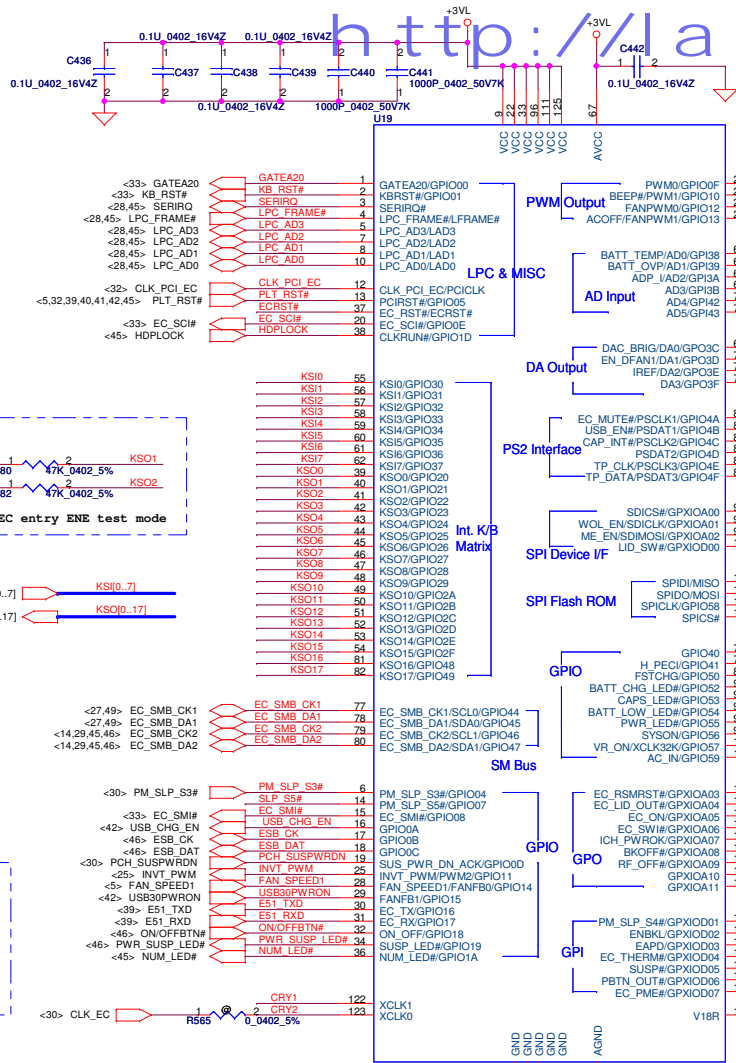
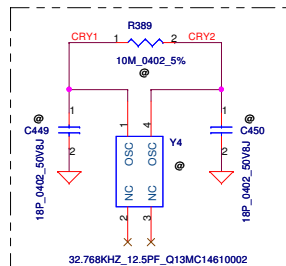
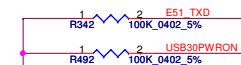
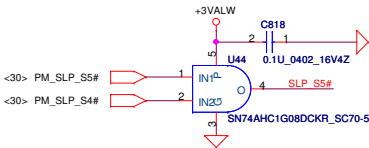
Speaker Connector



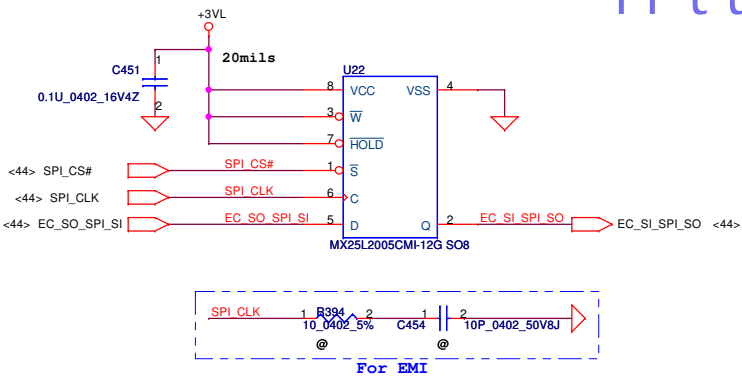
Security Classification		Compal Secret Data				Compal Electronics, Inc.							
Issued Date		200910/9		Deciphered Date		2010/01/23		Title		HDA-ALC269/HP/MIC			
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								Date:		Monday, August 02, 2010		Sheet	



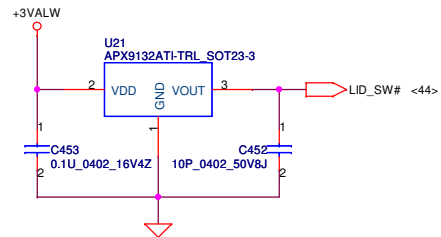
Close to EC



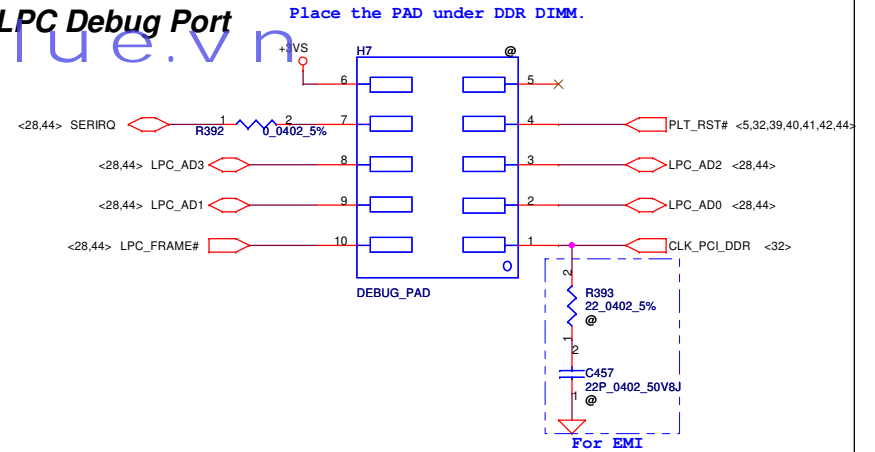
SPI Flash (256KB)



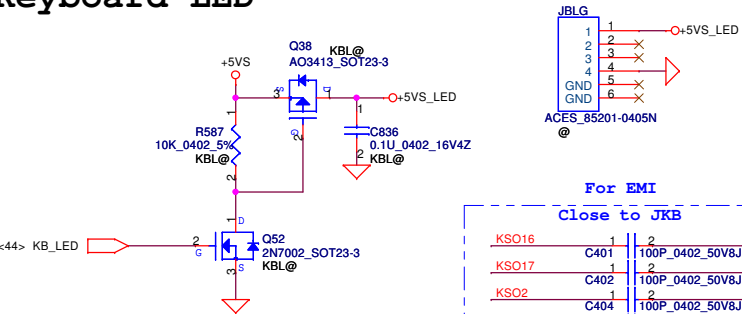
Lid SW



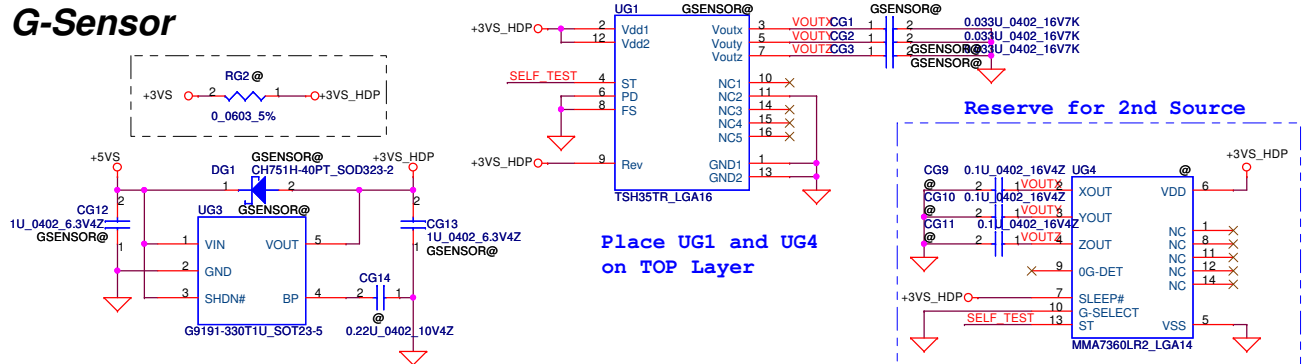
LPC Debug Port



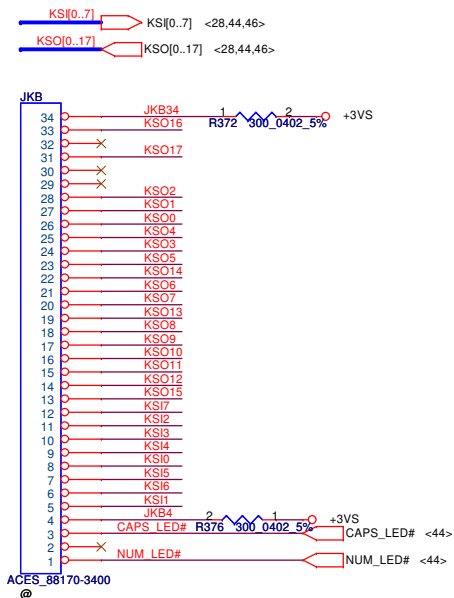
Keyboard LED



G-Sensor



KEYBOARD CONN.

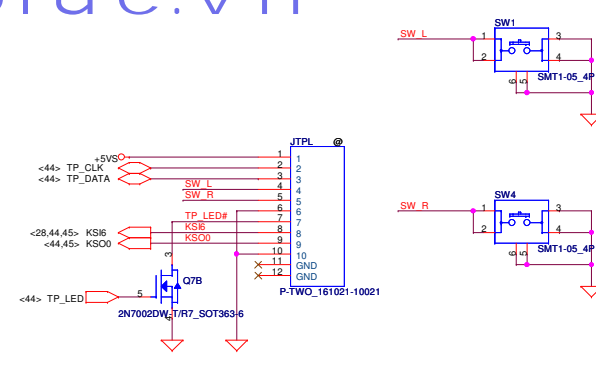
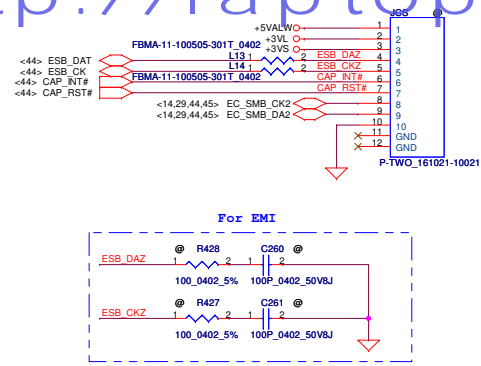


For EMI	Close to JKB
KSO16	C401
KSO17	C402
KSO2	C404
KSO1	C405
KSO0	C406
KSO4	C407
KSO3	C408
KSO5	C409
KSO6	C410
KSO7	C411
KSO13	C412
KSO8	C413
KSO9	C415
KSO10	C416
KSO11	C417
KSO12	C418
KSO14	C419
KSO15	C420
KSI7	C421
KSI2	C422
KSI3	C423
KSI4	C424
KSI0	C425
KSI5	C427
KSI6	C429
KSI1	C431
CAPS_LED#	C433
NUM_LED#	C435

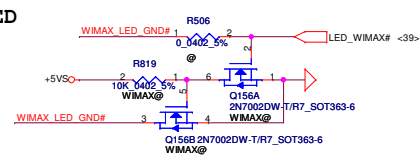
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Size	Document Number	PHQAA LA-6831P M/B		Rev 0.1
Date:	Monday, August 02, 2010	Sheet	45	of 58

Caps Sensor/Light Sensor Conn.

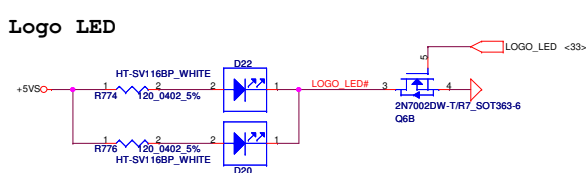
Caps Sensor/Light Sensor Conn. Touchpad & Light



WiMAX LED



Logo LED



VGA

H5 H_3P0
H6 H_3P0
H8 H_3P0
H9 H_3P0
H10 H_3P0
H11 H_3P0
H12 H_3P0
H13 H_3P0
H14 H_3P0

H1 H_2P7x3P2N
H26 H_2P7N

MINI CARD -- 3G

H2 H_2P9
H3 H_2P9x3P9
H4 H_2P9x3P9

CPU

H20 H_4P2
H21 H_4P2x4P7
H22 H_4P2x4P7
H23 H_4P7

MINI CARD -- WLAN

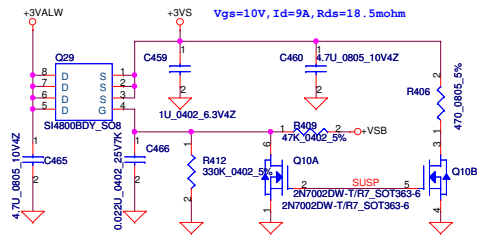
H15 H_3P3
H16 H_3P3
H17 H_3P3
H18 H_3P3
H19 H_3P3

Pin 120N connection diagram for the ACES_85201-120SN component. The diagram shows a 120-pin package with pins 1 through 12 connected to various signals. Pin 1 is JLED, pin 2 is +5VSWO, pin 3 is +5VSWO, pin 4 is WIMAX_LED_GND#, pin 5 is WL_BT_LED#, pin 6 is <33> WL_BT_LED#, pin 7 is PWR_ON_LED#, pin 8 is PWR_SUSP_LED#, pin 9 is PWR_ON_LED#, pin 10 is PWR_SUSP_LED#, pin 11 is CR_LED#, pin 12 is CR_LEDCON#, pin 13 is BATT_FULL_LED#, pin 14 is BATT_CHG_LOW_LED#, pin 15 is <44> BATT_FULL_LED#, pin 16 is <44> BATT_CHG_LOW_LED#, pin 17 is <41> CR_LED#, pin 18 is <44> BATT_FULL_LED#, pin 19 is <44> BATT_CHG_LOW_LED#, pin 20 is <41> CR_LED#. Pins 13 through 16 are connected to pins 13 through 16 of the ACES_85201-120SN component. Pins 17 through 20 are connected to pins 17 through 20 of the ACES_85201-120SN component.

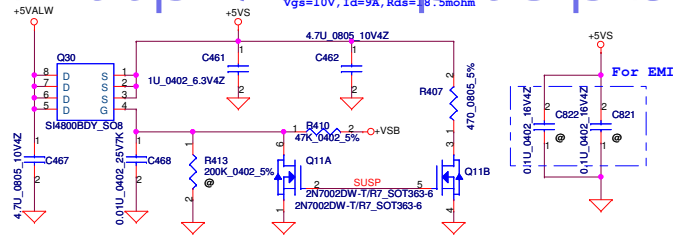
UV1 N12PGSR3@ N12P-GS-A1	UV1 N12MGER1@ N12M-GE-B-B1	U2 Q65R3@ PCH	ZZZ PCB LA-6831P
UV1 N12PGER1@ N12P-GE-A1	UV1 N12MGER3@ N12M-GE-B-B1	U2 Q67R1@ PCH	PJP1 45 PJP1
UV1 N12PGER3@ N12P-GE-A1		U2 Q67R3@ PCH	

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								PWR/Cap./TP/LED/LP/LS/Screw									
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										Size	Document Number						Rev
											PHQAA LA-6831P M/B						0.1
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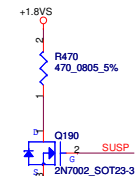
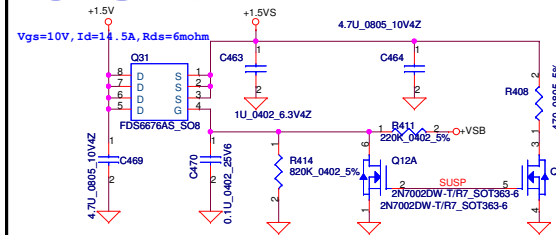
+3VALW TO +3VS



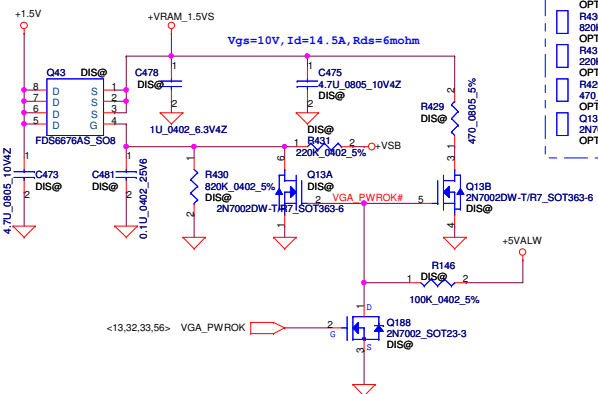
+5VALW TO +5VS



+1.5V to +1.5VS

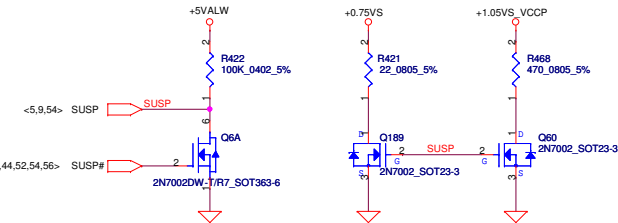
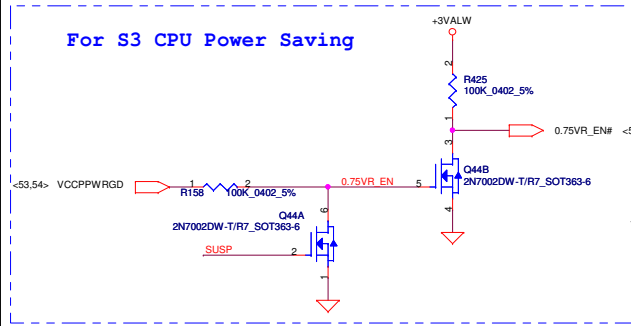


+1.5V to +VRAM_1.5VS



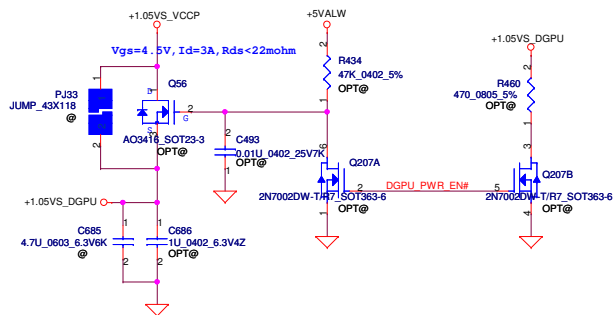
- Q43 FDS6676AS_S08 OPT@
- C481 0.1uF 0402_25V6 DIS@
- R430 820K_0402_5% OPT@
- R431 220K_0402_5% OPT@
- R429 470_0805_5% OPT@
- Q13 2N7002DW-T/R7_SOT363-6 OPT@
- C473 4.7uF 0805_10V4Z OPT@
- C479 1uF 0402_6.3V4Z OPT@
- C475 4.7uF 0805_10V4Z DIS@
- R146 100K_0402_5% OPT@
- Q188 2N7002_SOT23-3 OPT@

For S3 CPU Power Saving

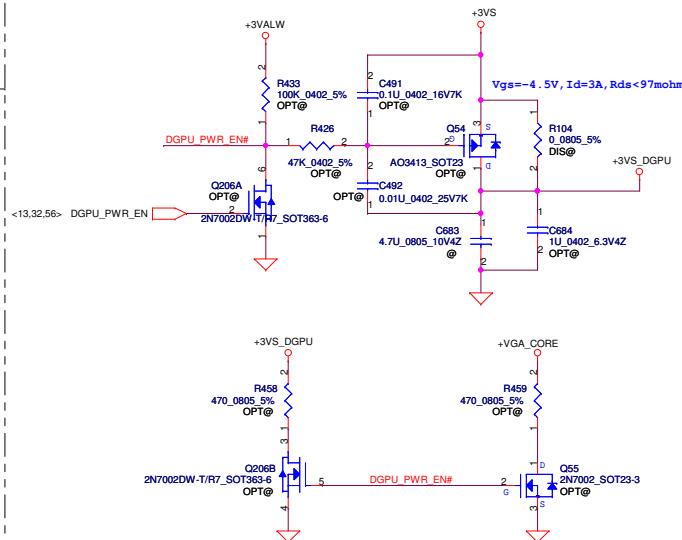


+1.05VS_VCCP to +1.05VS_DGPU

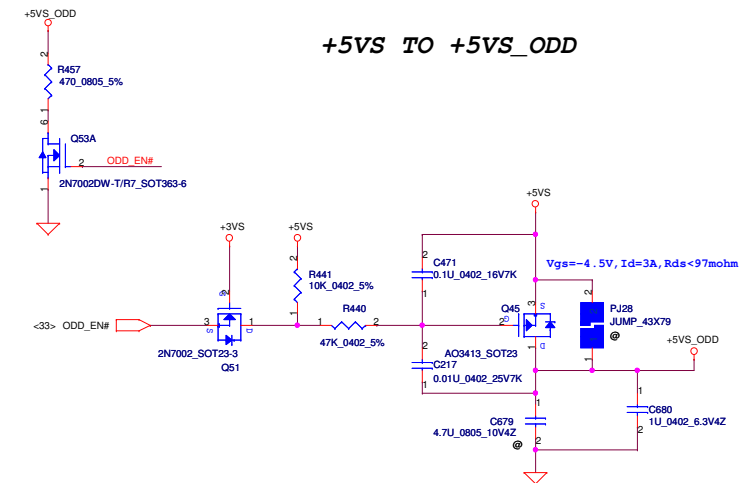
Short PJ33 for Discrete SKUs



+3VS to +3VS_DGPU

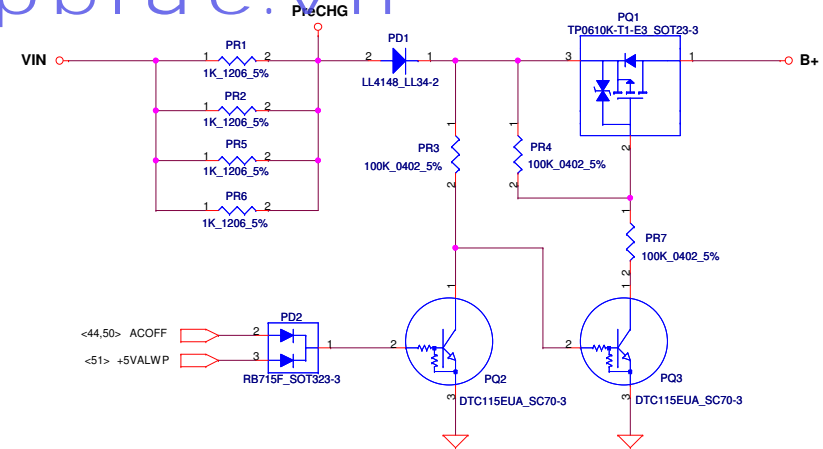
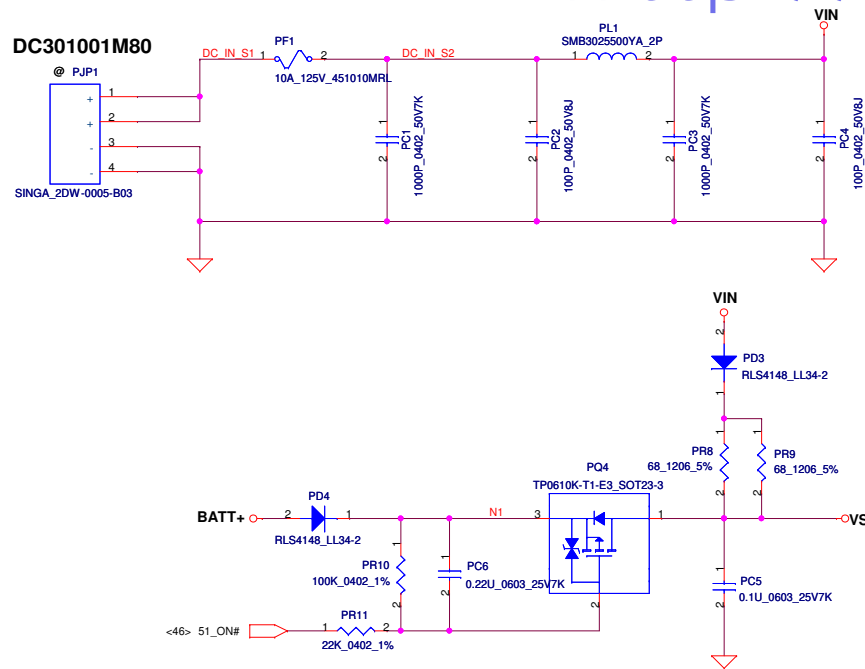


+5VS TO +5VS_ODD

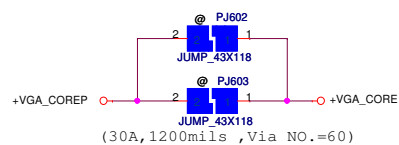
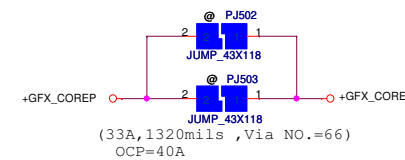
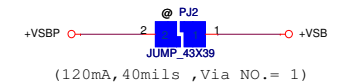
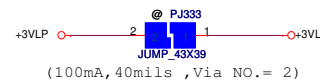
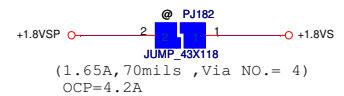
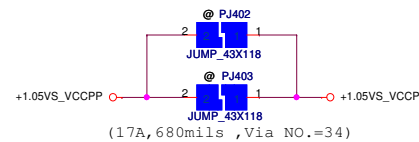
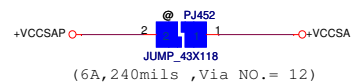
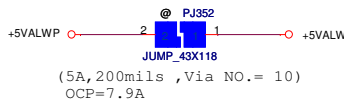
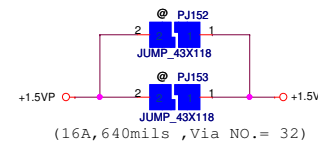
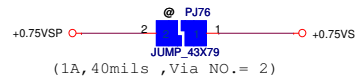
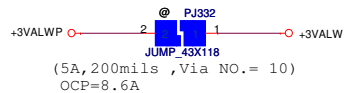
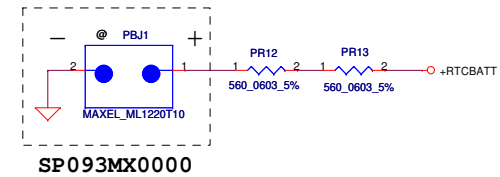


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Size	Document Number	Rev	P HQAA LA-6831P M/B	
Date	Monday, August 02, 2010	Sheet	47	of 58

DC301001M80



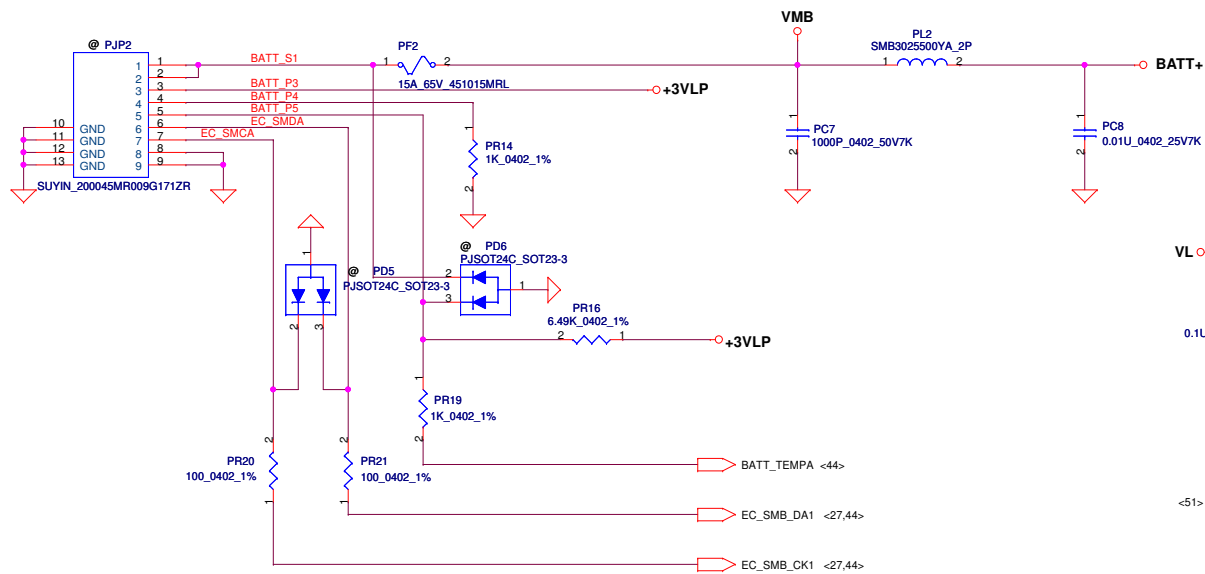
RTC Battery



ACIN

	Precharge detector		
	Min.	typ.	Max.
H->L	14.42V	14.74V	15.23V
L->H	15.39V	15.88V	16.39V

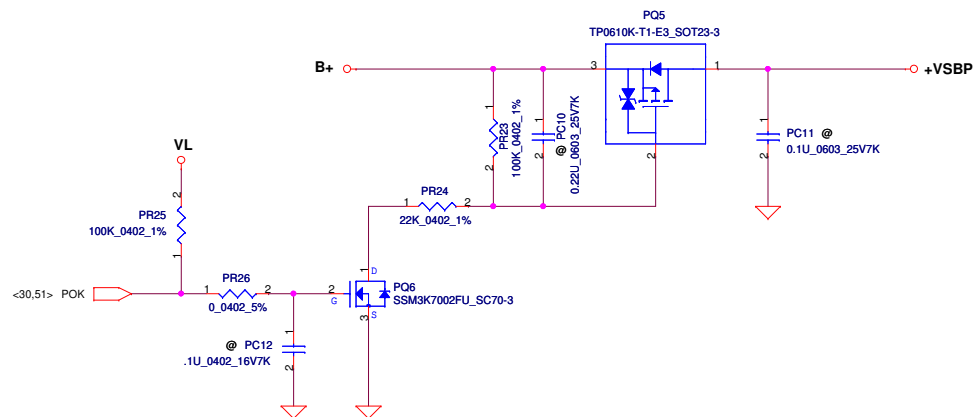
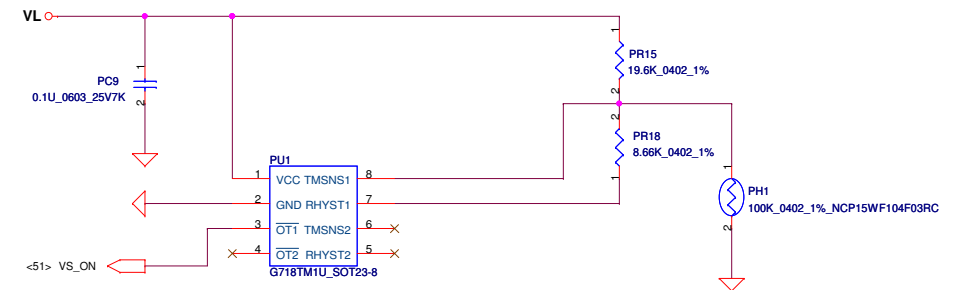
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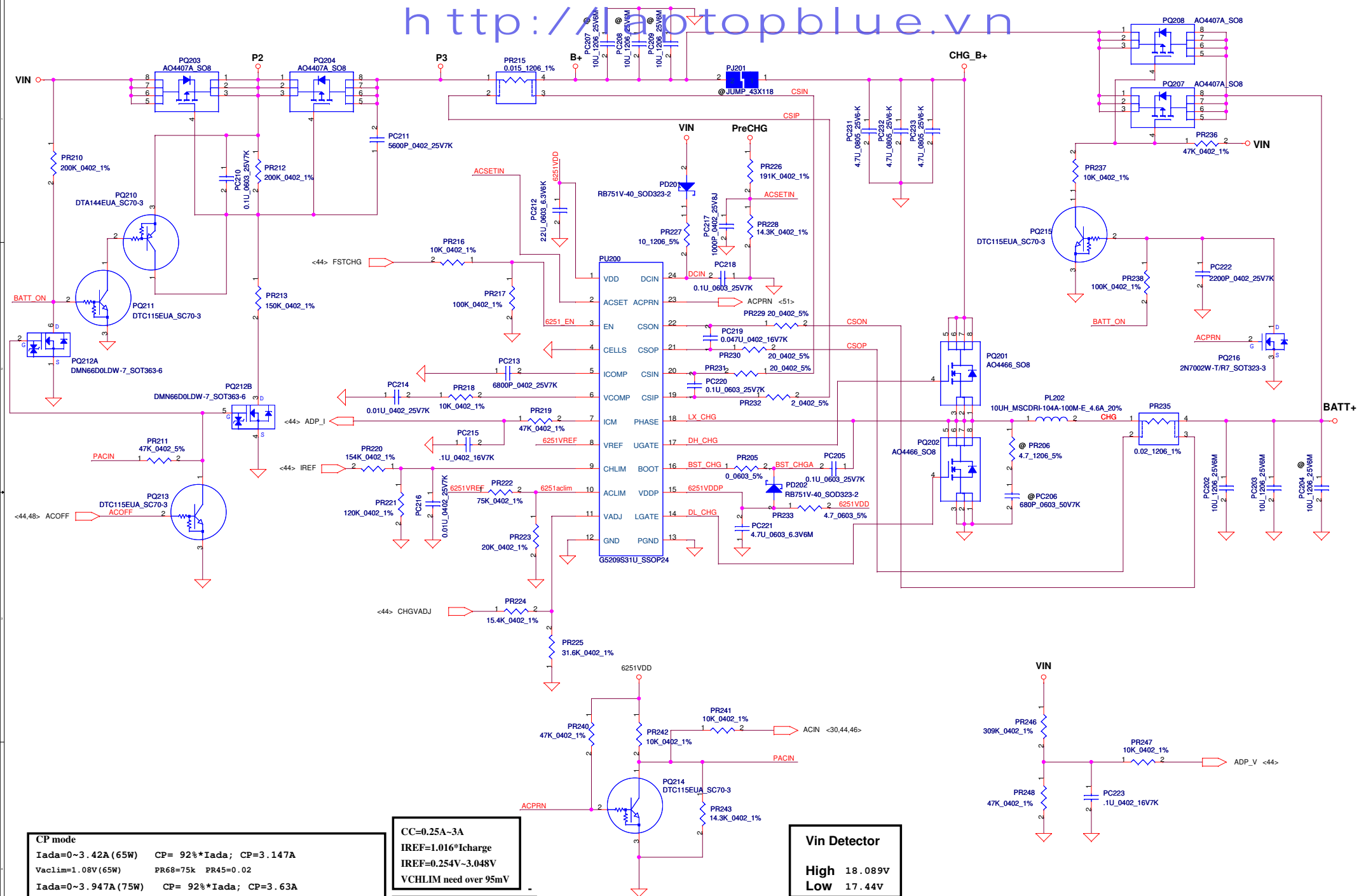
PH1 under CPU botten side :

CPU thermal protection at 95 degree C

Recovery at 56 degree C



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CP mode

Iada=0~3.42A (65W)	CP= 92%*Iada; CP=3.147A
Vac1im=1.08V (65W)	PR68=75k PR45=0.02
Iada=0~3.947A (75W)	CP= 92%*Iada; CP=3.63A
Vac1im=0.736V (75W)	PR68=24k PR70=20k PR49=0.02
Iada=0~4.737A (90W)	CP= 92%*Iada; CP=4.36A
Vac1im=0.736V (90W)	PR68=53.6k PR70=20k PR49=0.015
Iada=0~6.316A (120W)	CP= 92%*Iada; CP=5.81A
Vac1im=0.736V (120W)	PR68=8.25k PR70=26.7k PR49=0.015

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95

$$\text{CHGVAD.I} = (\text{Vcell} - 4) * 9.445$$

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

Vin Detector

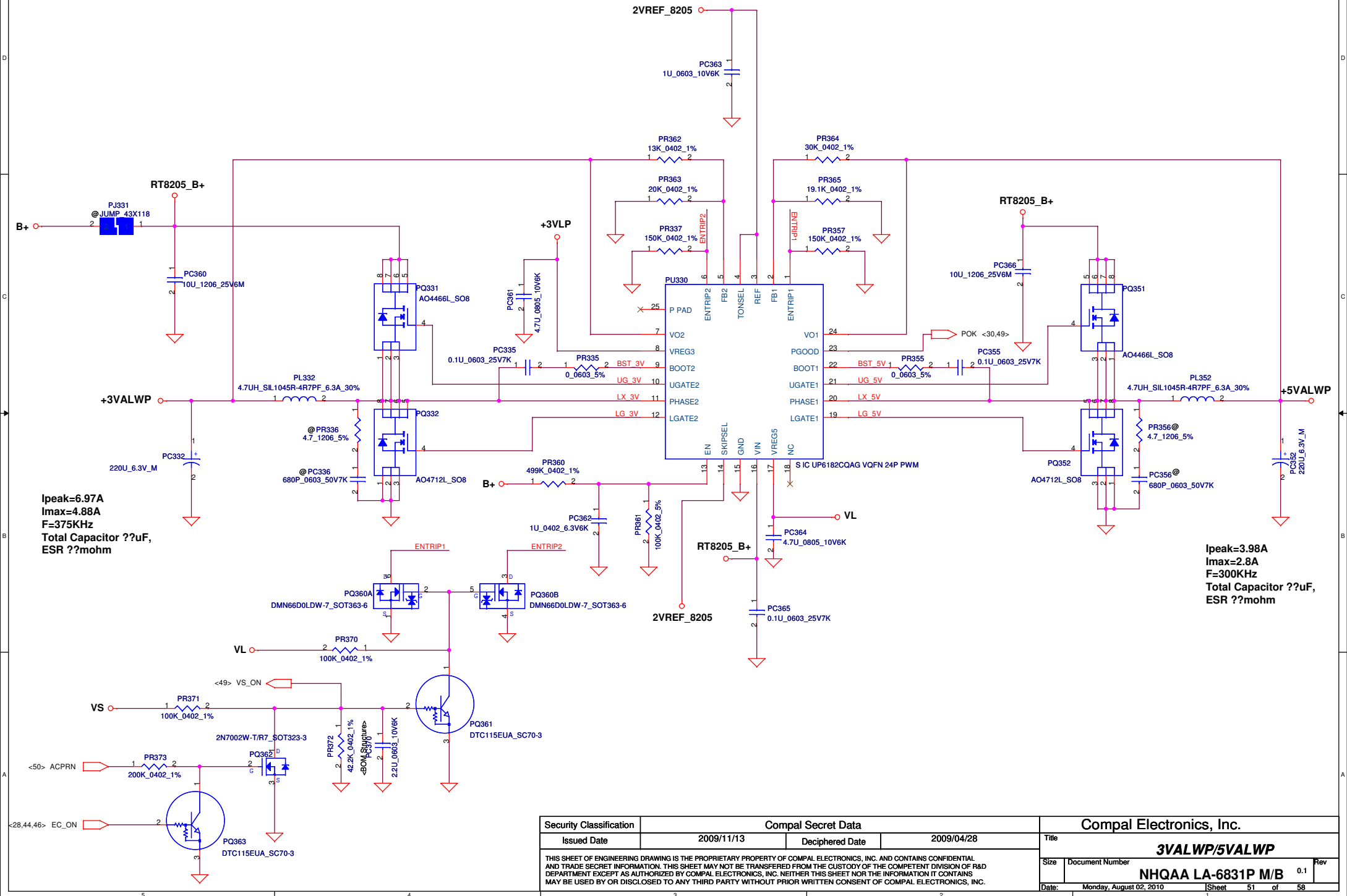
High	18.089V
Low	17.44V

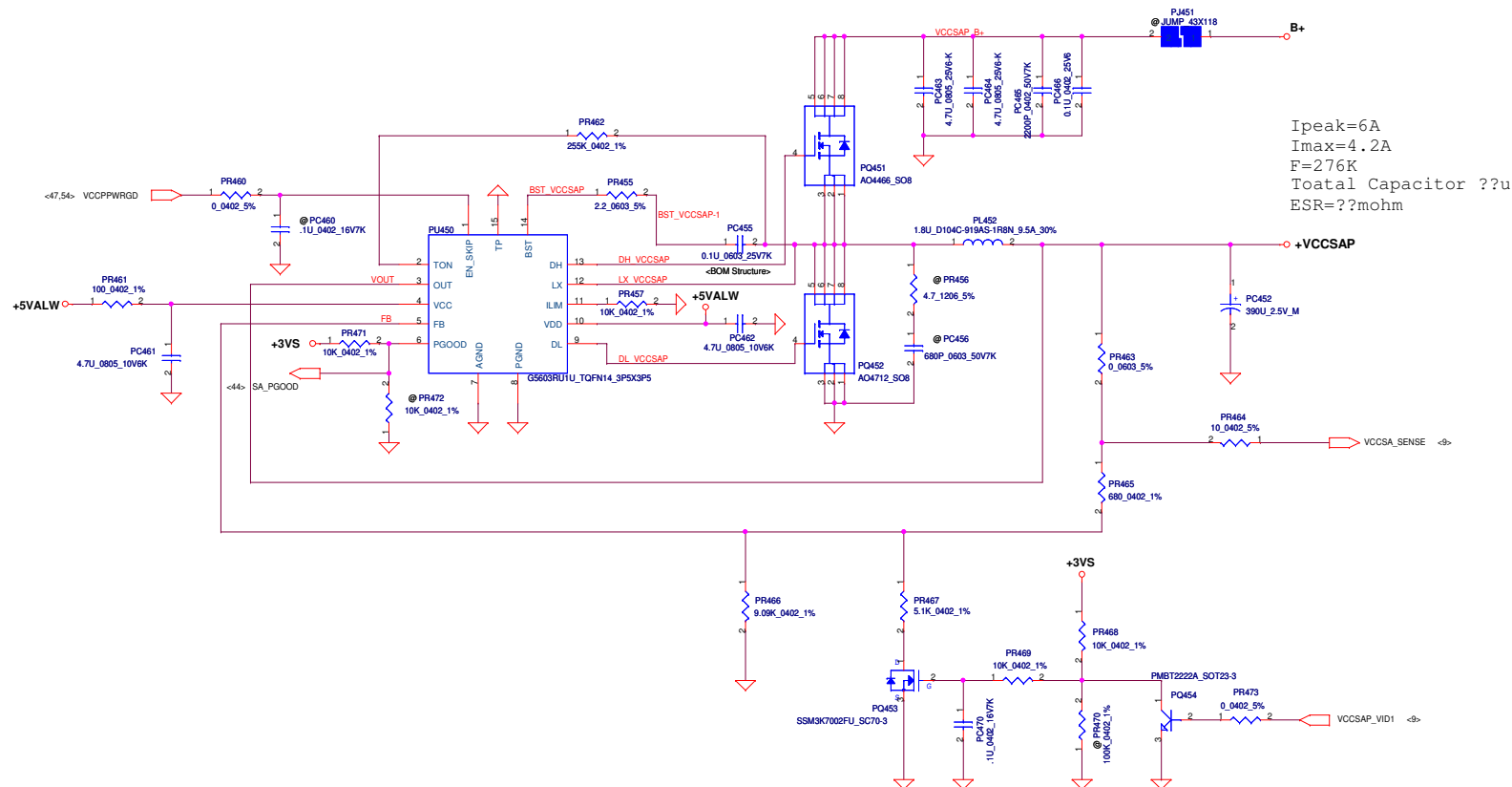
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CHARGER

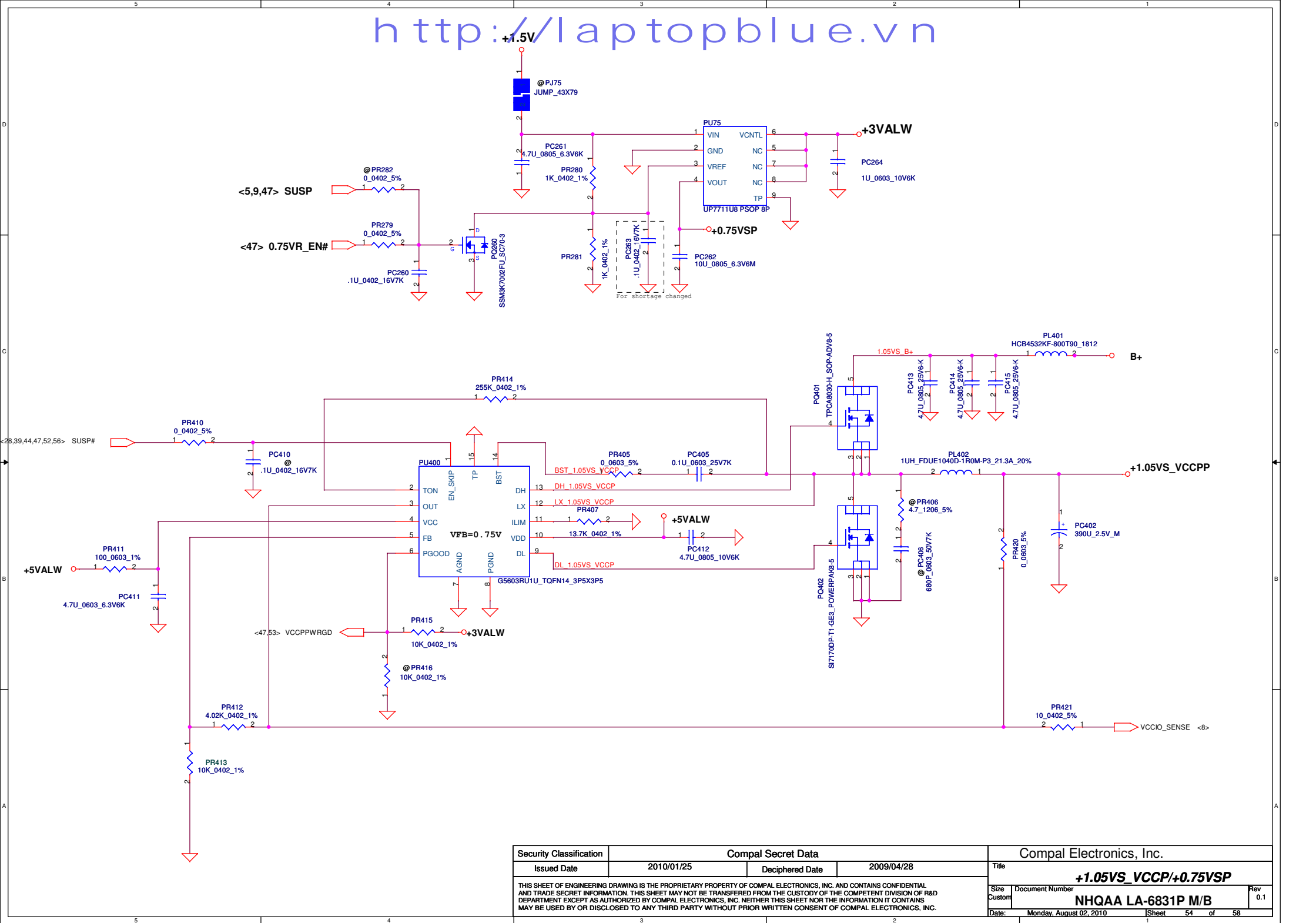
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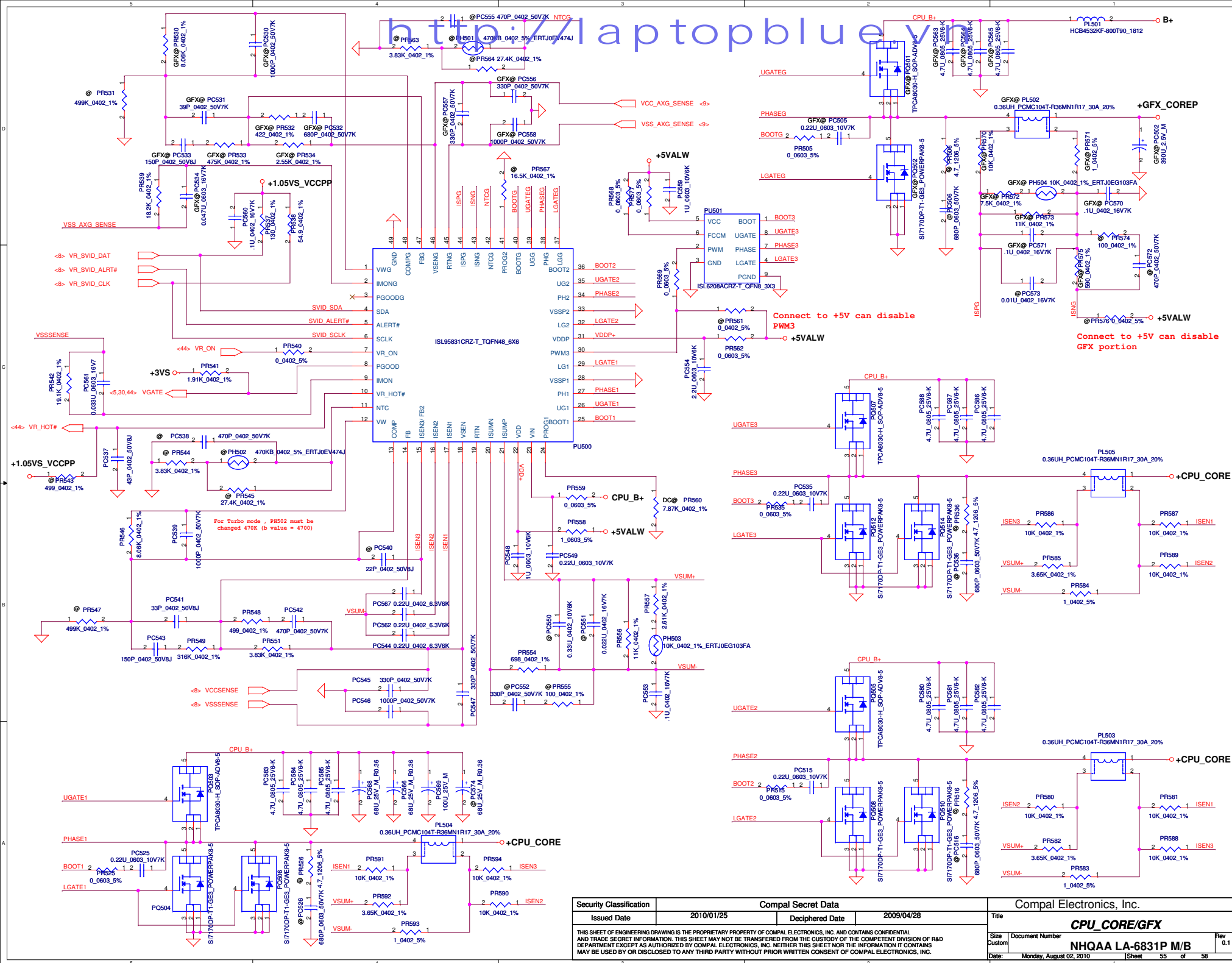




Ipeak=6A
Imax=4.2A
F=276K
Toatal Capacitor ??u
ESR=??mohm

VID1	+VCCSAP
1	0.8V
0	0.9V





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		58			

HW PIR (Product Improve Record)

NWQAA LA-6062P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2
GERBER-OUT DATE: 2009/12/30
NO DATE PAGE MODIFICATION LIST

PURPOSE

http://laptopblue.vn

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