

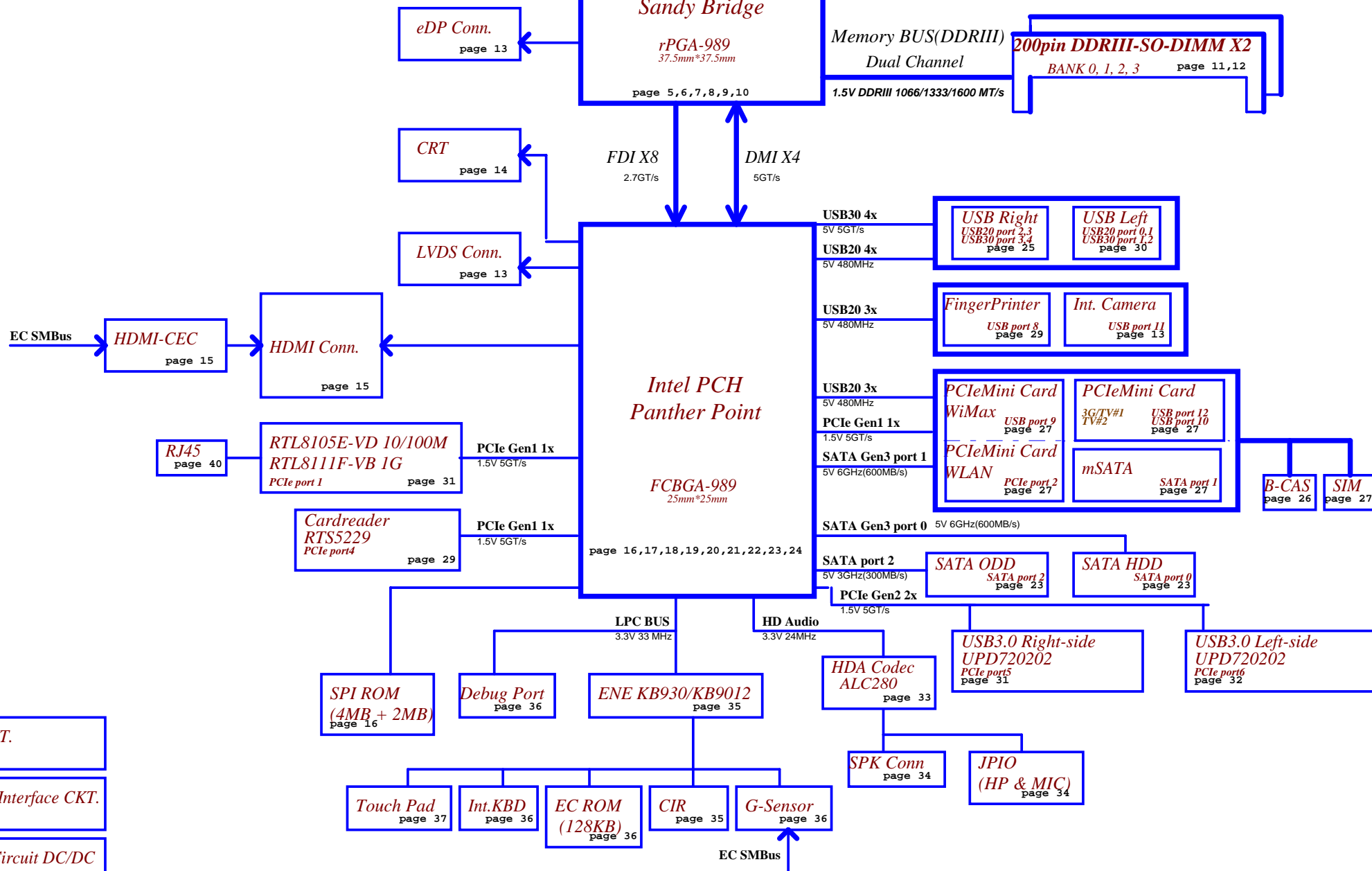
QFKAA

Yosemite 10F

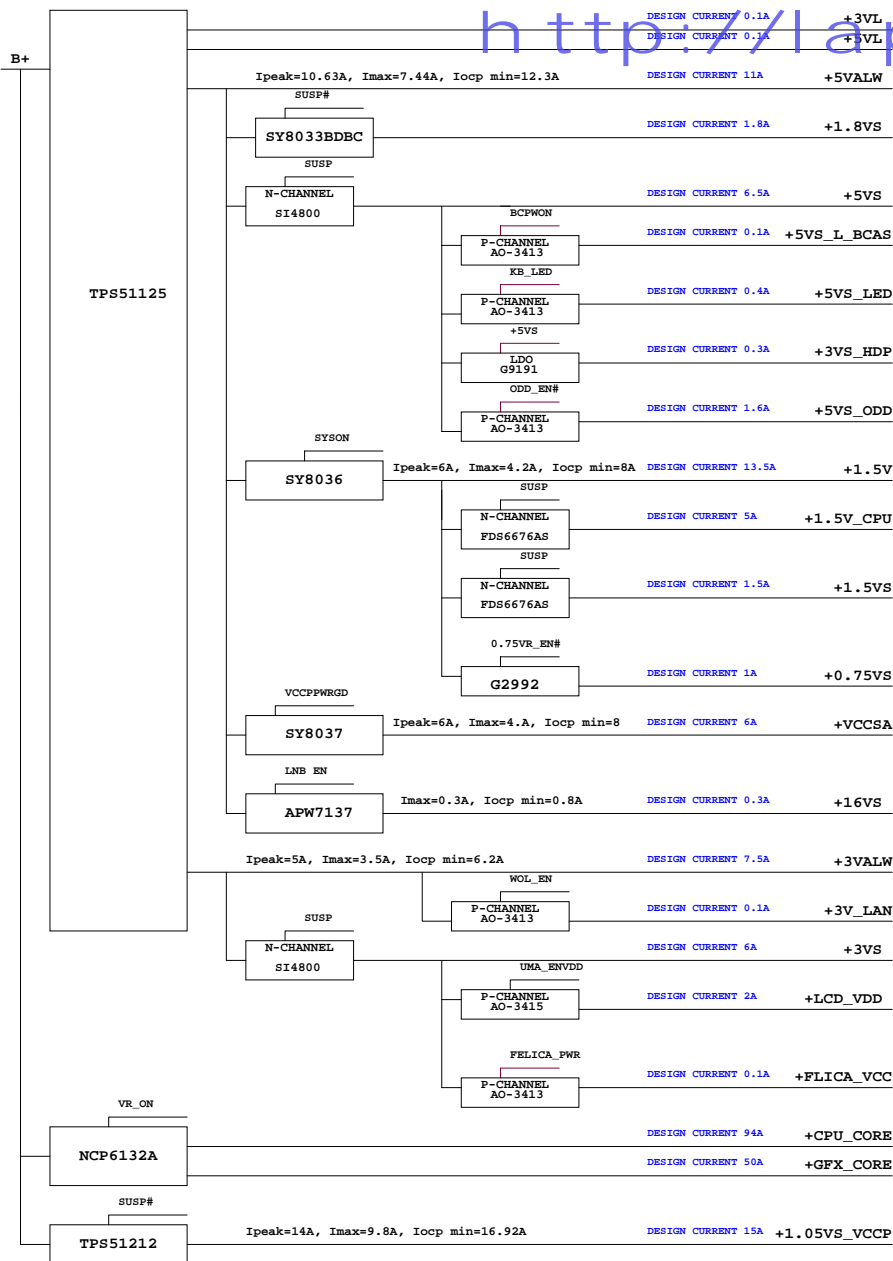
LA-8392P REV 1.0 Schematic

Intel Processor(Ivy Bridge / Sandy Bridge)
PCH(Panther Point)
2012-02-06 Rev 1.0

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9A H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b

BTO Option Table

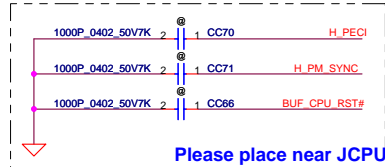
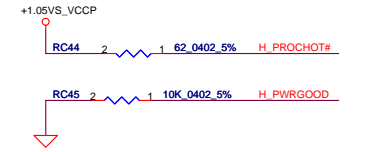
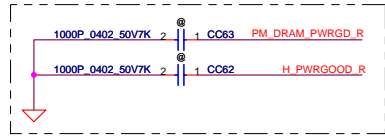
Function	HDMI		Internal Display Port		CPU		KB Light
description	HDMI		Internal Display Port		Sandy Bridge	Ivy Bridge	KB Light
explain	HDMI	CEC	LVDS	EDP	Sandy Bridge	Ivy Bridge	KB Light
BTO	HDMI@	CEC@	LVDS@	IEDP@	SANDY@	IVY@	KBL@

Function	MINI PCI-E SLOT					LAN		Fingerprint	CIR
description	SLOT2				SLOT1	LAN		Fingerprint	CIR
explain	3G	TV Tuner	BCAS	mSATA	WIMAX	10/100M	Giga	Fingerprint	CIR
BTO	3G@	TV@	BCAS@	mSATA@	WIMAX@	8105ELDO@	8111FVB@	FP@	CIR@

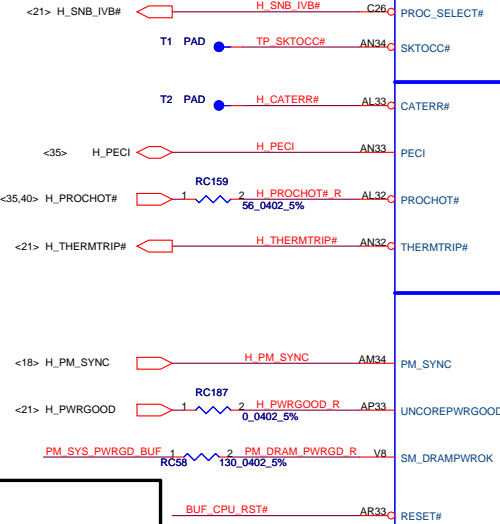
Function	SPI ROM	Green CLK		G-SENSOR	Sleep&Charge		USB 3.0		Camera & Mic
description	SPI ROM	Green CLK		G-SENSOR	Sleep&Charge		USB 3.0		Camera & Mic
explain	WIN8	Green CLK	NOGCLK	G-SENSOR	14600	14617	Internal	External	Camera & Mic
BTO	WIN8@	271@	NOGCLK@	GSENSOR@	14600@	14617@	IUSB30@	EUSB30@	CAM@

Function	USB Repeater			
description	USB Repeater			
explain	TIUR	PRUR		
BTO	TIUR@	PRUR@		

STATE	SIGNAL		
Full ON	SLP_S3#	SLP_S4#	SLP_S5#
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW



Please place near JCPU



TYCO_2013620-2_IVY BRIDGE

MISC

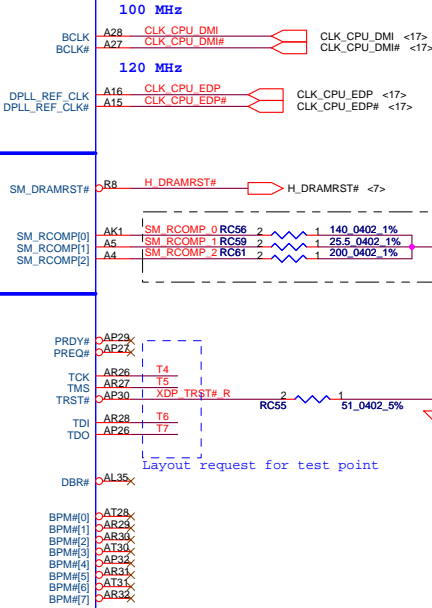
THERMAL

PWR MANAGEMENT

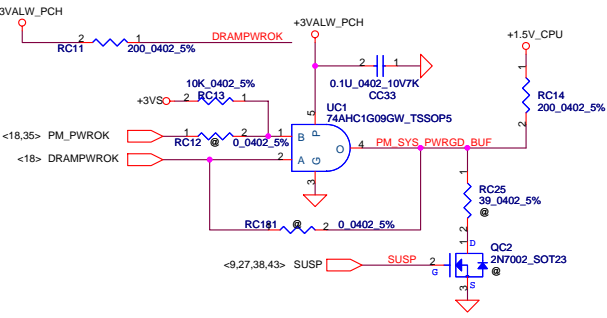
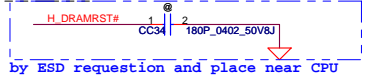
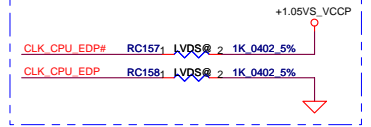
CLOCKS

DDR3 MISC

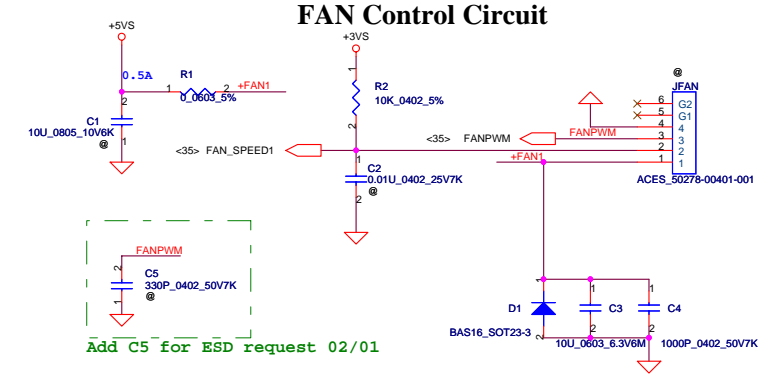
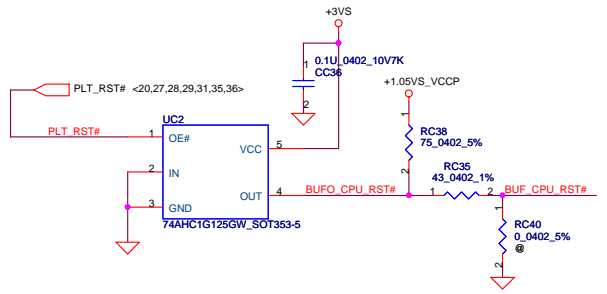
JTAG & BPM



Stuff R41 and R42 if do not support eDP

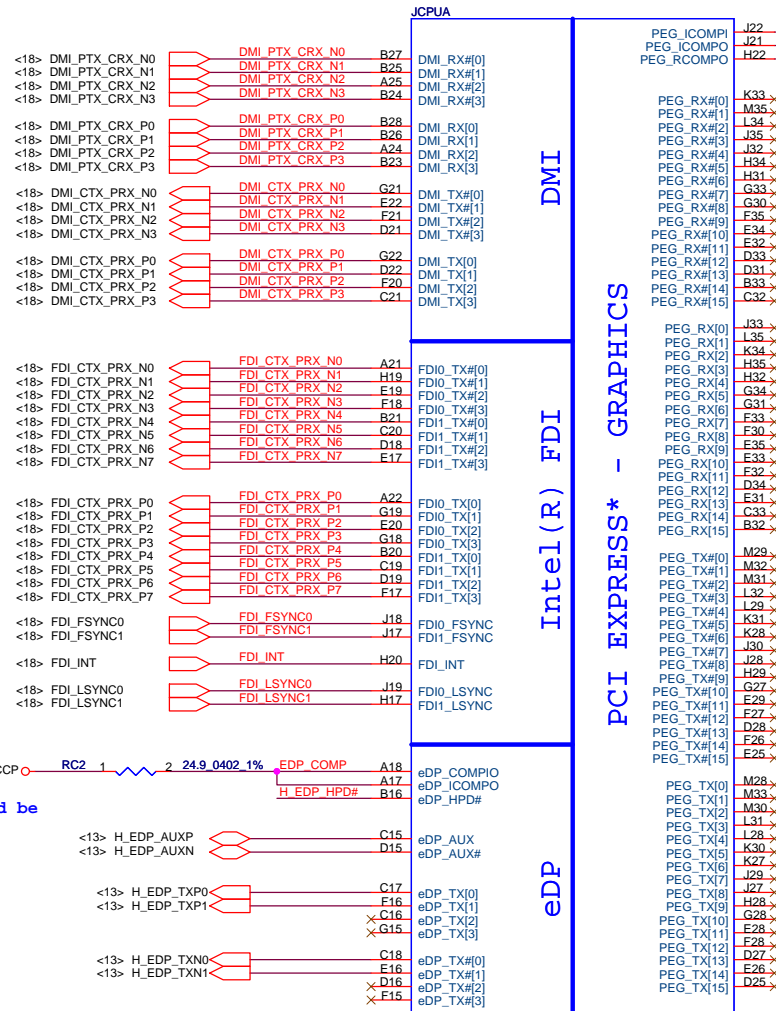


Buffered Reset to CPU

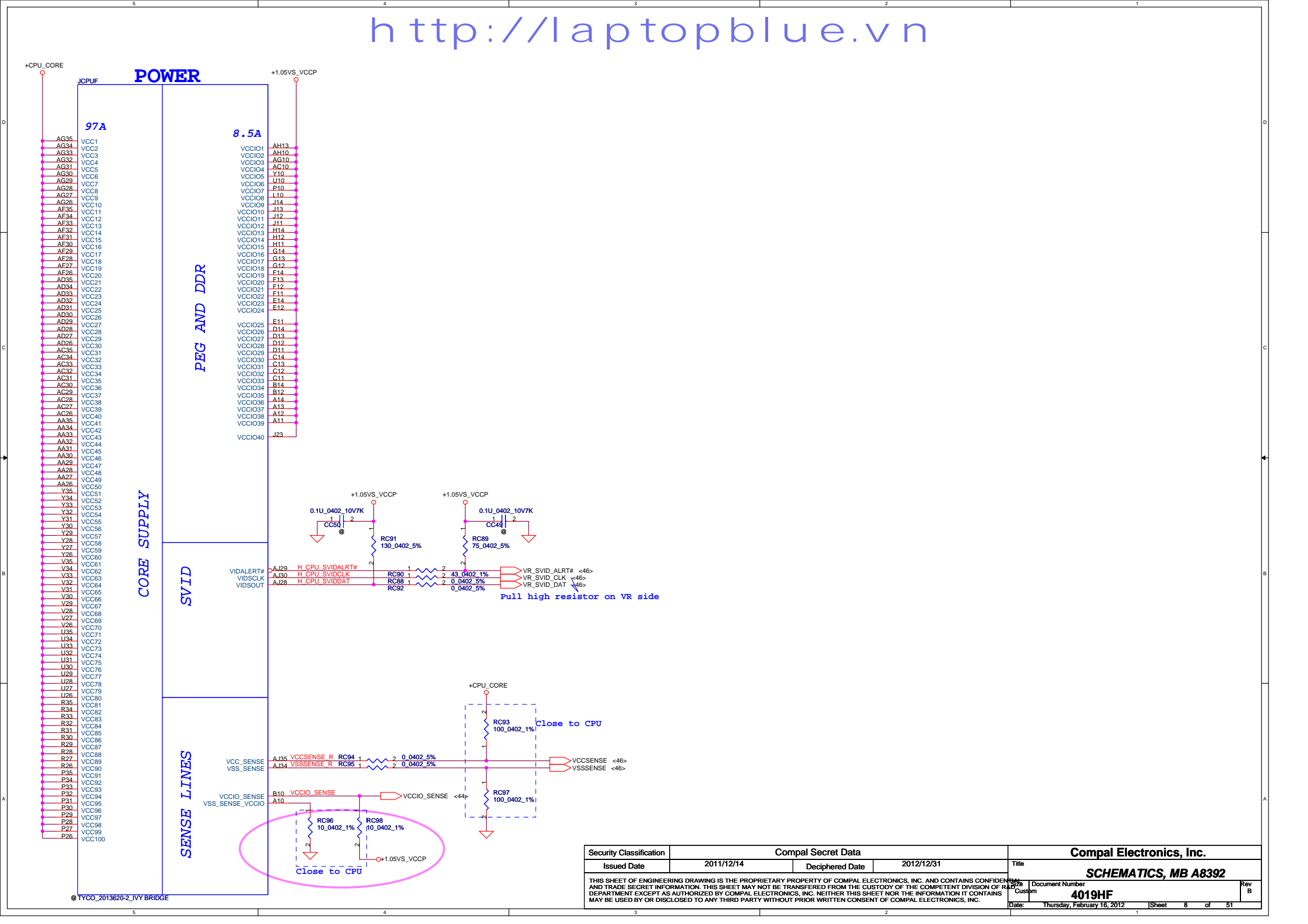


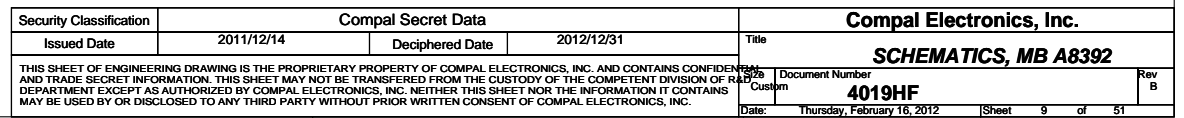
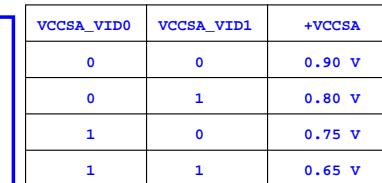
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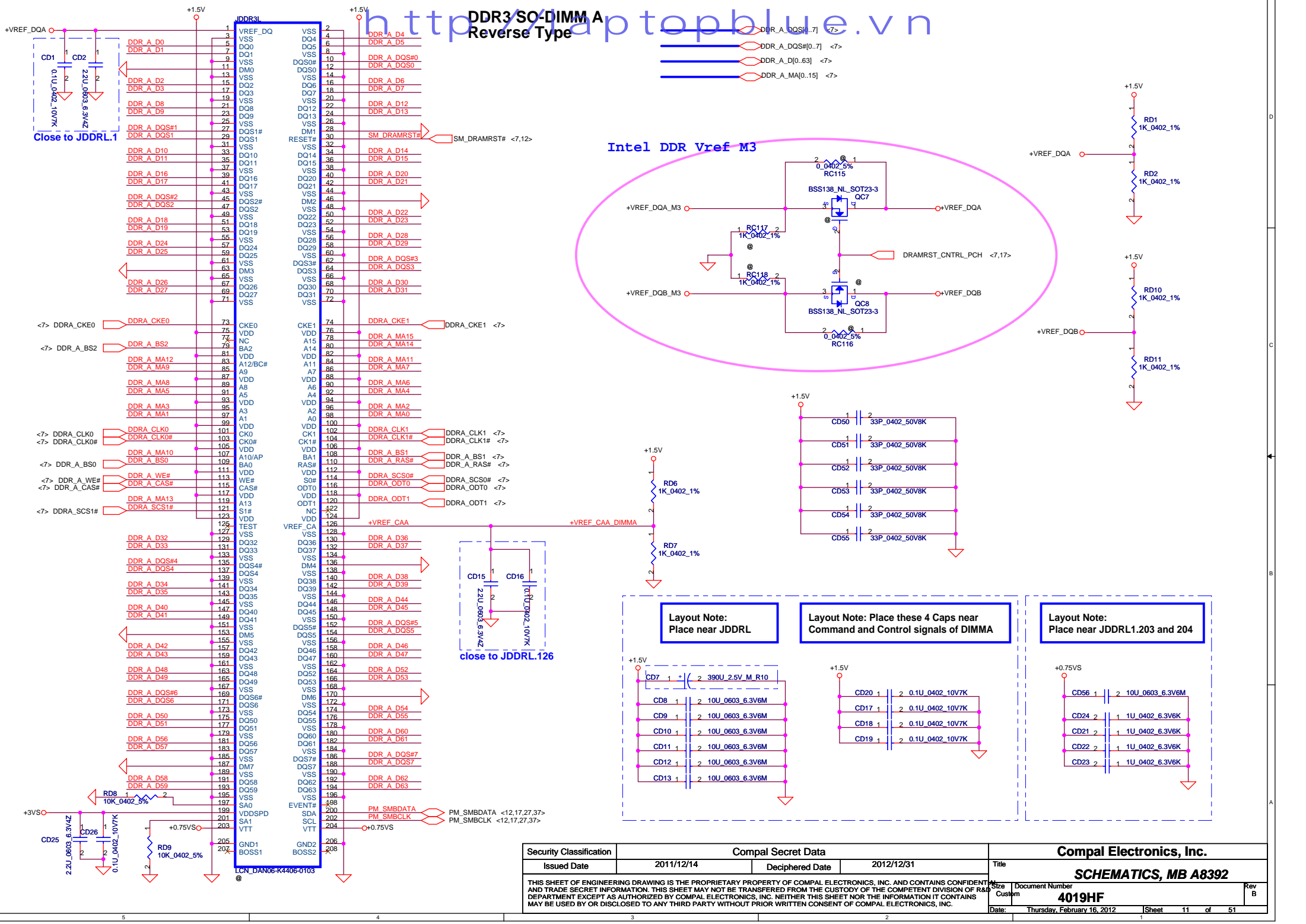
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)



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DDR3 SO-DIMM A Reverse Type

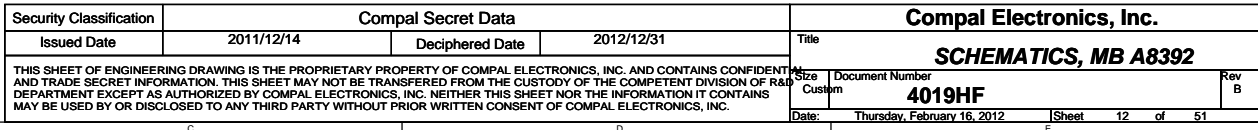
Intel DDR Vref M3

Layout Note:
Place near JDDR1

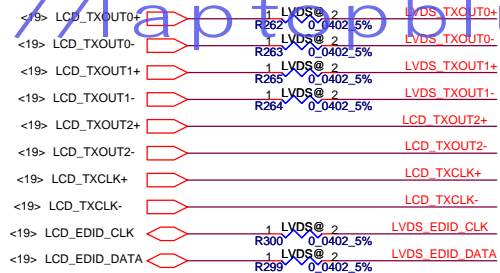
Layout Note: Place these 4 Caps near
Command and Control signals of DIMMA

Layout Note:
Place near JDDR1.203 and 204

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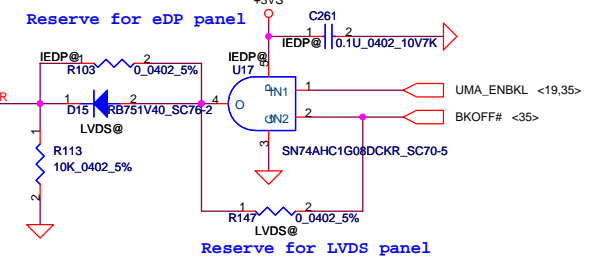
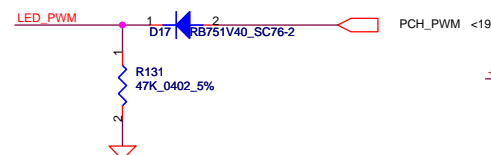
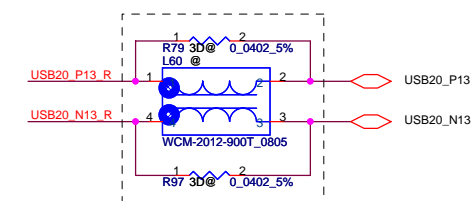
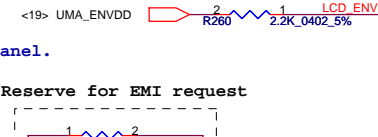
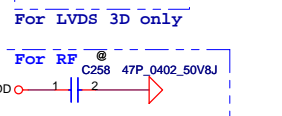
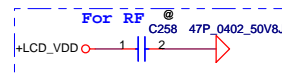
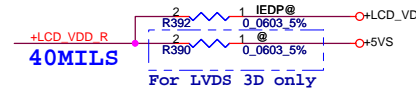


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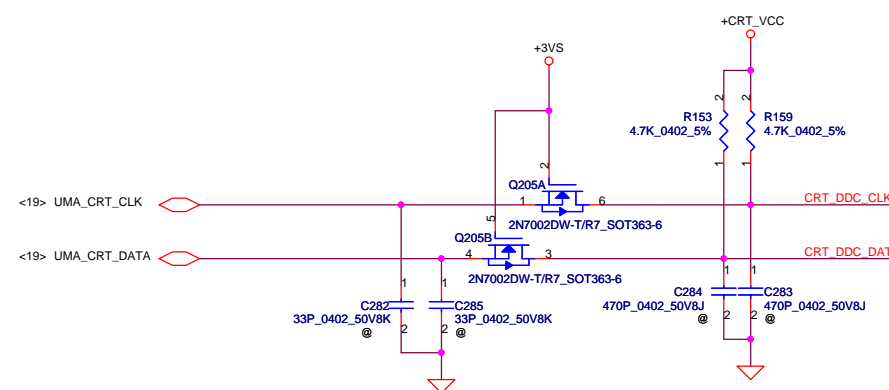
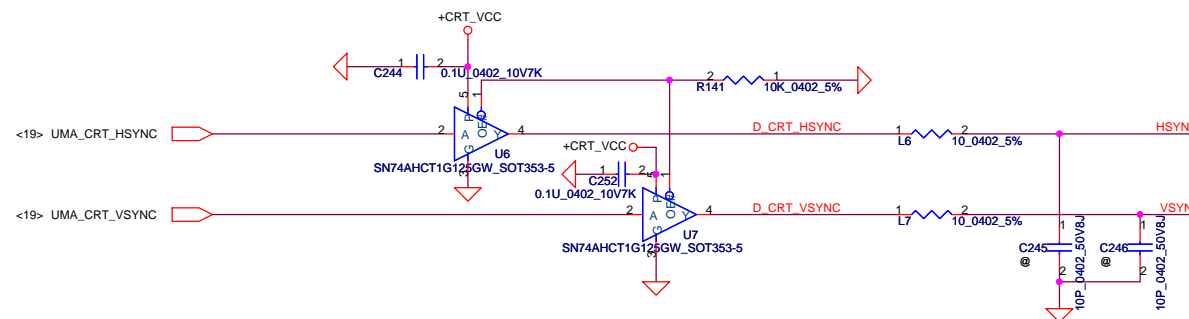
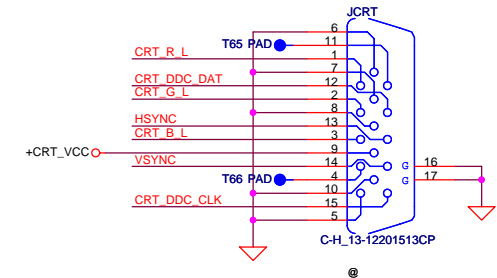
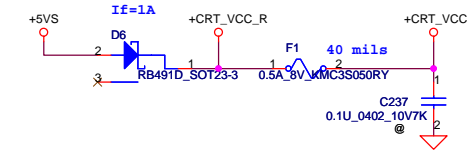
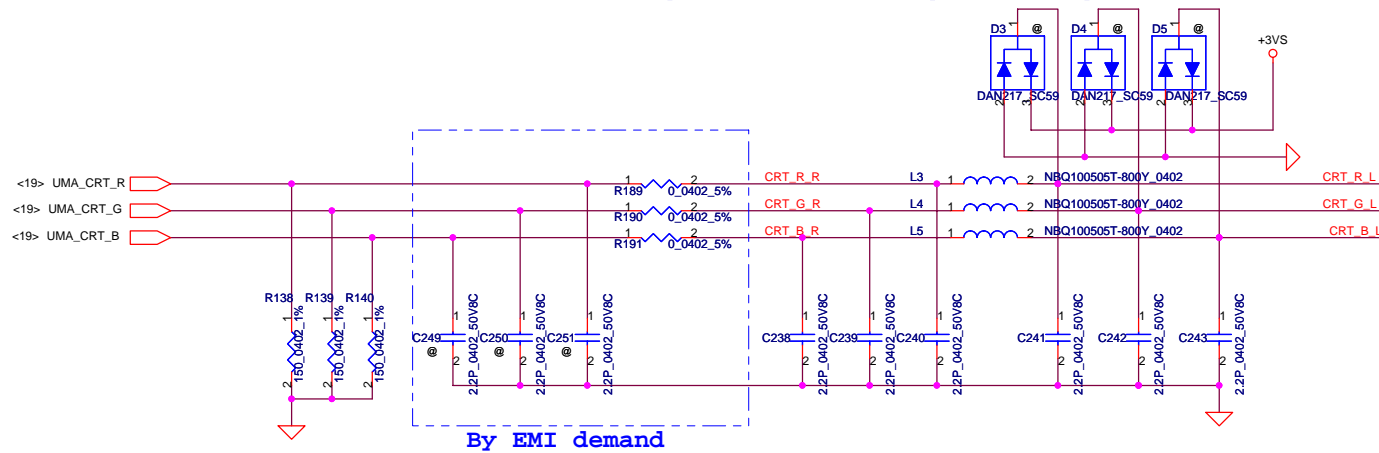
only need for 3D with DCDC/B
 ,JLVDS Pin8 can connect to
 +LCV_VDD directly for
 3D w/o DCDC/B

2 1 R1441 0.0603 5% +3VS
 2 1 R106 0.0603 5% +PANEL VDD +LCD_VDD



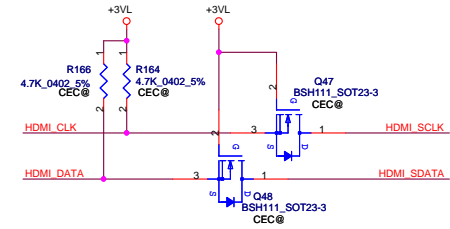
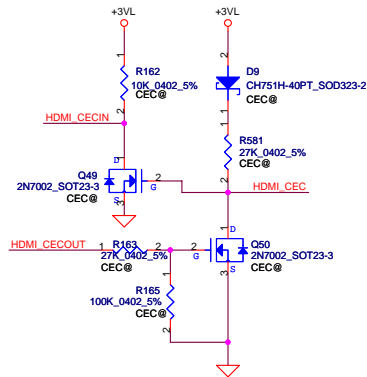
	LVDS cable MB side Pin 22	eDP cable MB side Pin 22
LVDS	GND	
eDP		NC

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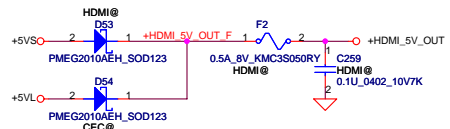
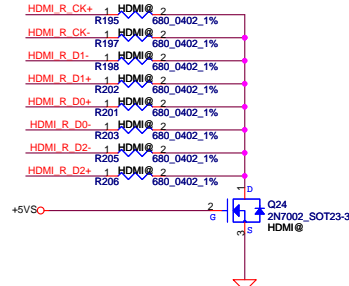
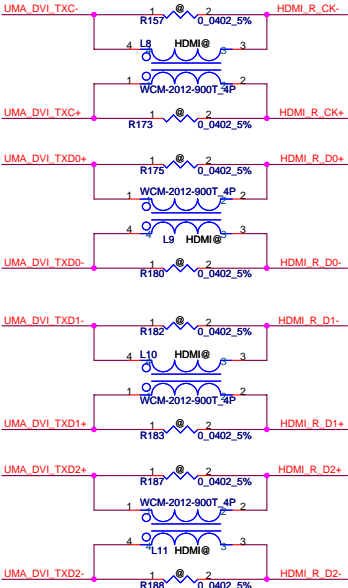
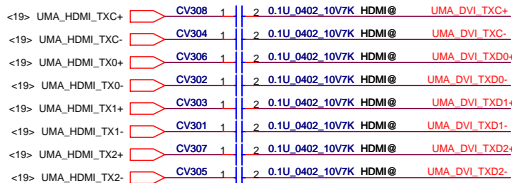
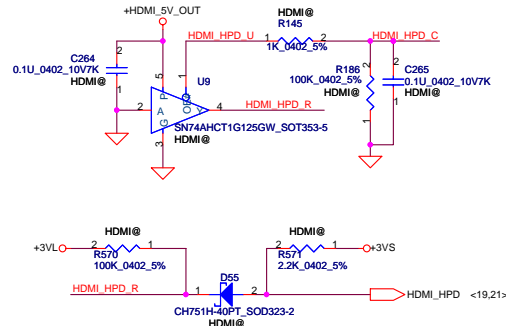
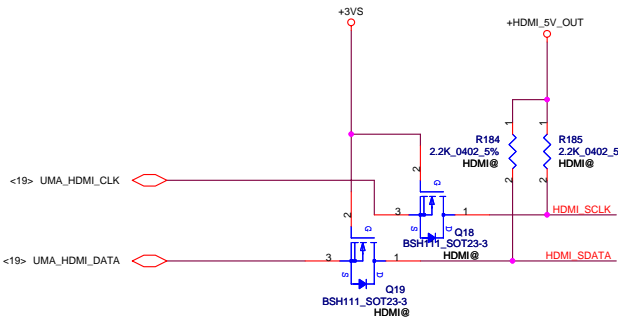
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HDMI CEC Controller

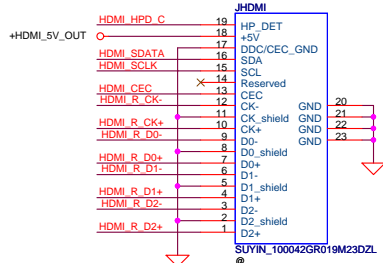


HDMI Royalty
RO0000003HM
HDMI W/Logo + HDCP

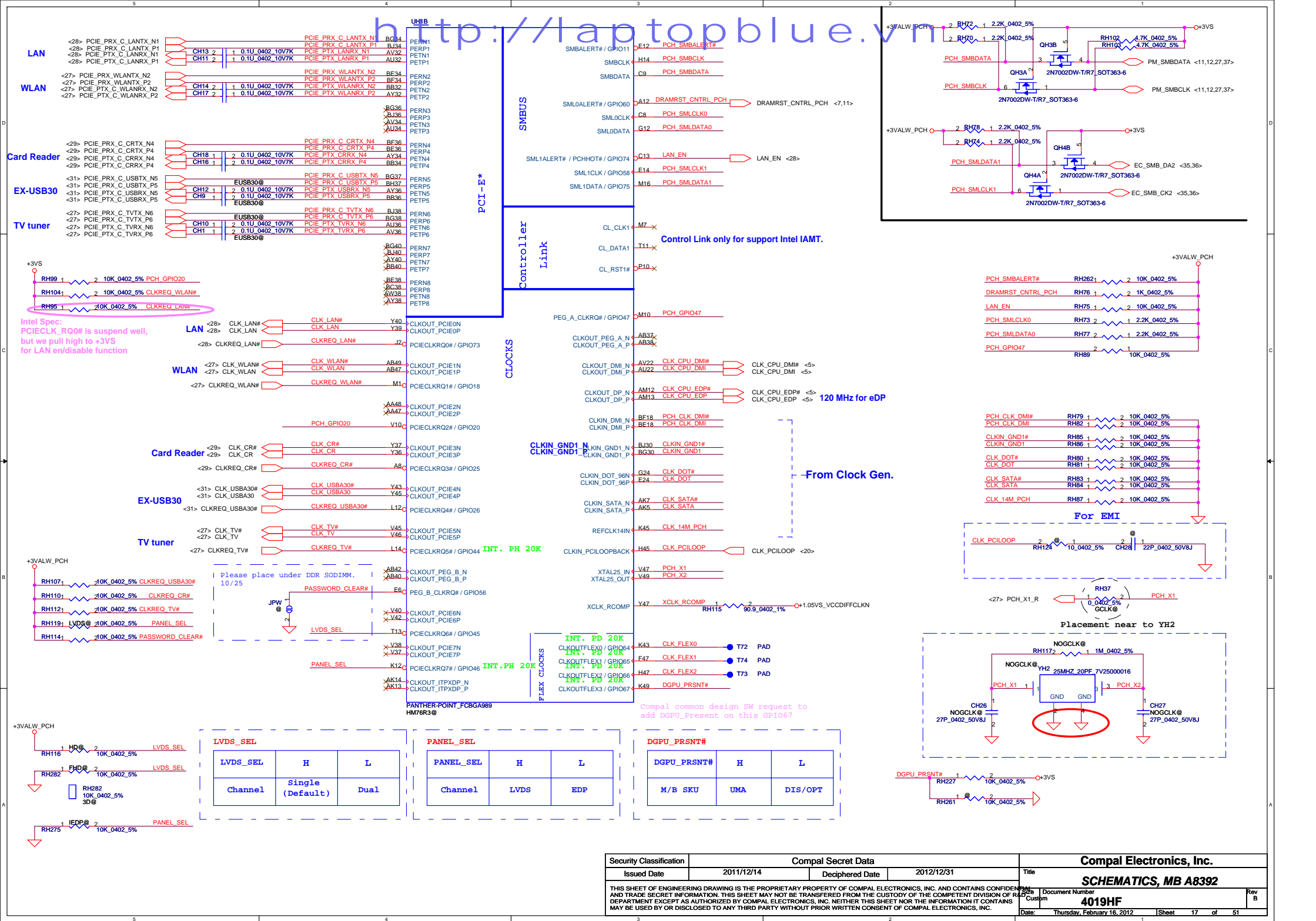
HDMI W/O Logo: RO0000001HM
HDMI W/Logo: RO0000002HM
HDMI W/Logo + HDCP: RO0000003HM



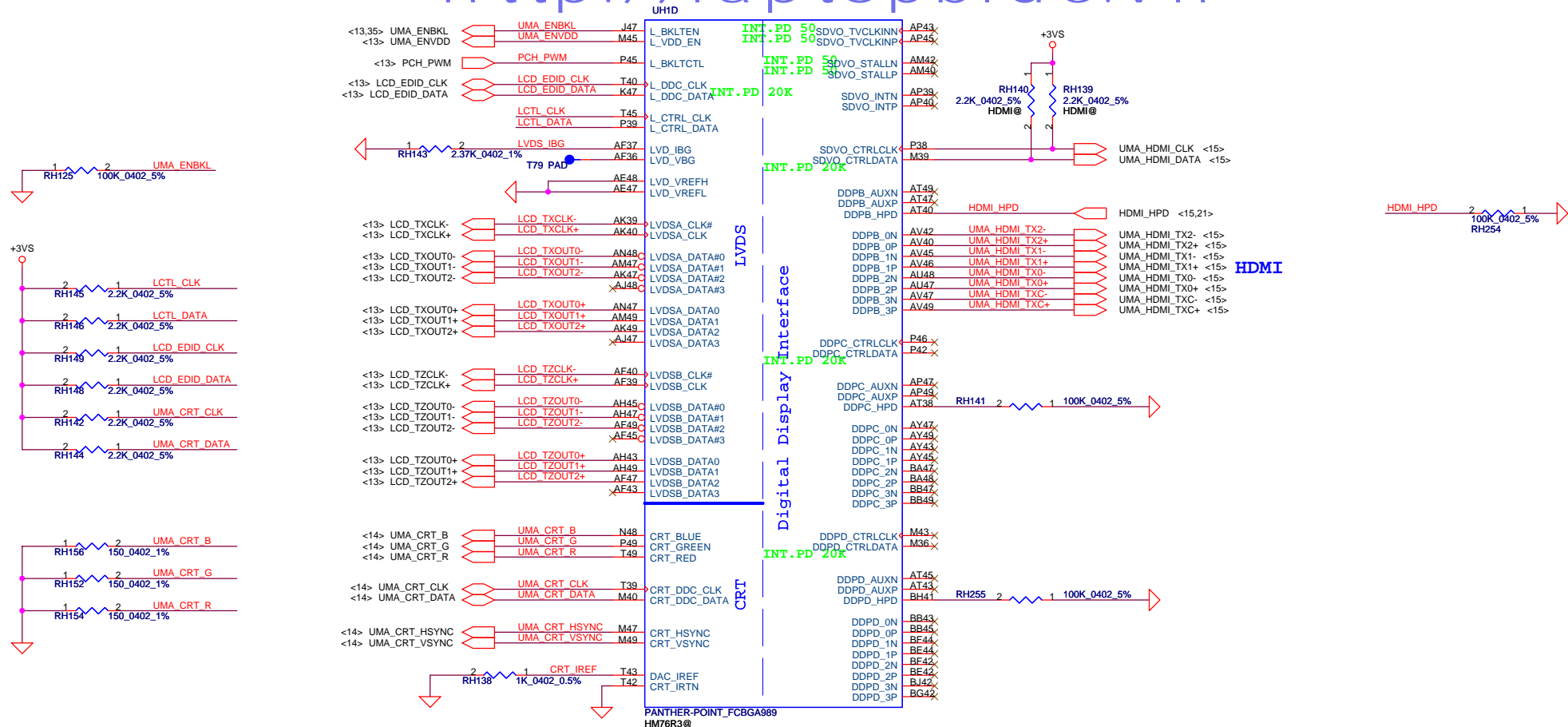
HDMI Connector



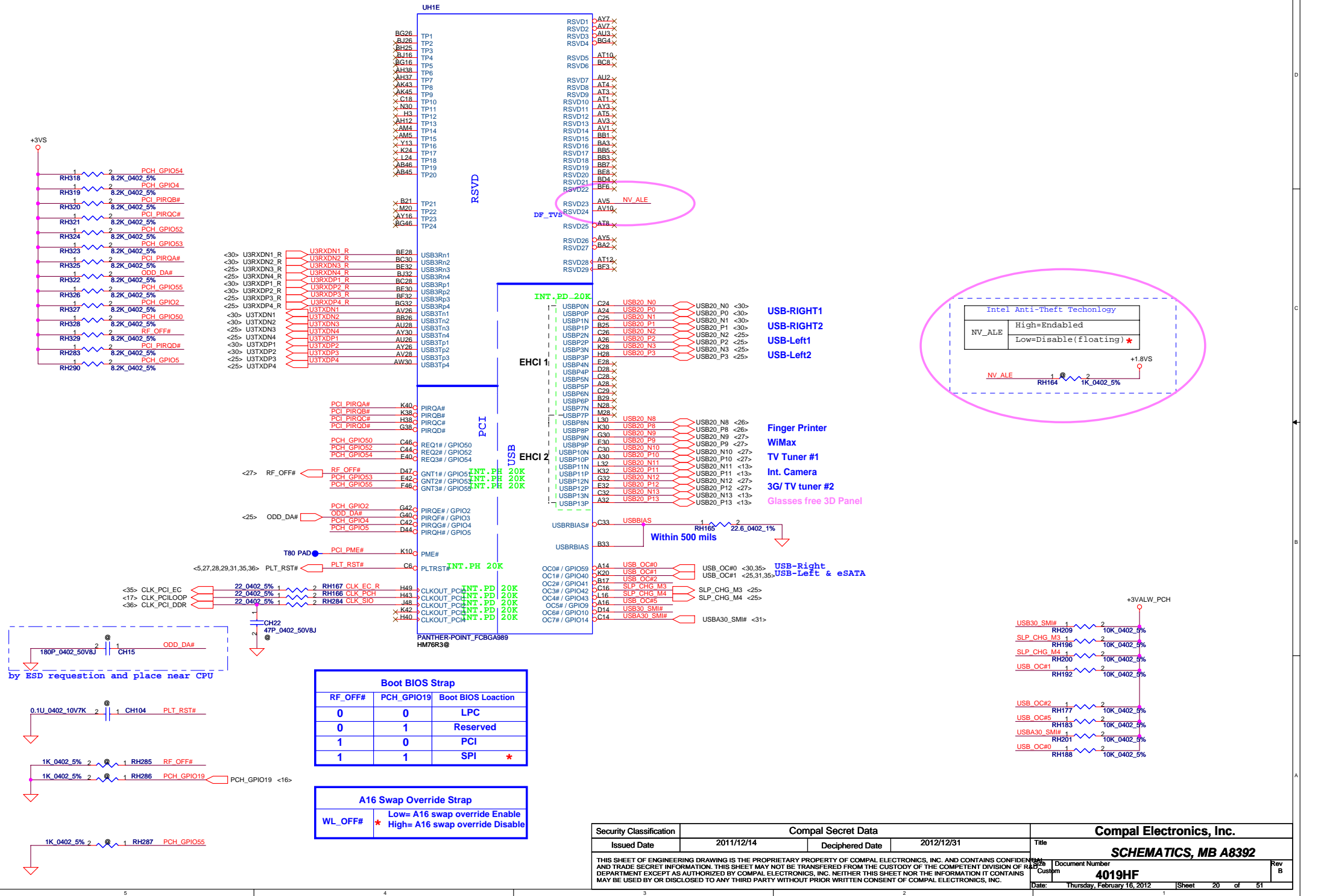
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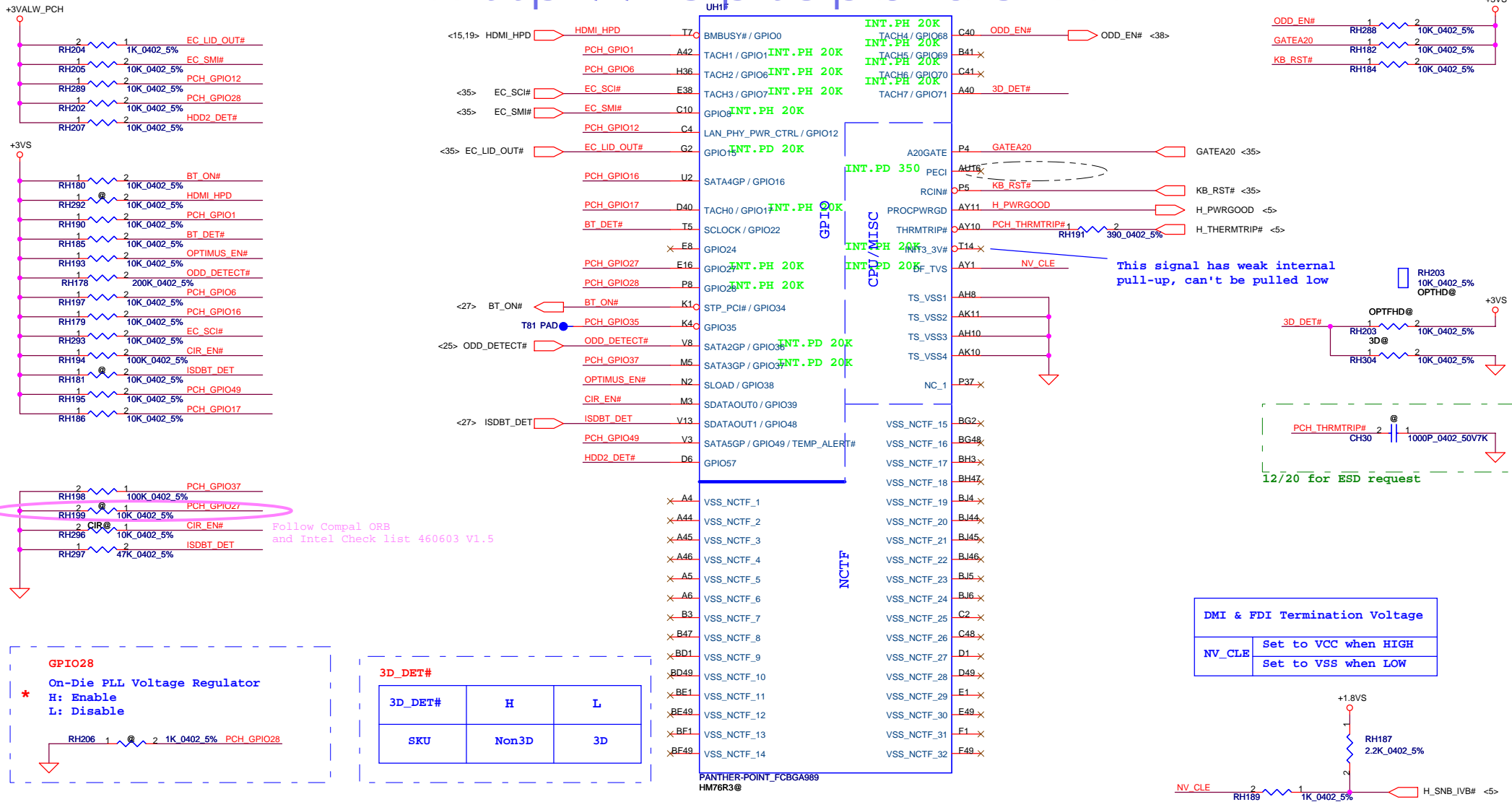


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GPIO28

*** On-Die PLL Voltage Regulator**
H: Enable
L: Disable

RH206 1 2 1K_0402_5% PCH_GPIO28

3D_DET#

3D_DET#	H	L
SKU	Non3D	3D

GPIO8

Integrated Clock Chip Enable (Removed)
H: Disable
*** L: Enable**

RH298 1 2 1K_0402_5% EC_SMI#

Integrated clock enable functionality is achieved by soft-strap
The current default is clock enable

OPTIMUS_EN#

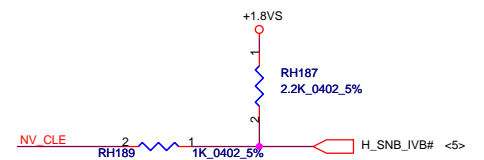
OPTIMUS_EN#	H	L
SKU	NonOPT	Optimus

HDD2_DET#

HDD2_DET#	H	L
SKU	ONE HDD	TWO HDD

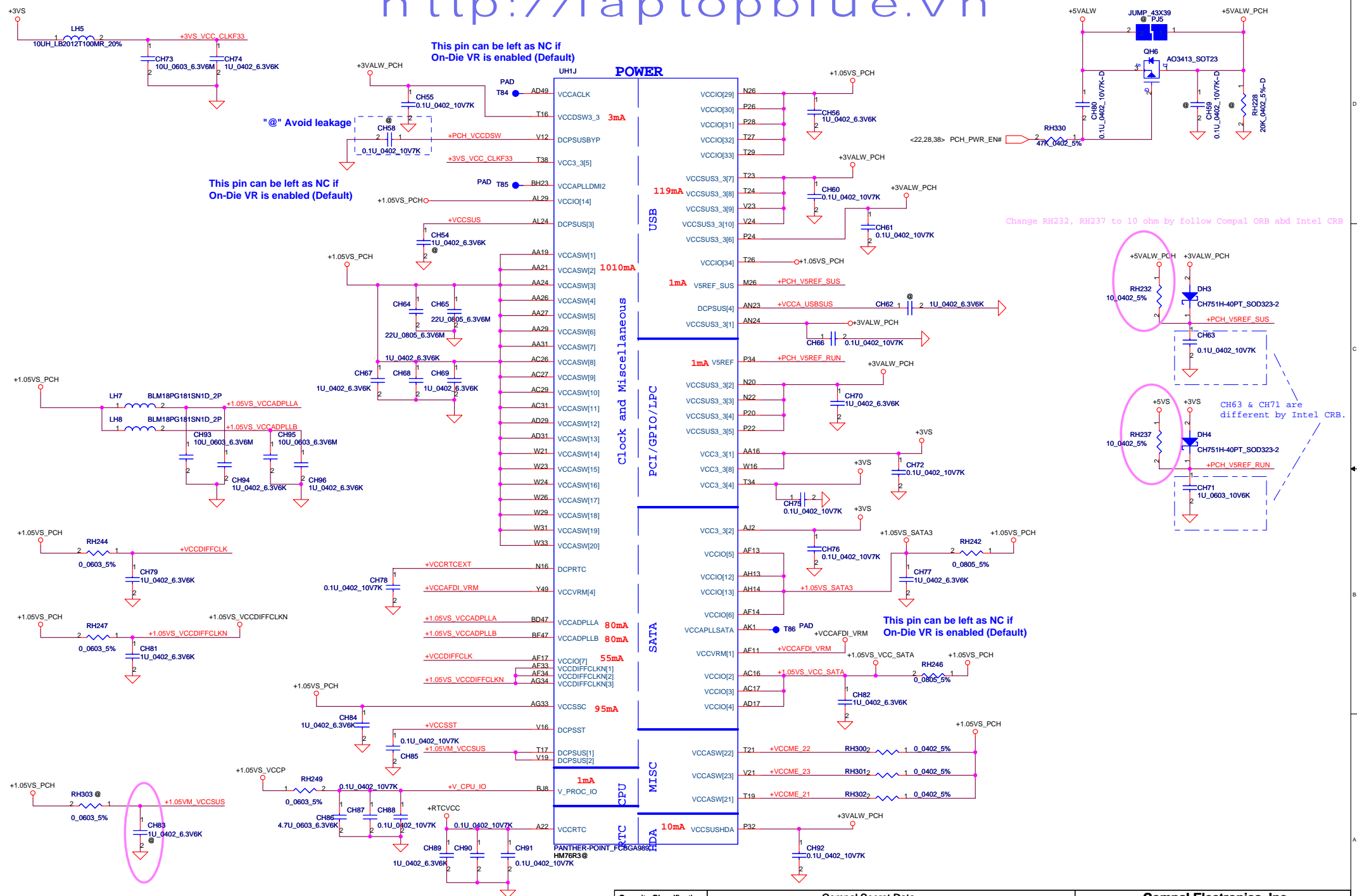
DMI & FDI Termination Voltage

NV_CLE	Set to VCC when HIGH Set to VSS when LOW
--------	---

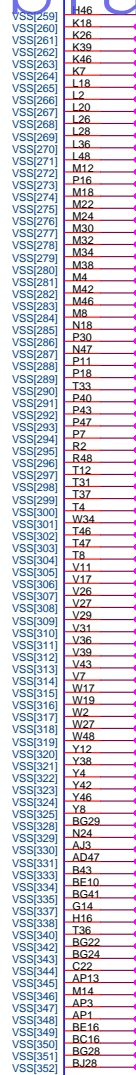
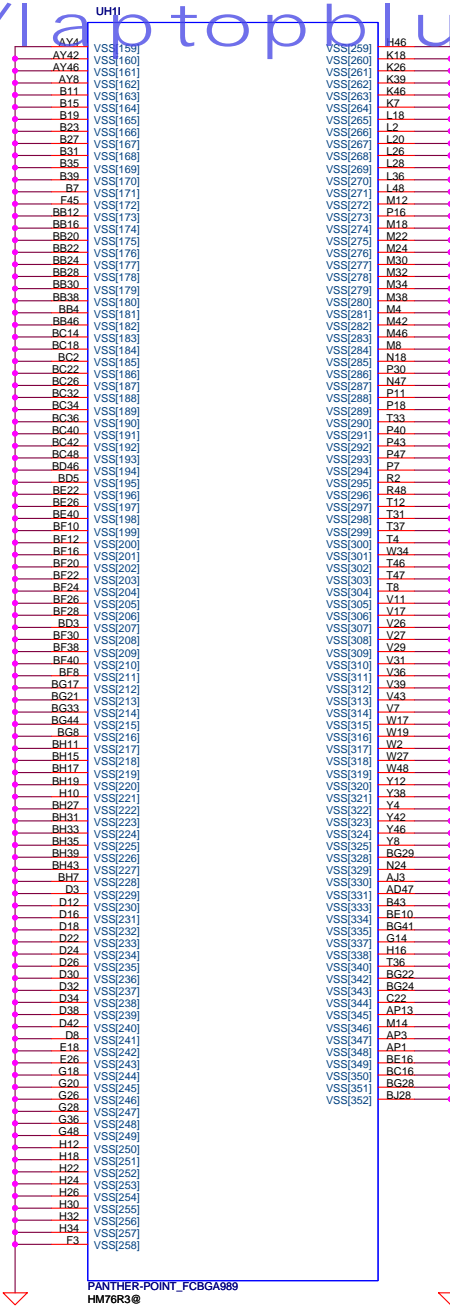
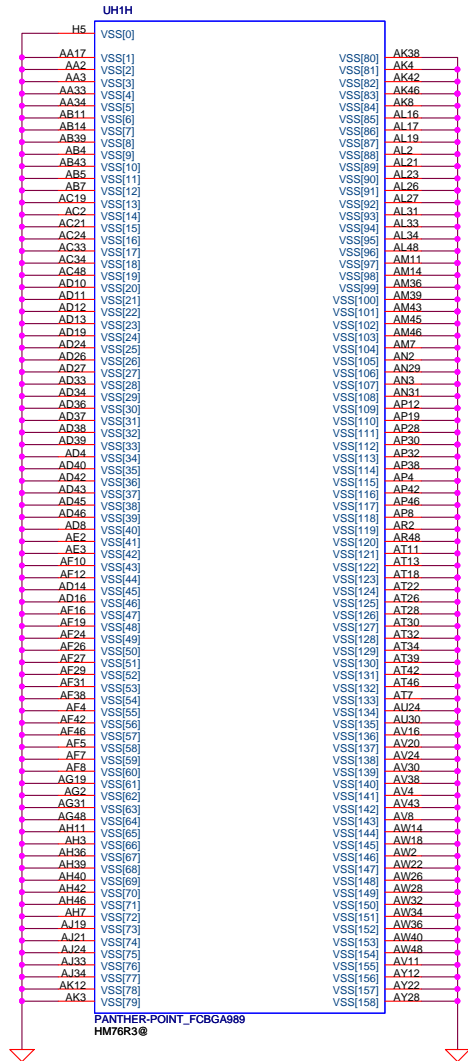


[illegible]

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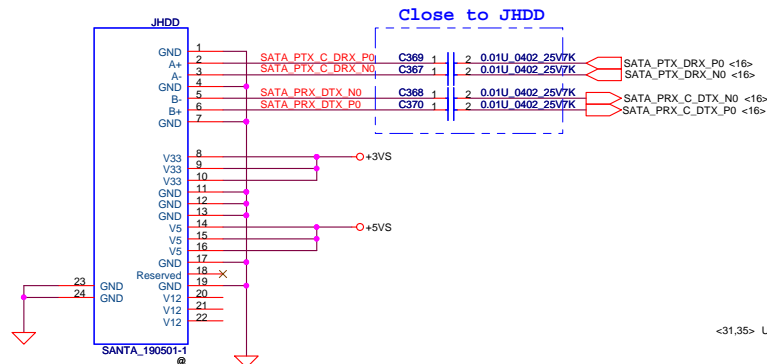
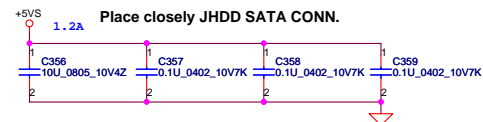


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				Doc Number	4019HF		Rev	8
				Date:	Thursday, February 16, 2012	Sheet	23	of

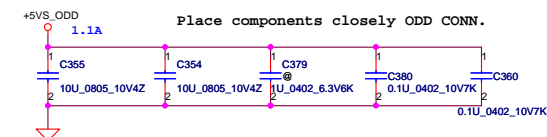
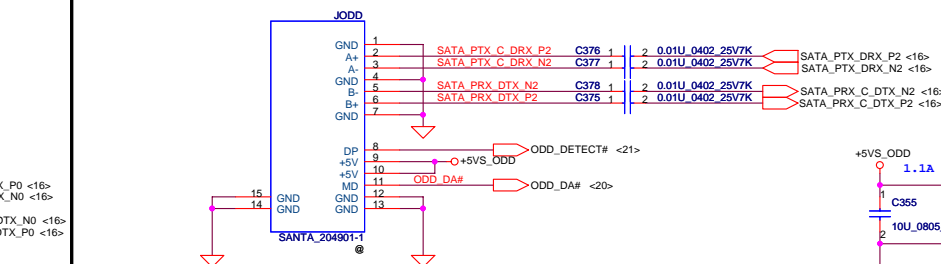


**SATA HDD
Conn.**

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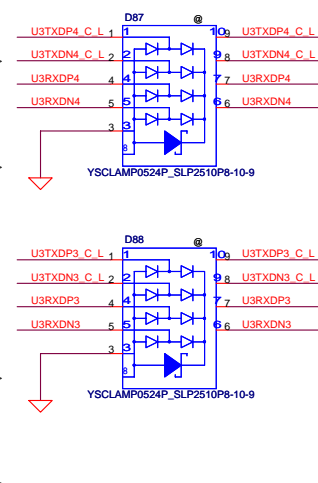
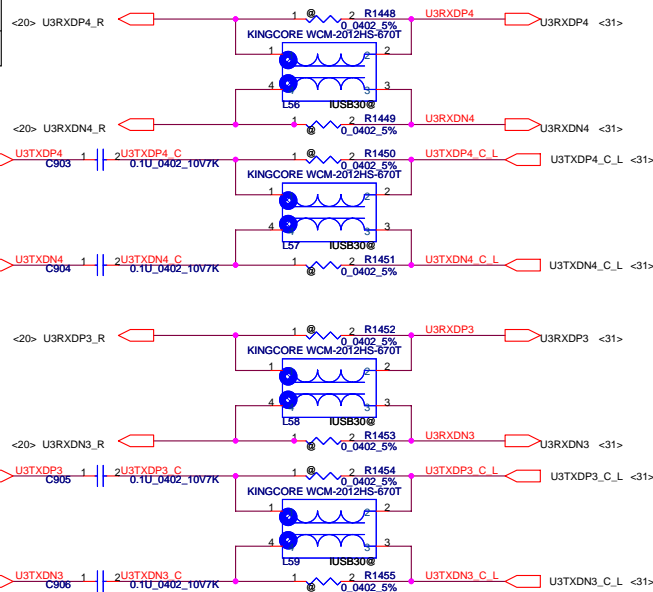
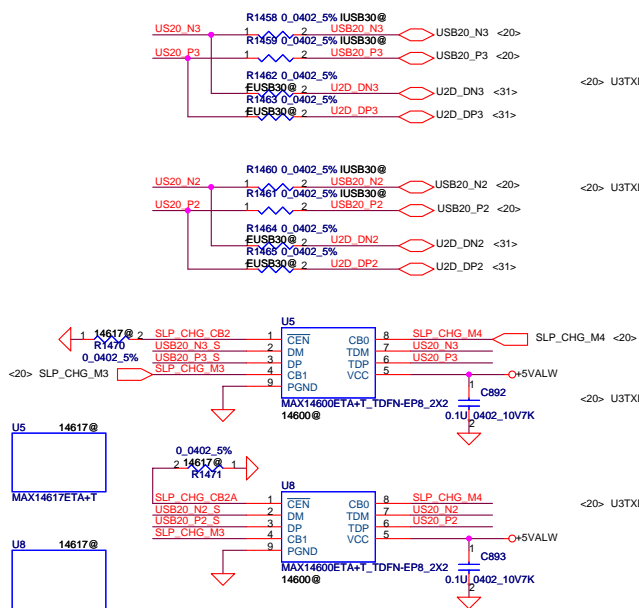
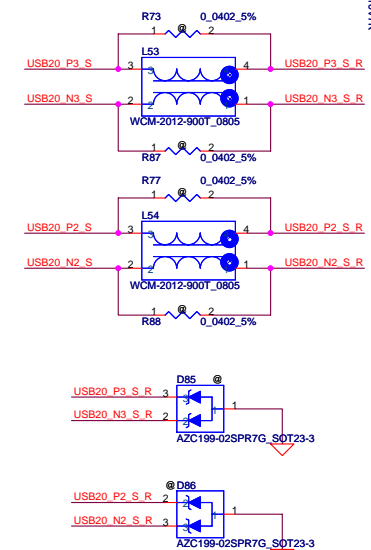
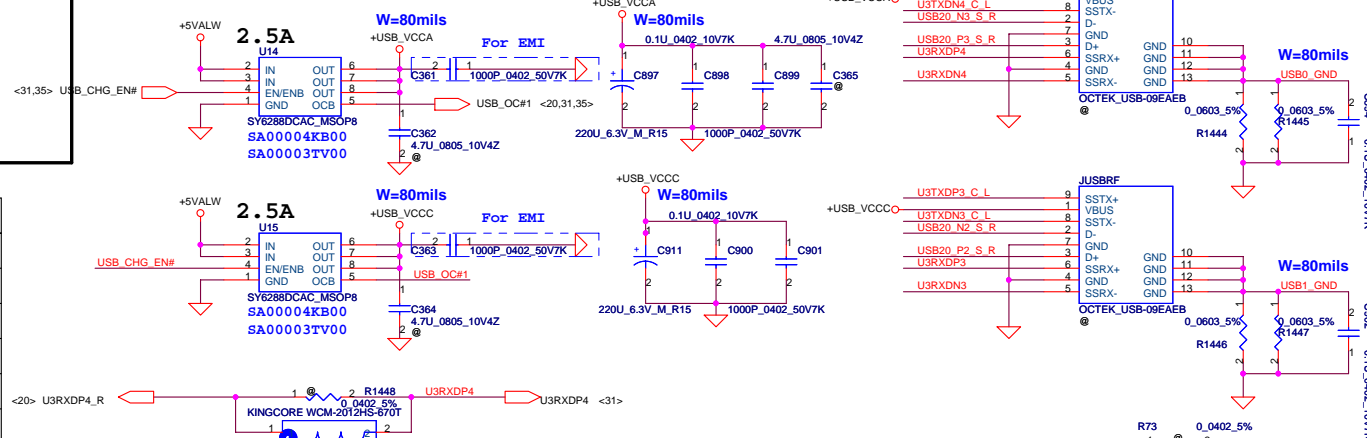


USB Right-Side



USB Sleep & Charge Auto-Mode/Mode3

MAX14600 & MAX14617			
CB0 SLP_CHG_M4	CB1 SLP_CHG_M3	CB2 (14617 only)	STATUS
0	0	0	AUTO MODE
0	1	0	Force Dedicated charger mode (MODE3)
1	0	0	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM
1	1	0	Pass-Through (USB) Mode with CDP Emulation: Auto Connect DP/DM to TDP/TDM depending on CDP status
X	X	1	Force Apple 2A Charger Mode: Apple 2A resistor dividers

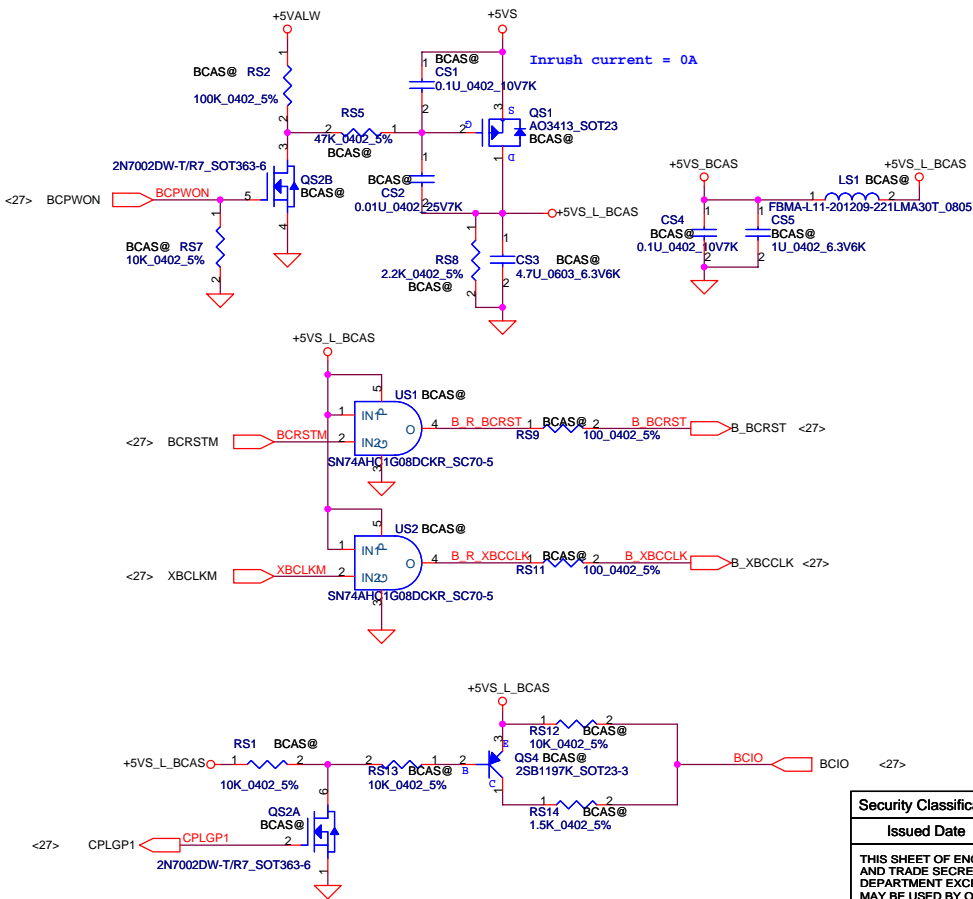


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				4019HF		
Date:	Thursday, February 16, 2012	Sheet	25	of	51	

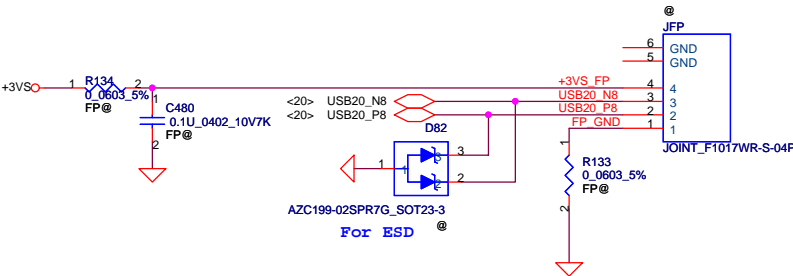
Screw cap for ESD request

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B-CAS Circuit

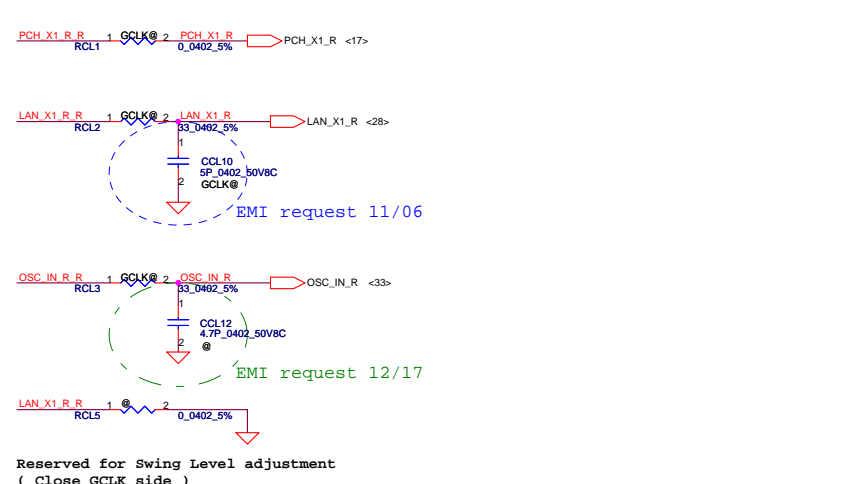
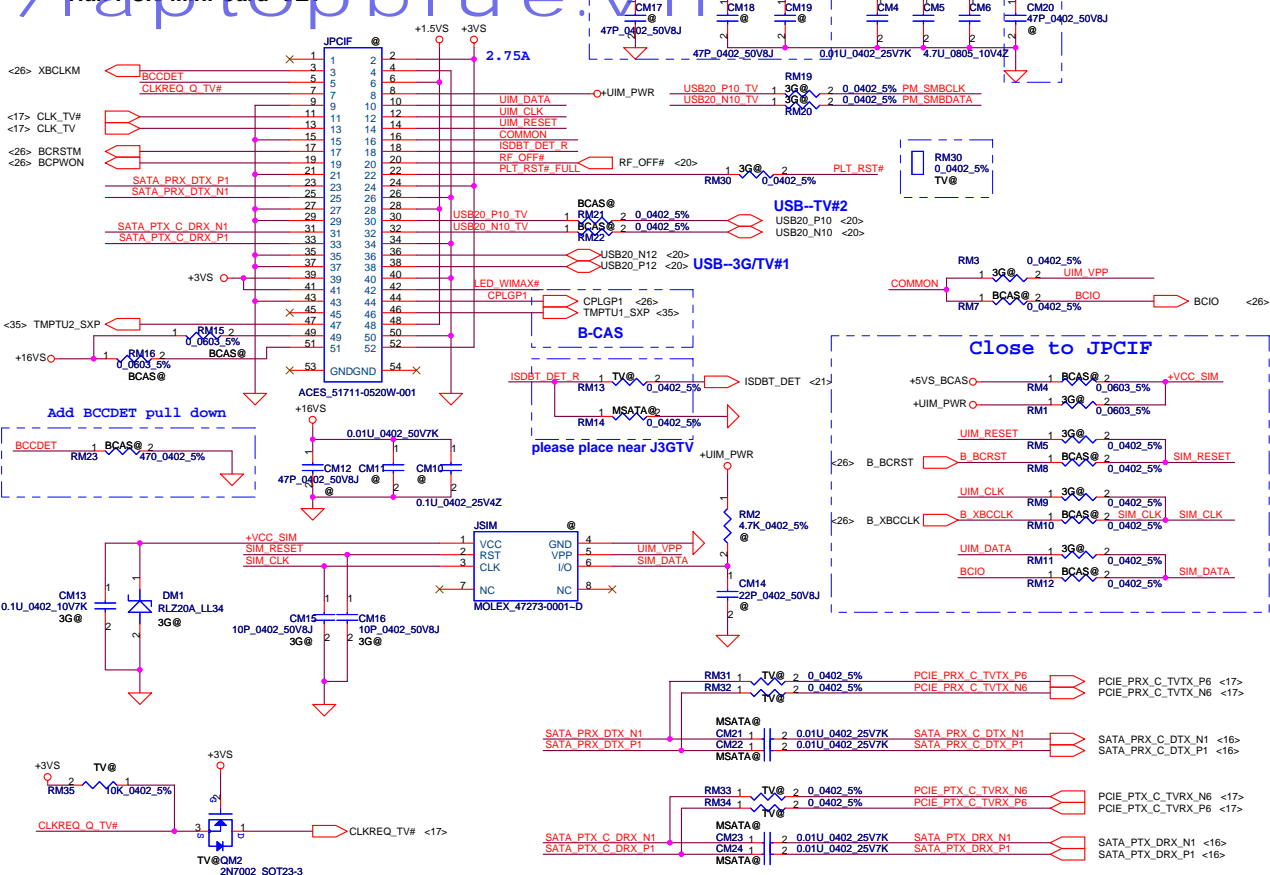


Finger printer

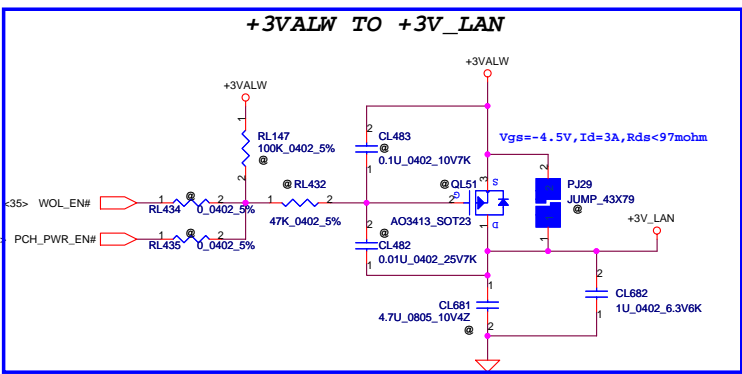
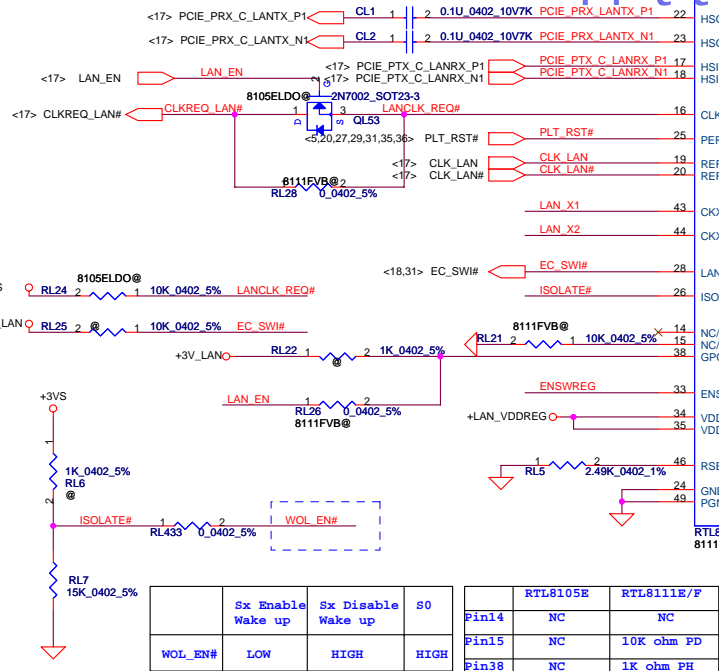


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								Size	Document Number	Rev
								4019HF		B
								Date:	Thursday, February 16, 2012	Sheet

Slot 2 Full PCIe Mini Card- 3G/ TV Tuner
Half PCIe Mini Card- JET



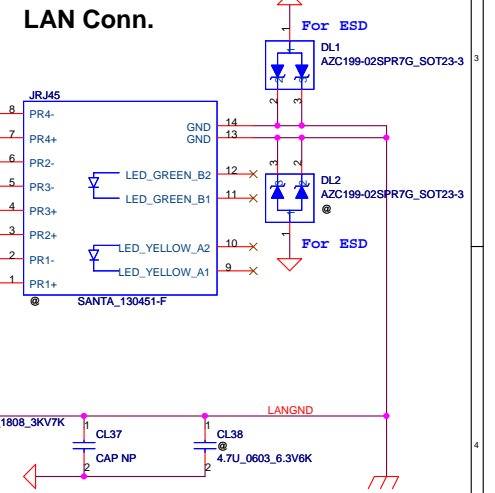
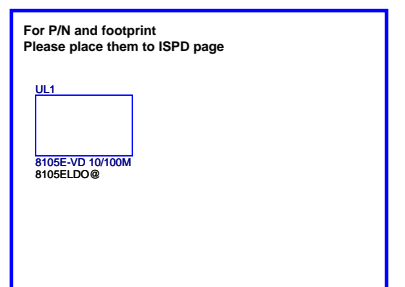
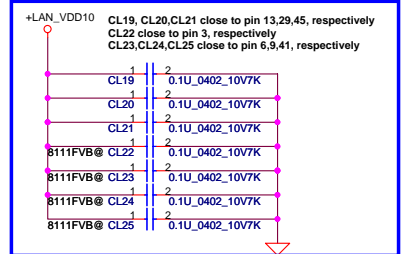
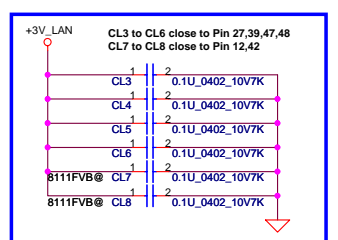
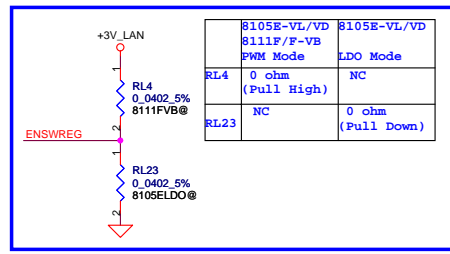
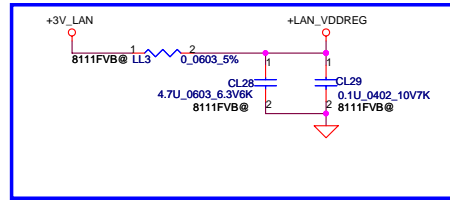
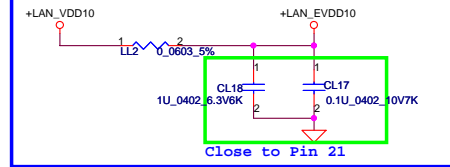
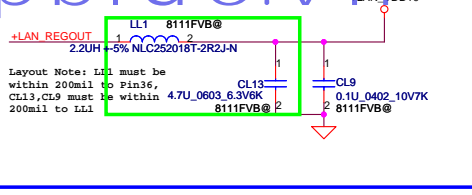
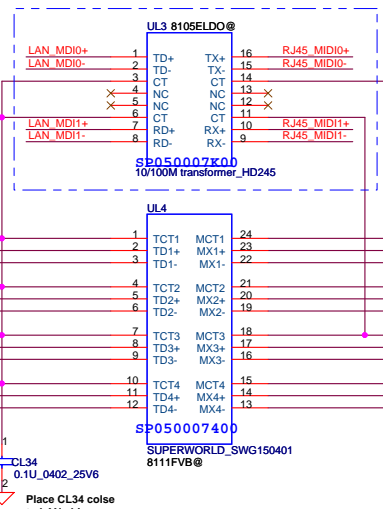
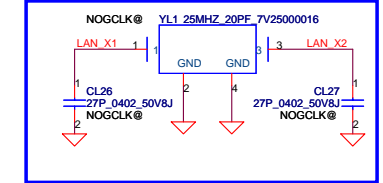
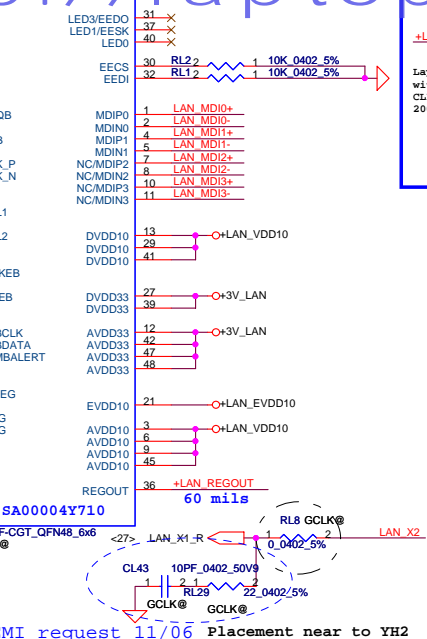
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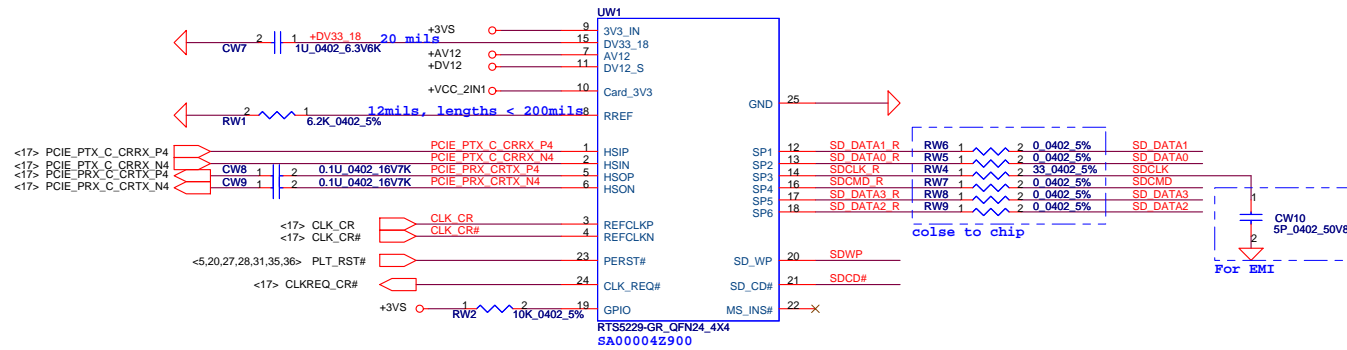
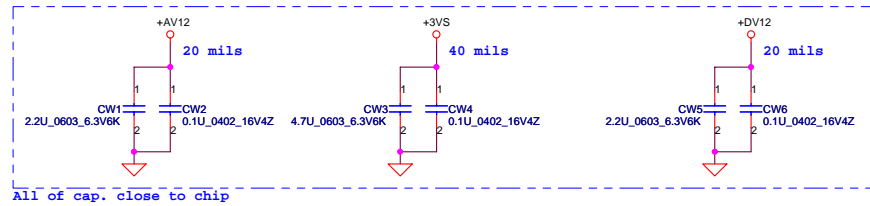


+3V_LAN rising time (10%-90%) need > 1ms and <100ms.

LAN	WOL	LAN_EN	ISOLATEB
		S0	Sx
0	0	0	1
0	1	0	1
1	0	1	1
1	1	1	0*

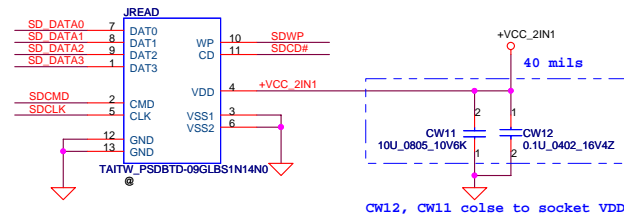
*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms



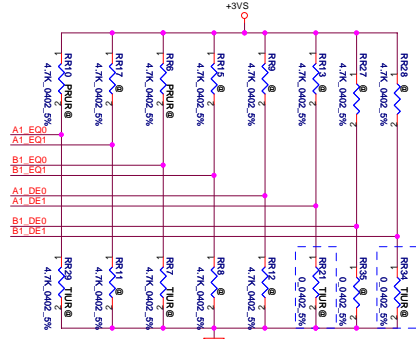


< 2 in 1 Card Reader >

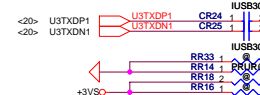
Connector on bottom side



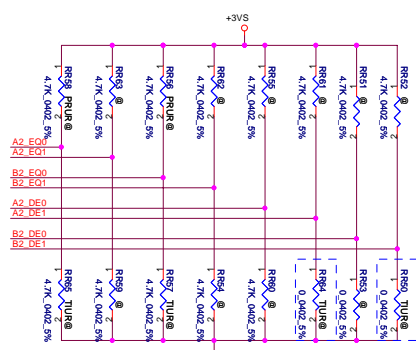
- Note:
- 1) keep differential trace mismatch less than +/- 5mil
 - 2) keep USB3 impedance follow Intel SPEC
 - 3) Power / GND pin trace 10mil



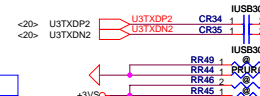
TI: A_DE1, B_DE1 need 0ohm to GND.
If use Parade and need control
A_DE1 & B_DE1 please use 4.7K



REXT - swing pin(2.5K~10K)
When test RX need add RR18



TI: A_DE1, B_DE1 need 0ohm to GND.
If use Parade and need control
A_DE1 & B_DE1 please use 4.7K



REXT - swing pin(2.5K~10K)
When test RX need add RR18

TI suggest EQ1(Pin2) & EQ2(Pin17) to pull Down use 7dB
DE1(Pin3) & DE2(Pin16) NC use 0dB
OS1(Pin4) & OS2(Pin15) NC use 1042mV

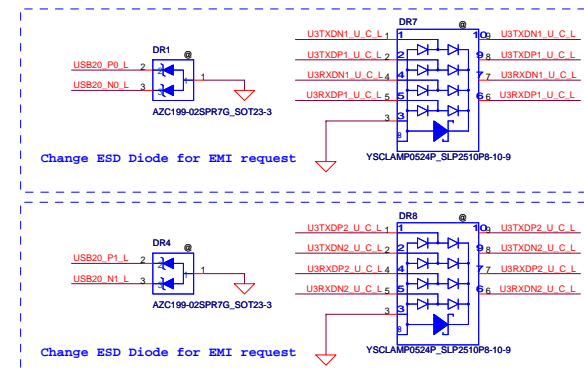
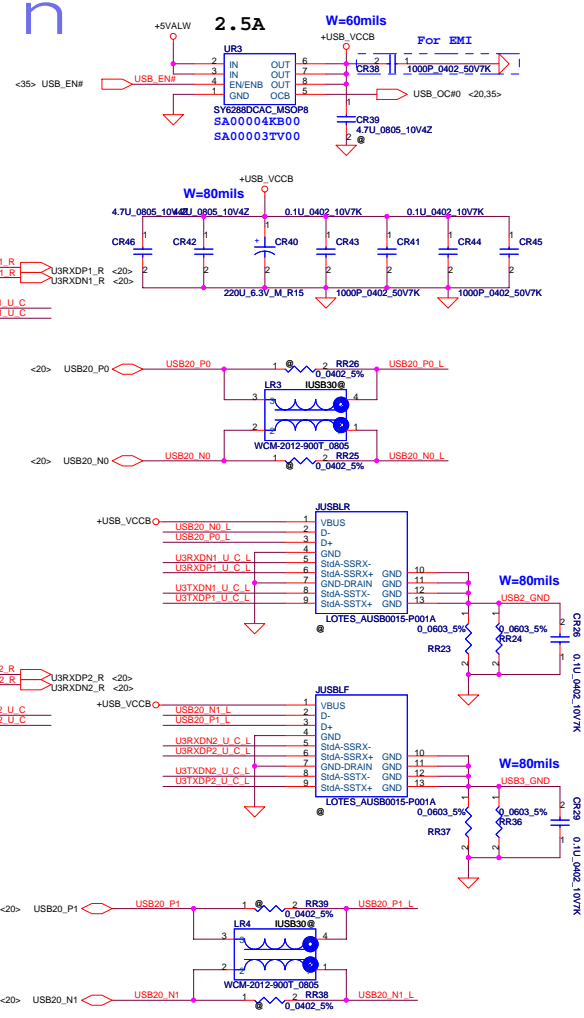
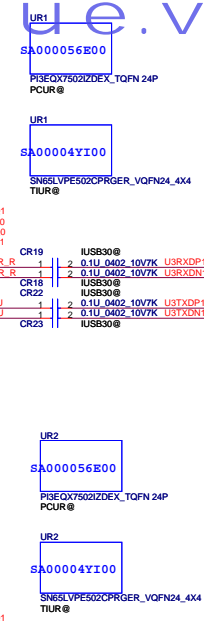
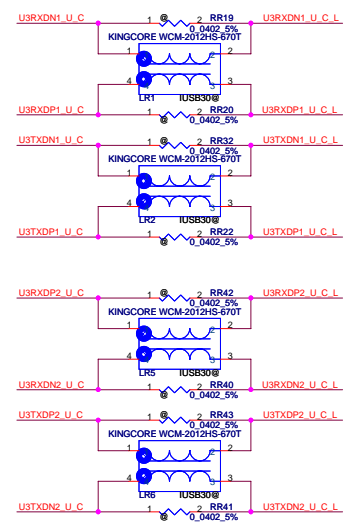
OUTPUT SWING AND EQ CONTROL (at 2.5 GHZ)			
OSx	TRANSISTION BIT AMPLITUDE (TYP mVpp)	EQx	EQUALIZATION (dB)
NC(default)	1042	NC(default)	0
0	908	0	7
1	1127	1	15
OUTPUT DE CONTROL (at 2.5GHZ)			
DEx	OSx = NC	OSx = 0	OSx = 0
NC(default)	0 dB	0 dB	0 dB
0	-3.5 dB	-2.2 dB	-4.4 dB
1	-6.0 dB	-5.2 dB	-6.0 dB
CONTROL PINS SETTINGS			
EN_RXD	DEVICE FUNCTION	CM	DEVICE FUNCTION
1(default)	Normal Operation	0(default)	Normal Operation
0	Sleep Mode	1	Compliance Test Mode

Parade suggest EQ1(Pin2) & EQ2(Pin17) to pull High use 7dB. All control has internally pulled down at ~150Kohm, If add ESD Diode A_DE0(Pin16) and B_DE0(Pin3) need pull high to 7dB otherwise 3dB

A_EQ1(Pin15)	A_EQ0(Pin17)	B_EQ1(Pin4)	B_EQ0(Pin2)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H
adaptive EQ enable		adaptive EQ enable	
Loss up to 7dB		Loss up to 7dB	
Loss up to 14.5dB		Loss up to 14.5dB	
Loss up to 11.5dB		Loss up to 11.5dB	
A_DE1(Pin18)	A_DE0(Pin16)	B_DE1(Pin6)	B_DE0(Pin3)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H
3.5dB		3.5dB	
No de-emphasis		No de-emphasis	
7dB		7dB	
5dB with boost output swing		5dB with boost output swing	

BOM Structure

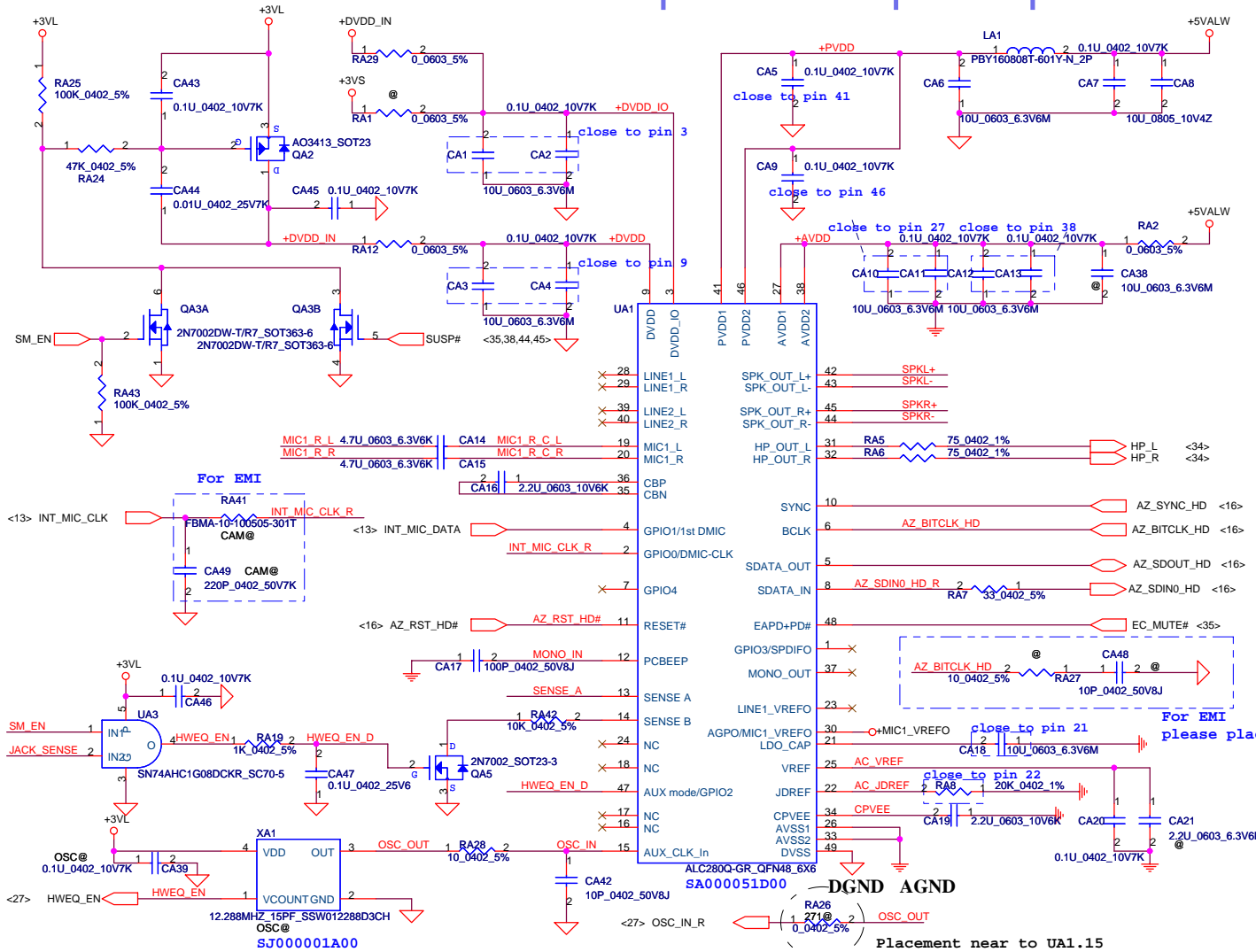
Pericom	PCUR@
TI	TIUR@
Parade	PRUR@
USB3.0	USB30R@



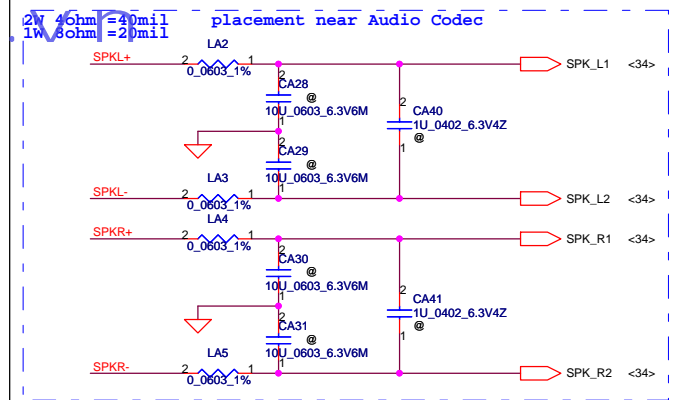
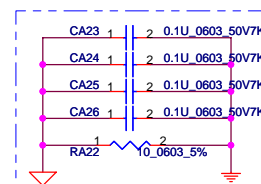
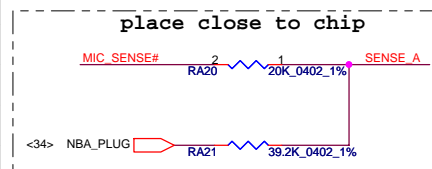
h t t p : / / l a p t o p b l u e . v n

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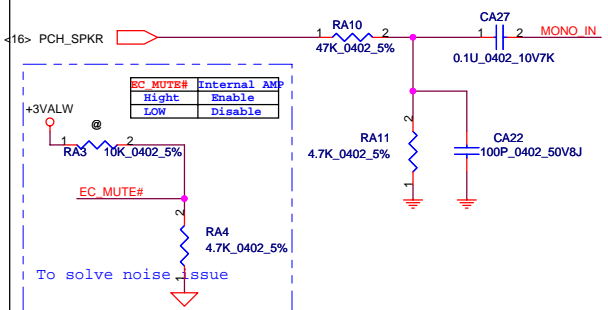
http://laptopblue



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 31, 32)	Headphone out
	20K	PORT-B (PIN 19, 20)	Ext. MIC
	10K	PORT-C (PIN 28, 29)	
	5.1K	PORT-E	
SENSE B	39.2K		
	20K		
	10K		

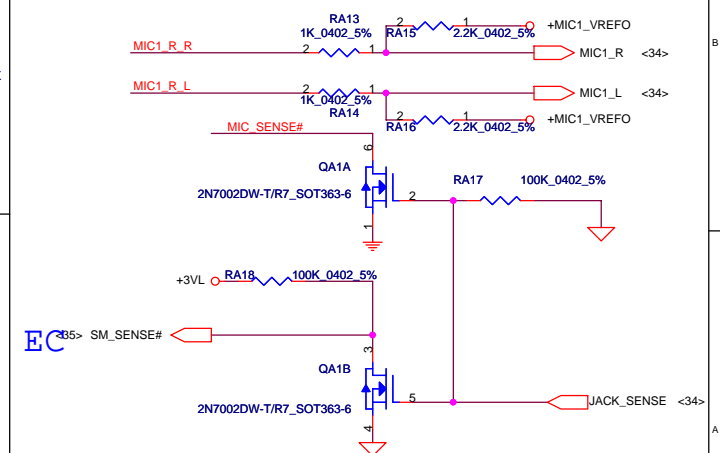


PCI Beep



Beep sound

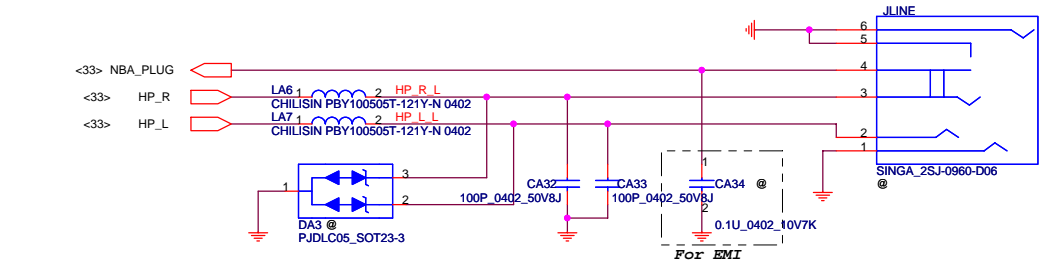
Ext.MIC/LINE IN JACK



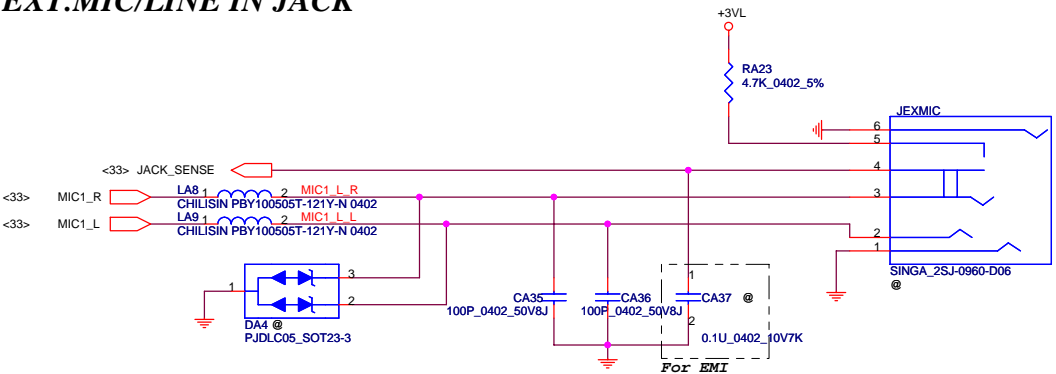
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HeadPhone/LINE OUT JACK

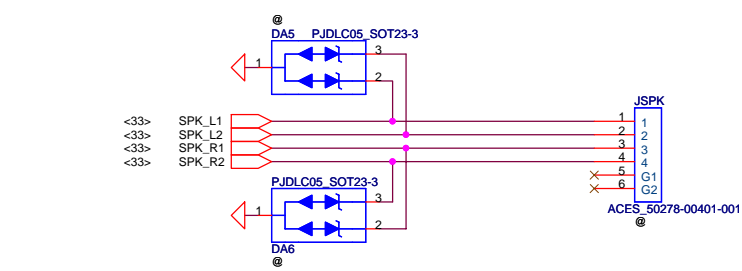
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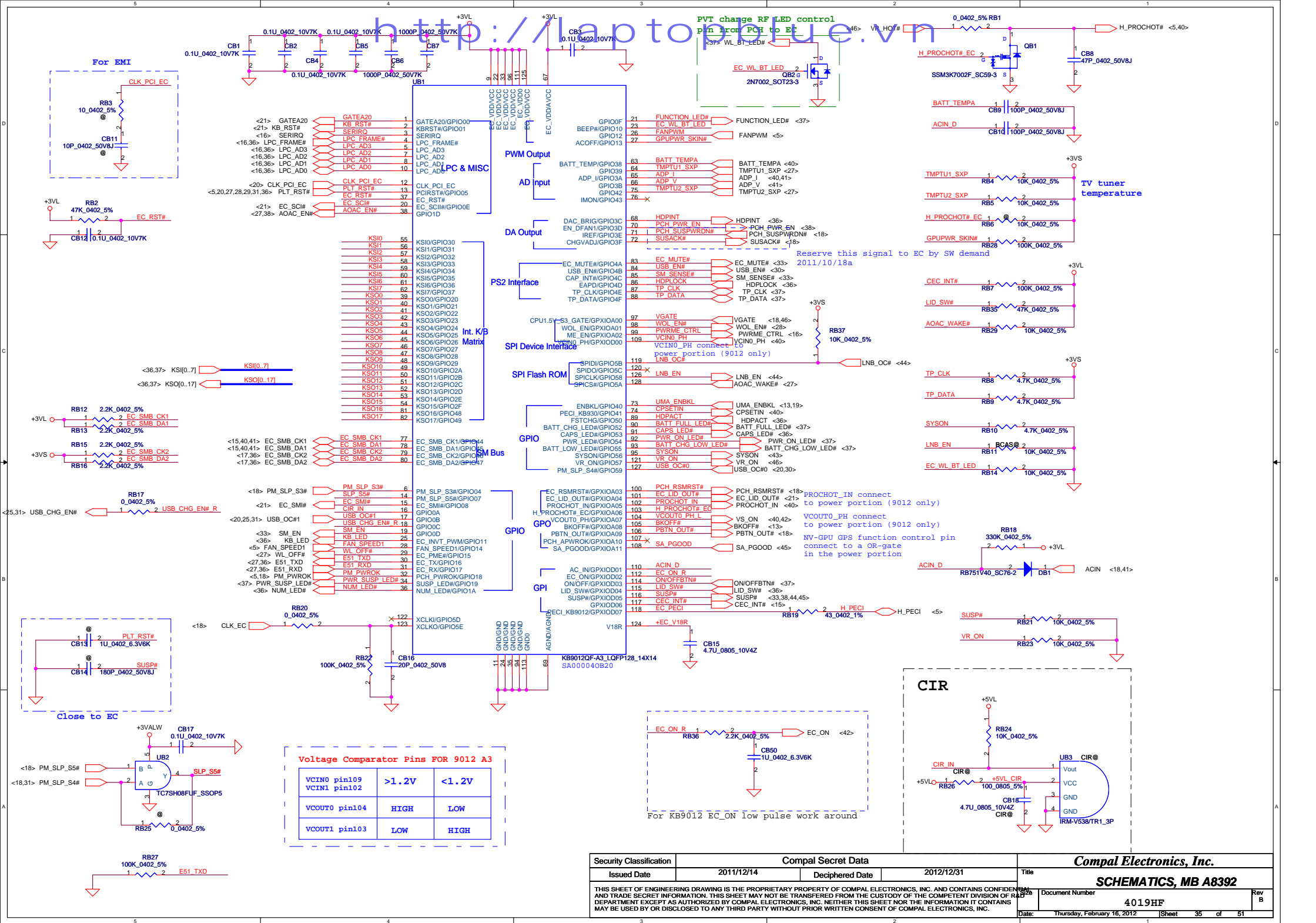
EXT.MIC/LINE IN JACK



SPK CONN.



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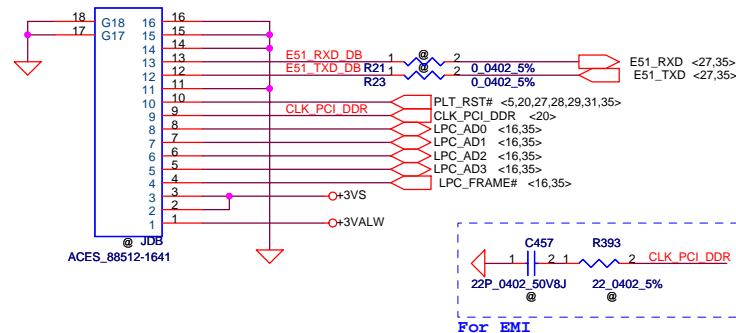
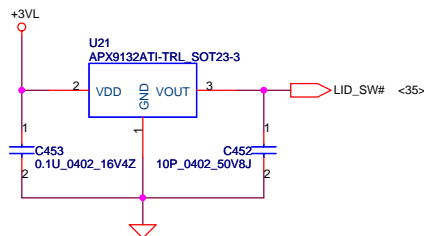
SPI Flash (128KB)

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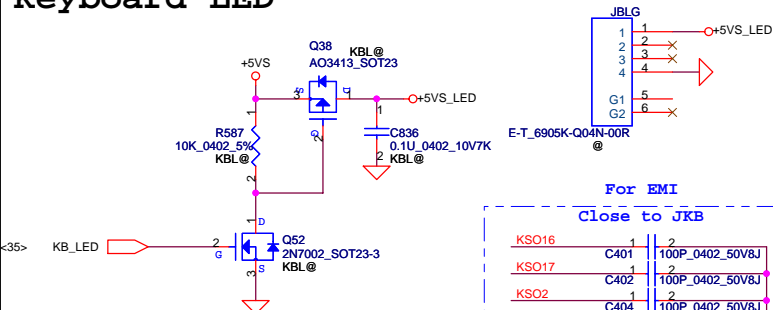
Lid SW

LPC Debug Port

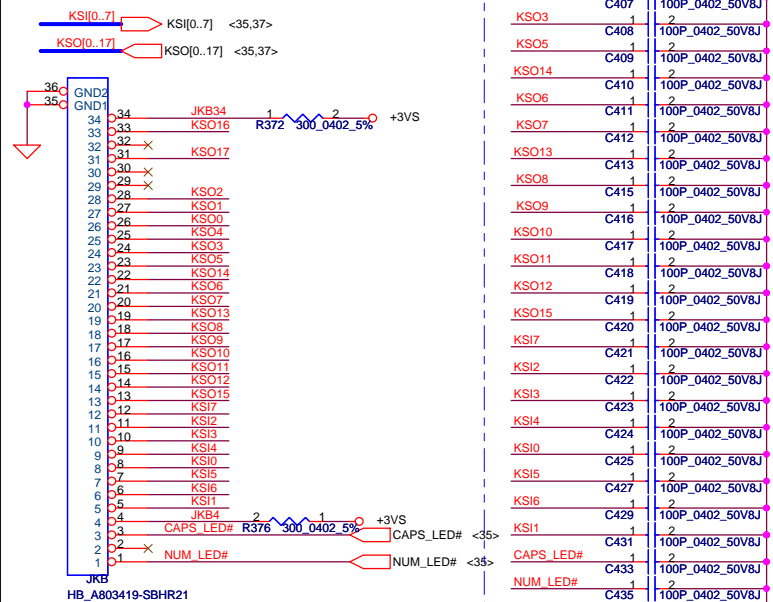
Place the JDB under DDR DIMM.



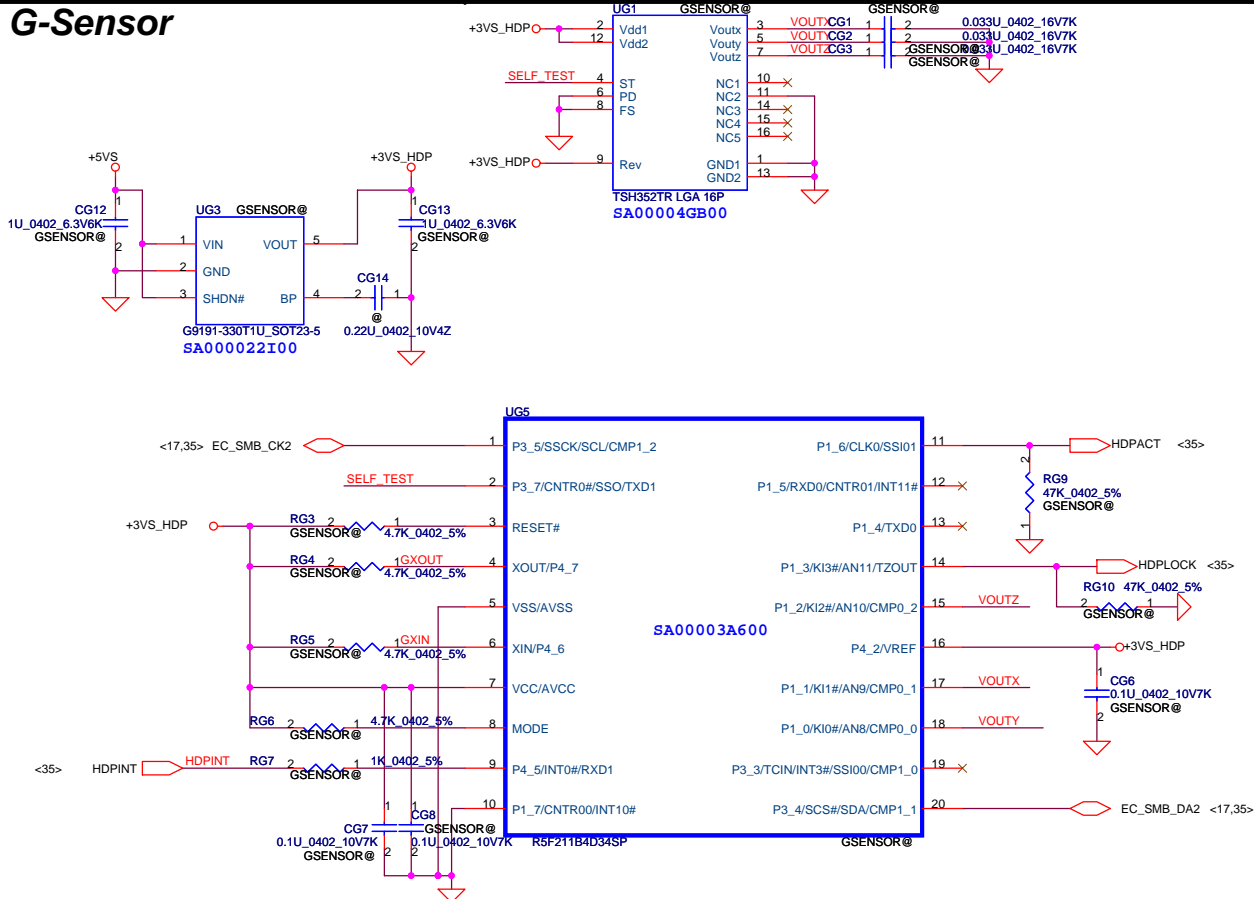
Keyboard LED



KEYBOARD CONN.

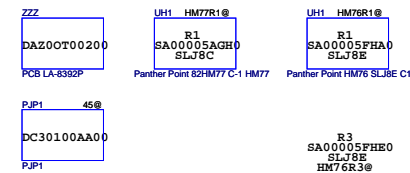
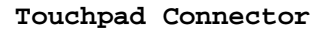


G-Sensor



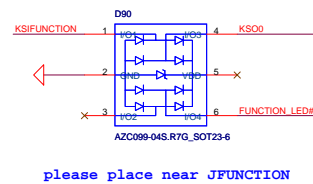
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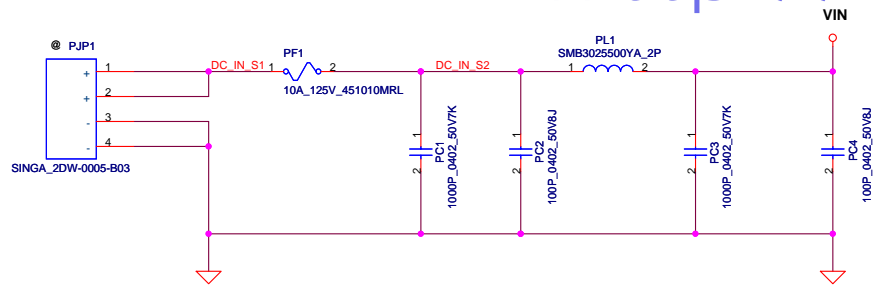


Green LED SC5000009S00 VF=2.8V~3.15V, Isink<15mA

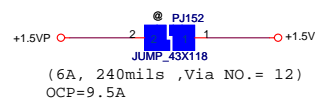
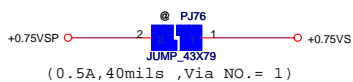
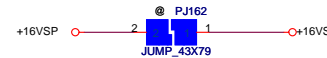
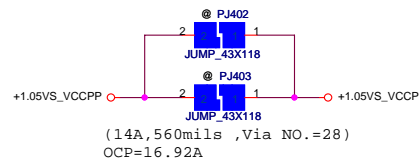
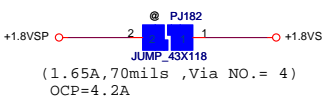
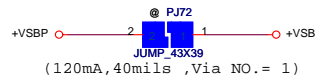
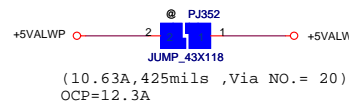
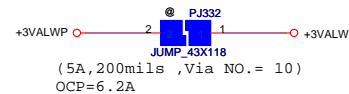
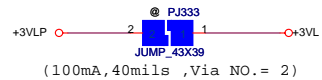
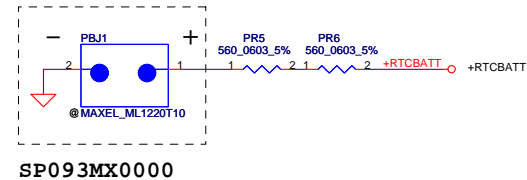
White LED SC5000004W00 VF=2.75V~3.15V, Isink<15mA



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				Date:	Thursday, February 16, 2012



RTC Battery



ACIN

	Precharge detector		
	Min.	typ.	Max
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

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				Date:	Thursday, February 16, 2012
				Sheet	39 of 51
				Rev	B

PH1 under CPU botten side :

CPU thermal protection at 90 degree C
Recovery at 56 degree C

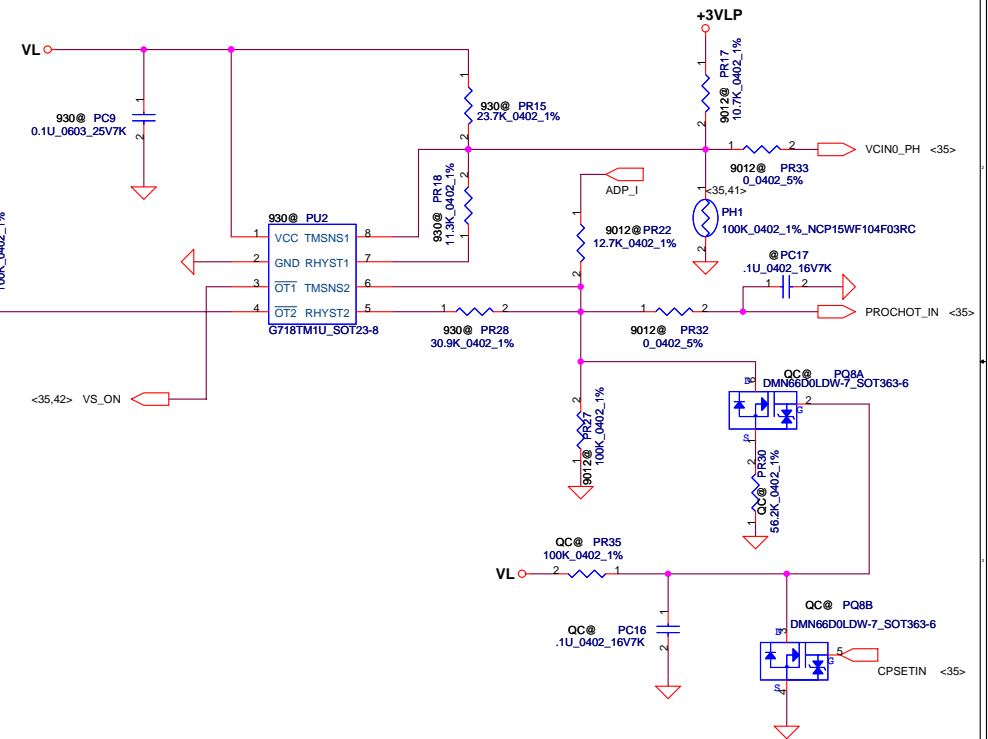
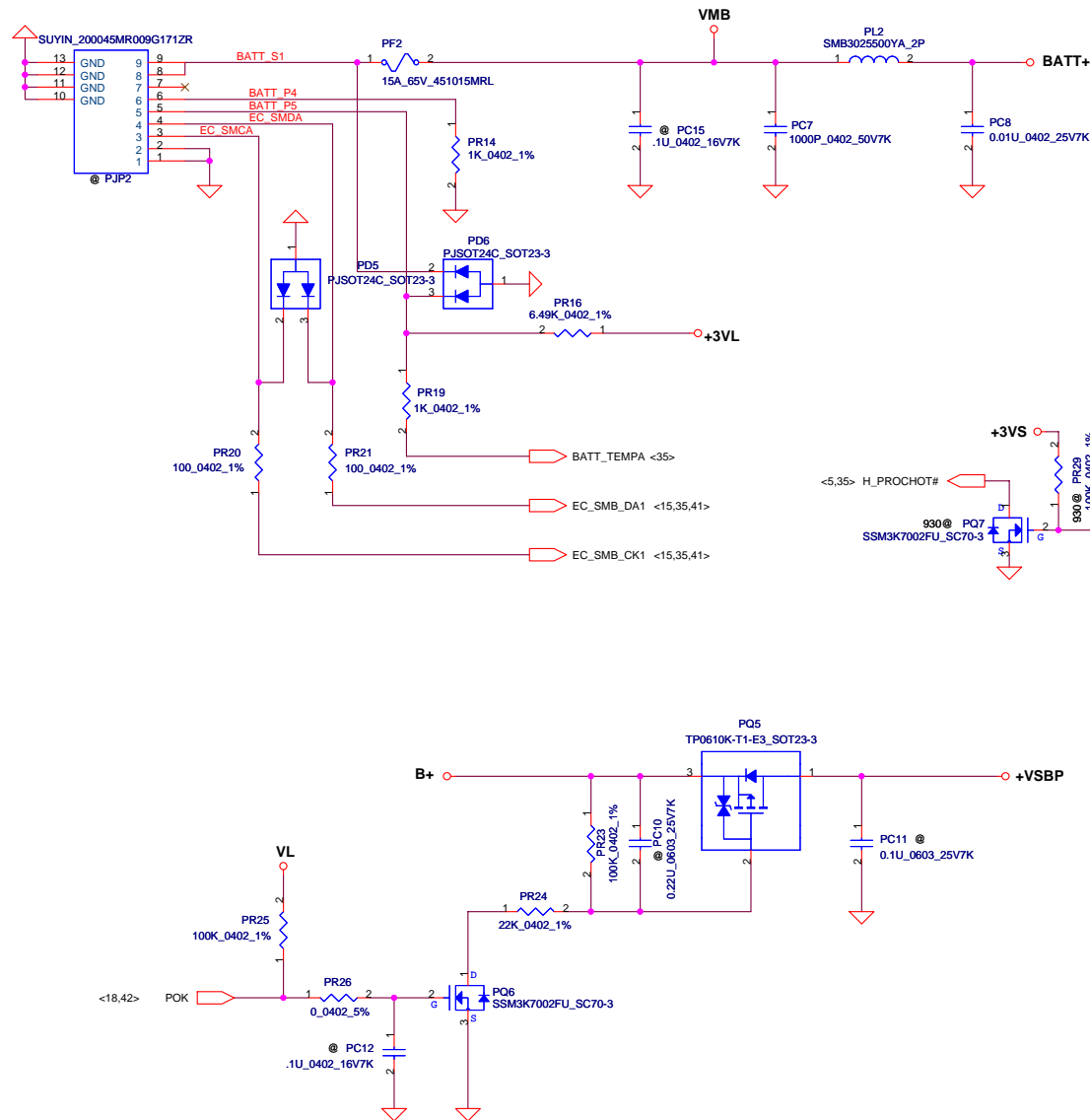
Rset = 3 * Rtmh

Rhyst = (Rset * Rtml) / (3 * Rtml - Rset)

Rtmh at 90C = 7.87K, Rtml at 56C = 26.1K

Rset = 3 * 7.87K = 23.61K ==> 23.7K

Rhyst = (23.7K * 26.1K) / (3 * 26.1K - 23.7K) = 11.33K ==> 11.3K



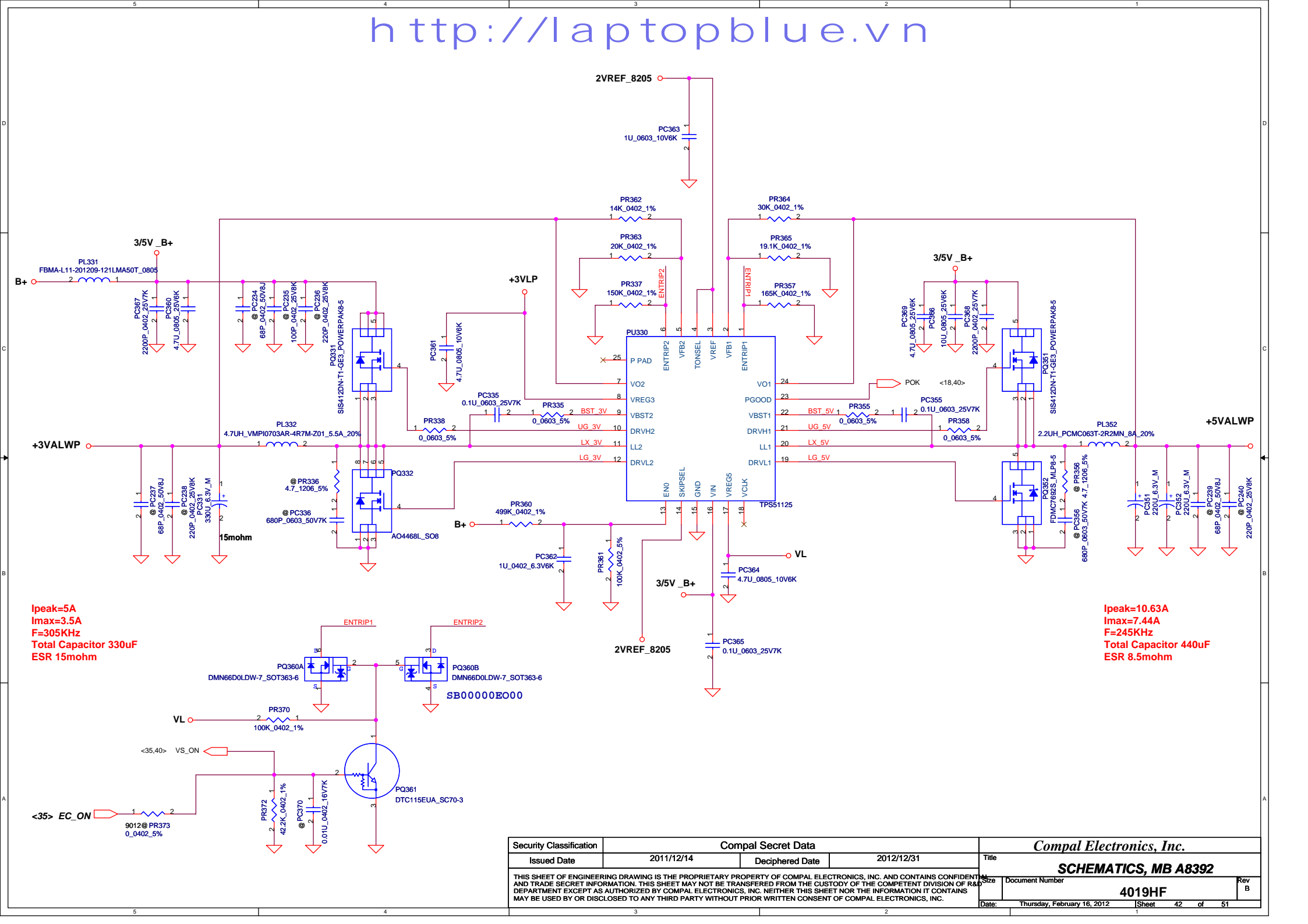
Adaptor protection				
Adaptor	Throttling point	ADP_I	Recovery point	ADP_I
90W	113.5W	1.783V	86.4W	1.357V
65W	71.8W	1.504V	62.5W	1.308V

for reverse input protection



ILIM and external DPM
3.97A

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						Doc Number		4019HF		Rev B	
						Date:		Thursday, February 16, 2012		Sheet 41 of 51	



http://laptopblue.vn

http://laptopblue.vn

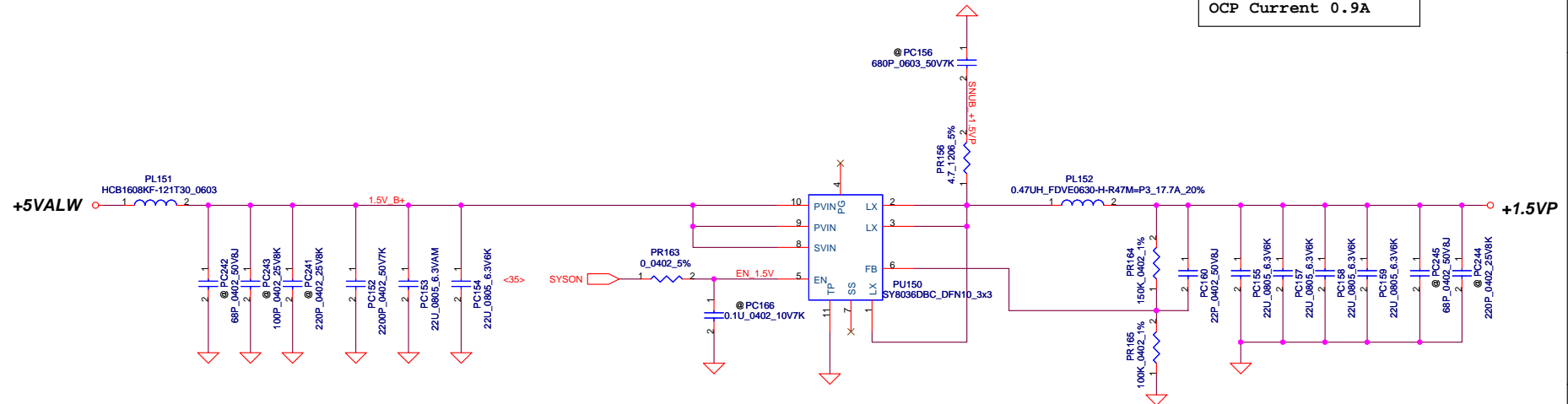
http://laptopblue.vn

HW side:
C106 330uF 17m
C218 390uF 10m
VGA @ CV122 390uF 10m
@ C189 330uF 15m

UMA
Ipeak=8.5A
Imax=5.95A
Rtrip=5.9K, OCP=11.338A
F=315KHz
Total Capacitor 1050uF,
ESR 4.43mohm

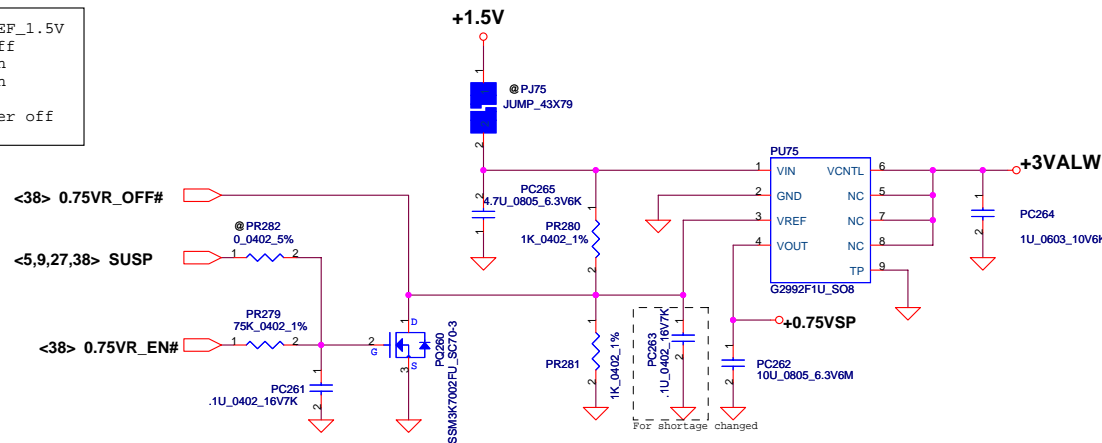
DIS
Ipeak=20A
Imax=14A
Rtrip=14K, OCP=24.136A
F=315KHz
Total Capacitor 1440uF,
ESR 3.07mohm

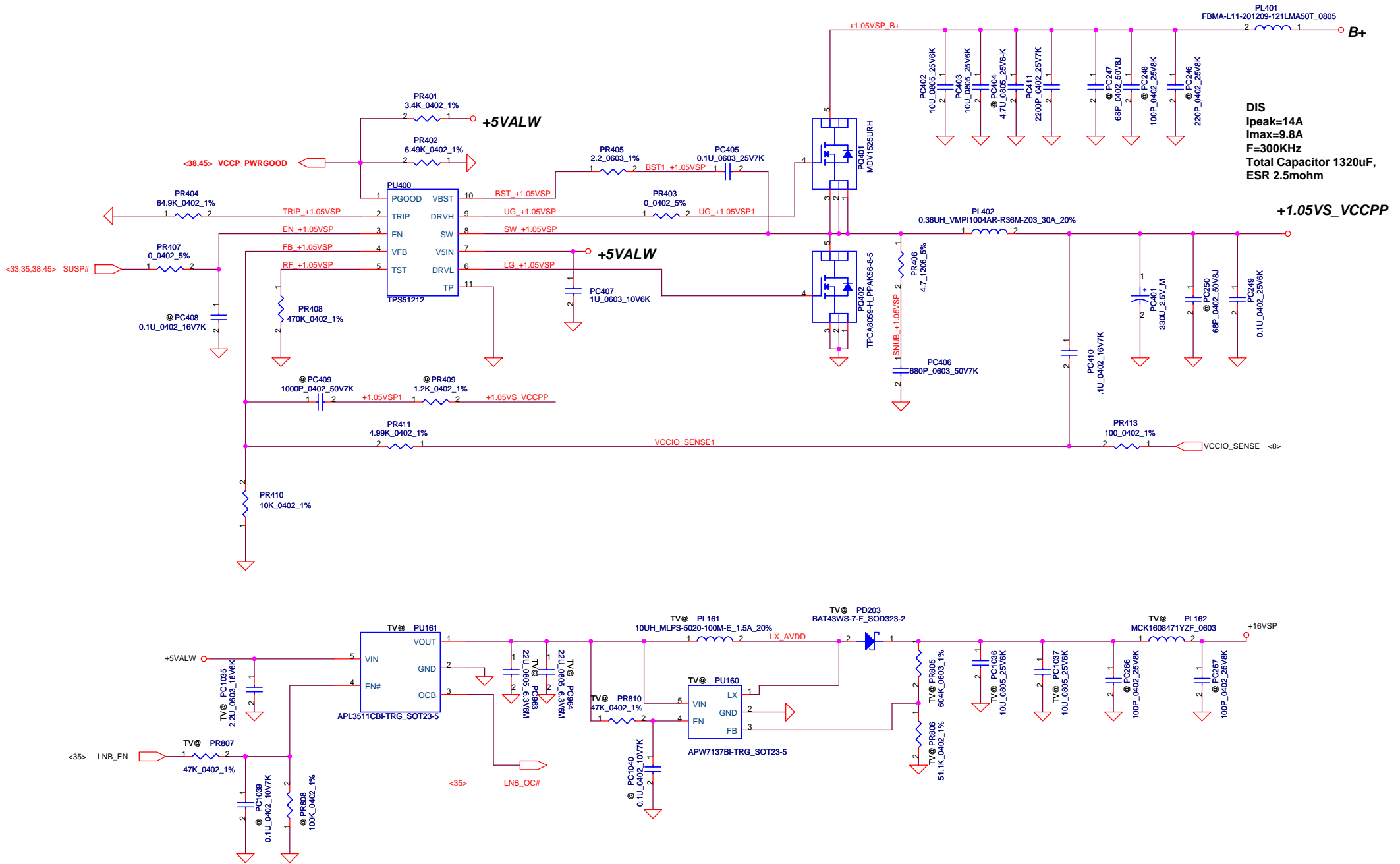
0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A



Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off



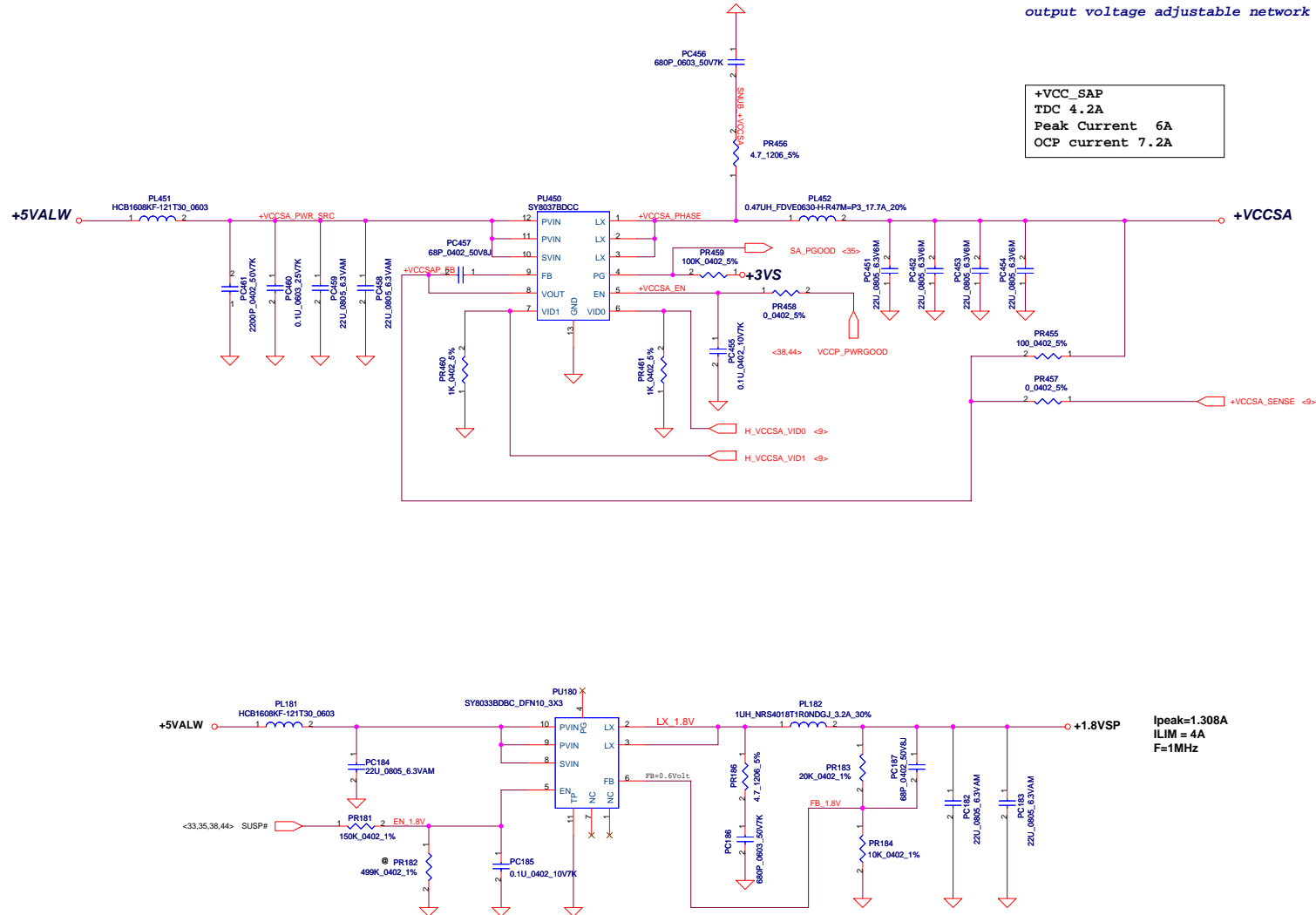


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The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

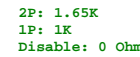
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

```
+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A
```



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QCG@PR564
39K_0402_1%



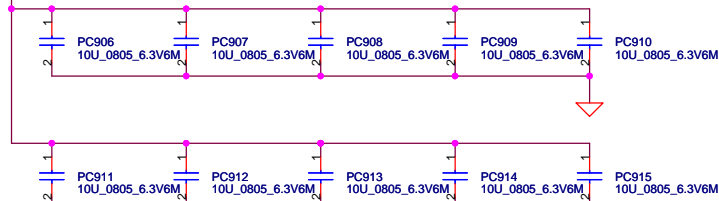
PC573
P_0402_50V7K

PR597
0402_1%

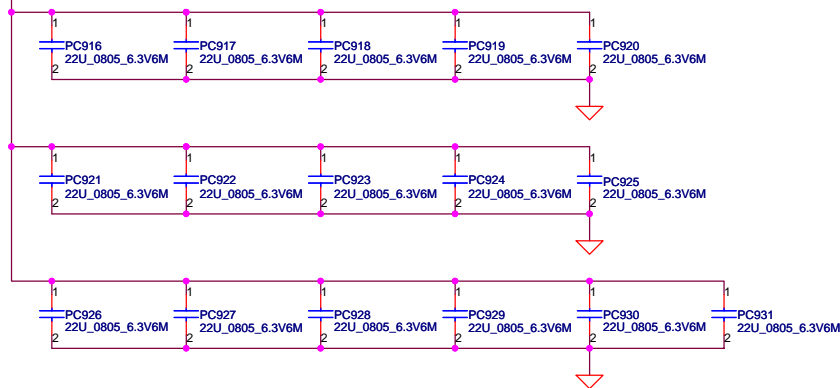
Re	
----	--

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

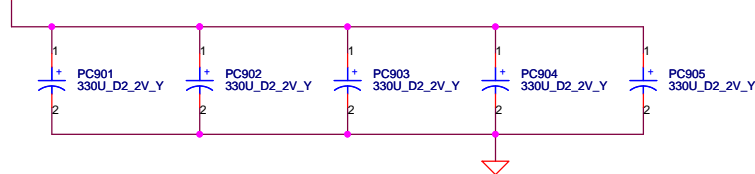
+CPU_CORE



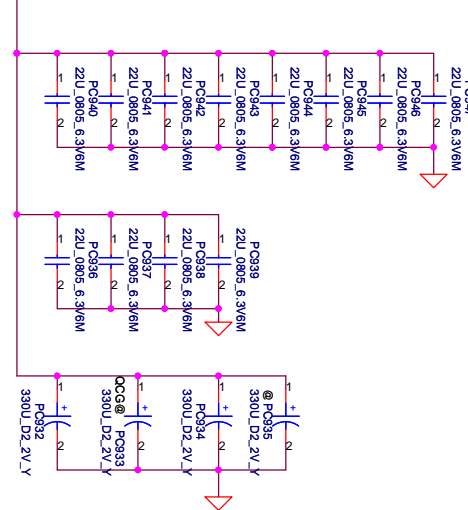
+CPU_CORE



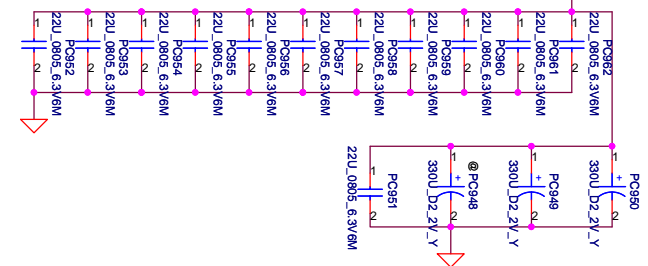
+CPU_CORE



+GFX_CORE



+1.05VS_VCCP



	Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4			16	10
8layer for QC CPU	5			16	10
6layer for DC CPU	5			16	10
6layer for QC CPU	4	1		16	10
GFX_CORE DC	2			12	
GFX_CORE QC	3			12	
1.05v_VCCP	2			12	

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1.	2011/09/29	P51-PWR_+3VALWP/+5VALWP	Change PU330 to RT8205L	Change source
2.	2011/09/29	P53-PWR_ +1.05VS_VCCP/+16VSP	Change PU400 to RT8237C	Change source
3.	2011/09/29	P54-PWR_+VCCSAP/1.8VSP	Change PU450 to SY8037B	Change source
4.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change HMOS to MDV1525	Change source
5.	2011/09/29	P53-PWR_ +1.05VS_VCCP/+16VSP	Change HMOS to MDV1525	Change source
6.	2011/09/29	P49-PWR_BATTERY CONN / OTP	Change PD5,PD6 to SCA00001G00	ESD team request
7.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PR589 from 348 to 8.06k	FAE suggestion
8.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PR590 from 3.65k to 806	FAE suggestion
10.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PC574 from 680P to 0.033u	FAE suggestion
11.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PC577 from 4700P to 0.033u	FAE suggestion
12.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PR548 from 1.21k to 8.06k	FAE suggestion
13.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PR550 from 10.7k to 806	FAE suggestion
14.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PC547 from 680P to 0.033u	FAE suggestion
15.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Change PC551 from 4700P to 0.033u	FAE suggestion
16.	2011/09/29	P57-PWR +CPU_CORE DECOUPLING	Add snubber and boost resistor	For 3x3 H-MOS solution
17.	2011/09/29	P49-PWR_BATTERY CONN / OTP	Add PR22 30k,PR27 100k, PR32 0 Ohm	For 120W adapter protect(9012)
18.	2011/09/29	P51-PWR_+3VALWP/+5VALWP	Change PC360 to SE000006R80	Change source
19.	2011/09/29	P49-PWR_BATTERY CONN / OTP	Add PR17 14k, PR33 0 Ohm	For CPU temperature protect(9012)
20.	2011/09/29	P51-PWR_+3VALWP/+5VALWP	Add PR373 0 Ohm	For 3/5V always power on(9012)

HW PIR (Product Improve Record)

QFKAA LA-8392P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2
GERBER-OUT DATE: 2011/11/11

Item	Page	Date	Request	Solution
1)	13	2011/9/29a	by RSD demand	change D84 to SCA00001L00
2)	26	2011/9/29a	by RSD demand	change D82 to SCA00001L00
3)	28	2011/9/29a	by RSD demand	change D92 to SCA00001L00
4)	05	2011/10/05a	follow HW4 check list	reserve decoupling cap CC66, CC71, CC70 for H_PM_SYNC & H_PBCI, BUF_CPU_RST#
5)	19	2011/10/05a	by Customer demand	add LVDS dual channel signal
6)	13	2011/10/05a	by Customer demand	add LVDS dual channel signal and 0ohm: R267 R268 R269 R270 R283 R329 R333 R337 (OPTFHD#) and R500 R501 R502 R503 R504 R505 R507 R508 (3D#)
7)	17	2011/10/05a	by Customer demand	change RH16 to HD# add RH282 FHD#
8)	35	2011/10/18a	discuss with EC	change Function_LED from EC_GPIO4D, PIN86 to EC_GPIO11, PIN25 change HDPLCK from EC_GPIO11, PIN28 to EC_GPIO4D, PIN86 add GPUPWR_SKIN# on EC_GPIO13, pin27. add RB28 for GPUPWR_SKIN#
9)	18	2011/10/18a	by SW ME demand.	change HDPACT from EC_GPIO43, PIN76 to EC_GPIO50, PIN89 reserve SUSACK# and PCH_SUSPWRDN# by SW demand change PCH_SUSPWRDN_R to PCH_SUSPWRDN# add PCH_SUSPWRDN# to EC and RH132 remove T75 change SUSACK# to SUSACK#_R add RH133 and SUSACK# to EC swap LR2, LR1, DR7 swap LT3, LT2
10)	30	2011/10/31a	by Layout demand	remove RH1, RH174, and change net-name from LNB_PWR_MONITOR to LNB_OC
11)	32	2011/10/31a	by Layout demand	add JTP connector Pin 5 (PM_SWCLK), Pin6 (PM_SWDATA)
12)	20	2011/10/31a	by PWR 16V OC control demand	add RMI5 and RMI6 reserve for TV tuner (BCAS)
13)	37	2011/11/1a	new touch pad add new function	reserve RA43 for SW_EN 100K pull down reserve
14)	27	2011/11/1a	TV tuner(BCAS) 16V reserve	exchange location of RA28 and CM2
15)	33	2011/11/1a	avoid SW_EN floating	RA26 pin2 change name from OSC_IN to OSC_OUT
16)	33	2011/11/1a	for vendor request	delete DAL. add RA19 ,QA5 ,RA42 ,
17)	33	2011/11/1a	for vendor request	delete CH57, RJ3 then add RJ5, QH6 ,CH59 , RH228
18)	33	2011/11/1a	for vendor request, S&M HP need shut down	add R5545, Q5527, R5529, R5534
19)	23	2011/11/1a	for lot6 0.5W power consumption	reserve RH228
20)	38	2011/11/2a	for lot6 0.5W power consumption	change D21 power from +5VL to +5VALW
21)	23	2011/11/2a	for lot6 0.5W power consumption	add CCL10
22)	37	2011/11/2a	for lot6 0.5W power consumption	add CL43, RL29
23)	27	2011/11/6a	by EMI demand	change RM4 from 0ohm to 33ohm, CW10 from 5pF to 6.8pF
24)	28	2011/11/6a	by EMI demand	change JUSB3LR to JUSBRR, JUSB3RP to JUSB3P
25)	29	2011/11/6a	common with ME define location	change JUSB3LR to JUSBLR, JUSB3LP to JUSBLP
26)	25	2011/11/7a	common with ME define location	change J3GTV to JPCIF
27)	30	2011/11/7a	common with ME define location	change JFUNCTION to JFUN
28)	27	2011/11/7a	common with ME define location	delete CH105, CH106; add QH2, CH97, CH98, RH1, RH3
29)	37	2011/11/7a	common with ME define location	add EC pin 70 for PCH_PWR_EN
30)	22	2011/11/7a	for lot6 0.5W power consumption	change PCH version to SA000048Q90(B0) and BOM option to SA00005AG10(C0)
31)	35	2011/11/7a	for lot6 0.5W power consumption	change net name from LNB_OC to LNB_OCN; add RH290 to pull high LNB_OCN
32)	37	2011/11/7b	by proto plan demand	delete H4, H8; modify H7, H22, H30 to NPTH
33)	20	2011/11/7b	by PWR 16V OC control demand	UHI.F46 and RH126 chagne net name from WL_OFF# to PCH_GPIO55
34)	37	2011/11/7b	by Layout team demand	change UB1.29 net name from CPSETIN to WL_OFF#
35)	20	2011/11/9a	EC common core for WL_OFF#	add RMI7 for WL_OFF# pull high to +3V_MLAN
36)	35	2011/11/9a	EC common core for WL_OFF#	CPSETIN signal change from UB1.29 to UB1.74
37)	27	2011/11/9a	EC common core for WL_OFF#	add RB37 10kohm pull high to +3VS for LNB_OC#
38)	35	2011/11/9a	by PWR 16V OC control demand	remove BOM selection IRDPS for R109, R110, C230, C233, Q1
39)	35	2011/11/9a	by PWR 16V OC control demand	change R108, C228, Q17 to LVDS#: change Q1, C230, C233, R109, R110 to always mount
40)	13	2011/11/9d	for dual-channel power support	add R390, R1442, R1441, R106
41)	13	2011/11/9d	for dual-channel power support	change R106 to LVDS#, R1441 to @, R361 to @, R1442 to 3D#, R390 to @
42)	13	2011/11/9d	for dual-channel power support	add R79, R97, L60
43)	13	2011/11/9d	for dual-channel power support	add R361; change R62 from 100 to 0
44)	13	2011/11/9d	for dual-channel power support	add RH104
45)	13	2011/11/9d	for dual-channel power support	change YCL1 from SJ10000CU00 to SJ10000EP00, CCL4 and CCL5 from 30pF to 15pF
46)	21	2011/11/9d	for dual-channel power support	change CW10 from 6.8pF to 5pF
47)	27	2011/11/14a	for vendor recomment	change BOM structure of CCL10 from @ to GCLK#
48)	29	2011/11/15a	by EMI demand	change BOM structure of RL29, CL43 from @ to GCLK#
49)	27	2011/11/15d	by EMI demand	
50)	28	2011/11/15d	by EMI demand	

HW PIR (Product Improve Record)

QFKAA LA-8392P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3
GERBER-OUT DATE: 2011/12/22

Item	Page	Date	Request	Solution
1)	18	2011/11/29a	For DVT hang	Add CH23,CH24,CH25 for SW-node noise.
2)	13	2011/11/29a	For ME request	Change location from JLVD5 to JLVD54
3)	38	2011/11/29a	For noise issue	Add C366, C470 at +5VALW power rail; add C381 at +1.8VS power rail
4)	05	2011/12/07a	For leakage	Change from +3VALW to +3VALW_PCH of UCI
5)	38	2011/12/07a	For design change	Add C382 for +1.8VS
6)	33	2011/12/13a	For Codec leakage	Add RA29 for leakage
7)	18	2011/12/13a	For noise issue	Mount CH23,CH24,CH25.
8)	05	2011/12/13a	For leakage	Change pin5 of UCI from +3VALW to +3VALW_PCH
9)	15	2011/12/13a	For leakage issue	Change pin5 of U9 from +5VL to +HDMI_5V_OUT
10)	38	2011/12/13a	For noise issue	Add C372,C373,C374,C383,C384,C385,C386,C387,C388,C389,C390,C391,C392
11)	35	2011/12/13a	For design change LNB_EN	Change LNB_EN from PCH to EC
12)	35	2011/12/13a	For design change RF LED	Change RF LED control pin from PCH to EC
13)	38	2011/12/13a	For S3 resume sequence	Add Q41 for S3 sequence
14)	26	2011/12/15a	For ME request	Change JPP/JPOWER/JFUN from zif to non-zif
15)	31	2011/12/15a	For adjust EXT 3.0 sequence	Change +3V to +3V_USB control pin from syson to PM_SLP_S4#
16)	32	2011/12/15a	For adjust EXT 3.0 sequence	Change +3V to +3V_USB control pin from syson to PM_SLP_S4#
17)	13	2011/12/17a	For Prevent LVDS burn issue	Add F3 (Poly fuse to prevent burn issue)
18)	37	2011/12/19a	For ME delete stand-off	Delete H25,H26,H27
19)	37	2011/12/19a	For Wimax flash issue	Change +5VS to +3VS of Wimax LED
20)	37	2011/12/19a	For layout request	Add net name +5VS_FUNC with Function conn power pin
21)	21	2011/12/22a	For ESD request	Reserve CH30(1000P) for PCH_THERMTRIP#
22)	13	2011/12/22a	For ME request	change C381, C382, C470, C366 from 0805 to 0603 size

QFKAA LA-8392P SCHEMATIC CHANGE LIST
REVISION CHANGE: 1.0
GERBER-OUT DATE: 2012/02/02

Item	Page	Date	Request	Solution
1)	27	2012/01/12a	For GLCK	Add CCL13(0.1u) for +3VALW
2)	27	2012/01/12a	For MSATA pin define.	Add RM30 (MSATA define that pin22 is reserve, so other function need to add PLT_RST#).
3)	27	2012/01/18a	For GLCK	Change CCL13 from +3VLAW to +3VALW_GCLK
4)	27	2012/01/30a	For TV tuner use PCIE interface	Add RM31-RM35 and QM2
5)	17	2012/01/30a	For TV tuner use PCIE interface	Change PCIE 6 from USB to TV tuner
6)	17	2012/01/30a	For TV tuner use PCIE interface	Change CLK_USB30 to CLK_TV and CLKREQ_USB30# to CLKREQ_TV#
7)	37	2012/01/30a	For MP	Unmount SW3
8)	11	2012/01/30a	For MI only	Unmount RC117/RC118/QC7/QC8
9)	32	2012/01/30a	For Internal USB30 only	Delete Page 32
10)	37	2012/02/01a	For ESD request	Add C469, C472-C479, C481-C488, C491