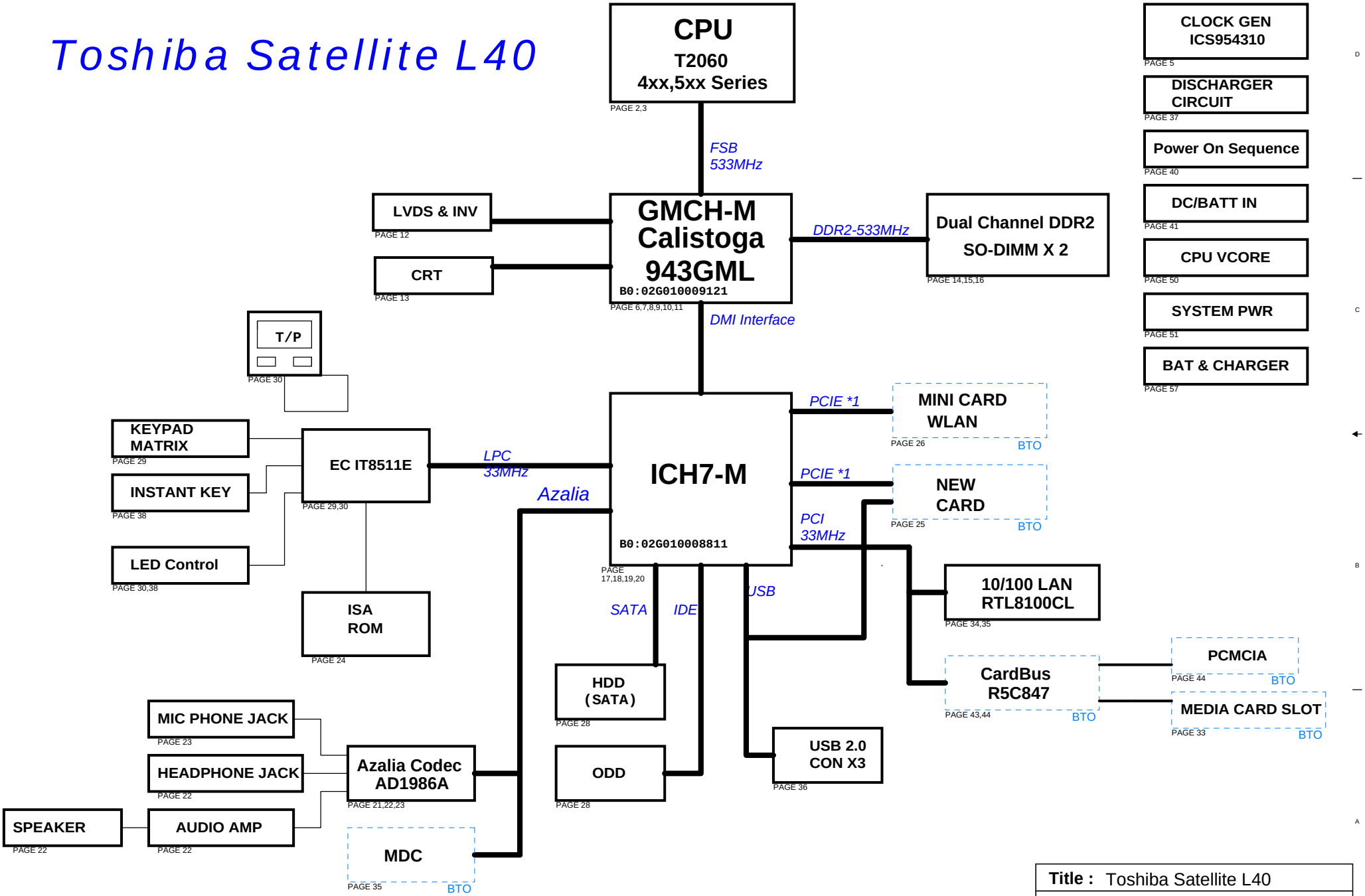
Toshiba Satellite L40



Title :	Toshiba Satellite L40	
Size	Project Name: Toshiba Satellite L40	Rev: 1.1
Date:	Sheet of	

6 H_A#[16..3]
6 H_REQ#[4..0]
6 H_A#[31..17]

U201A

ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
HCLK
RESERVED

T202
T201
T203
T204 TPC28T
T205

R201 56Ohm
R202 54.9Ohm @
R203 56Ohm@
R204 56Ohm
R205 56Ohm
R206 56Ohm@
R207 56Ohm
R208 56Ohm

+VCCP_AGTL+
GND

H_ADSTB#0
H_ADSTB#1
H_REQ#0
H_REQ#1
H_REQ#2
H_REQ#3
H_REQ#4
H_A20M#
H_FERR#
H_IGNNE#
H_STPCLK#
H_INTR
H_NMI
H_SMI#

H_ADS# H_BNR# H_BPRI#
H_DEFER# H_DRDY# H_DBSY#
H_BR0#
H_IERR# H_INIT#
H_LOCK#
H_CPURST# H_RS#0 H_RS#1 H_RS#2 H_TRDY#
H_HIT# H_HITM#
PRDY# H_PREQ# H_TCK H_TDI H_TDO H_TMS H_TRST#
CPU_DBR#
H_PROCHOT_S#
CPU_THRM_DA CPU_THRM_DC
PM_THRMTRIP#
CLK_CPU_BCLK CLK_CPU_BCLK#

H_ADS# 6
H_BNR# 6
H_BPRI# 6
H_DEFER# 6
H_DRDY# 6
H_DBSY# 6
H_BR0# 6
H_INIT# 17
H_LOCK# 6
H_CPURST# 6
H_RS#0 6
H_RS#1 6
H_RS#2 6
H_TRDY# 6
H_HIT# 6
H_HITM# 6
CPU_THRM_DA 4
CPU_THRM_DC 4
PM_THRMTRIP# 4,17
CLK_CPU_BCLK 5
CLK_CPU_BCLK# 5

(070122)Change CPU Socket into PN=12G011204796

68 ± 5% pull-up to Vcc1_05
If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 Ohm ± 5%

JP201 SHORT_PIN
2.5A
+VCCP
+VCCP_AGTL+
6,9,20,52
3,5,6,9

R217 56Ohm
R218 56Ohm@
29 H_PROCHOT_S#

H_D#[0..63] 6

U201B

DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC

H_DSTBN#0 6
H_DSTBP#0 6
H_DINV#0 6
H_DSTBN#1 6
H_DSTBP#1 6
H_DINV#1 6
H_DSTBN#2 6
H_DSTBP#2 6
H_DINV#2 6
H_DSTBN#3 6
H_DSTBP#3 6
H_DINV#3 6

R209 1KOhm 1%
R213 2KOhm 1%
C201 0.1UF/10V @
<500 mil (55 Ohm)
T/B trace 5
Space 25
@R214 1KOhm
R216 51Ohm
TEST1
TEST2
GTL_REF
CPU_BSEL0 CPU_BSEL1 CPU_BSEL2

R210 27.4Ohm 1%
R211 54.9Ohm 1%
R212 27.4Ohm 1%
R215 54.9Ohm 1%
H_COMP0 H_COMP1 H_COMP2 H_COMP3

H_DPRSTP# 17,50
H_DPSLP# 17
H_DPWR# 6
H_PWRGD 17
H_CPUSLP# 6,17
PM_PSI# 50

For Celeron M

BCLK	FSB	BSEL2	BSEL1	BSEL0
133MHz	533MHz	L	L	H

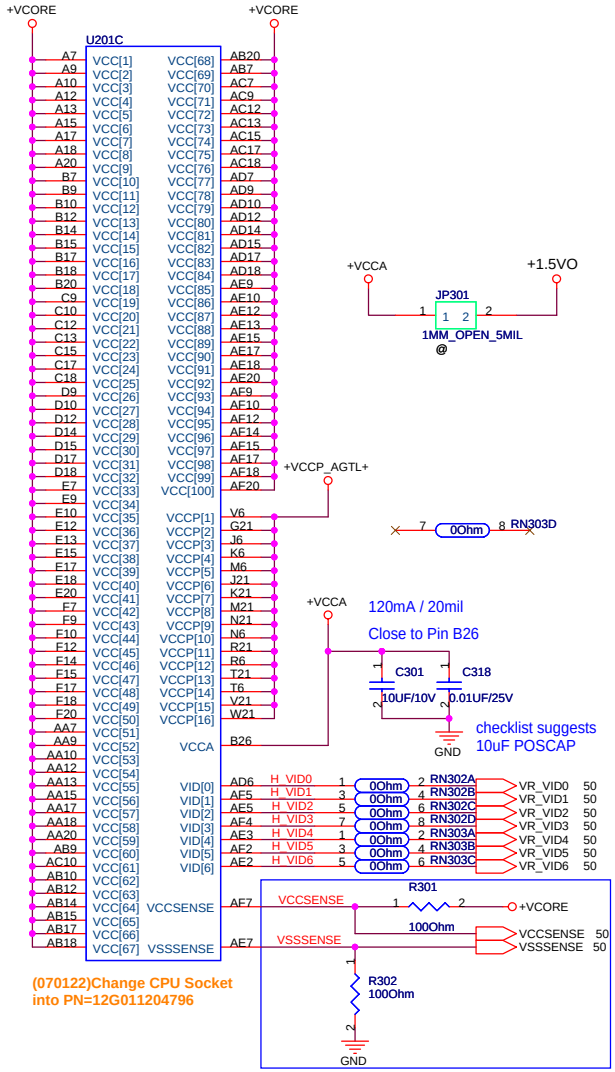
(070122)Change CPU Socket into PN=12G011204796

Layout Note:
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".
Comp[3:0] at least 25 mils away from any other toggling signal.
27.4 ohm connects with an ~18mil wide trace to comp0.
54.9 ohm connect with 5mil-wide to comp1

Celeron M FSB:533MHz			
	MIN	TYP	MAX
VCC	1.0V	1.2V	1.3V
	C3	C2	C0
ICC	14.7A	16.5A	29Ah

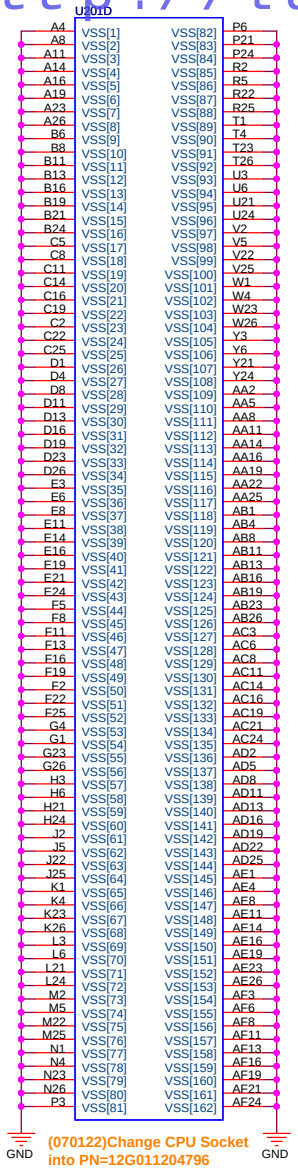
Celeron M FSB:533MHz			
	MIN	TYP	MAX
VCCP	0.997V	1.05V	1.102V
	MIN	TYP	MAX
ICCP			2.5A

Modity Table for Celeron M

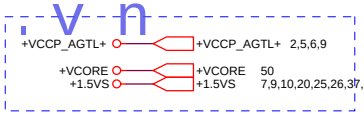


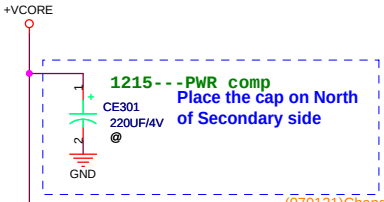
(070122)Change CPU Socket into PN=12G011204796

Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.



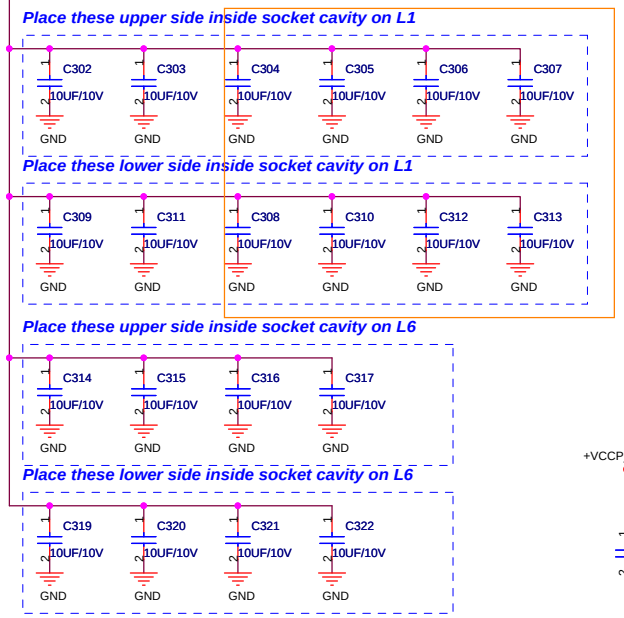
(070122)Change CPU Socket into PN=12G011204796



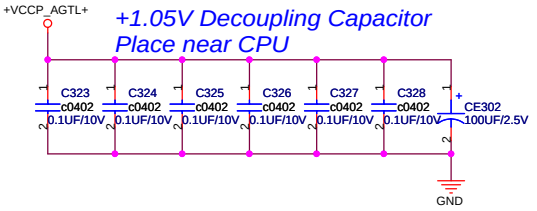


Vcc Core Decoupling Caps
Primary side => Bottom side
Secondary side => Top side

(070131)Change 22UF into 10UF



(061228)Change into 10UF/10V PN:11G236322636360
C302,C303,C309,C311
C314,C315,C316,C317
C319,C320,C321,C322



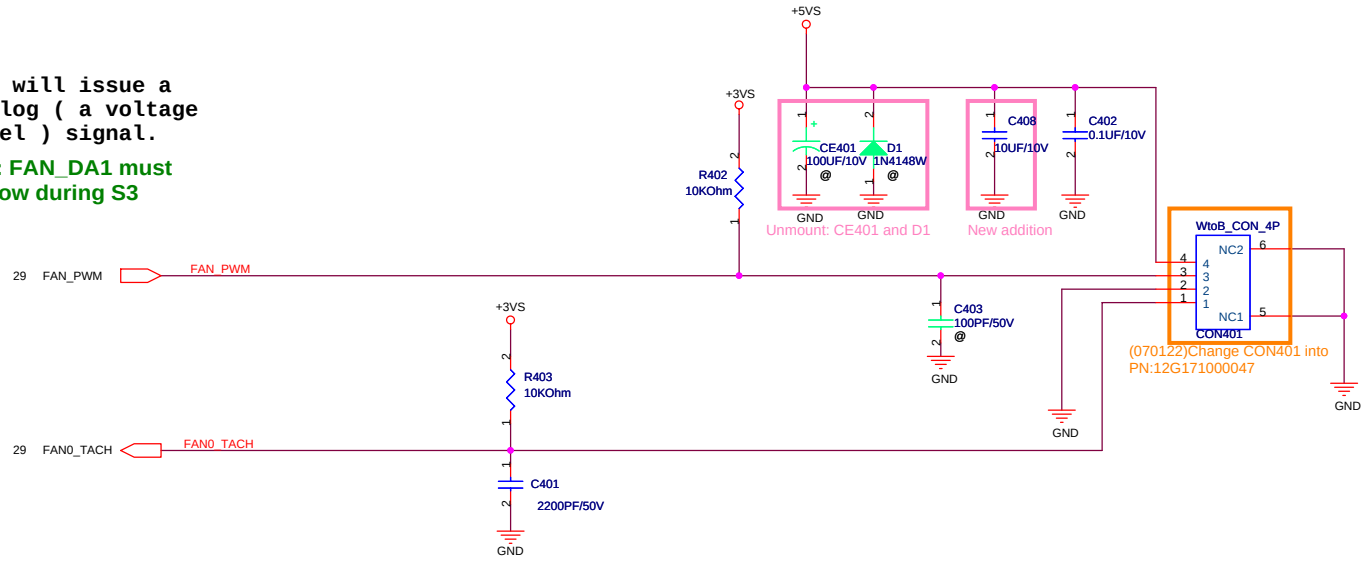
Fan Speed Control

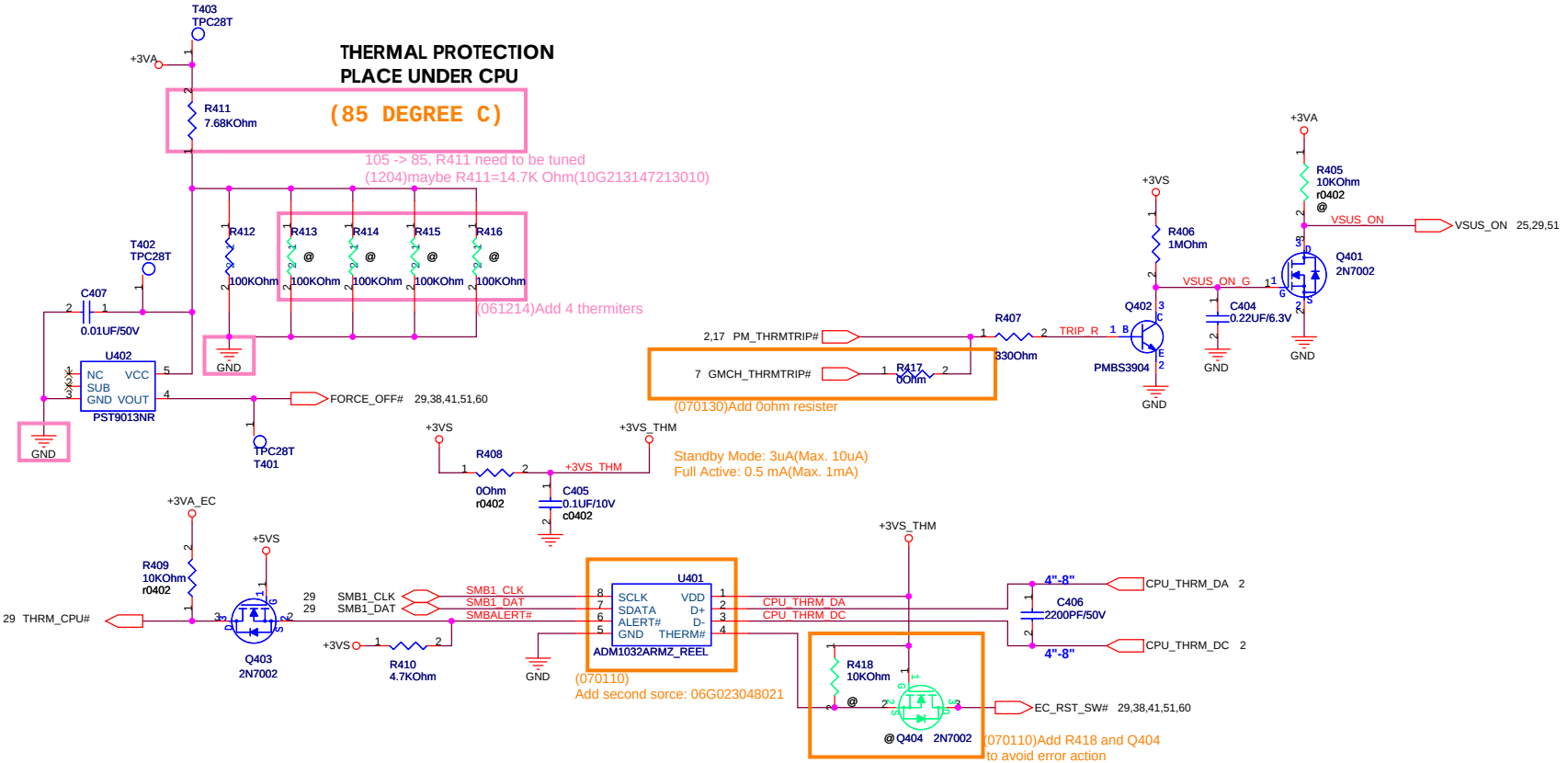
+5VS, +3VS, +3VA

+5VS	+5VS	13,19,20,21,22,28,29,30,34,37,38,50,61
+3VS	+3VS	5,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,40,43,50,52,60,61
+3VA	+3VA	12,22,29,37,38,40,41,54,59,63

KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3





Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#), PCIE7(#)	CLK_MCH_3GPLL(#)

		FSLC	FSLB	FSLA
Bclk	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

+VCCP_AGTL+ → +VCCP_AGTL+ 2,3,6,9

+3VS → +3VS 4,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,40,43,50,52,60,61

R501 @ 1KOhm, R503 @ 1KOhm, R504 @ 1KOhm, R506 @ 1KOhm

CPU_BSEL0 — R502 0Ohm → MCH_BSEL0 7

CPU_BSEL1 — R505 0Ohm → MCH_BSEL1 7

CPU_BSEL2 — R507 0Ohm → MCH_BSEL2 7

GND

+3VS

L501 120Ohm/100Mhz

L502 120Ohm/100Mhz

+3VS_CLK

C501 0.1UF/10V, C502 0.1UF/10V

C503 10UF/10V, C504 0.1UF/10V, C505 0.1UF/10V, C506 0.1UF/10V, C507 0.1UF/10V

+3VS_VDDPCI

C508 0.1UF/10V, C509 0.1UF/10V, C510 10UF/10V

R513 2.2Ohm

C511 0.1UF/10V, C512 10UF/10V

R514 1Ohm

C513 0.1UF/10V

Pin34 is PWRSAVE#

U501

VDDPCIEX1, VDDPCIEX2, VDDPCIEX3 (VDDPCI1, VDDPCI2)

VDD

VDDCPU

VDDA

GNDA

X1

X2

27FIX/LCD_SSCGT/PCIEX0T

27SS/LCD_SSCGC/PCIEX0C

FSLA/USB_48MHz

FSLB/TEST_MODE

SELPCIEX0_LCD#/PCICLK5

PCICLK4

PCICLK3

PCICLK2/REQ_SEL

SELLCD_27#/PCICLK_F1

ITP_EN/PCICLK_F0

SCLK

SDATA

IREF

GND1, GND2, GND3, GND4, GND5, GND6, GND7

VDD48 — +3VS_VDD48

VDDREF — +3VS_VDDREF

PCI/PCIEX_STOP# — STP_PCI# → STP_PCI# 19

CPU_STOP# — STP_CPU# → STP_CPU# 19,50

CPUCLKT1 / CPUCLKC1 — CLK_CPU R526 33Ohm, CLK_CPU# R527 33Ohm → CLK_CPU_BCLK 2, CLK_CPU_BCLK# 2

CPUCLKT0 / CPUCLKC0 — CLK_MCH R523 33Ohm, CLK_MCH# R524 33Ohm → CLK_MCH_BCLK 6, CLK_MCH_BCLK# 6

CPUCLKT2_ITP/PCIEXT8, CPUCLKC2_ITP/PCIEXC8

PEREQ1#/PCIEXT7, PEREQ2#/PCIEXC7 — R531 10KOhm +3VS; PEREQ#2 R534 10KOhm GND; PEREQ#1 R533 0Ohm → CLK_NEWCARD_REQ# 25

PCIEXT6 / PCIEXC6 — PCIE6 R537 33Ohm, PCIE# R538 33Ohm → CLK_PCIE_NEWCARD 25, CLK_PCIE_NEWCARD# 25

PCIEXT5 / PCIEXC5

PCIEXT4 / PCIEXC4 — PCIE4 R542 33Ohm, PCIE# R543 33Ohm → CLK_MCH_3GPLL 7, CLK_MCH_3GPLL# 7

PCIEXT3 / PCIEXC3 — PCIE3 R545 33Ohm, PCIE# R547 33Ohm → CLK_PCIE_MINICARD 26, CLK_PCIE_MINICARD# 26

PCIEXT2 / PCIEXC2 — PCIE2 R549 33Ohm, PCIE# R551 33Ohm → CLK_PCIE_ICH 18, CLK_PCIE_ICH# 18

PCIEXT1 / PCIEXC1

SATACLKT / SATACLKC — CLK_SATA R554 33Ohm, CLK_SATA# R555 33Ohm → CLK_PCIE_SATA 17, CLK_PCIE_SATA# 17

DOTT_96MHz / DOTC_96MHz — DOT96T R556 33Ohm, DOT96C R557 33Ohm → CLK_UMA_96M 7, CLK_UMA_96M# 7

PEREQ3# — MCH_CLK_REQ# 7

PEREQ4# — CLK_MINICARD_REQ# 26

Vtt_PwrGd#/PD — R560 10KOhm @ +3VS_CLK → CLK_EN# 50

REF1/FSLC/TEST_SEL — REF1 R563 2.2KOhm, REF0 R564 33Ohm → CPU_BSEL2 2, CLK_ICH14 19

ICS954310CGLFT

internal pull high

Remove 0ohm

+/-30ppm/20PF

X501 14.318Mhz

C516 33PF/50V, C517 33PF/50V

(070130)Change C516 from 27PF to 33PF

C514 10UF/10V, C515 0.1UF/10V

R517 2.2Ohm

+3VS_VDDA

ICS_X1

ICS_X2

ICS_IREF

R558 475Ohm

C518 10PF/50V, C519 10PF/50V, C520 10PF/50V, C522 10PF/50V, C521 10PF/50V, C522 10PF/50V

7 CLK_LCD_SSCG — R530 33Ohm LCD_SSCG

7 CLK_LCD_SSCG# — R532 33Ohm LCD_SSCG#

19 CLK_USB48, 2 CPU_BSEL0, 2 CPU_BSEL1 — R535 33Ohm FSA, R536 2.2KOhm

34 CLK_LAN_PCI — R539 33Ohm PCICLK5, R540 10KOhm

43 CLK_CBPCI — R541 33Ohm PCICLK4

R544 33Ohm PCICLK3

26 CLK_FWHPCI

29 CLK_ECPCI — R546 33Ohm PCICLK2, R548 10KOhm

+3VS_CLK — R550 10KOhm

18 CLK_ICHPCI — R552 33Ohm PCICLK_F0, R553 10KOhm +3VS_CLK

14,15,19,25,26 SMB_CLK_S

14,15,19,25,26 SMB_DAT_S

Delete CLK_ITPMPCI(connect to pin5)

Realtek:Mount R519,Remove R550 R534

SELPCIE0_LCD#:
0-->pin17,pin18=LCDCLK(96MHz) or 27M/27M_SS

SELLCD_27#/PCICLK_F1:
1-->pin17,pin18=LCDCLK(96MHz)

PCICLK2/REQ_SEL:
1-->pin40,pin41=PREQ1#,PREQ2#

ITP_EN/PCICLK_F0:
1-->CPU_ITP pair

Internal Pull-Up Resistor

Internal Pull-Down Resistor

Layout Note:
Place termination close to source IC

CLK_MCH_BCLK R508 49.9Ohm r0402

CLK_MCH_BCLK# R509 49.9Ohm r0402

CLK_CPU_BCLK R510 49.9Ohm r0402

CLK_CPU_BCLK# R511 49.9Ohm r0402

CLK_PCIE_ICH R512 49.9Ohm r0402

CLK_PCIE_ICH# R515 49.9Ohm r0402

CLK_MCH_3GPLL R516 49.9Ohm r0402

CLK_MCH_3GPLL# R518 49.9Ohm r0402

CLK_LCD_SSCG R519 49.9Ohm r0402

CLK_LCD_SSCG# R521 49.9Ohm r0402

CLK_UMA_96M R522 49.9Ohm r0402

CLK_UMA_96M# R525 49.9Ohm r0402

CLK_PCIE_MINICARD R528 49.9Ohm r0402

CLK_PCIE_MINICARD# R529 49.9Ohm r0402

CLK_PCIE_NEWCARD R566 49.9Ohm r0402

CLK_PCIE_NEWCARD# R567 49.9Ohm r0402

CLK_PCIE_SATA R568 49.9Ohm r0402

CLK_PCIE_SATA# R569 49.9Ohm r0402

GND

PREQ#1
0=PCIEX 6/0 Not Controlled
1=PCIEX 6/0 Controlled

PREQ#2
0=PCIEX 8/1 Not Controlled
1=PCIEX 8/1 Controlled

PREQ#3
0=PCIEX 4/2 Not Controlled
1=PCIEX 4/2 Controlled

PREQ#4
0=PCIEX 7/5/3 Not Controlled
1=PCIEX 7/5/3 Controlled

2 H_D#[0..63]

H_A#[31..3] 2

+VCCP +VCCP 2,9,20,52

+VCCP_AGTL+ +VCCP_AGTL+ 2,3,5,9

U601A

HOST

CALISTOGA_Q137

H_D#0	F1	H_D#_0	
H_D#1	J1	H_D#_1	
H_D#2	H1	H_D#_2	
H_D#3	J6	H_D#_3	
H_D#4	H3	H_D#_4	
H_D#5	K2	H_D#_5	
H_D#6	G1	H_D#_6	
H_D#7	G2	H_D#_7	
H_D#8	K9	H_D#_8	
H_D#9	K1	H_D#_9	
H_D#10	K7	H_D#_10	
H_D#11	J8	H_D#_11	
H_D#12	H4	H_D#_12	
H_D#13	J3	H_D#_13	
H_D#14	K11	H_D#_14	
H_D#15	G4	H_D#_15	
H_D#16	T10	H_D#_16	
H_D#17	W11	H_D#_17	
H_D#18	T3	H_D#_18	
H_D#19	U7	H_D#_19	
H_D#20	U9	H_D#_20	
H_D#21	U11	H_D#_21	
H_D#22	T11	H_D#_22	
H_D#23	W9	H_D#_23	
H_D#24	T1	H_D#_24	
H_D#25	T8	H_D#_25	
H_D#26	T4	H_D#_26	
H_D#27	W7	H_D#_27	
H_D#28	U5	H_D#_28	
H_D#29	T9	H_D#_29	
H_D#30	W6	H_D#_30	
H_D#31	T5	H_D#_31	
H_D#32	AB7	H_D#_32	
H_D#33	AA9	H_D#_33	
H_D#34	W4	H_D#_34	
H_D#35	W3	H_D#_35	
H_D#36	Y3	H_D#_36	
H_D#37	Y7	H_D#_37	
H_D#38	W5	H_D#_38	
H_D#39	Y10	H_D#_39	
H_D#40	AB8	H_D#_40	
H_D#41	W2	H_D#_41	
H_D#42	AA4	H_D#_42	
H_D#43	AA7	H_D#_43	
H_D#44	AA2	H_D#_44	
H_D#45	AA6	H_D#_45	
H_D#46	AA10	H_D#_46	
H_D#47	Y8	H_D#_47	
H_D#48	AA1	H_D#_48	
H_D#49	AB4	H_D#_49	
H_D#50	AC9	H_D#_50	
H_D#51	AB11	H_D#_51	
H_D#52	AC11	H_D#_52	
H_D#53	AB3	H_D#_53	
H_D#54	AC2	H_D#_54	
H_D#55	AD1	H_D#_55	
H_D#56	AD9	H_D#_56	
H_D#57	AC1	H_D#_57	
H_D#58	AD7	H_D#_58	
H_D#59	AC6	H_D#_59	
H_D#60	AB5	H_D#_60	
H_D#61	AD10	H_D#_61	
H_D#62	AD4	H_D#_62	
H_D#63	AC8	H_D#_63	
H_XRCOMP	E1	H_XRCOMP	
H_XSCOMP	E2	H_XSCOMP	
H_XSWING	E4	H_XSWING	
H_YRCOMP	Y1	H_YRCOMP	
H_YSCOMP	U1	H_YSCOMP	
H_YSWING	W1	H_YSWING	
CLK_MCH_BCLK	AG2	H_CLKIN	
CLK_MCH_BCLK#	AG1	H_CLKIN#	

5 CLK_MCH_BCLK

5 CLK_MCH_BCLK#

H_A#_3	H9	H_A#3	
H_A#_4	C9	H_A#4	
H_A#_5	E11	H_A#5	
H_A#_6	G11	H_A#6	
H_A#_7	F11	H_A#7	
H_A#_8	G12	H_A#8	
H_A#_9	F9	H_A#9	
H_A#_10	H11	H_A#10	
H_A#_11	J12	H_A#11	
H_A#_12	G14	H_A#12	
H_A#_13	D9	H_A#13	
H_A#_14	J14	H_A#14	
H_A#_15	H13	H_A#15	
H_A#_16	J15	H_A#16	
H_A#_17	F14	H_A#17	
H_A#_18	D12	H_A#18	
H_A#_19	A11	H_A#19	
H_A#_20	C11	H_A#20	
H_A#_21	A12	H_A#21	
H_A#_22	A13	H_A#22	
H_A#_23	E13	H_A#23	
H_A#_24	G13	H_A#24	
H_A#_25	F12	H_A#25	
H_A#_26	B12	H_A#26	
H_A#_27	B14	H_A#27	
H_A#_28	C12	H_A#28	
H_A#_29	A14	H_A#29	
H_A#_30	C14	H_A#30	
H_A#_31	D14	H_A#31	
H_ADS#	E8	H_ADS#	H_ADS# 2
H_ADSTB#_0	B9	H_ADSTB#0	H_ADSTB#0 2
H_ADSTB#_1	C13	H_ADSTB#1	H_ADSTB#1 2
H_AVREF	J13	H_VREF	
H_BNR#	C6	H_BNR#	H_BNR# 2
H_BPRI#	F6	H_BPRI#	H_BPRI# 2
H_BREQ#0	C7	H_BR0#	H_BR0# 2
H_CPURST#	B7	H_CPURST#	H_CPURST# 2
H_DBSY#	A7	H_DBSY#	H_DBSY# 2
H_DEFER#	C3	H_DEFER#	H_DEFER# 2
H_DPWR#	J9	H_DPWR#	H_DPWR# 2
H_DRDY#	H8	H_DRDY#	H_DRDY# 2
H_DVREF	K13		
H_DINV#_0	J7	H_DINV#0	H_DINV#0 2
H_DINV#_1	W8	H_DINV#1	H_DINV#1 2
H_DINV#_2	U3	H_DINV#2	H_DINV#2 2
H_DINV#_3	AB10	H_DINV#3	H_DINV#3 2
H_DSTBN#_0	K4	H_DSTBN#0	H_DSTBN#0 2
H_DSTBN#_1	T7	H_DSTBN#1	H_DSTBN#1 2
H_DSTBN#_2	Y5	H_DSTBN#2	H_DSTBN#2 2
H_DSTBN#_3	AC4	H_DSTBN#3	H_DSTBN#3 2
H_DSTBP#_0	K3	H_DSTBP#0	H_DSTBP#0 2
H_DSTBP#_1	T6	H_DSTBP#1	H_DSTBP#1 2
H_DSTBP#_2	AA5	H_DSTBP#2	H_DSTBP#2 2
H_DSTBP#_3	AC5	H_DSTBP#3	H_DSTBP#3 2
H_HIT#	D3	H_HIT#	H_HIT# 2
H_HITM#	D4	H_HITM#	H_HITM# 2
H_LOCK#	B3	H_LOCK#	H_LOCK# 2
H_REQ#_0	D8	H_REQ#0	H_REQ#[4..0] 2
H_REQ#_1	G8	H_REQ#1	
H_REQ#_2	B8	H_REQ#2	
H_REQ#_3	F8	H_REQ#3	
H_REQ#_4	A8	H_REQ#4	
H_RS#_0	B4	H_RS#0	H_RS#[0..2] 2
H_RS#_1	E6	H_RS#1	
H_RS#_2	D6	H_RS#2	
H_SLPCPU#	E3	N_CPUSLP#	2 R611 0Ohm 1 H_CPUSLP# 2,17
H_TRDY#	E7	H_TRDY#	H_TRDY# 2

+VCCP_AGTL+

R601 100Ohm 1%

R606 200Ohm 1%

C601 0.1UF/10V

GND GND

<500 mil (55 Ohm)
T/B trace 5.5 ,
Space 25

Layout Note:
0.1uF should be placed 100mils or less from GMCH pin.

+VCCP +VCCP

R602 54.9Ohm 1%

R603 54.9Ohm 1%

5.5/20 mils

H_XSCOMP H_YSCOMP

H_XRCOMP H_YRCOMP

R604 24.9Ohm 1%

R605 24.9Ohm 1%

10/20mils

GND GND

+VCCP

R607 221Ohm 1%

H_XSWING

R608 100Ohm 1%

C602 0.1UF/10V

10/20mils

GND GND

+VCCP

R609 221Ohm 1%

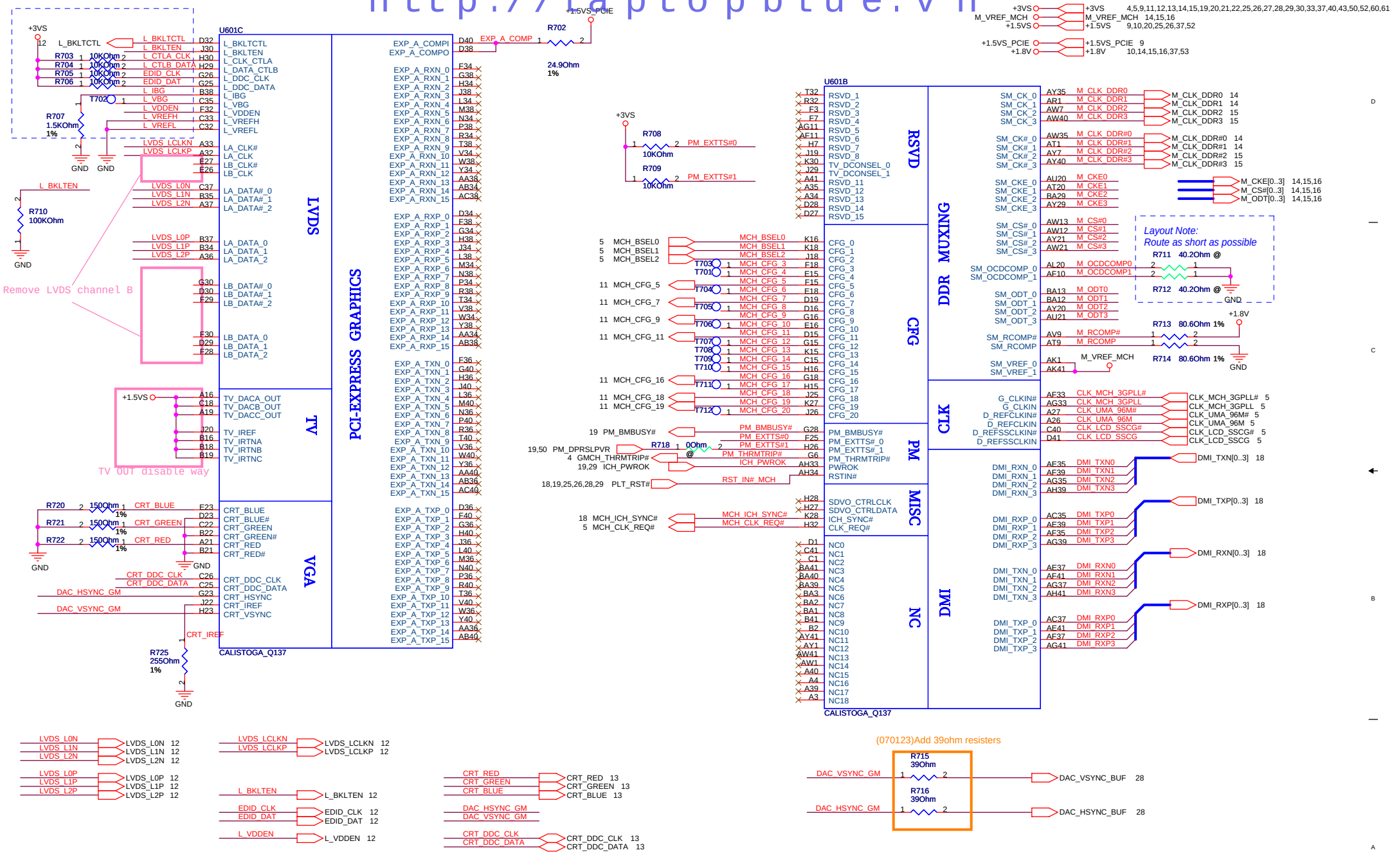
H_YSWING

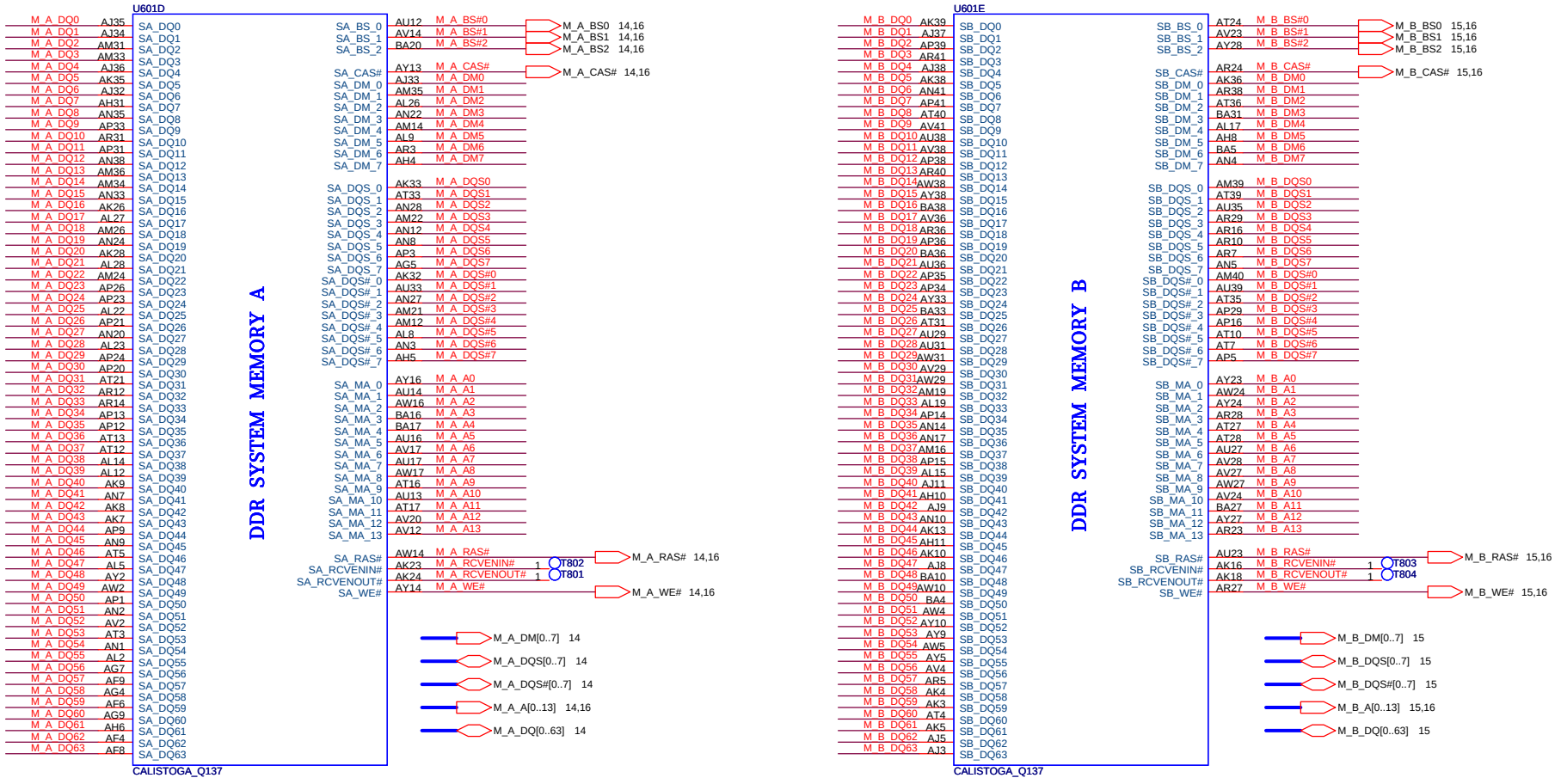
R610 100Ohm 1%

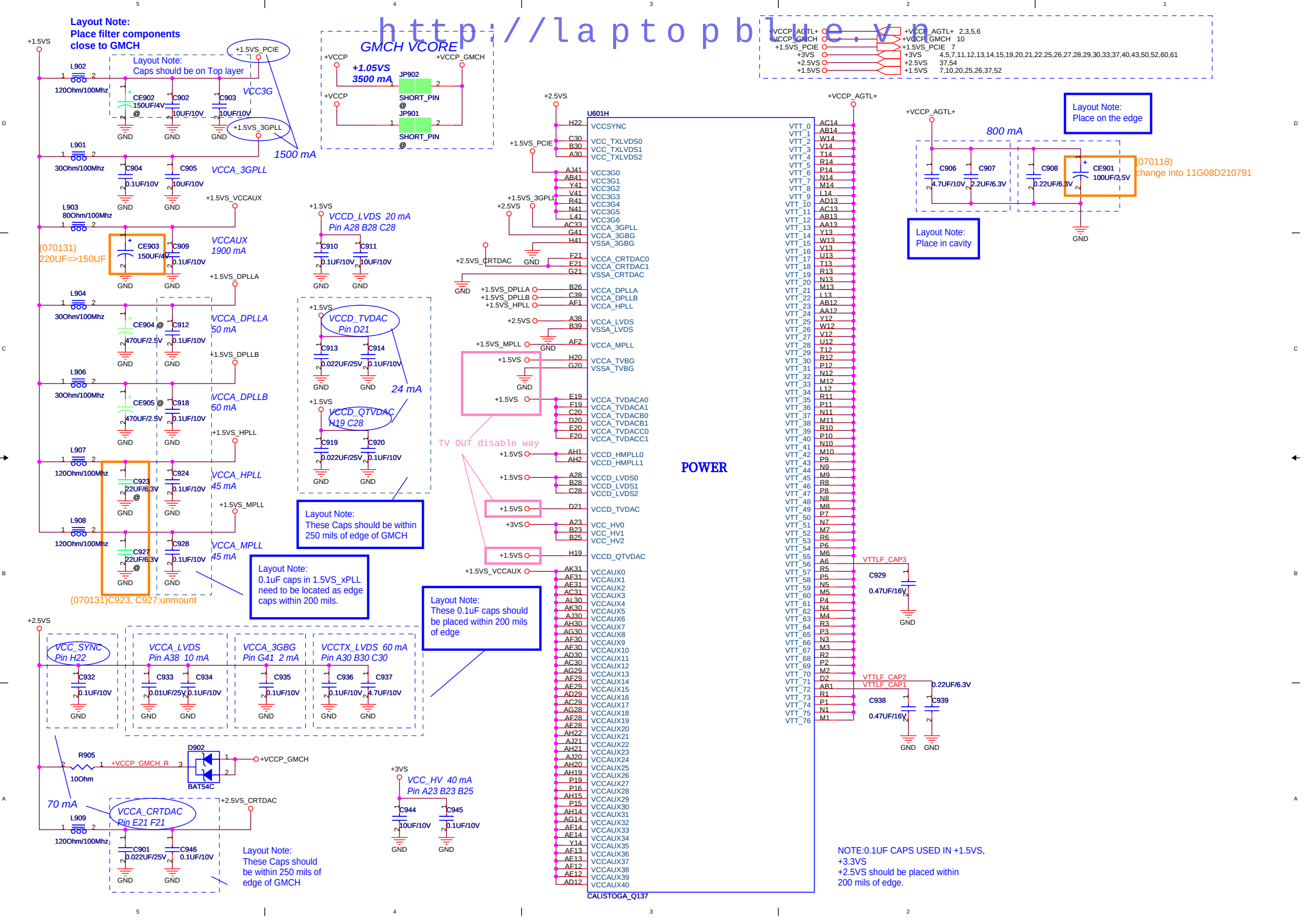
C603 0.1UF/10V

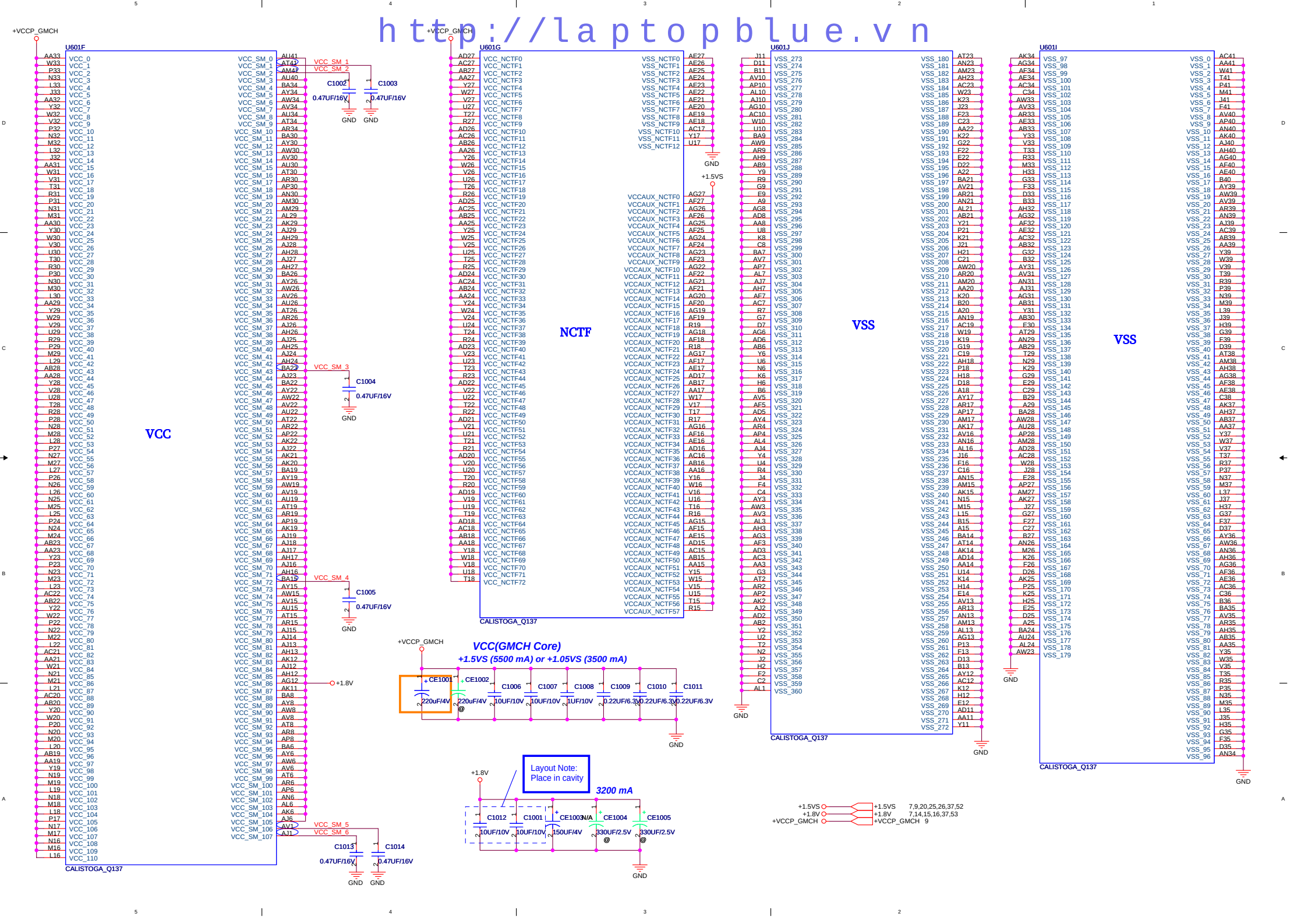
GND GND

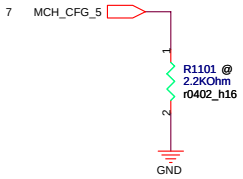
Signal voltage level =
0.3125*VCCP
Trace should be 10 mil wide
with 20 mil spacing



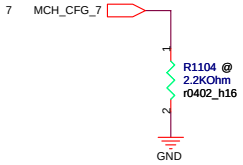




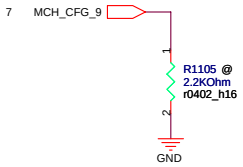




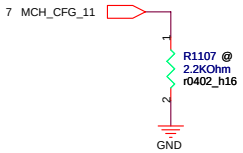
CFG5 : DMI X2 Select
LOW = DMI X 2
HIGH = DMI X 4 (Default)



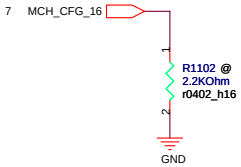
CFG7 : CPU STRAP
LOW = Reserved
HIGH = Mobility CPU (Default)



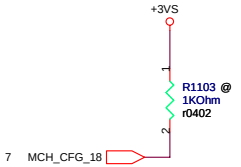
CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANES
HIGH = NORMAL OPERATION (Default)



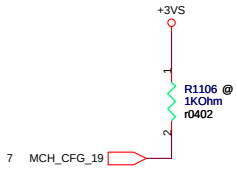
CFG11 : Reserved but need to be pull low



CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG18 : GMCH Core Voltage Level
LOW = 1.05V
HIGH = 1.5V (default)



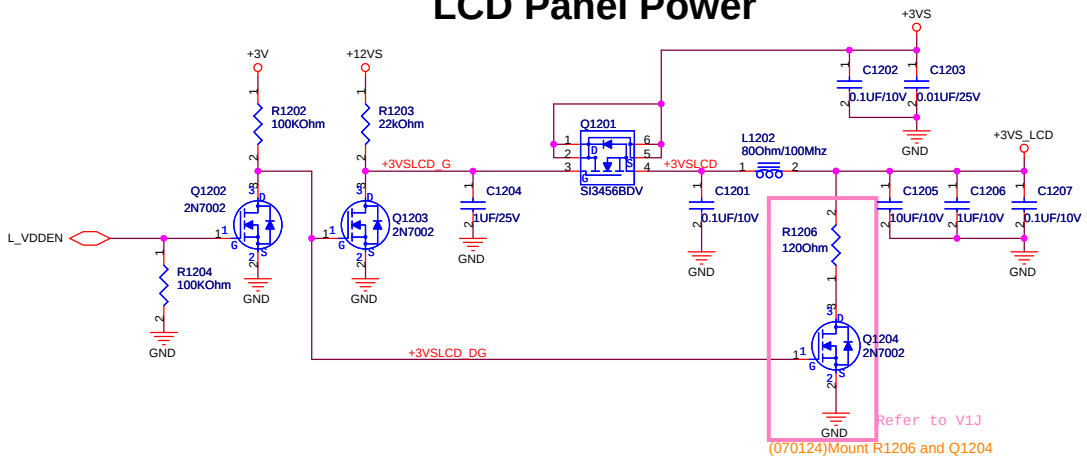
CFG19 : DMI LANE REVERSAL
LOW = NORMAL
HIGH = LANES REVERSED

CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

CFG	All are sampled with respect to the leading edge of the GMCH PWROK	
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4 (Default)
6		
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal (Default)
11:10		
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

3~3.6V
Full Active: 410 mA(Max. 500 mA)
3~3.6V
S0-S1 M: 410 mA(Max. 500 mA)

LCD Panel Power

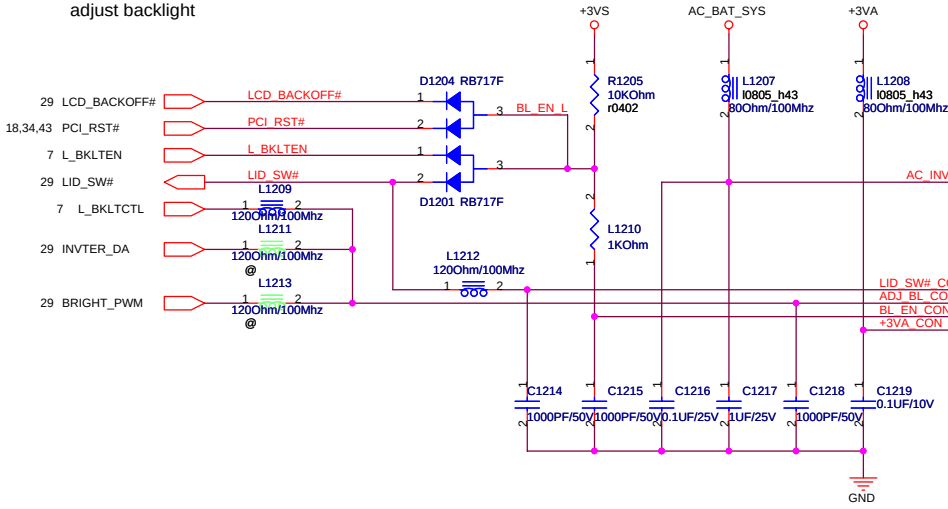


LCD Backlight Control

BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to adjust backlight

Inverter Board built in 15.4W LCD Panel



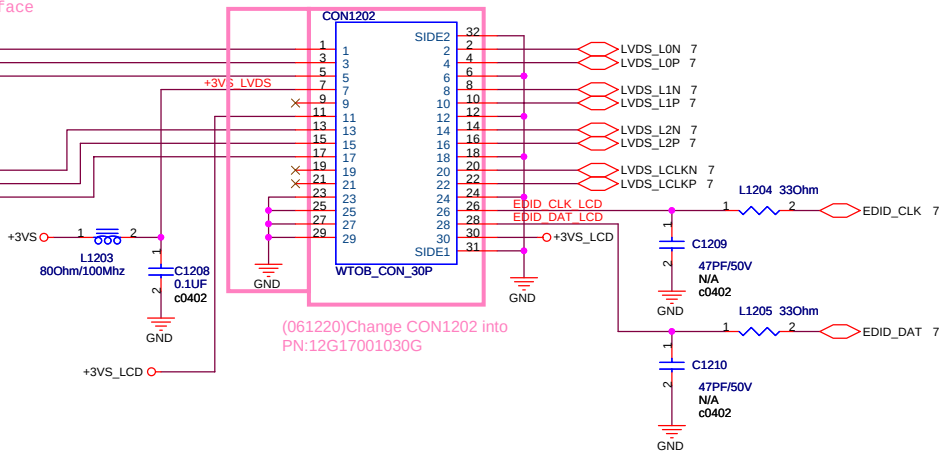
Combine Inverter interface into LVDS interface

(061206,EMI)
Add bead

LCD LVDS & INVERTER Interface

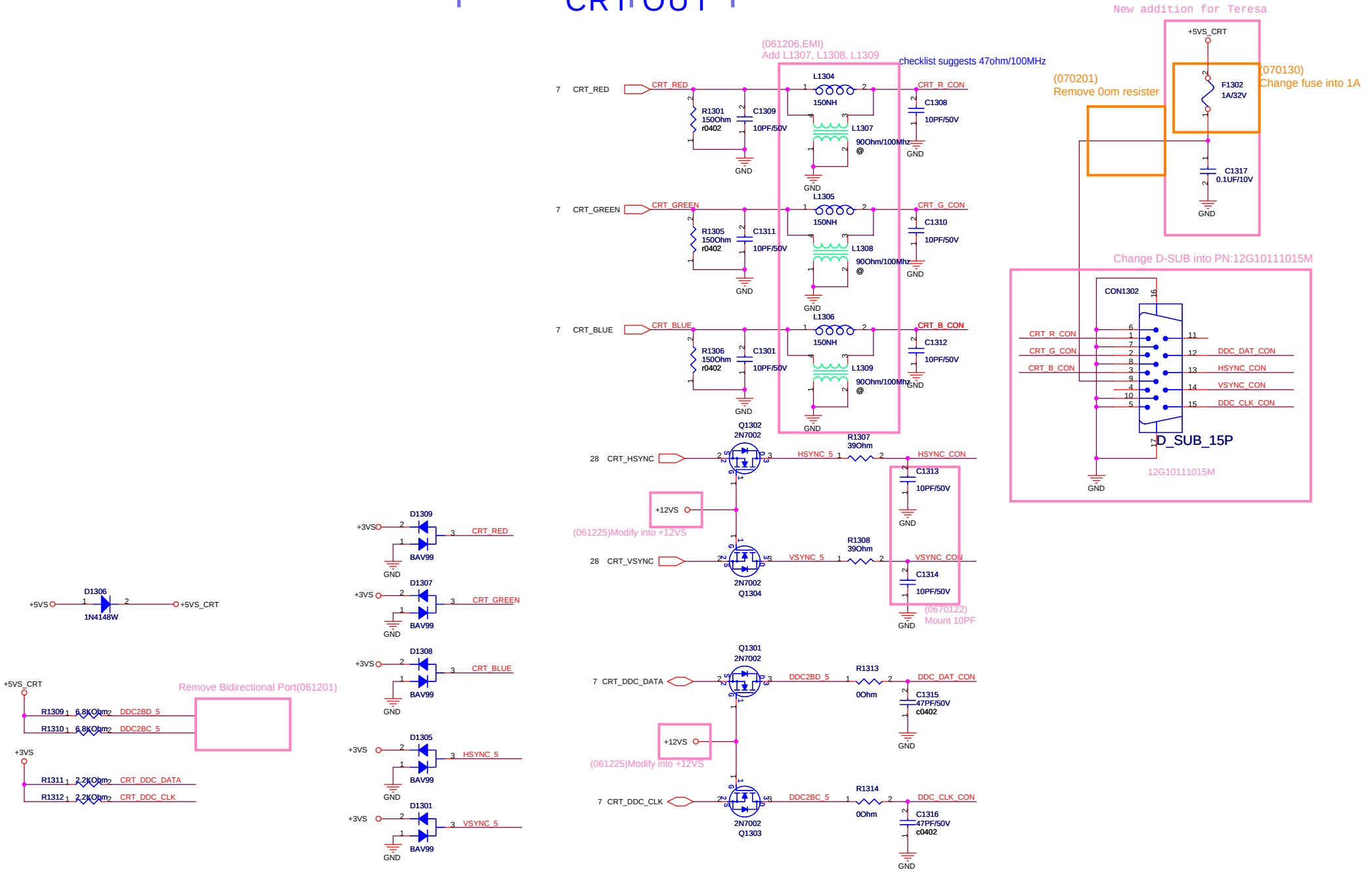
Delete LVDS channel B

Rearrange pin location(061201)

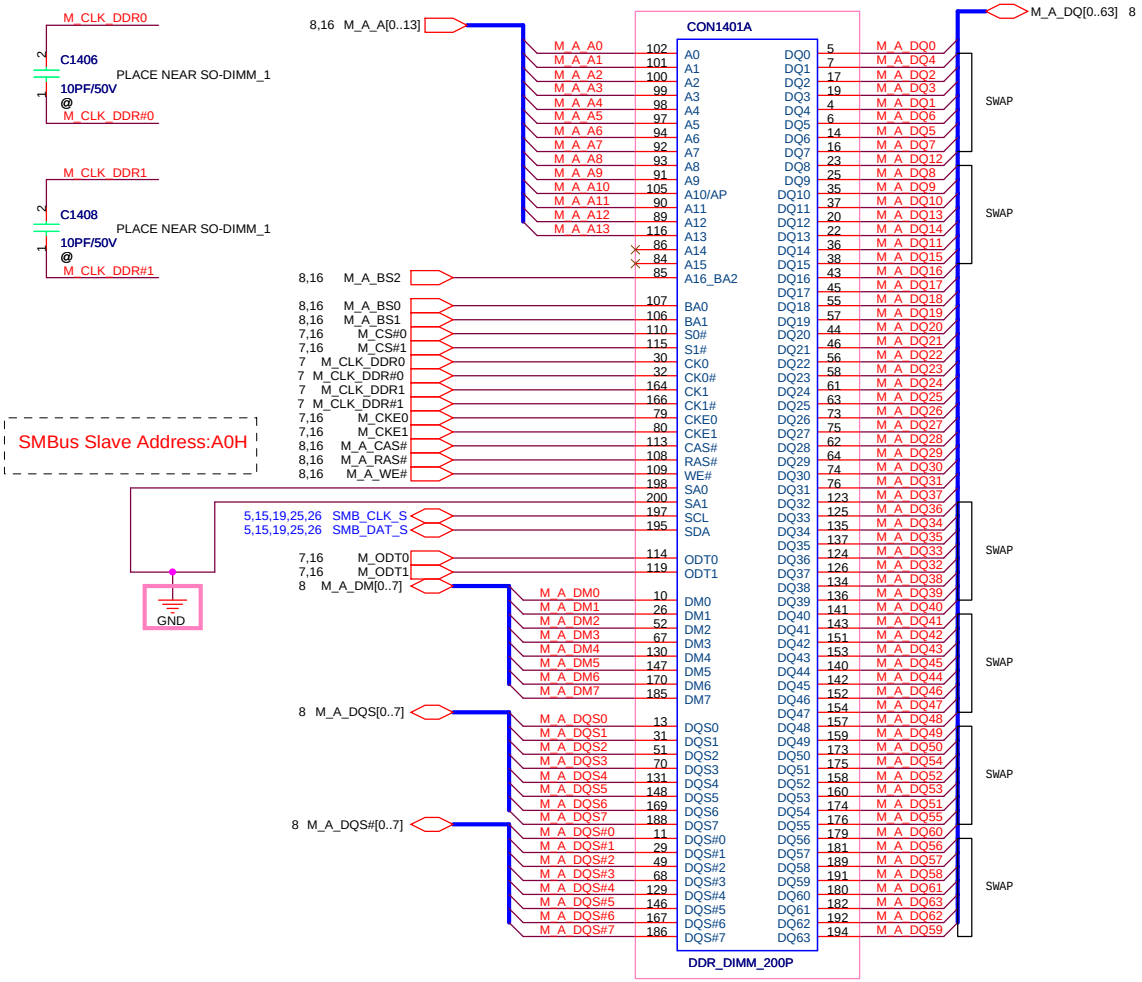


(061220)Change CON1202 into PN:12G17001030G

CRTOUT

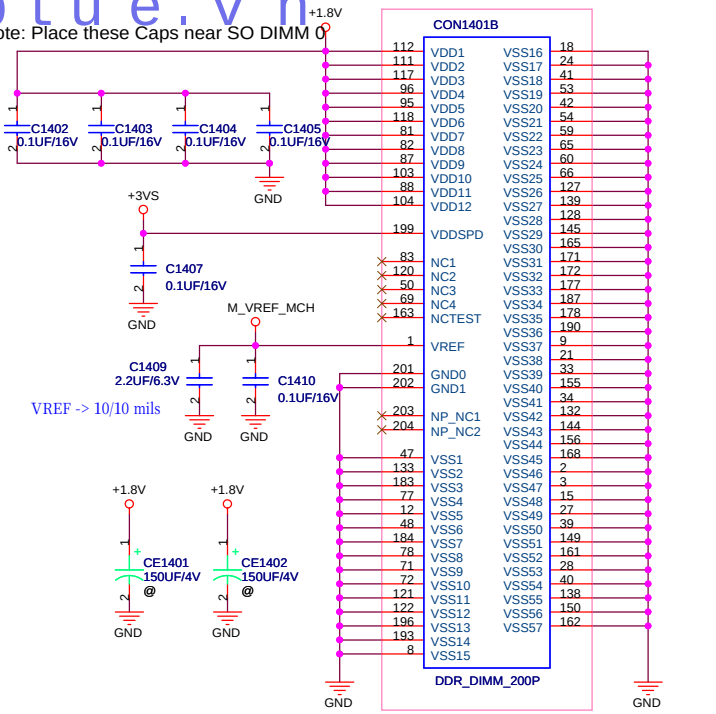


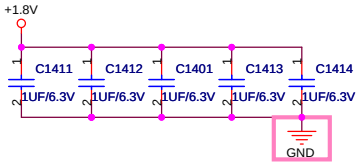
(061221)Change CON1401 into PN:12G02502200R

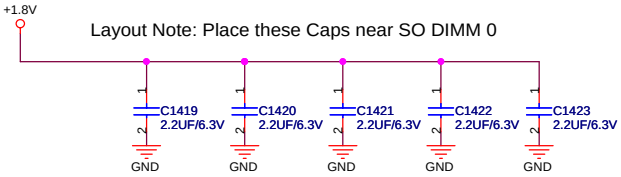


(061221)Change CON1401 into PN:12G02502200R

Layout Note: Place these Caps near SO DIMM 0







SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1

SMBus Slave Address:A4H

Address reference +1.8V, add four 0.1uF decoupling CAP.

(061227)Update PCB footprint
PN:12G025032008

CON1501A

DDR_DIMM_200P

SWAP

SWAP

SWAP

M_CLK_DDR2
C1507 PLACE NEAR SO-DIMM_0
10PF/50V
@
M_CLK_DDR#2

M_CLK_DDR3
C1509 PLACE NEAR SO-DIMM_0
10PF/50V
@
M_CLK_DDR#3

8,16 M_B_A[0..13]
8 M_B_DQ[0..63]
8,16 M_B_BS2
8,16 M_B_BS0
8,16 M_B_BS1
7,16 M_CS#2
7,16 M_CS#3
7 M_CLK_DDR3
7 M_CLK_DDR#3
7 M_CLK_DDR2
7 M_CLK_DDR#2
7,16 M_CKE2
7,16 M_CKE3
8,16 M_B_CAS#
8,16 M_B_RAS#
8,16 M_B_WE#
+3VS_SET

+3VS
R1501
10KOhm
GND

5,14,19,25,26 SMB_CLK_S
5,14,19,25,26 SMB_DAT_S

7,16 M_ODT2
7,16 M_ODT3
8 M_B_DM[0..7]
8 M_B_DQS[0..7]
8 M_B_DQS#[0..7]

Layout Note: Place these Caps near SO DIMM 0

+3VS
C1506
0.1UF/16V
GND

M_VREF_MCH
VREF -> 10/10 mils
C1508
1UF/6.3V
C1501
0.1UF/16V
GND

CON1501B
DDR_DIMM_200P

Layout Note: Place these Caps near SO DIMM 0

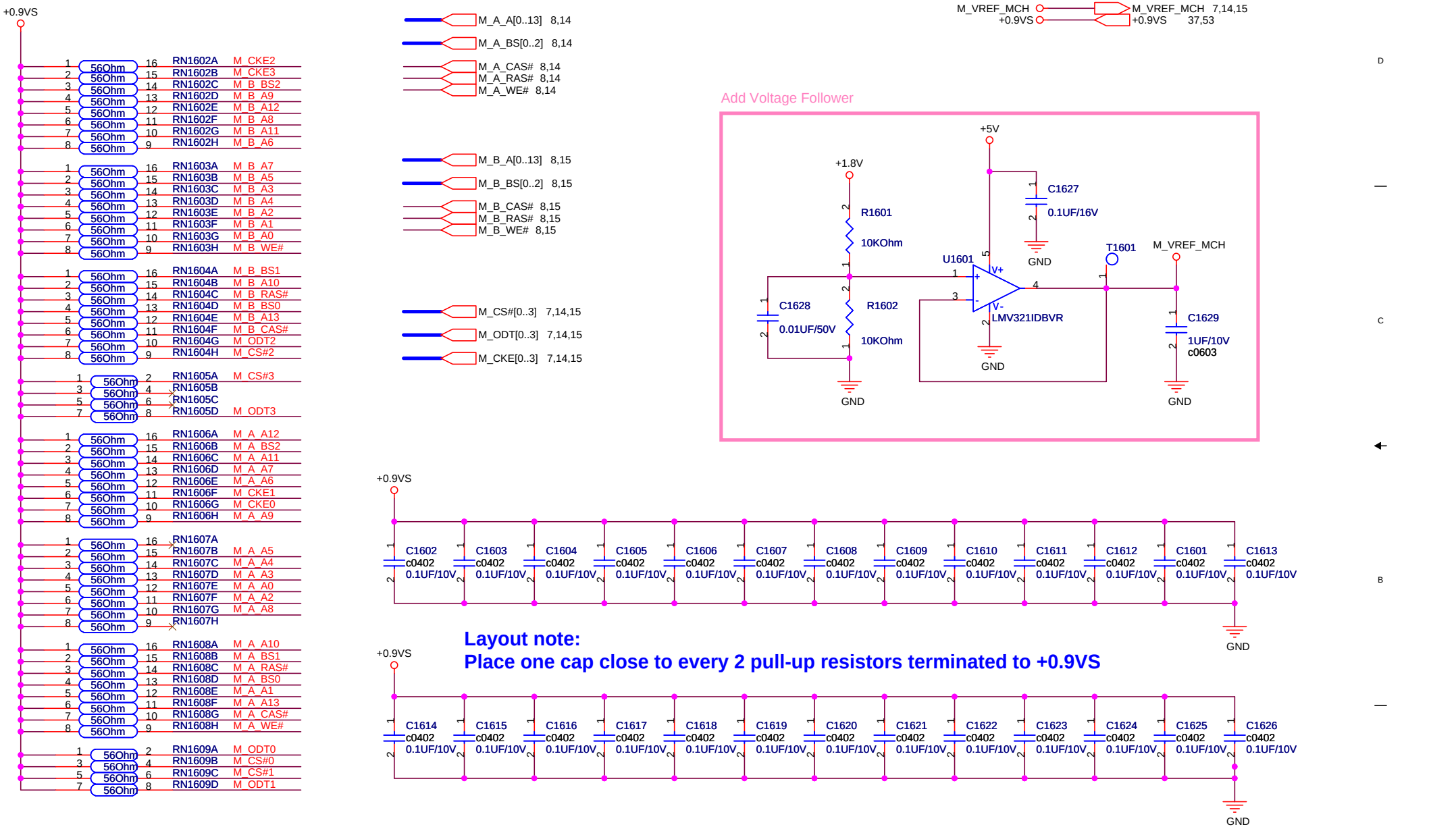
+1.8V
C1510
C1511
C1512
C1513
0.1UF/16V
GND

Layout Note: Place these High-Freq decoupling Caps near the GMCH

C1514
C1515
C1516
C1517
0.1UF/16V
c0402
GND

Layout Note: Place these CAPs near the GMCH

C1518
C1519
C1520
C1521
C1522
2.2UF/6.3V
GND



M_A_A[0..13] 8,14
M_A_BS[0..2] 8,14
M_A_CAS# 8,14
M_A_RAS# 8,14
M_A_WE# 8,14

M_B_A[0..13] 8,15
M_B_BS[0..2] 8,15
M_B_CAS# 8,15
M_B_RAS# 8,15
M_B_WE# 8,15

M_CS#[0..3] 7,14,15
M_ODT[0..3] 7,14,15
M_CKE[0..3] 7,14,15

M_VREF_MCH
+0.9VS
M_VREF_MCH 7,14,15
+0.9VS 37,53

Add Voltage Follower

Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS

+VCC_RTC
R1701 2 1 RTCRST#
20KOhm
C1704 1UF/16V
JRST1 1 2 2 @
GND (061227)Change reference from JRST1701 to JRST1

C1702 2 1 18PF/50V X1701
SIDE 1 2 3
C1703 2 1 18PF/50V
32.768KHZ
RTC_X1
R1702 10MOhm
RTC_X2
GND

+1.5VS_PCIE_ICH +1.5VS_PCIE_ICH 18,20
+VCCP_ICH +VCCP_ICH 20
+VCC_RTC +VCC_RTC 20
+VCCP +VCCP 2,6,9,20,52
+1.5VS +1.5VS 7,9,10,20,25,26,37,52
+5VS +5VS 4,13,19,20,21,22,28,29,30,34,37,38,50,61
+3VS +3VS 4,5,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,40,43,50,52,60,61
+3VA +3VA 4,12,22,29,37,38,40,41,54,59,63

Delete LPC interface of TPM

LPC_AD0_ICH R1728 33Ohm LPC_AD0 LPC_AD0 26,29
LPC_AD1_ICH R1720 33Ohm LPC_AD1 LPC_AD1 26,29
LPC_AD2_ICH R1722 33Ohm LPC_AD2 LPC_AD2 26,29
LPC_AD3_ICH R1724 33Ohm LPC_AD3 LPC_AD3 26,29
LPC_FRAME#_ICH R1726 33Ohm LPC_FRAME# LPC_FRAME# 26,29

close to ICH7

R1708 39Ohm
21 ACZ_BCLK_AUD
35 ACZ_BCLK_MDC
ACZ_BCLK
R1732 39Ohm

R1710 39Ohm
21 ACZ_SYNC_AUD
35 ACZ_SYNC_MDC
ACZ_SYNC
R1731 39Ohm

R1714 39Ohm
21,22 ACZ_RST#_AUD
ACZ_RST#
R1729 39Ohm
35 ACZ_RST#_MDC

R1717 39Ohm
21 ACZ_SDOUT_AUD
ACZ_SDOUT
R1730 39Ohm
35 ACZ_SDOUT_MDC

U1701A

+VCC_RTC
R1703 1MOhm
R1704 330KOhm
RTC_X1 AB1
RTC_X2 AB2
RTCRST# AA3
INTRUDER# Y5
INTVRMEN W4
RTC

EE_CS W1
EE_SHCLK Y1
EE_DOUT Y2
EE_DIN W3
LAN_CLK V3
LAN_RSTSYNC U3
LAN_RXD0 U5
LAN_RXD1 V4
LAN_RXD2 T5
LAN_TXD0 U7
LAN_TXD1 V6
LAN_TXD2 V7
LAN

ACZ_BCLK U1
ACZ_SYNC R6
ACZ_RST# R5
ACZ_SDIN0 T2
ACZ_SDIN1 T3
ACZ_SDIN2 T1
ACZ_SDOUT T4
21 ACZ_SDIN0
35 ACZ_SDIN1
T1703
AC-97/AZALIA

30 SATA_LED# AF18
SATA_RXN0 AF3
SATA_RXP0 AF3
SATA_TXN0 AG2
SATA_TXP0 AH2
C1705 3900PF/50V SATA_TXN0_ICH
C1701 3900PF/50V SATA_TXP0_ICH
Change to 3900PF
Remove 0 ohm
SATA2_R AE7
SATA2_TN AG6
SATA2_TP AH6
T1704
T1705
GND
5 CLK_PCIE_SATA# AE1
5 CLK_PCIE_SATA AE1
R1719 24.9Ohm 1% SATA2_RBIAS AH10 AG10
GND
SATA

28 IDE_PDIOR# IDE_PDIOR#_ICH AF15
28 IDE_PDIOW# IDE_PDIOW# AH15
28 IDE_PDDACK# IDE_PDDACK# AF16
28 INT_IRQ14 INT_IRQ14 AH16
28 IDE_PIORDY IDE_PIORDY AG16
28 IDE_PDDREQ IDE_PDDREQ AE15
IDE

ICH7M

LAD0 AA6 LPC_AD0_ICH
LAD1 AB5 LPC_AD1_ICH
LAD2 AC4 LPC_AD2_ICH
LAD3 Y6 LPC_AD3_ICH
LDRQ0# AC3 LPC_DRQ#0 LPC_DRQ#0 19
LDRQ1#/GPIO23 AA5 LPC_DRQ#1 T1702
LFRAME# AB3 LPC_FRAME#_ICH

A20GATE AE22 A20GATE A20GATE 29
A20M# AH28 H_A20M# H_A20M# 2
CPUSLP# AG27 S_CPUSLP# R1705 @ 0Ohm H_CPUSLP# 2,6
TP1/DPRSTP# AE24 S_DPRSTP# R1707 @ 0Ohm H_DPRSTP# 2,60
TP2/DPSLP# AH25 H_DPSLP# H_DPSLP# 2
FERR# AG26 H_FERR# H_FERR# 2
GPIO49/CPUPWRGD AG24 H_PWRGD H_PWRGD 2
+VCCP_ICH
R1706 56Ohm

IGNNE# AG22 H_IGNNE# H_IGNNE# 2
INIT3_3V# AG21 INIT3_3V# T1701
INIT# AE22 H_INIT# H_INIT# 2
INTR AE25 H_INTR H_INTR 2
RCIN# AG23 RCIN# RCIN# 29
NMI AH24 H_NMI H_NMI 2
SMI# AF23 H_SMI# H_SMI# 2
STPCLK# AH22 H_STPCLK# H_STPCLK# 2
THERMTRIP# AF26 S_THRMTRIP# R1713 24.9Ohm 1% PM_THRMTRIP# 2,4
+VCCP_ICH
R1711 56Ohm
CPU

DD0 AB15 IDE_PDD0 IDE_PDD0 28
DD1 AE14 IDE_PDD1_ICH IDE_PDD1 28
DD2 AG13 IDE_PDD2_ICH IDE_PDD2 28
DD3 AF13 IDE_PDD3 IDE_PDD3 28
DD4 AD14 IDE_PDD4 IDE_PDD4 28
DD5 AC13 IDE_PDD5 IDE_PDD5 28
DD6 AD12 IDE_PDD6 IDE_PDD6 28
DD7 AC12 IDE_PDD7 IDE_PDD7 28
DD8 AE12 IDE_PDD8 IDE_PDD8 28
DD9 AF12 IDE_PDD9_ICH IDE_PDD9 28
DD10 AB13 IDE_PDD10_ICH IDE_PDD10 28
DD11 AC14 IDE_PDD11 IDE_PDD11 28
DD12 AE14 IDE_PDD12 IDE_PDD12 28
DD13 AH13 IDE_PDD13 IDE_PDD13 28
DD14 AH14 IDE_PDD14 IDE_PDD14 28
DD15 AC15 IDE_PDD15 IDE_PDD15 28
DA0 AH17 IDE_PDA0 IDE_PDA0 28
DA1 AE17 IDE_PDA1 IDE_PDA1 28
DA2 AE17 IDE_PDA2 IDE_PDA2 28
DCS1# AE16 IDE_PDCS1# IDE_PDCS1# 28
DCS3# AD16 IDE_PDCS3# IDE_PDCS3# 28

DPRSTP# routing from Intel 82801GBM to Yonah processor is required. Routing to VR must be done last and must have de-bounce filtering to handle daisy chain topology.

24 ±5% series termination resistor placed within 2" from Intel 82801GBM, 56 ±5% pull-up resistor has to be within 2" from the series resistor

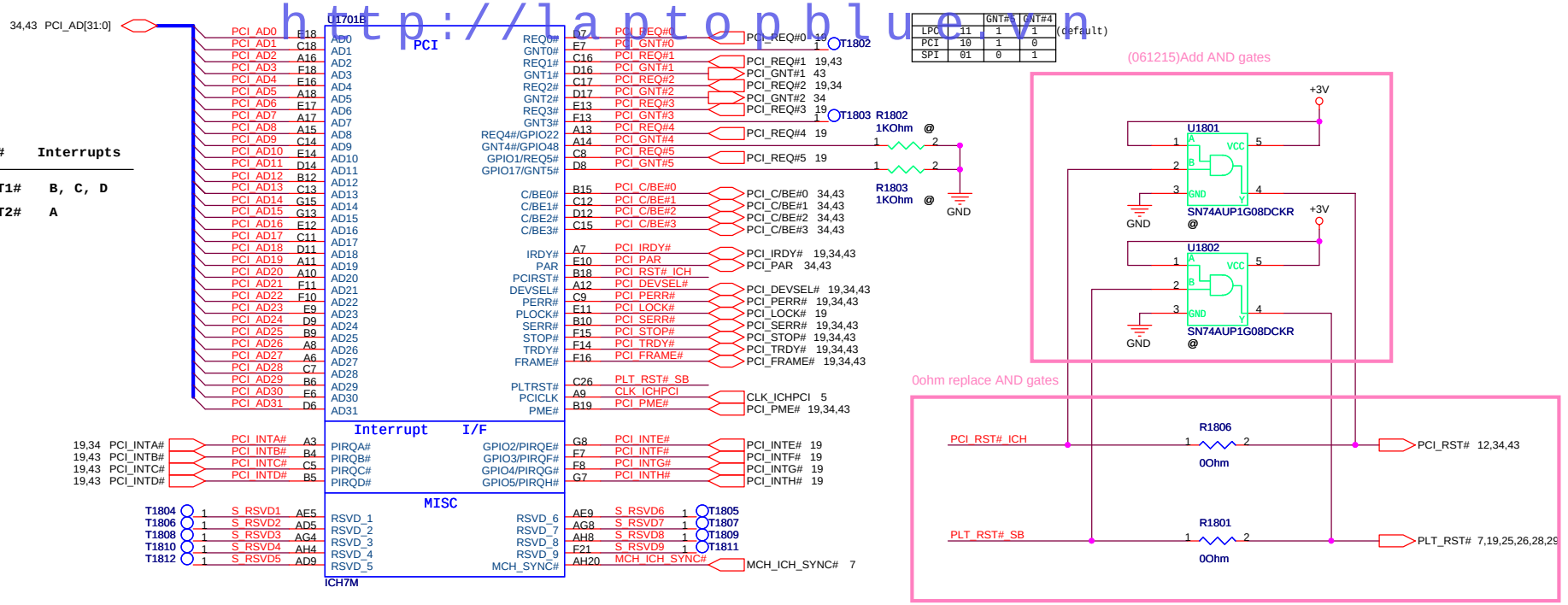
Check with EMI: remove 0 ohm
=>IDE_PDIOR#_ICH
IDE_PDD1_ICH
IDE_PDD2_ICH
IDE_PDD9_ICH
IDE_PDD10_ICH

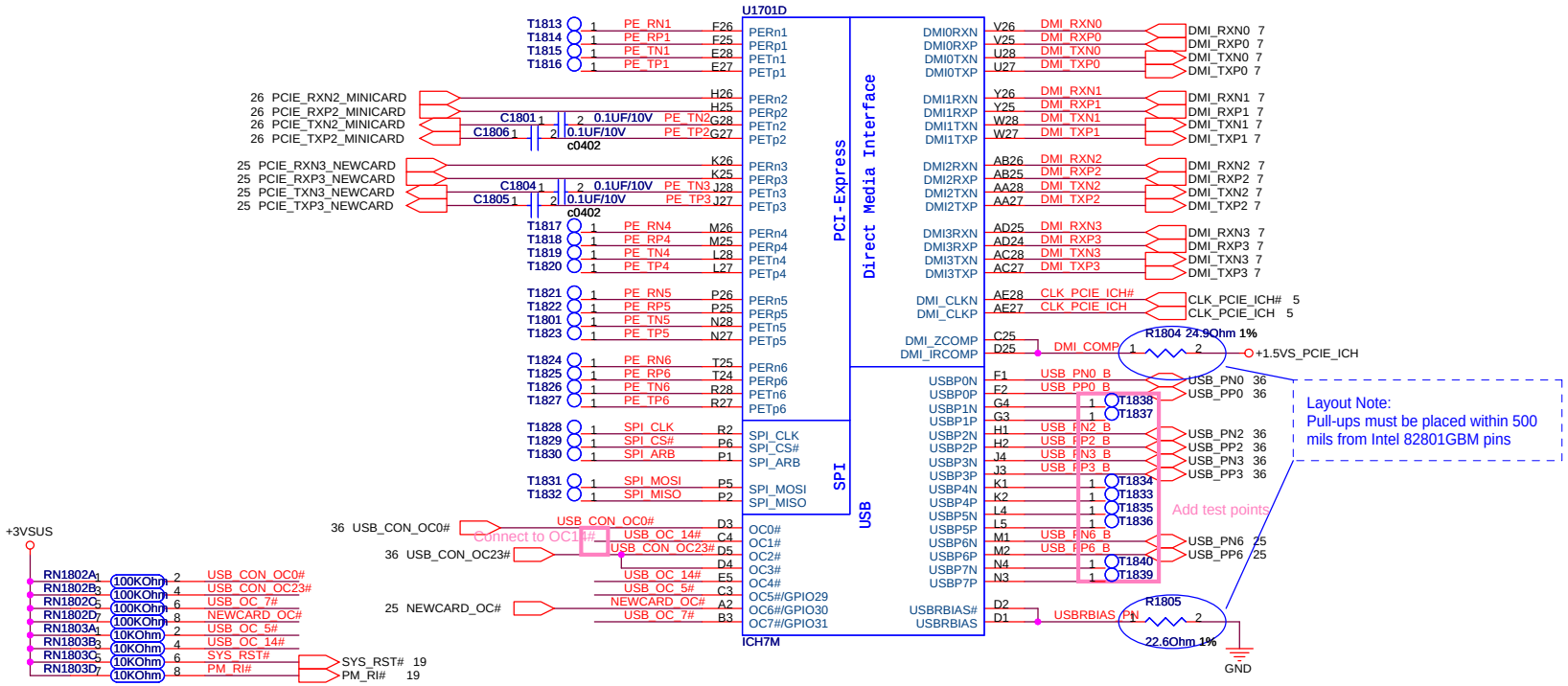
ACZ_SDOUT	PWROK rising	TP3 pull low: allow entrance to XOR Chain testing TP3 not pull low: sets bit 1 of RPC.PC	PD
ACZ_SYNC	PWROK rising	sets bit 0 of RPC.PC	PD
EE_CS		should not be pulled high	PD
EE_DOUT		should not be pulled low	PU
GNT2#		should not be pulled low	PU
GNT3#	PWROK rising	low: "top-block swap" mode	PU
GNT5#/GPIO17# GNT4#/GPIO48	PWROK rising	GNT5# GNT4# 0 1 SPI 1 0 PCI 1 1 LPC	PU

GPIO16 /DPRSLPVR		should not be pulled high	PD
GPIO25	RSMRST# rising	should not be pulled low	PU
INTVRMEN	ALWAYS	high: Enable integrated VccSus1_05 VRM	
LINKALERT#		REQUIRE an extenal pull-up R	Need PU
REQ[4:1]#	PWROK rising		
SATALED#		should not be pulled low	Conditional PU
SPKR	PWROK rising	high: "No reboot" mode	PD
TP3	PWROK rising	should not be pulled low unless using XOR Chain testing	PU

PCI Device

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A

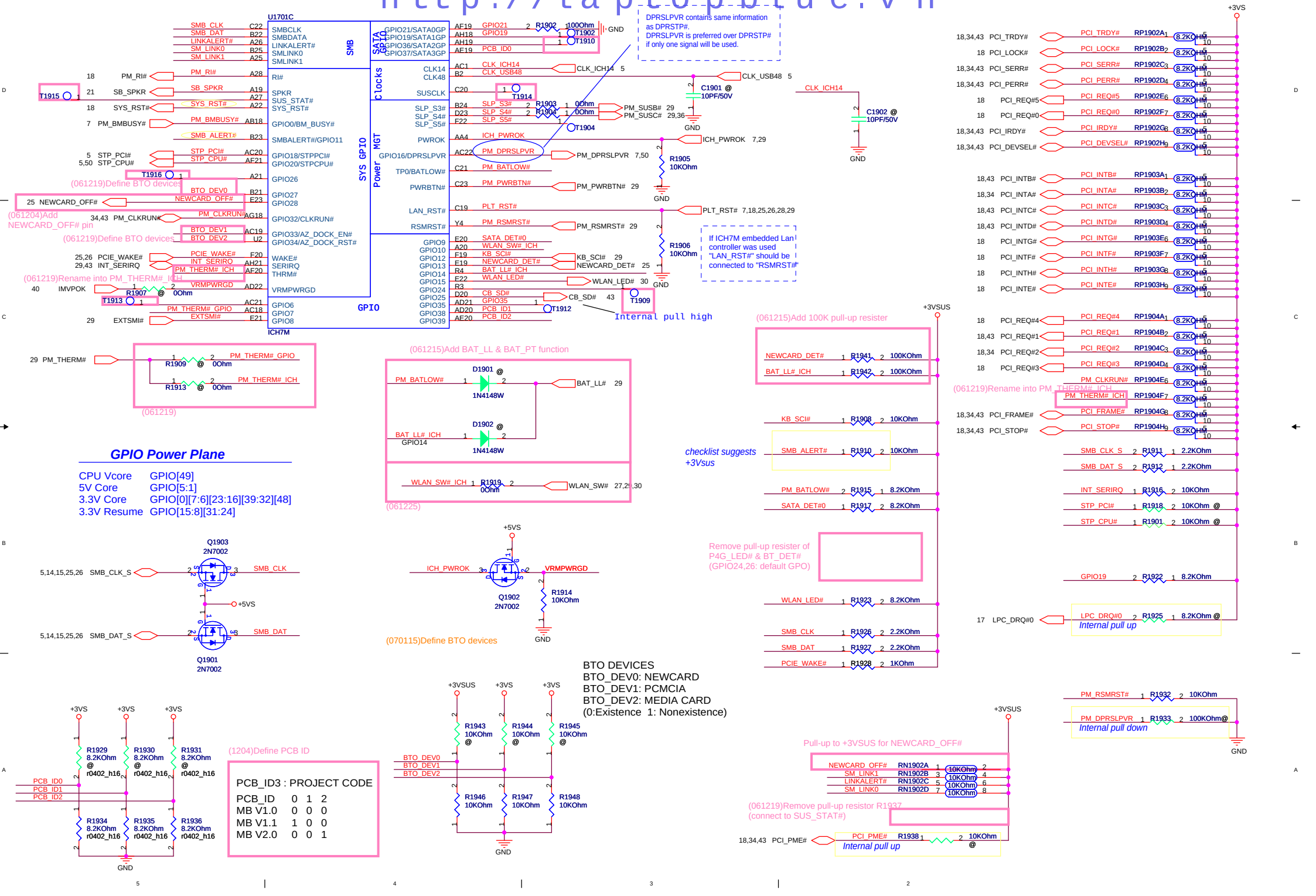




Modify USB Device table

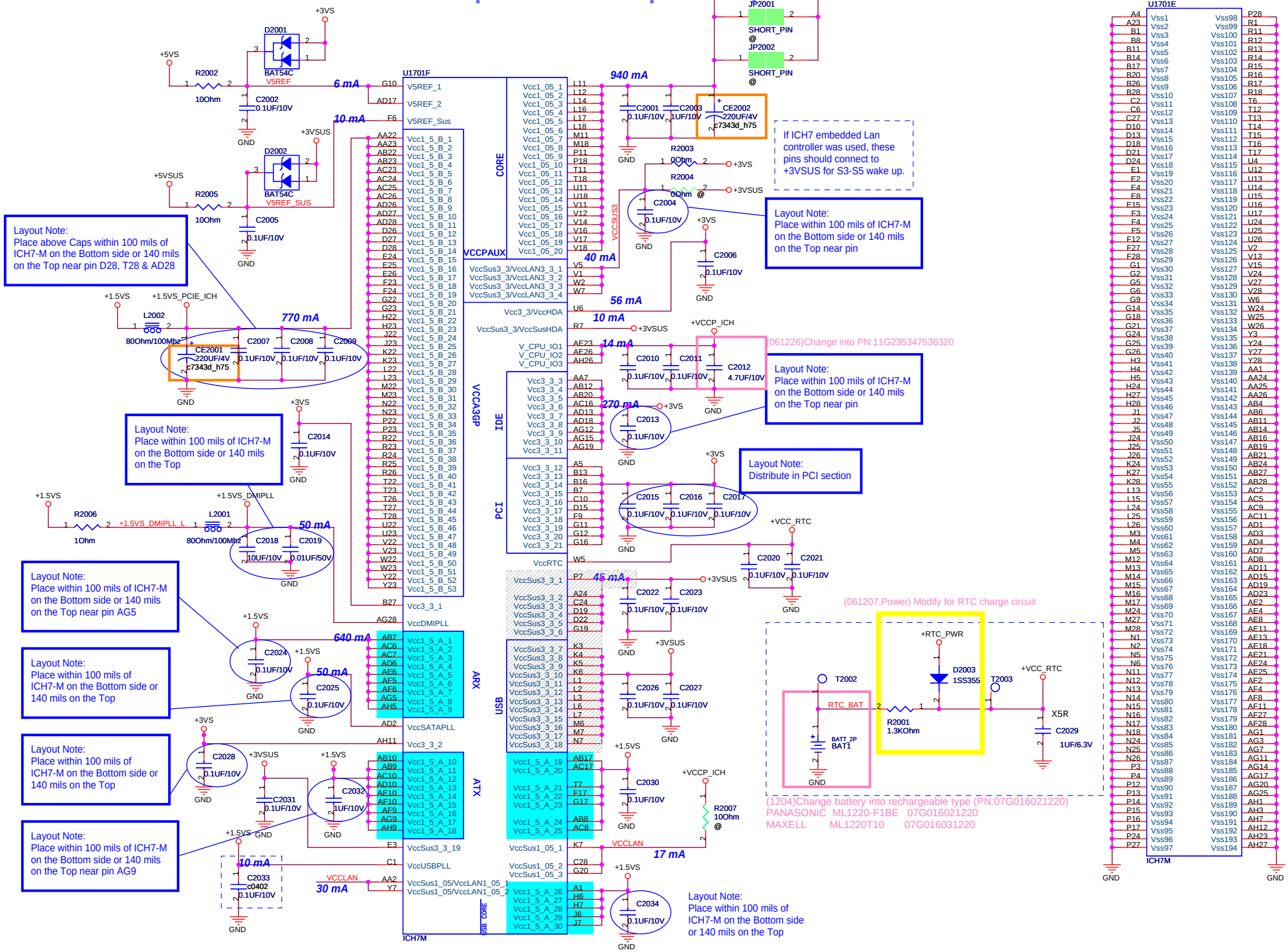
USB Devices

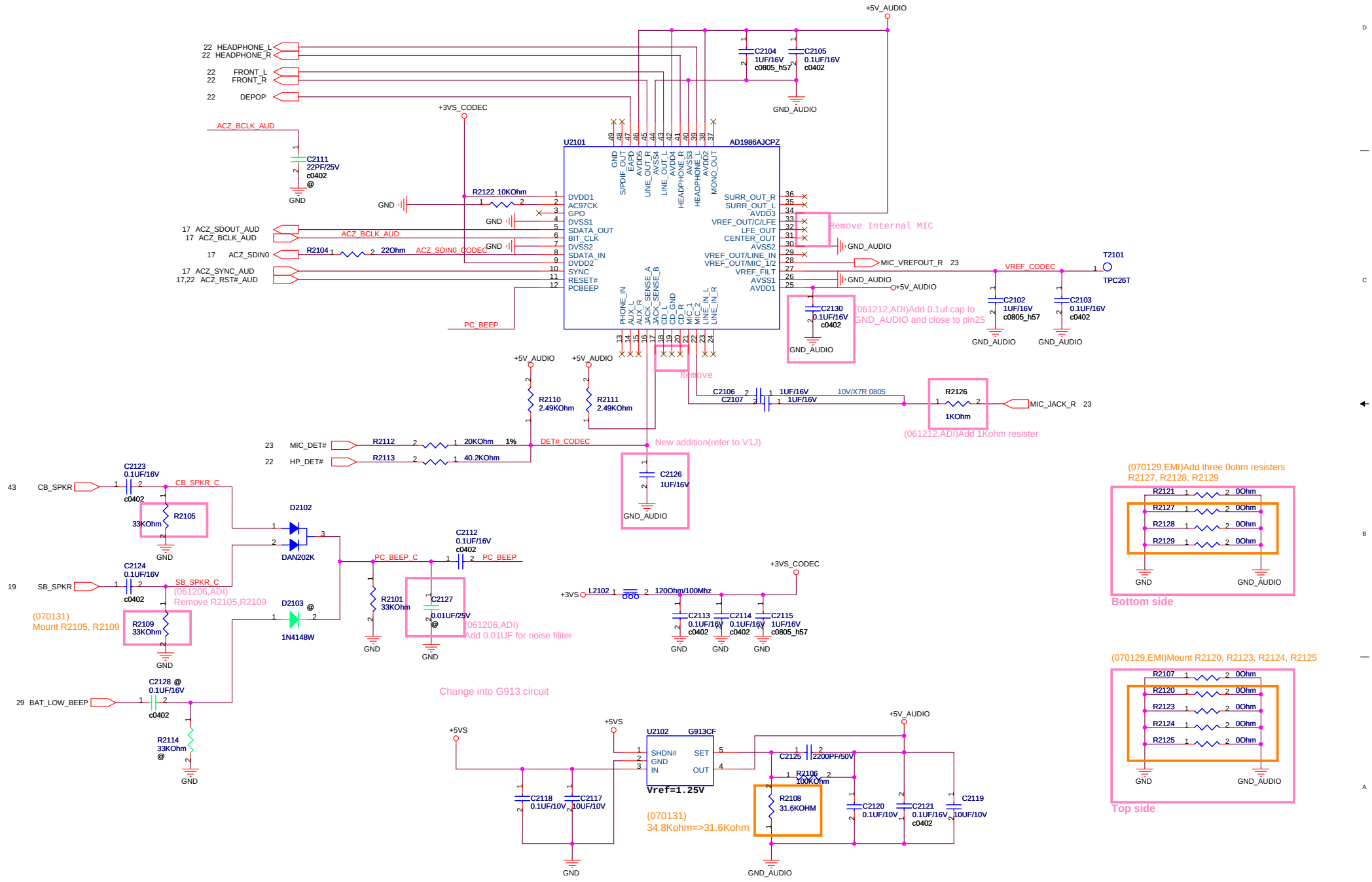
Port 0	CON3602
Port 1	Unused
Port 2	CON3601
Port 3	CON3601
Port 4	Unused
Port 5	Unused
Port 6	NewCard
Port 7	Unused

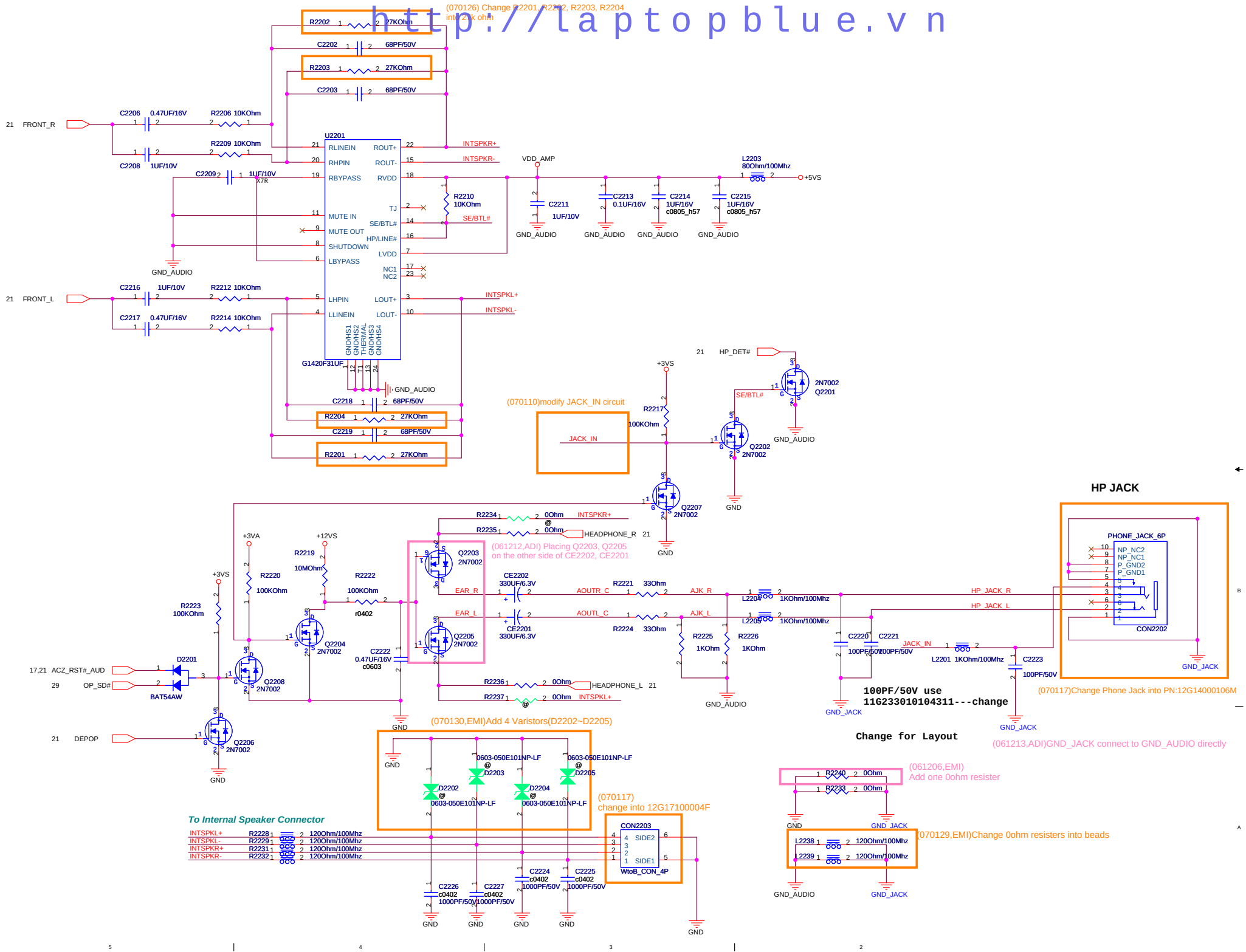


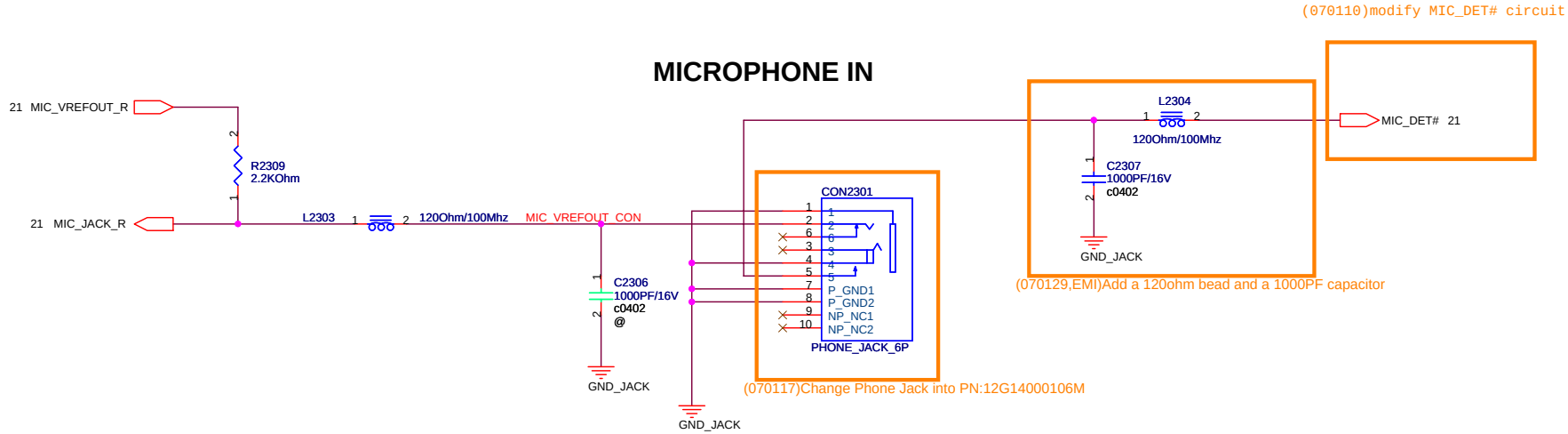
GPIO Power Plane

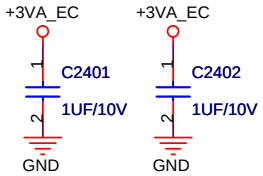
CPU Vcore	GPIO[49]
5V Core	GPIO[5:1]
3.3V Core	GPIO[0][7:6][23:16][39:32][48]
3.3V Resume	GPIO[15:8][31:24]



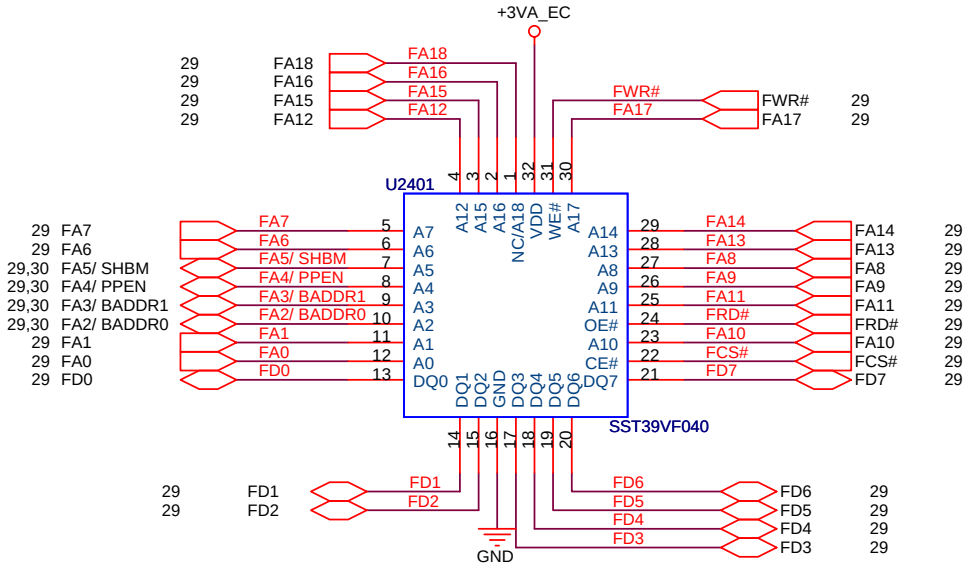








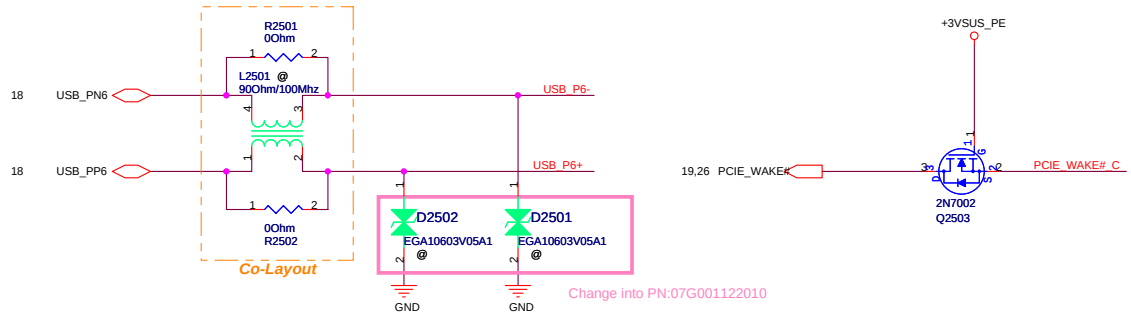
ISA ROM

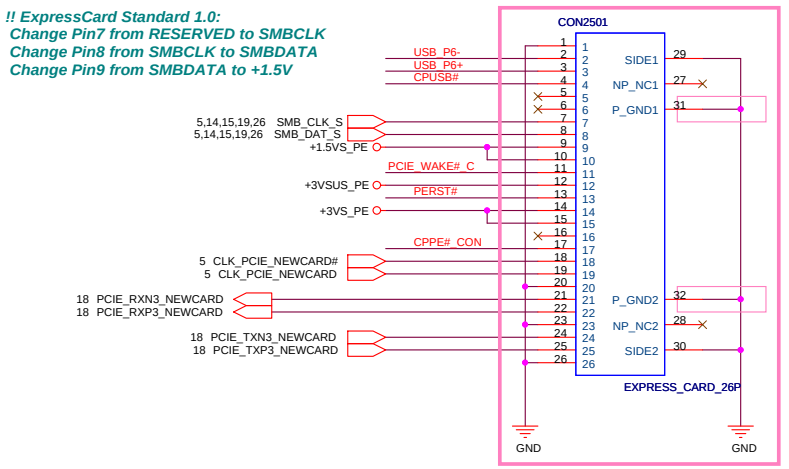


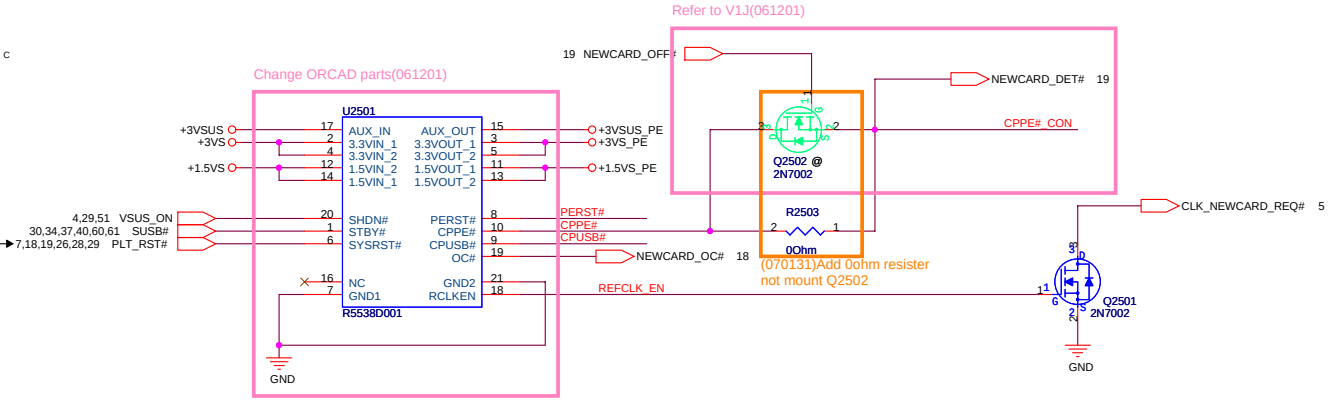
NewCard Header

(061227)Change
Schematic Part=>EXPRESS_CARD_26P_6HOLD_SA
PCB Footprint=>nb_exp_card_26p_6hd_sa_lf2
PN=12G161300269

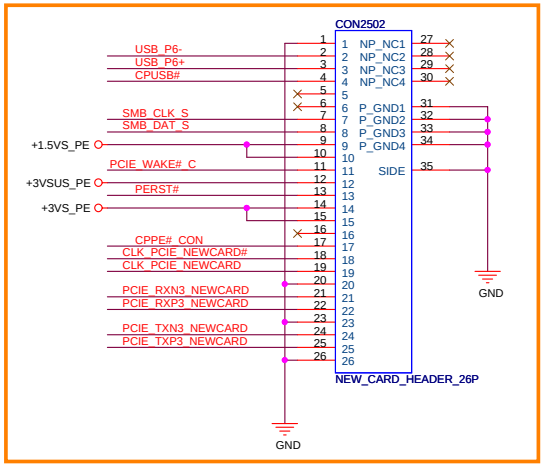
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

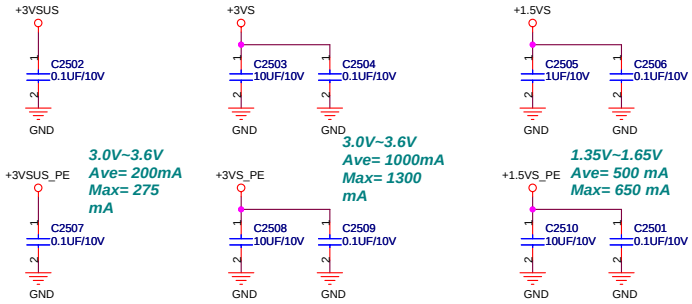




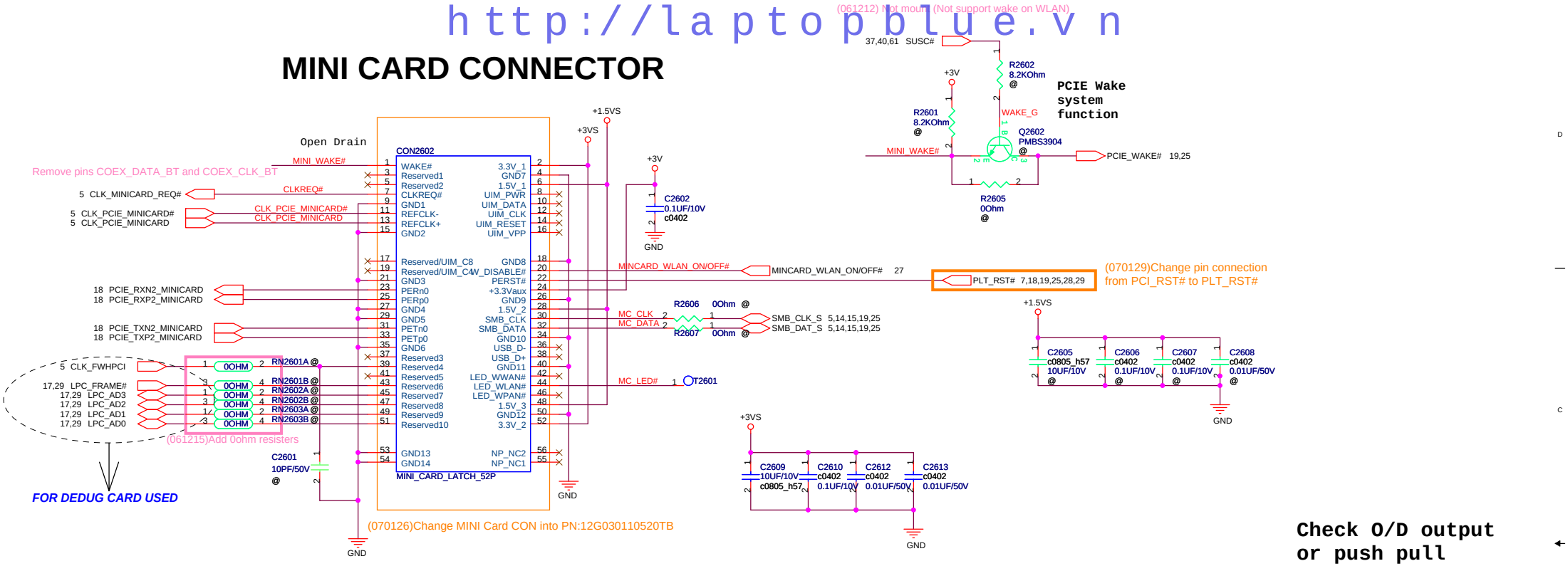


(070201)Add CON2502 in other to colayout with CON2501



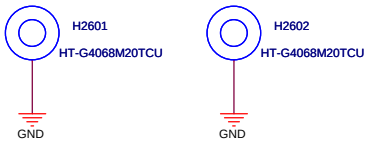


MINI CARD CONNECTOR



Check O/D output or push pull

Instead of Mini-PCIE latch connecter.For cost down.



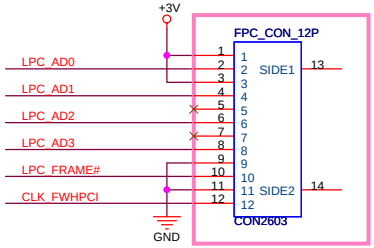
(070201)Change MINI Card NUT into PN:13G021056061TB

WLAN SPEC:

		WLL3140	WLL4080
Transmit Mode Current	11.a		550mA
	11.b	525mA	560mA
	11.g	560mA	550mA
	11.n		
Receive Mode Current	11.a		280mA
	11.b	430mA	270mA
	11.g	460mA	280mA
	11.n		
Sleep Mode Current		220mA	20mA
Supplied Voltage(VCC)	MIN	3.0V	3.0V
	TYP	3.3V	3.3V
	MAX	3.6V	3.6V

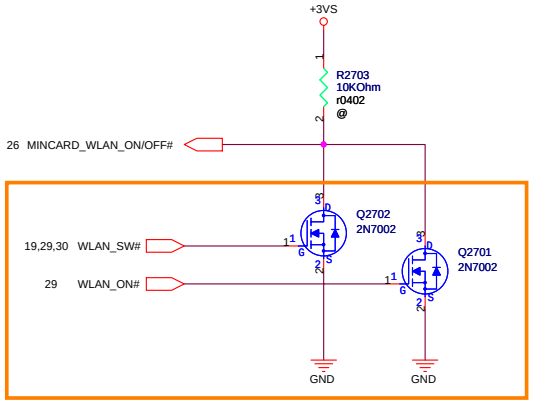
Debug Card CON

(061206)Change Debug CON into PN:12G18340120E



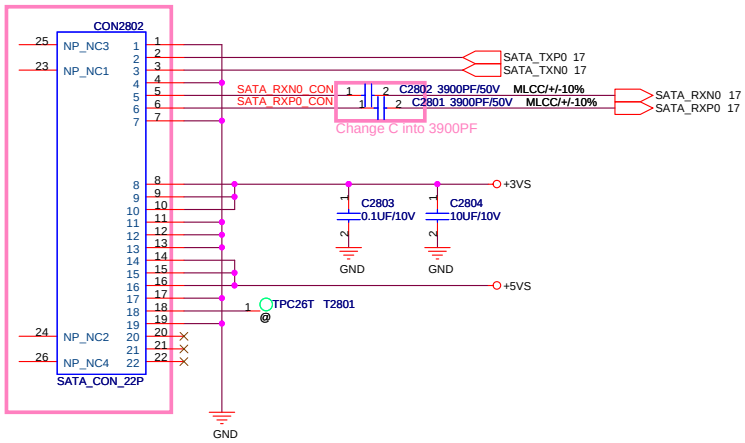
For Side SW

WLAN ON/OFF Control

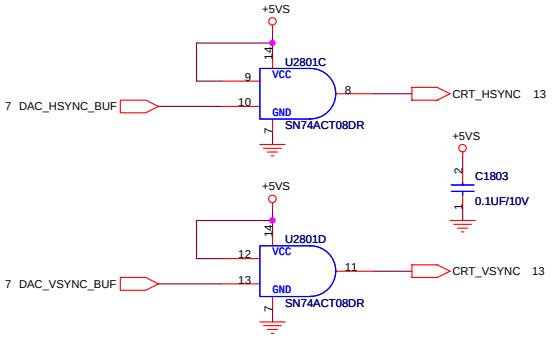


(070202)Modify WLAN on/off circuit

(061208)Change SATA CON into PN:12G15101022A

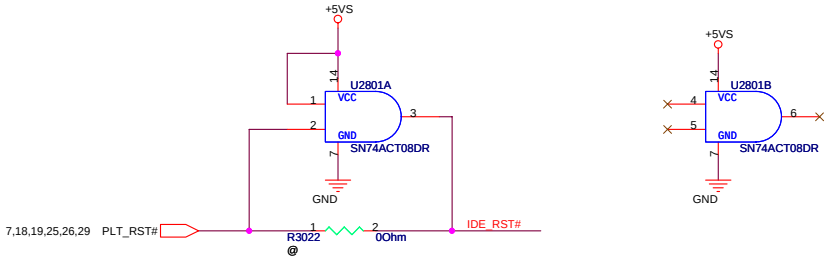


Change AND gate into 5V Vcc

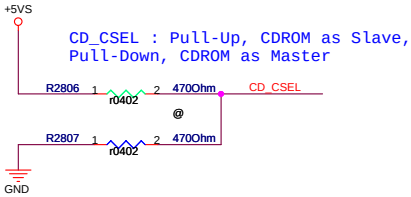


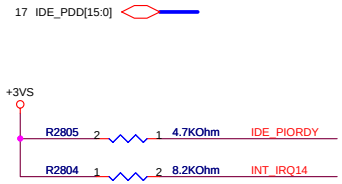
SATA HDD

Modify



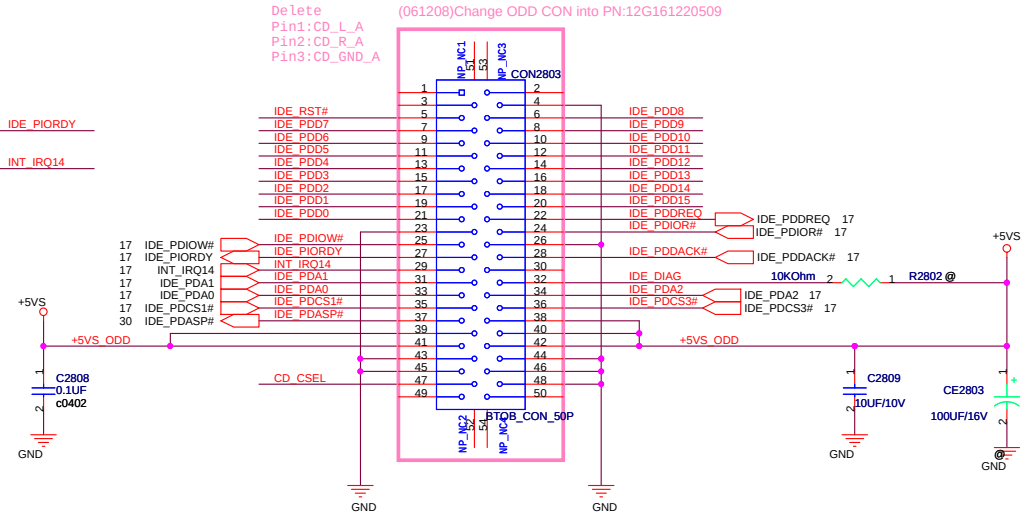
CD-ROM



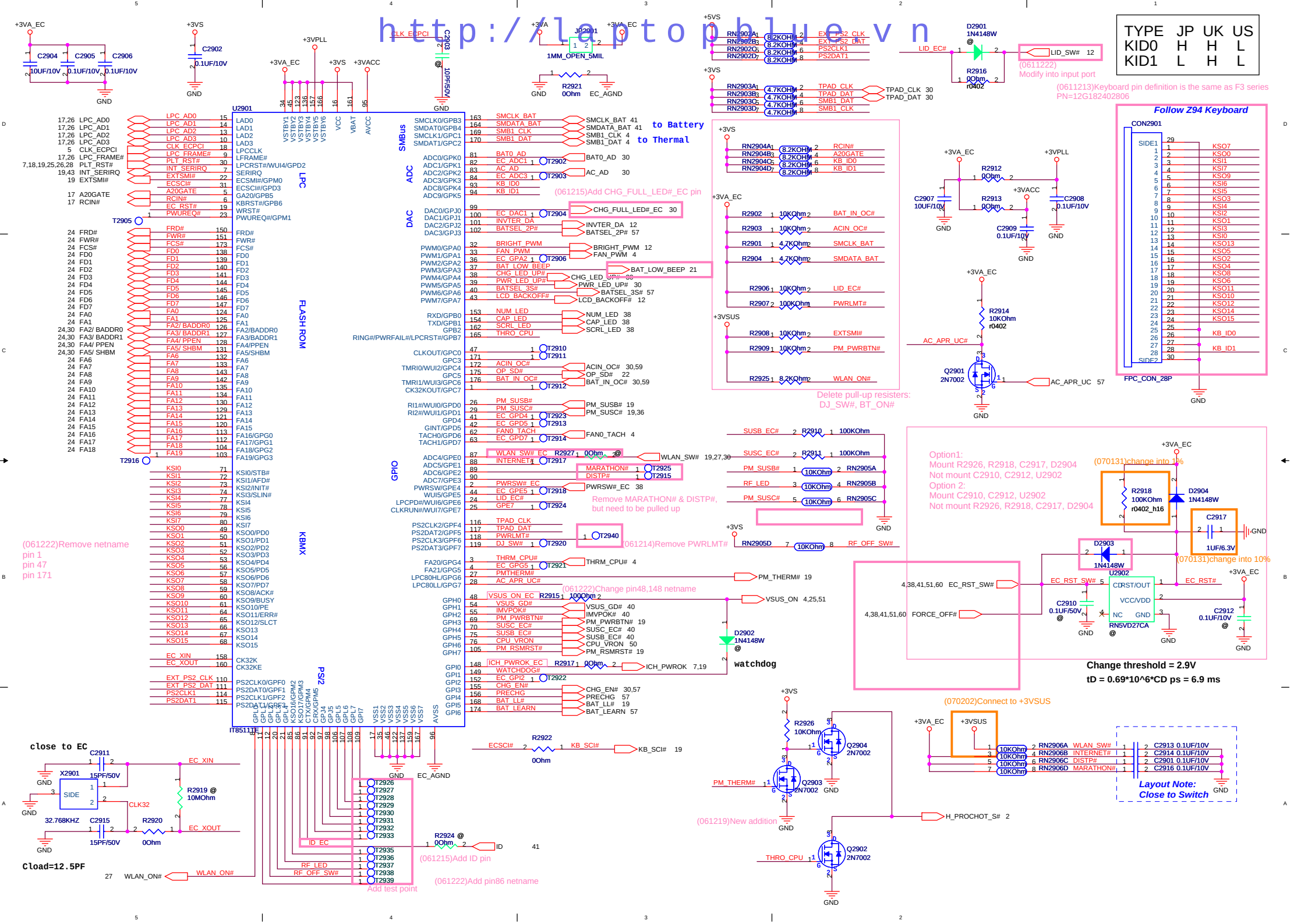


Delete
Pin1:CD_L_A
Pin2:CD_R_A
Pin3:CD_GND_A

(061208)Change ODD CON into PN:12G161220509

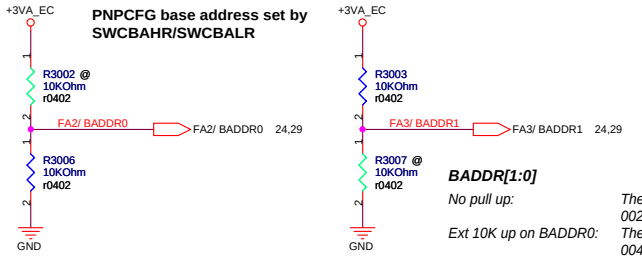


TYPE	JP	UK	US
KID0	H	H	L
KID1	L	H	L



EC Hardware Strap

Strap value sampled after VSTBY power up reset

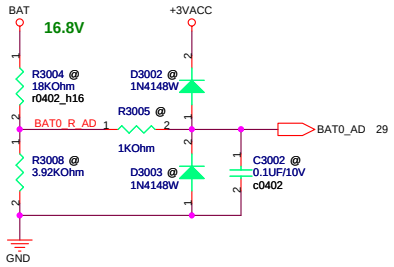


BADDR[1:0]

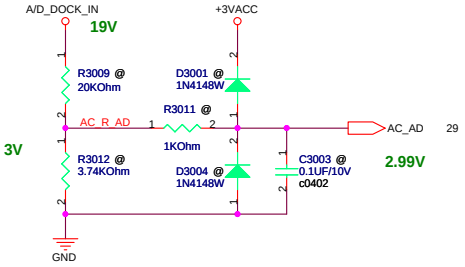
No pull up:	*The register pair to access PNPCFG is 002Eh and 002Fh.*
Ext 10K up on BADDR0:	*The register pair to access PNPCFG is 004Eh and 004Fh.*
Ext 10K up on BADDR1:	*The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.*

EC ADC

Battery

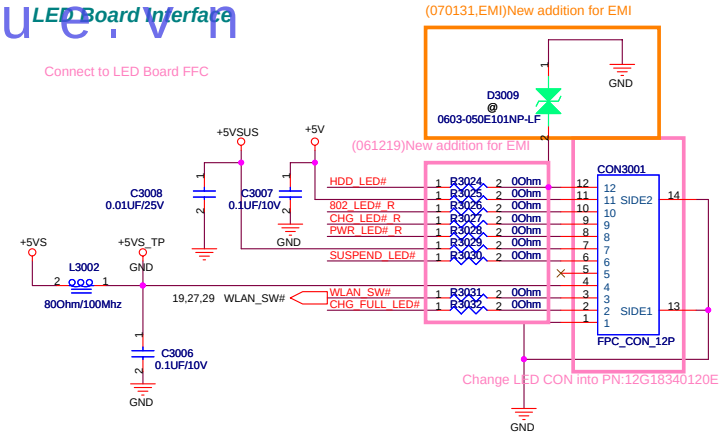


Adaptor

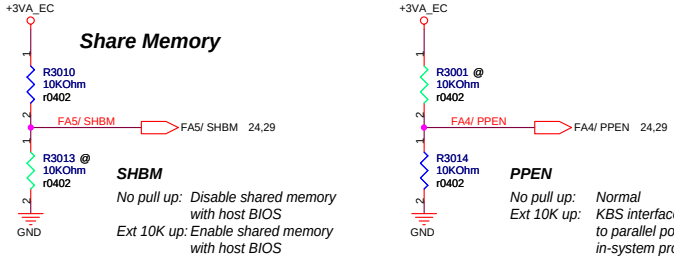


LED Board Interface

Connect to LED Board FFC



Share Memory



SHBM

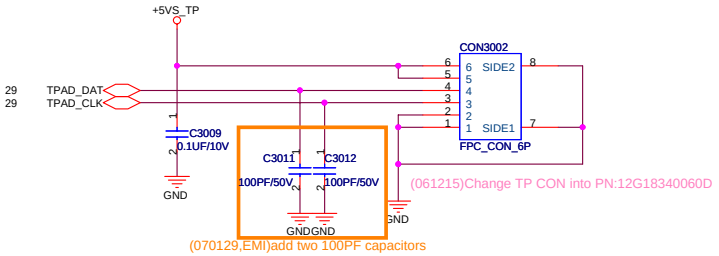
No pull up:	*Disable shared memory with host BIOS*
Ext 10K up:	*Enable shared memory with host BIOS*

PPEN

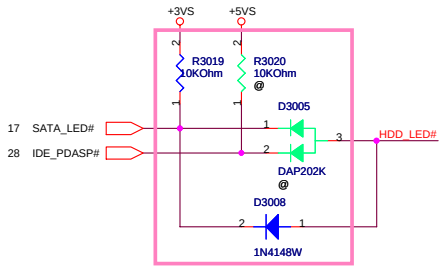
No pull up:	*Normal*
Ext 10K up:	*KBS interface pins are switched to parallel port interface for in-system programming.*

Touchpad Board Interface

Connect to Touchpad Board FFC



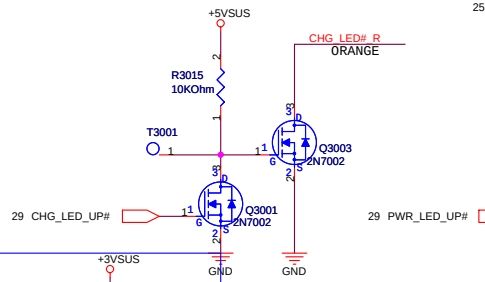
HDD LED



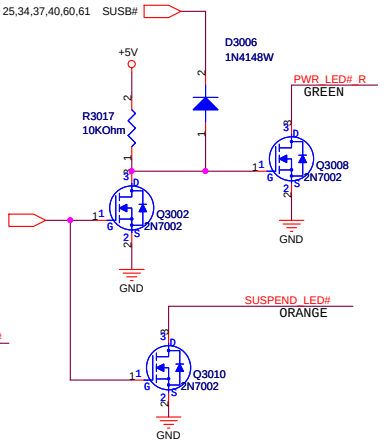
(061212)Modify HDD LED circuit

(061201)Modify Charge & Power circuit

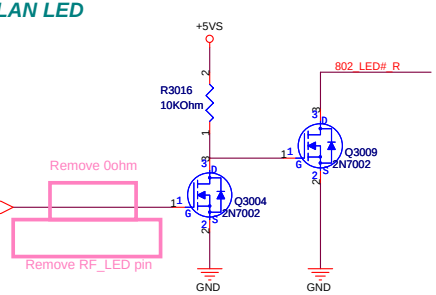
CHARGE LED



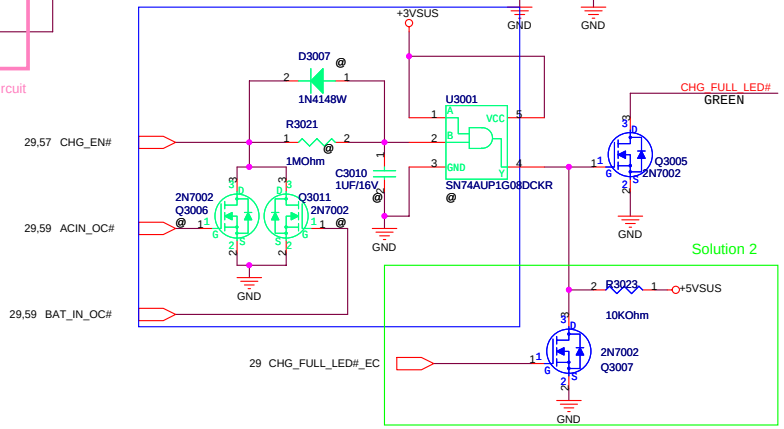
POWER LED



WLAN LED



Solution 1



(061212)Modify charge full circuit : solution1 & solution2

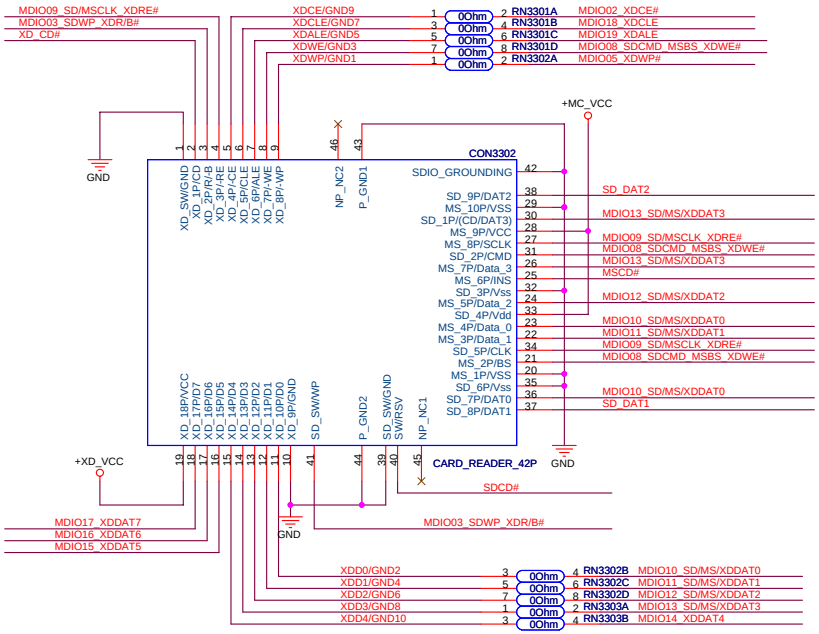
MEDIA CARD SLOT

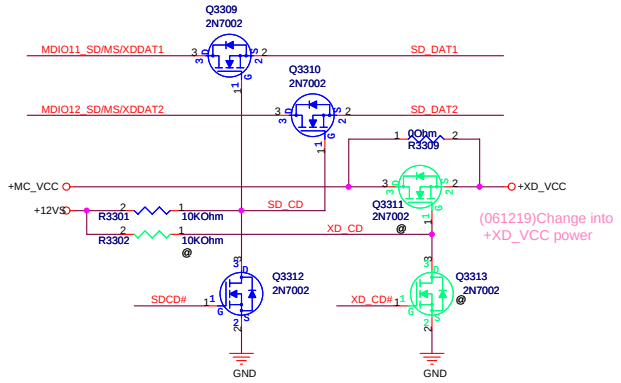
(070124)Add Media Card CON for colayout

(070130)Add RN3301, RN3302, RN3303

Solve MS Duo adaptor short problem / XD short problem

Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU

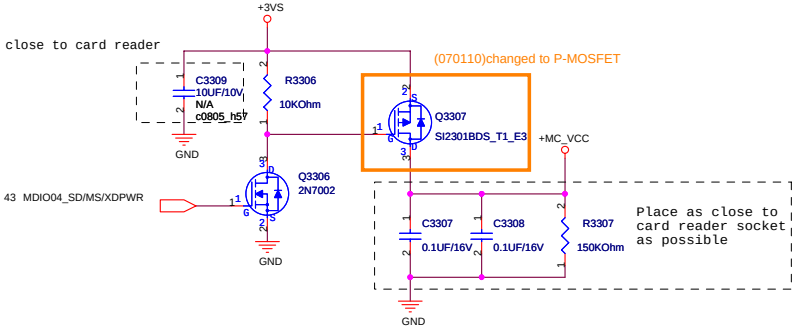




(061219)Change into +XD_VCC power

Change circuit from AAT4610A to SI2301

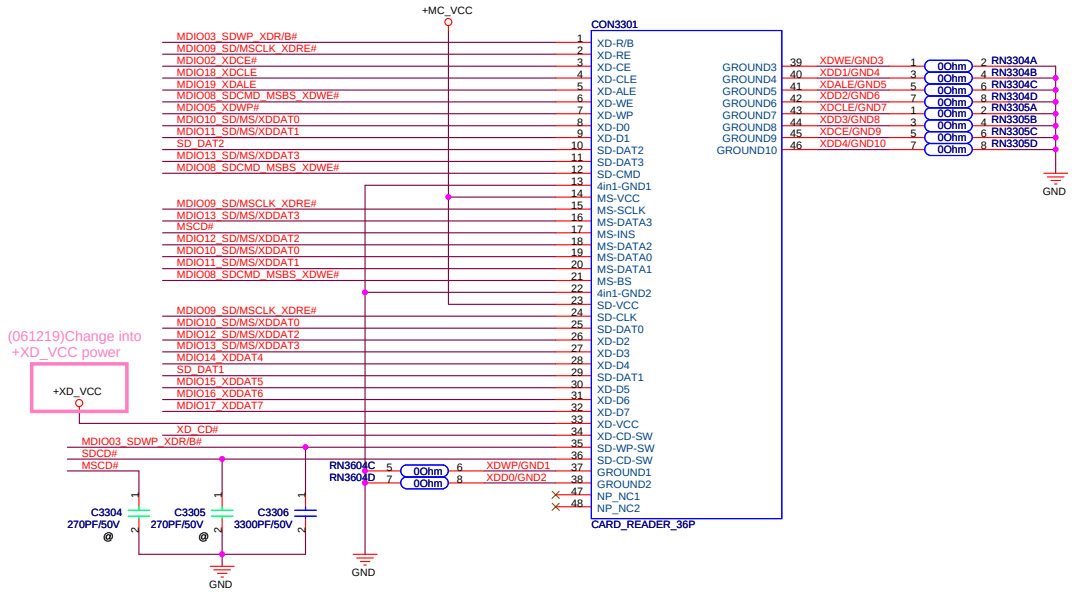
Card Detect Table		
	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low



MEDIA CARD SLOT

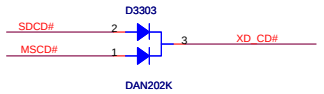
(061208)Change CON3301 into PN:12G340003601
(061225)Change schematic part & PCB Footprint

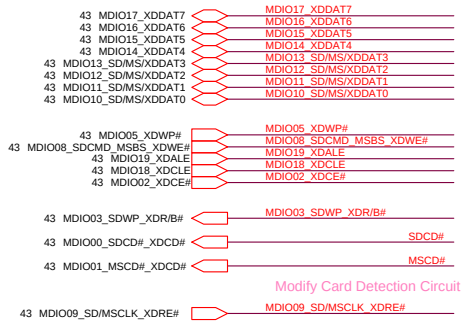
(070130)Add RN3303, RN3304, RN3305



(061219)Change into +XD_VCC power

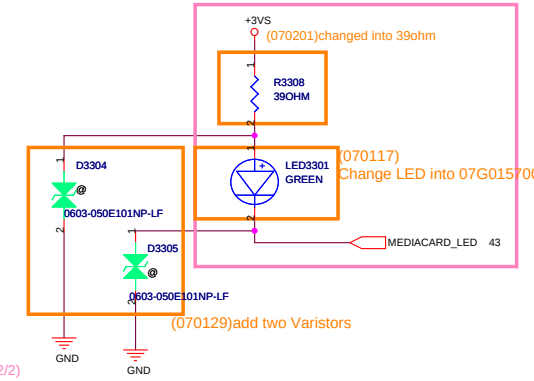
Modify Card Detection Circuit (1/2)





Modify Card Detection Circuit (2/2)

(161219)Change reference into R3308&LED3301



Support Wake On LAN
=>Adapter In mode: S3, S4 and S5
Battery mode: S3

(061207,REALTEK)Connect 0ohm to GND

R3412 0Ohm @

PCI_AD[0..31] 18,43

18,43 PCI_C/BE#0 — PCI_C/BE#0

+3VSUS, DVDD

PCI_C/BE#1 18,43
PCI_PAR 18,43
PCI_SERR# 18,19,43
PCI_PERR# 18,19,43
PCI_STOP# 18,19,43
PCI_DEVSEL# 18,19,43
PCI_TRDY# 18,19,43

CLKRUN — R3402 @ 0Ohm r0402 — PM_CLKRUN# 19,43

U3401

PCI_AD1
PCI_AD0
EECS
EEDO
EEDI/AUX
EESK
XTAL1
XTAL2

PCI_IRDY# — PCI_IRDY# 18,19,43
PCI_FRAME# — PCI_FRAME# 18,19,43
PCI_C/BE#2 18,43
PCI_AD16
PCI_AD17
PCI_AD18
+3VSUS
PCI_AD19
DVDD
PCI_AD20
PCI_AD21
PCI_AD22
PCI_AD23
LAN_IDSEL — R3407 33Ohm — PCI_AD23
PCI_C/BE#3 — PCI_C/BE#3 18,43
PCI_AD24
PCI_AD25
PCI_AD26
PCI_AD27

RTL8100CL

R3408 need close to LAN chip
R3408 5.6KOhm 1% — LAN_RSET

AVDDL
L_TDP
L_TDN
L_RDP
L_RDN
CTRL25
C3405 0.1UF/10V c0402

PCI_AD28
PCI_AD29
PCI_AD30
PCI_AD31

18,19 PCI_INTA# — PCI_INTA#
12,18,43 PCI_RST# — PCI_RST#
5 CLK_LAN_PCI — CLK_LAN_PCI

PCI_PME# — PCI_PME# 18,19,43
PCI_REQ#2 — PCI_REQ#2 18,19
PCI_GNT#2 — PCI_GNT#2 18

C3408 @ 10PF/50V c0402

R3410 1KOhm 1% — +5VS
R3409 0Ohm @
R3411 15KOhm 1%

25,30,37,40,60,61 SUSB# — SUSB#

(061207,REALTEK)Add voltage divider

Layout Note:
L_TDP, L_TDN termination resistors should be near chip

C3402 0.01UF/25V c0402
LAN_T_T — R3403 49.9Ohm 1% r0402 — L_TDP — L_TDP 35
R3404 49.9Ohm 1% r0402 — L_TDN — L_TDN 35
C3403 0.01UF/25V c0402
LAN_T_R — R3405 49.9Ohm 1% r0402 — L_RDP — L_RDP 35
R3401 49.9Ohm 1% r0402 — L_RDN — L_RDN 35

Layout Note:
L_RDP, L_RDN termination resistors should be near transformer

R3406 3.6KOhm r0402_h15

U3402 AT93C46
EECS
EESK
EEDI/AUX
EEDO

C3404 0.1UF/10V c0402

(061207)Change to PN:07G010Q12500

X3401 25Mhz
C3406 30PF/50V
C3407 30PF/50V

(070131)change into 30PF

Q3401 MW772M3L 07G003231011
CTRL25
Change trace wide into 30mil
30 mil
C3417 10UF/10V c0805_h57
C3418 c0402 0.1UF/10V
C3419 c0402 0.1UF/10V
C3420 c0402 0.1UF/10V
C3421 c0402 0.1UF/10V

(061207,REALTEK)Recommend change to 22UF

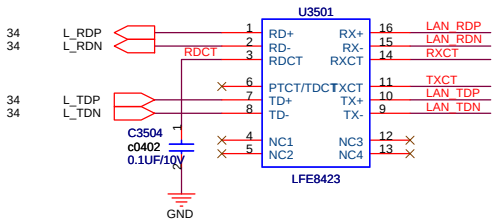
L3401 120Ohm/100Mhz
20 mil
C3414 c0402 0.1UF/10V
C3415 c0402 0.1UF/10V
C3416 c0402 0.1UF/10V

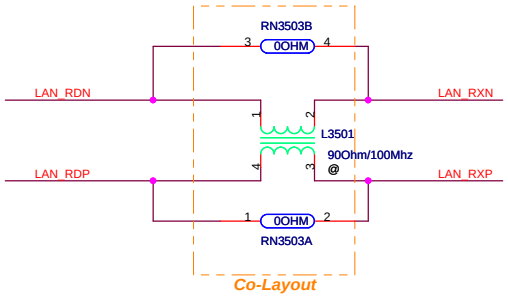
30 mil
30 mil
C3409 c0402 0.1UF/10V
C3410 10UF/10V c0805_h57
C3401 c0402 0.1UF/10V
C3411 c0402 0.1UF/10V
C3412 c0402 0.1UF/10V
C3413 c0402 0.1UF/10V

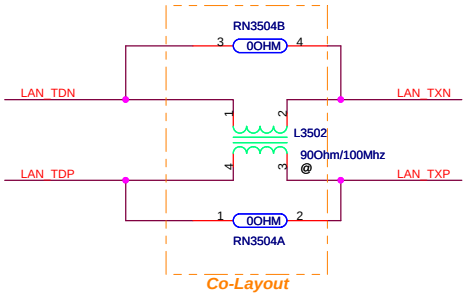
(061207,REALTEK)Remove capacitors

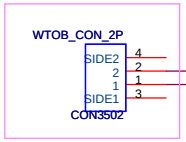
LAN PORT

TRANSFORMER 10/100MB



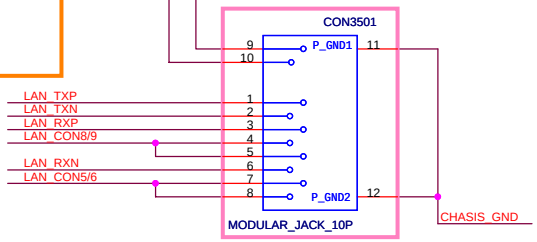




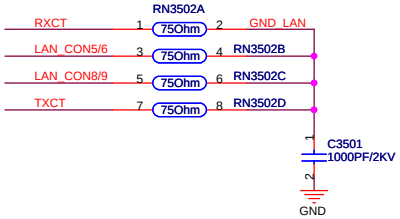


(061214)Change CON3502 into PN:12G17000002B

RJ11&RJ45



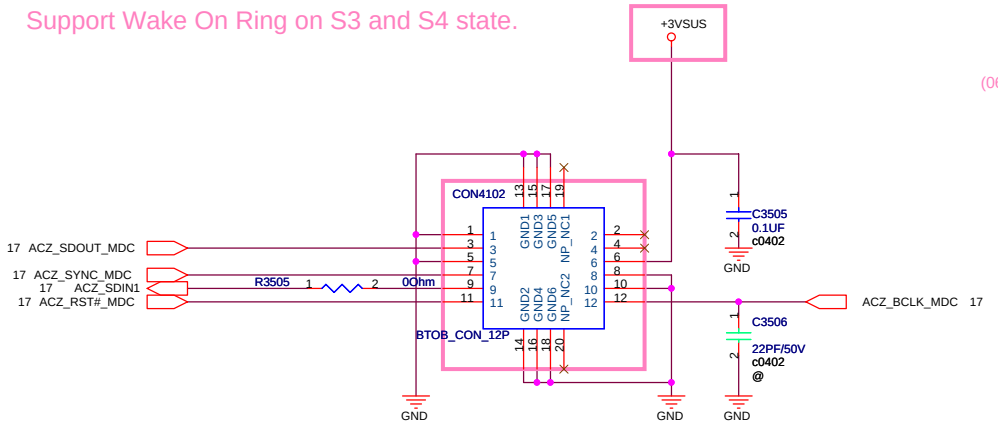
(061214)Change RJ11&RJ45 into PN:12G142011109



MDC CONNECTOR

Support Wake On Ring on S3 and S4 state.

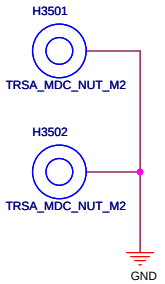
Change power from +3V to +3VSUS

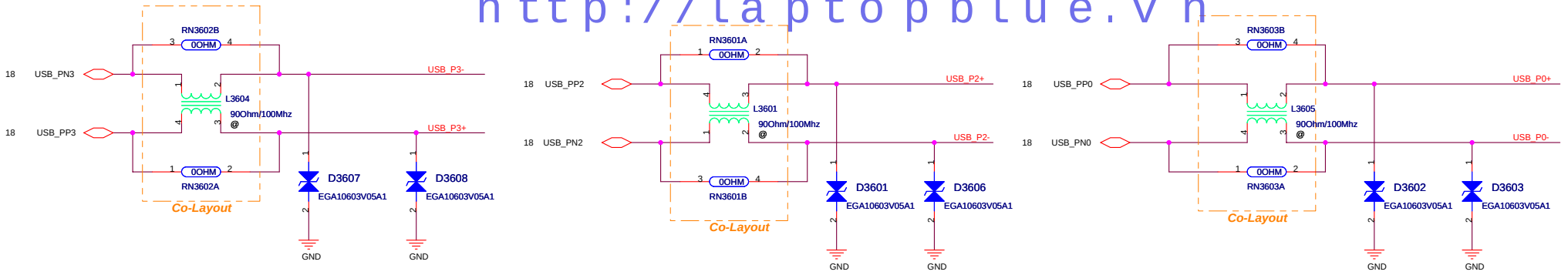


(061214)Change MDC CON into PN:12G16020012D

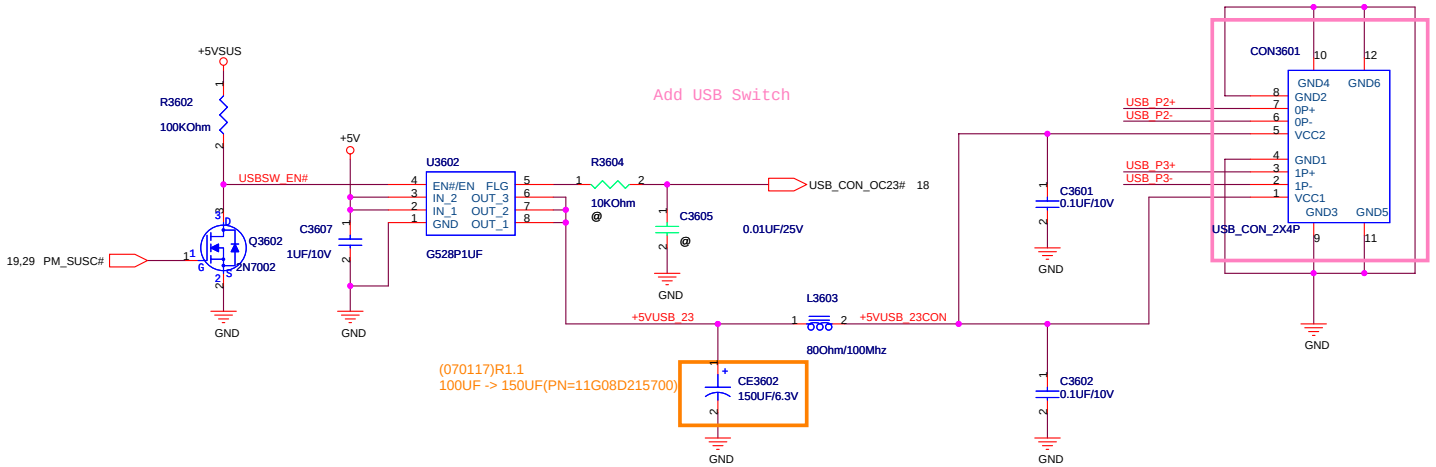
B:MDC NUT

(061219)Change MDC NUT into PN:13G021054000

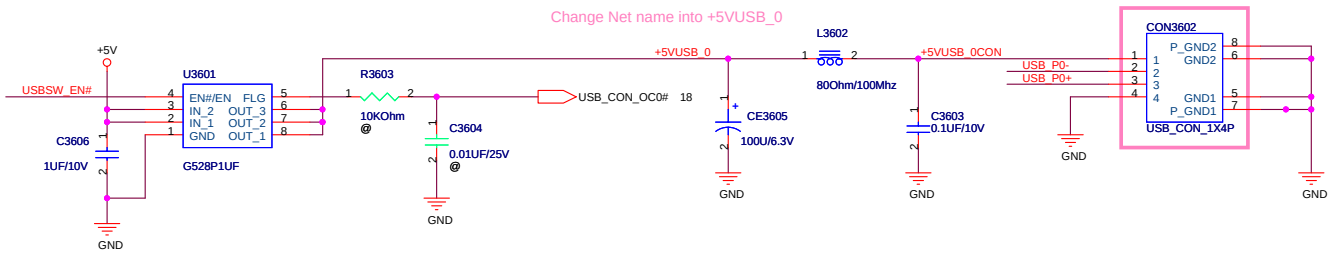


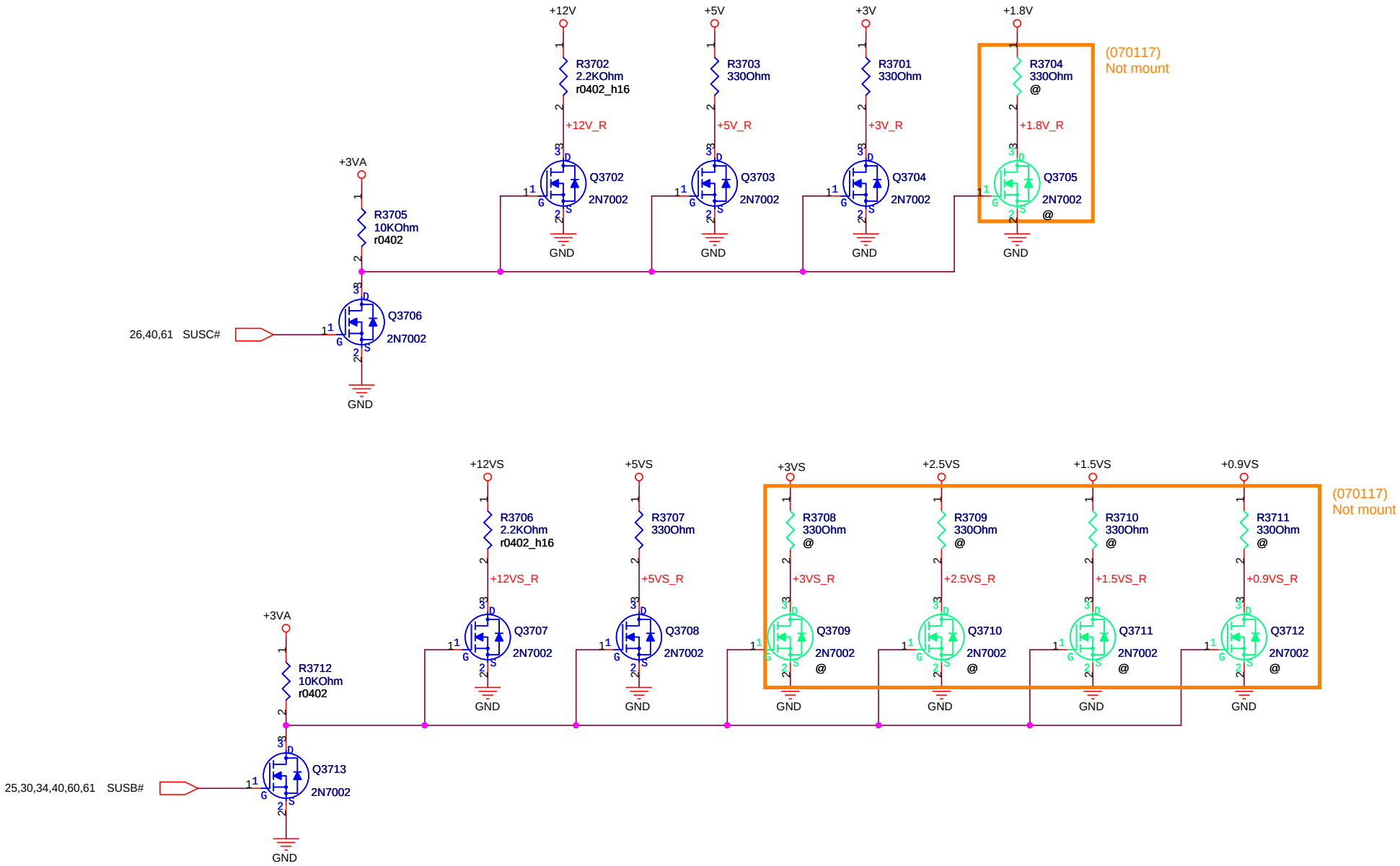


(061211)Change USB CON into PN:12G13111108F

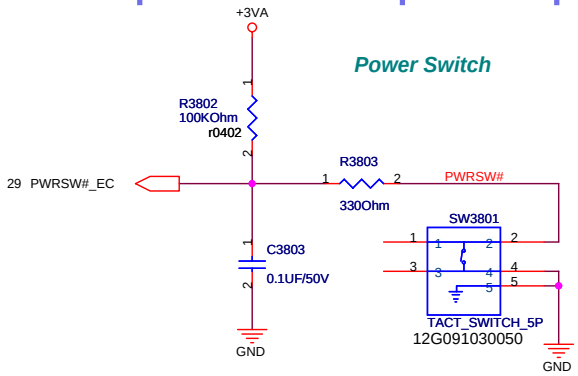


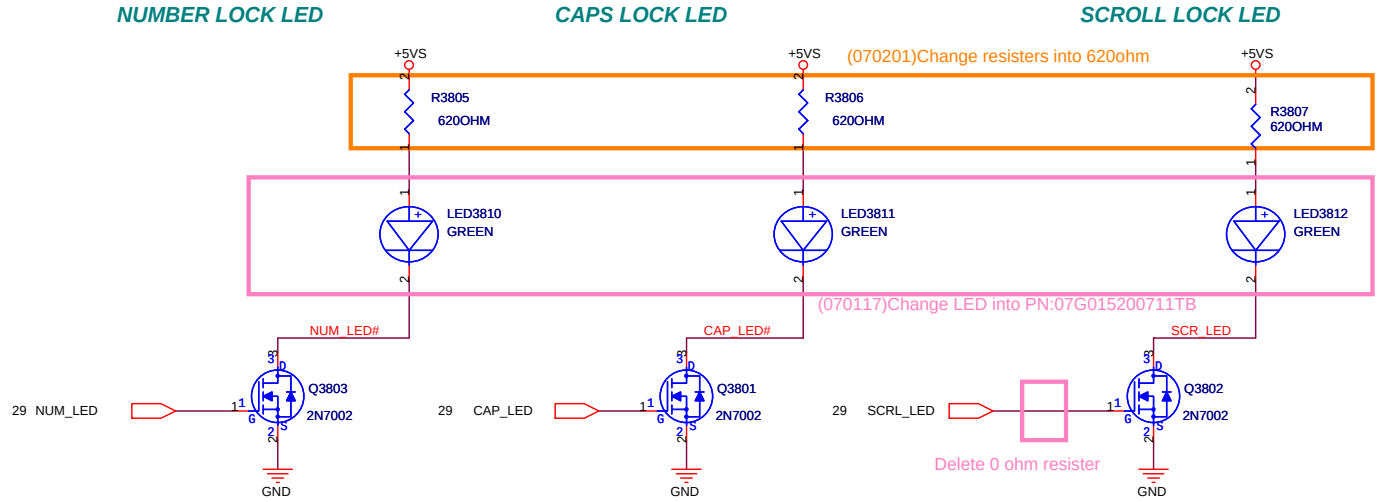
(061206)Change USB CON into PN:12G131030043

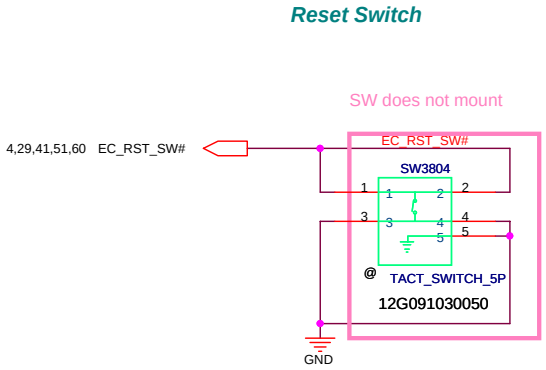


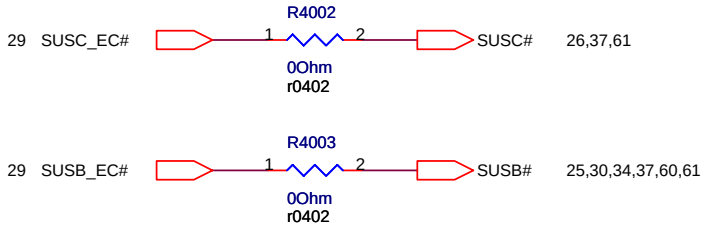


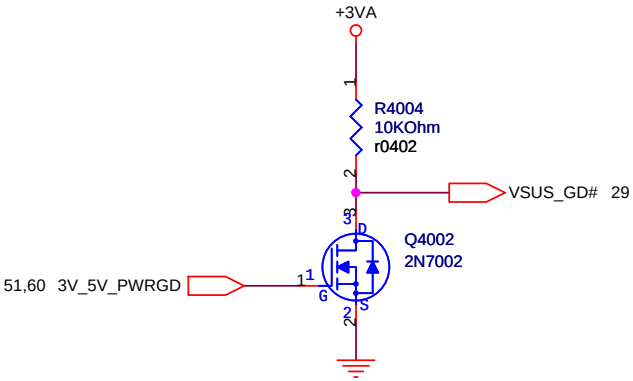
Main Board SW & LED

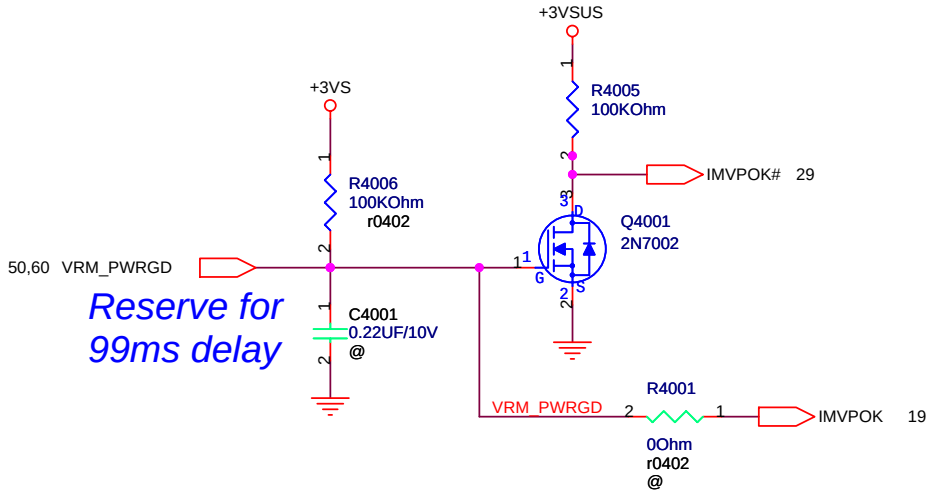




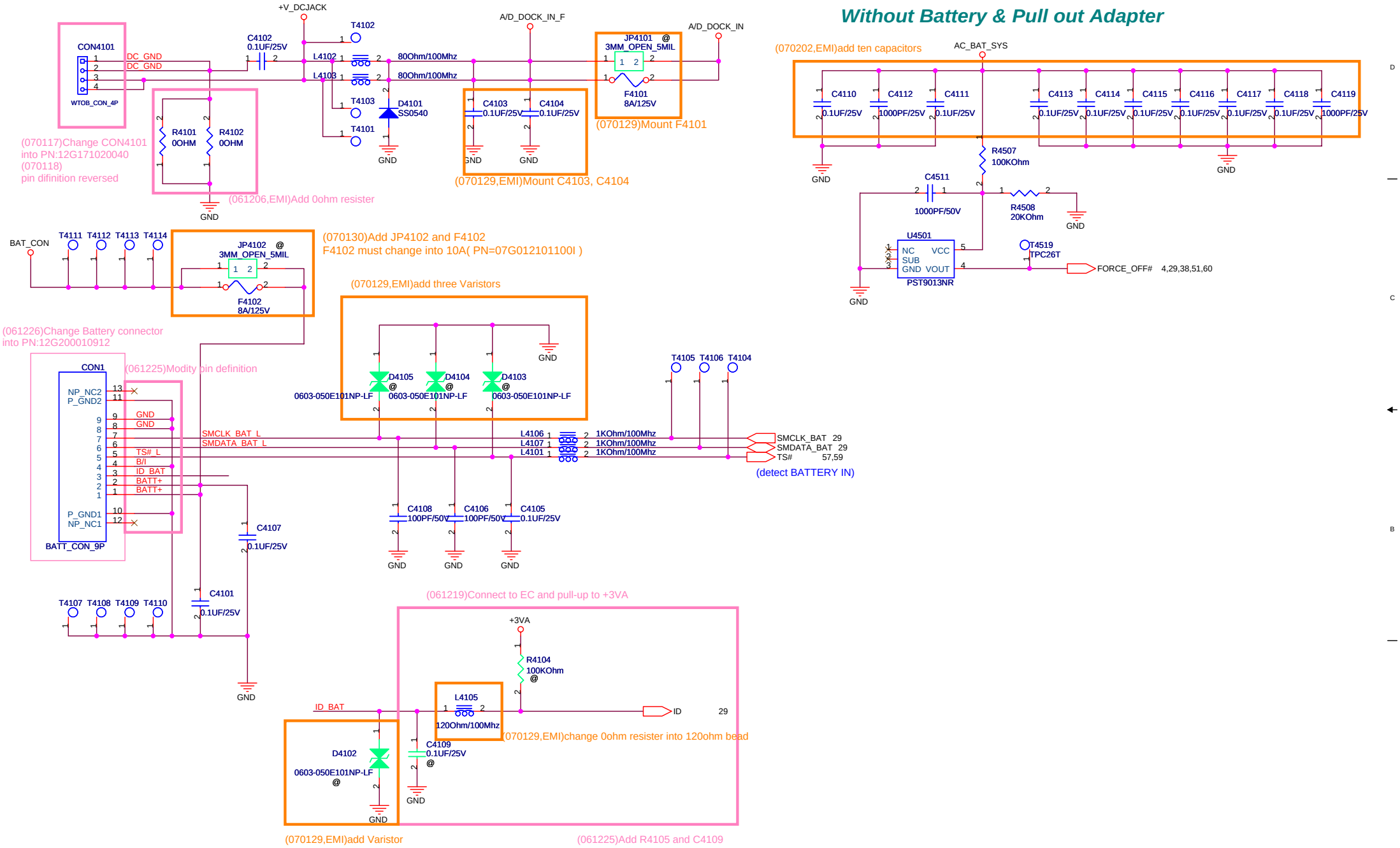


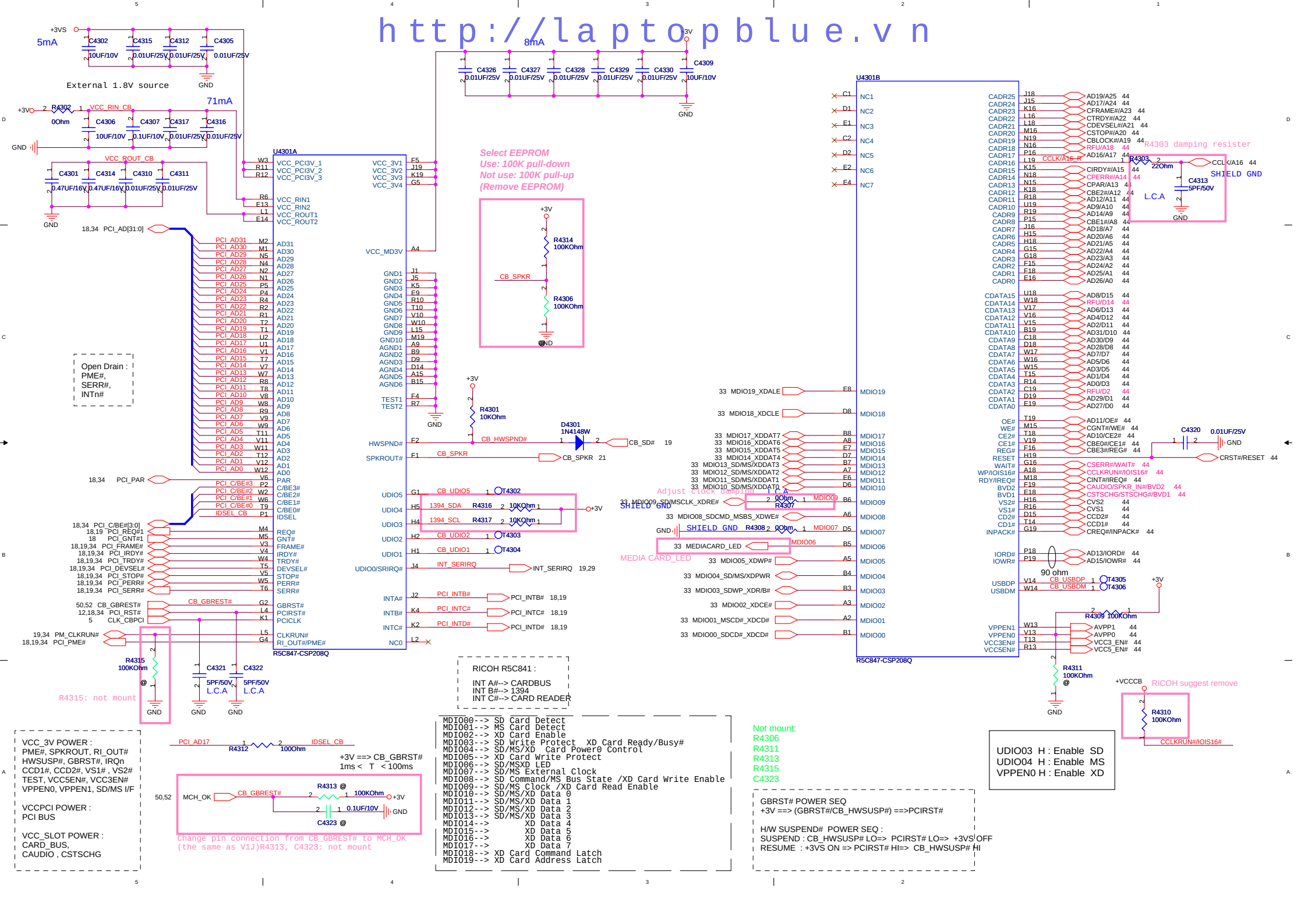




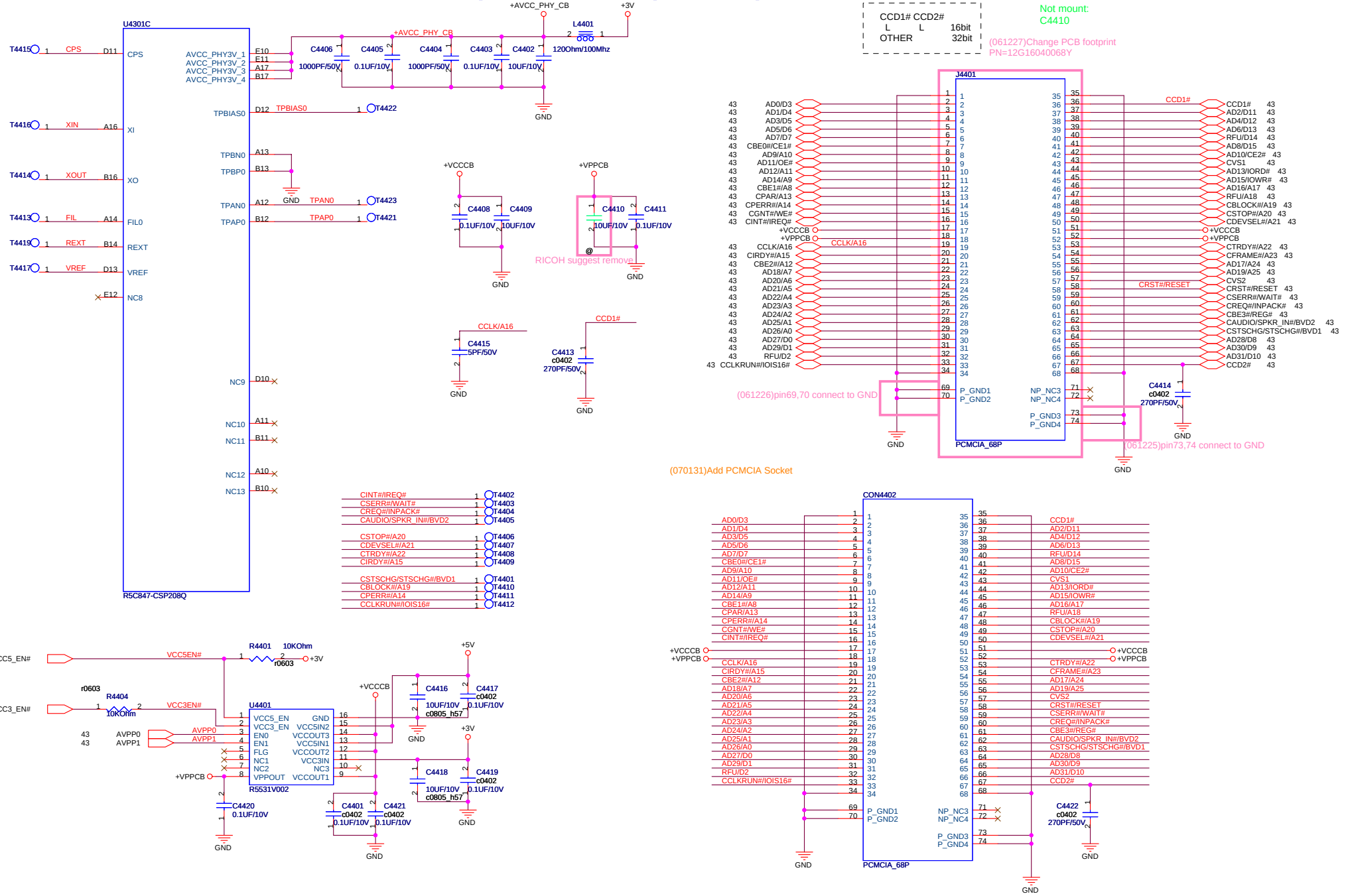


DC Power Jack

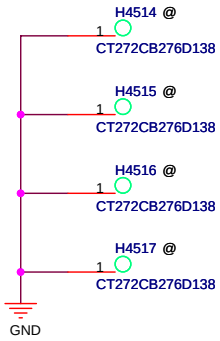




PCMCIA SOCKET



A:CPU BKT
PN:s01756



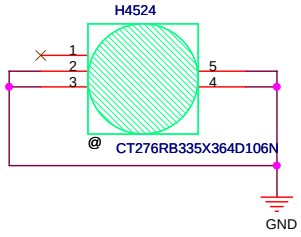
B:MDC NUT

MDC NUT put on page35
(H3501, H3502)

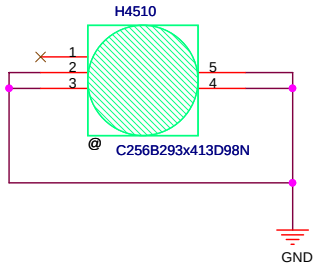
F:MINI CARD NUT

MINI CARD NUT put on
page26(H2601, H2602)

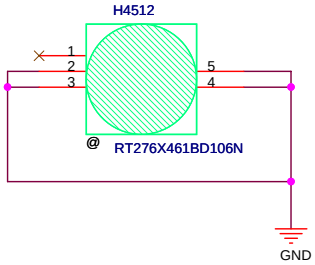
C:TOP TO BTM
PN:S01912



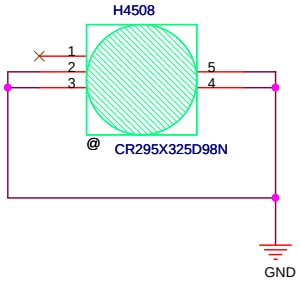
D:FIX MB
PN:s01769



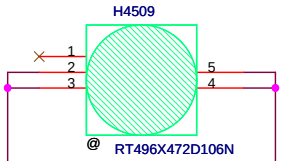
E:TOP TO BTM
PN:S01911



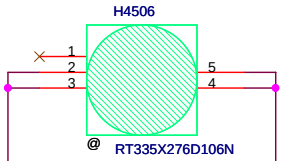
G:FIX MB
PN:s01783



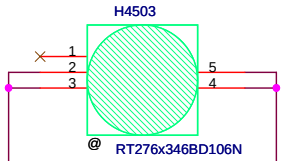
H:SYS BOSS
PN:S01914



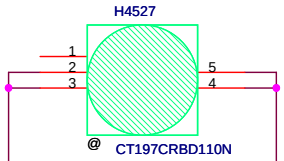
I:MB TO IO BKT
PN:S01913



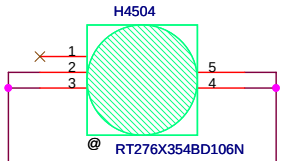
J:SYS BOSS
PN:S01915



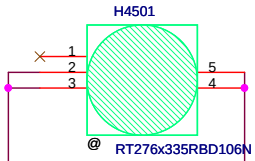
K:MB TO IO BKT
PN:S01705



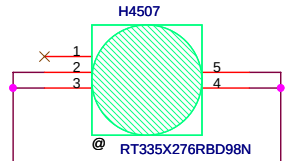
L:TOP TO BTM
PN:S01916



M:SYS BOSS
PN:s01917

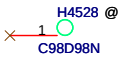


N:TOP TO BTM
PN:S01851

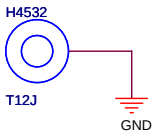


GND

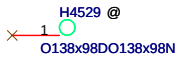
O:ALIGNMENT HOLE
PN:temp_5262_gh15



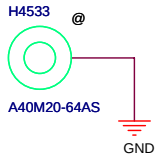
T:NB SINK NUT
PN:13GNJ510M170-1



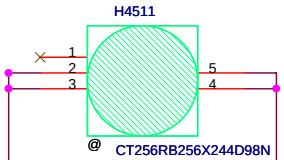
P:ALIGNMENT HOLE
PN:s01724



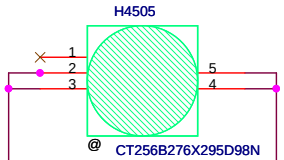
EMI NUT
for LVDS cable
PN:13G021029050



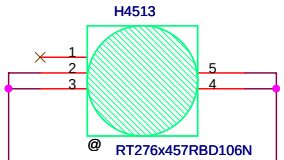
U:TOP TO BTM
PN:S01854



V:TOP TO BTM
PN:S01857

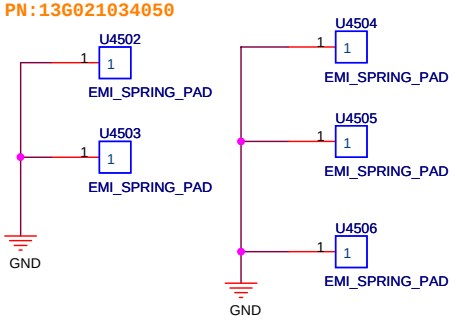


W:TOP TO BTM
PN:S01918



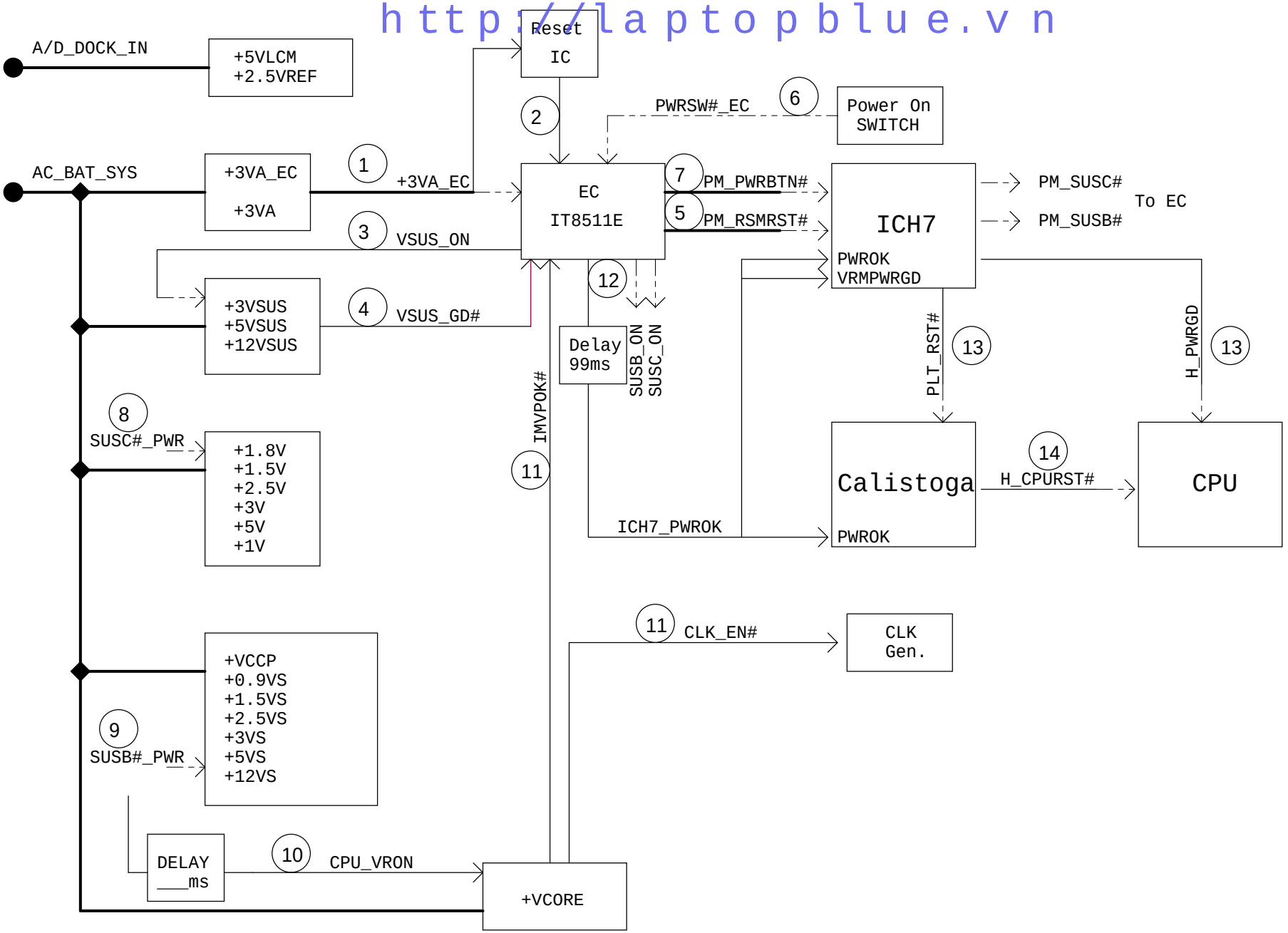
GND

EMI SPRING
PN:13G021034050



R1.0 to R1.1

Page	Action
3	Change C304, C305, C306, C307, C308, C310, C312, C313 into 10UF for cost down.
4	Add R418 and Q404 to avoid error action.
7	Add R715 and R716 in other to improve signal quality.
12	Mount R1206 and Q1204 in other to reduce discharge time.
13	Change C1313, C1314 into 22PF in other to improve undershoot.
13	Change the rated current of the fuse(F1302) into 1A for customer's demand.
21	Mount R2105 and R2109, or there is no dialing tone.
21	Modify R2108 into 31.6Kohm in other to tune +5V_AUDIO.
21	Add three 0ohm resisters R2127, R2128, R2129 for EMI.
22	Change R2201~R2204 into 27Kohm for speaker volume.
22	Change 0ohm resisters(R2238, R2239) into beads.
22	Remove a N-MOS and a resistor on JACK_IN side due to change a new HP JACK.
22	Add 4 Varistors(D2202~D2205) for EMI.
23	Remove a N-MOS due to change a new MIC JACK.
23	Add a 120ohm bead L2304 and a 1000PF capacitor C2307 for EMI.
25	Add 0ohm resister R2503 and change Q2502 into unmount.
25	Add CON2502 in other to colayout with CON2501.
26	Connect not PCI_RST# but PLT_RST# to the RESET# signal of PCIE MiniCard for customer's demand.
27	Connect pin20 of MiniCard to the signal of OR conditions of WLAN_SW# and WLAN_ON# for customer's demand.
29	Change tolerance of R2918 into 1% and C2917 into 10% for the timing of EC_RST#.
29	Change WLAN_SW# into pull-up +3VSUS
30	Add 100PF capacitors C3011 and C3012 for EMI.
33	Add CON3302, RN3301, RN3302, RN3303, RN3304, RN3305 in other to colayout with CON3301.
33	Add Varistors D3304 and D3305 for EMI.
33	Change R3308 into 39ohm for the brightness of LED3301.
34	Change C3406, C3407 into 30PF in other to fit 25MHz frequency.
35	Place C3502, C3503 on the other side of L3503, L3504 for layout.
36	Change CE3602 from 100UF to 150UF in other to fit droop SPEC.
37	Change R3704, Q3705, R3708, Q3709, R3709, Q3710, R3710, Q3711, R3711, Q3711 into unmount because they don't affect the discharge circuit.
38	Change resisters R3805, R3806, R3807 into 620ohm in other to tune brightness.
41	Change the fuse F4101 into mount for customer's demand.
41	Add the colayout of JP4102 and F4102 for customer's demand.
41	Change 0ohm resister R4105 into 120ohm bead L4105 for EMI.
41	Add four Varistors D4102, D4103, D4104, D4105 and ten capacitors C4110~C4119 for EMI.
41	Chane C4103, C4104 into mount for EMI.
70	Chane R7002 into 80.6ohm for brightness.



Power ON Sequence

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM	O	48	GPH0	VSUS_ON_EC	O
33	PWM1/GPA1	FAN_PWM	O	54	GPH1	VSUS_GD#	I
36	PWM2/GPA2	/	O	55	GPH2	IMVPOK#	I
37	PWM3/GPA3	BAT_LOW_BEEP(Reserved)	O	69	GPH3	PM_PWRBTN#	O
38	PWM4/GPA4	CHG_LED_UP#	O	70	GPH4	SUSC_EC#	O
39	PWM5/GPA5	PWR_LED_UP#	O	75	GPH5	SUSB_EC#	O
40	PWM6/GPA6	BATSEL_3S#	O	76	GPH6	CPU_VRON	O
43	PWM7/GPA7	LCD_BACKOFF#	O	105	GPH7	PM_RSMRST#	O
153	RXD/GPB0	NUM_LED	O	148	GPI0	ICH_PWROK_EC	O
154	TXD/GPB1	CAP_LED	O	149	GPI1	WATCHDOG#	O
162	GPB2	SCRL_LED	O	152	GPI2	/	
163	SMCLK0/GPB3	SMCLK_BAT	I/0	155	GPI3	CHG_EN#	O
164	SMDAT0GPB4	SMDATA_BAT	I/0	156	GPI4	PRECHG	O
5	GA20/GPB5	A20GATE	O	168	GPI5	BAT_LL#	O
6	KBRST#/GPB6	RCIN#	O	174	GPI6	BAT_LEARN	O
165	GPB7	THRO_CPU	O	109	GPI7	/	
47	CLKOUT/GPC0	/	O	99	DAC0/GPJ0	CHG_FULL_LED#_EC	O
169	SMCLK1/GPC1	SMB1_CLK	I/0	100	DAC1/GPJ1	/	
170	SMDAT1/GPC2	SMB1_DAT	I/0	101	DAC2/GPJ2	INVTER_DA	O
171	GPC3	/	I	102	DAC3/GPJ3	BATSEL_2P#	O
172	TMRI0/WUI2/GPC4	ACIN_OC#	I	97	GPJ4	/	
175	GPC5	OP_SD#	O	98	GPJ5	/	
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I			/	
1	CK32KOUT/GPC7	/	O			/	
26	RI1#/WUI0/GPD0	PM_SUSB#	I	81	ADC0/GPK0	BAT0_AD	I
29	RI2#/WUI1/GPD1	PM_SUSC#	I	82	ADC1/GPK1	/	
30	LPCRST#/WUI4//GPD2	PLT_RST#	I	83	ADC2/GPK2	AC_AD	I
31	ECSCI#/GPD3	ECSCI#	O	84	ADC3/GPK3	/	
41	GPD4	/		93	ADC8/GPK4	KB_ID0	I
42	GINT/GPD5	/		94	ADC9/GPK5	KB_ID0	I
62	TACH0/GPD6	FAN0_TACH	I				
63	TACH1/GPD7	/	O				
87	ADC4/GPE0	WLAN_SW#_EC(Reserved)	I	8	GPL0	/	O
88	ADC5/GPE1	/	I	11	GPL1	/	O
89	ADC6/GPE2	/	I	12	GPL2	/	I
90	ADC7/GPE3	/	I	20	GPL3	/	O
2	PWRSW/GPE4	PWRSW#_EC	I	21	GPL4	/	
44	WUI5/GPE5	/		106	GPL5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I	107	GPL6	/	
25	CLKRUN#/WUI7/GPE7	/	O	108	GPL7	/	
110	PS2CLK0/GPF0	/		22	ECSMI#/GPM0	EXTSMI#	O
111	PS2DAT0/GPF1	/		23	PWUREQ#/GPM1	/	
114	PS2CLK1/GPF2	/	I/0	85	KSO16/GPM2	/	
115	PS2DAT1/GPF3	/	I/0	86	KSO17/GPM3	ID_EC (Reserved)	I
116	PS2CLK2/GPF4	TPAD_CLK		91	CTX/GPM4	/	
117	PS2DAT2/GPF5	TPAD_DAT		92	CRX/GPM5	/	
118	PS2CLK3/GPF6	/					
119	PS2DAT3/GPF7	/	I				
113	FA16/GPG0	FA16					
112	FA17/GPG1	FA17					
104	FA18/GPG2	FA18					
103	FA19/GPG3	/					
3	FA20/GPG4	THRM_CPU#	I				
4	FA21/GPG5	/					
27	LPC80HL/GPG6	PMTHERM#	O				
28	LPC80LL/GPG7	AC_APR_UC#	I				

ICH7-M GPIO SETTING

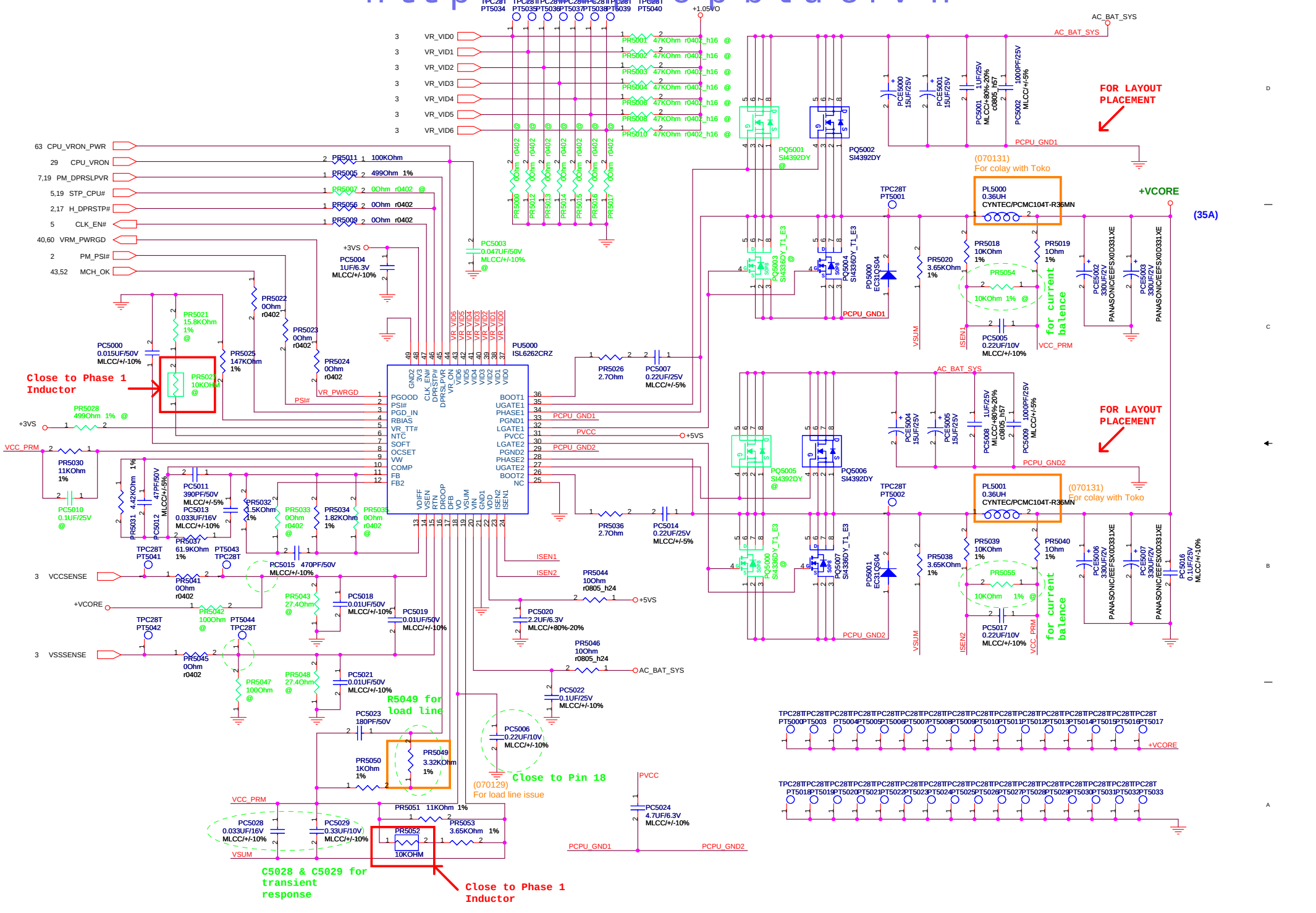
Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	/	I/O
AC18	GPIO07	PM_THERM#_GPIO (Reserved)	I
E21	GPIO08	EXTSMI#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	WLAN_SW#_ICH	I
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	NEWCARD_DET#	I
R4	GPIO14	BAT_LL#_ICH (Reserved)	I
E22	GPIO15	WLAN_LED#	O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STPPCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	/	I
AF21	GPIO20/STPCPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	/	I
A13	REQ4#/GPIO22	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	/	
R3	GPIO24	/	
D20	GPIO25	CB_SD#	O
A21	GPIO26	/	
B21	GPIO27	BTO_DEV0	I
E23	GPIO28	NEWCARD_OFF#	O
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	I/O
AC19	GPIO33/AZ_DOCK_EN#	BTO_DEV1	I
U2	GPIO34/AZ_DOCK_RST#	BTO_DEV2	I
AD21	GPIO35	/	O
AH19	GPIO36/SATA2GP	/	
AE19	GPIO37/SATA3GP	PCB_ID0	I
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

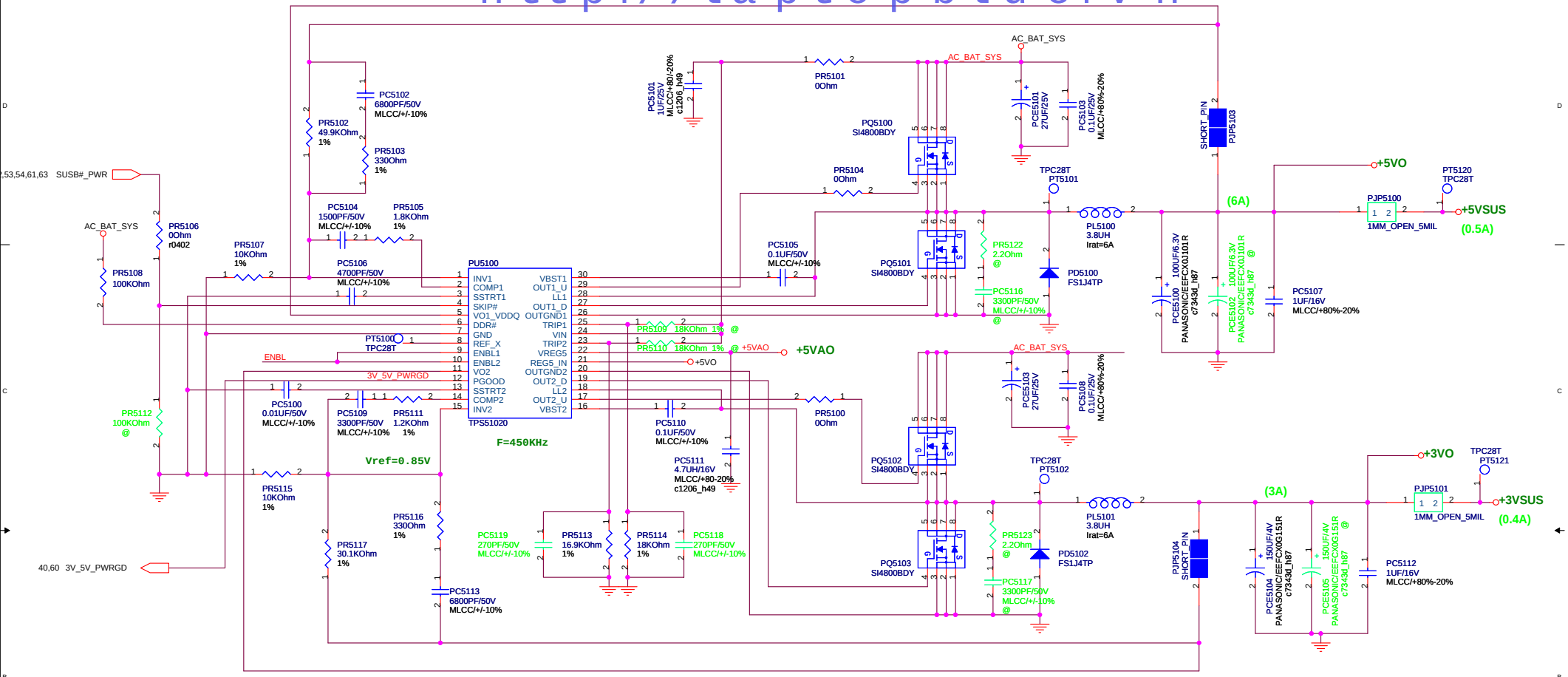
Indigo: the same as T12F
Pink: different from T12F

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

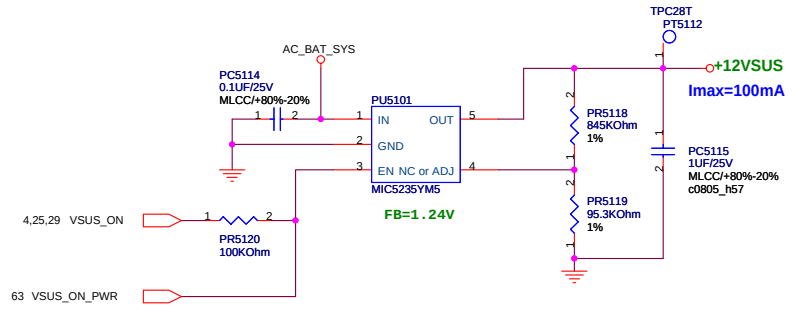
PCIE Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

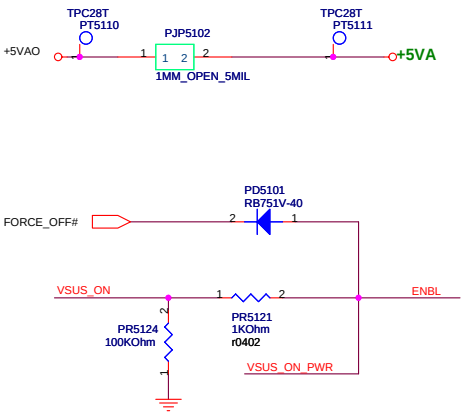
SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

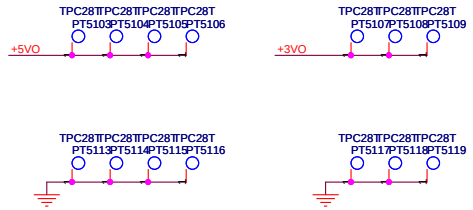


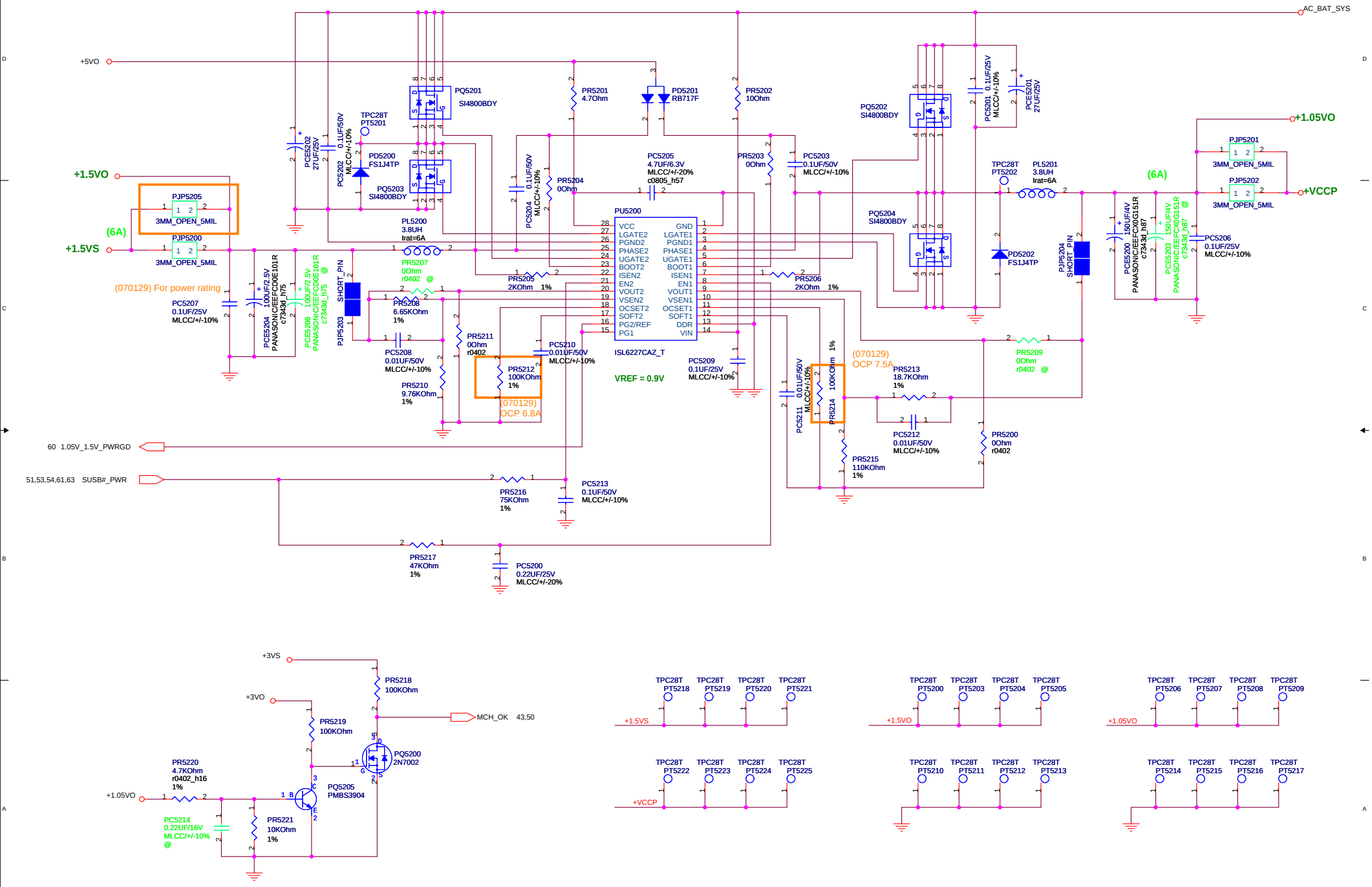


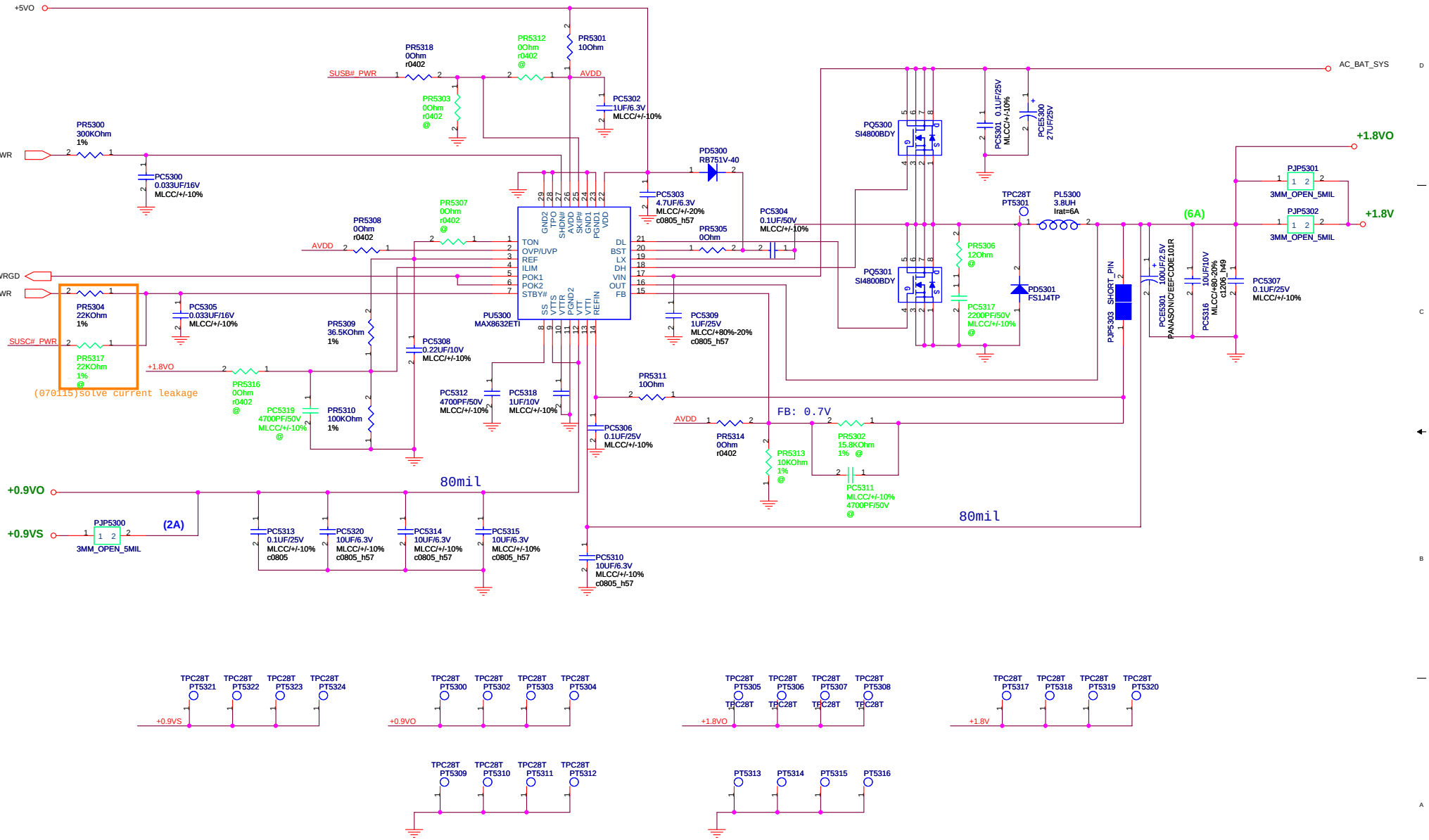
+12VSUS



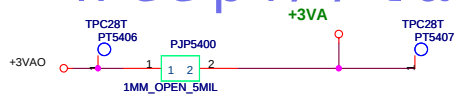


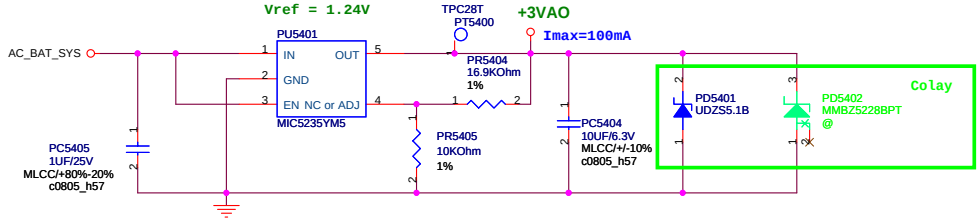




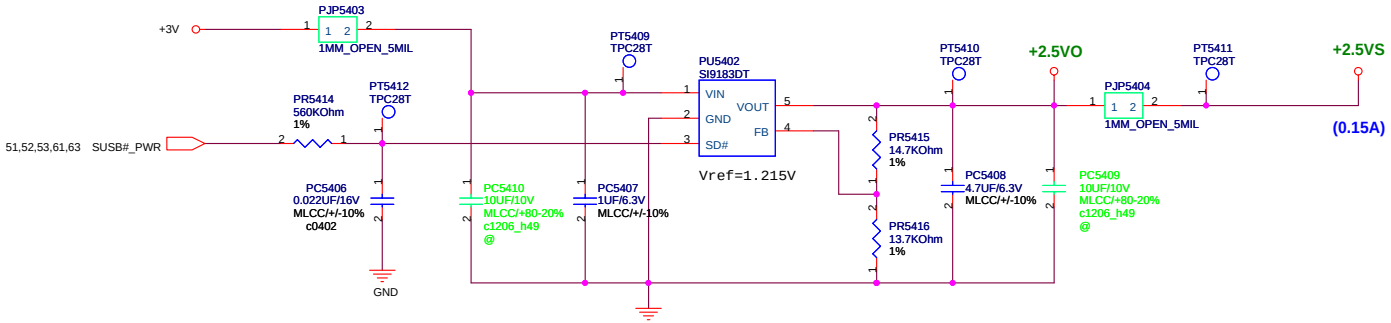


+3VAO

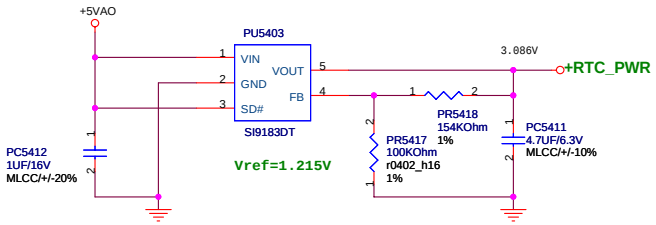




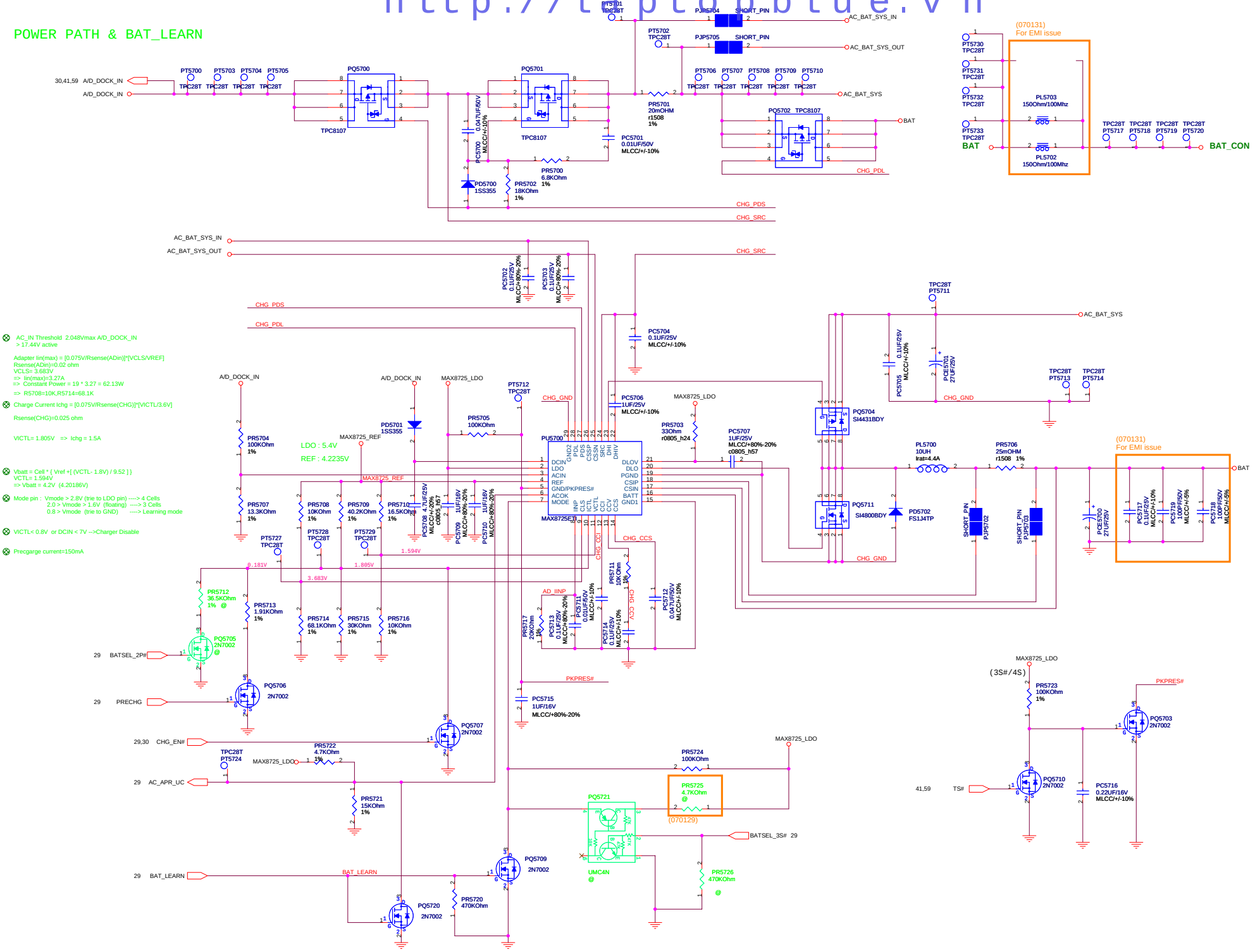
+2.5VS



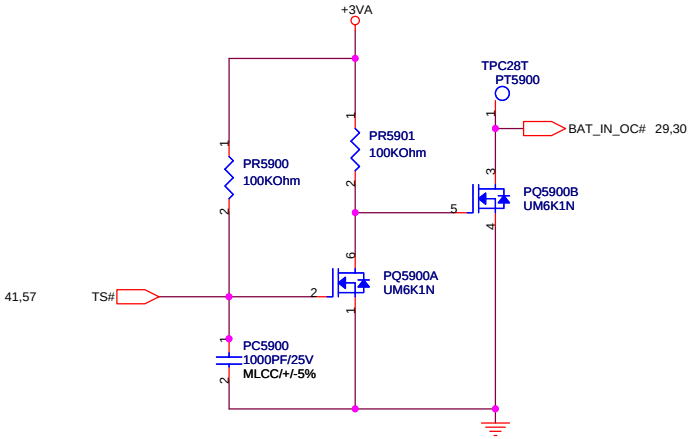
+RTC_PWR



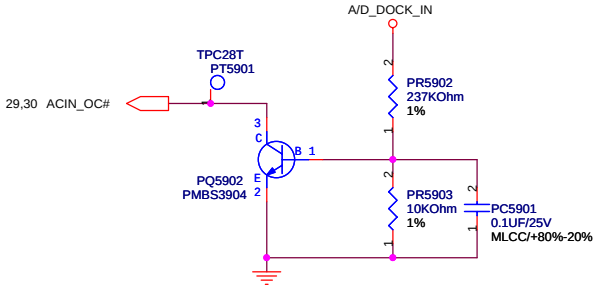
POWER PATH & BAT_LEARN



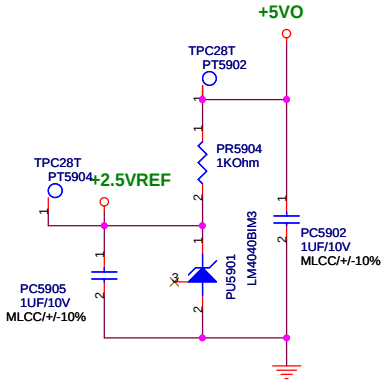
BATTERY IN DETECT



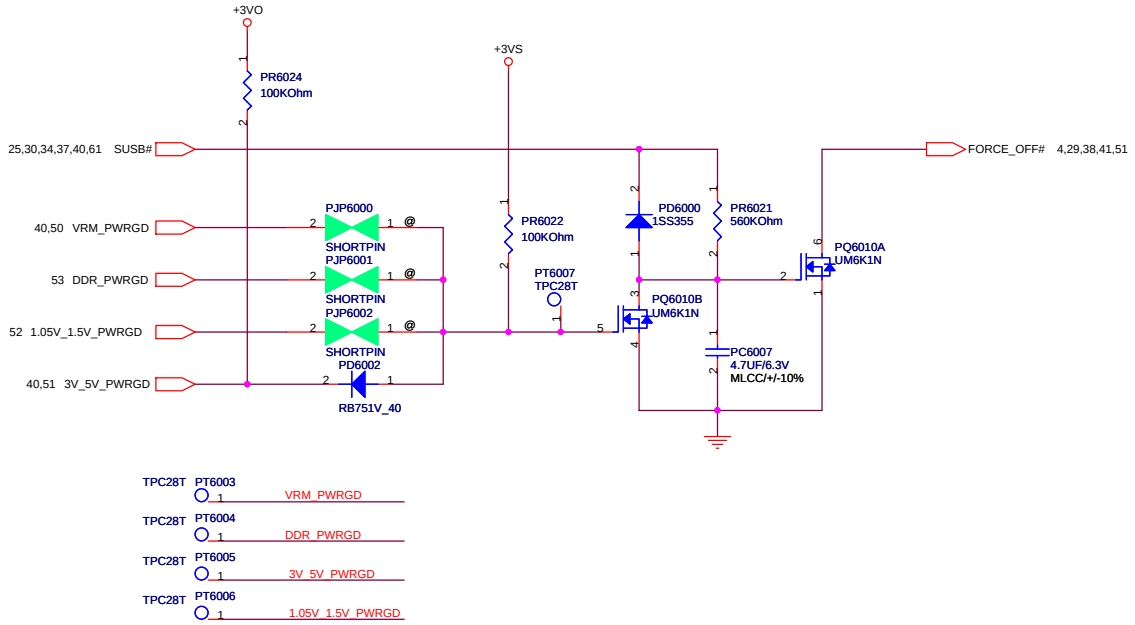
ADAPTER IN DETECT



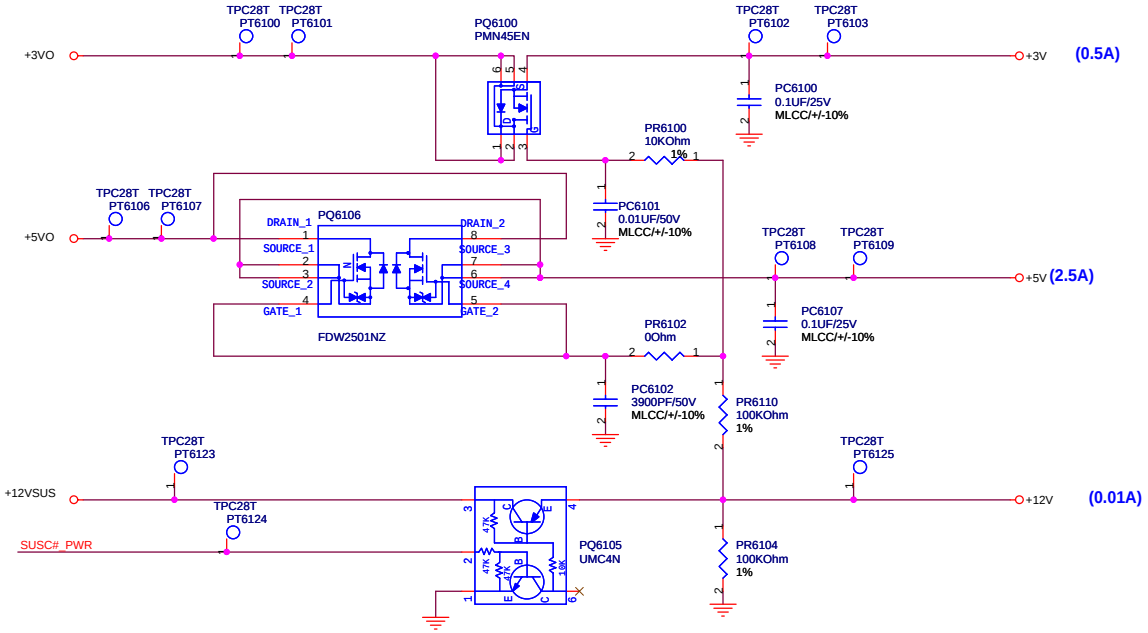
+2.5VREF

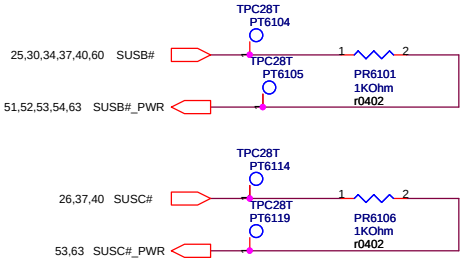


POWER GOOD DETECTER

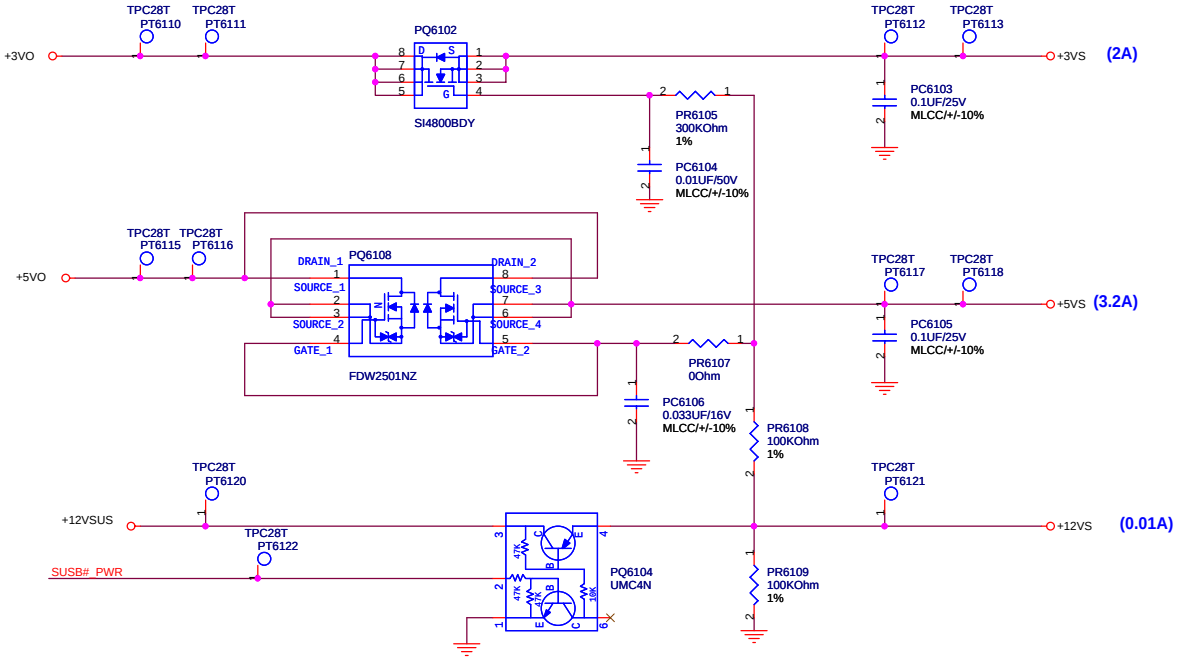


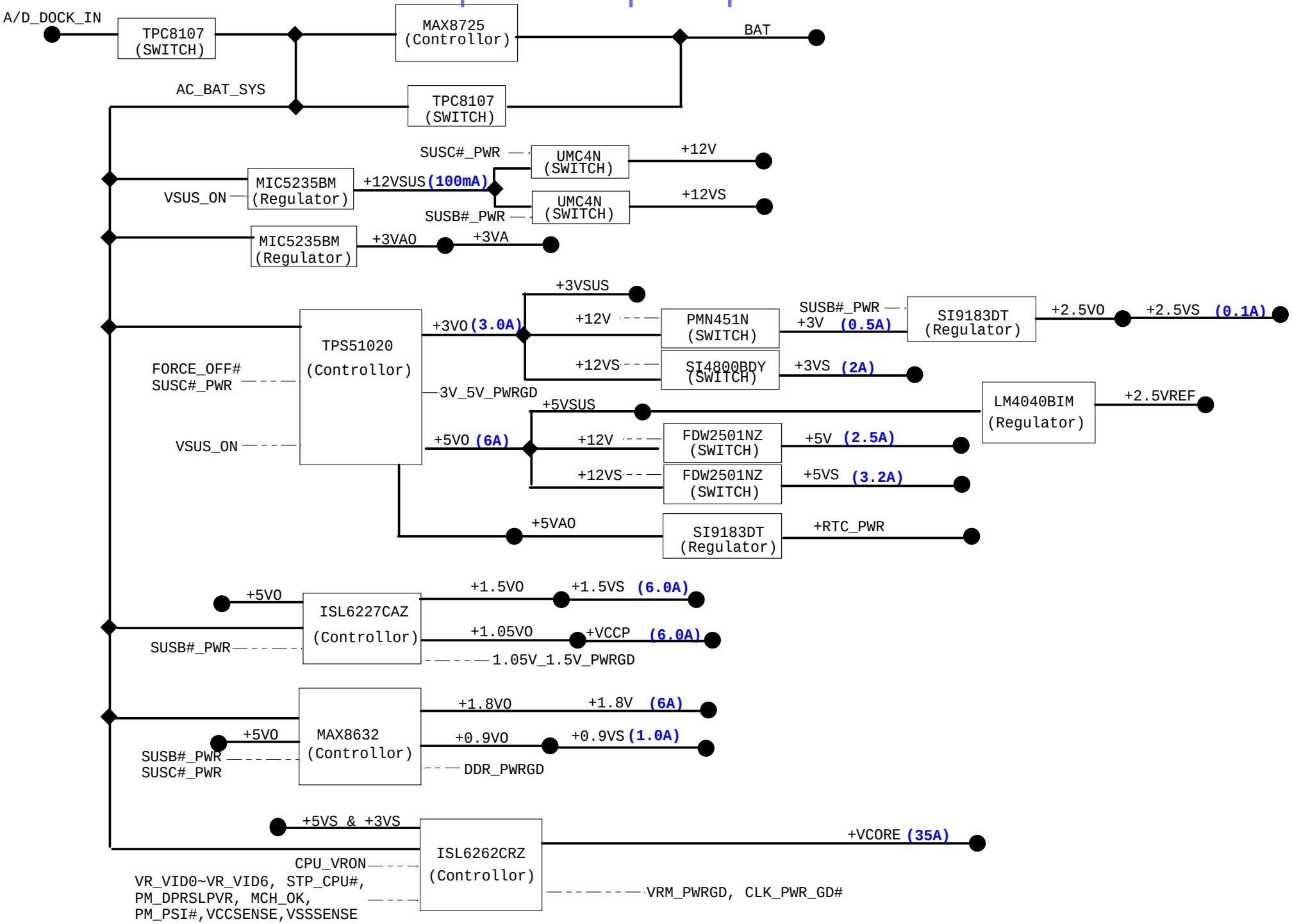
SUSC#_PWR POWER



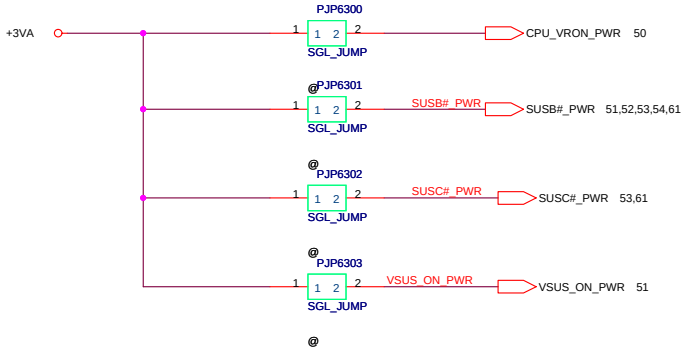


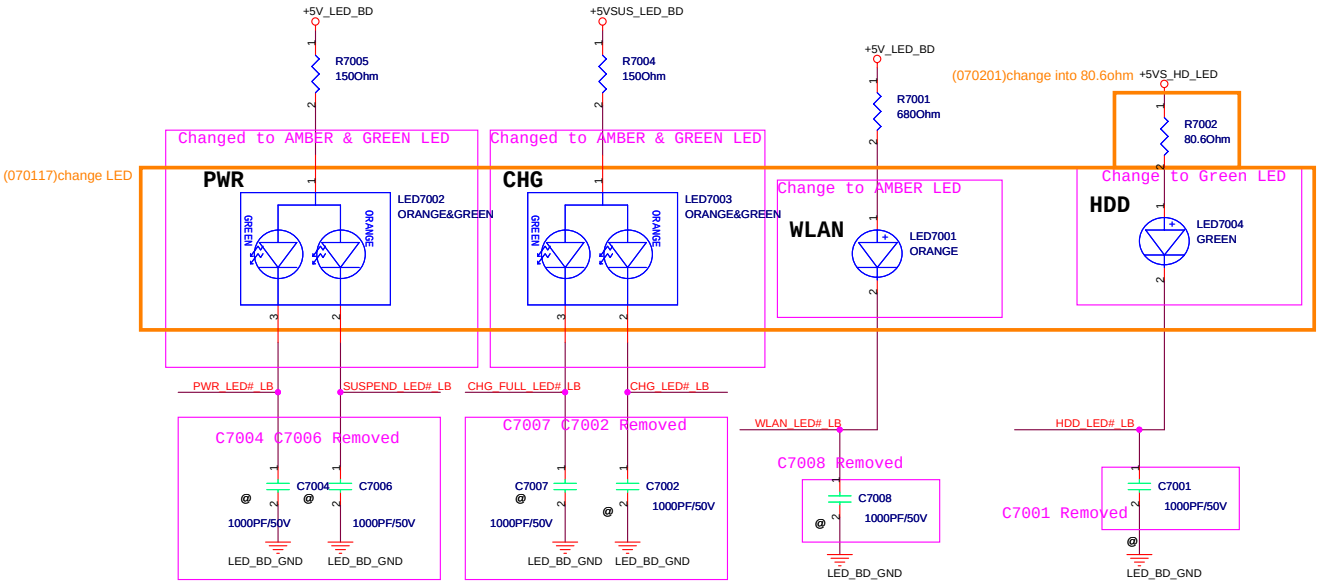
SUSB#_PWR POWER

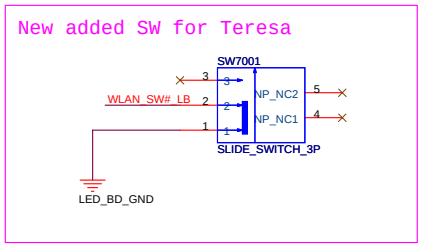


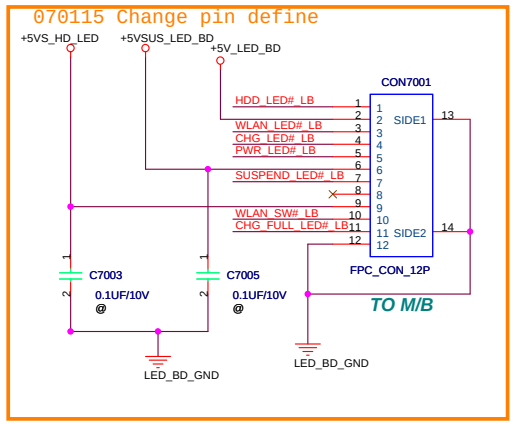


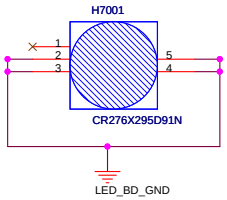
FOR POWER TEST



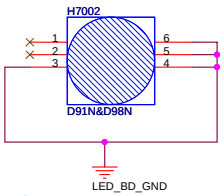








DETAIL: Q



DETAIL: S

Toshiba Satellite L40 schematic rev 1.1