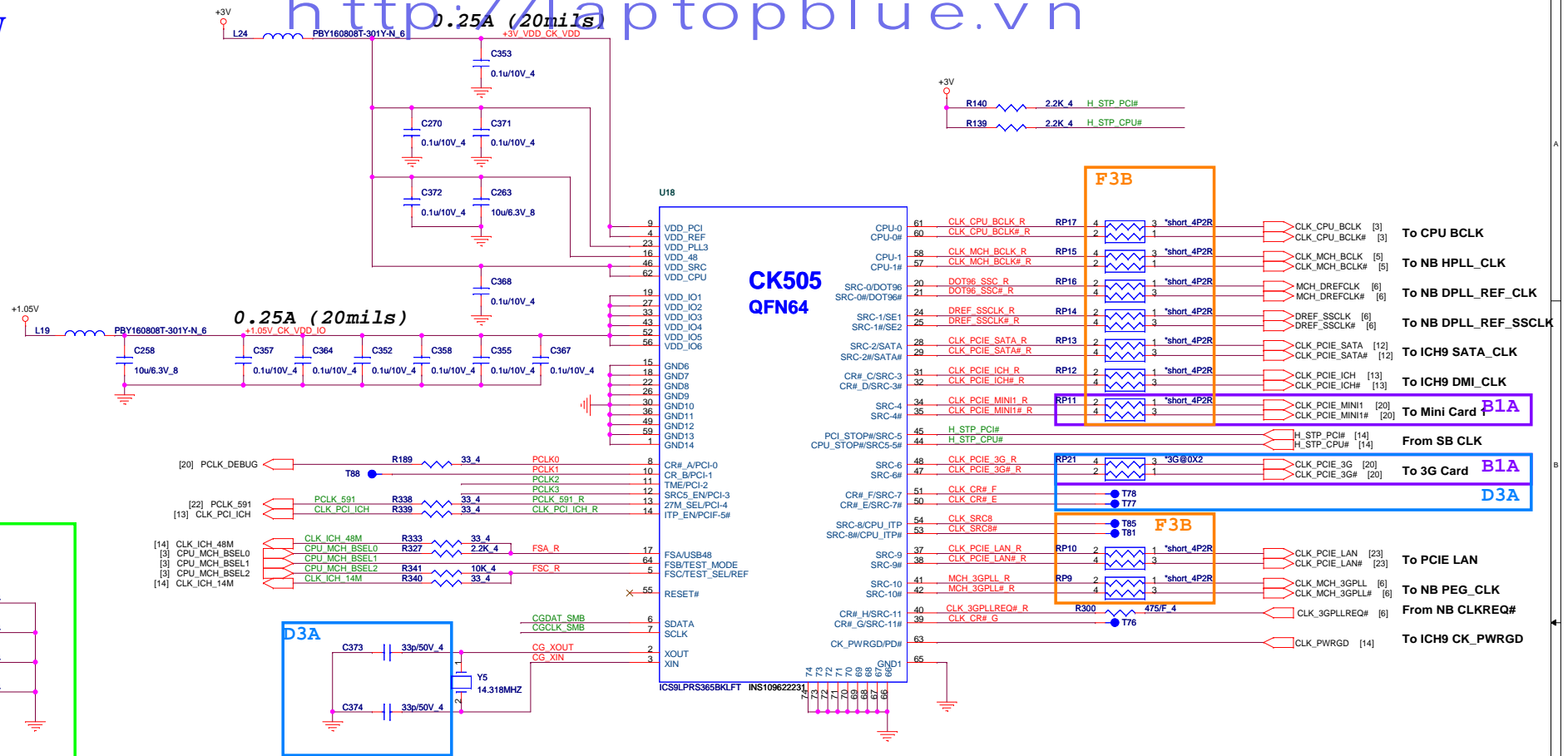


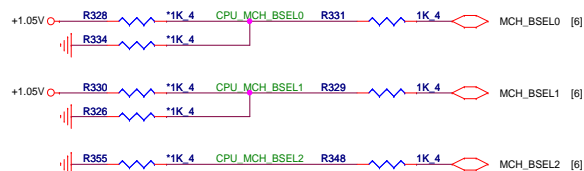
CLOCK GEN

0.25A (20mils)



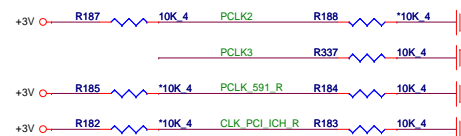
BSEL Frequency Select Table

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	23
0	0	1	123	100	23
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	233	100	35
1	1	0	400	100	33
1	1	1	SSVD	100	23

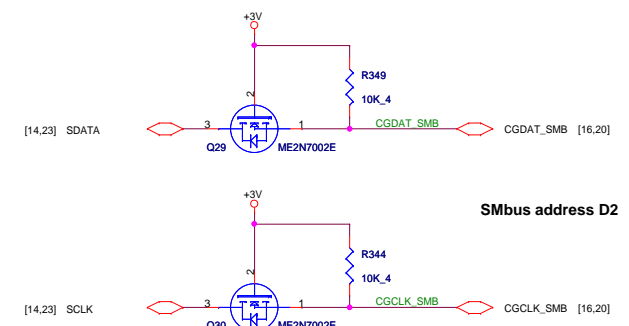


Clock Gen Strap

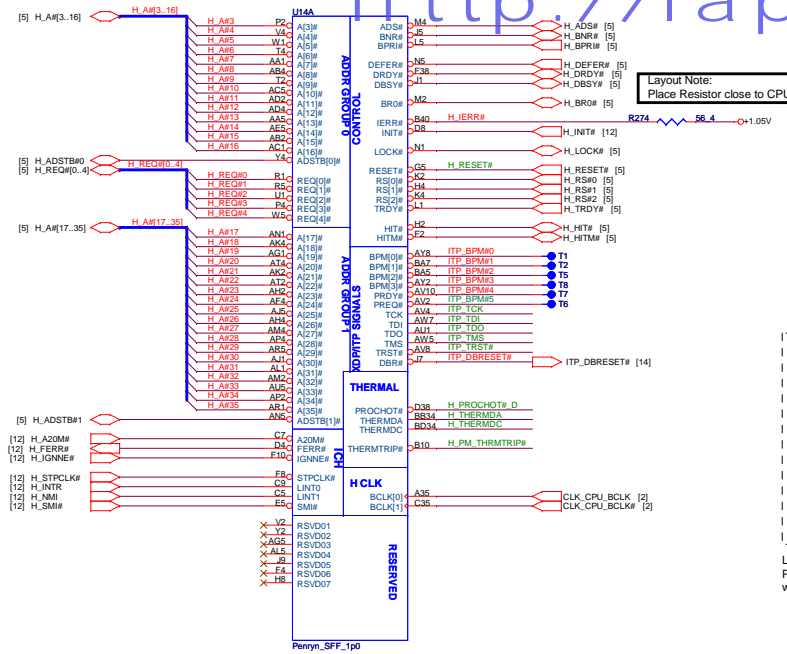
	SLG8SF513	PULL HIGH	PULL DOWN
PIN11	PCI2/TWE	NO OVERCLOCKING (default)	NORMAL RUN
PIN12	PCI-3	PIN44/45 IS SRC5	PIN44/45 IS PCI_STOP/CPU_STOP (default)
PIN13	PCI-4/27M_SEL	PIN 24/25 IS 27MHz	PIN 21/20 IS SRC/DOT (default)
PIN14	PCIF-5/ITP_EN	PIN 53/54 IS CPUITP	PIN 53/54 IS SRC (default)

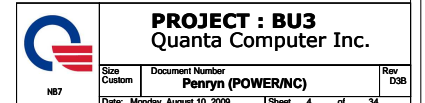


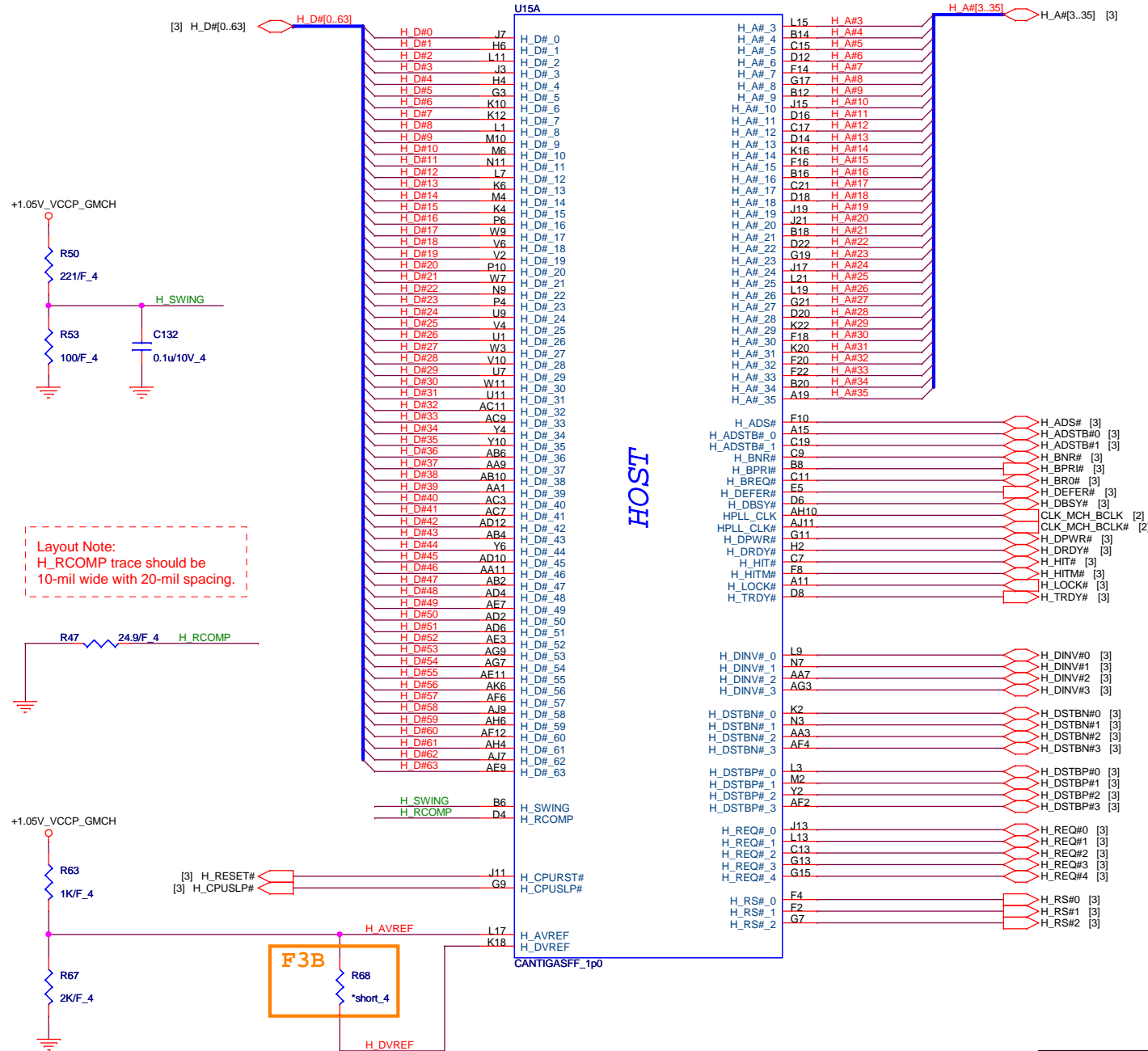
Clock Gen I2C



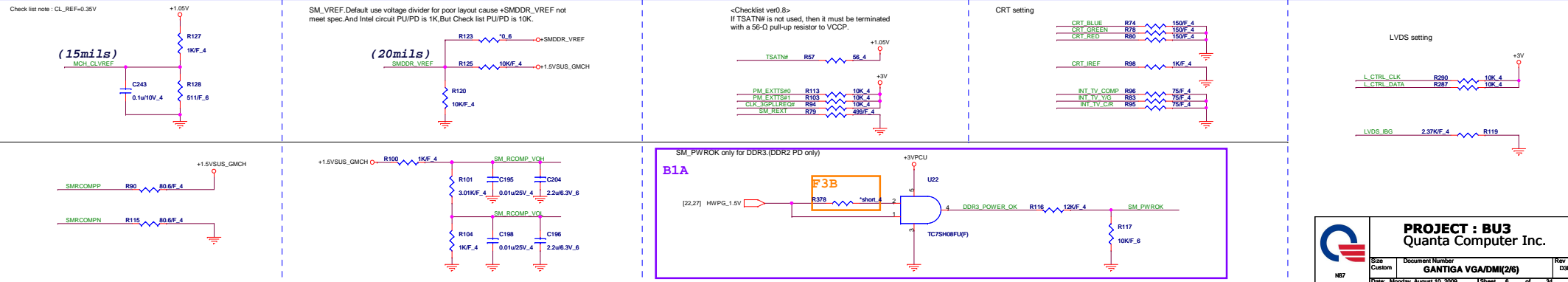
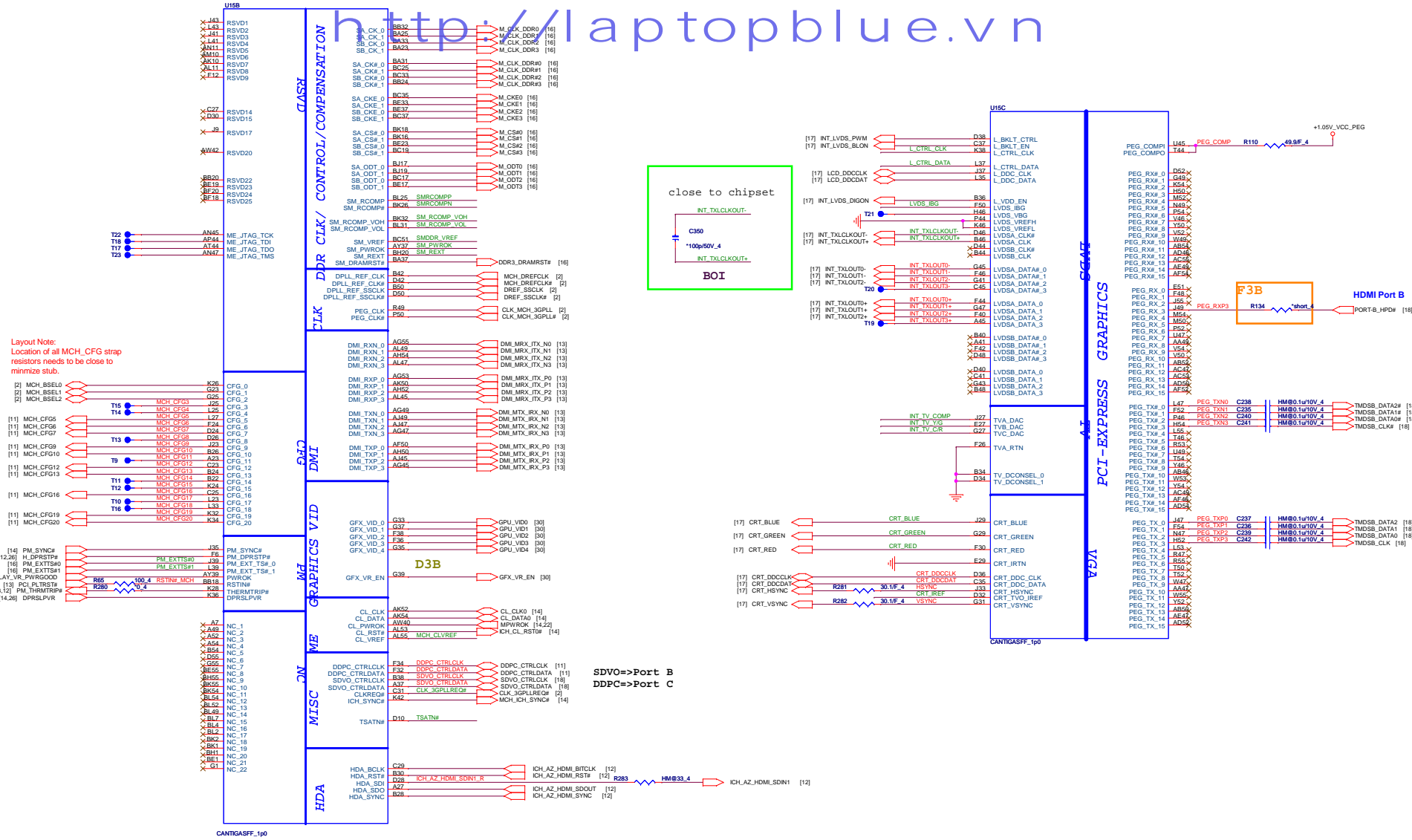
CPU

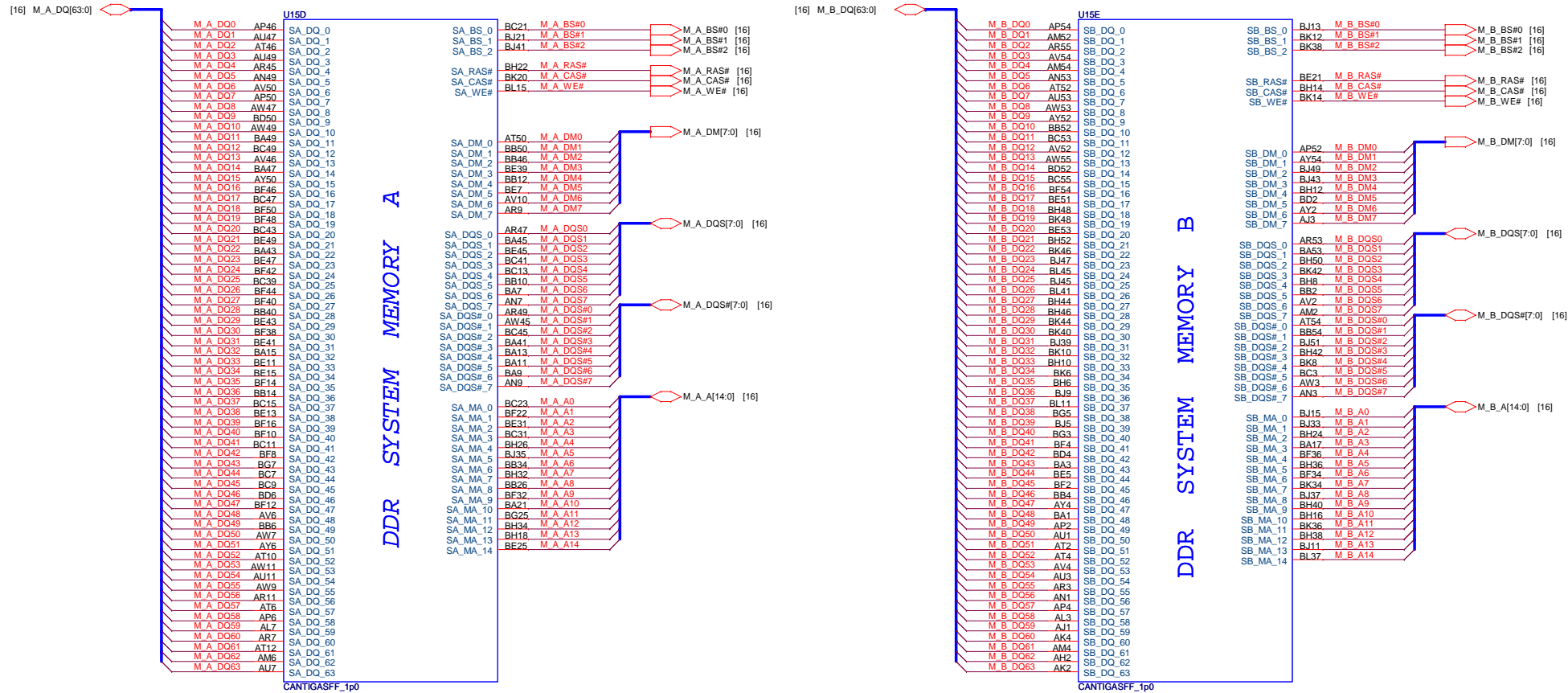


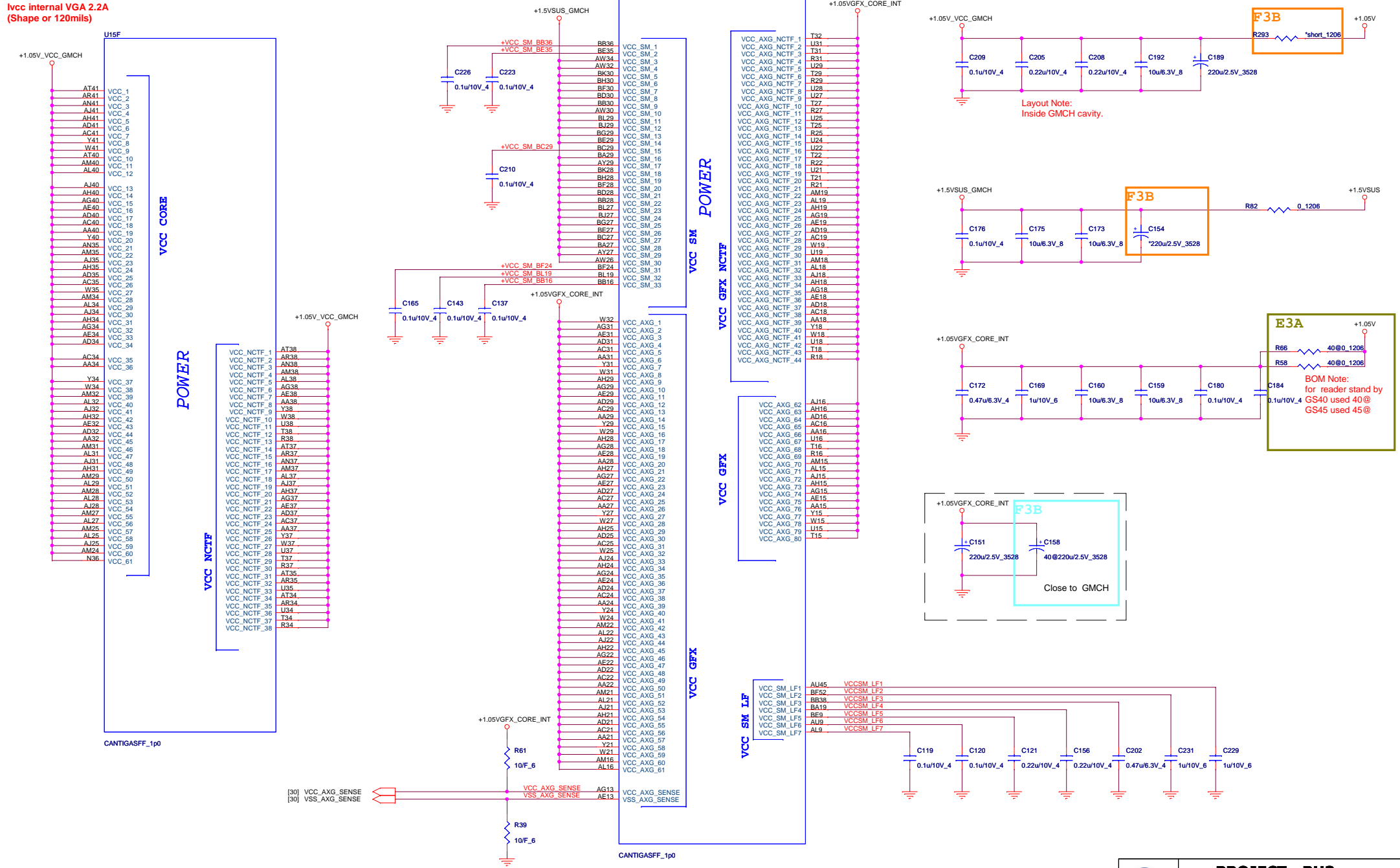


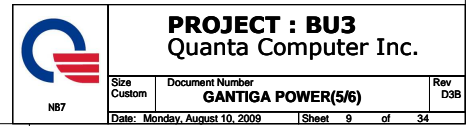


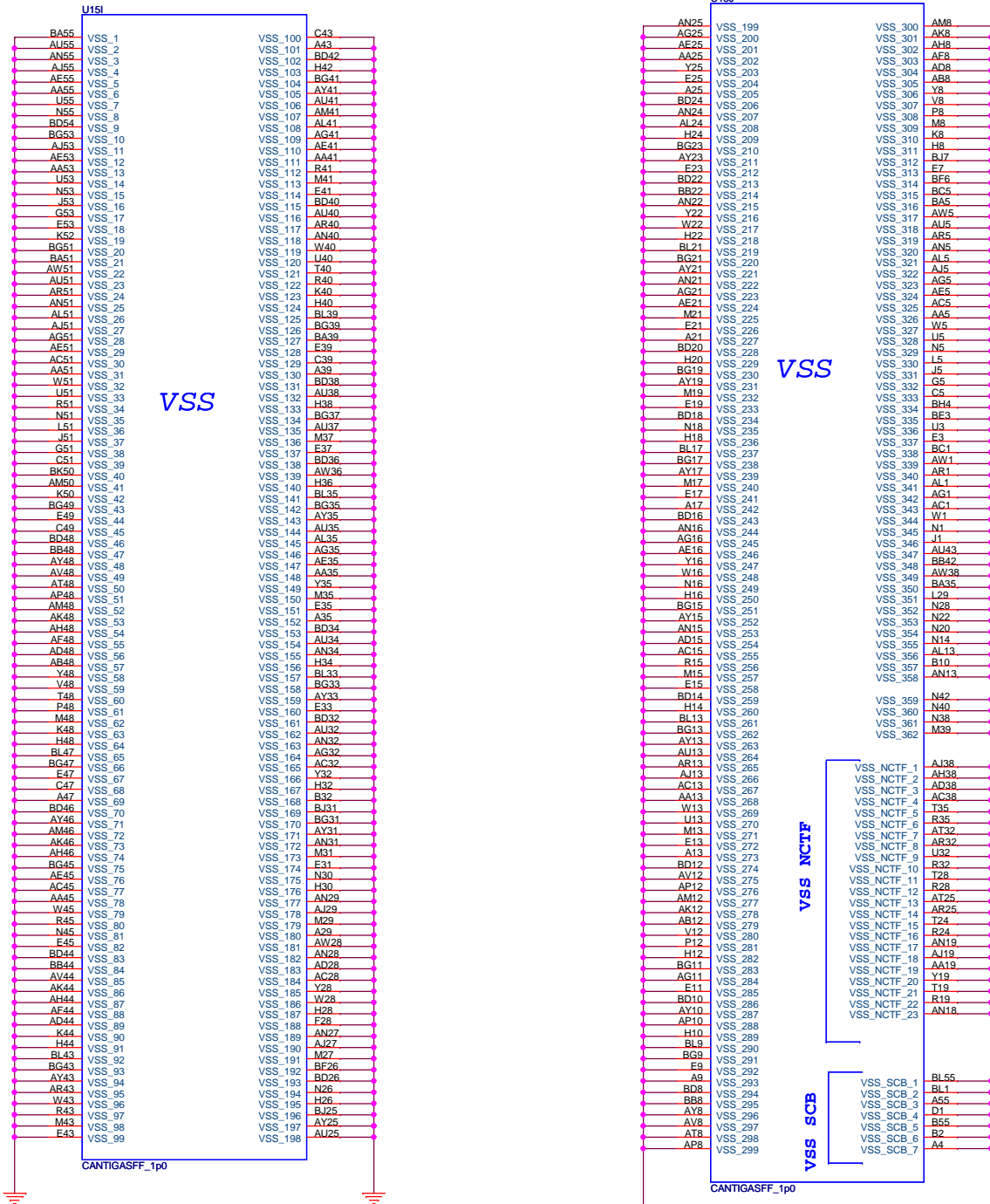
PROJECT : BU3
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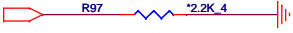
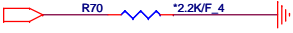
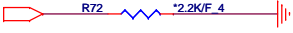
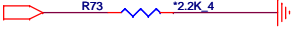
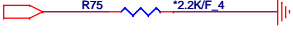
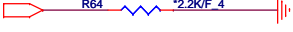
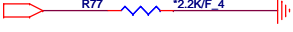
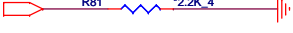
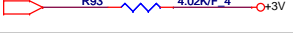
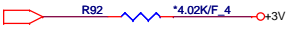





North Bridge Strap Pin Configuration Table

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(See DG 2.0 P306 Table 187)
(See NB EDS 1.0 P187 Table 74)

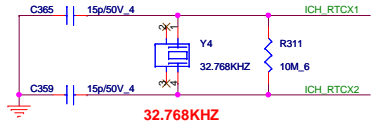
Pin Name	Strap description	Configuration	PU<4.02K> PD <2.21K>	Note
CFG[2:0]	FSB Frequency Select	[000]= FSB 1066MHz [010] = FSB 800MHz [011] = FSB 667MHz	See Page 2 FSB selection table	
CFG[4:3]	Reserved			
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)	[6] MCH_CFG5 	
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)	[6] MCH_CFG6 	
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)	[6] MCH_CFG7 	
CFG8	Reserved			
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)	[6] MCH_CFG9 	
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)	[6] MCH_CFG10 	
CFG11	Reserved			
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)	[6] MCH_CFG12 	
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)	[6] MCH_CFG13 	
CFG[15:14]	Reserved			
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)	[6] MCH_CFG16 	
CFG[18:17]	Reserved			
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed	[6] MCH_CFG19 	
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port	[6] MCH_CFG20 	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI/DP Device Present(Default) 1 = SDVO/HDMI/DP Device present	Strap on P18 SDVO_CTRLDATA	
L_DDC_DATA	Local Flat Panel(LFP) Present	0 = LFP Disable(Default) 1 = LFP Card Present;PCIE disable	Strap on P17 INT_LVDS_EDIDDATA	
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present	[6] DDPC_CTRLDATA 	

[6] DDPC_CTRLCLK 

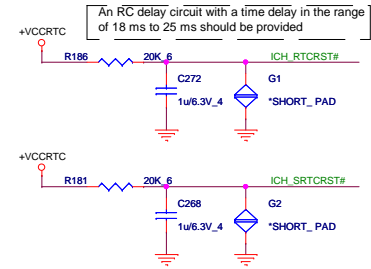
Enable iTPM Table

PAGE	Net Name	PU & PD	NOTE
11	MCH_CFG_6	PD 10K to GND	NB Strap pin
13	SPI_MOSI	PU 20K to +3V_S5	SB Strap pin
14	CLGPIO5	PU 10K to +3V_S5	SB Strap pin

RTC CRYSTAL

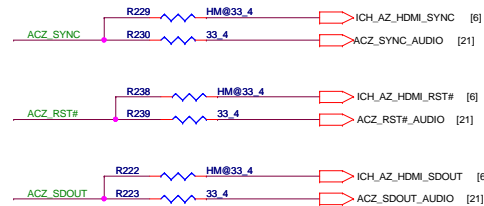
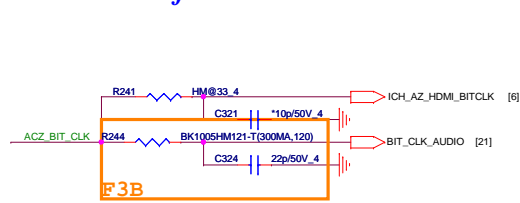


RESET JUMP



ICH_SATA_LED#	
0	PCIe Lane Reversed
1	PCIe Straight(default)

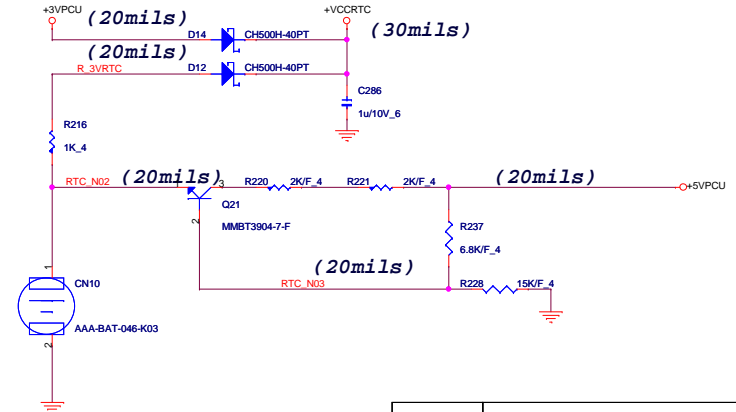
HD Audio Interface

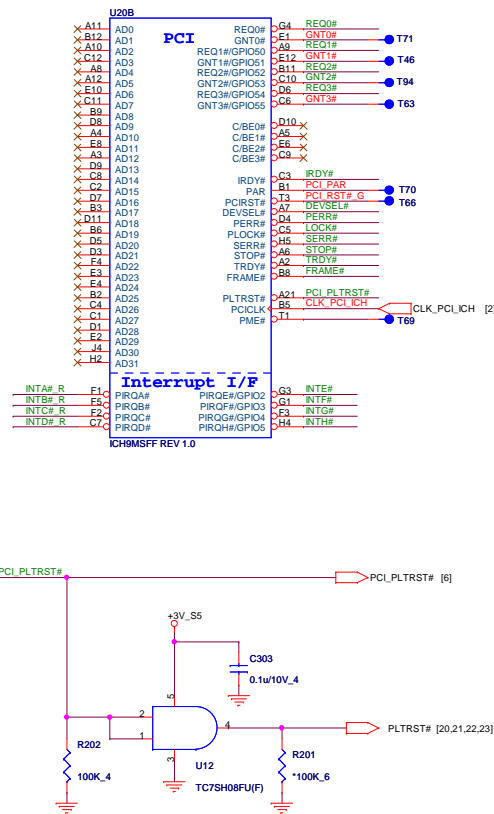


South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration			PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect			This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU			
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	ICH_TP3	HDA_SDOUT	Description	+1.5V_HDA_IO_ICH
			0	0	RSVD	
			0	1	Enter XOR Chain	
			1	0	Normal operation(Default)	
			1	1	Set PCIe port config bit 1	

RTC BATTERY





Pin Name	Strap description	Sampled	Configuration			PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0			+1.5V_HDA_IDA_IO_ICH
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default			
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default			
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default			
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable			
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0	SPI_CS#1	Boot Location	
			0	1	SPI(Default)	
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1	0	PCI	

The image contains three circuit diagrams, each showing a resistor network connected to a +3V supply and various signals.

Diagram 1: RP4 (8.2KX8)

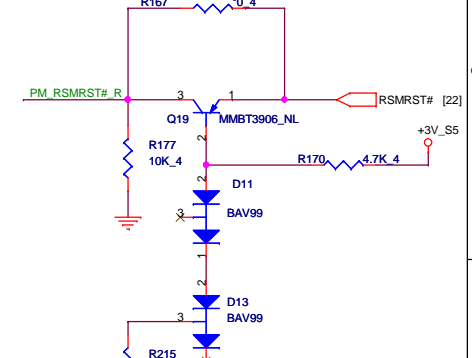
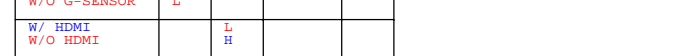
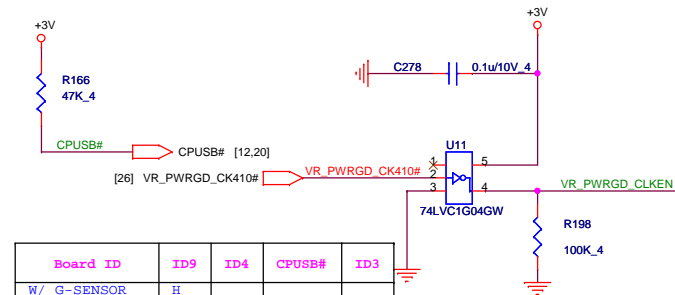
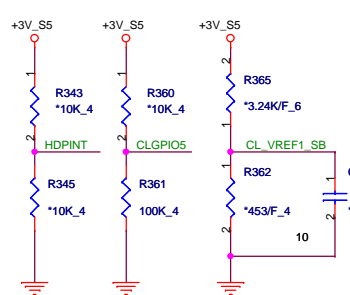
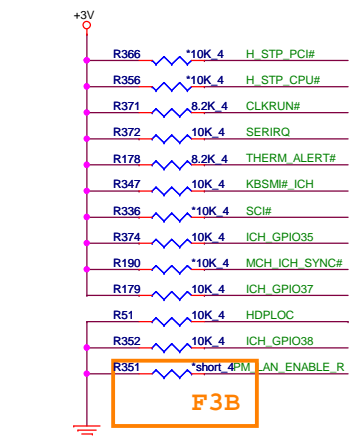
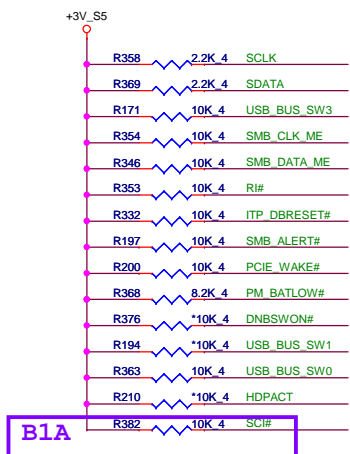
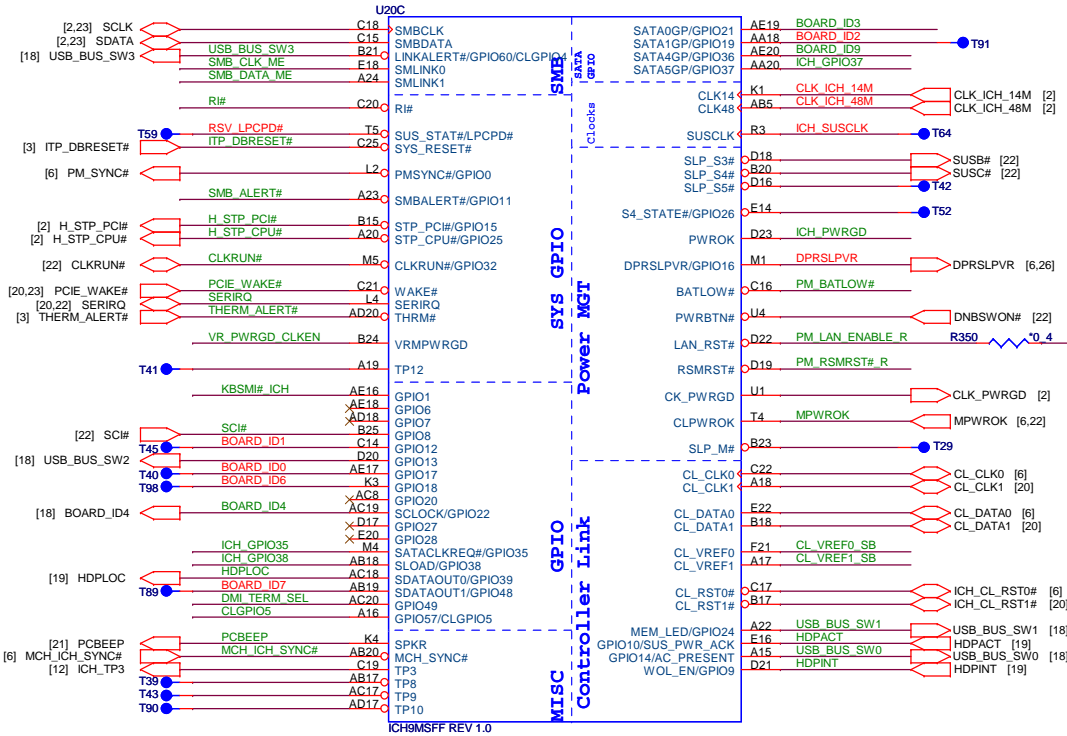
- Resistor network: RP4 (8.2KX8)
- Inputs (left):
 - 6: REO3#
 - 7: X
 - 8: X
 - 9: X
 - 10: +3V
- Outputs (right):
 - 5: +3V
 - 4: REO2#
 - 3: REO1#
 - 2: REO0#
 - 1: IRDY#

Diagram 2: RP18 (8.2KX8)

- Resistor network: RP18 (8.2KX8)
- Inputs (left):
 - 6: DEVSEL#
 - 7: X
 - 8: PERR#
 - 9: LOCK#
 - 10: +3V
- Outputs (right):
 - 5: +3V
 - 4: SERR#
 - 3: STOP#
 - 2: TRDY#
 - 1: FRAME#

Diagram 3: RP19 (8.2KX8)

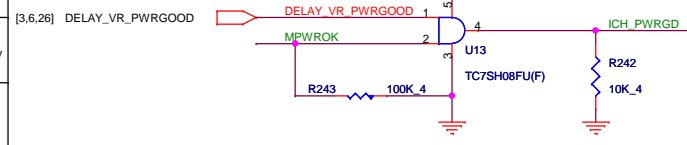
- Resistor network: RP19 (8.2KX8)
- Inputs (left):
 - 6: INTF#
 - 7: INT#
 - 8: INTB#
 - 9: INTG#
 - 10: +3V
- Outputs (right):
 - 5: +3V
 - 4: INTG#_R
 - 3: INTF#_R
 - 2: INTB#_R
 - 1: INTD#_R



South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
PCBEEP	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCBEEP R245 1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R172 1K_4

Board ID	ID9	ID4	CPUSB#	ID3
W/ G-SENSOR W/O G-SENSOR	H L			
W/ HDMI W/O HDMI		L H		
W/ 3G W/O 3G			H L	
FOR 11" FOR 13"				H L



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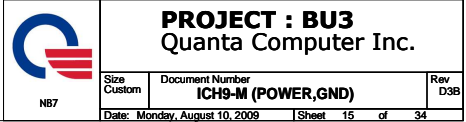
Size Custom

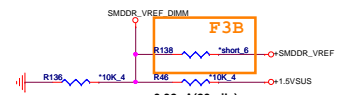
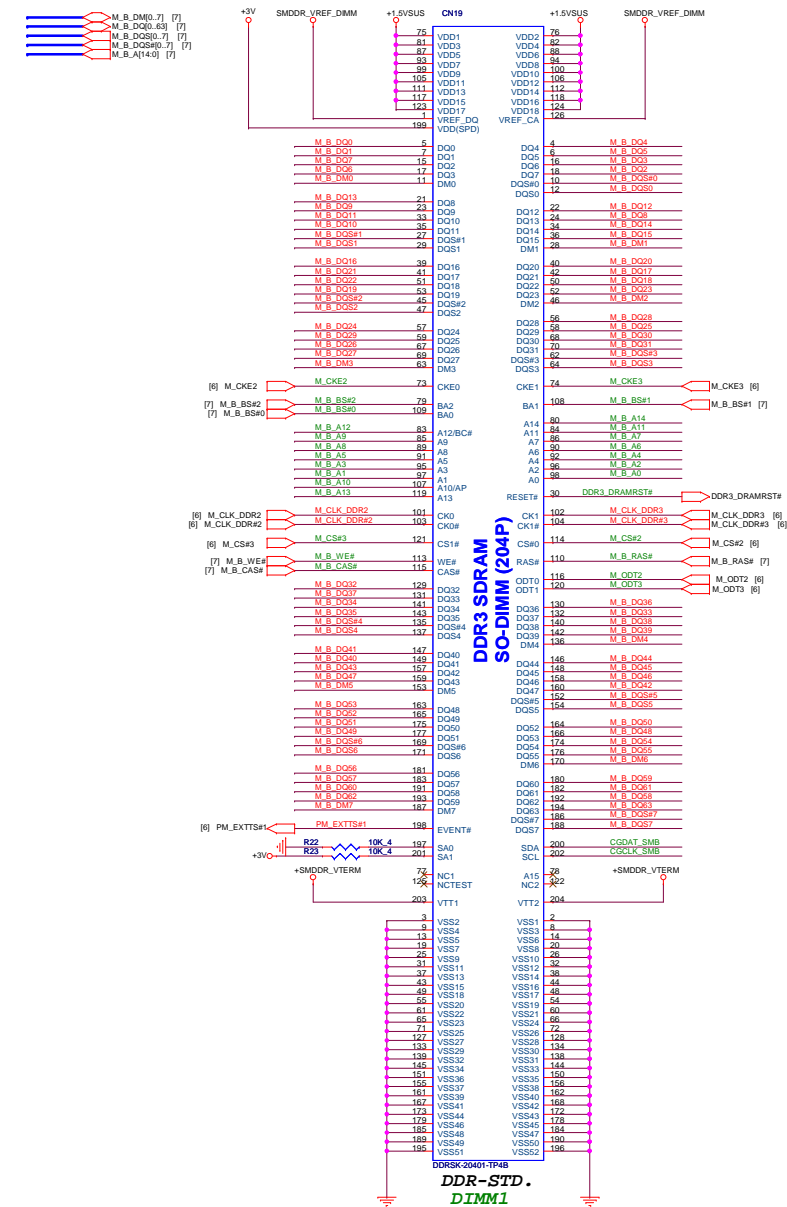
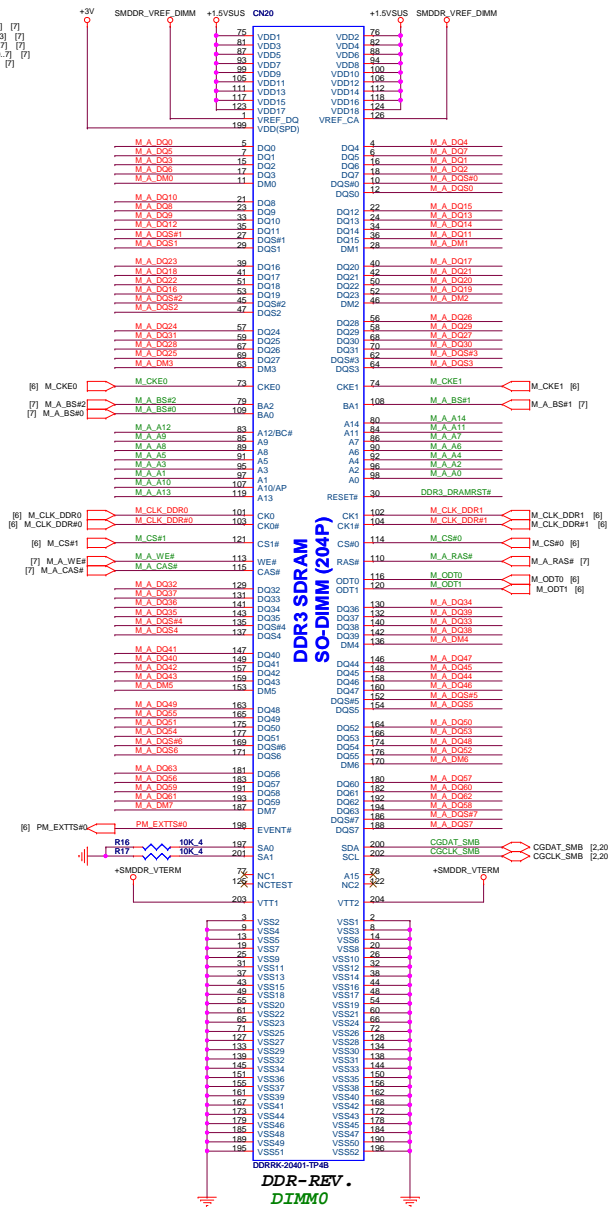
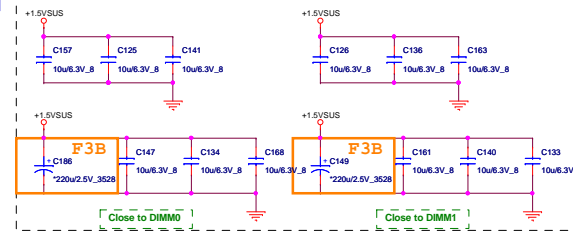
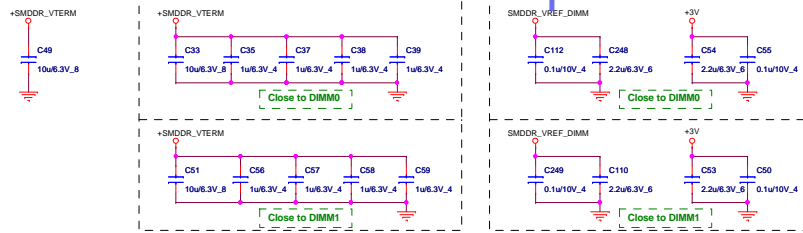
Document Number
ICH9-M (PM,GPIO,SMB)

Date: Monday, August 10, 2009

Rev D3B

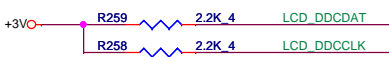
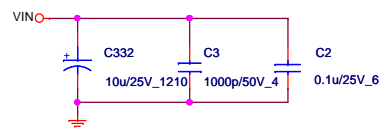
Sheet 14 of 34



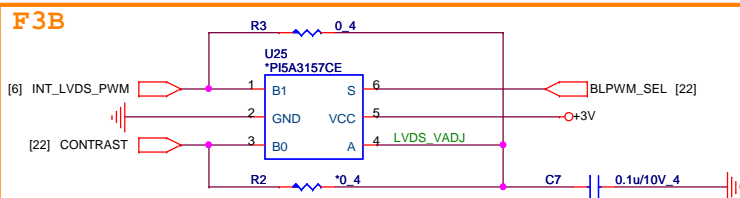
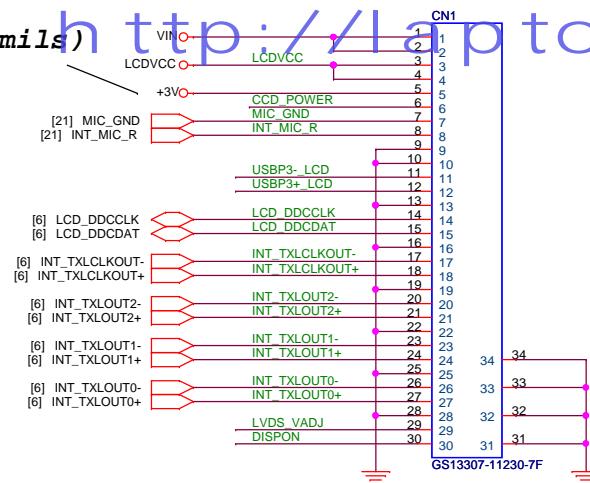


LCD Panel Module

0.3A (20mils)

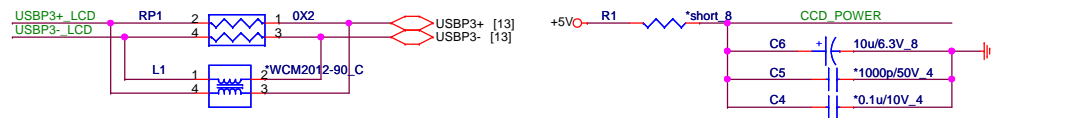


NB Strap
INT_LVDS_EDIDDATA

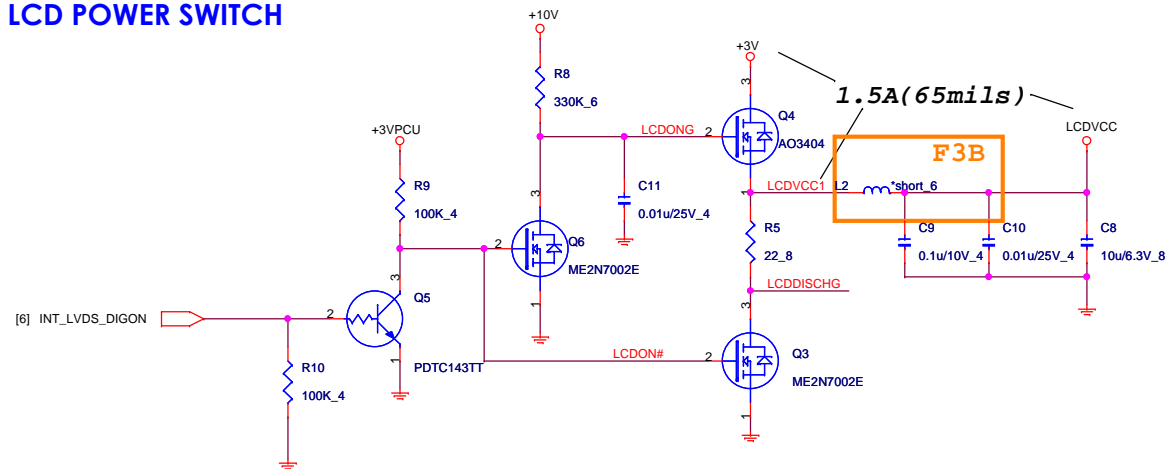


input S	S	S
output A		
INT_LVDS_PWM	H	
CONTRAST		L

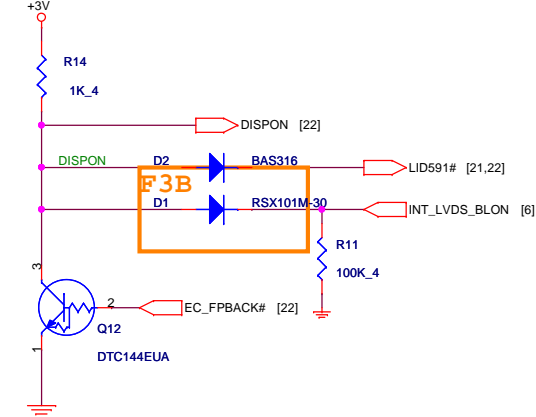
CCD



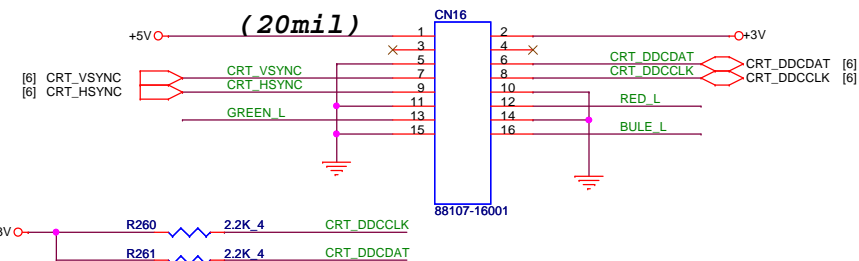
LCD POWER SWITCH



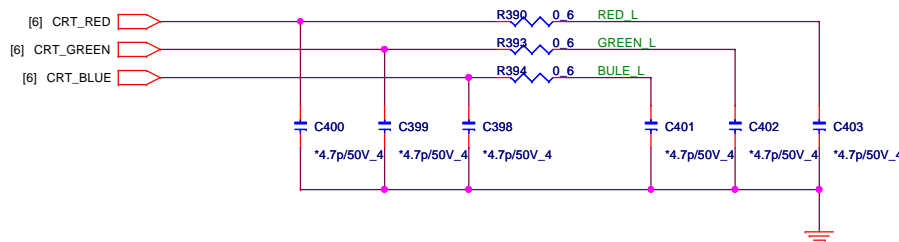
HALL SENSOR&BACK LIGHT SWITCH



CRT CON.



E3A

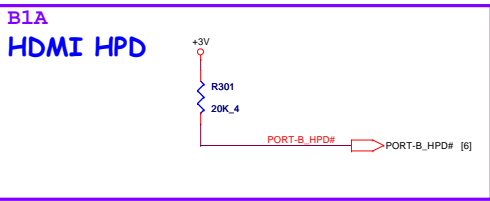
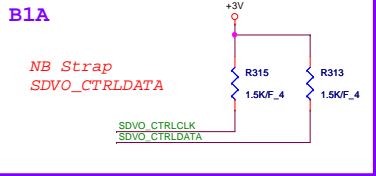


CRT CON. co-lay

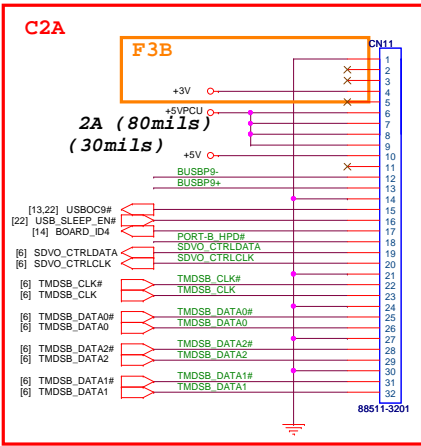
E3A

HDMI IC

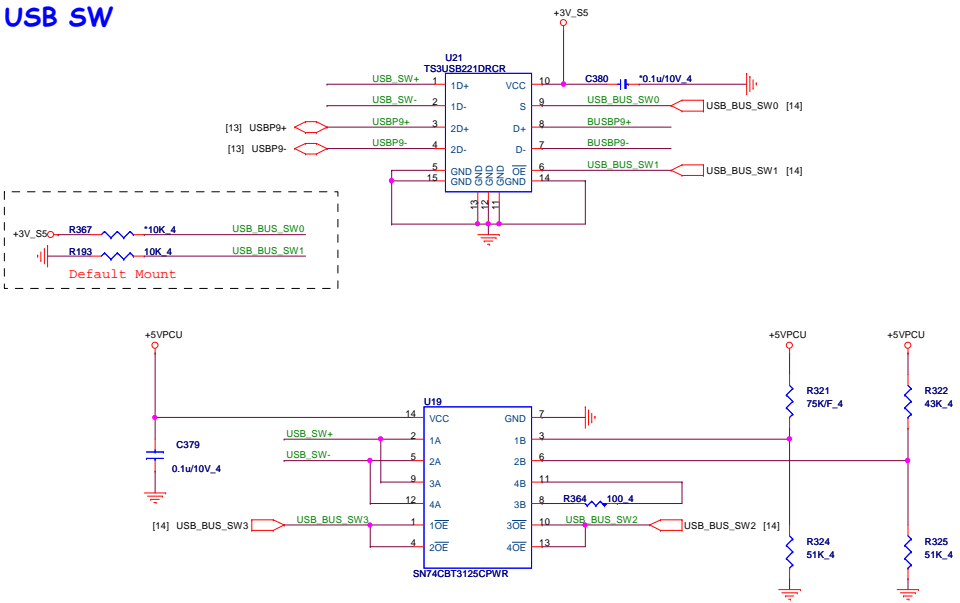
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HDMI CON.



USB SW



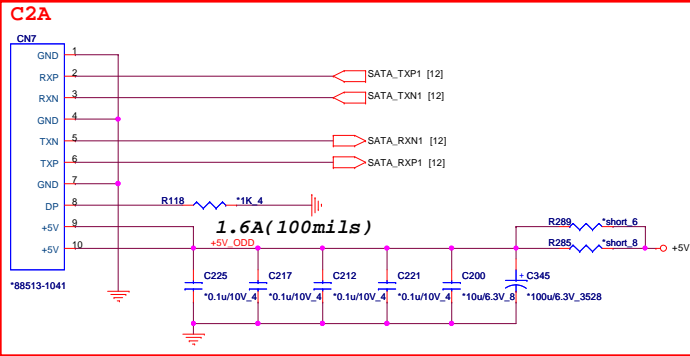
EMI

S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

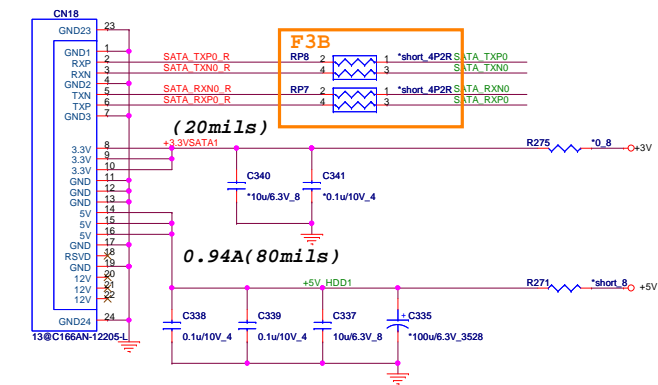
OE#	Function
H	Disconnect
L	A port= B port

OE#	1OE#	2OE#	3OE#	4OE#
Mode3	High	High	Low	Low
Mode4	Low	Low	High	High

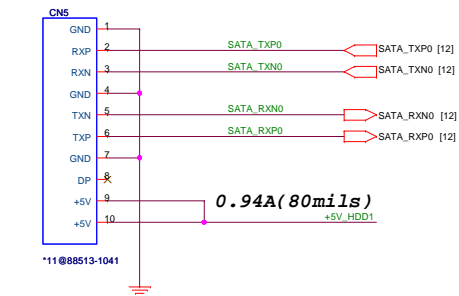
SATA ODD



Main SATA HDD

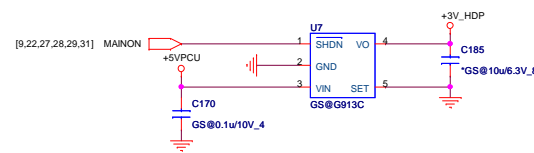


Main SATA HDD (For 11.6")



CO-LAYOUT With MAIN SATA HDD

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FS (Full Scale) selection

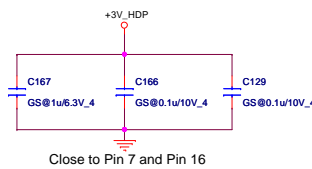
FS	0	1
2g Full-Scale		
6g Full-Scale		

PD (Power Down) selection

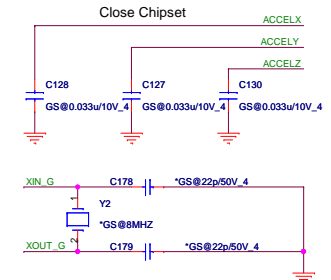
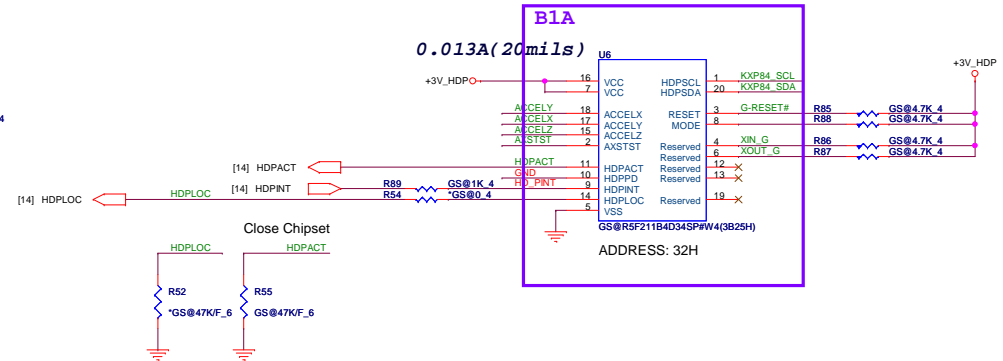
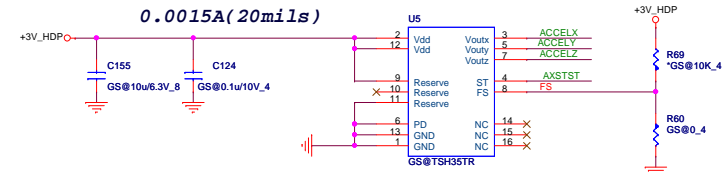
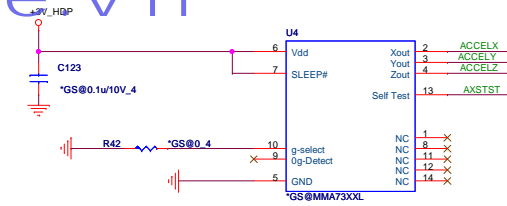
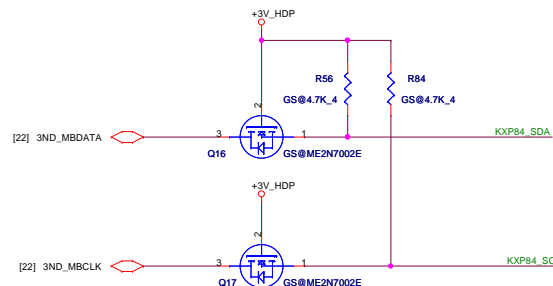
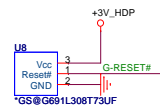
PD	0	1
Normal Mode		
Power-down mode		

HDPPD selection

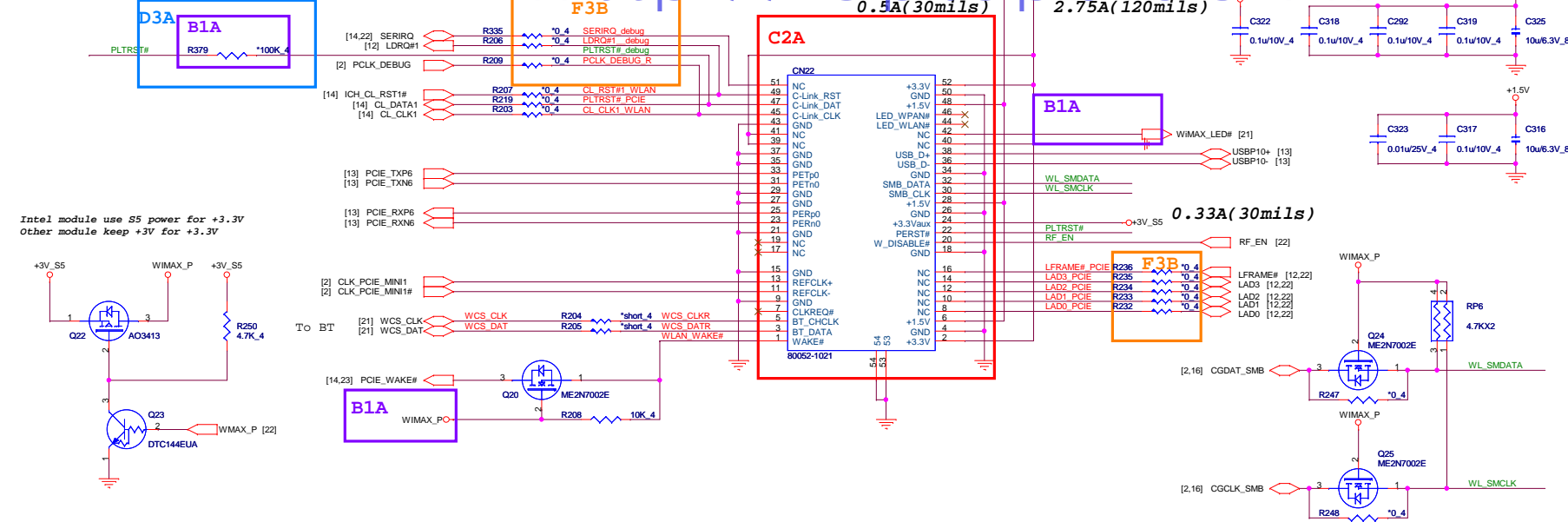
HDPPD	0	1
Normal Mode		
Power-down mode		



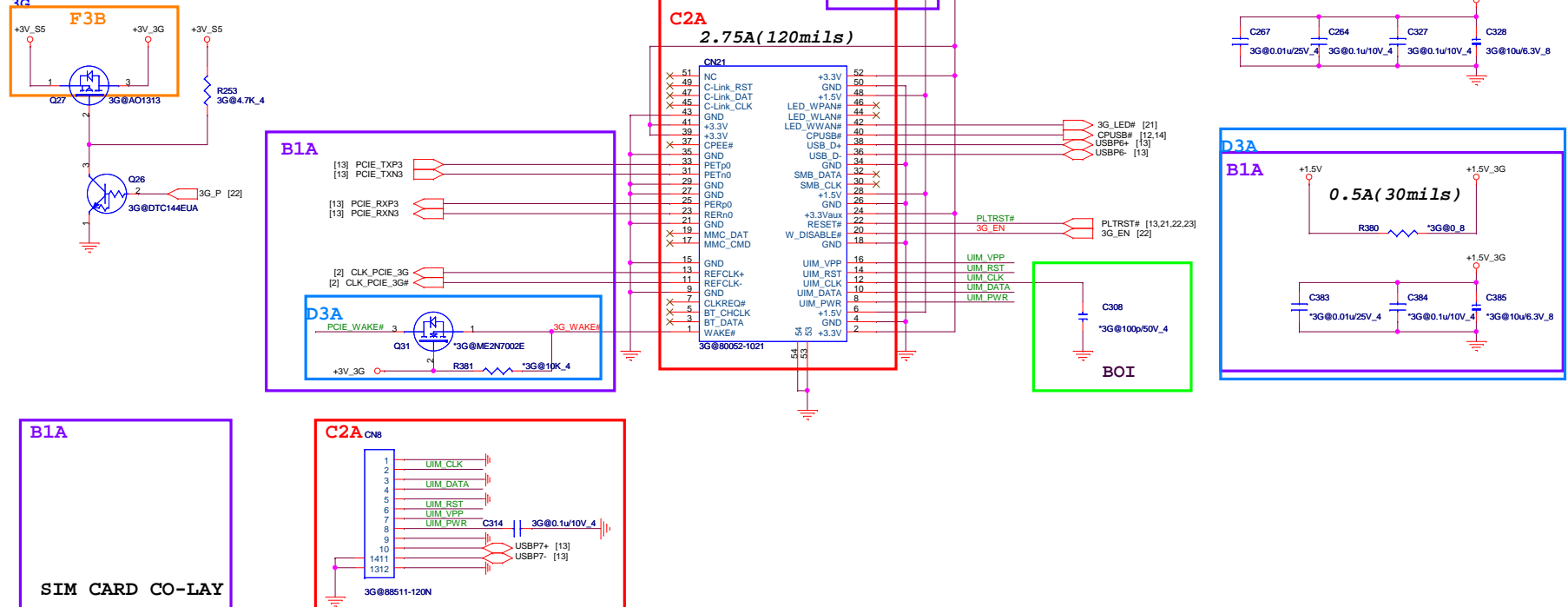
Close to Pin 7 and Pin 16



MINI Card Slot#1 (WLAN)



MINI Card Slot#2 3G



SIM CARD CO-LAY

The schematic diagram illustrates the LED driver circuit for the 10mil5 LED. The circuit is powered by a 3VPCU input, which is connected to a 10KX8 resistor network. The output of the resistor network is connected to the LED driver IC, 196130-340201. The IC has 36 pins, with pins 36 and 35 connected to ground. The output of the IC is connected to a 150 ohm resistor and a 10mil5 LED. The circuit also includes a 100pF/50V capacitor and a 100pF/50V capacitor. The LED is labeled (10mil5) and the resistor is labeled 150_4. The circuit is powered by a 3V0 source.

Diagram showing the pinout for CN9 connector. The pins are numbered 1 through 40. The connections are as follows:

- Pin 1: ACZ_SDINO_AUDIO [12]
- Pin 2: ACZ_SDOUT_AUDIO [12]
- Pin 3: ACZ_SYNC_AUDIO [12]
- Pin 4: ACZ_RST#_AUDIO [12]
- Pin 5: BIT_CLK_AUDIO [12]
- Pin 6: MIC_GND [17]
- Pin 7: INT_MIC_R [17]
- Pin 8: PCBPBEE [14]
- Pin 9: AMP_MUTE# [22]
- Pin 10: USBOCIO_1 [13,22]
- Pin 11: USBP0+ [13]
- Pin 12: USBP0- [13]
- Pin 13: USBP1+ [13]
- Pin 14: USBP1- [13]
- Pin 15: USB_EN#0_1 [22]
- Pin 16: +3V
- Pin 17: VDDIO_CODEC R176
- Pin 18: +1.5V
- Pin 19: +5V
- Pin 20: +5VPCU
- Pin 21: 3A (140mils)
- Pin 22: MMC_LED#
- Pin 23: PLTRST# [13,20,22,23]
- Pin 24: USBP4+ [13]
- Pin 25: USBP4- [13]

Current specifications for several pins:

- Pin 16: 0.34A (20mils)
- Pin 18: 0.61mA (15mils)
- Pin 19: 1.008A (45mils)
- Pin 21: 3A (140mils)

Other labels include: CN9, F3B, 88511-400N.

Timing diagram for USBP2+ and USBP2- signals. The diagram shows a 10-bit bus with signals for USBP2+, USBP2-, BT_RESET, BT_EN, and WCS_CLK. A red arrow indicates a 0.18A (20mils) timing constraint on the BT_RESET signal.

B1A

CN6

Pin	Signal	Notes
18	+5V	
17	+3VPCU	
16	+3V	
15	ACIN	[22,24]
14	PWRLED#	[22]
13	SUSLED_EC	[22]
12	BAT_SATO	[22]
11	BAT_SAT1	[22]
10	SATA LED# C	
9	RF_LED	[22]
8	3G_WIMAX LED#	
7	MMC_LED#	
6	TPDATA	[22]
5	TPCLK	[22]
4	LID591#	[17,22]
3	Ground	
2	Ground	
1	Ground	

88511-180N

C2a

The diagrams show three different hole configurations for the C2a component. Each diagram includes a pinout table and a circuit schematic.

- HOLE6:** Pinout table shows pins 7, 6, 5, 4, 3, 2, 1. The schematic shows a 1N4148 diode connected to pin 1 (anode) and pin 2 (cathode).
- HOLE7:** Pinout table shows pins 7, 6, 5, 4, 3, 2, 1. The schematic shows a 1N4148 diode connected to pin 1 (anode) and pin 2 (cathode).
- HOLE8:** Pinout table shows pins 7, 6, 5, 4, 3, 2, 1. The schematic shows a 1N4148 diode connected to pin 1 (anode) and pin 2 (cathode).

HOLE11

H-C154D91P2

HOLE10

H-C154D91P2

HOLE9

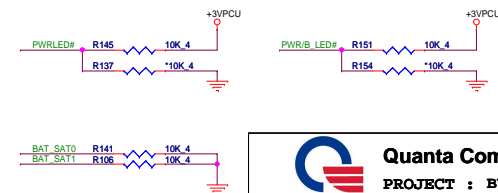
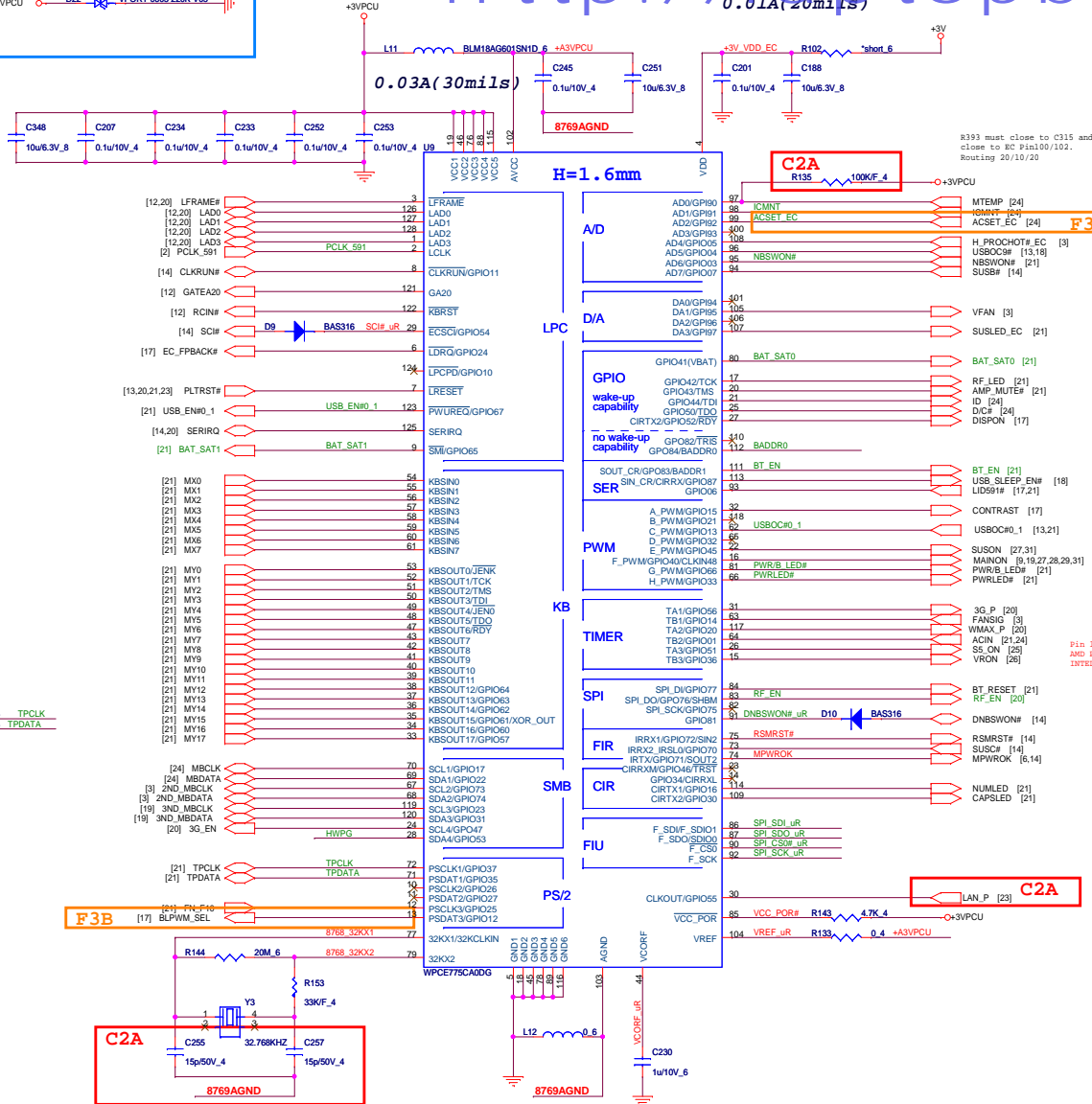
H-C154D91P2

HOLE12 HOLE13 HOLE14

¹H-C154D81P2 ¹H-C154D81P2 ¹H-C154D81P2

E3A +1.5V_{DS}

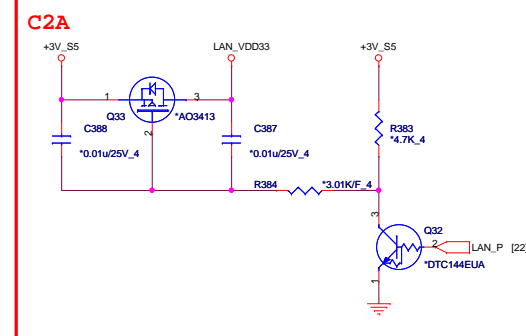
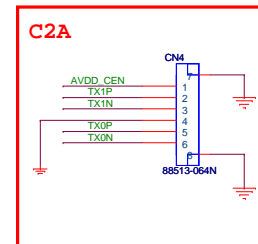
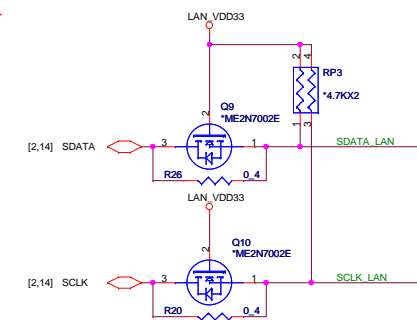
The diagram shows a ladder network of capacitors. A +1.5V_{DS} source is connected to a series of capacitors C397, C396, C395, C394, C393, C392, C391, and C390. Each capacitor has a value of 0.1uF/10V_4. The capacitors are connected in a ladder configuration, with the input source connected to the top of C397, and the bottom of each capacitor connected to the top of the next capacitor in the series. The bottom of the last capacitor, C390, is connected to ground.

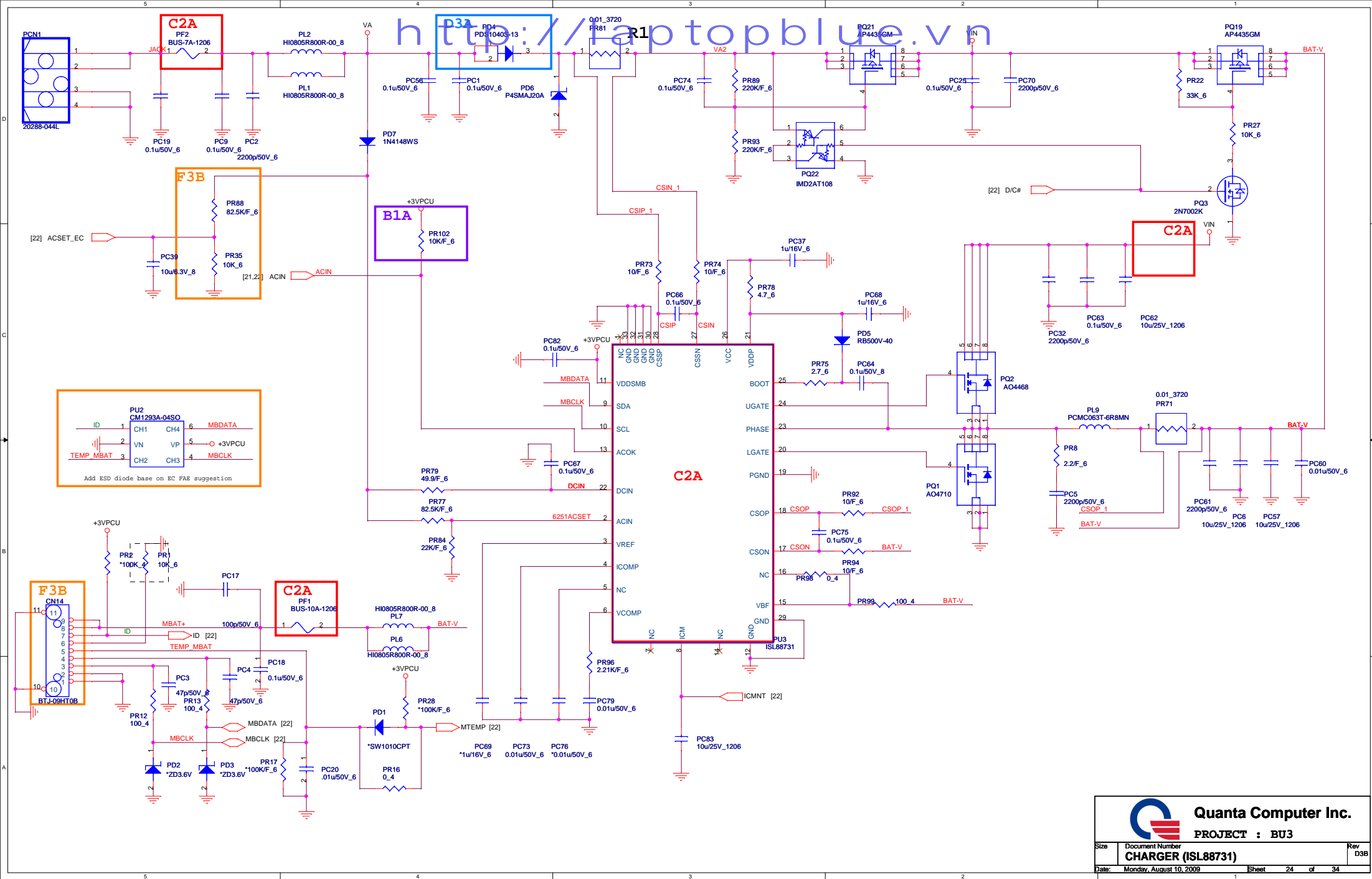


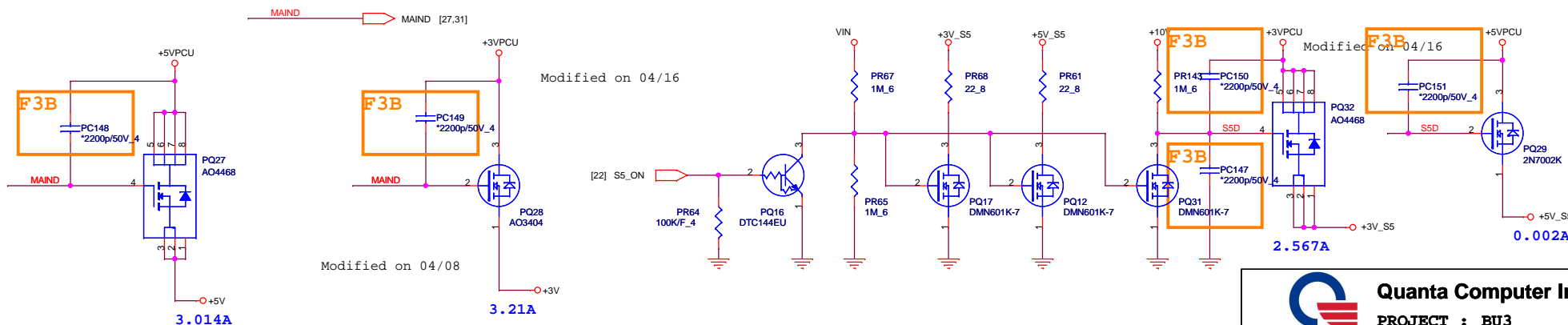
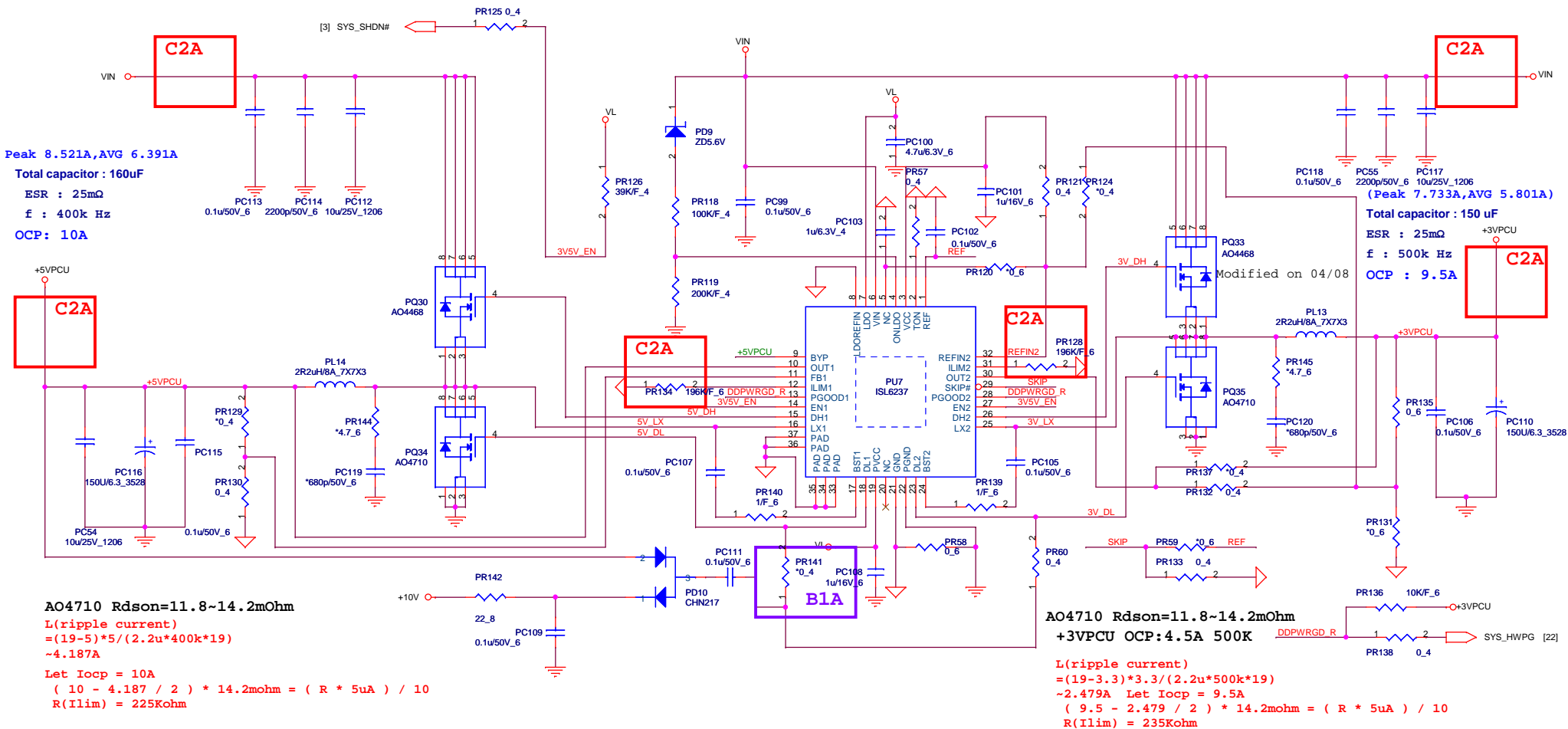
 **Quanta Computer Inc.**
PROJECT : BU3

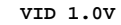
Size	Document Number EC-WPCE775CA0DG	Rev D3
Date	Monday, August 10, 2009	Sheet 22 of 24

SMBUS	Devices	Address
1	Battery	
2	CPU Thermal Sensor1	98H
	EC EEPROM	A0H
3	3D Sensor	40H









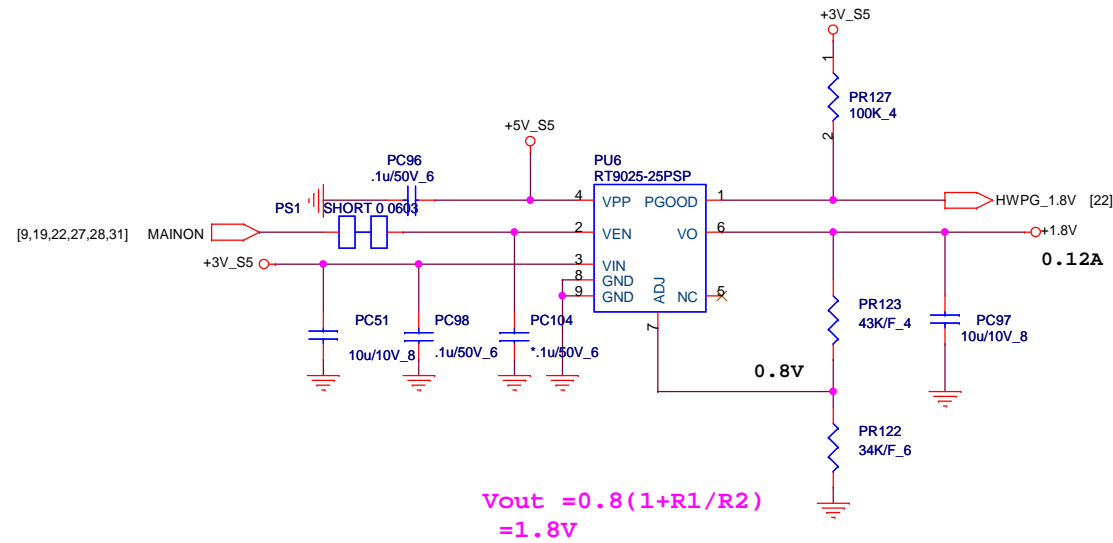
Peak 18A,AVG 15A
Total capacitor : 440uF
ESR : 4.5mΩ
f : 300k Hz
OCP: 20A

```
Rfset(Kohm) = ( period(us) - 0.29) * 2.33
Period(us) = Rfset(Kohm) / 2.33 + 0.29 = 3.213 * 10-6 s
Frequency = 1 / (3.213 * 10-6) = 311K
```

$$L(\text{ripple current}) = (19-1) \cdot 1 / (1.0 \mu \cdot 311 \text{ k} \cdot 19) \sim 3.05 \text{ A}$$

```
Rocset = ( Ioc * Rdroop) / 10uA
Rdroop = 4mV/A
Ioc = Rocset * 10uA / Rdroop = 20.15A
```


http://laptopblue.vn

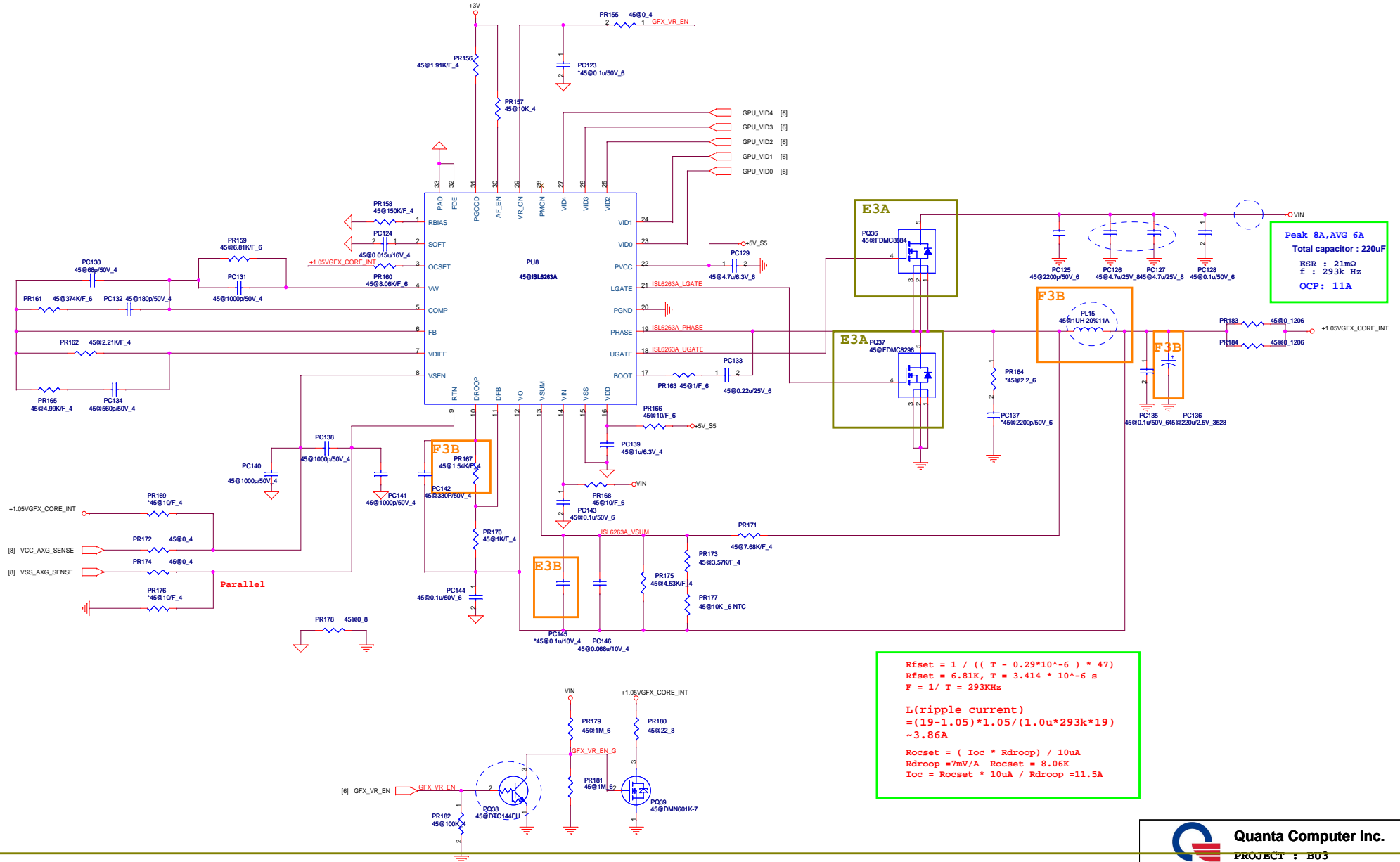



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PROJECT : BU3


Size	Document Number	Rev
	VCCP 1.05V(UP6111AQDD)	D3B

Date:	Monday, August 10, 2009	Sheet	29	of	34
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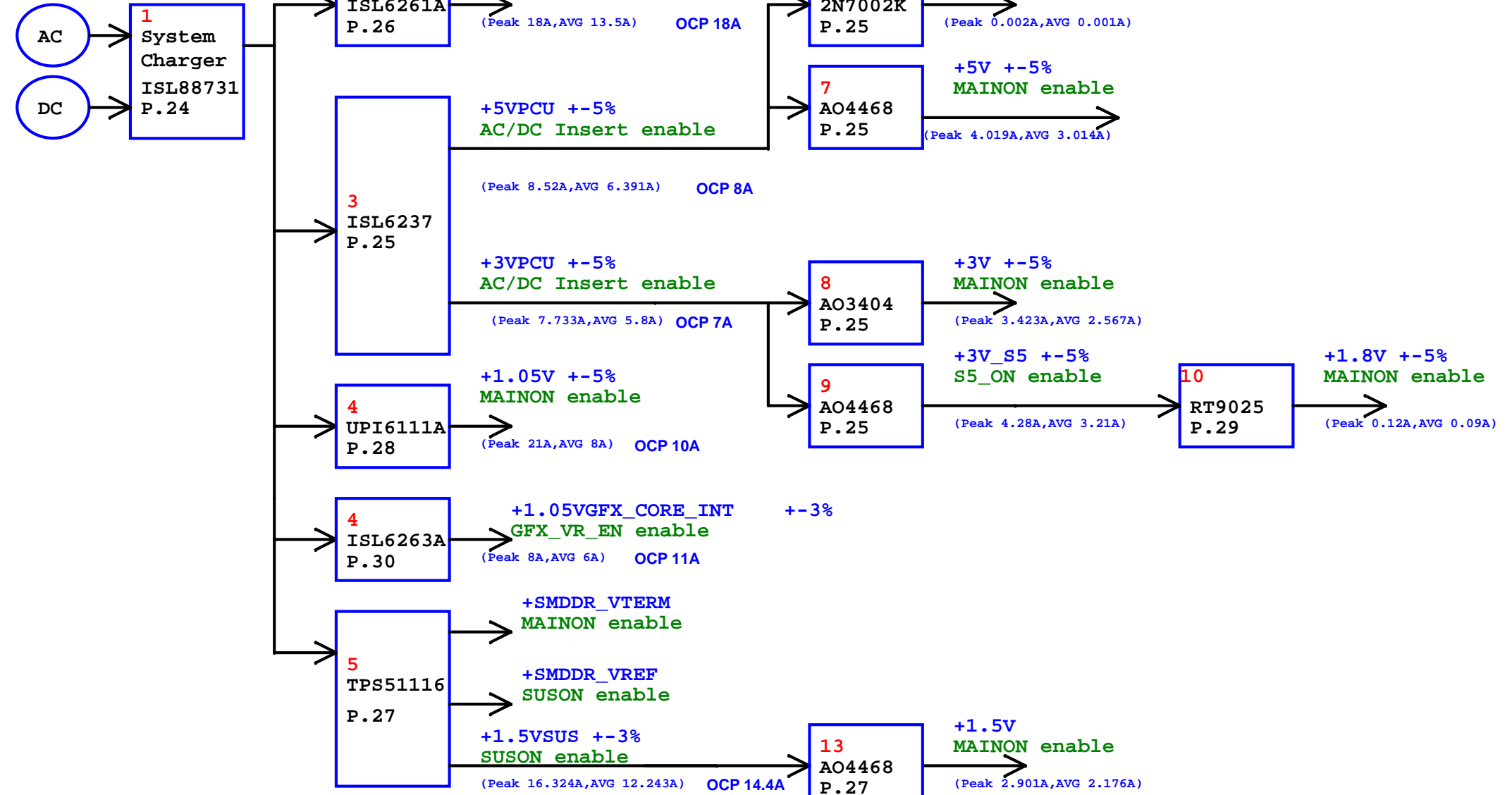
E3A



 Quanta Computer Inc. PROJECT : BU3		
Size	Document Number Discharge/1.5/2.5V	Rev D3B
Date:	Monday, August 10, 2009	Sheet 31 of 34

Model		REV	MODEL			BU3		
			PAGE	FROM	To			
BU3 MB	D3A	PAGE 26: Add PR146,PR147,PR148 value 0_4 ,PR149 value 10K/F_4 for power suggest	1	1A	1B			
		PAGE 22: Add D22 for ESD/EOS suggestion - Power pin EOS	2	1A	1B			
		PAGE 22: C386,C382,RP21不上件	3	1A	1B			
		PAGE 02: change C373,C374 value to 33p/50V_4 for XTAL report	4	1A	1B			
		PAGE 20: reserve Q31,R381,R380,C383,C384,C385	5	1A	1B			
	E3A	PAGE 17: reserve CRT FILTER R390,R393,R394,C398,C399,C400,C401,C402,C403 for EMI requirement.	6	1A	1B			
		PAGE 21: add C390,C391,C392,C393,C394,C395,C396,C397 for EMI requirement .	7	1A	1B			
		PAGE 30: add 1.05v GFX SCHEMATIC for reader stand by function (GS45 only)	8	1A	1B			
		PAGE 28: change PQ8 and PQ9 value and footprint .	9	1A	1B			
		PAGE 17: Add R3,R2 BOI-OPTION for GS40.	10	1A	1B			
	F3A	PAGE 17: Add R392 ,R391 for Board ID3	11	1A	1B			
		PAGE 21: Add HOLE 9,HOLE 11, HOLE 10.	12	1A	1B			
		PAGE (12) :Change R244 to bead 120ohm, C324 to 22PF for EMI requirement.	13	1A	1B			
		PAGE (24) : Add PR88, PR35 for Adapter Voltage monitor	14	1A	1B			
		PAGE (17) : Reserve U25 for LVDS_VADJ option (support XP function key).	15	1A	1B			
		PAGE (25) : Reserve PC147,PC148,PC149,PC150,PC151,PC152 for power soft start	16	1A	1B			
		PAGE (21) : Change CN9 connector pin define to 40 pin	17	1A	1B			
		PAGE (17) : Change D1 footprint	18	1A	1B			
		PAGE (18) : Change HDMI CN11 connector PIN DEFINE	19	1A	1B			
		PAGE (22) : R176,RP7,RP8,L2,R138,R161,R377,R199,R251,R351,R213,R225,R211,R373,R357,R240,R212,R217,R175,R342,R155,R48,R59,R112,R111,R130,R131,R288,R284,R62,R91,R41,R134 replace by short pad	20	1A	1B			
		PAGE (22) : R378,R68,R279,R12,RP17,RP15,RP16,RP14,RP13,RP12,RP11,RP10,RP9,R293,R8 replace by short pad	21	1A	1B			
		PAGE (22) : Change CN9 pin define. 40PINS	22	1A	1B			
		PAGE (30) : Change PL15 from 2.2uH to 1uH , PC145 change to unmounted , PR167 change to 1.54K , PC136 should be mounted for 3D hang up issue.	23	1A	1B			
		PAGE (09) : reserve C186,C149,C269,C247,C113,C342,C154,C135 for cost down	24	1A	1B			
			25	1A	1B			
			26	1A	1B			
			27	1A	1B			
			28	1A	1B			
			29	1A	1B			
			30	1A	1B			
DOC NO. 204		PROJECT MODEL :	BU3	APPROVED BY:	Mosy Li	DATE:	2009/04/27	 Quanta Computer Inc. PROJECT : BU3
		PART NUMBER:	31BU3MB0000	DRAWING BY:	Mosy Li	REVISION:	1B	
Date: Monday, August 10, 2009								Sheet 32 of 33

Power Tree Table



Quanta Computer Inc.
PROJECT : BU3

Size	Document Number	Rev
		D3B
Power Tree Table		
Date:	Monday, August 10, 2009	Sheet 34 of 34