

***NDU00/NDU10***

***Streamline-S 11.6"***

***Streamline-M 13.3"***

# LA-6031P REV 1.0 Schematic

Intel Arrandale SFF/IBEX PEAK

2010-04-12 Rev 1.0

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# Compal Confidential

Model Name :NDU00/NDU10

File Name : LA-6031P

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Mobile

Arrandale CPU  
BGA 1288pins

Memory BUS(DDRIII)  
Dual Channel

200pin DDRIII-SO-DIMM X2  
BANK 0, 1, 2, 3

Clock Generator  
SLG8SP587VTR  
page 12

1.5V DDRIII 800/1066 MT/s

page 5, 6, 7, 8, 9

FDI X8  
2.7GHz

DMI X4  
2.5GHz

USB/B  
USB port 0,1  
page 30

BT conn  
USB port 5  
page 25

3G  
USB port 12  
page 26

Int. Camera  
USB port 11  
page 12

LCD Conn.  
page 12

LVDS-A

CRT (Sub-board)  
page 13

RGB

HDMI Conn.  
page 14

HDMI Level Shifter  
page 14

DDP-C

3G  
PCIe port 4  
page 26

PCIe 1x

RJ45+Transformer (Sub-board)  
page 27

RTL8105E 10/100M  
PCIe port 1  
page 27

PCIe 1x

Cardreader conn.  
page 28

CardReader JMB389  
PCIe port 5  
page 28

PCIe 1x

Intel Ibex Peak

FCBGA1071

page 15~23

USB  
5V 480MHz

USB  
5V 480MHz

PCIe 1x  
1.5V 2.5GHz(250MB/s)

SATA port 1  
5V 3GHz(300MB/s)

SATA port 5  
5V 3GHz(300MB/s)

USB port 3  
5V 480MHz

PCIeMini Card  
WiMax  
USB port 13  
page 26

PCIeMini Card  
WLAN  
PCIe port 2  
page 26

SATA HDD0  
page 24

eSATA  
page 24

USB  
USB port 3  
page 24

SPI

LPC BUS  
3.3V 33 MHz

HD Audio  
3.3V/1.5V 24MHz

Power/B  
page 33

RTC CKT.  
page 15

DC/DC Interface CKT.  
page 34

Power Circuit DC/DC  
page 37~43

SPI ROM  
page 15

Debug Port  
page 32

ENE KB926 E0  
page 31

Touch Pad  
page 33

Int.KBD  
page 25

EC ROM  
page 32

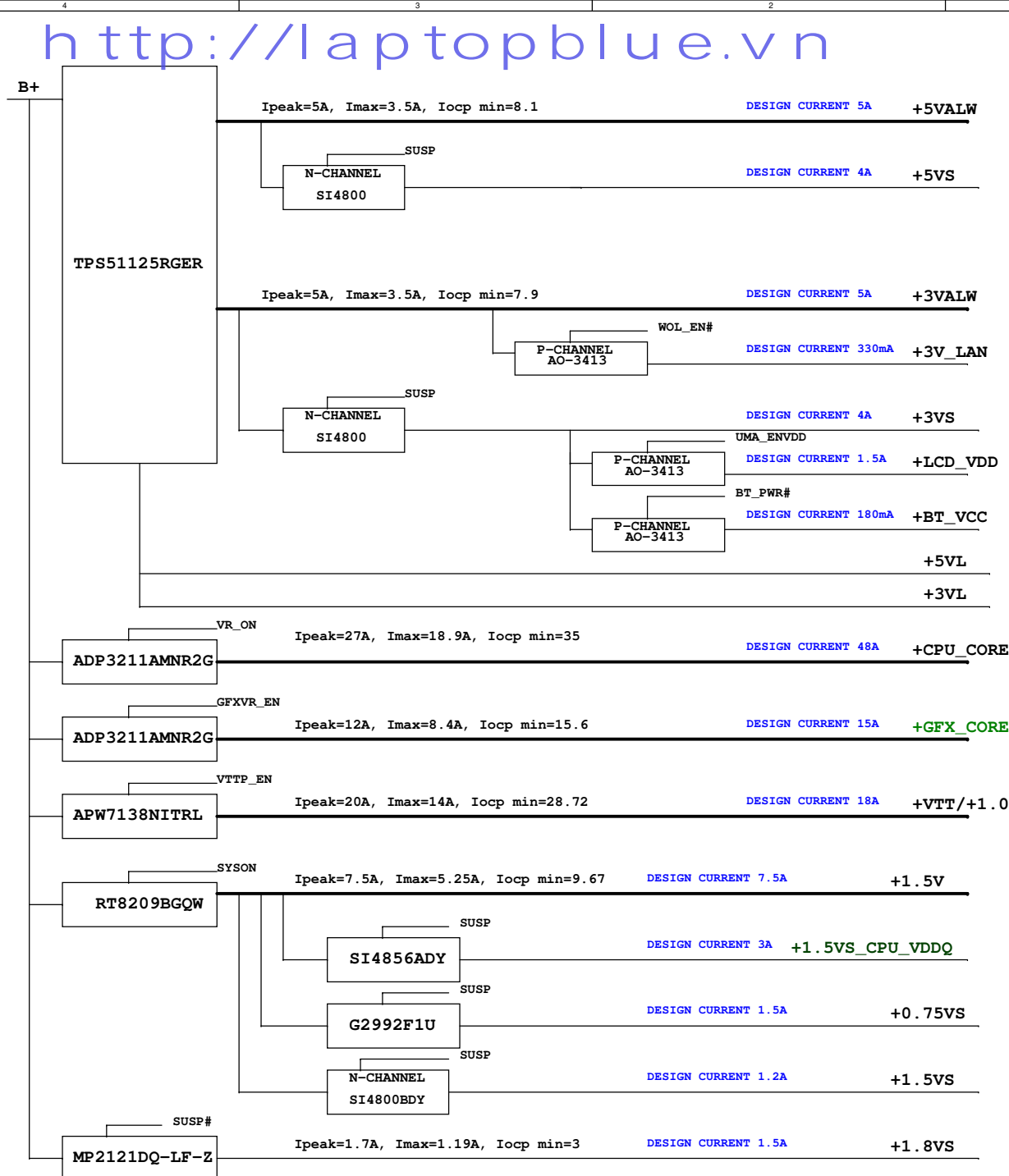
HDA Codec  
ALC259  
page 29

Audio sub-board  
page 30

SPK CONN  
page 30

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NSWAA Liverpool Intel Arrandale  
NTWAA Sunderland Intel Arrandale



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Voltage Rails

( O MEANS ON X MEANS OFF )

BTO Option Table

<div>power plane</div> <div>State</div>	+RTCVCC	+B +5VL +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +GFX_CORE +CPU_CORE +VTT +0.75VS +1.8VS +1.5VS_CPU_VDDQ
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

Function	Bluetooth	HDMI	3G	Mini Card	Mini Card	Gensor	
explain	Bluetooth	HDMI	3G	WIRELESS	WIMAX	main	2nd
						R5F211B4D31SP	R5F211B4D34SP
BTO	BT@	IHDMI@	3G@	WLAN@	WIMAX@	GSENSOR@ 1STGSENSOR@ 1ST@	GSENSOR@ 2NDGSENSOR@ 2ND@

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

EC SM Bus1 address

EC SM Bus2 address

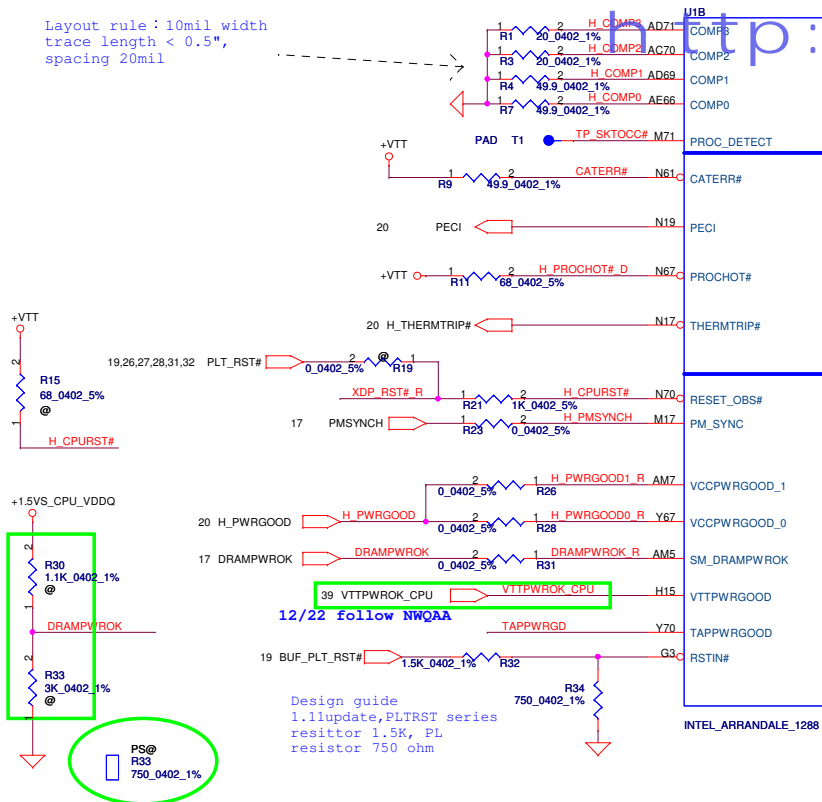
Power	Device	Address	Power	Device	Address
+3VL	EC KB926 D3		+3VS	EC KB926 D3	
+3VL	Smart Battery	0001 011x b	+3VS	Gensor	
			+3VS	PCH	0100 110x b

PCH SM Bus address

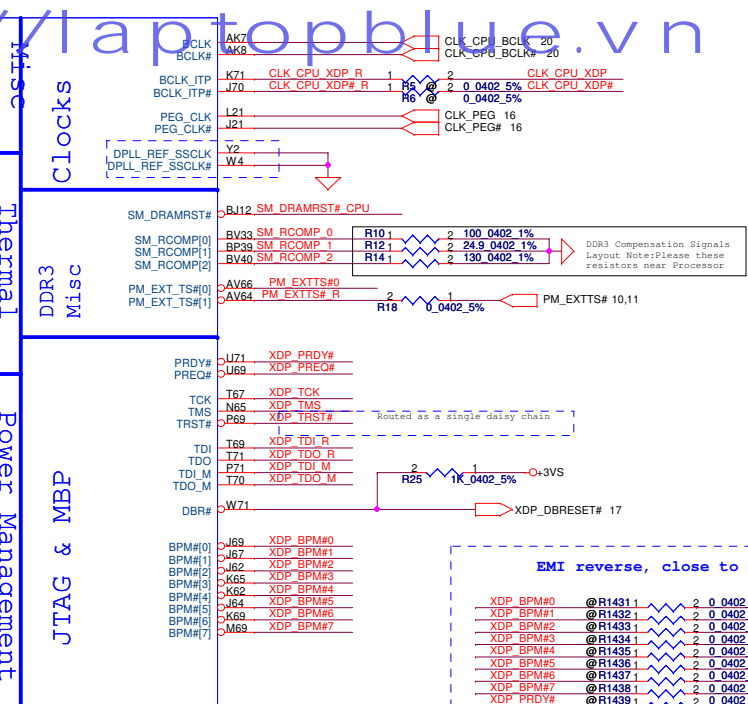
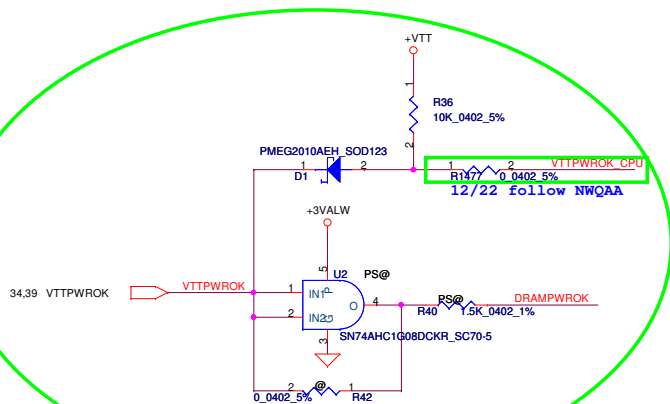
Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMM0	1001 000x b
+3VS	DDR DIMM1	1001 010x b
+3VS	WLAN/Wimax/3G	

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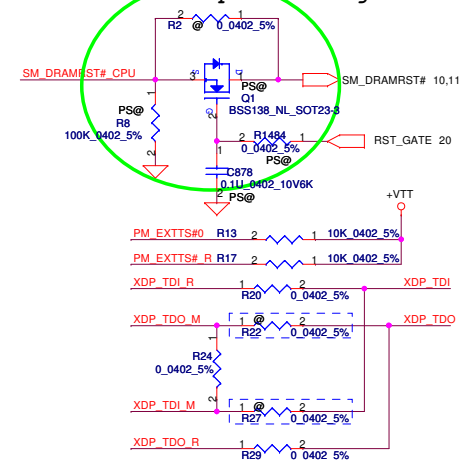
Layout rule: 10mil width  
trace length < 0.5",  
spacing 20mil



For S3 CPU power saving



For S3 CPU power saving



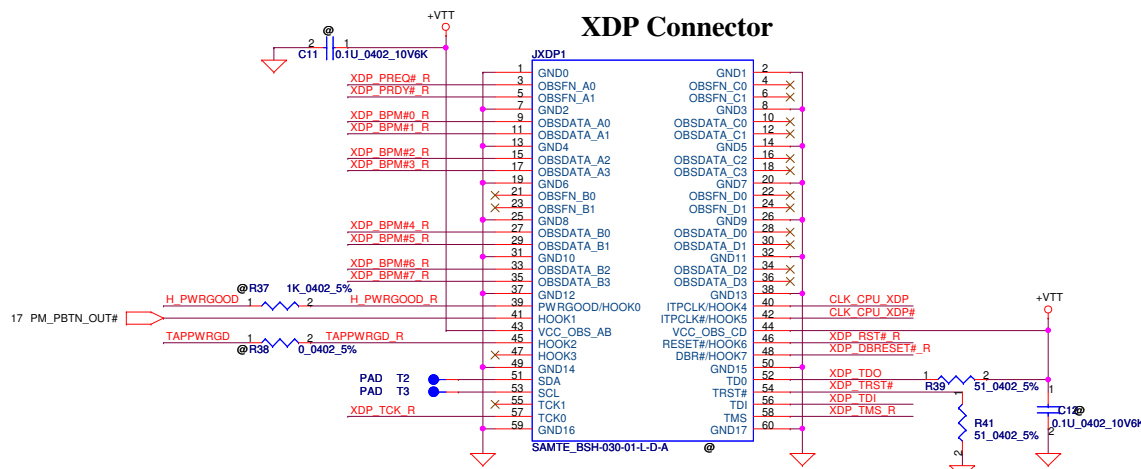
JTAG MAPPING

Scan Chain (Default)	STUFF -> R20, R23, R27 NO STUFF -> R21, R26
CPU Only	STUFF -> R20, R21 NO STUFF -> R23, R26, R27
GMCH Only	STUFF -> R26, R27 NO STUFF -> R20, R21, R23

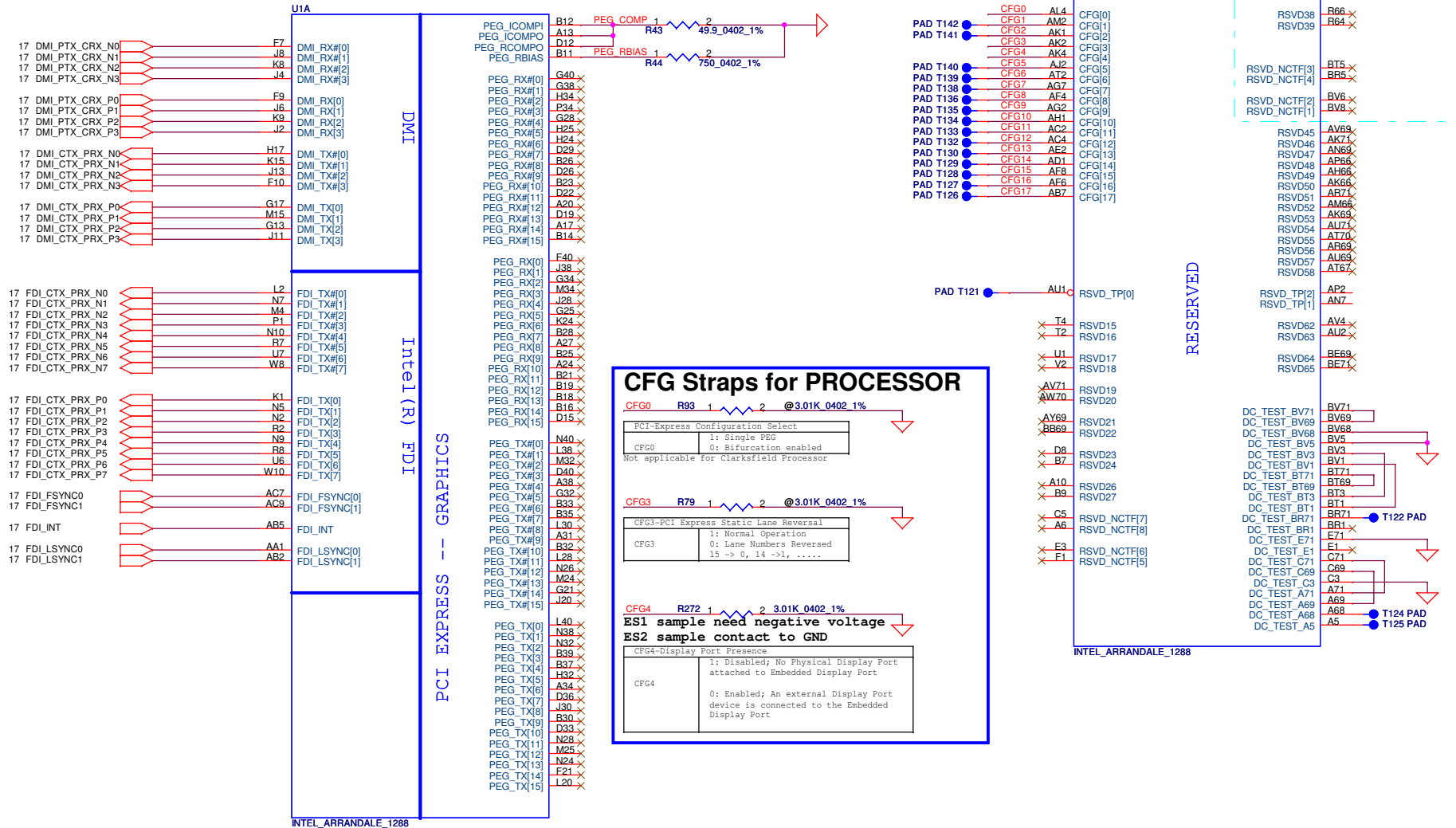
EMI reverse, close to CPU

XDP BPM#0	@ R1431	2	0.0402 5%	XDP BPM#0 R
XDP BPM#1	@ R1432	2	0.0402 5%	XDP BPM#1 R
XDP BPM#2	@ R1433	2	0.0402 5%	XDP BPM#2 R
XDP BPM#3	@ R1434	2	0.0402 5%	XDP BPM#3 R
XDP BPM#4	@ R1435	2	0.0402 5%	XDP BPM#4 R
XDP BPM#5	@ R1436	2	0.0402 5%	XDP BPM#5 R
XDP BPM#6	@ R1437	2	0.0402 5%	XDP BPM#6 R
XDP BPM#7	@ R1438	2	0.0402 5%	XDP BPM#7 R
XDP PRDY#	@ R1439	2	0.0402 5%	XDP PRDY# R
XDP PREQ#	@ R1440	2	0.0402 5%	XDP PREQ# R
XDP TCK	@ R1441	2	0.0402 5%	XDP TCK R
XDP TMS	@ R1442	2	0.0402 5%	XDP TMS R
XDP DBRESET#	@ R1443	2	0.0402 5%	XDP DBRESET# R

XDP Connector

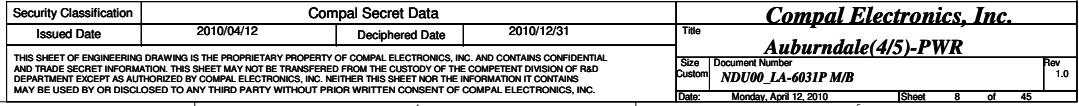


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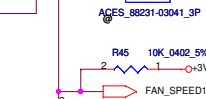
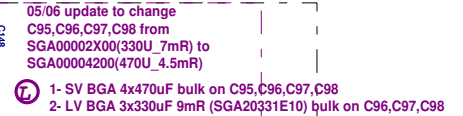




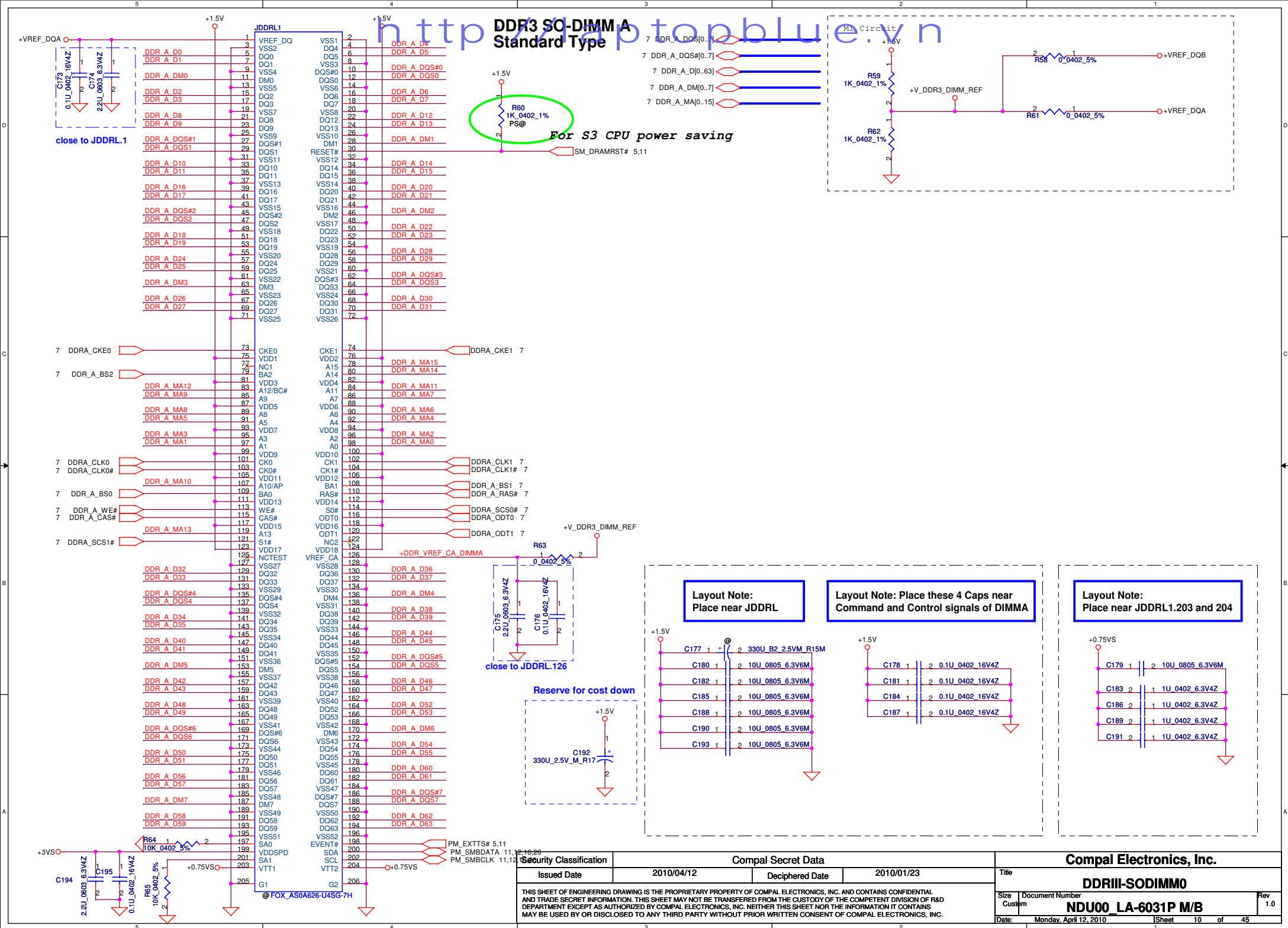








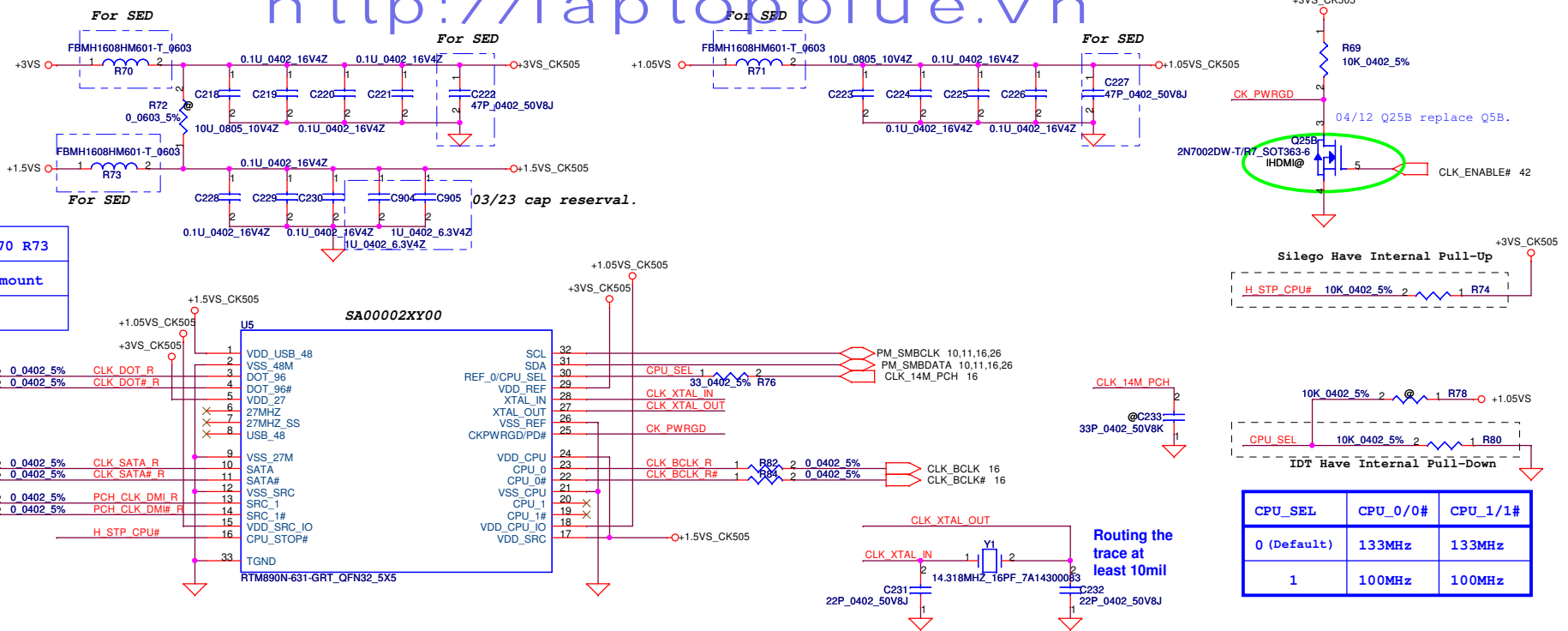
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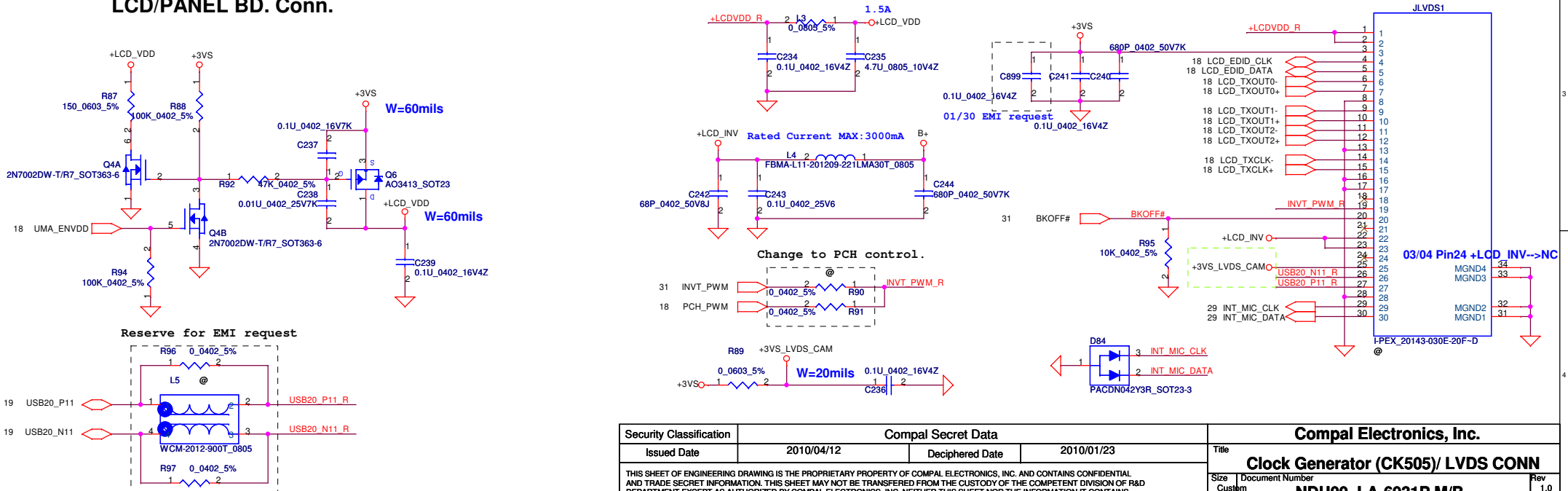


## Clock Generator

<http://laptopblue.vn>



**LCD/PANEL BD. Conn.**

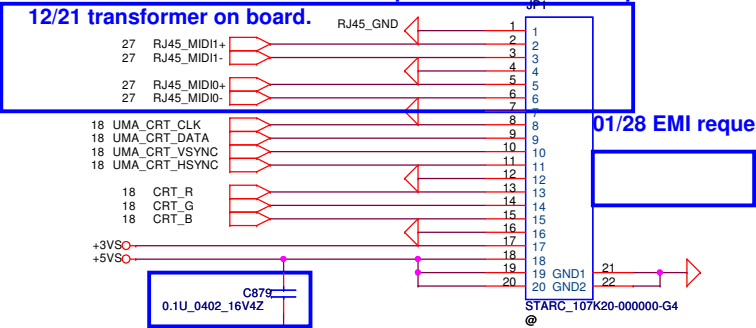


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Issued Date	2010/04/12	Deciphered Date	2010/01/23	Title <b>Clock Generator (CK505)/ LVDS CONN</b>		
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CRT CONNECTOR

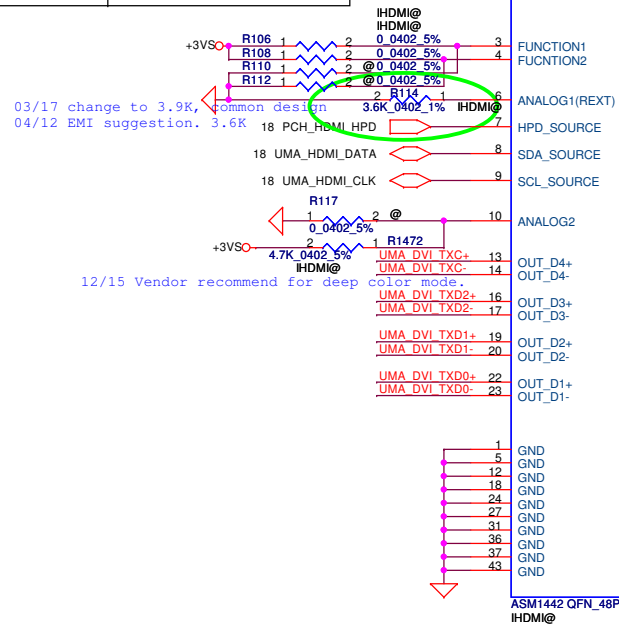
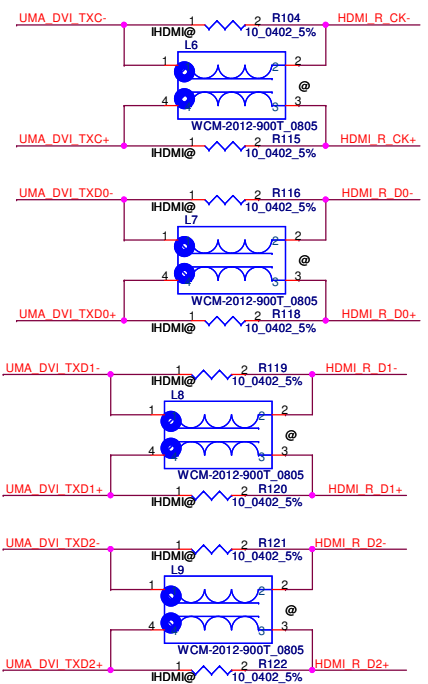
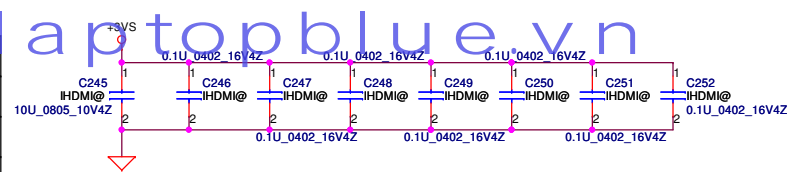
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12/14 Fine tune pin define JP1 Pin1 Pin2 Pin8-->GND  
12/21 pin 2,3 to RJ45\_GND  
12/22 Fine tune JP4 pin define 02/08 update connector footprint.



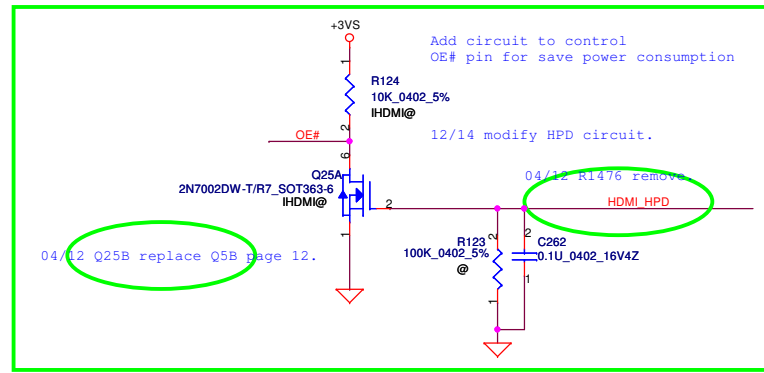
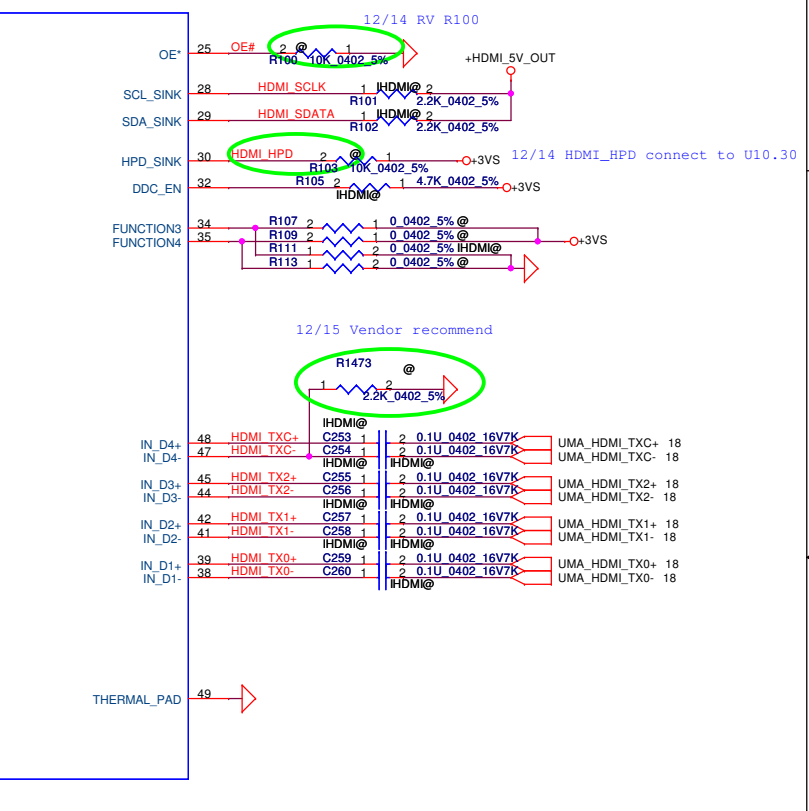
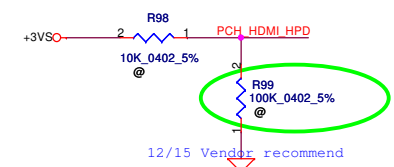
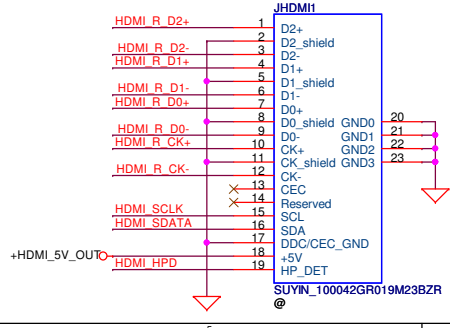
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ANALOG2	Function2	Function1	Swing	Pre-Amp	Slew-rate	Note
Low	Low	Low	450	0	0	
Low	Low	High	420	0	-3dB	Shortest trace
Low	High	Low	450	0	-3dB	Shortest trace
Low	High	High	460	0	-4dB	Streamline PVT2 setting
High	Low	Low	340	0	0	Longest Trace
High	High	Low	400	2dB	0	Longest Trace
High	High	High	420	0	0	



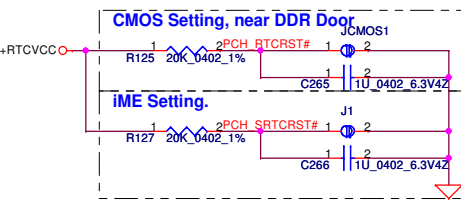
# HDMI Connector

<01/27 update HDMI Connector >



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**Integrated SUS 1.05V VRM Enable**

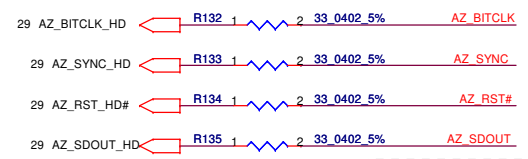
PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)
--------------	---

**HDA\_SYNC**  
This signal has a weak internal pull down.  
H=>On Die PLL is supplied by 1.5V  
L=>On Die PLL is supplied by 1.8V

**HDA\_SDO**  
This signal has a weak internal pull down.  
This signal can't PU

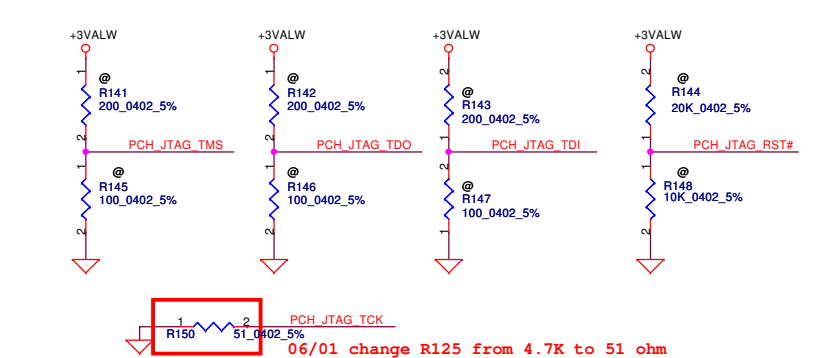
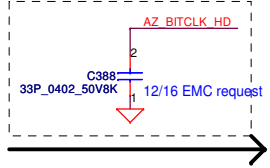
**Flash Descriptor Security Override**

HDA_DOCK_EN#	Low = Enabled High = Disabled *
--------------	------------------------------------



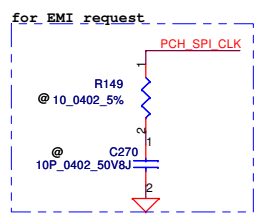
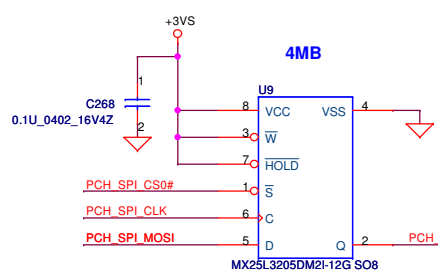
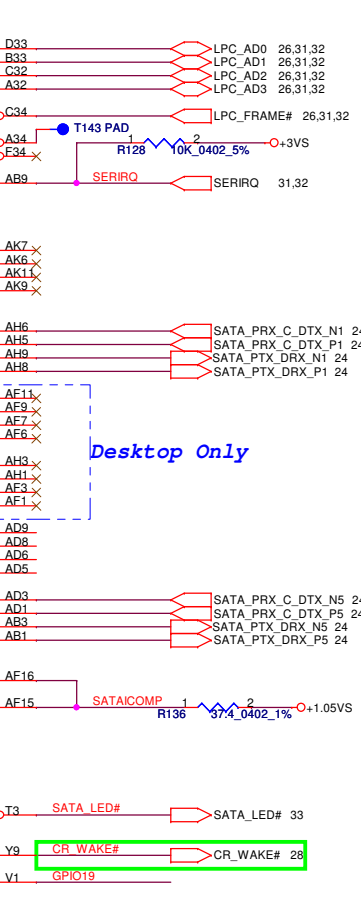
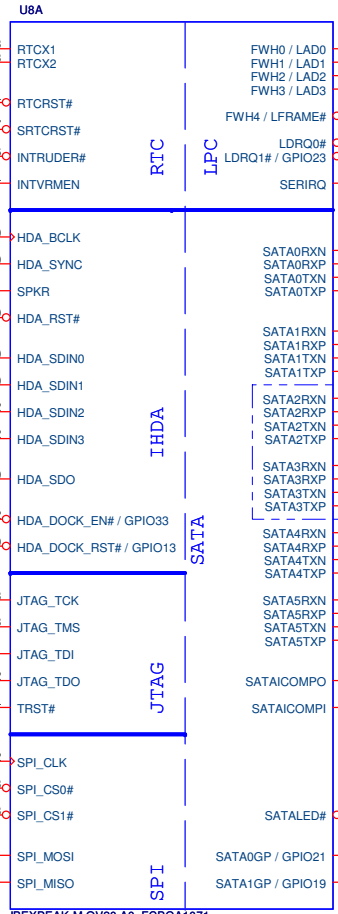
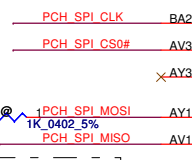
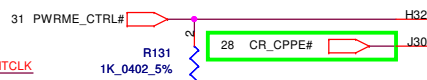
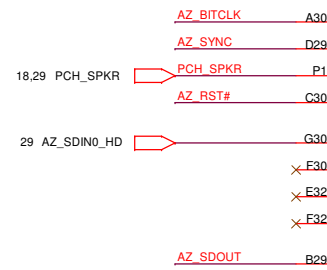
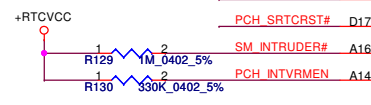
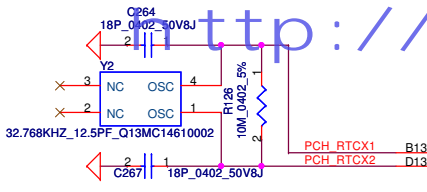
**ITPM Enabled Internal: Pull down 20k**

SPI_MOSI	High = Enabled Low = Disabled (Default)
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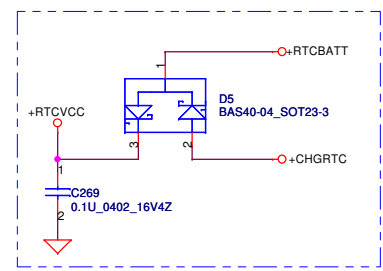
PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TCK	R356	200ohm	200ohm	20Kohm	No Install
PCH_JTAG_RST#	R517	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install
PCH_JTAG_RST#	R353	10Kohm	10Kohm	No Install	No Install

06/01 change R125 from 4.7K to 51 ohm



1ST HDD

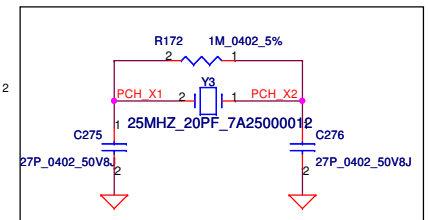
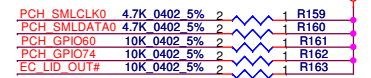
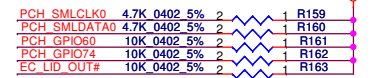
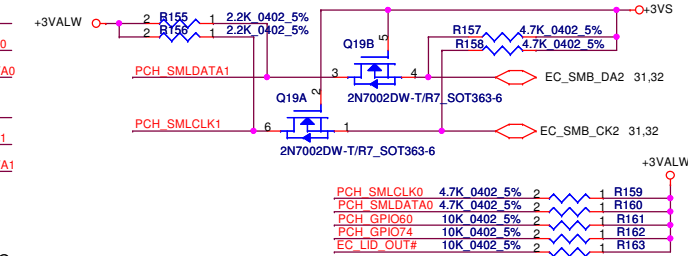
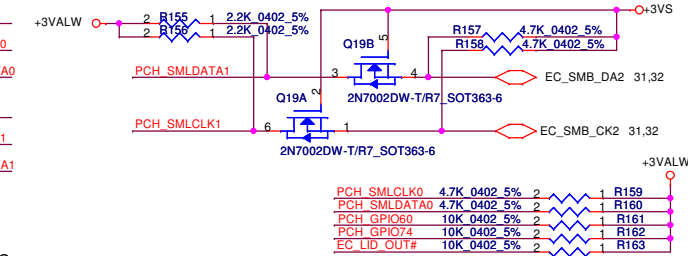
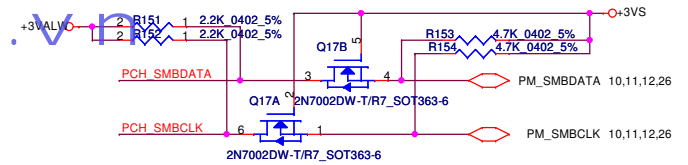
eSATA



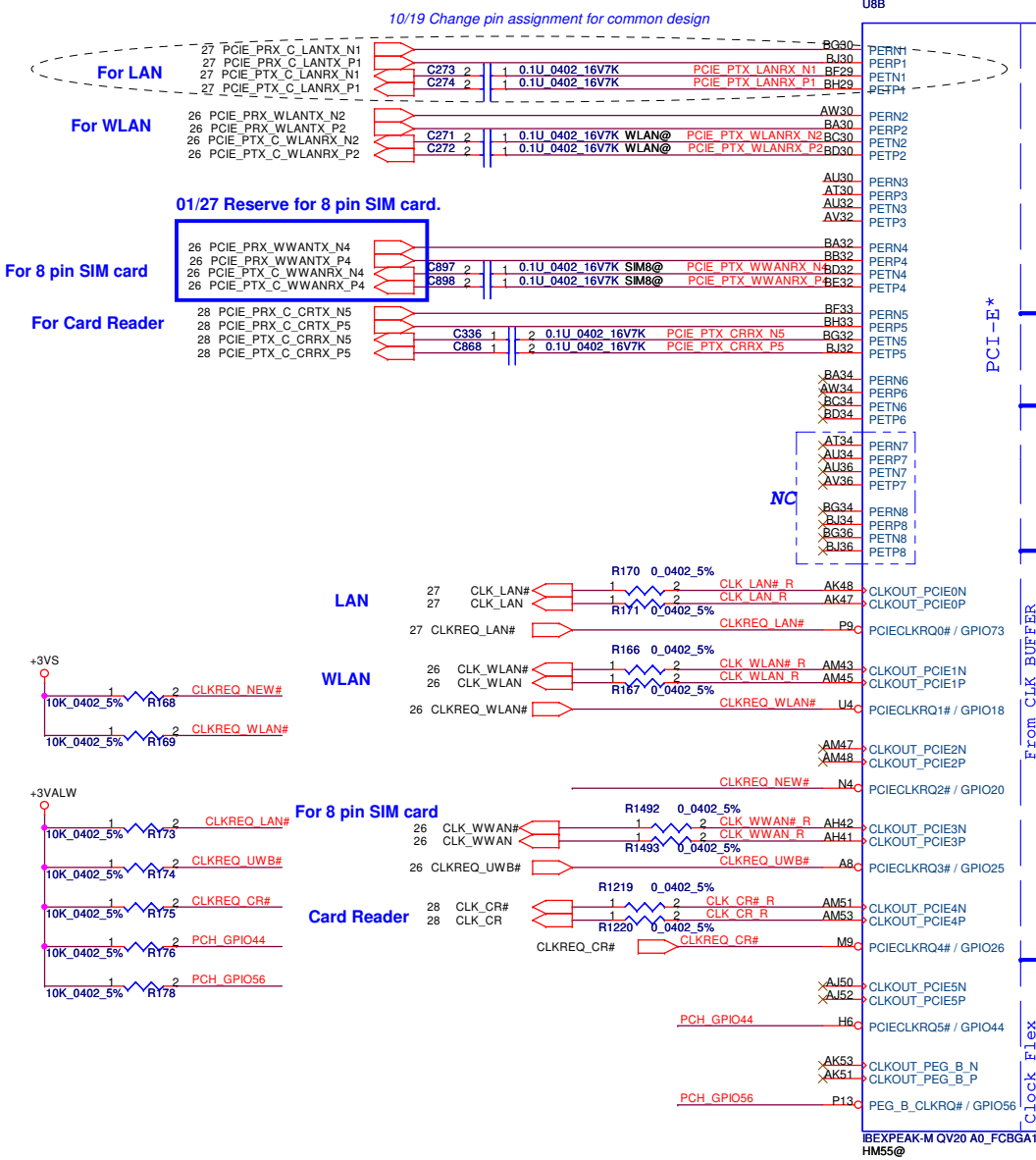
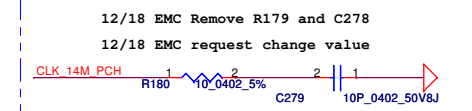
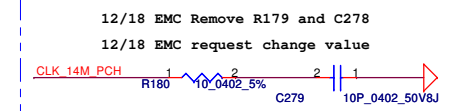
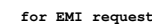
2/8 change back to original.(Lion Wang)  
del D86 and R1494.  
2/1 Add R1494 D86 (EMI)



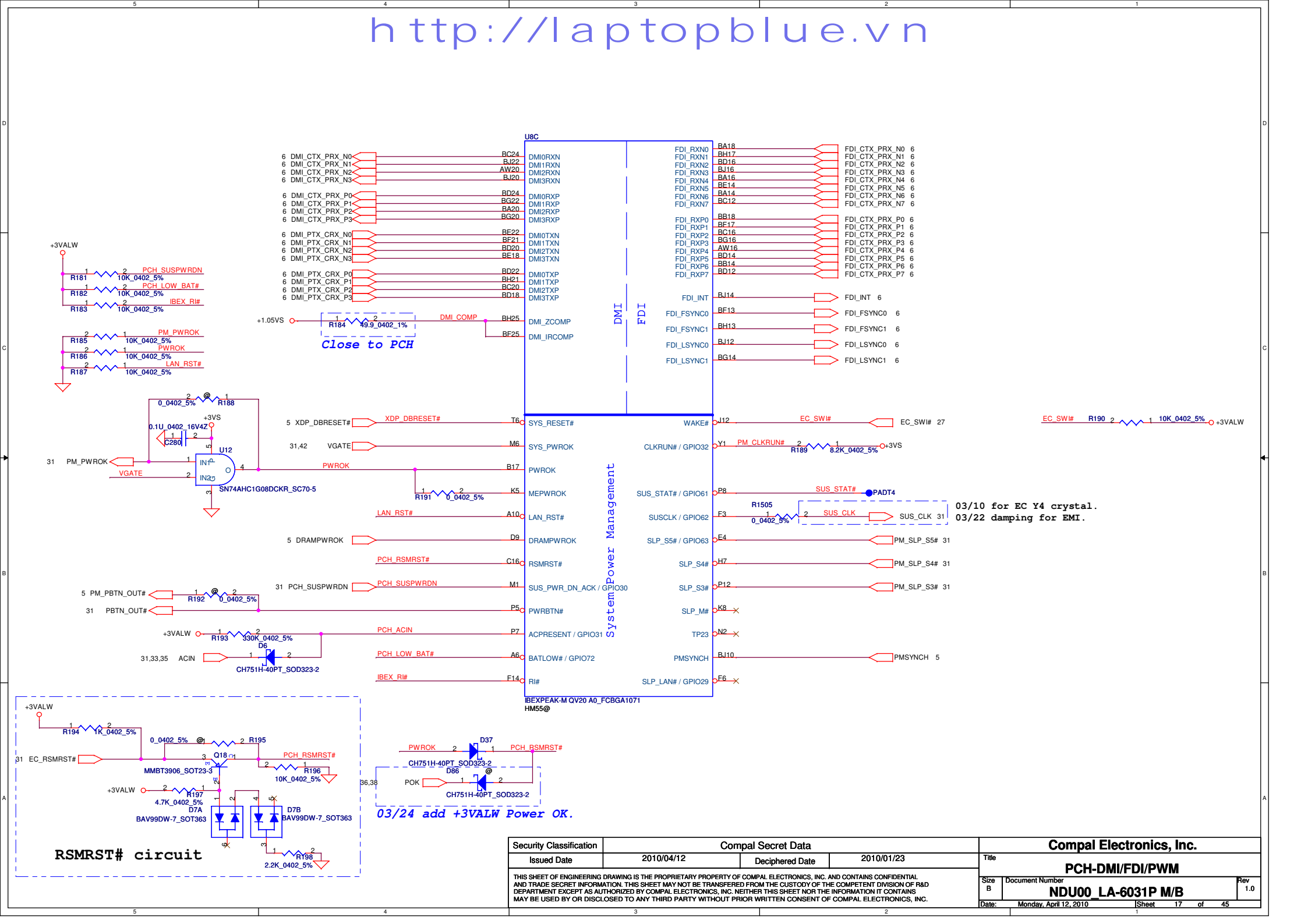
The schematic diagram illustrates the PM\_SMB interface circuit. A 3V3 supply is connected to a network of resistors (R151, R152, R153, R154) and two NPN transistors (Q17A, Q17B) from the 2N7002DW-T/R7\_SOT363-6 package. The input signals PCH\_SMBDATA and PCH\_SMBCLK are connected to the base of Q17A. The output signals PM\_SMBDATA and PM\_SMBCLK are connected to the collector of Q17B. The emitters of both transistors are connected to ground.

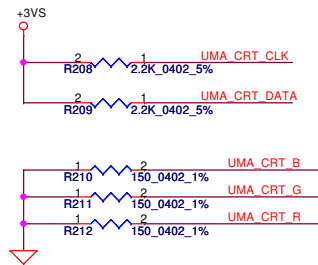
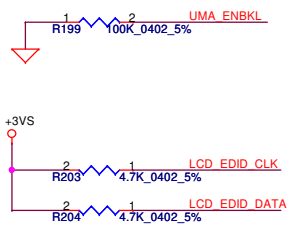


**Note:** Stuff 0 ohm if 25MHz crystal un-stuff

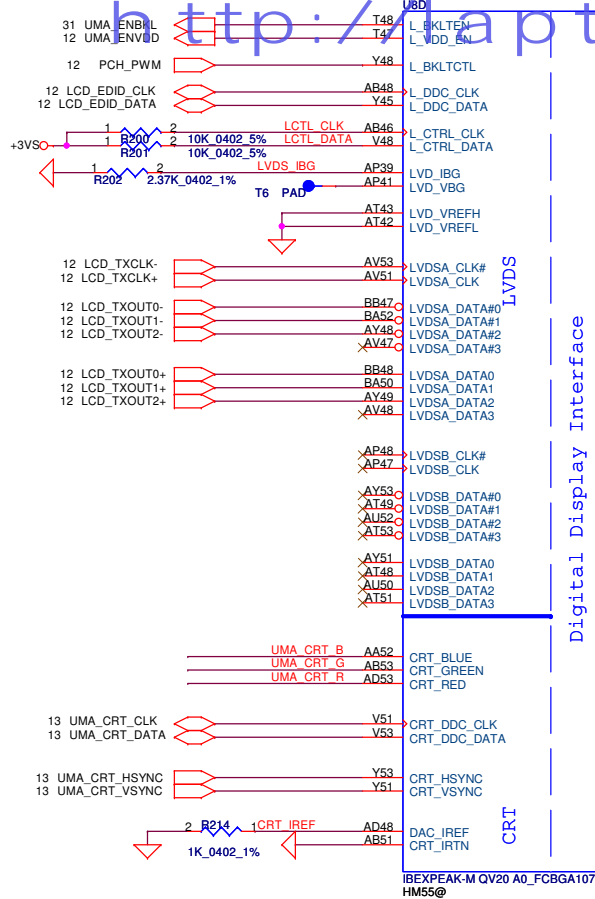
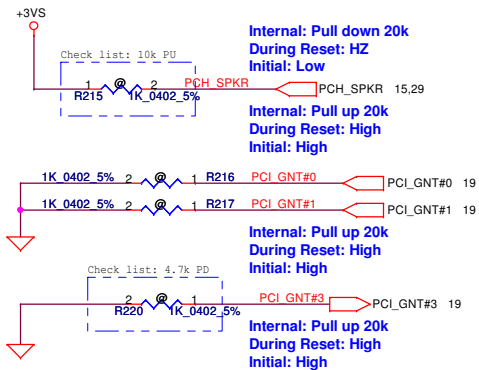


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				Size B	Document Number	Rev 1.0
				NDU00 LA-6031P M/B Date: Monday, April 12, 2010 Sheet 16 of 45		

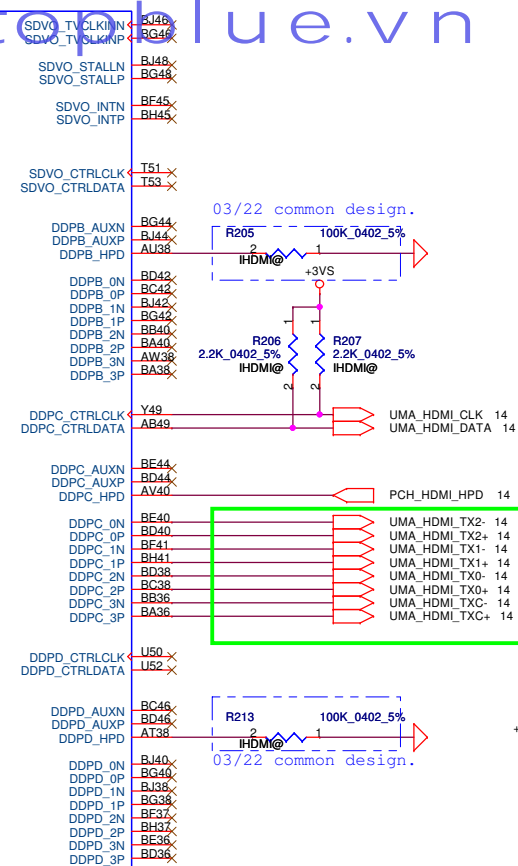
[illegible]



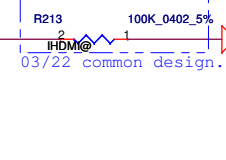
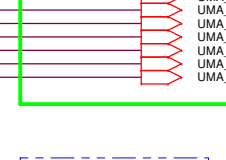
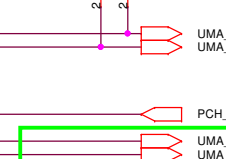
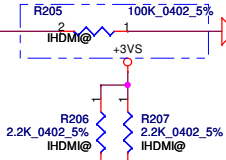
## PCH Strap Pin



## Digital Display Interface

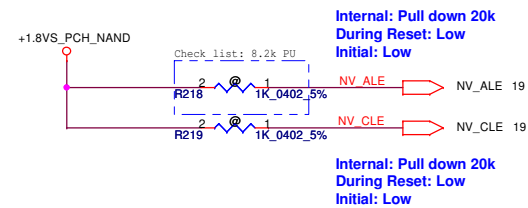


03/22 common design.



## HDMI

Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)



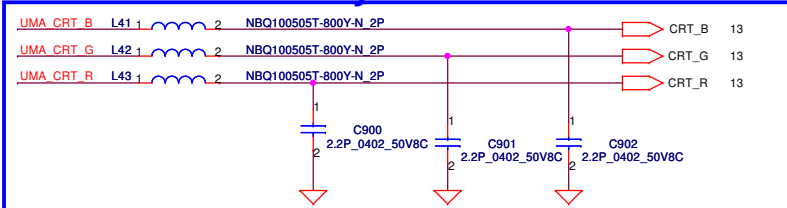
DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc

NO REBOOT Strap	
PCH_SPKR	Low= Disable High= Enable

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

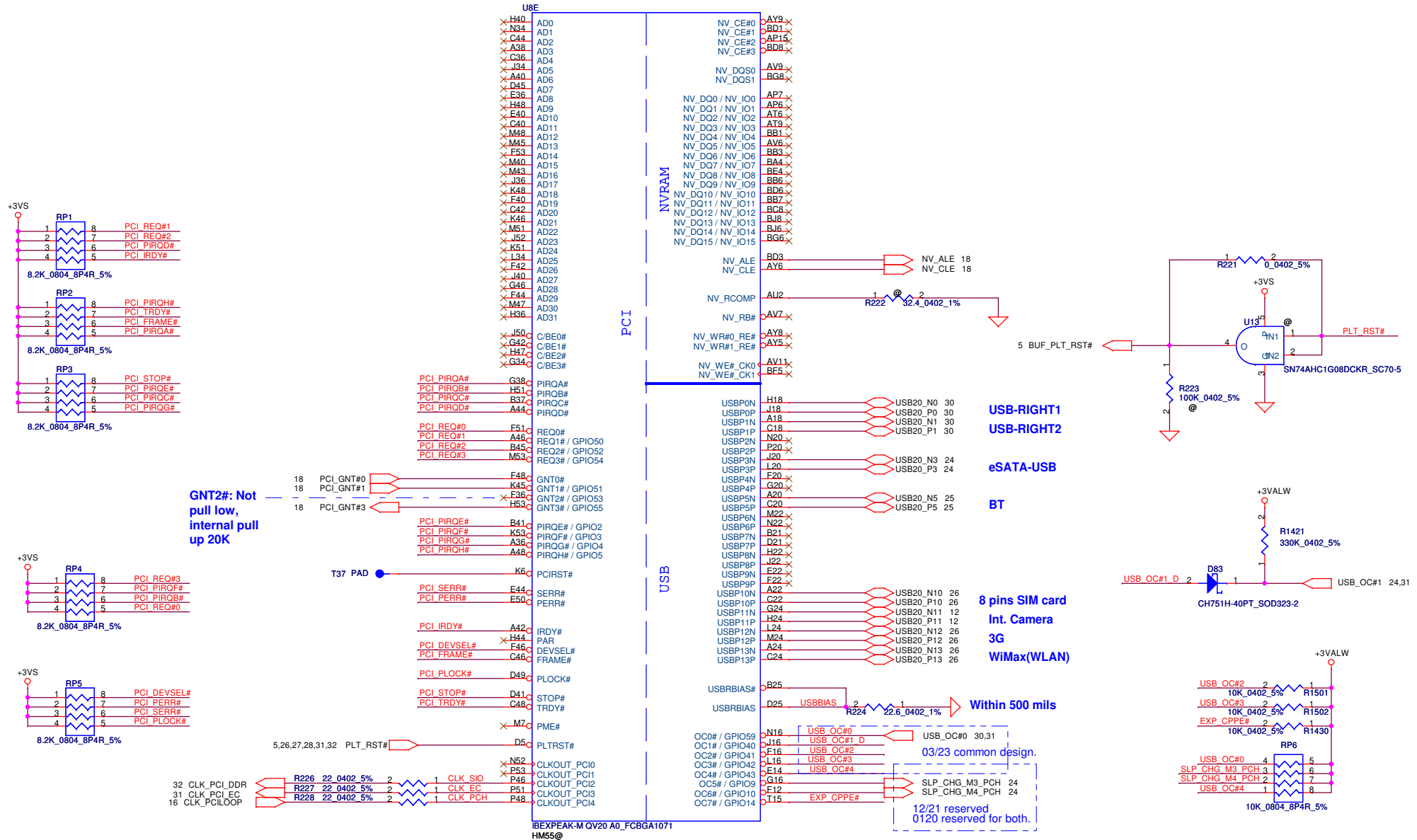
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable

## modify....



2/2 Add L41 L42 L43 C900 C901 C902 for EMI request

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				Date: Monday, April 12, 2010	Sheet 18 of 45

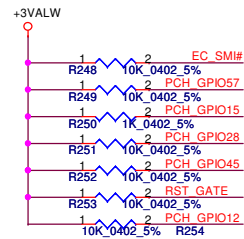
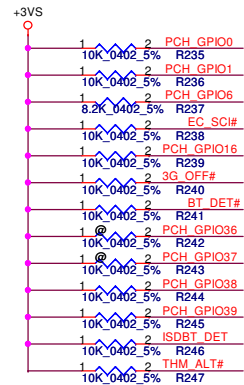


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Size B	Document Number	Rev		1.0	
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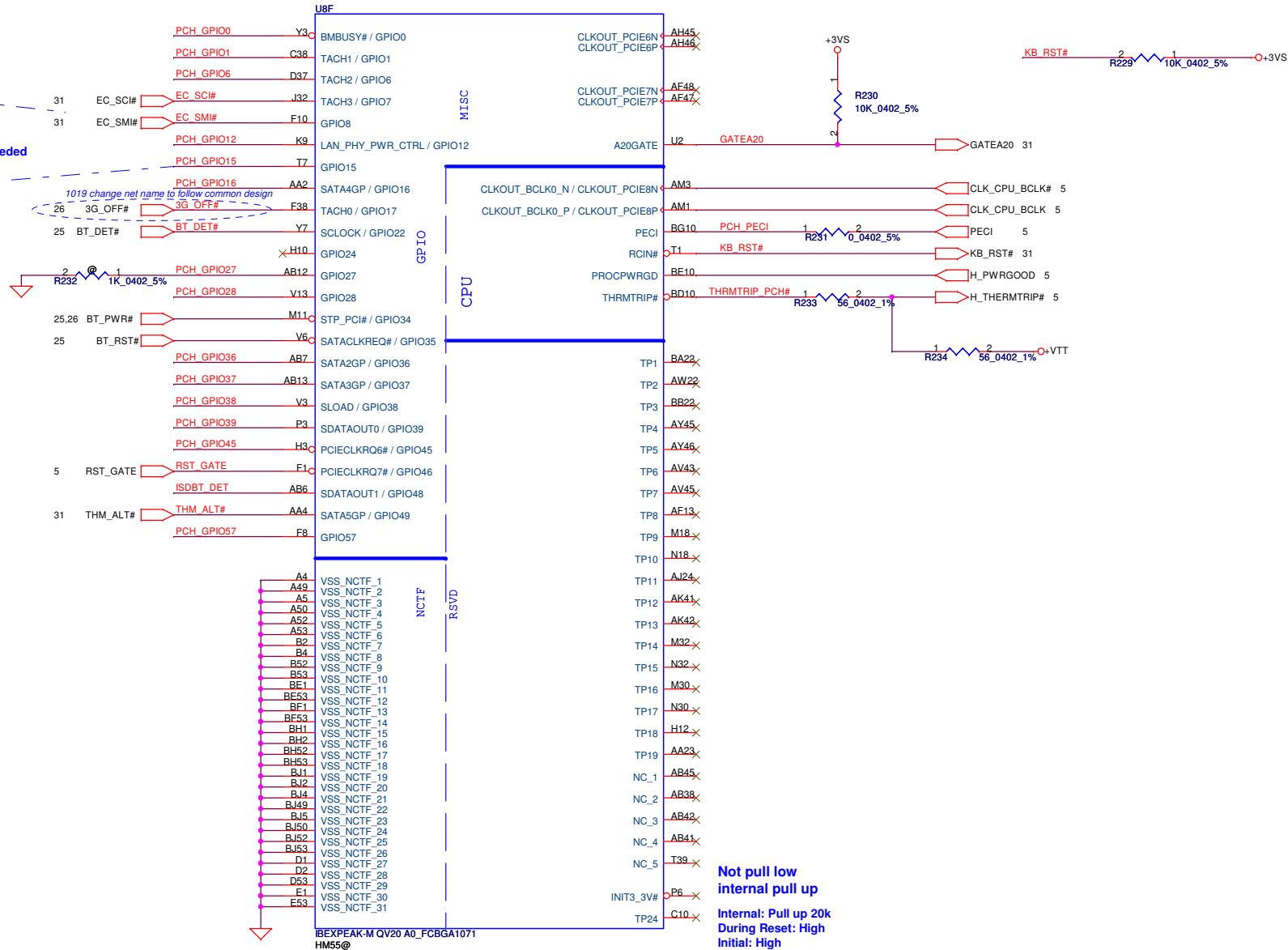
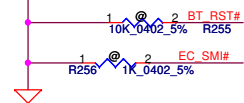
**Internal: Pull up 20k**  
**During Reset: High**  
**Initial: High**

**GPIO15**  
a Strong pull up may be needed  
for GPIO Functionality  
Internal: Pull down 20k  
During Reset: Low  
Initial: Low

PCH_GPIO27	High = Enabled (Default) Low = Disabled
------------	--



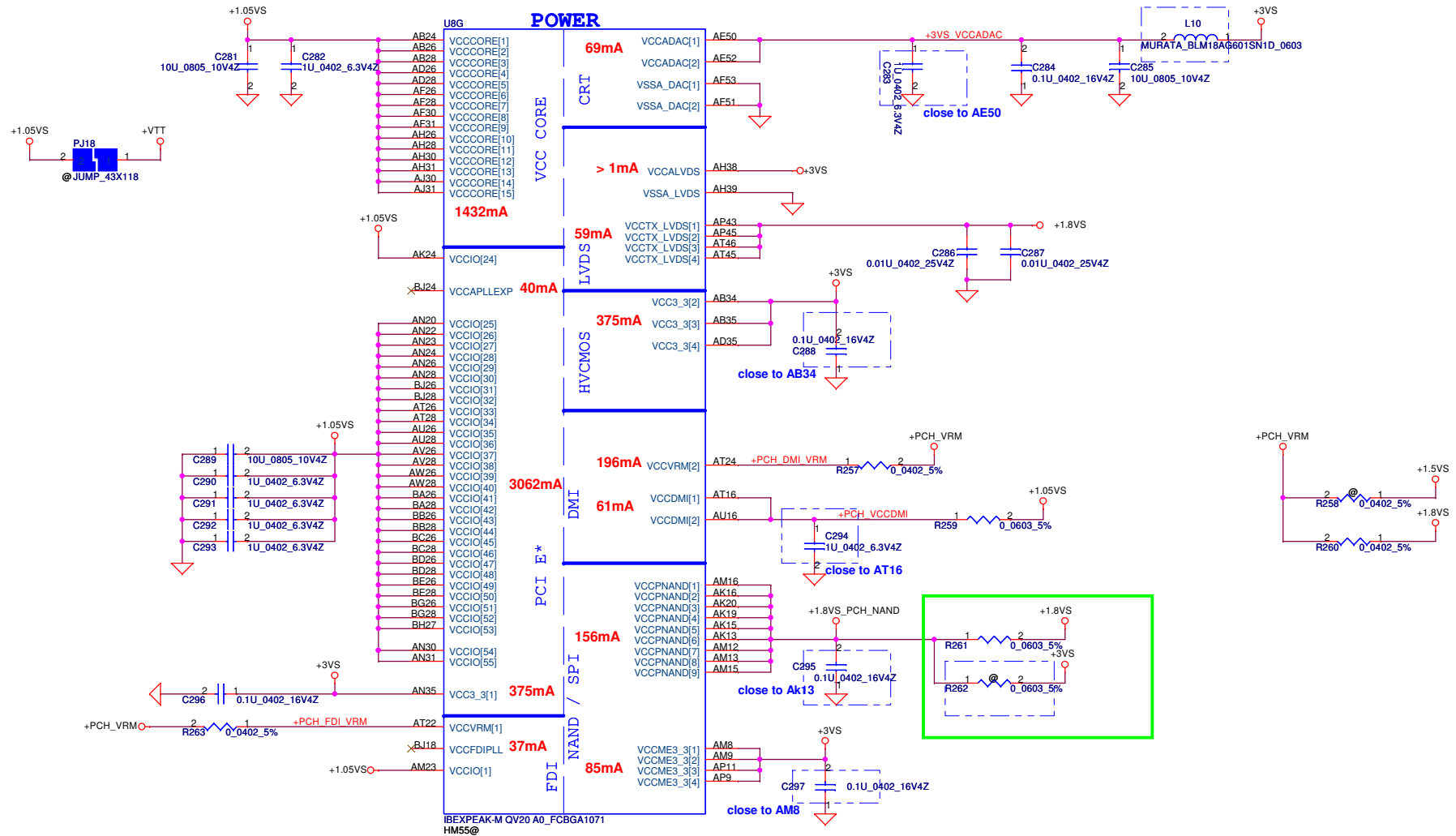
02/08 reserved for project ID.



**Not pull low  
internal pull up**

Internal: Pull up 20  
During Reset: High  
Initial: High

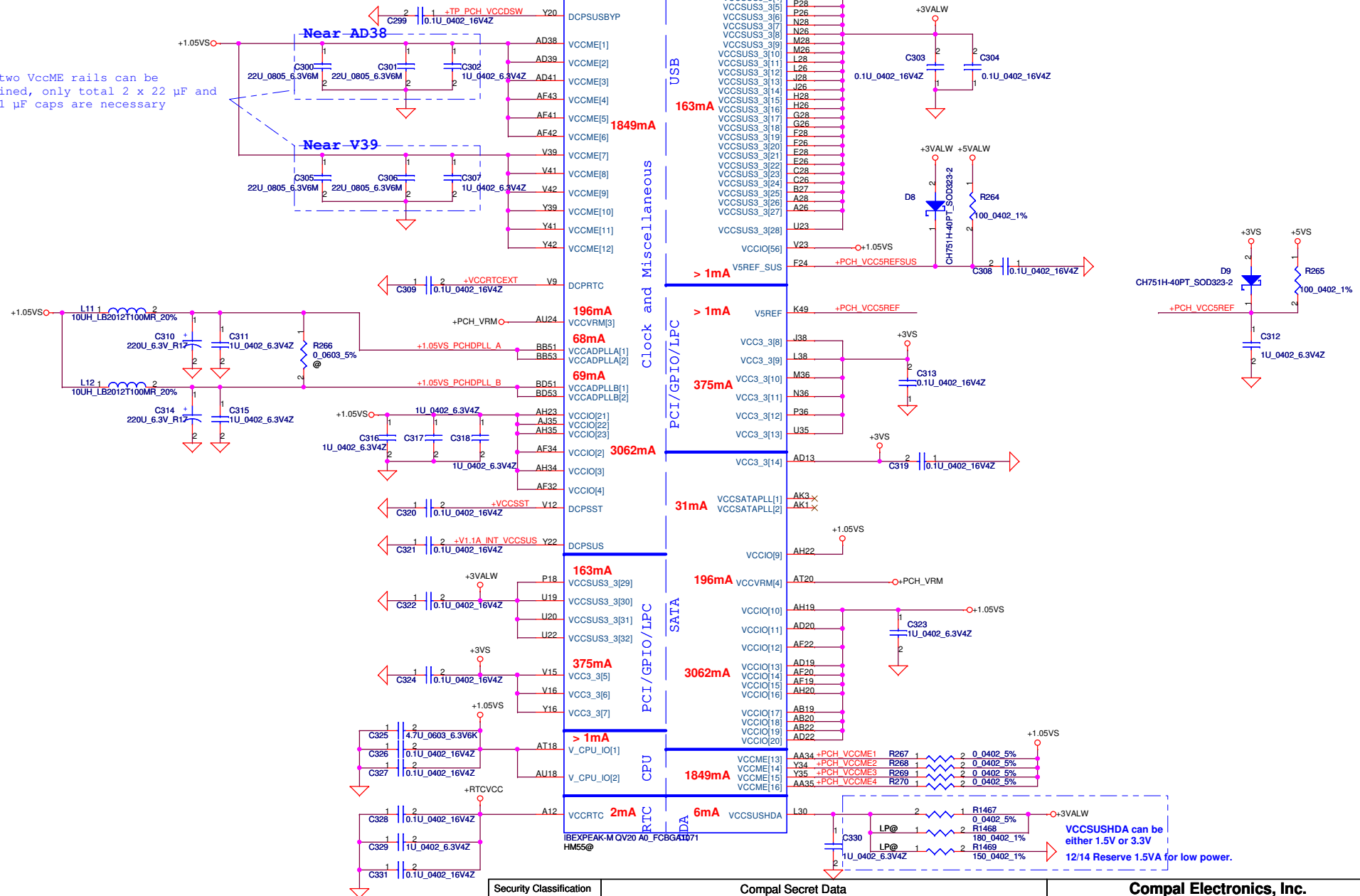
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VccLAN may be grounded if Intel LAN is disabled

If two VccME rails can be combined, only total 2 x 22  $\mu$ F and 2 x 1  $\mu$ F caps are necessary



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UBI

AY7	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L2
B7	VSS[169]	VSS[269]	L22
BC12	VSS[170]	VSS[270]	L32
BB12	VSS[171]	VSS[271]	L36
BB16	VSS[172]	VSS[272]	L40
BB20	VSS[173]	VSS[273]	L52
BB24	VSS[174]	VSS[274]	M12
BB30	VSS[175]	VSS[275]	M16
BB34	VSS[176]	VSS[276]	M20
BB38	VSS[177]	VSS[277]	N38
BB42	VSS[178]	VSS[278]	M34
BB49	VSS[179]	VSS[279]	M38
BB5	VSS[180]	VSS[280]	M42
BC10	VSS[181]	VSS[281]	M46
BC14	VSS[182]	VSS[282]	M49
BC18	VSS[183]	VSS[283]	M5
BC2	VSS[184]	VSS[284]	M8
BC22	VSS[185]	VSS[285]	N24
BC32	VSS[186]	VSS[286]	P11
BC36	VSS[187]	VSS[287]	AD15
BC40	VSS[188]	VSS[288]	P22
BC44	VSS[189]	VSS[289]	P30
BC52	VSS[190]	VSS[290]	P32
BH0	VSS[191]	VSS[291]	P34
BD48	VSS[192]	VSS[292]	P42
BD49	VSS[193]	VSS[293]	P45
BD5	VSS[194]	VSS[294]	P47
BE12	VSS[195]	VSS[295]	R2
BE16	VSS[196]	VSS[296]	R52
BE20	VSS[197]	VSS[297]	T12
BE24	VSS[198]	VSS[298]	T41
BE30	VSS[199]	VSS[299]	T46
BE34	VSS[200]	VSS[300]	T49
BE38	VSS[201]	VSS[301]	T5
BE42	VSS[202]	VSS[302]	T8
BE48	VSS[203]	VSS[303]	U30
BE49	VSS[204]	VSS[304]	U31
BE50	VSS[205]	VSS[305]	U32
BE6	VSS[206]	VSS[306]	U34
BE8	VSS[207]	VSS[307]	P38
BF3	VSS[208]	VSS[308]	V11
BF49	VSS[209]	VSS[309]	P16
BF51	VSS[210]	VSS[310]	V19
BG18	VSS[211]	VSS[311]	V20
BG24	VSS[212]	VSS[312]	V22
BG4	VSS[213]	VSS[313]	V30
BG50	VSS[214]	VSS[314]	V31
BH11	VSS[215]	VSS[315]	V32
BH15	VSS[216]	VSS[316]	V34
BH19	VSS[217]	VSS[317]	V35
BH23	VSS[218]	VSS[318]	V38
BH31	VSS[219]	VSS[319]	V43
BH35	VSS[220]	VSS[320]	V45
BH39	VSS[221]	VSS[321]	V46
BH43	VSS[222]	VSS[322]	V47
BH47	VSS[223]	VSS[323]	V49
BH7	VSS[224]	VSS[324]	V5
C12	VSS[225]	VSS[325]	V7
C50	VSS[226]	VSS[326]	V8
D51	VSS[227]	VSS[327]	W2
E12	VSS[228]	VSS[328]	W52
E16	VSS[229]	VSS[329]	Y11
E20	VSS[230]	VSS[330]	Y12
E24	VSS[231]	VSS[331]	Y15
E30	VSS[232]	VSS[332]	Y19
E34	VSS[233]	VSS[333]	Y23
E38	VSS[234]	VSS[334]	Y28
E42	VSS[235]	VSS[335]	Y30
E46	VSS[236]	VSS[336]	Y31
E48	VSS[237]	VSS[337]	Y32
E6	VSS[238]	VSS[338]	Y38
F8	VSS[239]	VSS[339]	Y43
F49	VSS[240]	VSS[340]	Y46
F5	VSS[241]	VSS[341]	P49
G10	VSS[242]	VSS[342]	Y5
G14	VSS[243]	VSS[343]	Y6
G18	VSS[244]	VSS[344]	Y8
G2	VSS[245]	VSS[345]	P24
G22	VSS[246]	VSS[346]	T43
G32	VSS[247]	VSS[347]	AD51
G36	VSS[248]	VSS[348]	AT8
G40	VSS[249]	VSS[349]	AD47
G44	VSS[250]	VSS[350]	Y47
G52	VSS[251]	VSS[351]	AT12
AF39	VSS[252]	VSS[352]	AM6
H16	VSS[253]	VSS[353]	AT13
H20	VSS[254]	VSS[354]	AM5
H30	VSS[255]	VSS[355]	AK45
H34	VSS[256]	VSS[356]	AK38
H38	VSS[257]	VSS[357]	AV14
H42	VSS[258]	VSS[358]	

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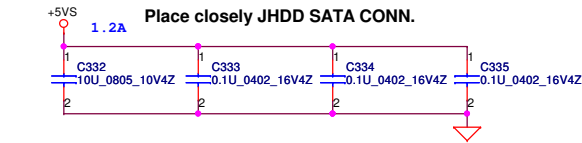
UBH

AB16	VSS[0]		
AA19	VSS[1]	VSS[80]	AK30
AA20	VSS[2]	VSS[81]	AK31
AA22	VSS[3]	VSS[82]	AK32
AM19	VSS[4]	VSS[83]	AK33
AA24	VSS[5]	VSS[84]	AK34
AA26	VSS[6]	VSS[85]	AK35
AA28	VSS[7]	VSS[86]	AK38
AA30	VSS[8]	VSS[87]	AK43
AA31	VSS[9]	VSS[88]	AK46
AB11	VSS[10]	VSS[89]	AK49
AB15	VSS[11]	VSS[90]	AK5
AB23	VSS[12]	VSS[91]	AL2
AB30	VSS[13]	VSS[92]	AL52
AB31	VSS[14]	VSS[93]	AM11
AB32	VSS[15]	VSS[94]	BB44
AB39	VSS[16]	VSS[95]	AD24
AB43	VSS[17]	VSS[96]	AM20
AB47	VSS[18]	VSS[97]	AM22
AB5	VSS[19]	VSS[98]	AM24
AB6	VSS[20]	VSS[99]	AM26
AC3	VSS[21]	VSS[100]	AM28
AC52	VSS[22]	VSS[101]	BA42
AD11	VSS[23]	VSS[102]	AM30
AD12	VSS[24]	VSS[103]	AM31
AD16	VSS[25]	VSS[104]	AM32
AD23	VSS[26]	VSS[105]	AM33
AD30	VSS[27]	VSS[106]	AM34
AD31	VSS[28]	VSS[107]	AM35
AD32	VSS[29]	VSS[108]	AM38
AD34	VSS[30]	VSS[109]	AM39
AD42	VSS[31]	VSS[110]	AM42
AD46	VSS[32]	VSS[111]	AM46
AD49	VSS[33]	VSS[112]	AV22
AD7	VSS[34]	VSS[113]	AM49
AE2	VSS[35]	VSS[114]	AM7
AE4	VSS[36]	VSS[115]	AA50
AE5	VSS[37]	VSS[116]	BB10
AF12	VSS[38]	VSS[117]	AN32
Y13	VSS[39]	VSS[118]	AN50
Y18	VSS[40]	VSS[119]	AN52
Y19	VSS[41]	VSS[120]	AP12
Y23	VSS[42]	VSS[121]	AP22
Y28	VSS[43]	VSS[122]	AP46
Y30	VSS[44]	VSS[123]	AP49
Y31	VSS[45]	VSS[124]	AP5
Y32	VSS[46]	VSS[125]	AP8
Y34	VSS[47]	VSS[126]	AP2
Y35	VSS[48]	VSS[127]	AP52
Y38	VSS[49]	VSS[128]	AT11
Y43	VSS[50]	VSS[129]	AT12
Y45	VSS[51]	VSS[130]	AT32
Y46	VSS[52]	VSS[131]	AT36
Y47	VSS[53]	VSS[132]	AT41
Y49	VSS[54]	VSS[133]	AT47
Y5	VSS[55]	VSS[134]	AT7
Y7	VSS[56]	VSS[135]	AV12
Y8	VSS[57]	VSS[136]	AV16
W2	VSS[58]	VSS[137]	AV20
W52	VSS[59]	VSS[138]	AV24
Y11	VSS[60]	VSS[139]	AV30
Y12	VSS[61]	VSS[140]	AV34
Y15	VSS[62]	VSS[141]	AV38
Y19	VSS[63]	VSS[142]	AV42
Y23	VSS[64]	VSS[143]	AV46
Y28	VSS[65]	VSS[144]	AV49
Y30	VSS[66]	VSS[145]	AV5
Y31	VSS[67]	VSS[146]	AV8
Y32	VSS[68]	VSS[147]	AW14
Y38	VSS[69]	VSS[148]	AW18
Y43	VSS[70]	VSS[149]	AW2
Y46	VSS[71]	VSS[150]	BF9
Y47	VSS[72]	VSS[151]	AW32
Y49	VSS[73]	VSS[152]	AW36
Y5	VSS[74]	VSS[153]	AW40
Y7	VSS[75]	VSS[154]	AW52
Y8	VSS[76]	VSS[155]	AY11
W2	VSS[77]	VSS[156]	AY43
W52	VSS[78]	VSS[157]	AY47
Y11	VSS[79]	VSS[158]	

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Size	Document Number	Rev		1.0	
Custom	NDU00_LA-6031P M/B				
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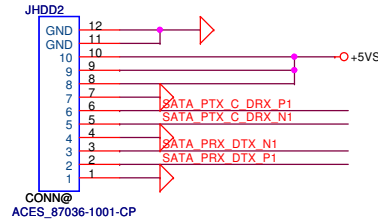
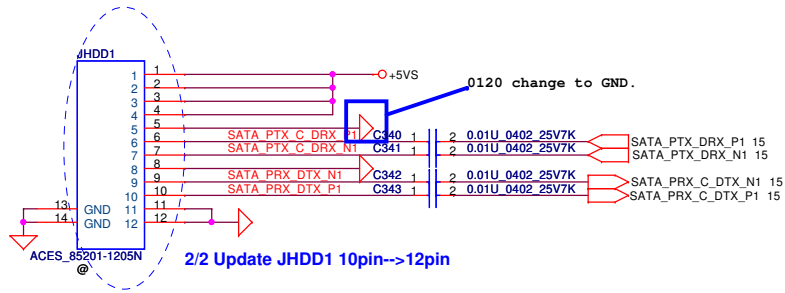
## SATA HDD Conn.



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1/28 Add JHDD2

JHDD2 Layout symbol reverse JHDD1, reverse the pin define

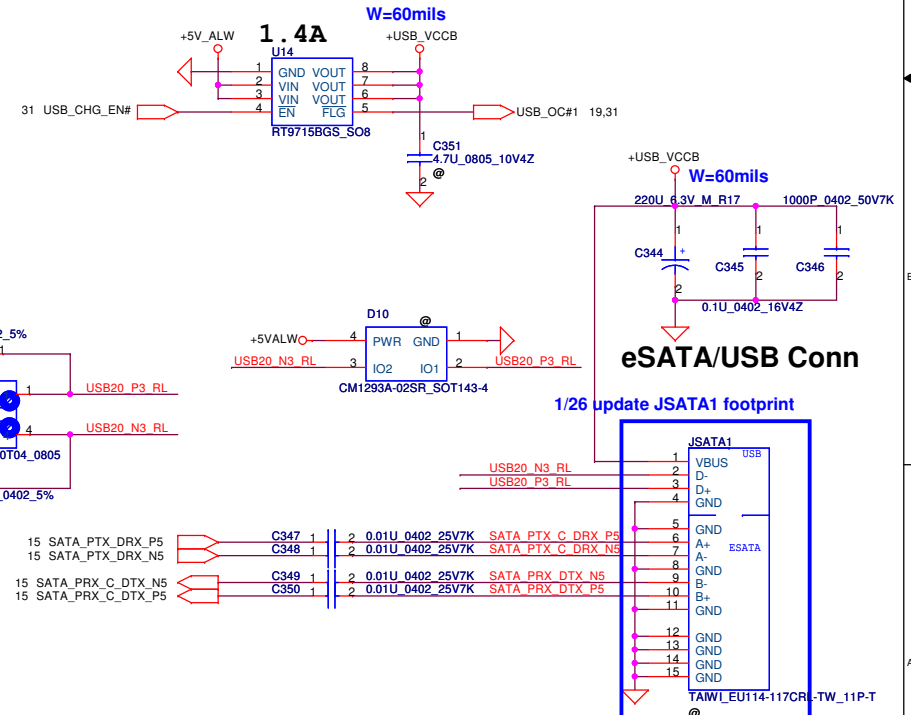
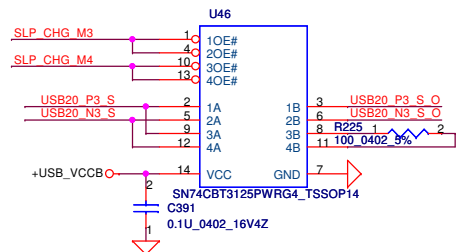
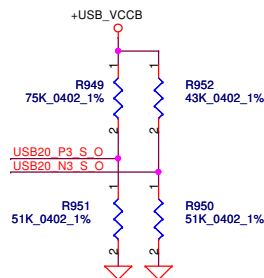
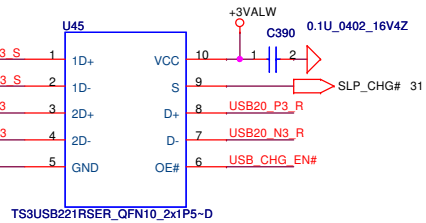
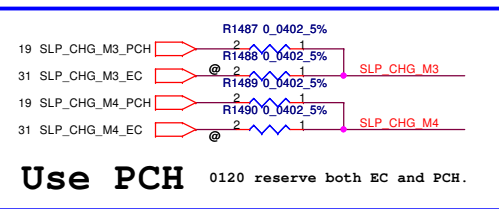


Add wire connector for H/W SATA verify

## eSATA/USB Combo

	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D

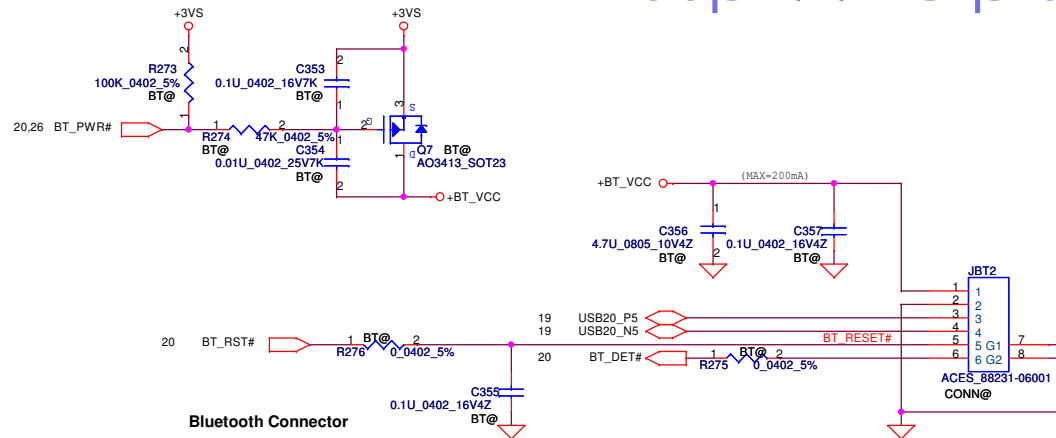


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2010/04/12		Deciphered Date		2010/01/23		Title			
								SATA-HDD/ODD/USB			
								Size			
								Document Number			
								NDU00_LA-6031P M/B			
								Date			
								Monday, April 12, 2010			
								Sheet			
								24 of 45			

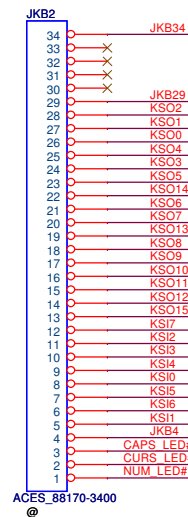
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# BlueTooth Interface

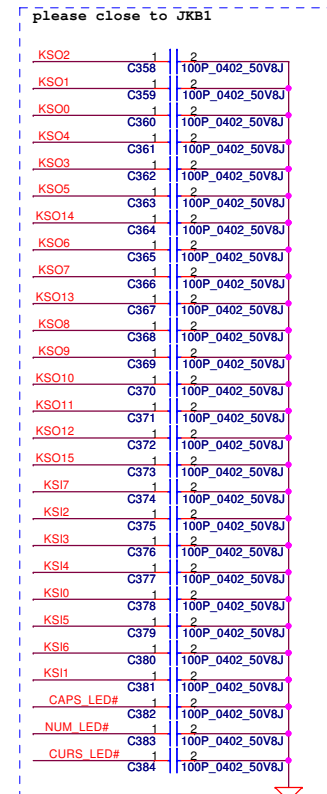
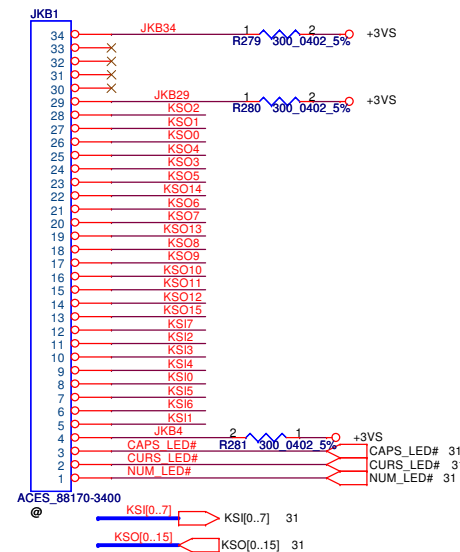
http://laptopblue.vn



## KEYBOARD CONN. for 11.6"

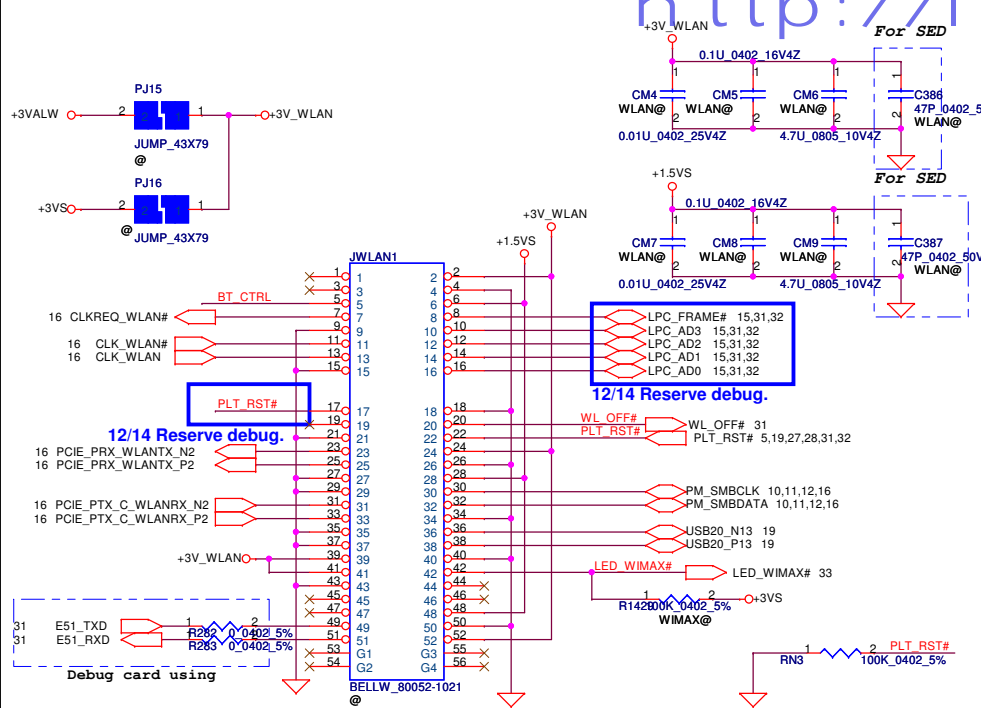


## KEYBOARD CONN. for 13.3"

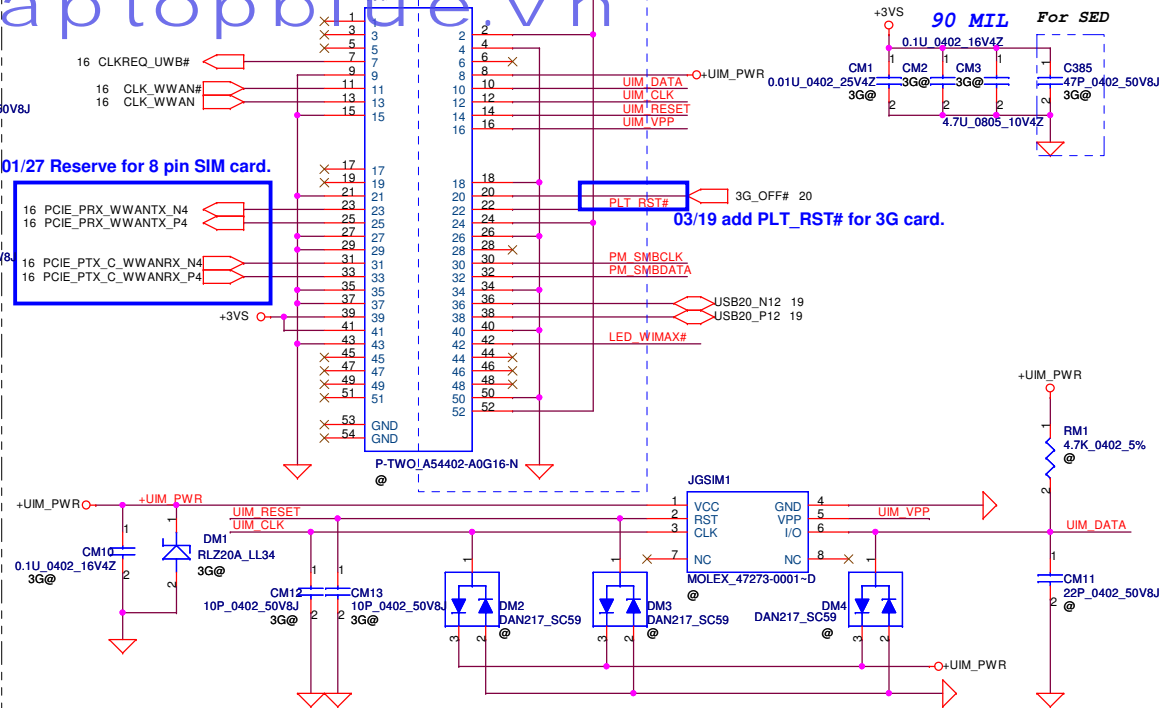


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Size		Document Number		Rev	
Date		Monday, April 12, 2010		Sheet 25 of 45	
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# PCIe Mini Card-WLAN/WiMax



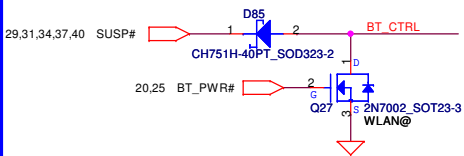
# PCIe Mini Card-3G

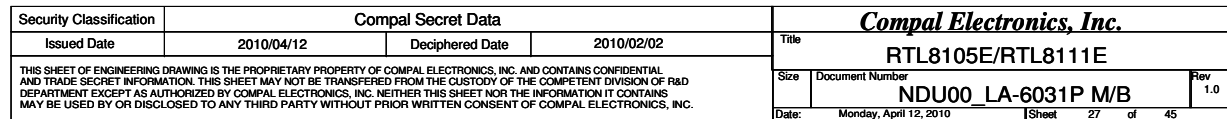
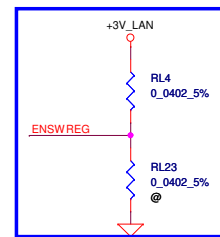
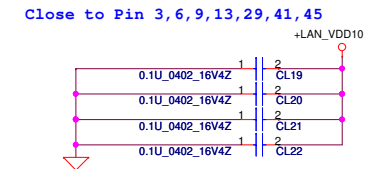
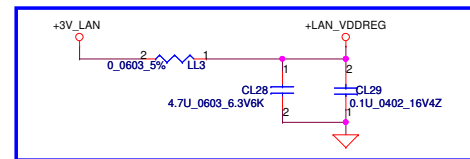
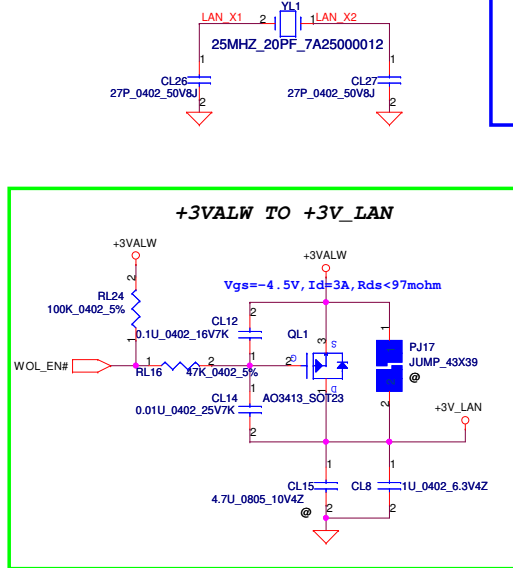


## WLAN&BT Combo module circuits

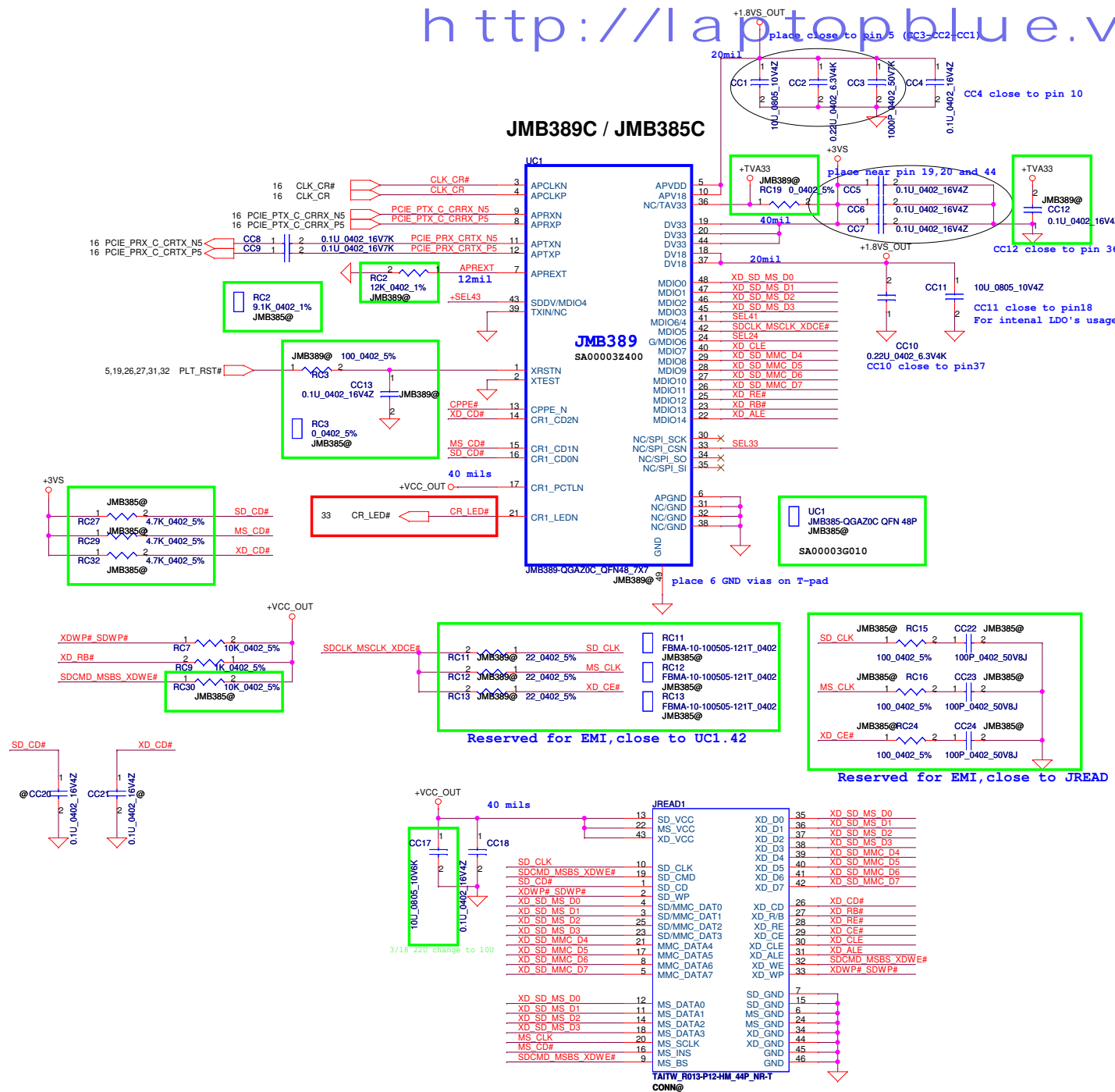
	BT on module Enable	BT on module Disable
BT_CTRL	HI	LO
BT_PWR#	LO	HI

\*\*If +3V\_WLAN is +3VS, please remove D21.

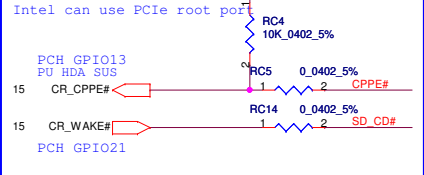




# JMB389C / JMB385C

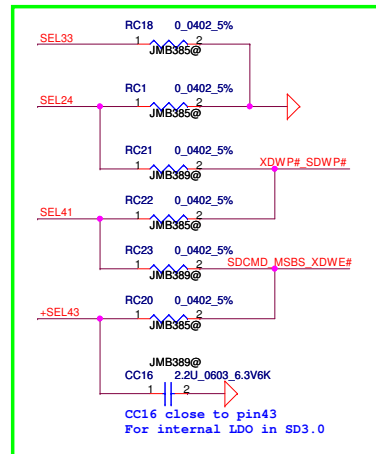
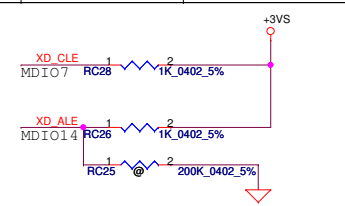


## D3E mode (Intel only)



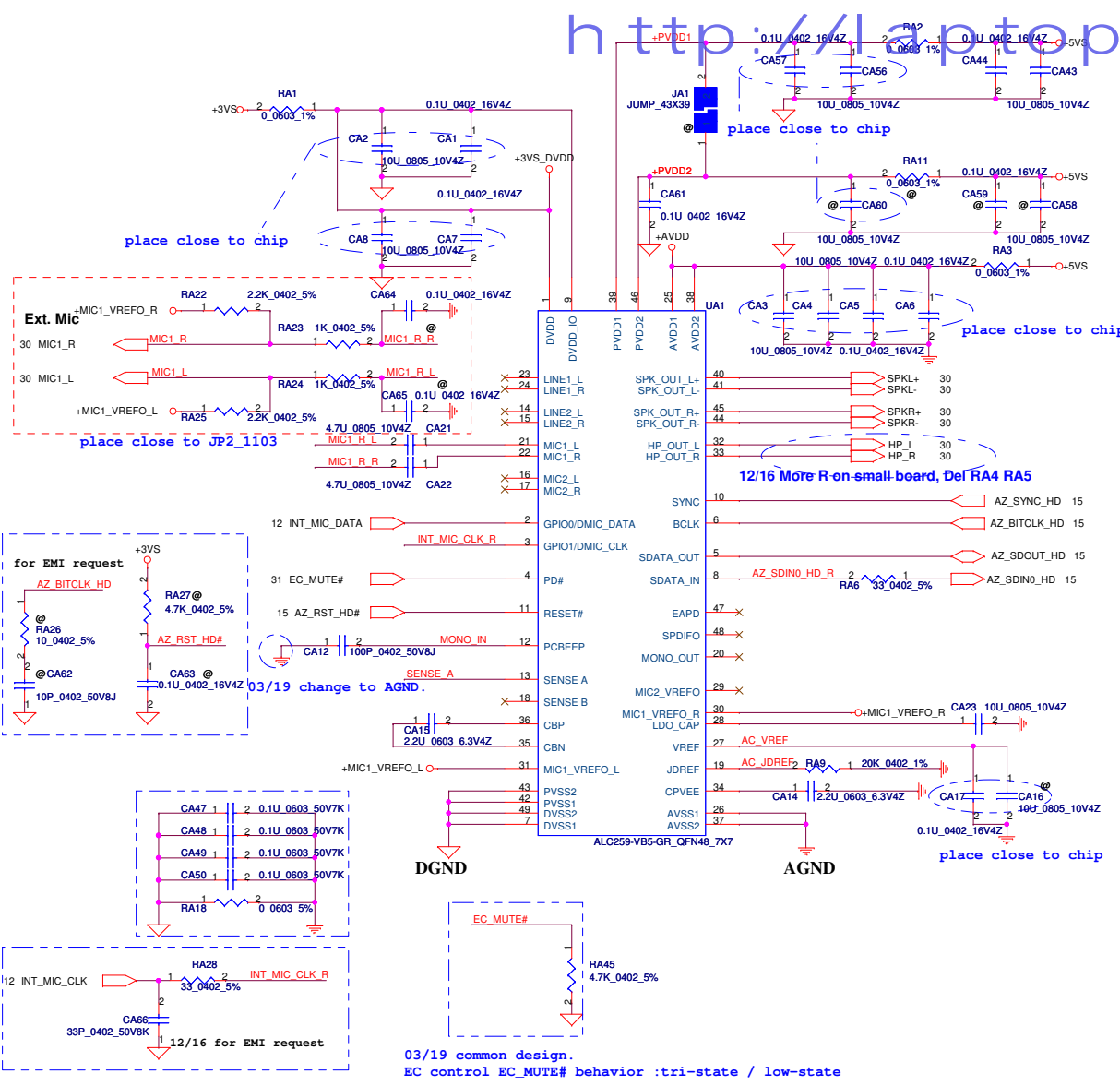
## Power On Strapping setting

Pin name	Description	
	High	low
MDIO7	on-board★	add-in card
MDIO14	CR_LED high active	CR_LED low active★

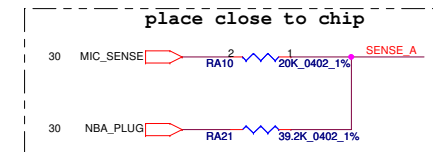


01/26 Update new card reader symbol to EVT

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Date: Monday, April 12, 2010				Sheet 28 of 45	



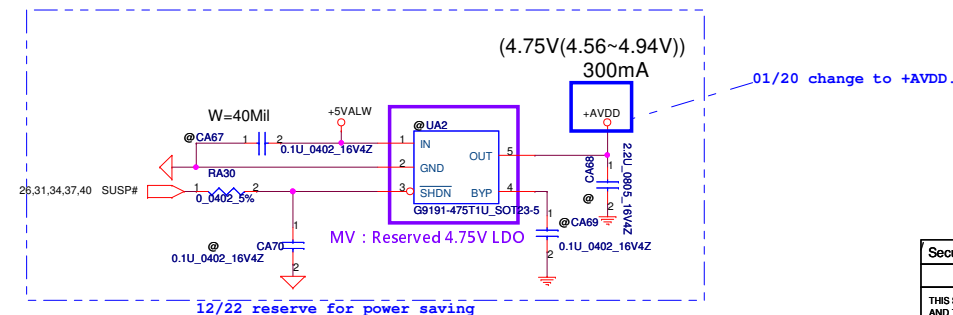
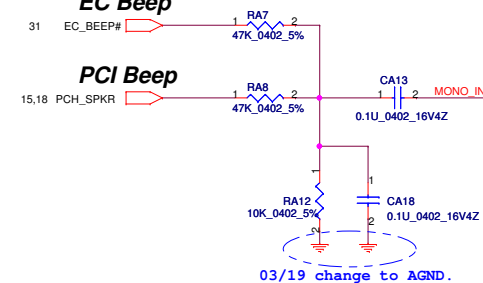
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



## Beep sound

### EC Beep

### PCI Beep



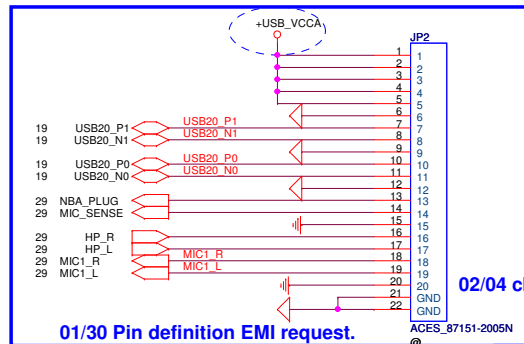
Security Classification		Compal Secret Data		Title	
Issued Date	2010/04/12	Deciphered Date	2009/04/14	<b>Compal Electronics, Inc.</b>	
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				Customer	NDU00_LA-6031P M/B
				Date	Monday, April 12, 2010
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				Rev	1.0



## USB+Audio FFC conn

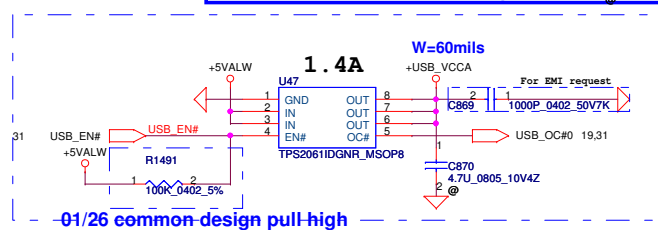
Pin=20pin, pitch=0.5

01/30 New JP2 Layout symbol reverse old conn, reserse the pin define

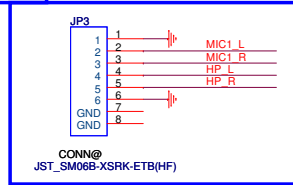


02/04 change back to 20 pins.

01/30 Pin definition EMI request.

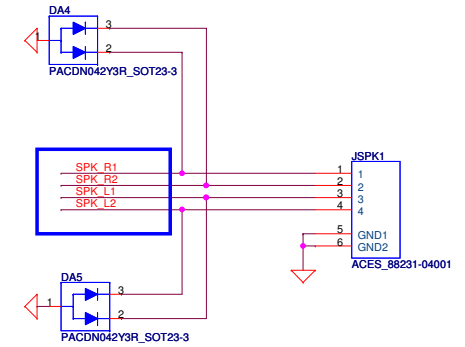
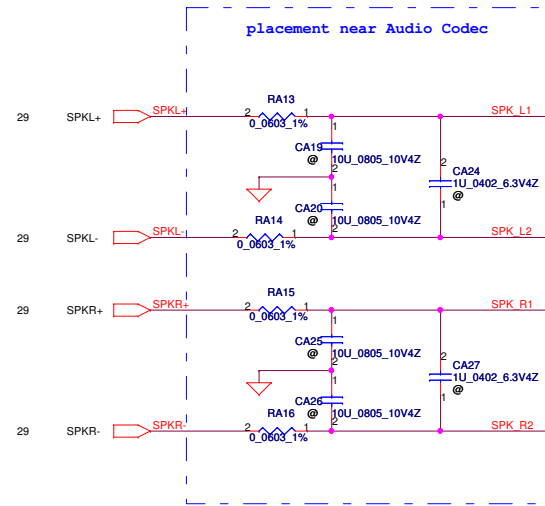


-01/26 common-design pull-high



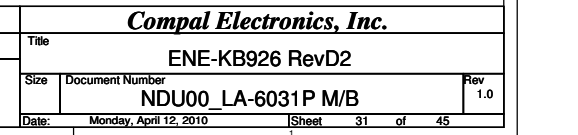
12/19 Reserved JP6 for audio test

## Speaker Connector



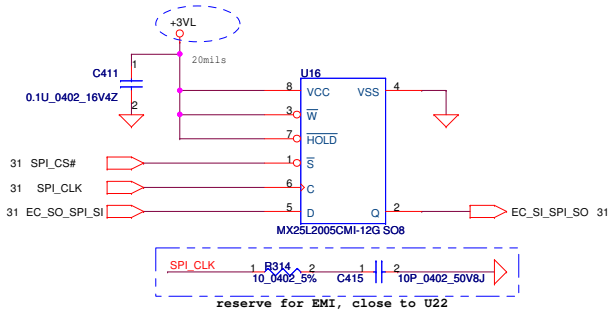
12/16 Fine tune SPK\_L1,SPK\_L2,SPK\_R1 and SPK\_R2 for SPK

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								AMP/Audio Jack/HP/SPEAKER/VR			
								Size			
								Document Number			
								NDU00_LA-6031P M/B			
								Date			
								Monday, April 12, 2010			
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								30 of 45			
								Rev			
								1.0			



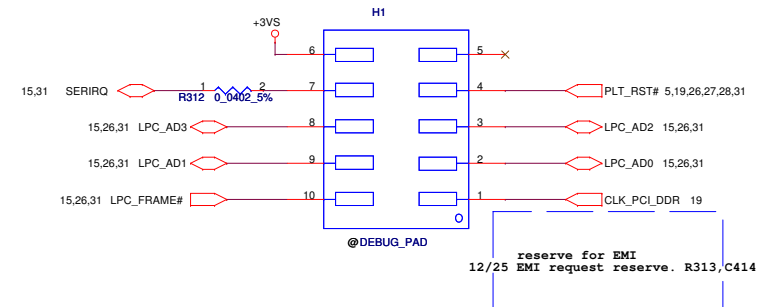
SPI Flash (256KB)

**Socket : SP07000F500 & SP07000H900**

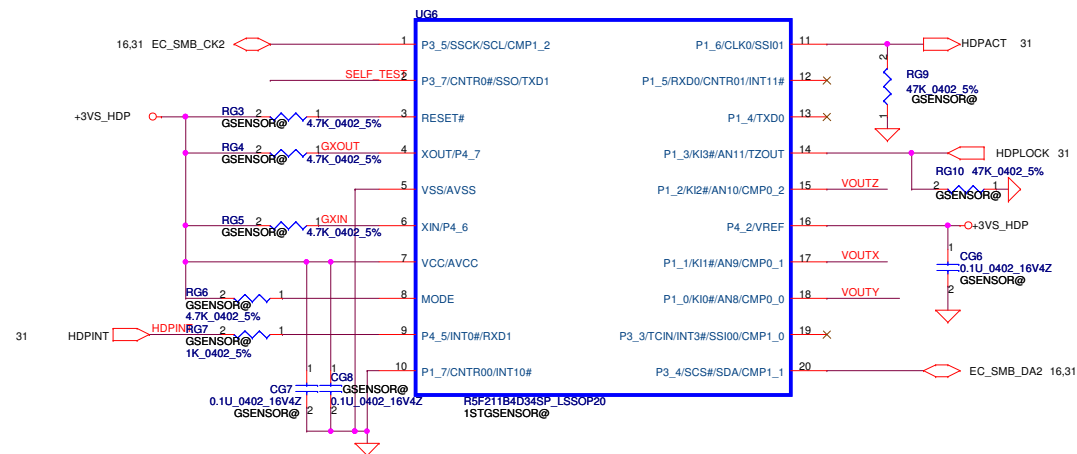
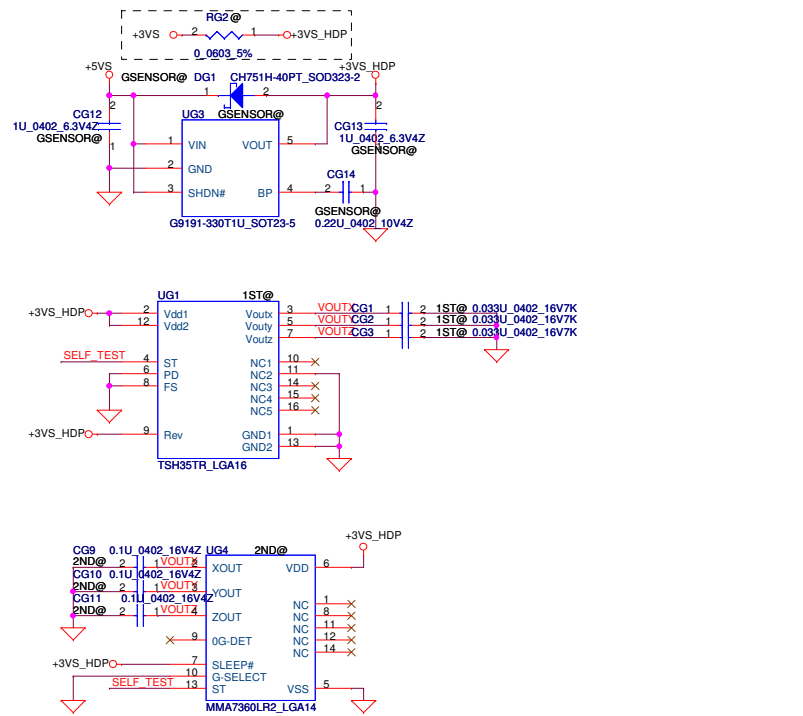


## LPC Debug Port

Please place the PAD under DDR DIMM.

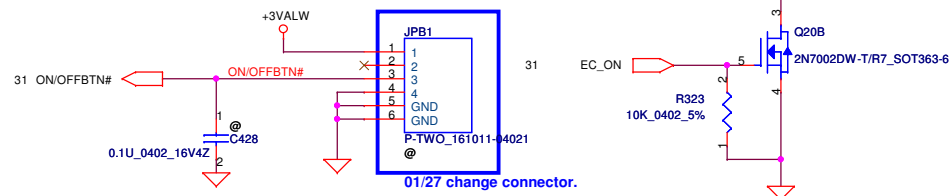


### ***G-Sensor***

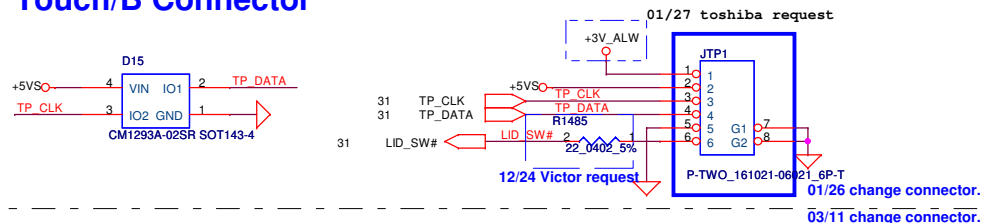


Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>		
Issued Date	2010/04/12	Deciphered Date	2009/04/14	Title <b>SPI/LPC/PS2/MDC/FM/CIR</b>		
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				Custom:		
				Date:	Monday, April 12, 2010	Sheet

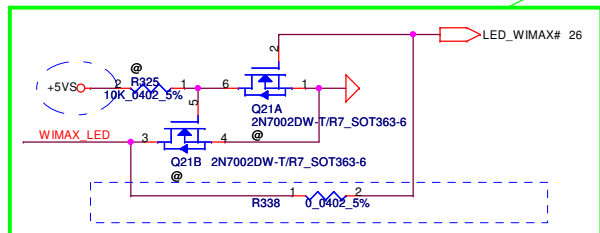
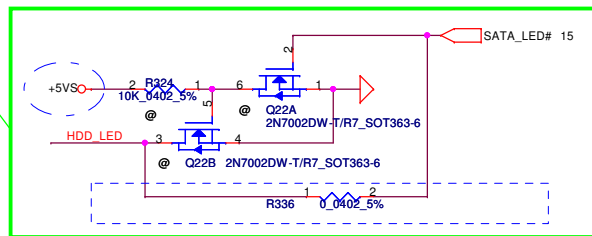
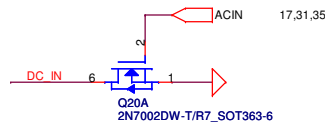
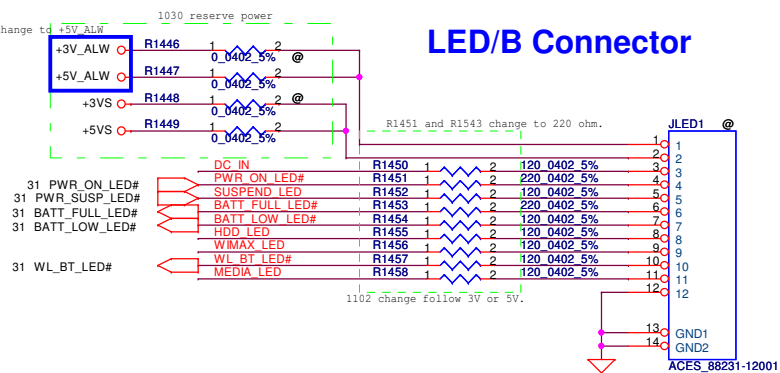
## Power Button & Lid switch



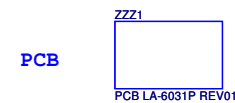
## Touch/B Connector



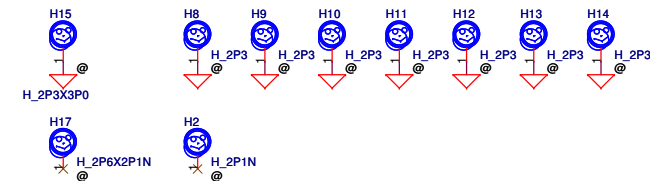
## LED/B Connector



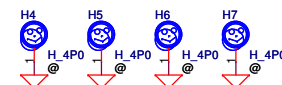
## ISPD



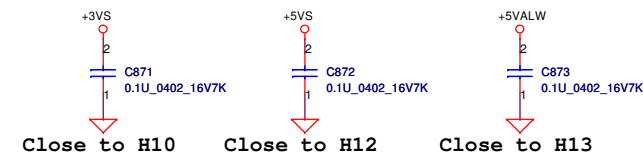
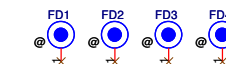
## Screw Hole



## CPU

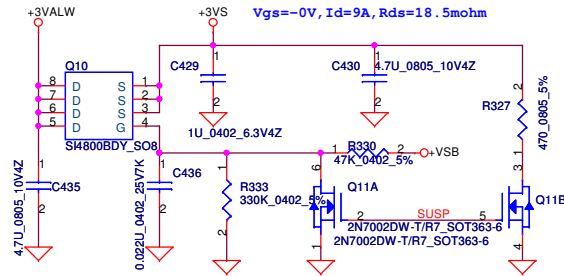


## PCB Fedical Mark PAD

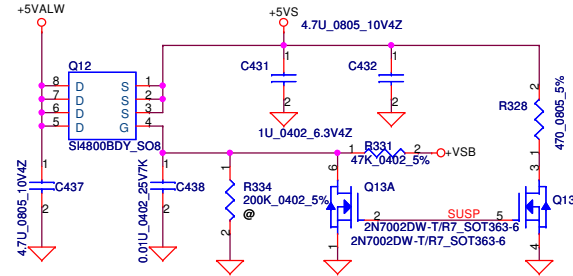


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Issued Date	2010/04/12	Deciphered Date	2010/01/23	Title	
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				Size	Document Number
				NDU00_LA-6031P M/B	
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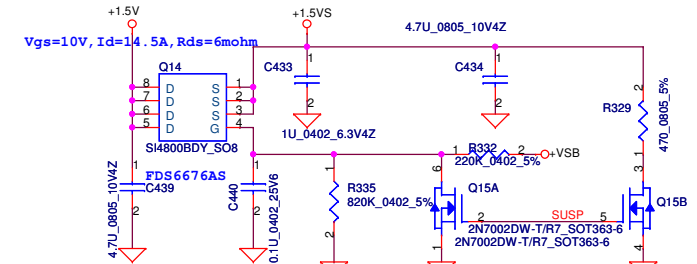
### +3VALW TO +3VS



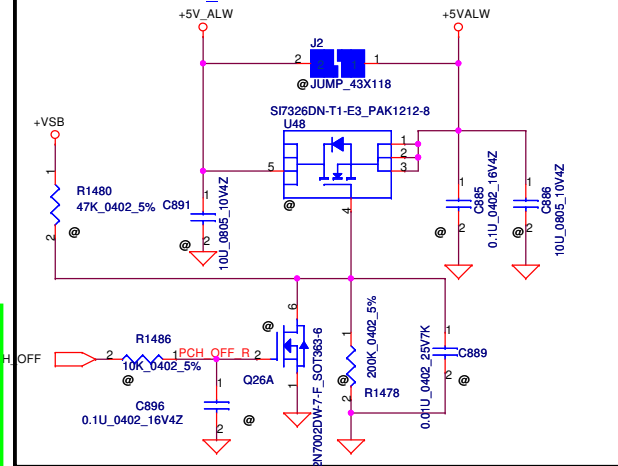
### +5VALW TO +5VS



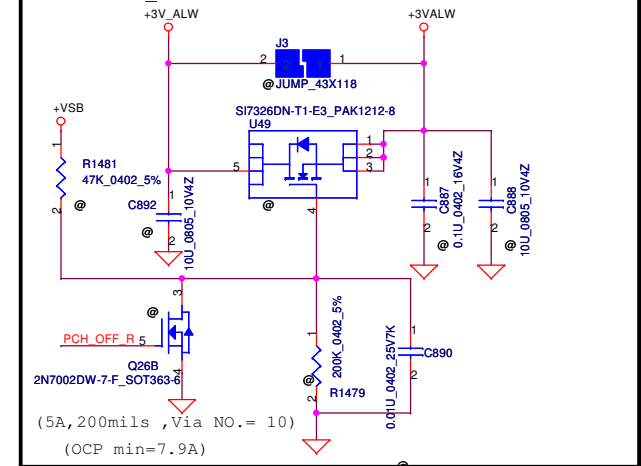
### +1.5V to +1.5VS



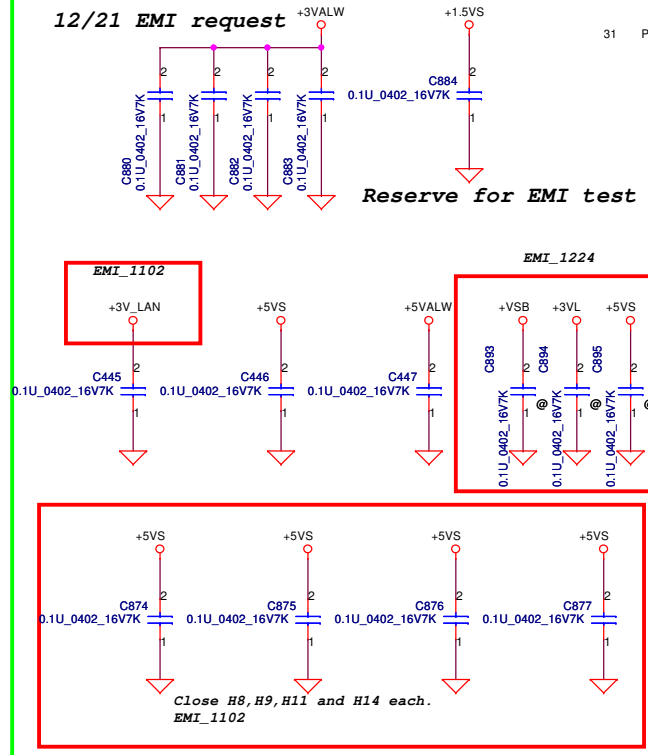
### +5V\_ALW to +5VALW Transfer



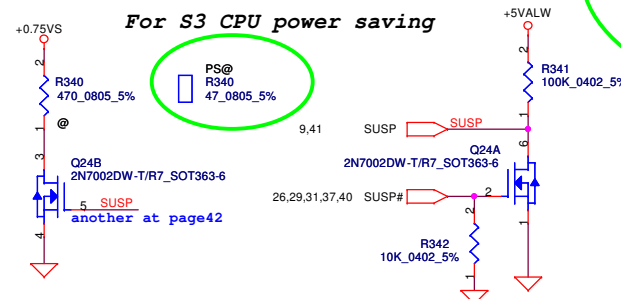
### +3V\_ALW to +3VALW Transfer



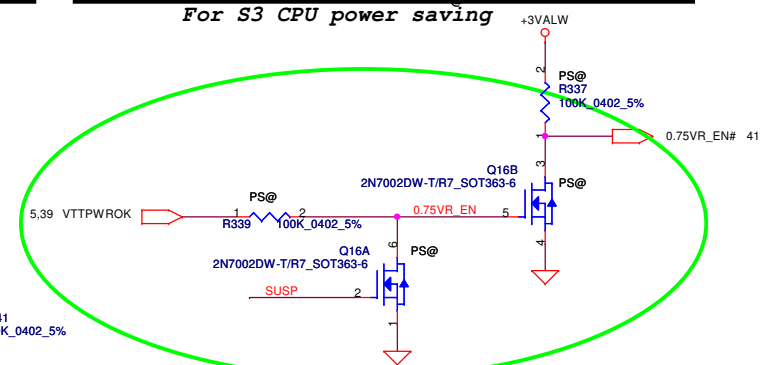
### 12/21 EMI request



### For S3 CPU power saving

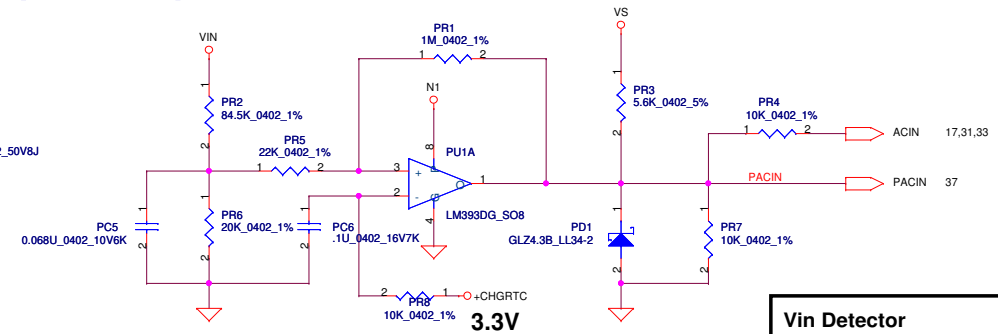
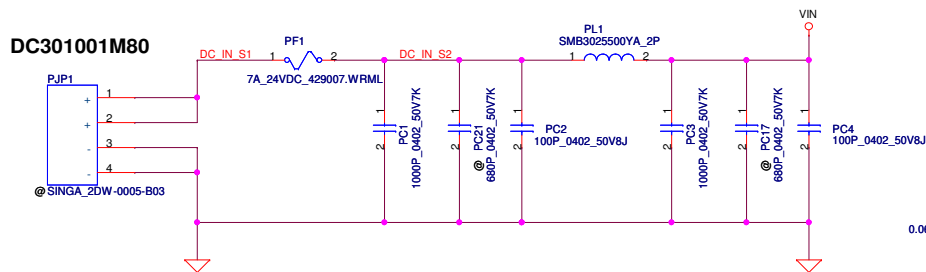


### For S3 CPU power saving



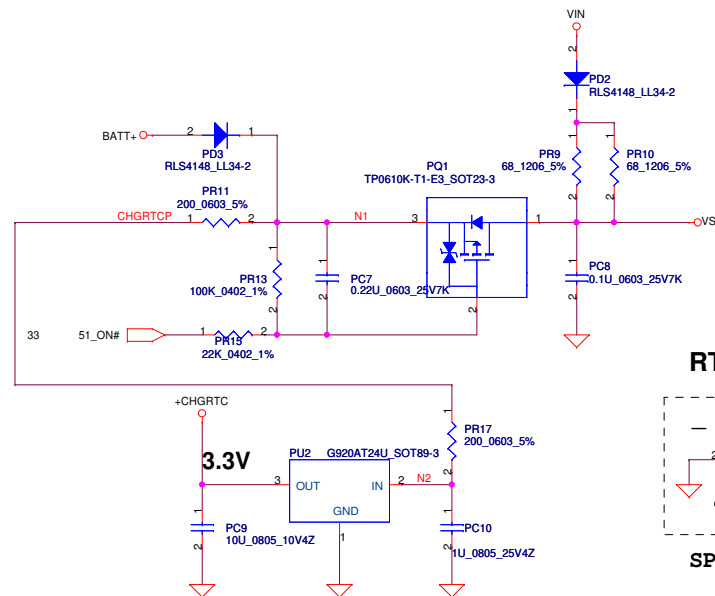
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Issued Date	2010/04/12	Deciphered Date	2010/01/23	Title	
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Size	Document Number	NDU00_LA-6031P M/B		Rev	1.0
Date	Monday, April 12, 2010	Sheet	34	of	45

**DC301001M80**

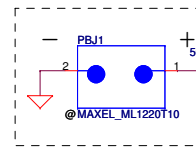


## Vin Detector

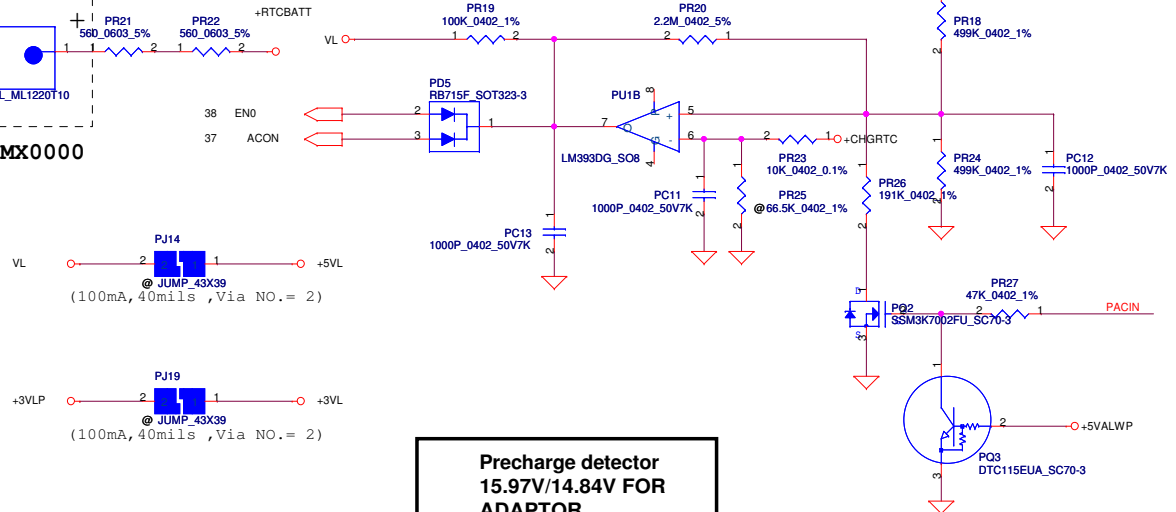
High	18.384	17.901	17.430
Low	17.728	17.257	16.976



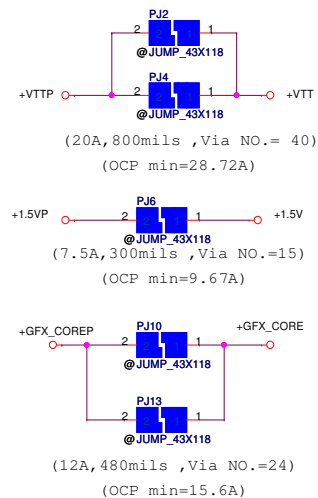
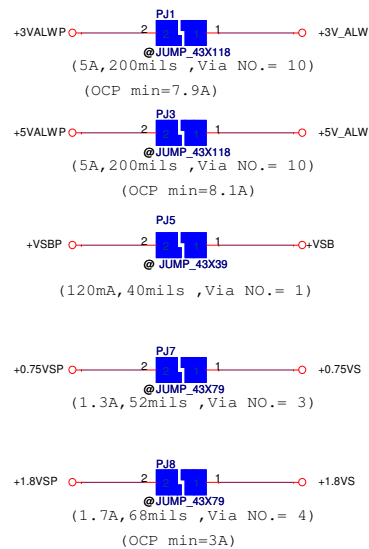
## RTC Battery



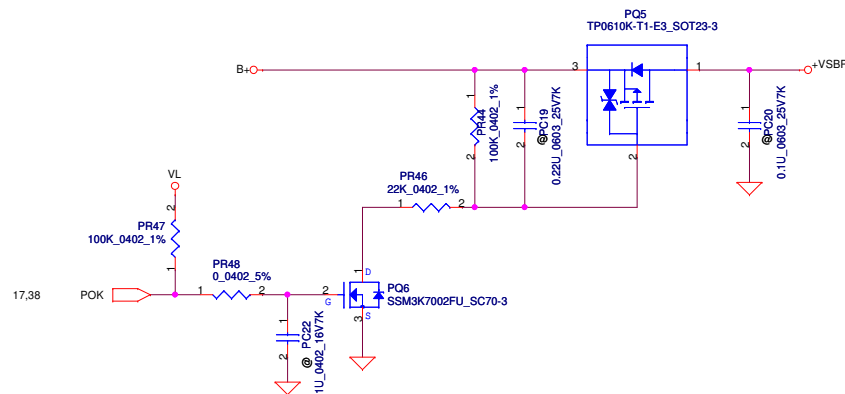
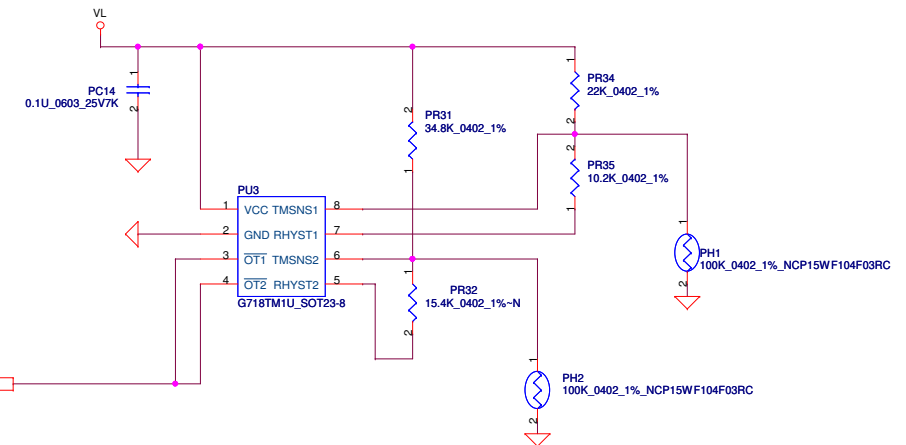
SP093MX0000



**Precharge detector  
15.97V/14.84V FOR  
ADAPTOR**

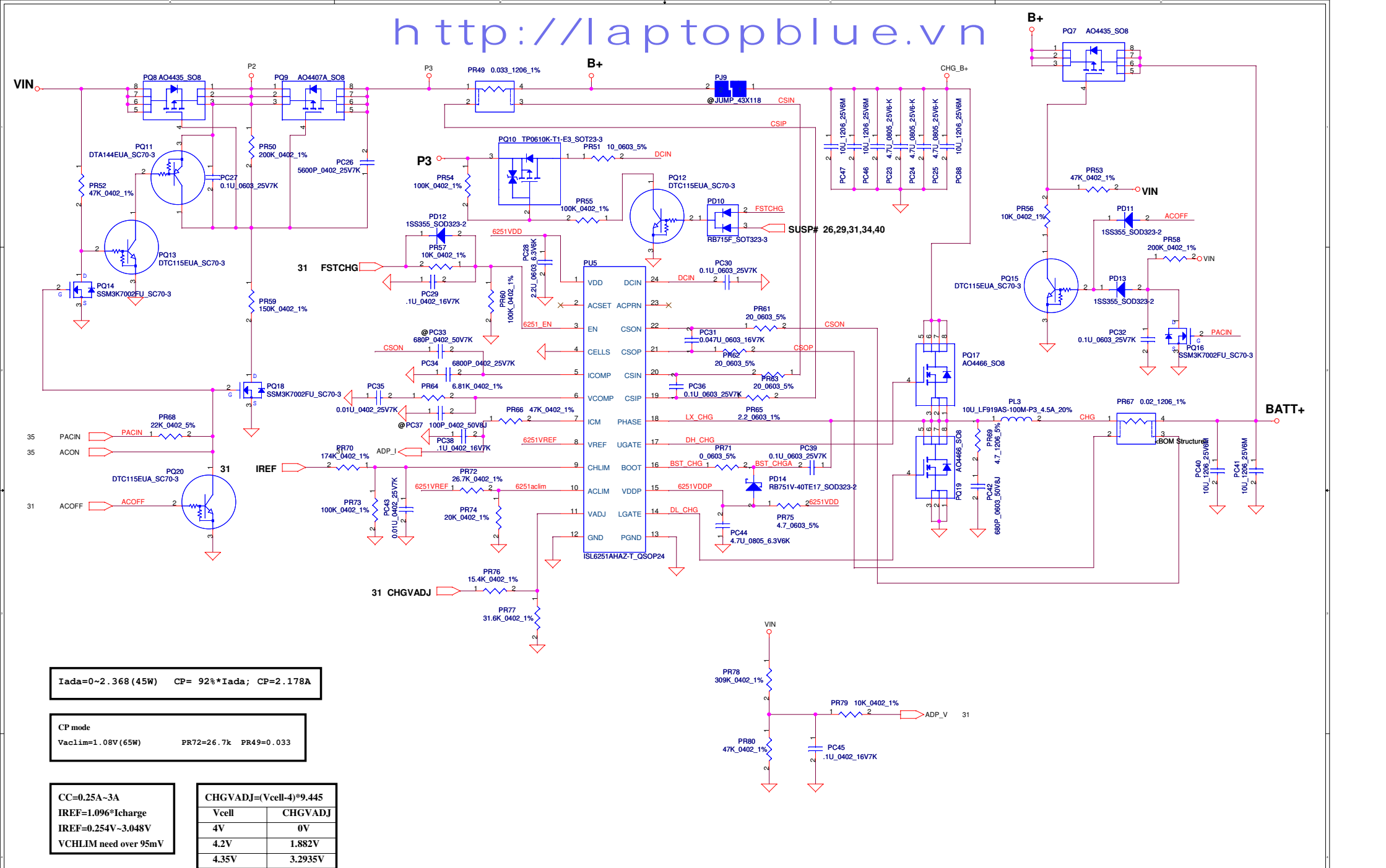


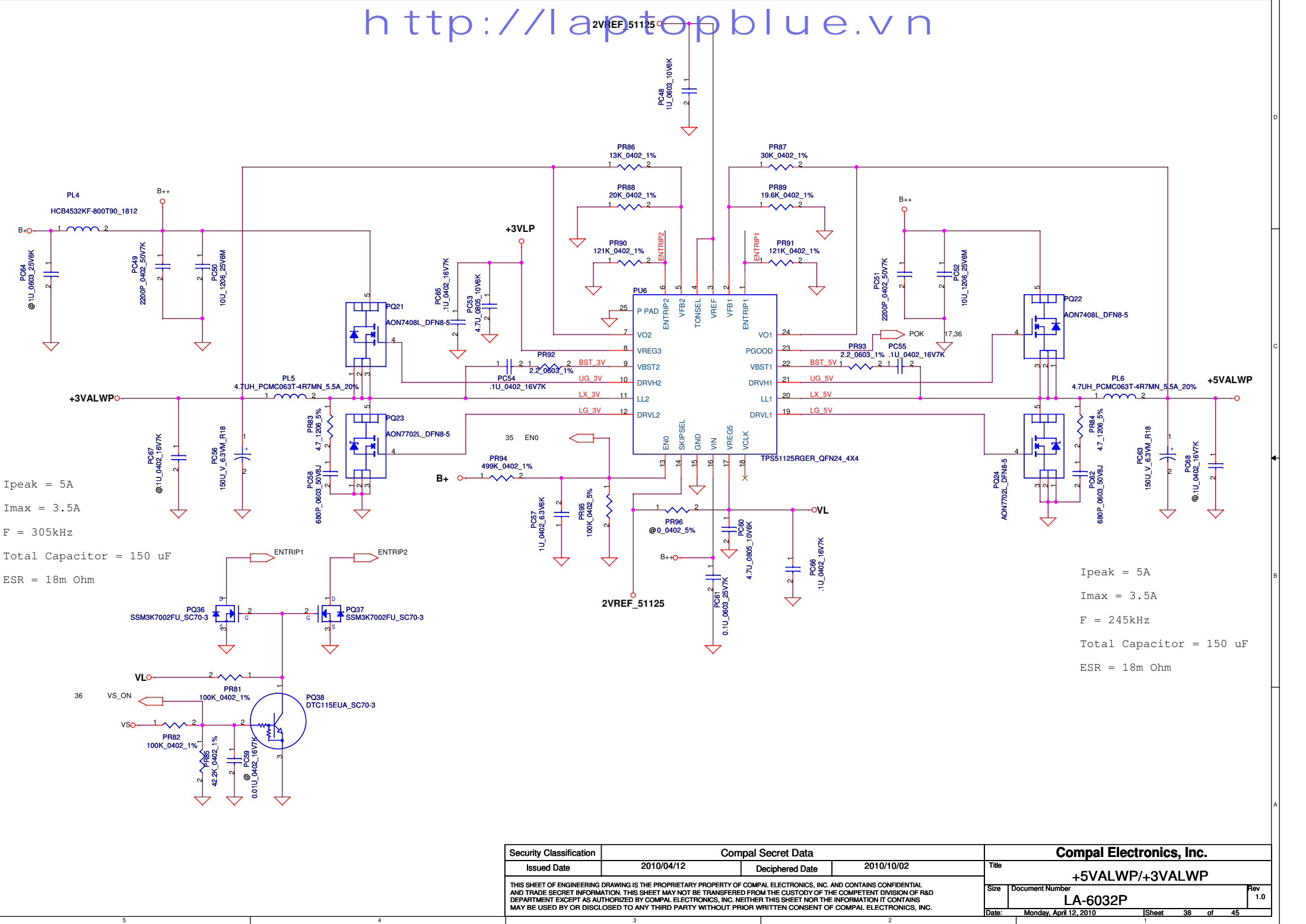
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								Size	Document Number			LA-6031P		Rev
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Ipeak = 5A  
 Imax = 3.5A  
 F = 305kHz  
 Total Capacitor = 150 uF  
 ESR = 18m Ohm

Ipeak = 5A  
 Imax = 3.5A  
 F = 245kHz  
 Total Capacitor = 150 uF  
 ESR = 18m Ohm

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ESR = 3m Ohm

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$I_{peak} = 7.5A$   
 $I_{max} = 5.25A$   
 $F = 313kHz$   
 Total Capacitor = 550 uF  
 ESR = 6.6m Ohm

$I_{peak} = 1.7A$   
 $I_{max} = 5.25A$   
 $F = 1.5MHz$   
 Total Capacitor = 44 uF  
 ESR = 2.5m Ohm

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31 SYSON

PR118 0\_0402\_5%

PC83 0.1U\_0402\_16V7K

PR121 100\_0603\_1%

PC86 4.7U\_0603\_6.3V6K

PR122 18K\_0402\_1%

PR123 10K\_0402\_1%

PR124 10K\_0402\_1%

PC88 4.7U\_0603\_6.3V6K

PC89 4.7U\_0805\_10V6K

PR117 255K\_0402\_1%

PR119 2.2\_0603\_1%

PC84 0.1U\_0603\_25V7K

PR120 4.7\_1206\_5%

PC90 680P\_0603\_50V8J

PC91 4.7U\_0805\_25V6K

PC92 4.7U\_0805\_25V6K

PC93 4.7U\_0805\_25V6K

PC94 4.7U\_0805\_25V6K

PC95 220U\_6.3V\_M

PL10 1.8UH\_SIL104R-1R8PF\_9.5A\_30%

PU8 RT8209BGQW\_WQFN14\_3P5X3P5

TON EN/DEM

VOUT

VDD

FB

PGOOD

GND

PGND

NC

BOOT

UGATE

PHASE

CS

VDDP

LGATE

BST 1.5V

DH 1.5V

LX 1.5V

DL 1.5V

PL9 HCB2012KF-121T50\_0805

1.5V B+

PL10 1.8UH\_SIL104R-1R8PF\_9.5A\_30%

PR120 4.7\_1206\_5%

PC90 680P\_0603\_50V8J

PC91 4.7U\_0805\_25V6K

PC92 4.7U\_0805\_25V6K

PC93 4.7U\_0805\_25V6K

PC94 4.7U\_0805\_25V6K

PC95 220U\_6.3V\_M

+1.5VP

Ipeak = 7.5A

Imax = 5.25A

F = 313kHz

Total Capacitor = 550 uF

ESR = 6.6m Ohm

+5V\_ALW

PJ12 @ JUMP\_43X39

PC134 0.1U\_0402\_25V6

PC135 10U\_0805\_10V4Z

PC136 10U\_0805\_10V4Z

PC137 22U\_0805\_6.3V6M

PC138 22U\_0805\_6.3V6M

PC139 680P\_0603\_50V7K

PR193 316K\_0402\_1%

PR194 402K\_0402\_1%

PR195 0\_0402\_5%

PR196 4.7\_1206\_5%

PL15 2.2UH\_SILM320A-2R2\_1.6A\_30%

PU9 MP2121DQ-LF-Z\_QFN10\_3X3

FB EN/SYNC

GND

SW

IN

BS

POK

TP

PC132 0.1U\_0402\_16V7K

PC133 0.1U\_0402\_16V7K

PR193 316K\_0402\_1%

PR194 402K\_0402\_1%

PR195 0\_0402\_5%

PR196 4.7\_1206\_5%

PL15 2.2UH\_SILM320A-2R2\_1.6A\_30%

PC137 22U\_0805\_6.3V6M

PC138 22U\_0805\_6.3V6M

PC139 680P\_0603\_50V7K

+1.8VSP

SUSP# 26,29,31,34,37

Ipeak = 1.7A

Imax = 5.25A

F = 1.5MHz

Total Capacitor = 44 uF

ESR = 2.5m Ohm

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31 SYSON

PR118 0\_0402\_5%

PC83 0.1U\_0402\_16V7K

PR121 100\_0603\_1%

PC86 4.7U\_0603\_6.3V6K

+5V\_ALW

PR123 10K\_0402\_1%

PR124 10K\_0402\_1%

PR117 255K\_0402\_1%

PR119 2.2\_0603\_1%

PU8 RT8209BGQW\_WQFN14\_3P5X3P5

TON EN/DEM

VOUT

VDD

FB

PGOOD

GND

PGND

BOOT

UGATE

PHASE

CS

VDDP

LGATE

BST 1.5V

PR122 18K\_0402\_1%

PC84 0.1U\_0603\_25V7K

+5V\_ALW

PC89 4.7U\_0805\_10V6K

PQ28 AO4466\_S08

PQ29 AO4712\_S08

PR120 4.7\_1206\_5%

PC87 680P\_0603\_50V8J

PL10 1.8UH\_SIL104R-1R8PF\_9.5A\_30%

PC35 220U\_6.3V\_M

1.5V B+

PC81 4.7U\_0805\_25V6-K

PC82 4.7U\_0805\_25V6-K

1.5VP

Ipeak = 7.5A

Imax = 5.25A

F = 313kHz

Total Capacitor = 550 uF

ESR = 6.6m Ohm

+1.8VSP

PR193 316K\_0402\_1%

PR194 402K\_0402\_1%

PC133 0.1U\_0402\_16V7K

PR195 0\_0402\_5%

PU9 MP2121DQ-LF-Z\_QFN10\_3X3

FB EN/SYNC

GND

SW

IN

BS

POK

TP

PR192 0\_0402\_5%

PC132 0.1U\_0402\_16V7K

SUSP# 26,29,31,34,37

PC134 0.1U\_0402\_25V6

PC135 10U\_0805\_10V4Z

PC136 10U\_0805\_10V4Z

PJ12 @ JUMP\_43X39

PC137 22U\_0805\_6.3V6M

PC138 22U\_0805\_6.3V6M

PL15 2.2UH\_SILM320A-2R2\_1.6A\_30%

PC139 680P\_0603\_50V7K

PR196 4.7\_1206\_5%

PC17 B340A\_SMA2

+1.8VSP

Ipeak = 1.7A

Imax = 5.25A

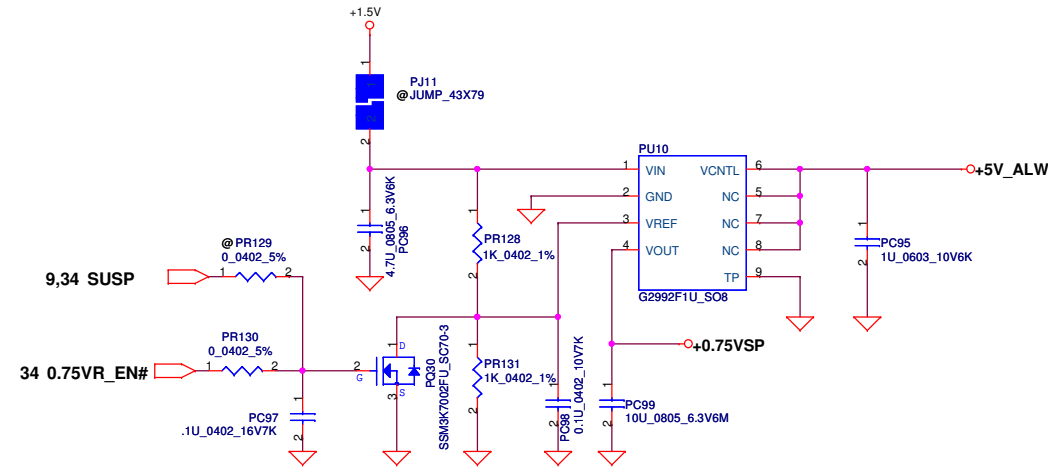
F = 1.5MHz

Total Capacitor = 44 uF

ESR = 2.5m Ohm

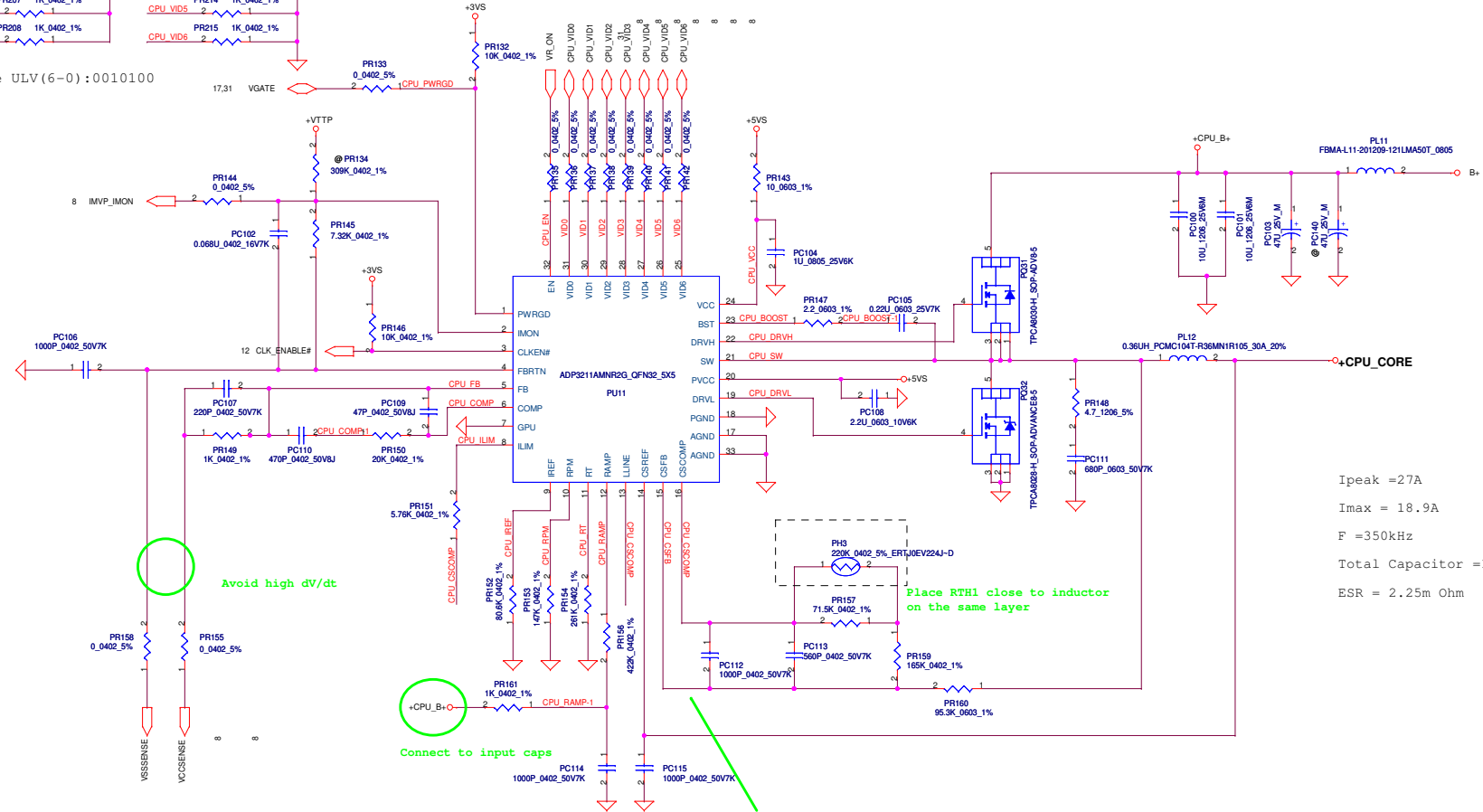
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								0.75VSP					
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Figure 10 is a schematic diagram of the power supply for the CPU. It shows a +3VS input connected to a network of resistors (PR129, PR130, PR131, PR132, PR133, PR134, PR144, PR145) and capacitors (PC102, PC103). The output of the network is connected to the CPU PWRGD pin. The diagram is labeled with component values and pin numbers.



I<sub>peak</sub> = 27A  
I<sub>max</sub> = 18.9A  
F = 350kHz  
Total Capacitor = 1320 uF  
ESR = 2.25m Ohm

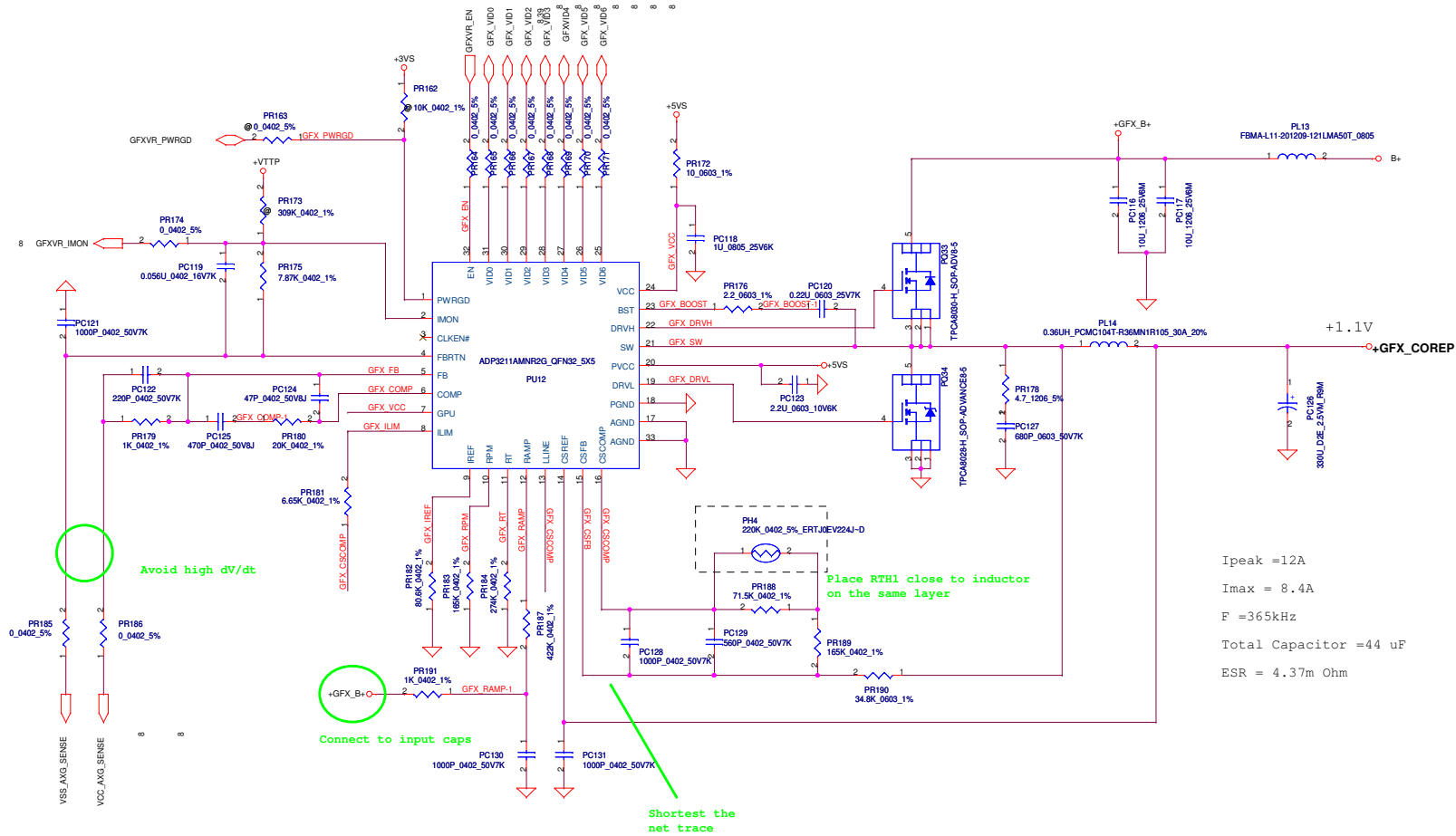
Connect to input caps

PC114  
1000P\_0402\_50V7K

PC115  
1000P\_0402\_50V7K

Shortest the net trace

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
2009/11/9 (EVT)	P38	+5VALWP/+3VALWP	PC54,PC55,PC65,PC66 change SE076104K8M8 to SE076104K80	change to A51 material
2009/11/9 (EVT)	P39	+VTTP	Resever PD15	Design change
2009/11/9 (EVT)	P41	+0.75VSP	Change PQ30 to SB000009610	Design change
2009/11/9 (EVT)	P42	CPU_CORE	Change PU11 change to ADP3211	Design change
2009/11/9 (EVT)	P42	CPU_CORE	Change PH3 &PH4	change to A51 material
2009/11/9 (EVT)	P37	CHARGE	Change PR49 change to 33m	Design change
2009/11/9 (EVT)	P38	+5VALWP/+3VALWP	PR90 & PR91 change to 121K	Design change
2009/12/1 (DVT)	P39	+CPU-CORE	Add PR202-PR215 pull-up & pull-down	Design change
2009/12/17 (DVT)	P36	Battery	Change PR31,PR32,PR34,PR35	Design change
2009/12/17 (DVT)	P37	CHARGE	Change PC23,PC24,PC25,PC81,PC82 1206 to 0805	Design change
2009/12/22 (DVT)	P42	CPU_CORE	Change PR147 0 ohm change to 2.2 ohm	EMI commond
2009/12/22 (DVT)	P43	GFX	Change PR176 0 ohm change to 2.2 ohm	EMI commond
2009/12/22 (DVT)	P39	+VTTP	ADD material PR125 & PR104 & PR102 and add net VTTPWORK_CPU	Design change
2010/01/25 (PVT)	P36	Battery	Add PD7,PD8	EMI require
2010/01/27 (PVT)	P37	CHARGE	Add 10u x3 PC46,PC47,PC88	EMC require
2010/02/04 (PVT)	P41	+0.75VSP	Resever PR129 Add PR130 and PC97	Design change
2009/02/04 (PVT)	P38	+5VALWP/+3VALWP	Change PQ38	Design change
2010/02/04 (PVT)	P42	CPU_CORE	Change PR160 to 95.3K and PR145 to 7.32K	Design change
2010/02/08 (PVT-2)	P36	Battery	Change PR21&PR22 and +CHGRTC	Design change

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Intel S3 power saving	05	Install Q1, R1484, C87 8, R8, R4C and Remove R2, R42	12/25	DVT
2	HDMI Detection function	14	modify HDMI_HPD circuit (Remove U7)	12/25	DVT
3	Sleep charge control method change	19 & 31	SLP_CHG_M3_R & SLP_CHG_M4_R change from PCH to Pin103 & 74 of EC	12/25	DVT
4	Implement Low power HDA	22	Reserve R1468 & R1469 for 1.5VALW (Low Power HDA)	12/25	DVT
5	Debug usage	26	Reserve LPC bus at WLAN soft	12/14	DVT
6	LAN circuit change for Vendore request	27	RL21 contact to GND	12/18	DVT
7	Avoid power leakage & reduce double pull up	27	Remove RL3	12/25	DVT
8	Transformer change	27	Move Transformer from Sub-board to M/B	12/21	DVT
9	Prevent Card Reader IC damage when insert dummy card	28	Add F2	12/24	DVT
10	Audio PD# issue (Could not work)	29	Add RA29 pull up	12/19	DVT
11	Avoid Audio noise	29	reserve and unistall CA70, CA68, CA69, UA2, RA30, CA67	12/22	DVT
12	Enhance Right side USB ability	30	modify JP2 pin assignment and reserve JP3 pad for test	12/19	DVT
13	Sleep charge control method change	31	add pin 21 of EC for control ALW power MOS	12/21	DVT
14	Sleep charge control method change	34	add two v_ALW power transfer circuits (3v_ALW to 3VALW & 5v_ALW to 5VALW)	12/21	DVT
15	system idle hang up issue	8	CPU_PSI# Pull down 1k ohm & H_DPRS LPVR pull up 1k ohm to Vtt	12/19	DVT
16	Sleep charge control method change	24	change U14 power from 5VALW to 5V_ALW	12/21	DVT
17					
18	EC_SW# pull up twice. R190	27	RL3 reserved.	01/20	PVT
19	Audio LDO reserved for AVDD.	29	UA2 pin 5 for +AVDD	01/20	PVT
20	For S3 power saving.	05	Reserve R2 and change R1484 to 0 ohm.	01/20	PVT
21	For 3G LED flash when resume from S3.	33	Reserve Q21 and Q22 circuit. Add R338 and R336.	01/20	PVT
22	Don't need discharge circuit.	34	Modify Q26 and Q27 circuit.	01/20	PVT
23	Reserve for PCH and EC both.	19,24, 31	Add R1487, R1488, R1489 and R1490.	01/20	PVT
24	Change JHDD1 pin 4 to GND.	24		01/20	PVT
25	Add BT power control circuit.	26	Add D85 and Q27.	01/20	PVT
26	change card reader connector.	28	ME request	01/26	PVT
27	change LED always power	33	3G LED flash issue.	01/26	PVT
28	change TP connector.	33	ME request	01/26	PVT
29	JGSIM2 connector.	26		01/26	PVT
30	add R1491 in USB_EN#	30		01/26	PVT
31	Lid switch change to +3V_ALW	31,33	Toshiba request.	01/26	PVT
32	add USB port 9 and PCIe port 4 for 8 pin SIM card.	16,19,26		01/27	PVT
33	add R1494 and D84 near D5, and add L_C near U8	15,18	EMI request	02/03	PVT
34	change MIC1_R and MIC1_L pull high.	29	MIC issue.	02/03	PVT
35	JLVDS1 pin24 change to NC.	12	Common design.	03/04	PVT2
36	CRT trace modify.	18	wrong trace.	03/04	PVT2
37	D5 layout close to PCH(U8)		layout change.	03/04	PVT2
38	Change O2 to JMicom card reader.	28		03/22	PVT2
39	USB OC# change.	19	Common design.	03/22	PVT2
40	Add R1505.	17	EMI request	03/22	PVT2

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