

Compal confidential

Thin & Light

NDU01/NDU11 LA-6032P REV 1.0 Schematics Document

Mobile AMD ASB2/RS880M/SB820M
2010-03-22 Rev. 1.0

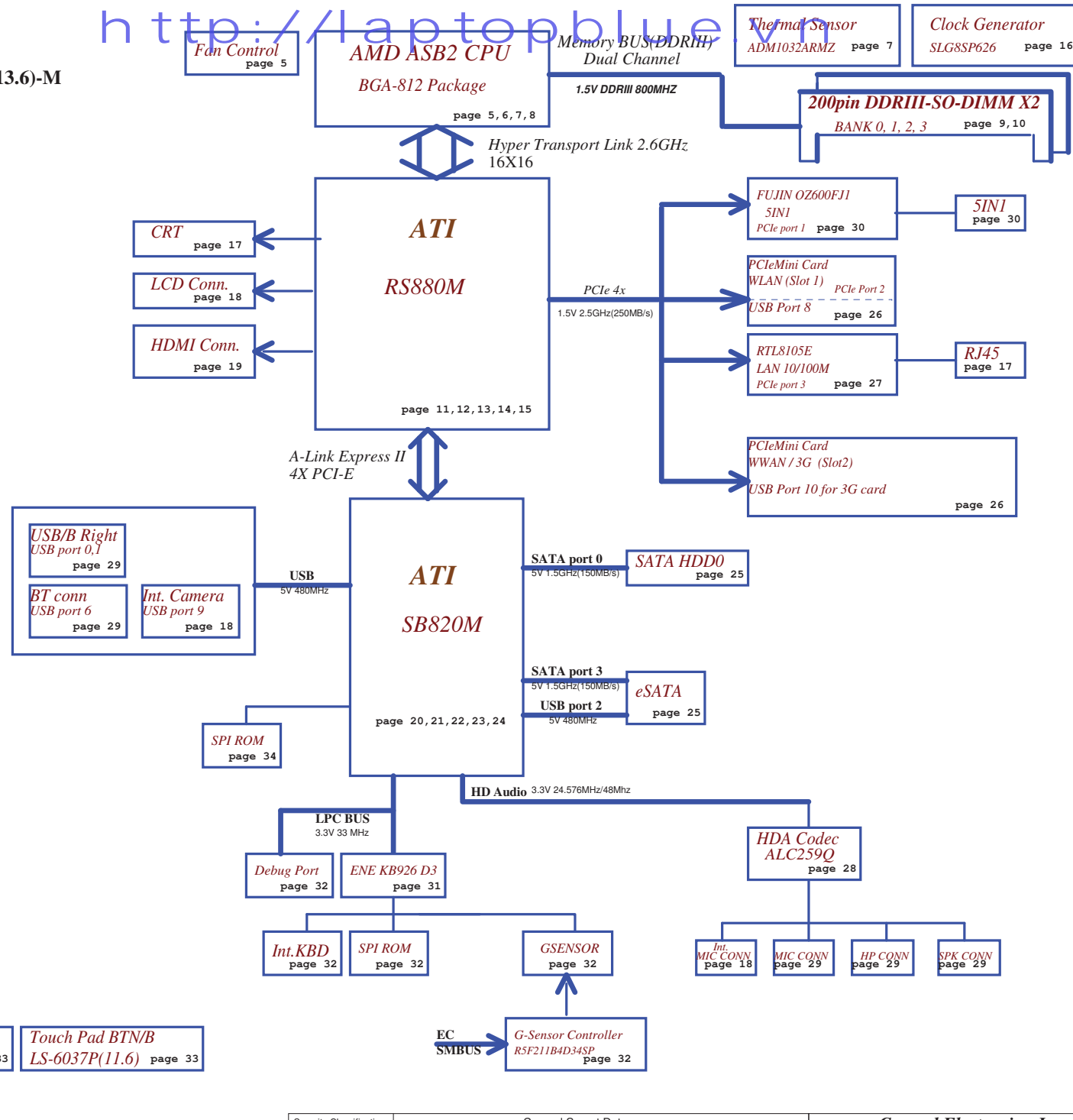
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Issued Date	2008/04/14	Deciphered Date	2009/04/14	Cover Sheet	
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				LA-6032P	1.0
				Date: Tuesday, March 23, 2010	Sheet 1 of 45

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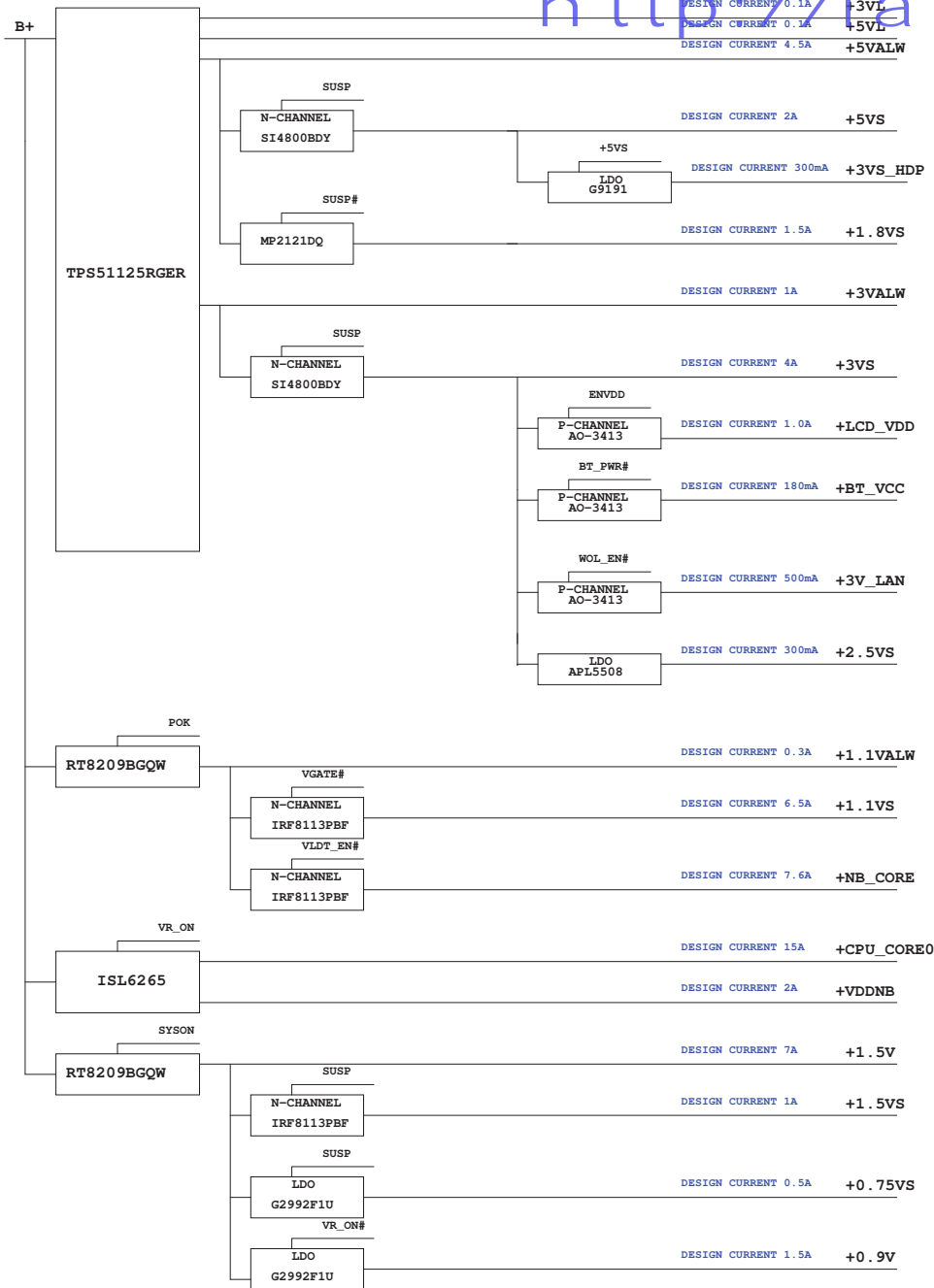
Model Name : NDU01(11.3)-S/NDU11(13.6)-M

File Name : LA-6032P

http://laptopblue



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	Title	Block Diagram
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				Date	Tuesday, March 23, 2010
				Sheet	2 of 45
				Rev	1.0



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				Date:	Tuesday, March 23, 2010	Sheet 3 of 45

Voltage Rails

O MEANS ON X MEANS OFF

power plane State	B+ +3VL +5VL +RTCVC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +0.9VS +0.75VS +NB_CORE +VDDNB +CPU_CORE_0
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

http://laptopblue.vn

Symbol Note



: means Digital Ground



: means Analog Ground

@ : means just reserve , no build
 K625R3@ : means just for 1.5G CPU
 K125R3@ : means just for 1.7G CPU
 K325R3@ : means just for 1.3G CPU
 K625R1@ : means just for 1.5G CPU
 K125R1@ : means just for 1.7G CPU
 K325R1@ : means just for 1.3G CPU
 M@ : means just reserve for 13.3 control
 S@ : means just reserve for 11.6 control
 GSENSOR@ : means just reserve for G sensor part
 1ST@ : means just reserve 1st G sensor IC
 1STGSENSOR@ : means just reserve 1st G sensor IC
 2ND@ : means just reserve 2nd G sensor IC
~~2NDGSENSOR@ : means just reserve 2nd G sensor IC~~
 NOSIDE@ : means just reserve NOSIDE
 SIDE@ : means just reserve SIDE port
 RS880MR1@ : means just for RS880MR1
 RS880MR3@ : means just for RS880MR3
 SB820MR1@ : means just for SB820MR1
 SB820MR3@ : means just for SB820MR3

K625 mean 1.7G CPU

 U1 K625R3@
K125 CPU

For 11.6 and 13.3 DAZ



PCB-MB

K125 mean 1.7G CPU

 U1 K125R1@
K125 CPU

K325 mean 1.3G CPU

 U1 K325R1@
K325 CPU

K125 mean 1.7G CPU

 U1 K125R3@
K125 CPU

K325 mean 1.3G CPU

 U1 K325R3@
K325 CPU

RS880M

 U5 RS880MR3@
RS880M

SB820M

 U7 SB820MR3@
SB820M

SB SM Bus1 Address

SB SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b	+3VALW	WLAN/WIMAX		
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b				
+3VS	Clock Generator	D2 H	1101 0010 b				

EC SM Bus1 Address

EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 011X b	+3VS	CPU_ADM1032-1	98 H	1001 100X b
				+3VS	G-Sensor		

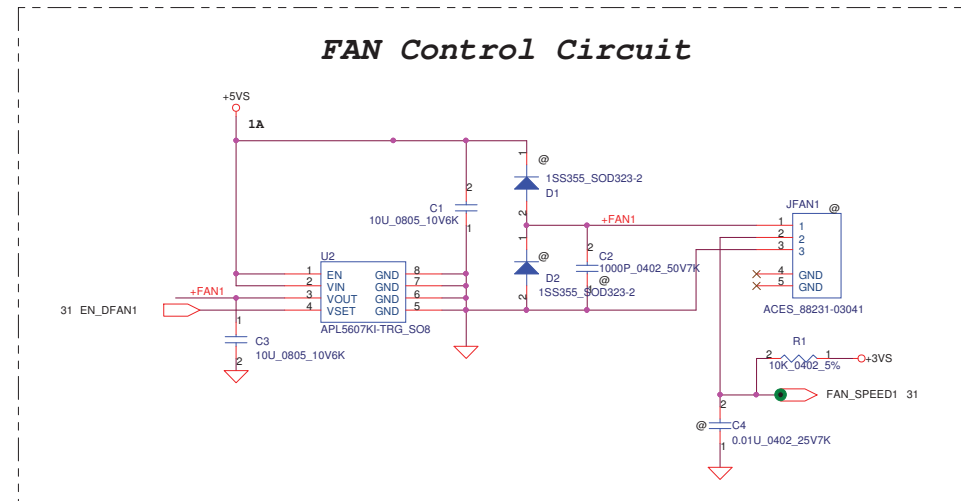
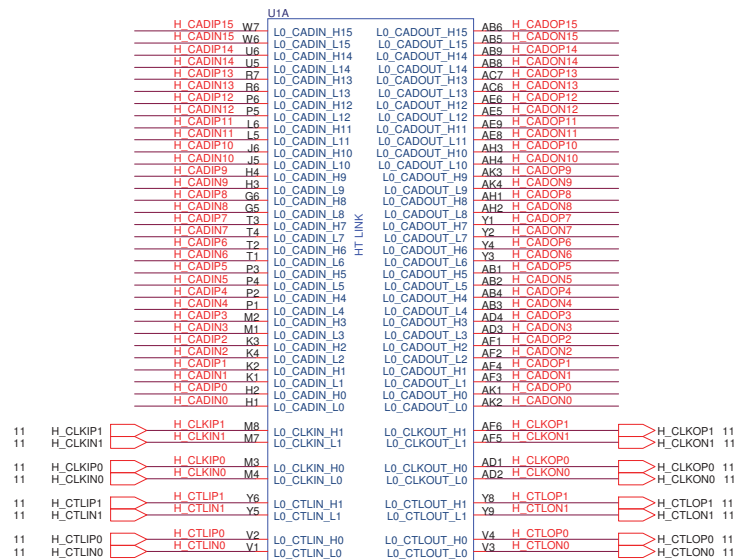
SMBUS Control Table

	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM	G-sensor
EC_SMB_CK1	KB926	V							
EC_SMB_DA1									
EC_SMB_CK2	KB926		V						V
EC_SMB_DA2									
I2C_CLK	RS880M						V		
I2C_DATA									
DDC_CLK0	RS880M							V	
DDC_DATA0									
SCL0	SB820			V	V				
SDA0									
SCL1	SB820								
SDA1						V			

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				Date	Tuesday, March 23, 2010	Sheet 4 of 45

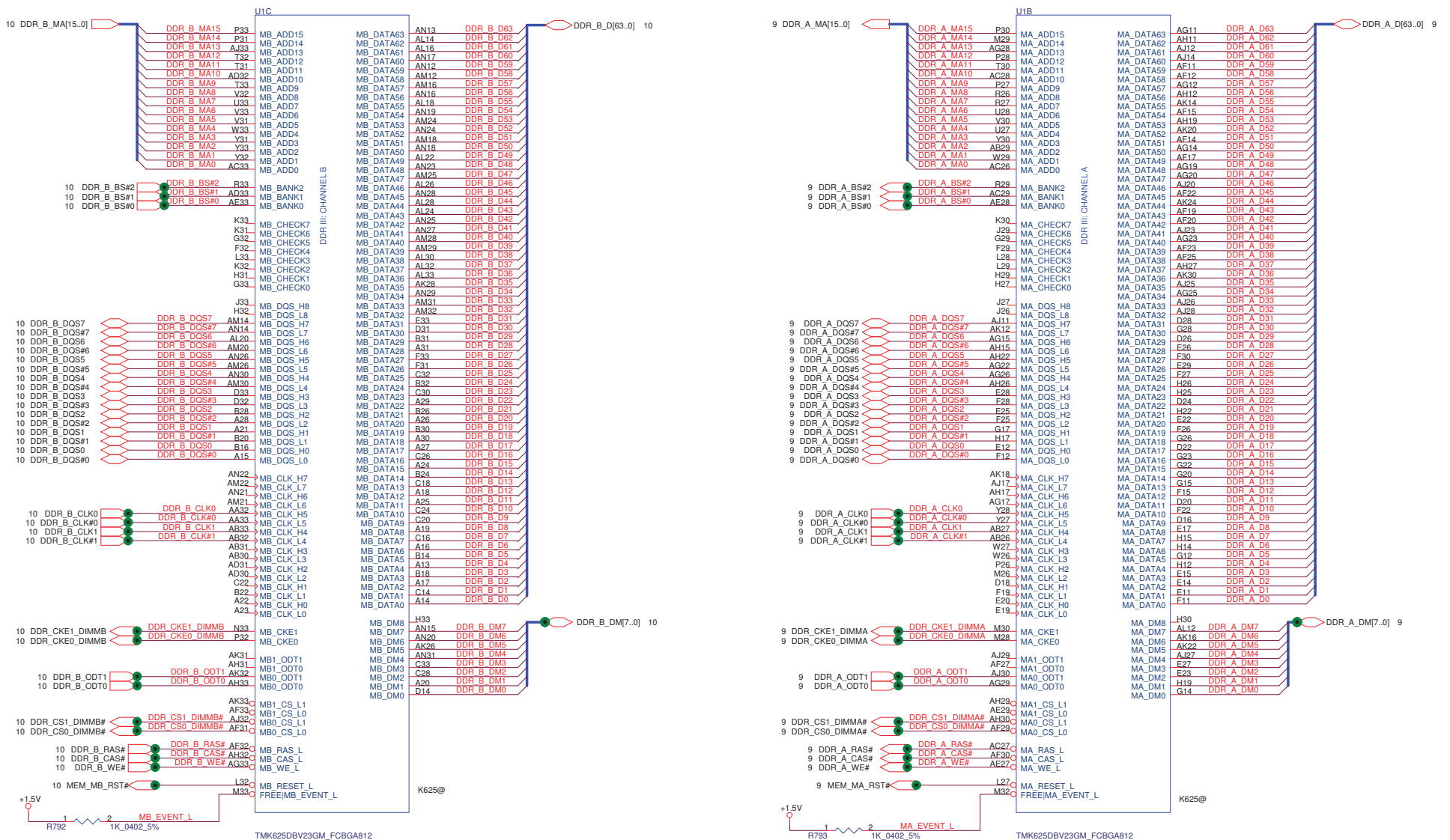
11 H_CADIP[0..15] H_CADIP[0..15]
11 H_CADIN[0..15] H_CADIN[0..15]

H_CADOP[0..15] H_CADOP[0..15]
H_CADON[0..15] H_CADON[0..15]

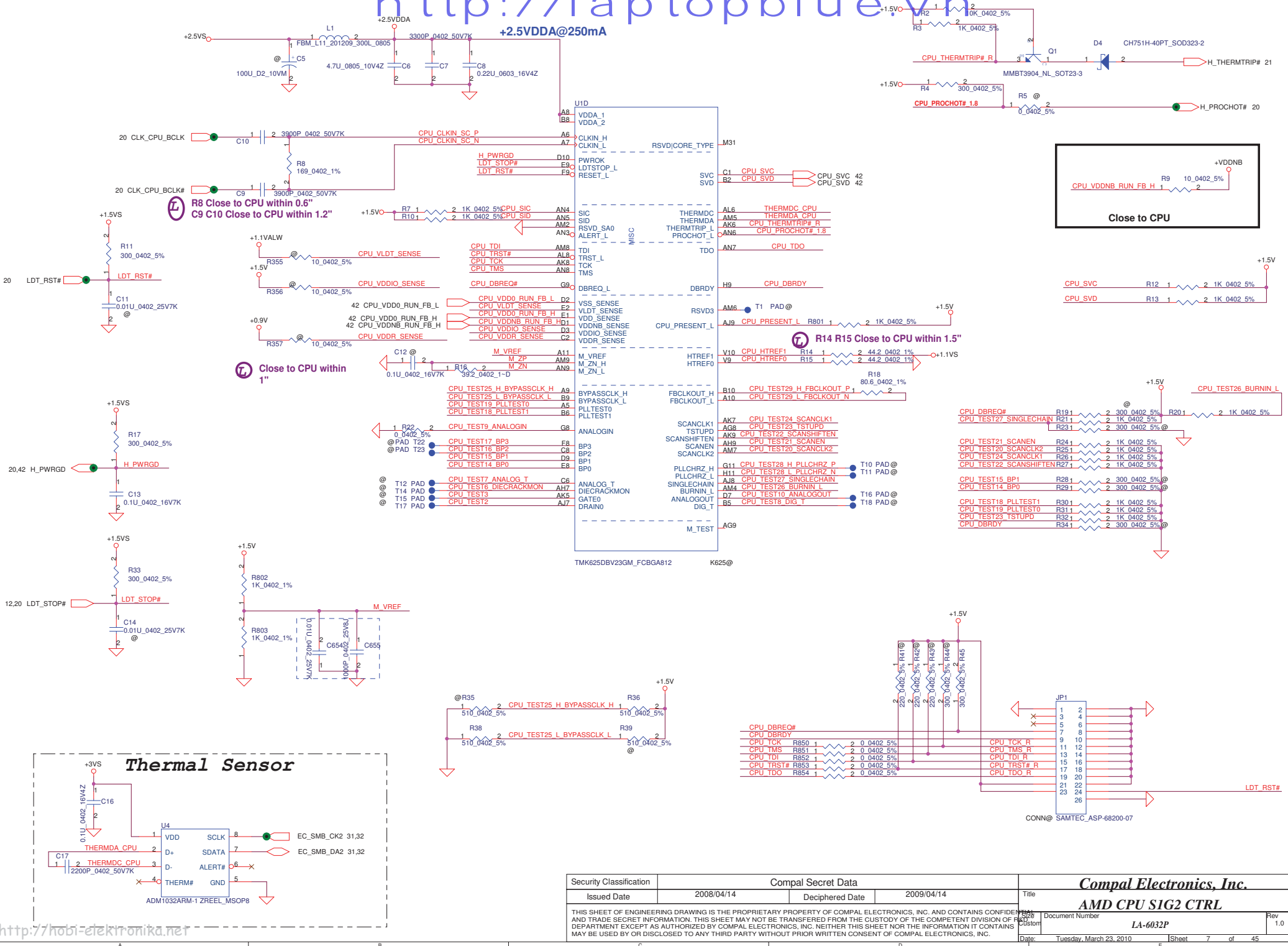


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Date: Tuesday, March 23, 2010				Rev 1.0
Sheet 5 of 45				LA-6032P

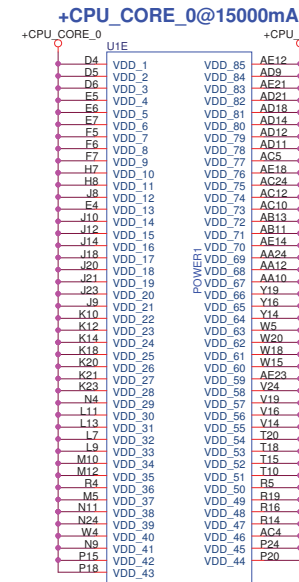
<http://laptopblue.vn>



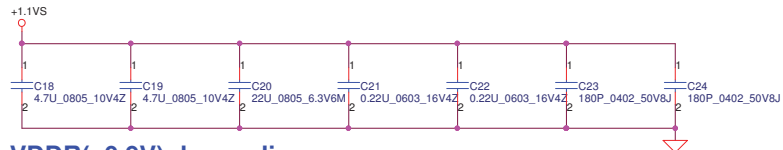
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				Date:	Tuesday, March 23, 2010	Sheet 6 of 45



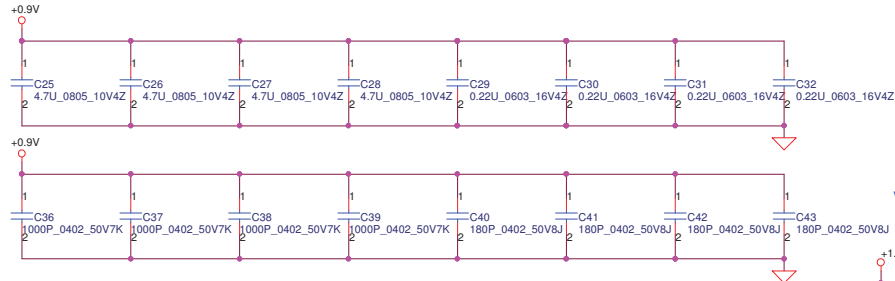
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Issued Date	2008/04/14	Deciphered Date	2009/04/14	AMD CPU SIG2 CTRL	
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Date: Tuesday, March 23, 2010				Sheet	7 of 45



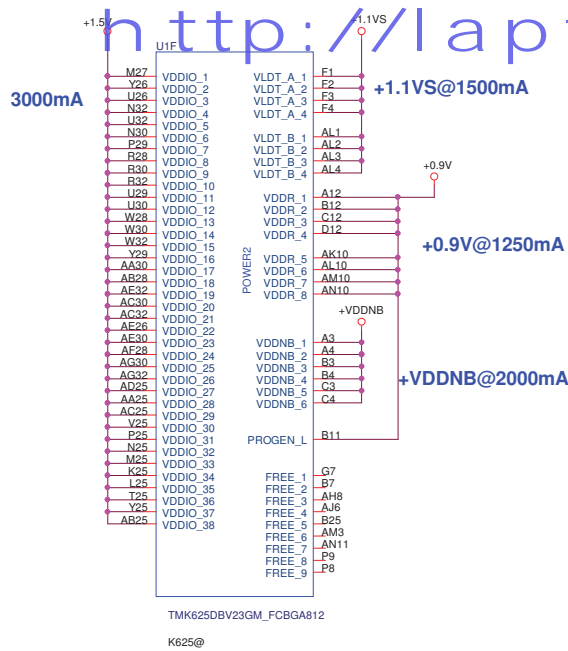
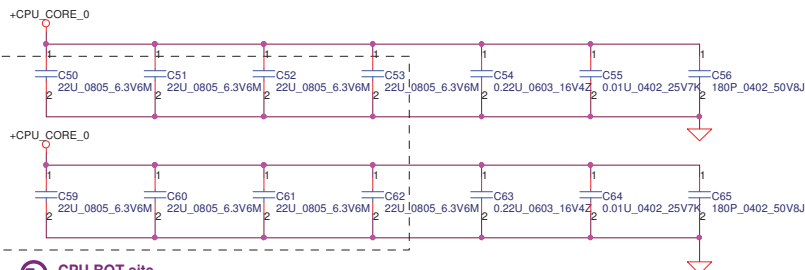
VLDT_A&VLDT_B(+1.1VS) decoupling.



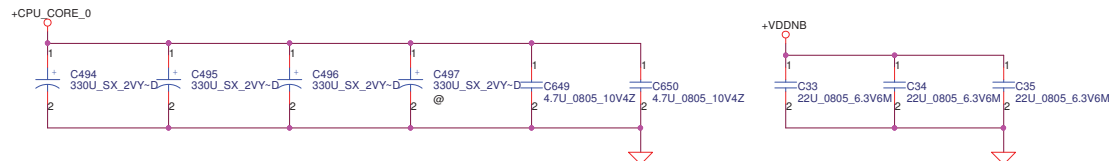
VDDR(+0.9V) decoupling.



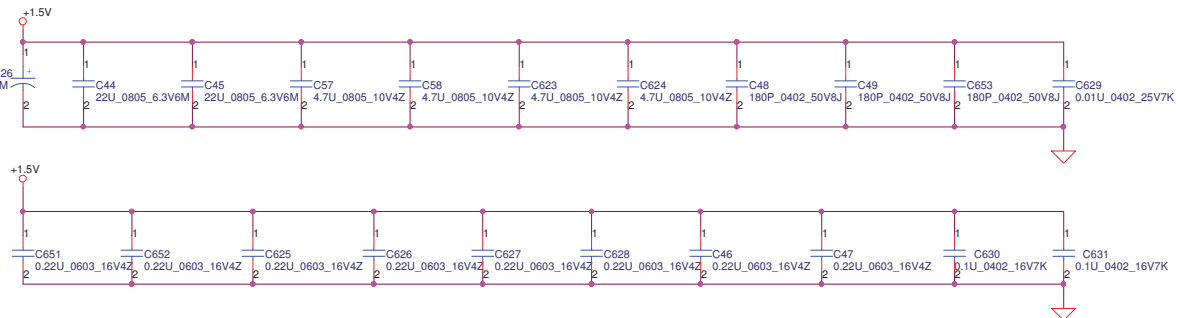
VDD(+CPU_CORE_0) decoupling.



VDD(+CPU_CORE_0) decoupling.



VDDIO(+1.5V) decoupling.

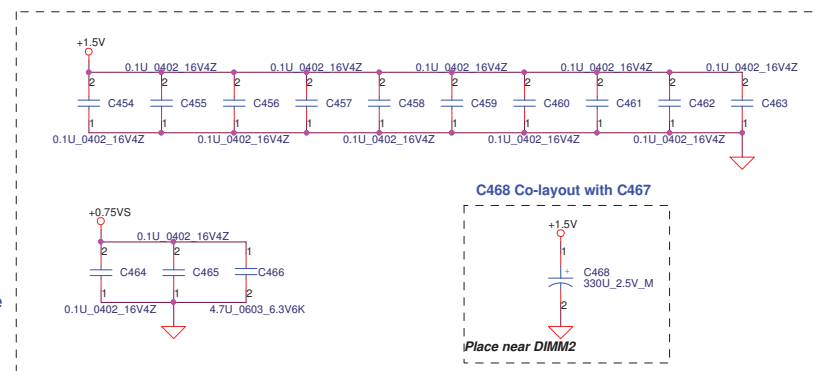
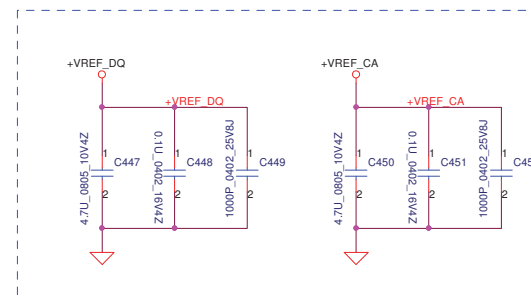
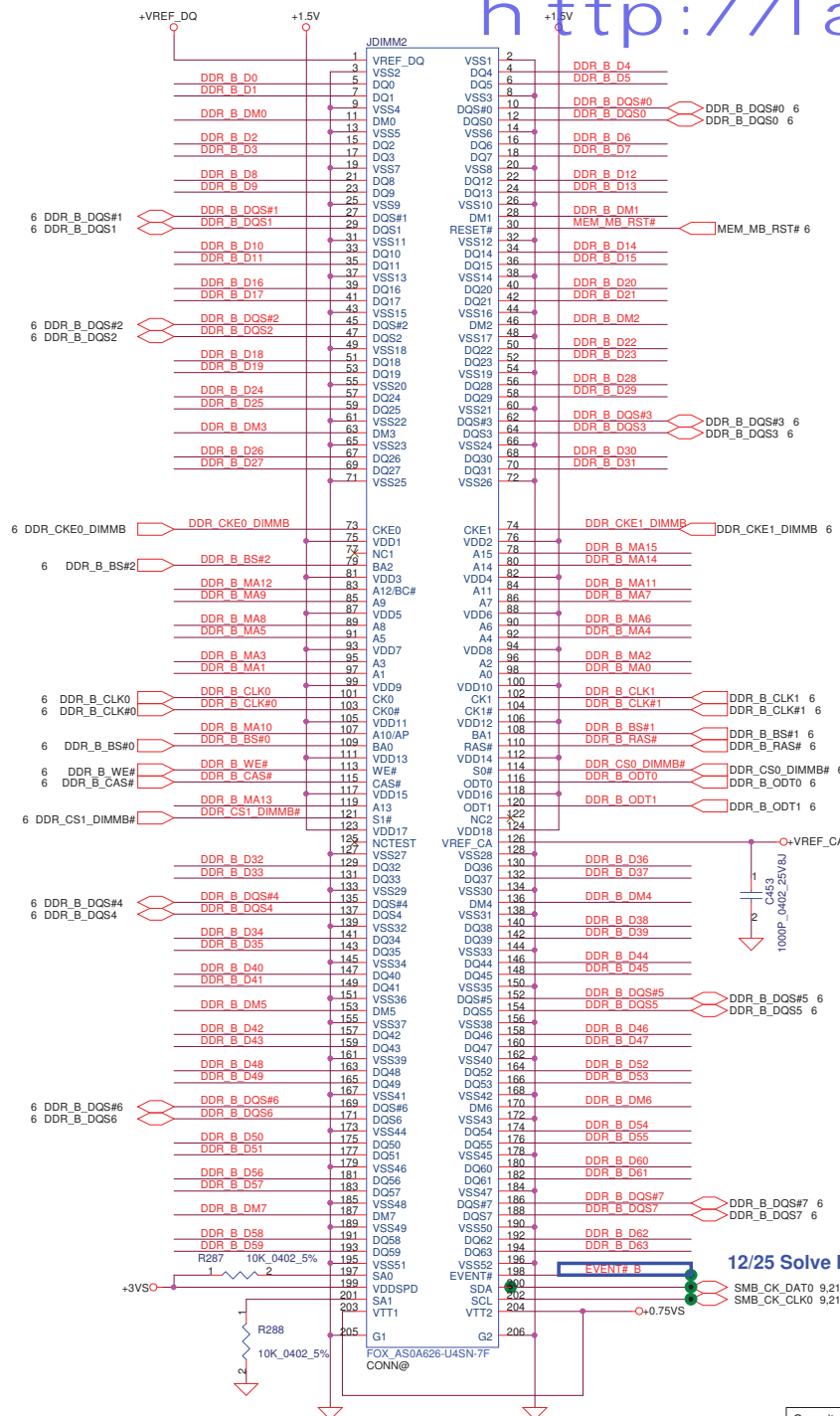


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				Date				Tuesday, March 23, 2010			
				Sheet				8 of 45			

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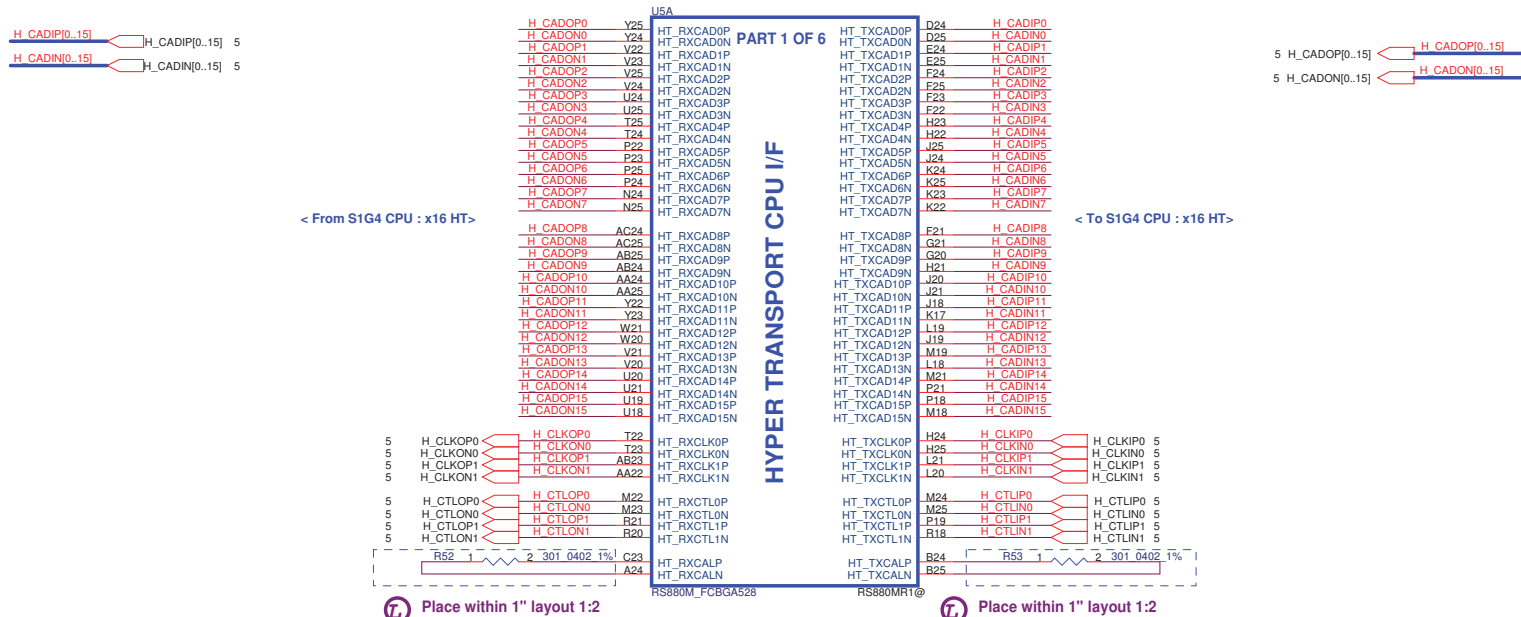
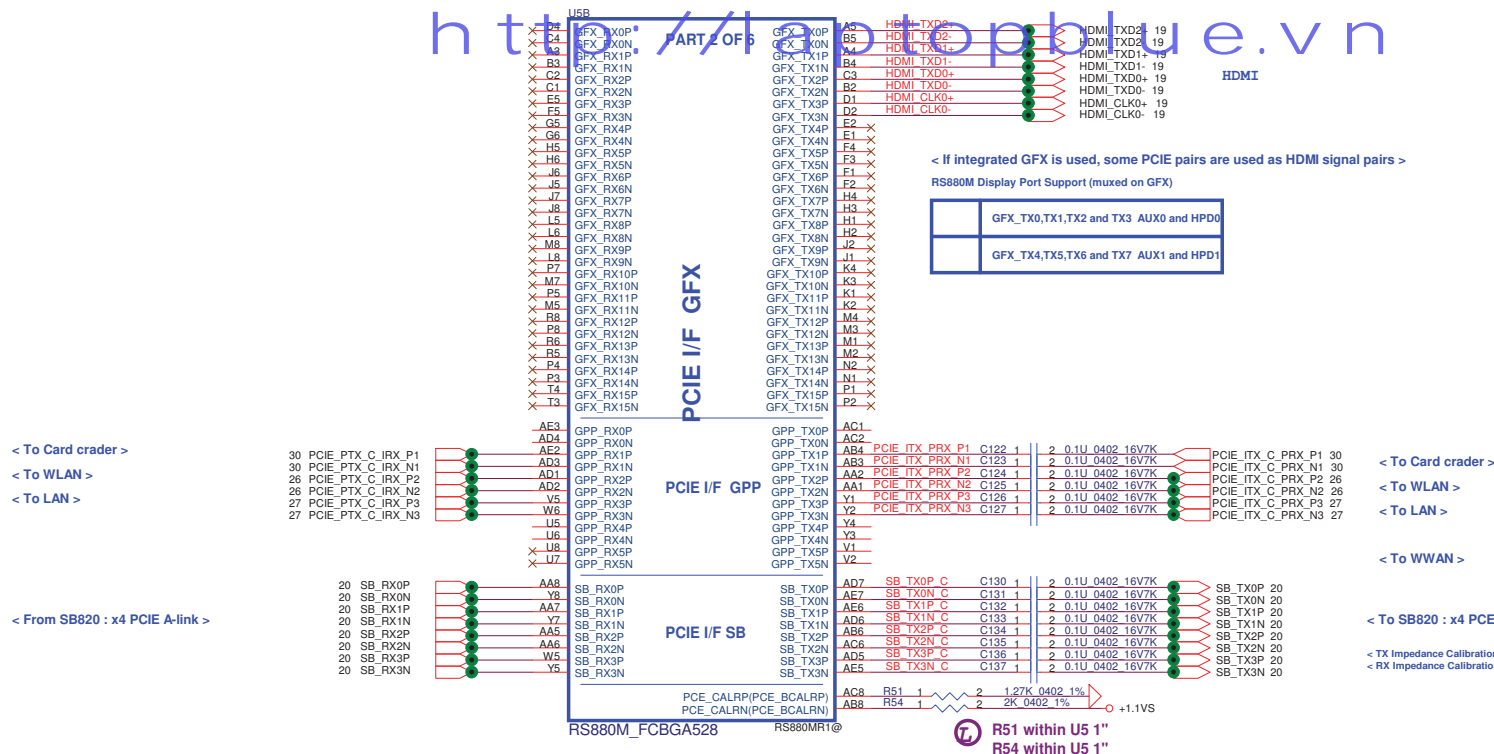


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Issued Date	2008/10/06	Deciphered Date	2010/03/12	Title	DDRII SO-DIMM 1	
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				Custom	LA-6032P	1.0
				Date:	Tuesday, March 23, 2010	Sheet 9 of 45

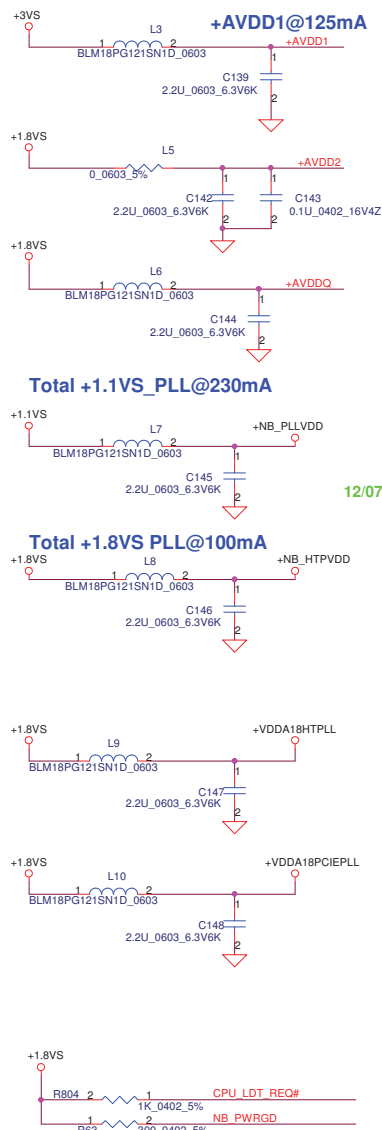


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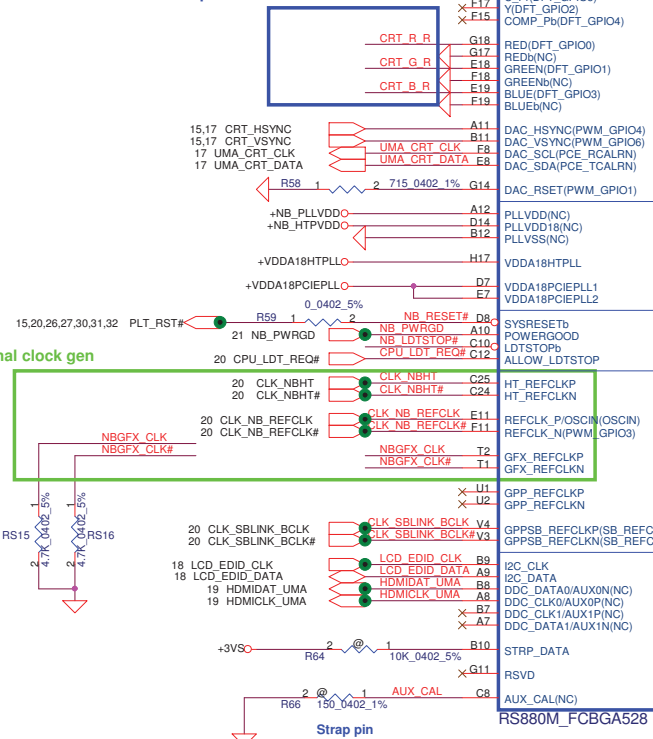
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				LA-6032P	1.0
				Date: Tuesday, March 23, 2010	Sheet 10 of 45



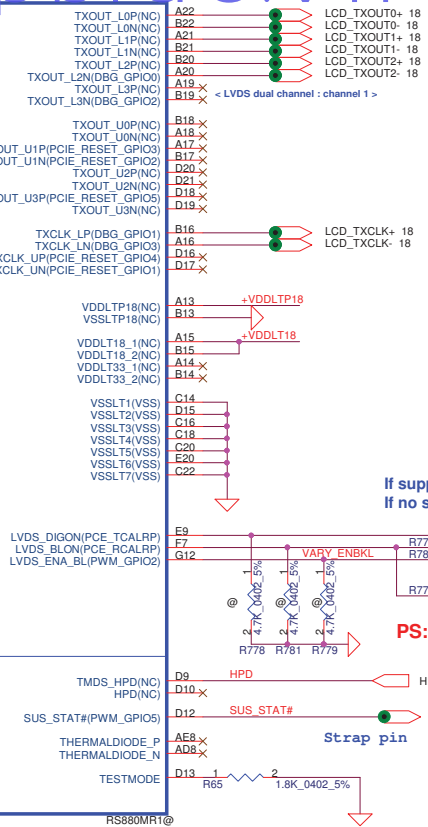
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				LA-6032P	1.0
Date:				Tuesday, March 23, 2010	Sheet 11 of 45



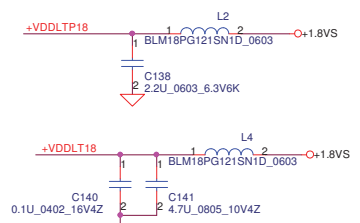
2/2 Fine tune pin define



CRT/TVOUT
LVTM
PM
PLL PWR
CLOCKS
MIS



+VDDT18@220mA



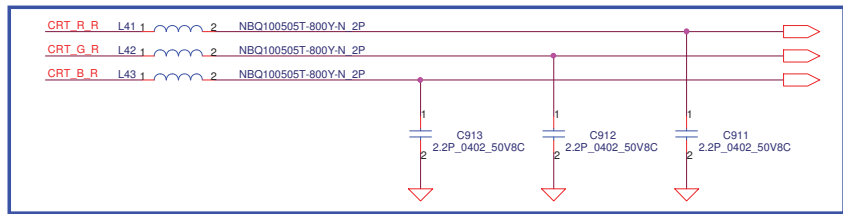
If support VB, R780 R777->SMT, R776->@
If no support VB, R776->SMT, R780 R777->@

PS:Need to fine tune R783 and R784 on Page17

< HDMI hot-plug detection >
< Strap option pin or gate side-port memory IO >

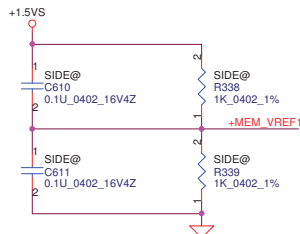
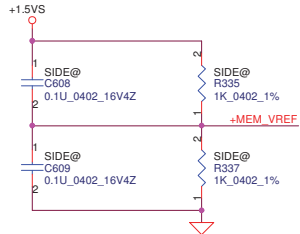
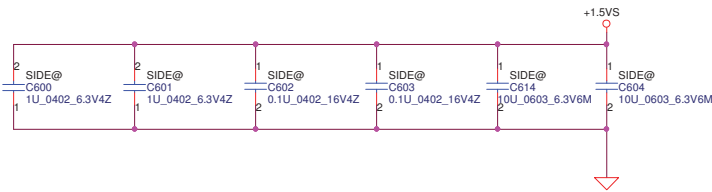
Contact with NB signal

Contact to CRT conn signal



2/2 Add L41 L42 L43 C911 C912 C913 for EMI request

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Issued Date	2008/04/14	Deciphered Date	2009/04/14	RS880M VEDIO/CLK GEN	
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				LA-6032P	
				Tuesday, March 23, 2010	Sheet 12 of 45



MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions

For Side port only

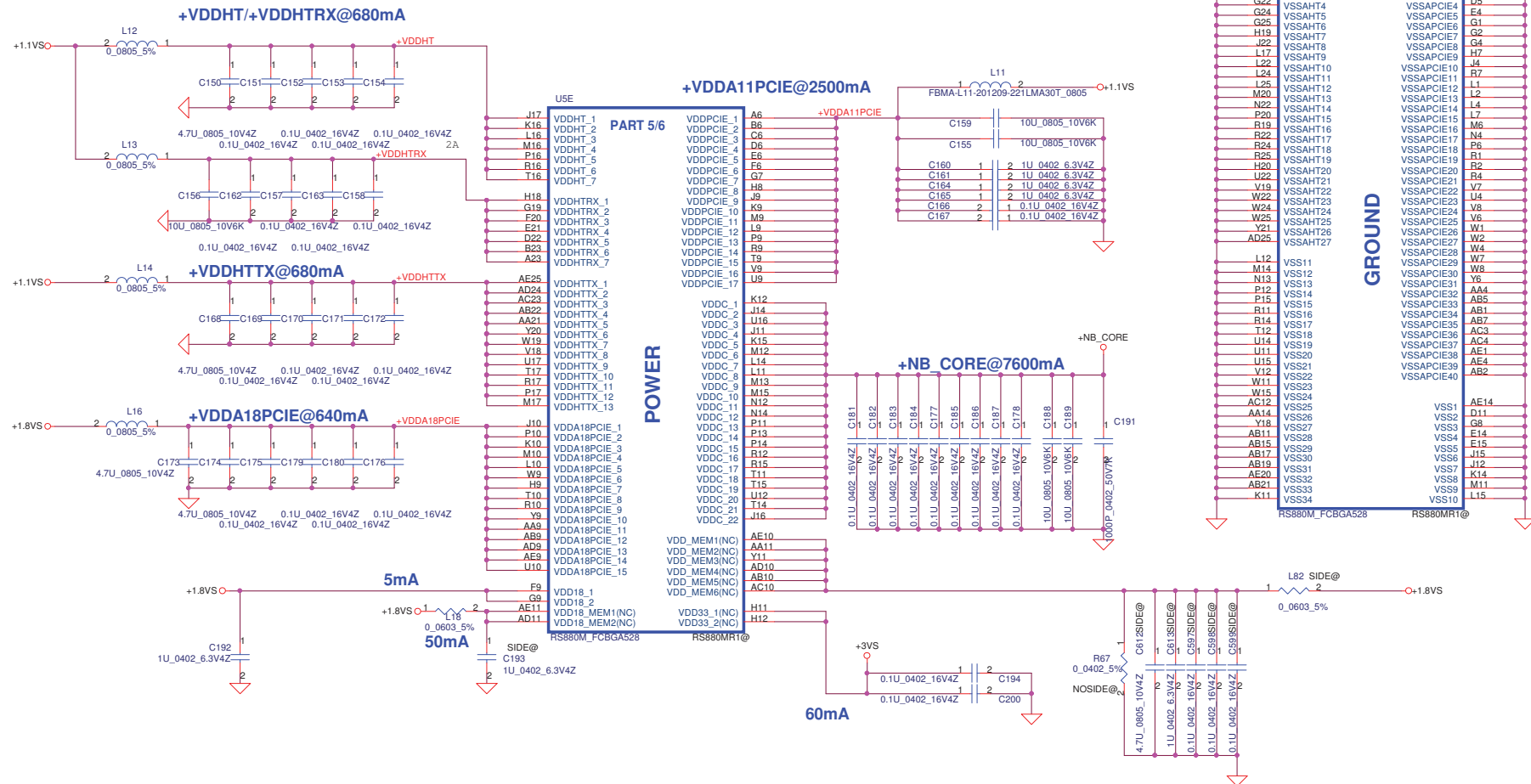


MEM_A0	AB12	MEM_A0(1NC)	MEM_DQ0/DV0_VSYNC(1NC)	AA18	MEM_DQ0
MEM_A1	AE16	MEM_A1(1NC)	MEM_DQ1/DV0_HS(1NC)	AA20	MEM_DQ1
MEM_A2	V11	MEM_A2(1NC)	MEM_DQ2/DV0_DE(1NC)	AA19	MEM_DQ2
MEM_A3	AA12	MEM_A3(1NC)	MEM_DQ3/DV0_D0(1NC)	Y19	MEM_DQ3
MEM_A4	AB16	MEM_A4(1NC)	MEM_DQ4/DV0_D1(1NC)	Y17	MEM_DQ4
MEM_A5	AD14	MEM_A5(1NC)	MEM_DQ5/DV0_D2(1NC)	AA17	MEM_DQ5
MEM_A6	AD15	MEM_A6(1NC)	MEM_DQ6/DV0_D3(1NC)	AA15	MEM_DQ6
MEM_A7	AC16	MEM_A7(1NC)	MEM_DQ7/DV0_D4(1NC)	Y15	MEM_DQ7
MEM_A8	AD13	MEM_A8(1NC)	MEM_DQ8/DV0_D5(1NC)	AC20	MEM_DQ8
MEM_A9	AC15	MEM_A9(1NC)	MEM_DQ9/DV0_D6(1NC)	AD19	MEM_DQ9
MEM_A10	AE13	MEM_A10(1NC)	MEM_DQ10/DV0_D7(1NC)	AE22	MEM_DQ10
MEM_A11	Y14	MEM_A11(1NC)	MEM_DQ11/DV0_D8(1NC)	AC18	MEM_DQ11
MEM_A12	AD17	MEM_A12(1NC)	MEM_DQ12/DV0_D9(1NC)	AB20	MEM_DQ12
MEM_A13	Y14	MEM_A13(1NC)	MEM_DQ13/DV0_D10(1NC)	AD22	MEM_DQ13
MEM_BA0	AD16	MEM_BA0(1NC)	MEM_DQ14/DV0_D11(1NC)	AC22	MEM_DQ14
MEM_BA1	AE17	MEM_BA1(1NC)		AD21	MEM_DQ15
MEM_BA2	AD17	MEM_BA2(1NC)			
MEM_RAS#	W12	MEM_RAS(1NC)		Y17	MEM_DQS_P0
MEM_CAS#	Y12	MEM_CAS(1NC)		W18	MEM_DQS_N0
MEM_WE#	AD18	MEM_WE(1NC)		AD20	MEM_DQS_P1
MEM_CS#	AB13	MEM_CS(1NC)		AE21	MEM_DQS_N1
MEM_CKE	AB18	MEM_CKE(1NC)		W17	MEM_DM0
MEM_ODT	V14	MEM_ODT(1NC)		AE19	MEM_DM1
MEM_CLKP	V15	MEM_CLKP(1NC)			
MEM_CLKN	W14	MEM_CLKN(1NC)			
MEM_COMP_P	AE12	MEM_COMP(1NC)		AE23	+1.8V IOPLLVDD
MEM_COMP_N	AD12	MEM_COMP(1NC)		AE24	+NB IOPLLVDD

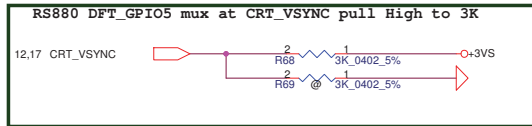
MEM_A0	N4	MEM_A0	DQ0	MEM_DQ0
MEM_A1	P8	MEM_A1	DQ1	MEM_DQ1
MEM_A2	P4	MEM_A2	DQ2	MEM_DQ2
MEM_A3	N3	MEM_A3	DQ3	MEM_DQ3
MEM_A4	P9	MEM_A4	DQ4	MEM_DQ4
MEM_A5	P3	MEM_A5	DQ5	MEM_DQ5
MEM_A6	R9	MEM_A6	DQ6	MEM_DQ6
MEM_A7	R3	MEM_A7	DQ7	MEM_DQ7
MEM_A8	T9	MEM_A8	DQ8	MEM_DQ8
MEM_A9	R4	MEM_A9	DQ9	MEM_DQ9
MEM_A10	L8	MEM_A10	DQ10	MEM_DQ10
MEM_A11	R8	MEM_A11	DQ11	MEM_DQ11
MEM_A12	N8	MEM_A12	DQ12	MEM_DQ12
MEM_A13	T4	MEM_A13	DQ13	MEM_DQ13

MEM_BA0	M3	MEM_BA0	DQ14	MEM_DQ14
MEM_BA1	N9	MEM_BA1	DQ15	MEM_DQ15
MEM_BA2	M4	MEM_BA2	DQ16	MEM_DQ16
MEM_CLKP	J8	MEM_CLKP	DQ17	MEM_DQ17
MEM_CLKN	K8	MEM_CLKN	DQ18	MEM_DQ18
MEM_CKE	K10	MEM_CKE	DQ19	MEM_DQ19
MEM_ODT	K2	MEM_ODT	DQ20	MEM_DQ20
MEM_CS#	L3	MEM_CS#	DQ21	MEM_DQ21
MEM_RAS#	J4	MEM_RAS#	DQ22	MEM_DQ22
MEM_CAS#	K4	MEM_CAS#	DQ23	MEM_DQ23
MEM_WE#	L4	MEM_WE#	DQ24	MEM_DQ24
MEM_DQS_P0	F4	MEM_DQS_P0	DQ25	MEM_DQ25
MEM_DQS_P1	C8	MEM_DQS_P1	DQ26	MEM_DQ26
MEM_DM0	E8	MEM_DM0	DQ27	MEM_DQ27
MEM_DM1	D4	MEM_DM1	DQ28	MEM_DQ28
MEM_DQS_N0	G4	MEM_DQS_N0	DQ29	MEM_DQ29
MEM_DQS_N1	B8	MEM_DQS_N1	DQ30	MEM_DQ30

MEM_DM0	E8	MEM_DM0	DQ31	MEM_DQ31
MEM_DM1	D4	MEM_DM1	DQ32	MEM_DQ32
MEM_DQS_N0	G4	MEM_DQS_N0	DQ33	MEM_DQ33
MEM_DQS_N1	B8	MEM_DQS_N1	DQ34	MEM_DQ34
MEM_CLKP	J8	MEM_CLKP	DQ35	MEM_DQ35
MEM_CLKN	K8	MEM_CLKN	DQ36	MEM_DQ36
MEM_CKE	K10	MEM_CKE	DQ37	MEM_DQ37
MEM_ODT	K2	MEM_ODT	DQ38	MEM_DQ38
MEM_CS#	L3	MEM_CS#	DQ39	MEM_DQ39
MEM_RAS#	J4	MEM_RAS#	DQ40	MEM_DQ40
MEM_CAS#	K4	MEM_CAS#	DQ41	MEM_DQ41
MEM_WE#	L4	MEM_WE#	DQ42	MEM_DQ42
MEM_DQS_P0	F4	MEM_DQS_P0	DQ43	MEM_DQ43
MEM_DQS_P1	C8	MEM_DQS_P1	DQ44	MEM_DQ44
MEM_DM0	E8	MEM_DM0	DQ45	MEM_DQ45
MEM_DM1	D4	MEM_DM1	DQ46	MEM_DQ46
MEM_DQS_N0	G4	MEM_DQS_N0	DQ47	MEM_DQ47
MEM_DQS_N1	B8	MEM_DQS_N1	DQ48	MEM_DQ48



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				LA-6032P	1.0
Date:		Tuesday, March 23, 2010		Sheet	14 of 45



DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

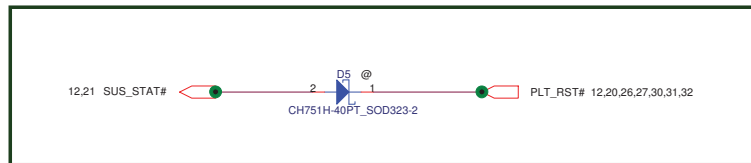
1 : Disable (RS880) ☐
 0 : Enable (RS880)
 PIN: RS880-->VSYNC#

RS780 use register to control PCI-E configure

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.

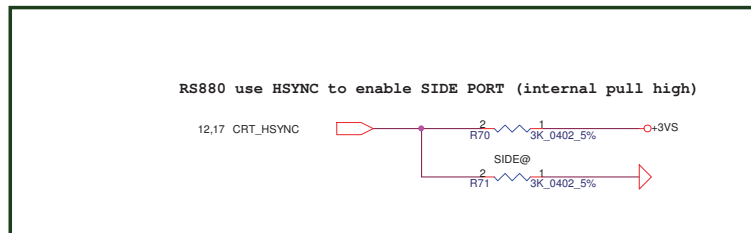
000 : 00001
 001 : 00010
 010 : 01011
 011 : 00100
 100 : 01010
 101 : 01100
 111 : 01011



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RS880:SUS_STAT#



DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

RX881: Enables the Test Debug Bus using PCIE bus

1 : Disable (Can still be enabled using nbcfg register access)
 0 : Enable

RS880: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS880) ☐
 0 : Enable (RS880)

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				LA-6032P	1.0
				Date: Tuesday, March 23, 2010	Sheet 15 of 45

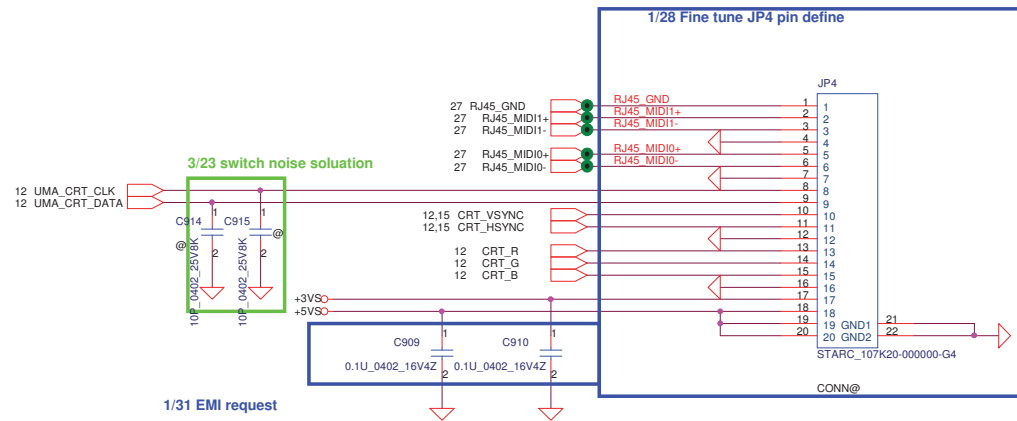
Use SB820M internal clock gen

http://laptopblue.vn

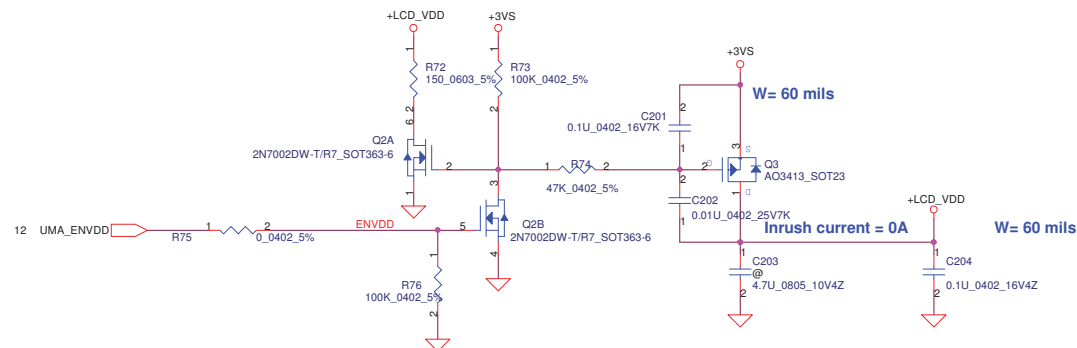
Security Classification		Compal Secret Data		Title	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	CLOCK GENERATOR	
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				LA-6051P	1.0
Date: Tuesday, March 23, 2010				Sheet	16 of 45

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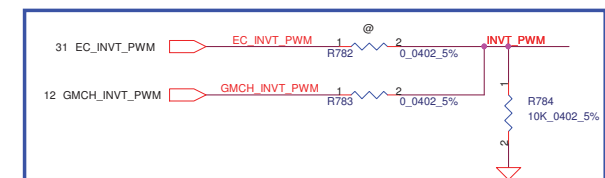
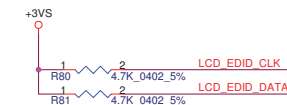
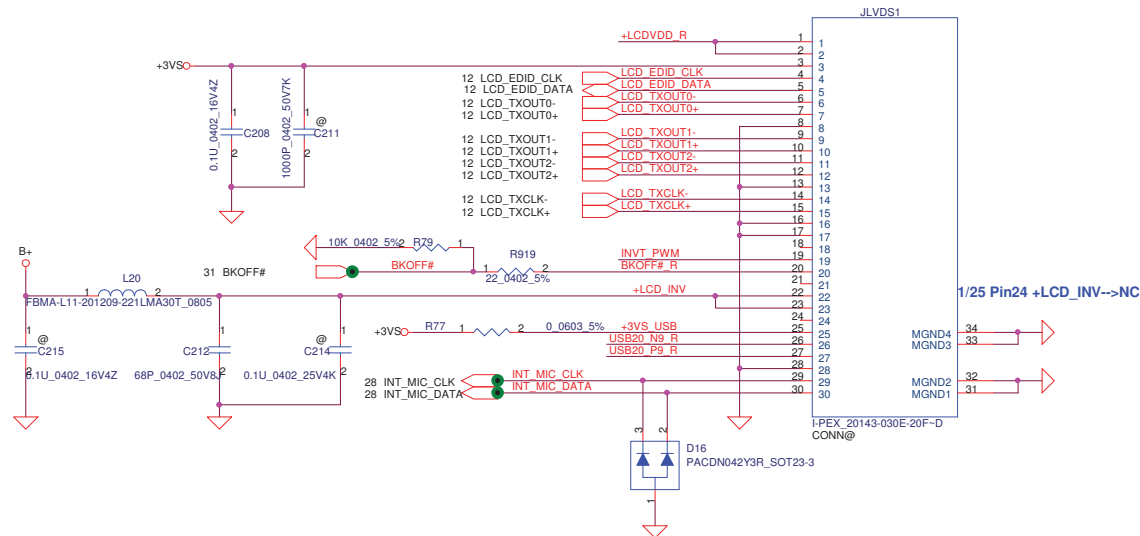
CRT+RJ45 FFC conn
Pin=20pin, pitch=0.5



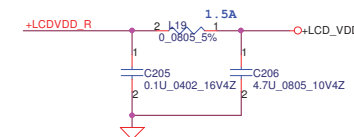
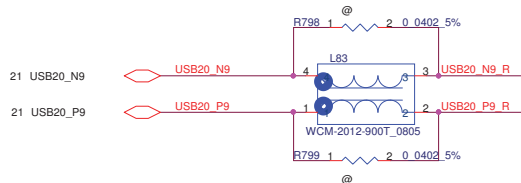
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	CRT/TV-OUT Connector	
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				LA-6032P	1.0
				Date: Tuesday, March 23, 2010	Sheet 17 of 45



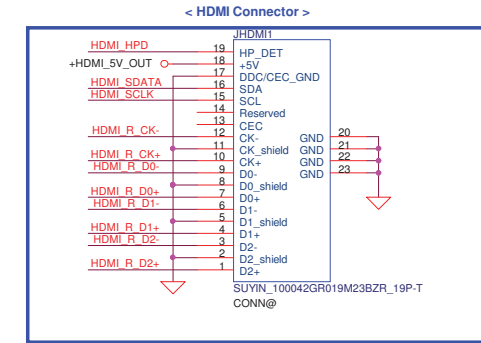
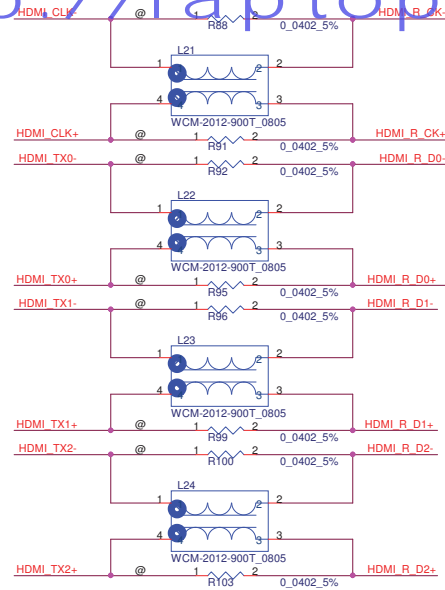
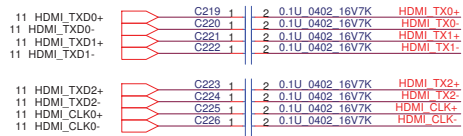
< LVDS Connector >



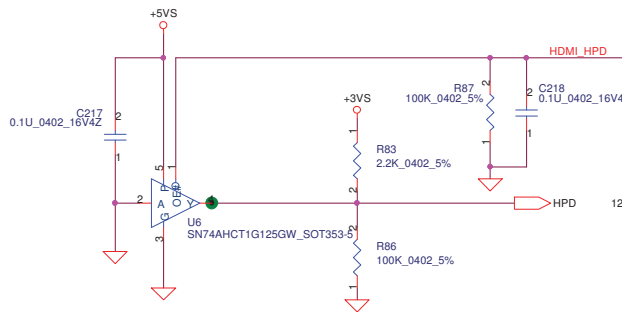
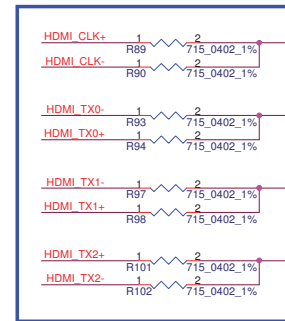
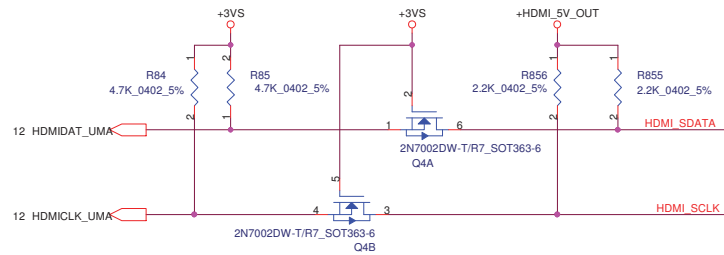
1/19 R782-->@ and R783/R784-->SMT for VB function



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2009/04/14				Title				LCD CONN.			
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Date:				Tuesday, March 23, 2010				Sheet 18 of 45			
Rev 1.0											



1/28 Update JHDMI1 footprint



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Document Number				LA-6032P
Date				Tuesday, March 23, 2010
Sheet				19 of 45

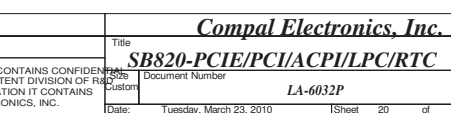
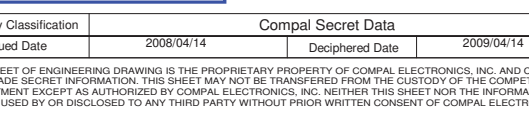
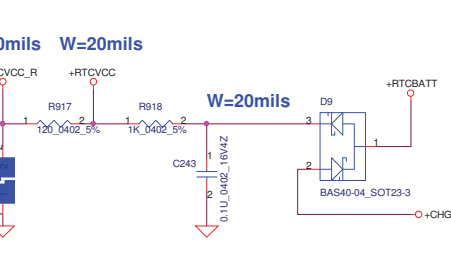
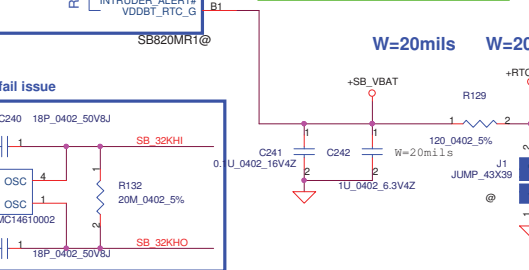
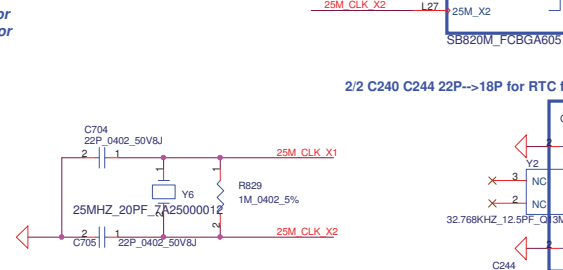
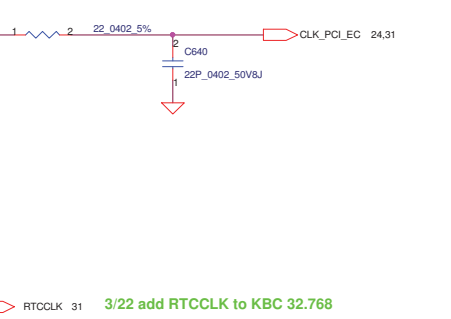
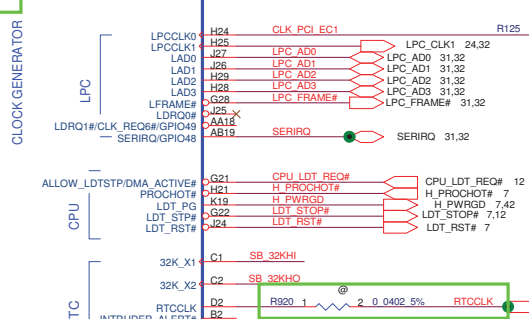
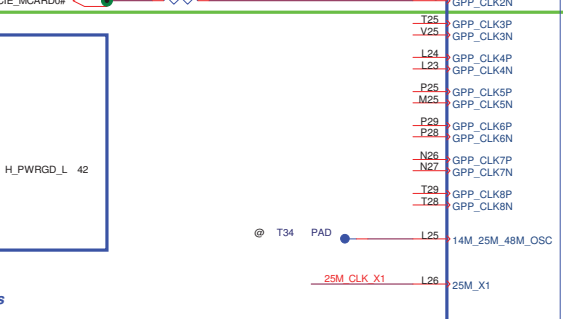
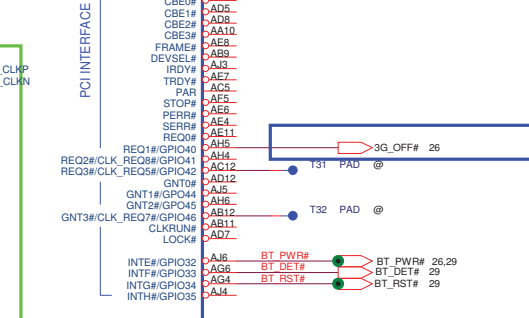
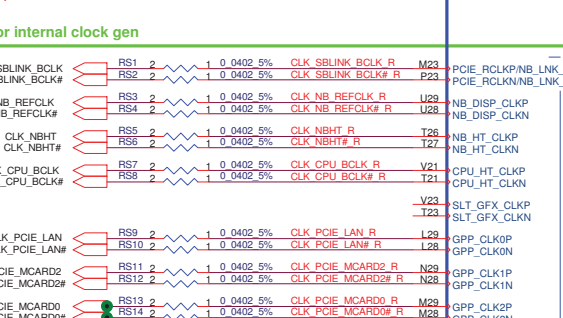
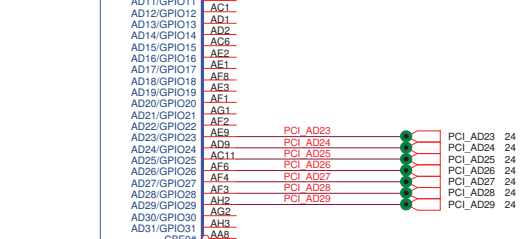
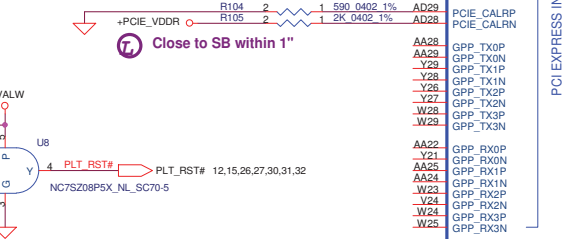
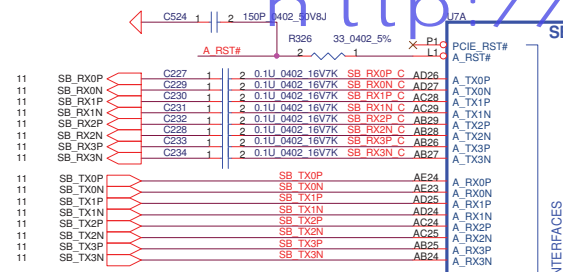
Compal Electronics, Inc.

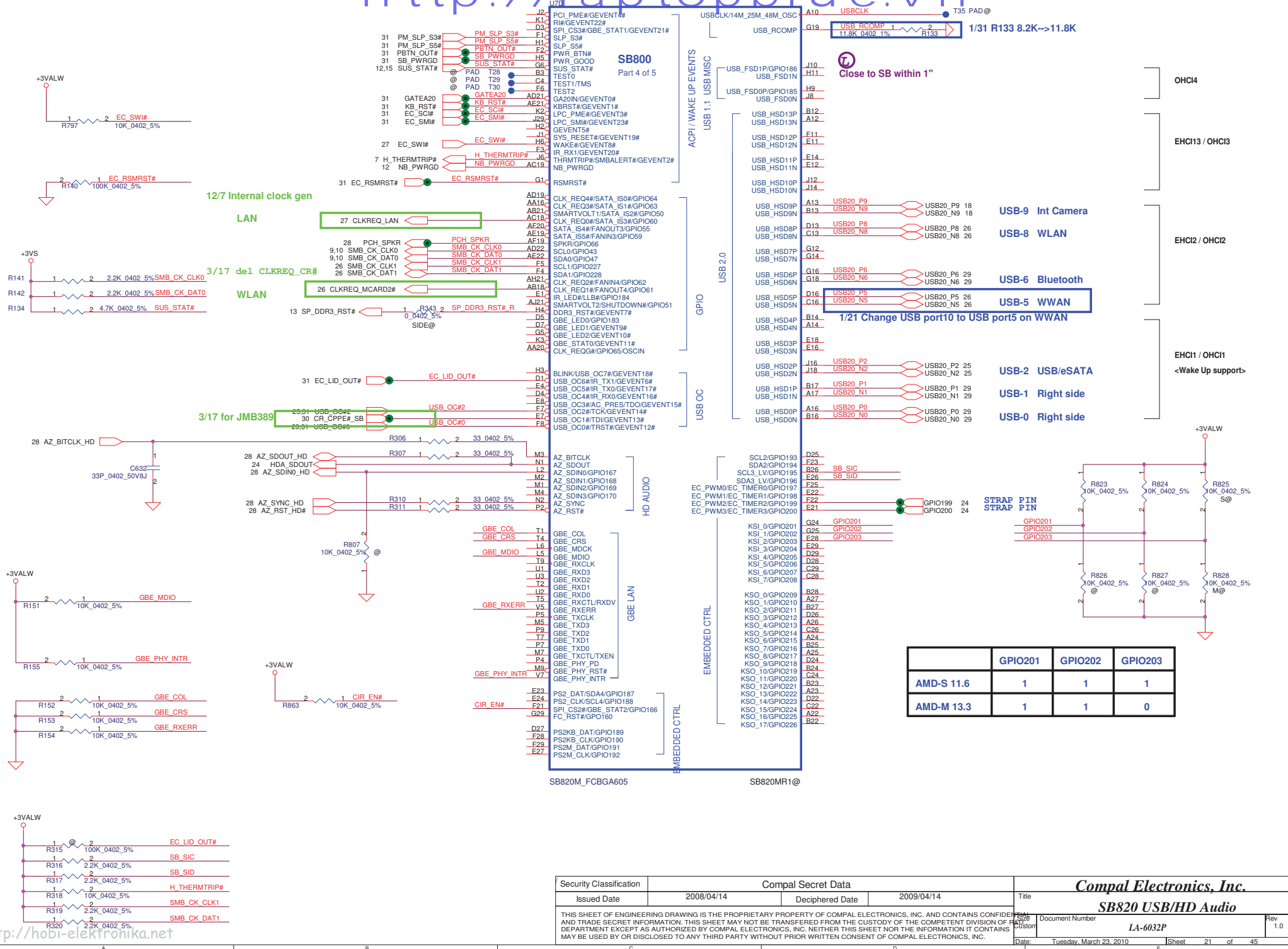
HDMI/CEC

LA-6032P

Rev 1.0

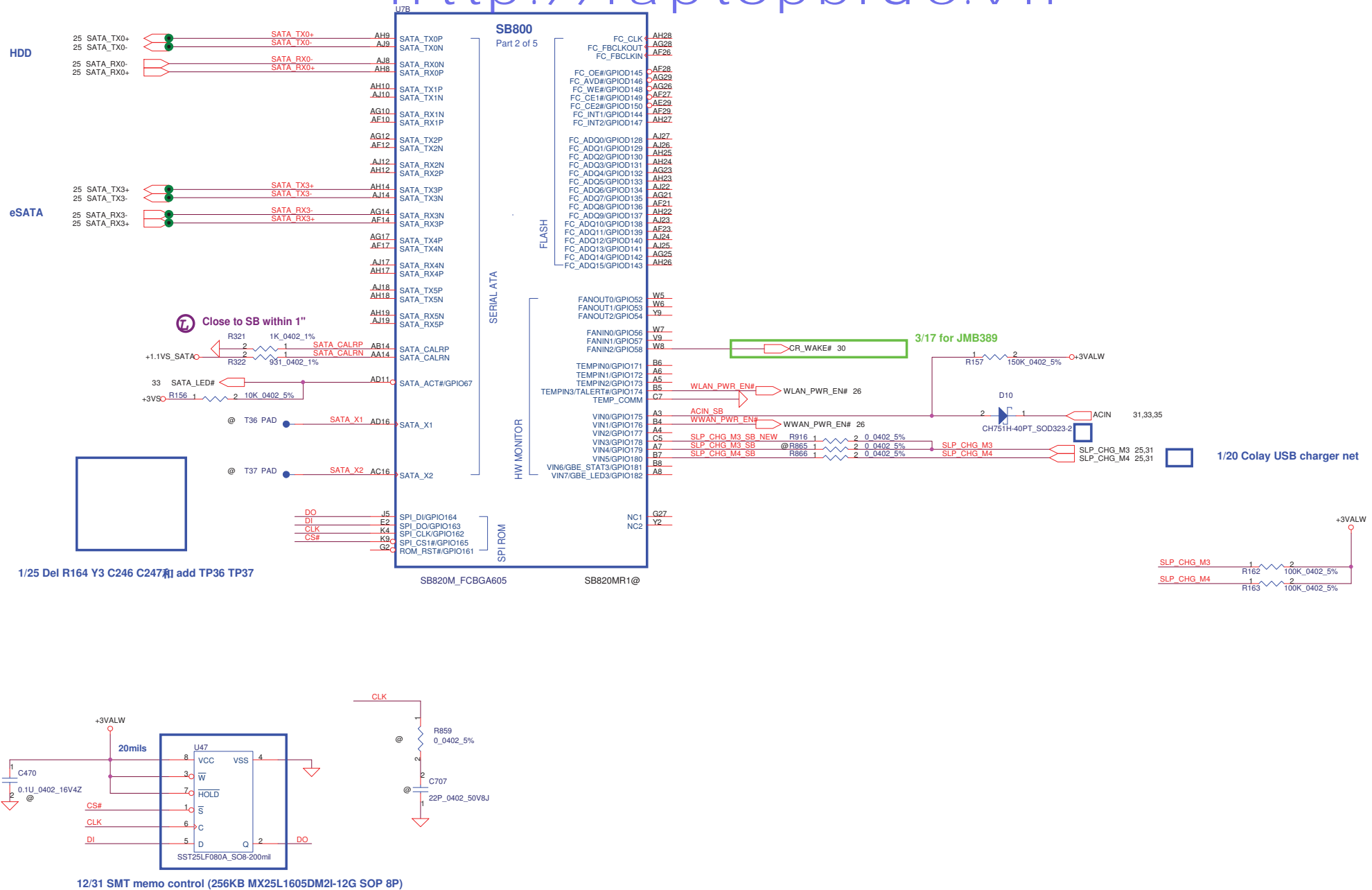
Sheet 19 of 45



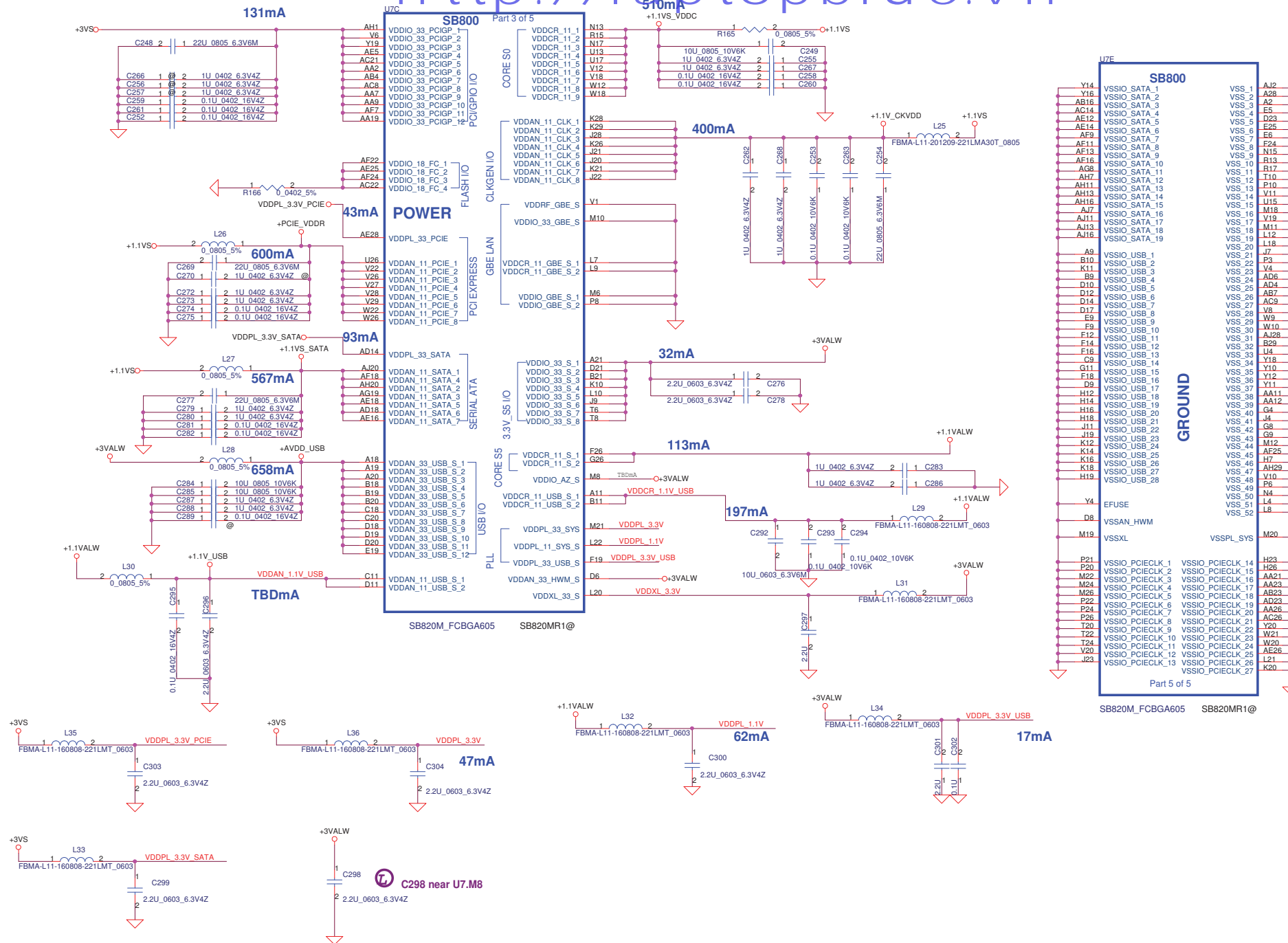


	GPIO201	GPIO202	GPIO203
AMD-S 11.6	1	1	1
AMD-M 13.3	1	1	0

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2008/04/14	Deciphered Date	2009/04/14	Title	SB820 USB/HD Audio	
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				Date:	Tuesday, March 23, 2010	Sheet 21 of 45



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						Document Number		LA-6032P		Rev 1.0	
						Date: Tuesday, March 23, 2010		Sheet 22 of 45			



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				LA-6032P	1.0
Date:		Tuesday, March 23, 2010		Sheet	23 of 45

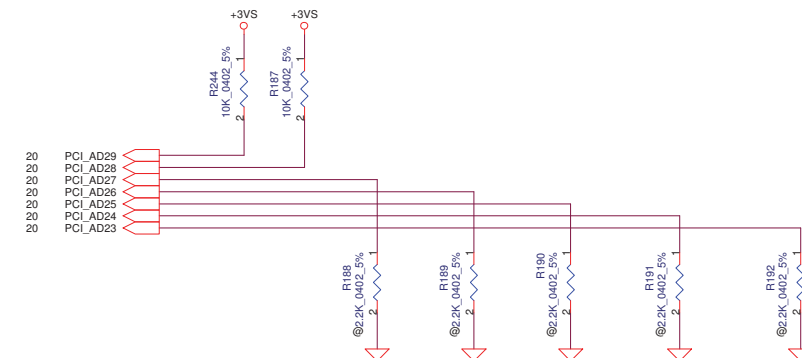
L,H = LPC ROM(Default)
Option 1:SPI Flash (2MB*1) for EC

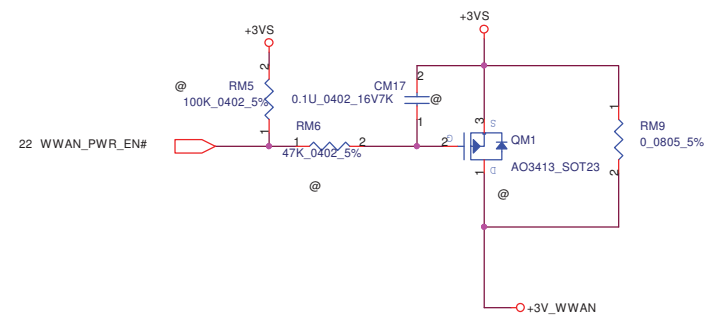
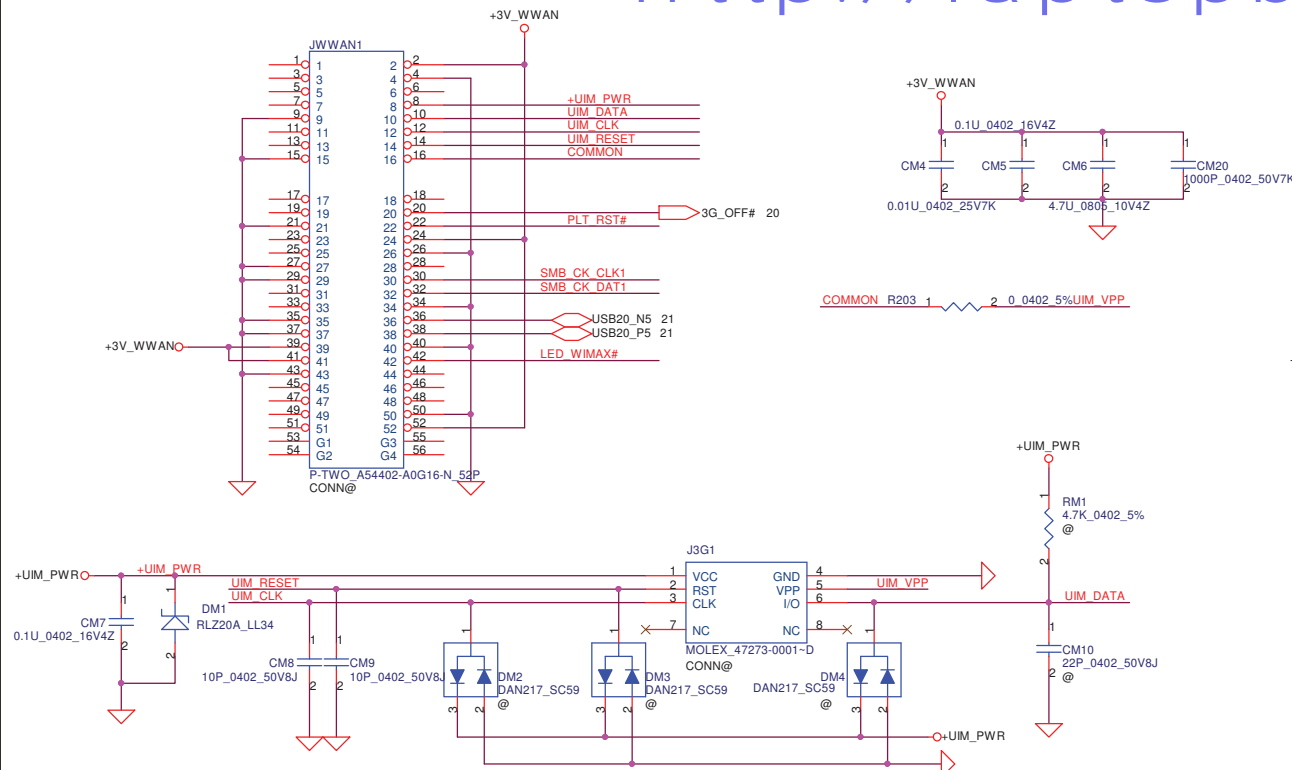


SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

Check AD29,AD28 strap function

check default

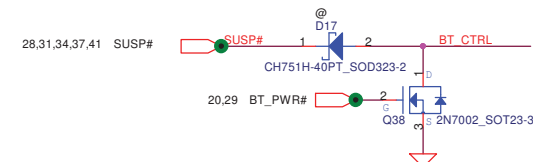




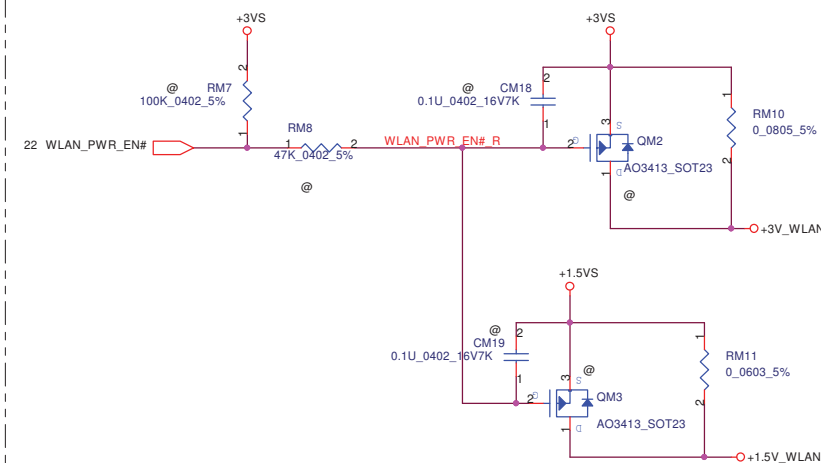
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	HI	LO
BT_PWR#	LO	HI

**If +3V_WLAN is +3VS, please remove D17.

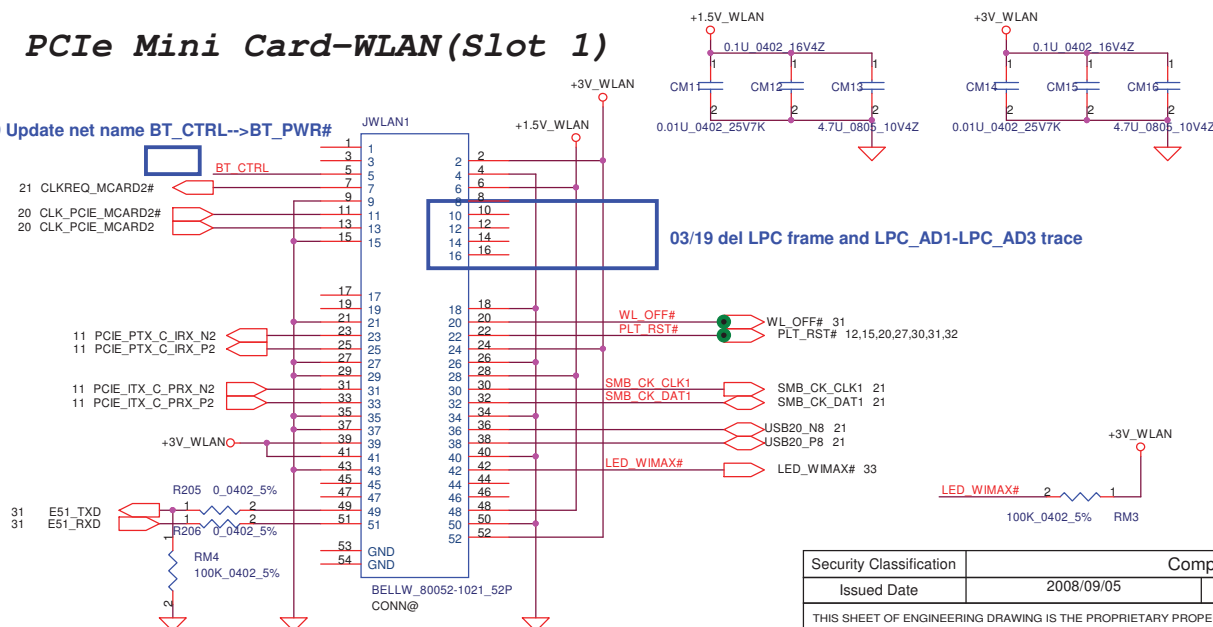


01/21 Add D17 and Q38 for BT control



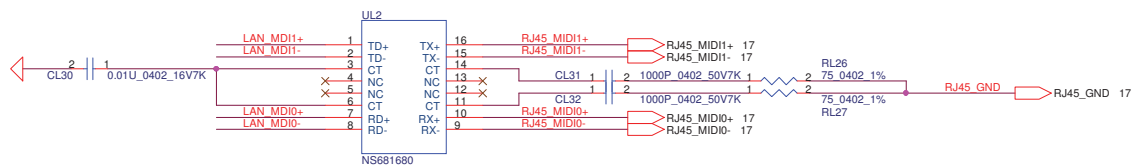
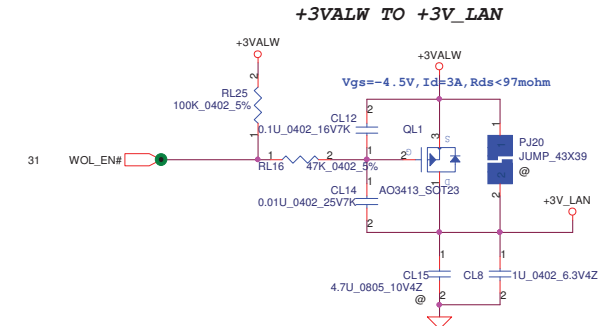
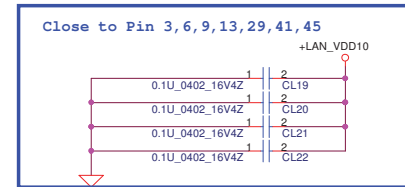
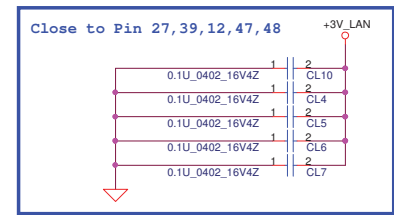
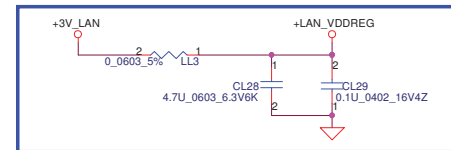
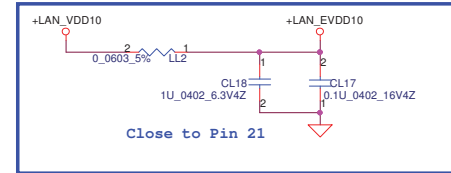
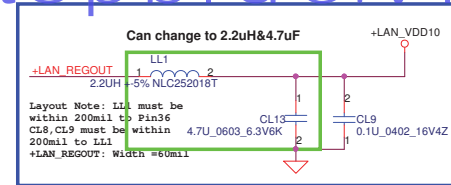
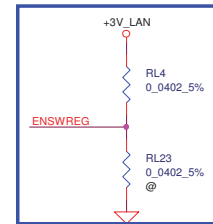
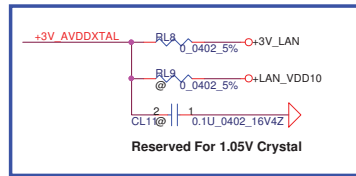
PCiE Mini Card-WLAN (Slot 1)

01/19 Update net name BT_CTRL-->BT_PWR#

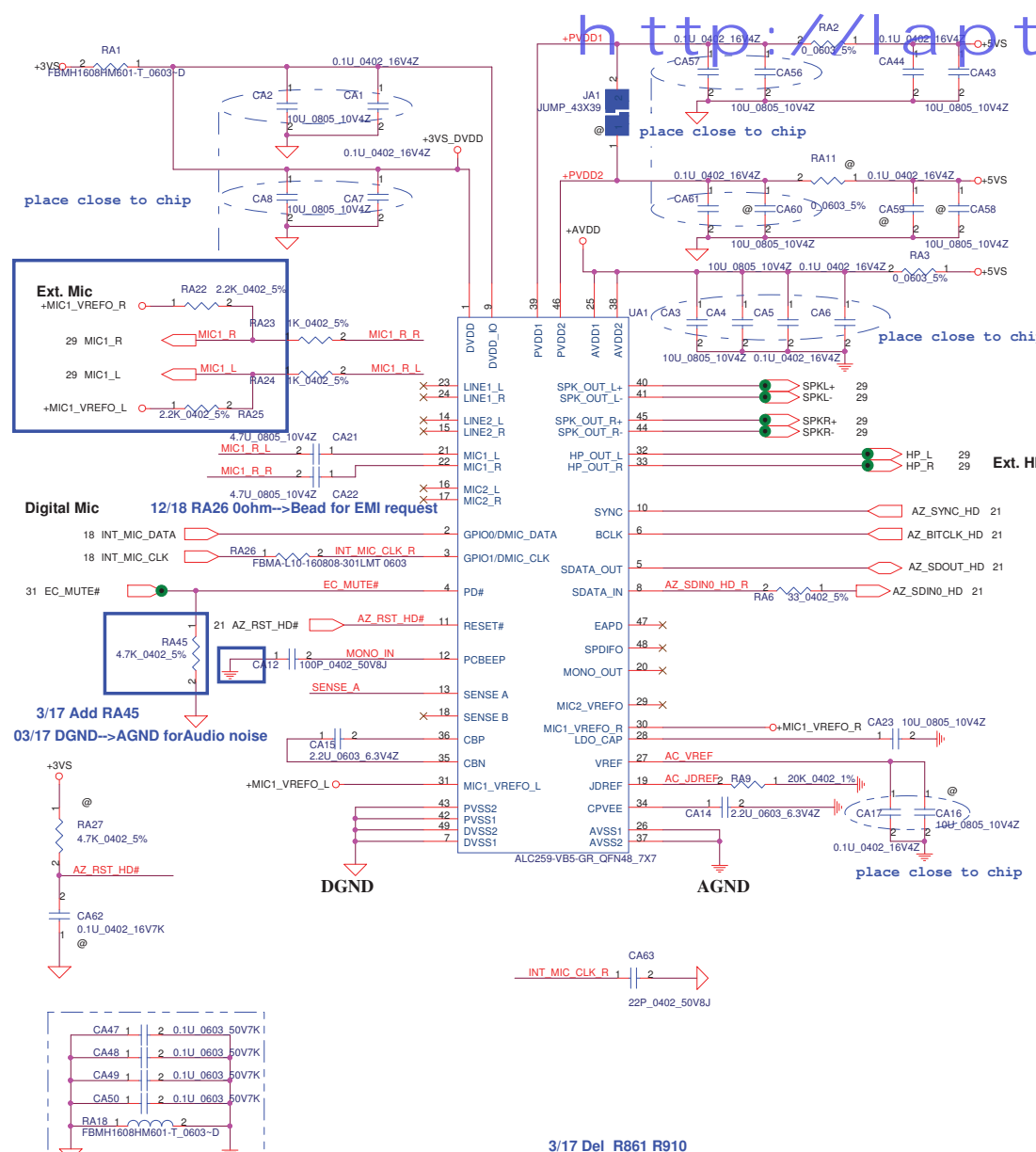


03/19 del LPC frame and LPC_AD1-LPC_AD3 trace

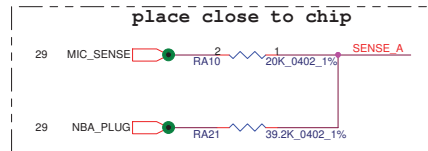
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Size	Document Number	LA-6032P		Rev 1.0
Date:	Tuesday, March 23, 2010	Sheet	26	of 45



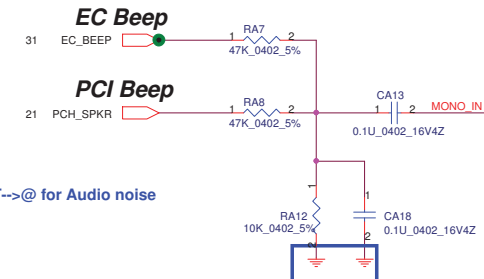
Sheet 27 of 45



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

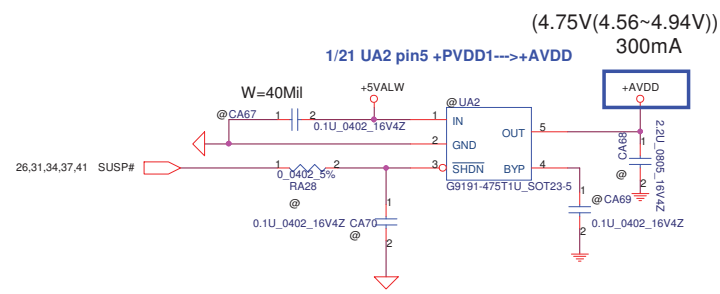


Beep sound



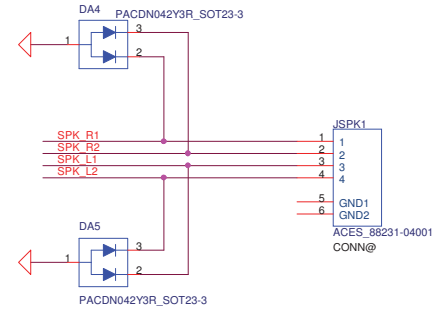
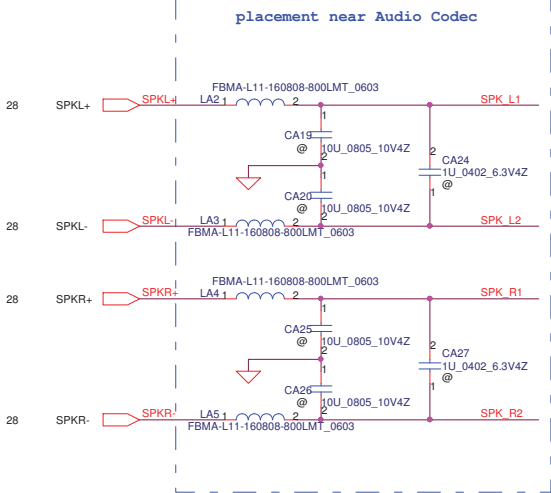
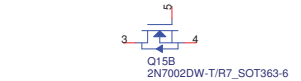
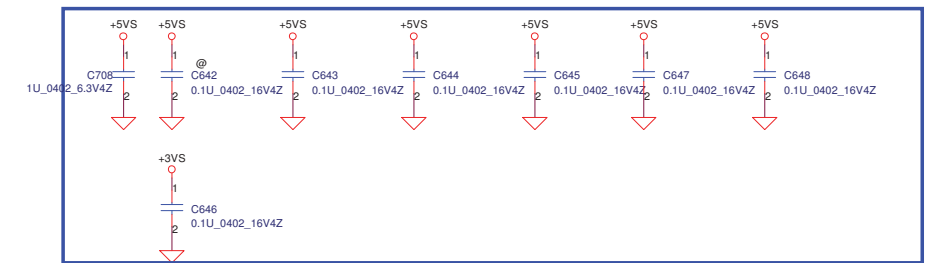
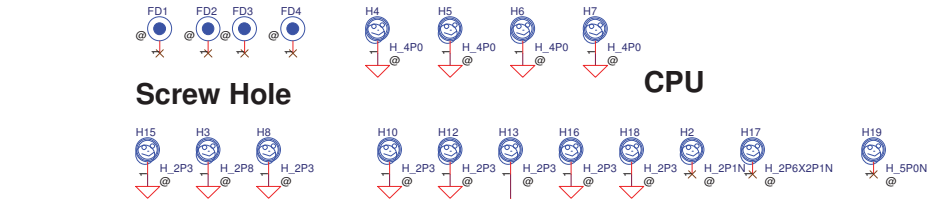
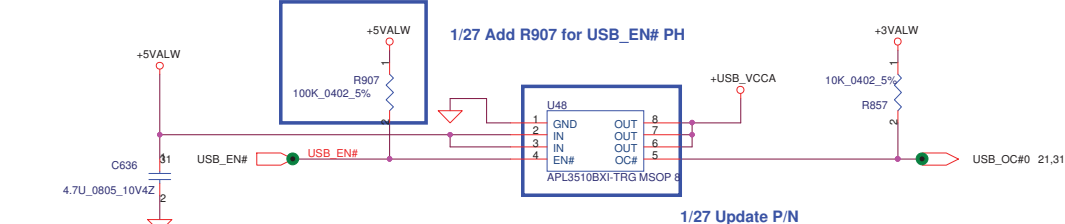
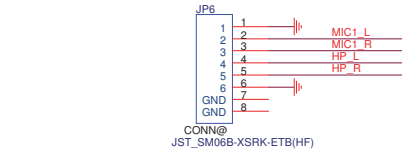
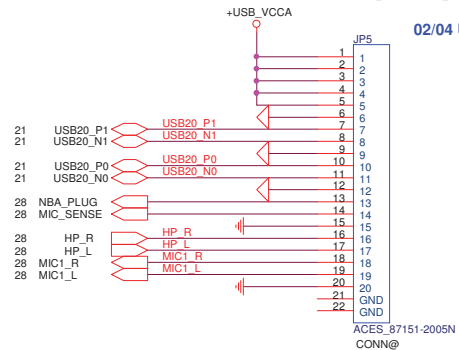
03/12 CA15 SMT-->@ for Audio noise

03/17 DGND-->AGND for Audio noise

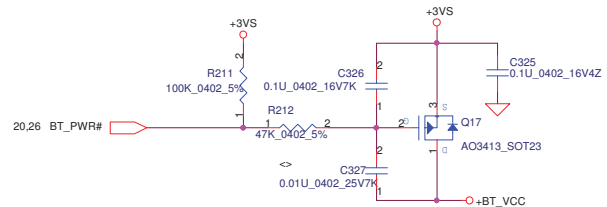


USB+Audio FFC conn <http://laptopblue.vn>

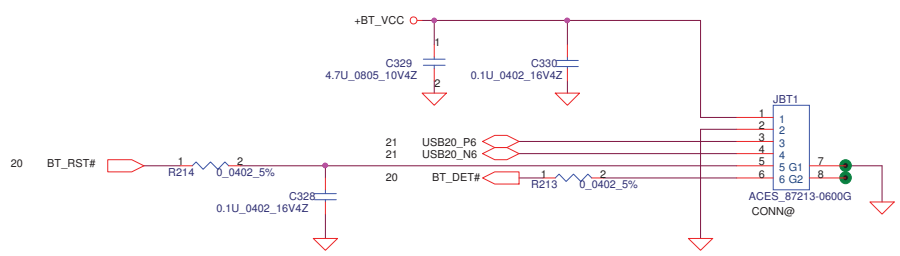
Pin=20pin, pitch=0.5



BlueTooth Interface

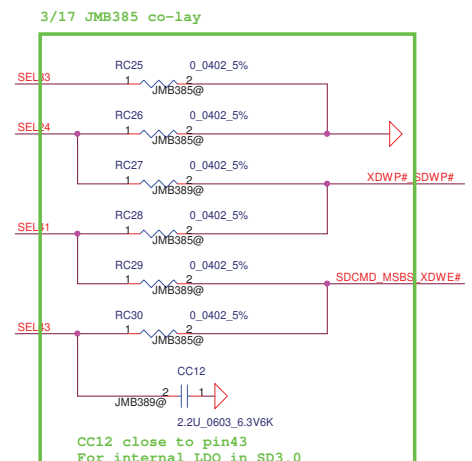
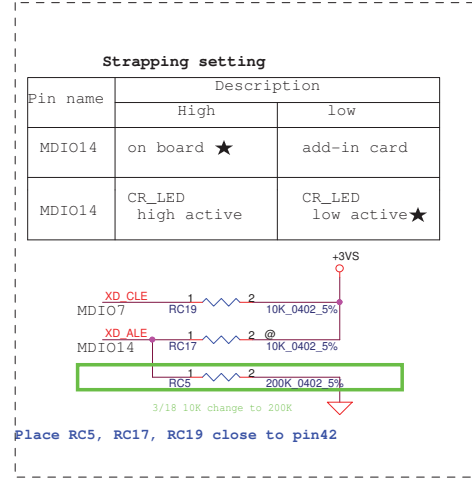
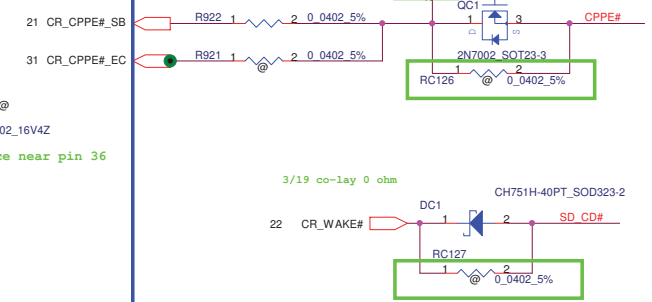
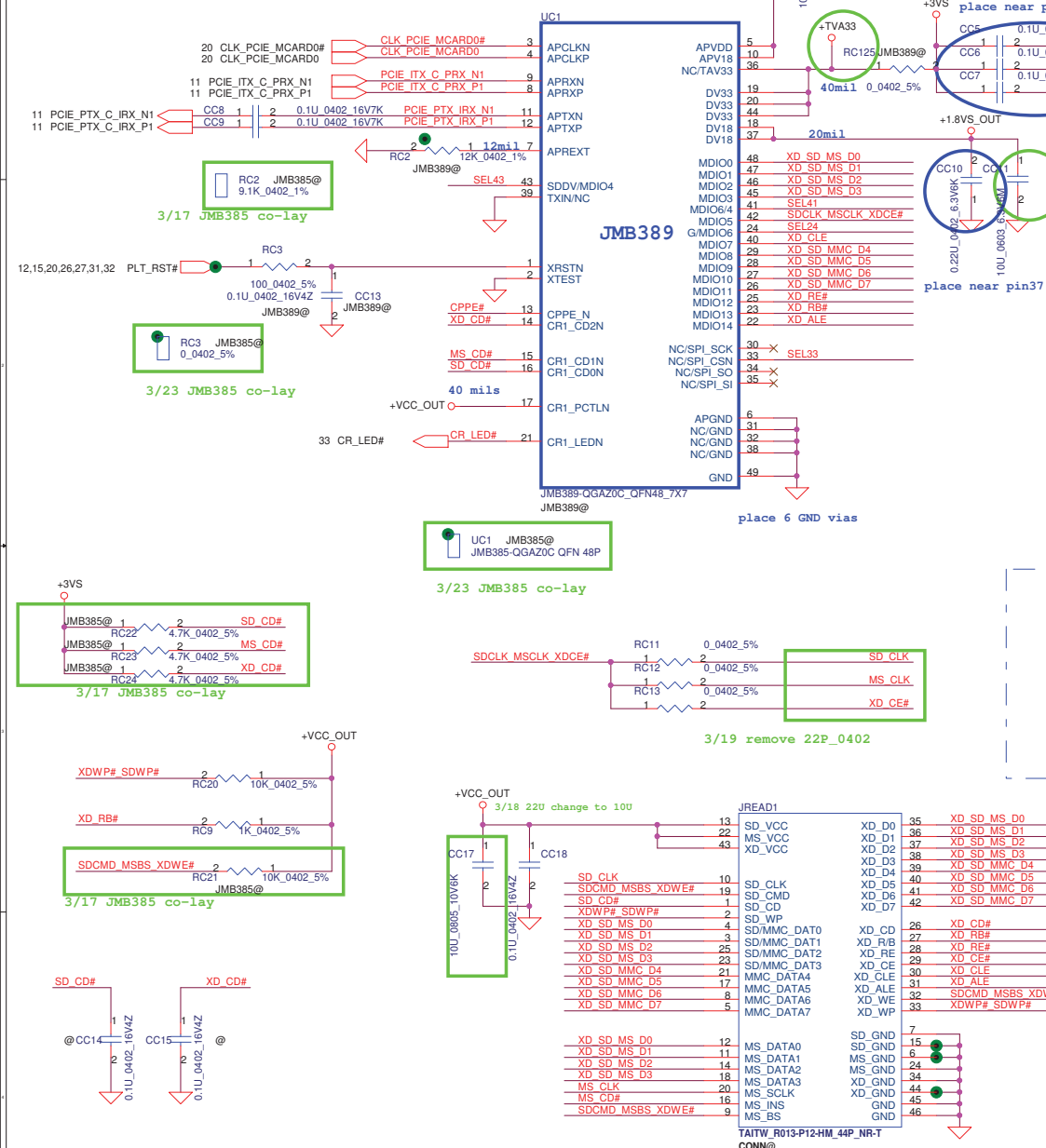


(MAX=200mA)



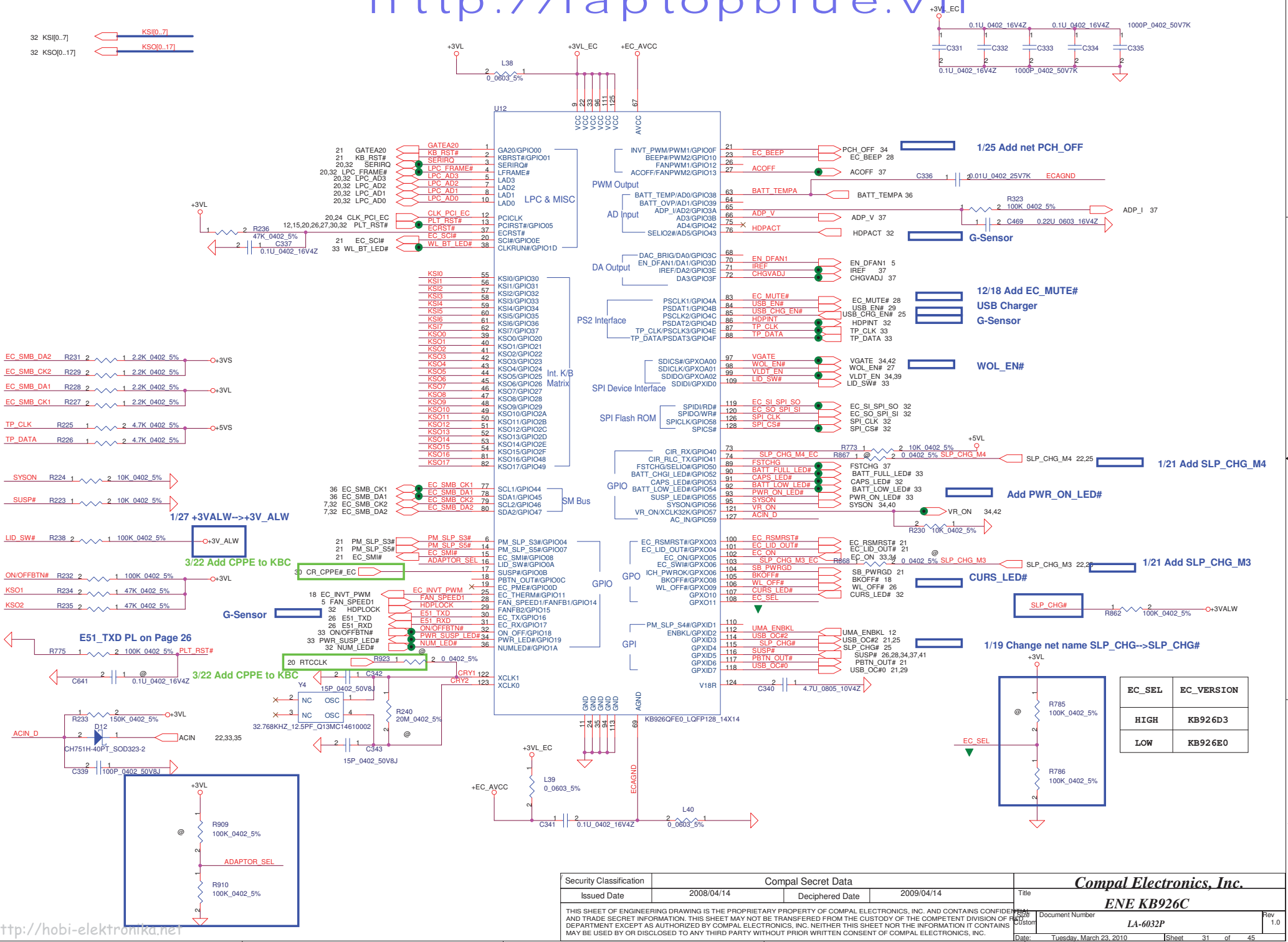
Security Classification	Compal Secret Data			Title	Compal Electronics, Inc.	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	Rev	AMP/Audio Jack/HP/SPEAKER/VR	
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				Date:	Tuesday, March 23, 2010	Sheet 29 of 45

Power Circuit



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		2011/01/22
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Compal Electronics, Inc.	
Card Reader JMB389	
Title	
Size	Document Number
Custom	
Date	Tuesday, March 23, 2010
Sheet	30 of 45
Rev	0.1

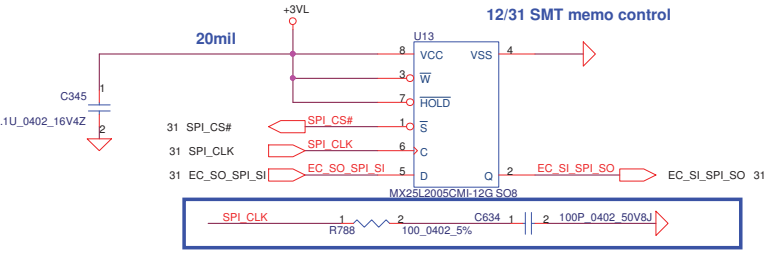


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Issued Date	2008/04/14	Deciphered Date	2009/04/14	Title	ENE KB926C	
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				LA-6032P	1.0	
Date:				Tuesday, March 23, 2010	Sheet	31 of 45

Option 1:SPI Flash (2MB*1) for EC
Option 2:SPI Flash (256KB*1) for EC
SPI Flash (2MB*1) for SB (set up strap pin)

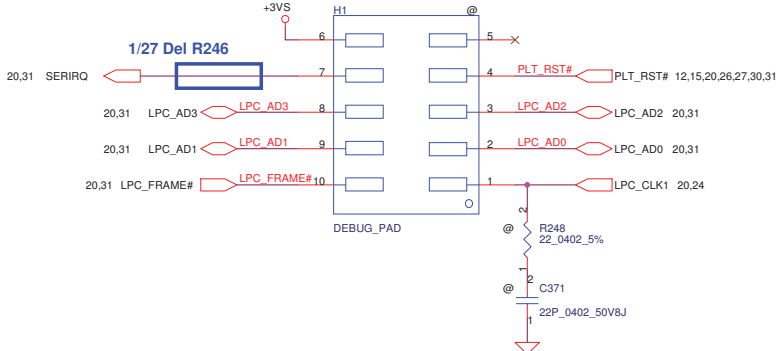
http://laptopblue.com

SPI Socket: SP07000F500 & SP07000H900
2MB P/N:MXIC SA00002TO00 S IC FL 16M MX25L1605DM2I-12G SOP 8P ROM
256KB P/N:MXIC SA00003GK00 S IC FL 2M MX25L2005CMI-12G SOP 8P

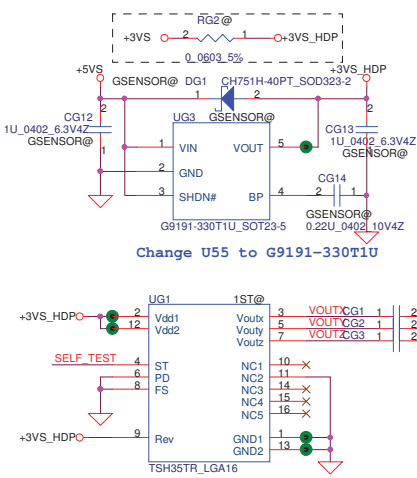


12/18 <BOM>R788 @-->100ohm and C634 @-->100P for RF request

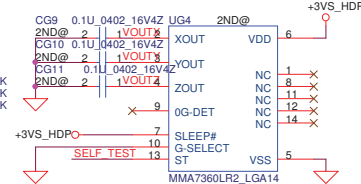
LPC Debug Port (Please place the PAD under DDR DIMM)



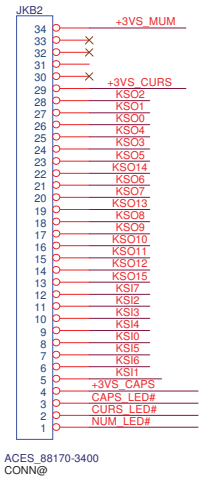
G-Sensor



Reserve Freescale

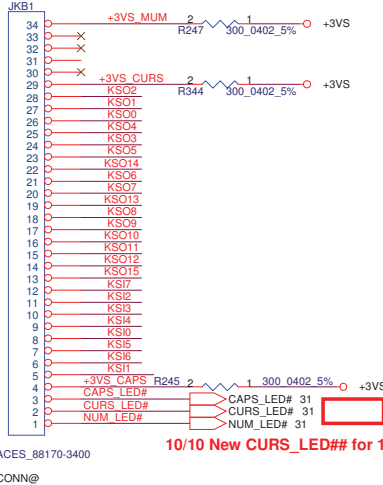


11.6 KEYBOARD CONN.

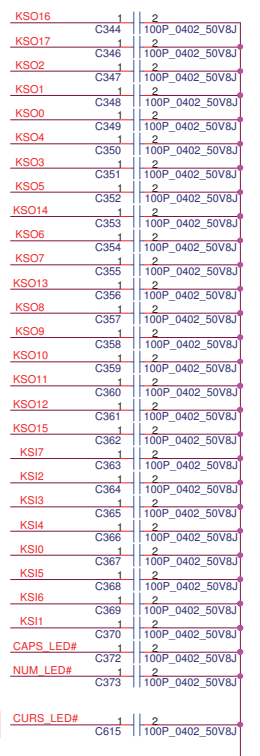


New keyboard

13.3 KEYBOARD CONN.



10/10 New CURS_LED# cap for 11.3&13.6



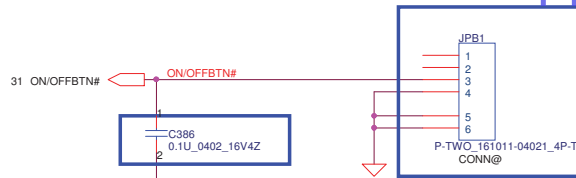
10/10 New CURS_LED# cap for 11.3&13.6

03/11 update G-sensor P/N

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Date	Tuesday, March 23, 2010	Sheet	32 of 45

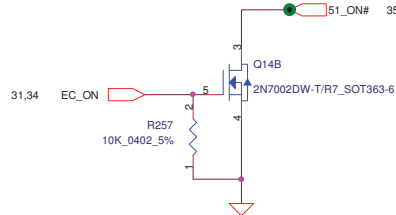
Power Button & Lid switch

http://laptopblue.vn



12/15<BOM> C386 @-->0.1u

1/27 Update footprint



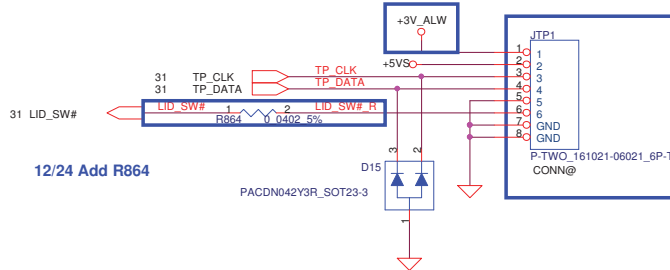
1/27 Del R808 R809 R810 R811

1/27 +3VALW-->+3V_ALW and +5VALW-->+5V_ALW

Touch/B Connector

1/27 +3VALW-->+3V_ALW

03/11 Update JTP1 footprint



12/24 Add R864

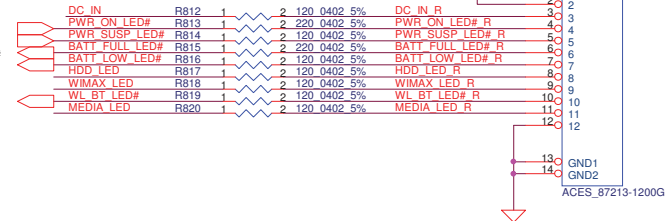
12/17 Q8 Q9 R258 R259-->@, R790 R791-->SMT

LED/B Connector

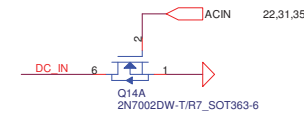
03/10 Fine tune R813 R815 120ohm-->220ohm



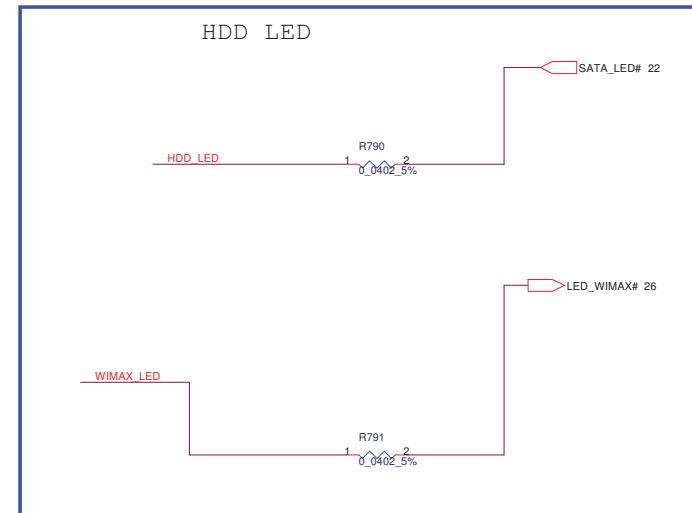
31 PWR_ON_LED#
31 PWR_SUSP_LED#
31 BATT_FULL_LED#
31 BATT_LOW_LED#
31 WL_BT_LED#



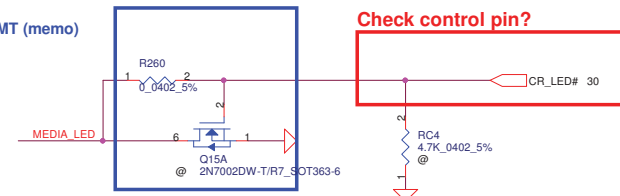
DC-IN LED



HDD LED



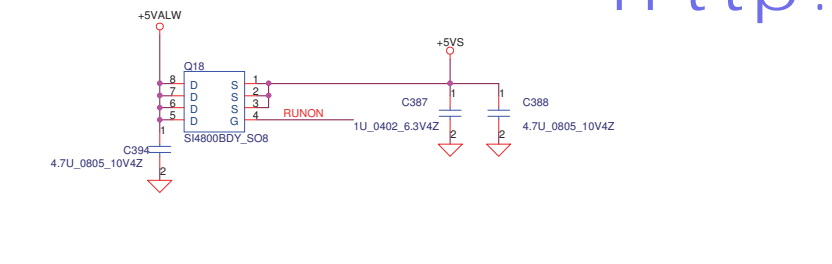
03/10 Q15-->@ and R260 @-->SMT (memo)



Check control pin?

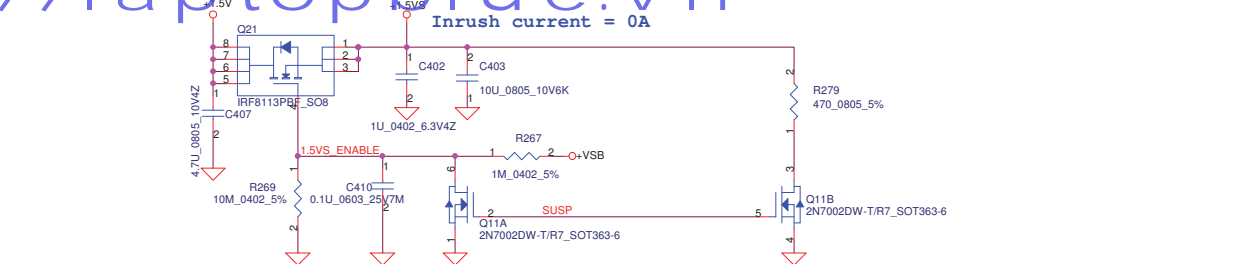
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Issued Date	2008/04/14	Deciphered Date	2009/04/14	Document Number
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			LA-6032P	
			Tuesday, March 23, 2010	Sheet 33 of 45

< +5VALW TO +5VS >

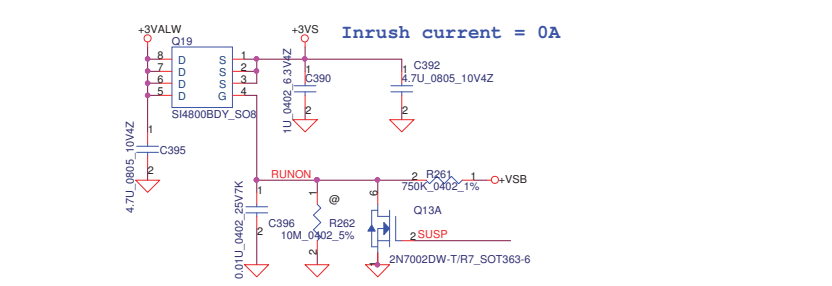


http://laptopblue.vn

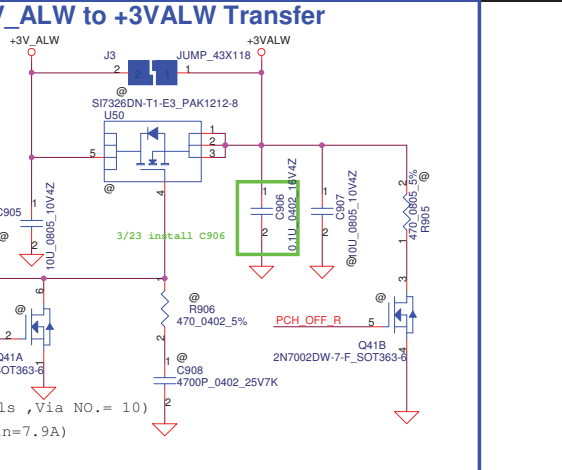
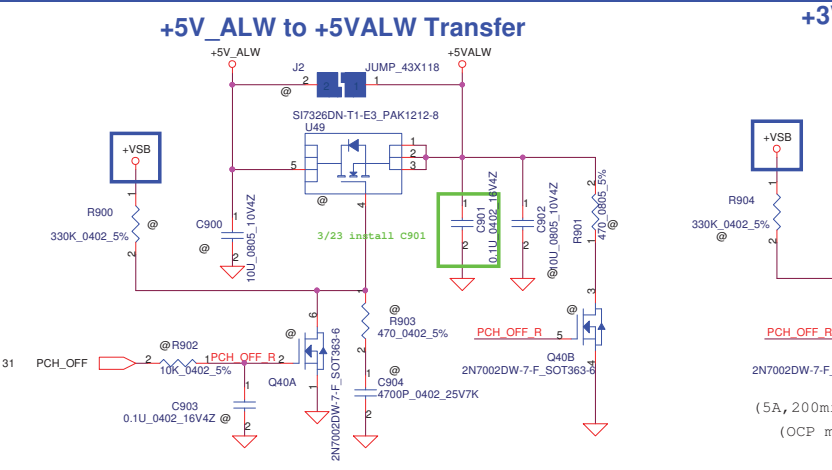
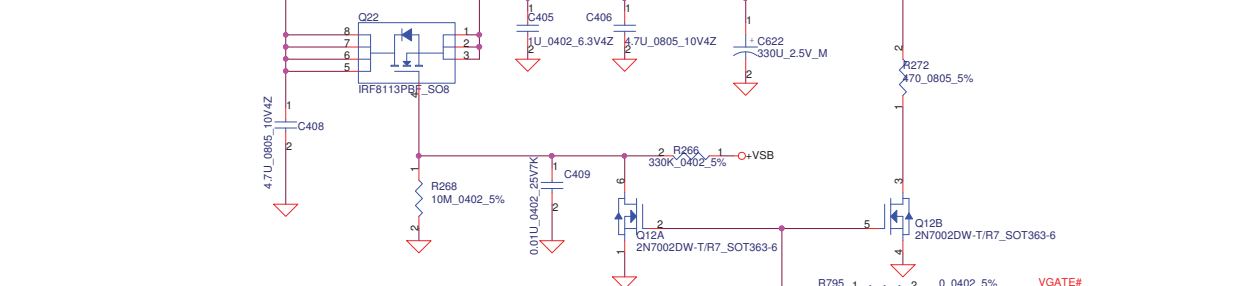
< +1.5V TO +1.5VS >



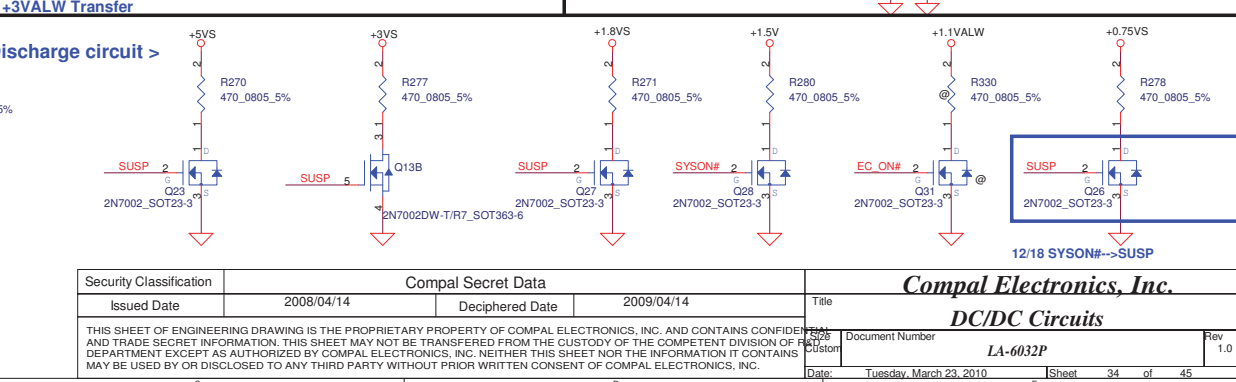
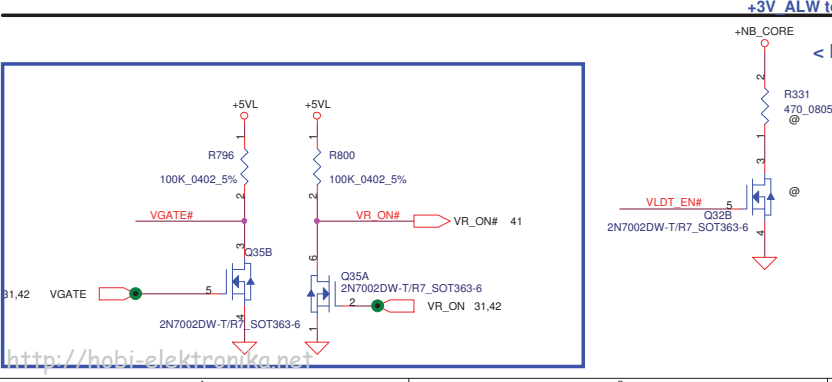
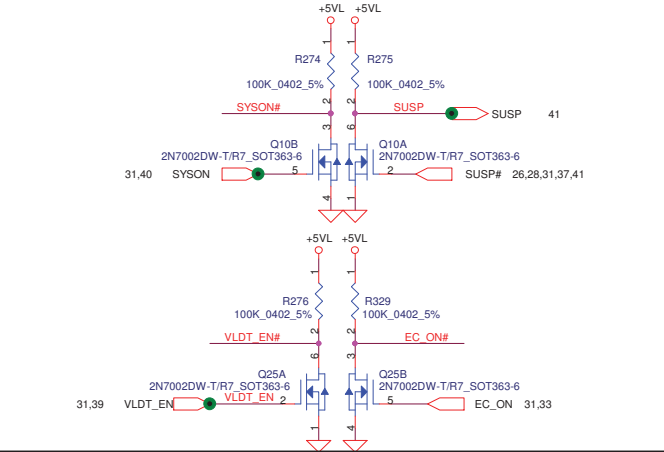
< +3VALW TO +3VS >



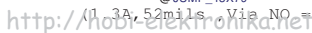
< +1.1VALW TO +1.1VS >



< Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >



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PH1 under CPU bottom side:

CPU thermal protection at 92 degree C

Recovery at 56 degree C

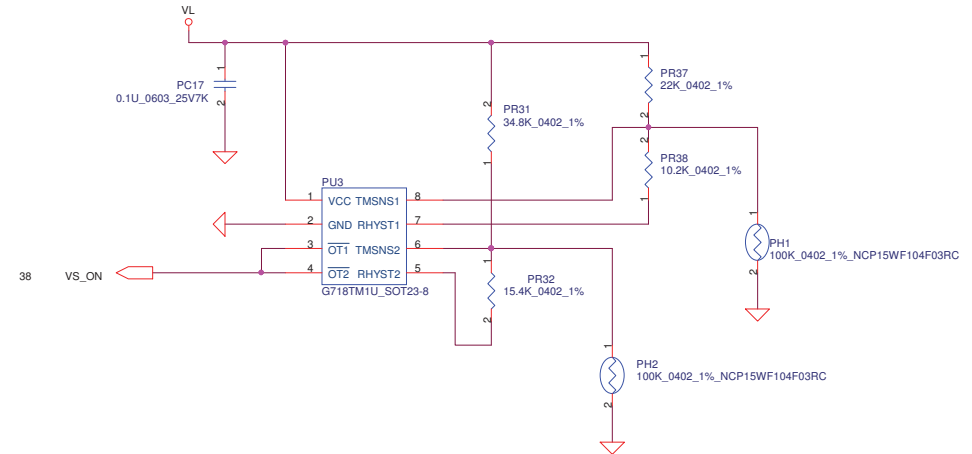
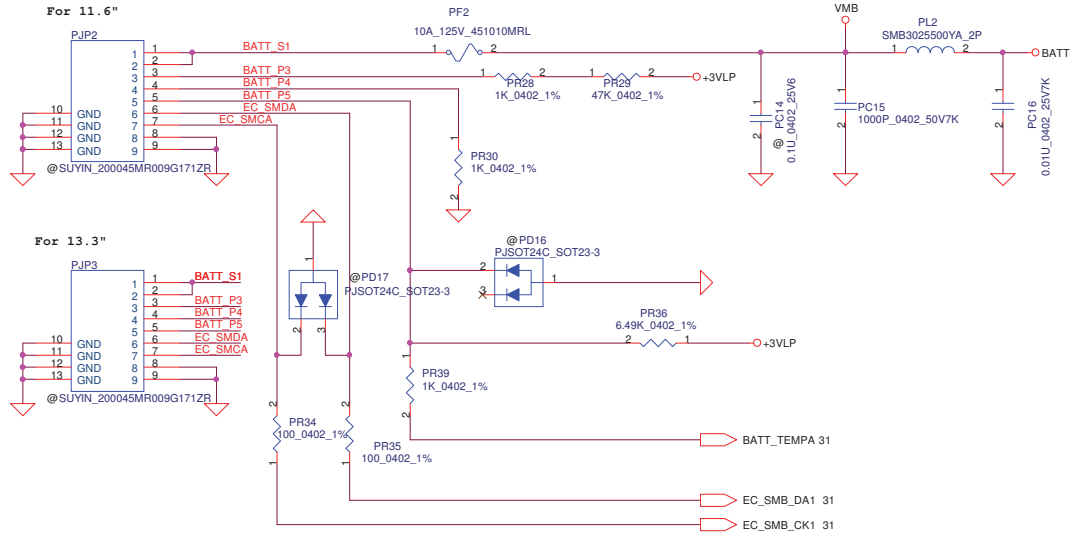
PH2 near main Battery CONN:

BAT thermal protection at 78 degree C

Recovery at 42 degree C

$R_{set} = 3 * R_{tmh}$

$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$



R_{tmh} at 92C = 7.71K, R_{tml} at 56C = 26.1K

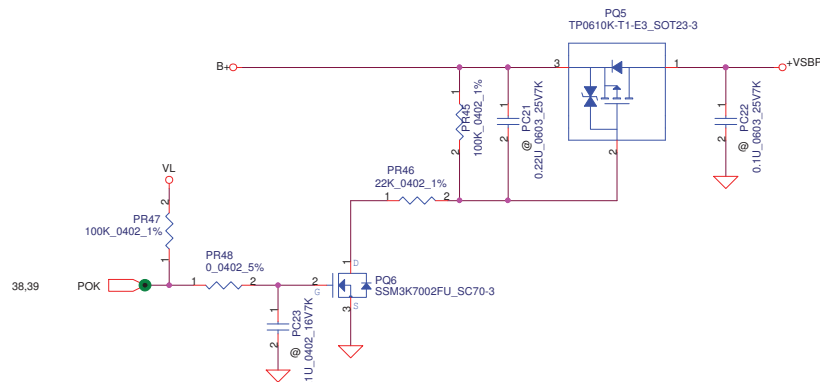
$R_{set} = 3 * 7.31 = 21.9K \implies PR37 = 22K$

$R_{hyst} = (22K * 26.1K) / (3 * 26.1K - 22K) = 10.199K \implies PR38 = 10.2K$

R_{tmh} at 78C = 11.635.K, R_{tml} at 42C = 46.38K

$R_{set} = 3 * 11.635 = 34.91K \implies PR31 = 34.8K$

$R_{hyst} = (34.8K * 46.38K) / (3 * 46.38K - 34.8K) = 15.468K \implies PR32 = 15.4K$



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Date: Tuesday, March 23, 2010				1.0
Sheet 36 of 45				

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BATTERY CONN / OTP

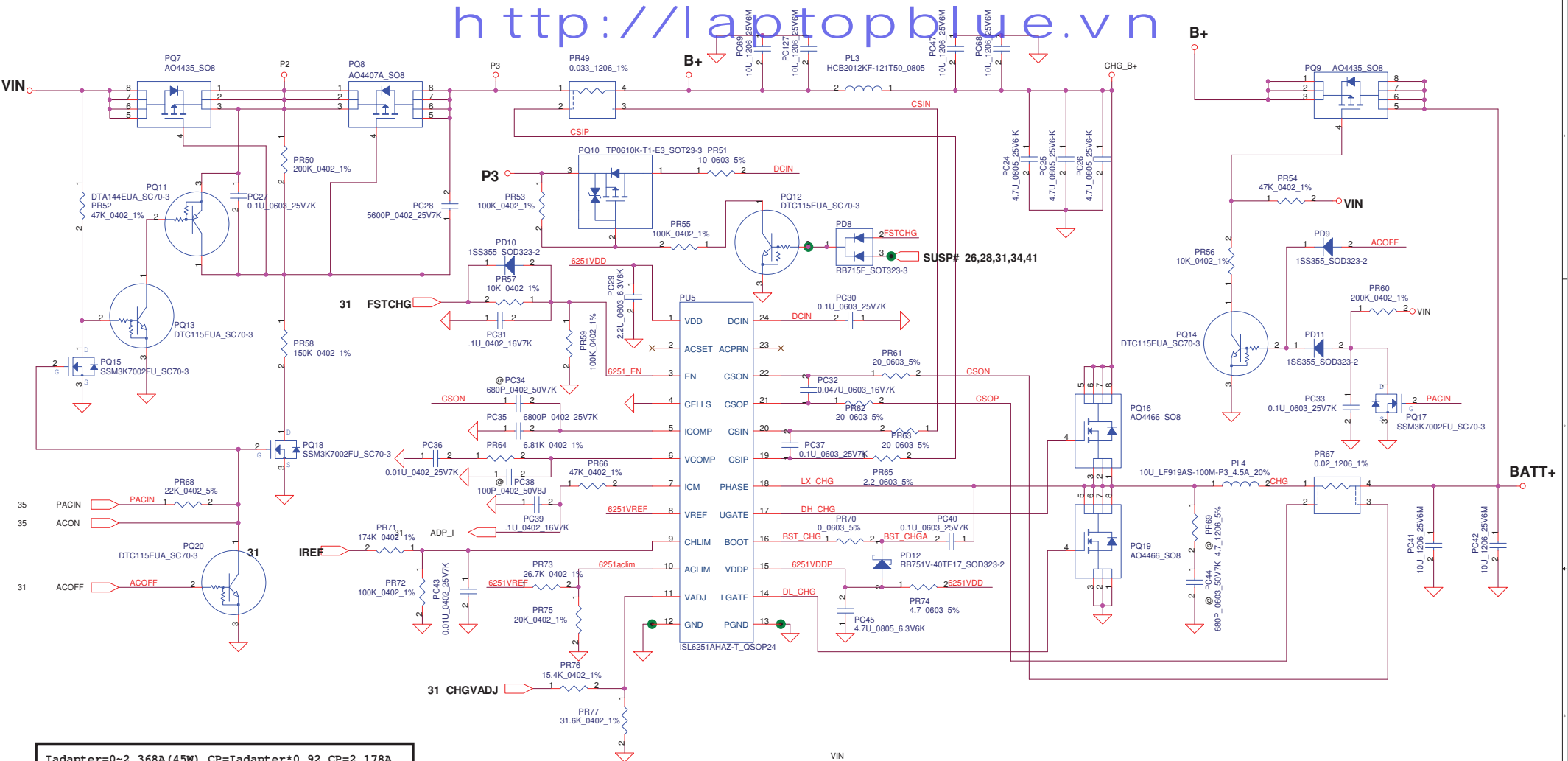
LA6032P

Rev

1.0

Date: Tuesday, March 23, 2010

Sheet 36 of 45

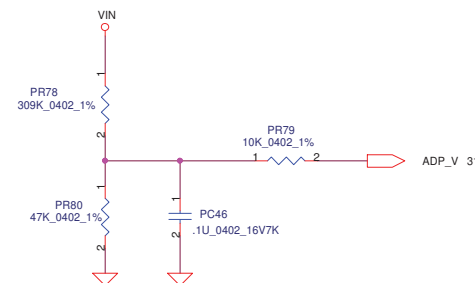


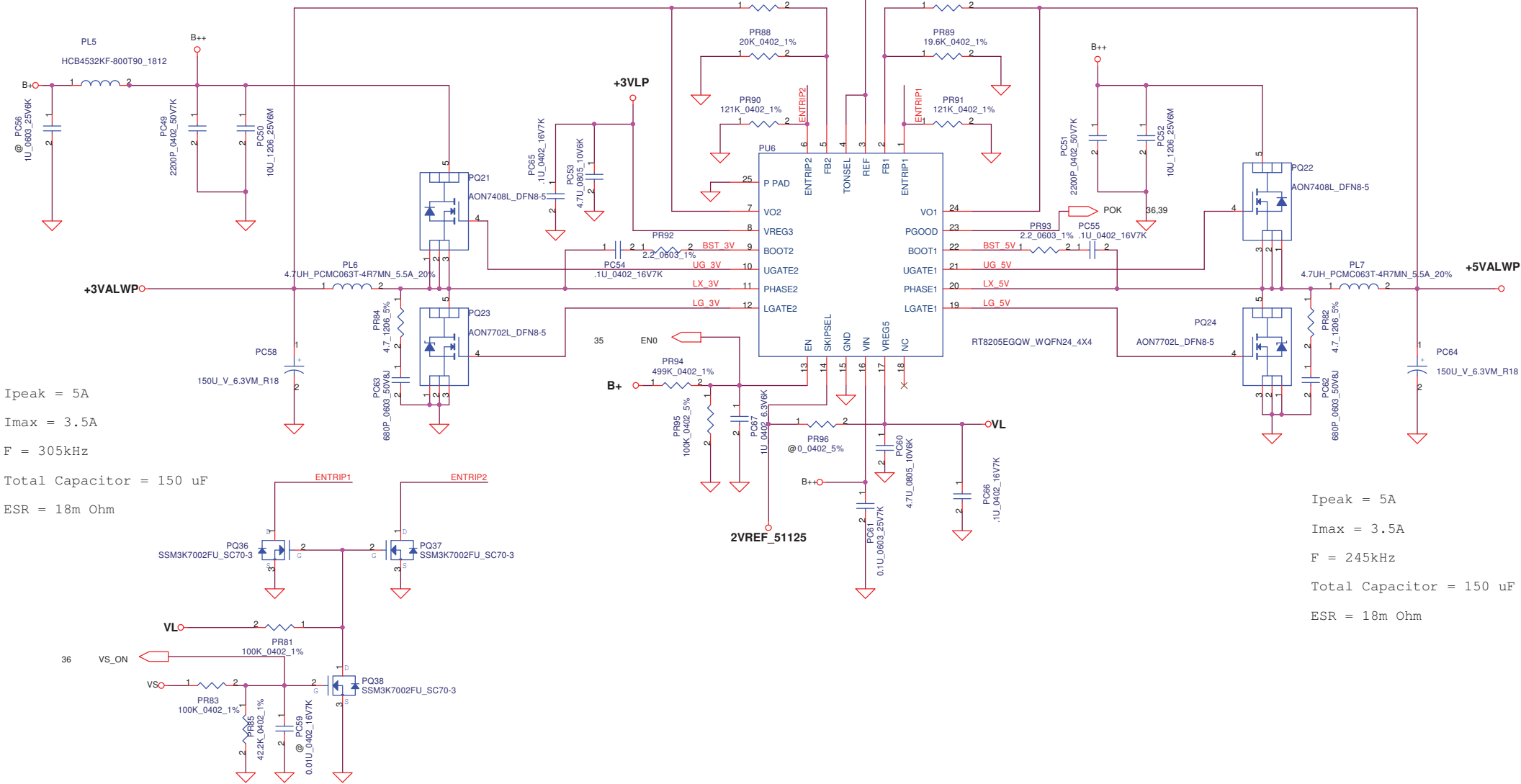
Iadapater=0~2.368A (45W) CP=Iadapater*0.92 CP=2.178A

CC=0.25A~3A
IREF=1.096*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.445	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CP mode
Vaclm=2.39* (20K//152K/ (20K//152K+26.7K//152K))=1.04596V
Iinput=(1/0.02) ((0.05*Vaclm)/2.39+0.05)
where Vaclm=1.04596V, Iinput=2.178A

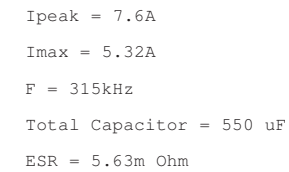
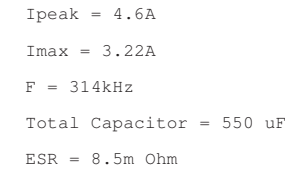




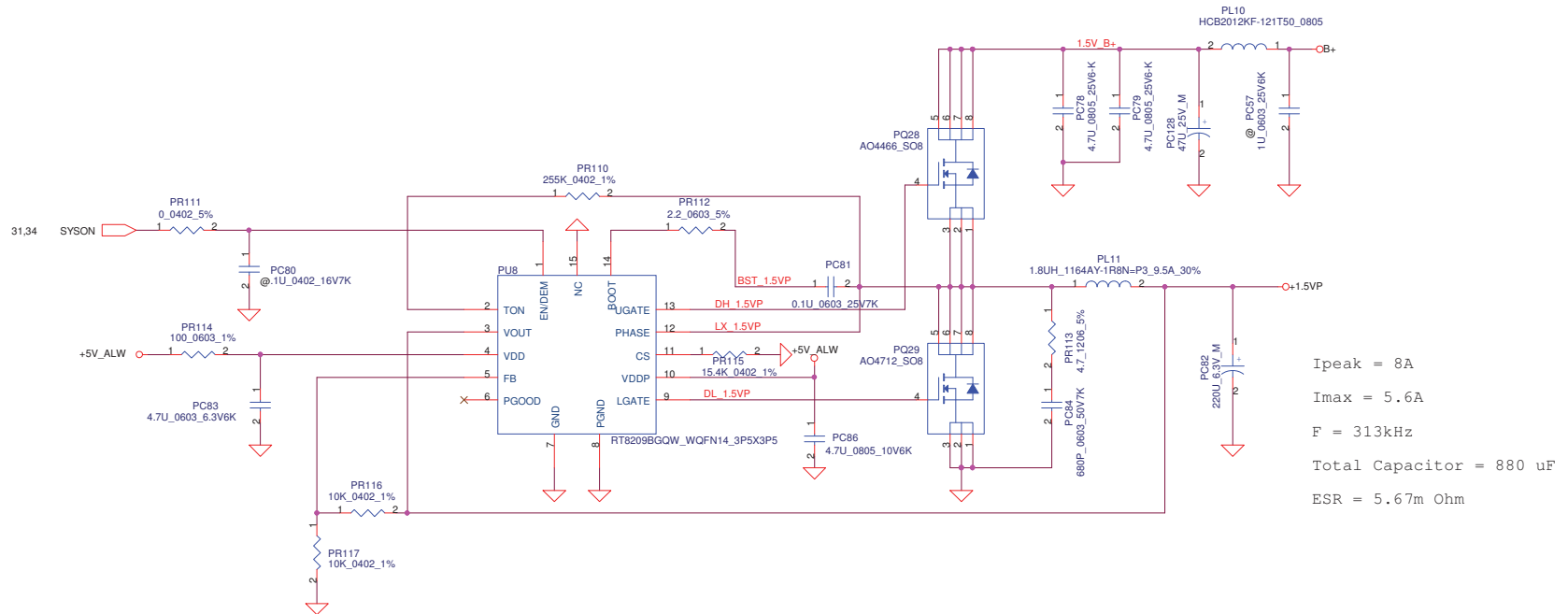
Ipeak = 5A
 Imax = 3.5A
 F = 305kHz
 Total Capacitor = 150 uF
 ESR = 18m Ohm

Ipeak = 5A
 Imax = 3.5A
 F = 245kHz
 Total Capacitor = 150 uF
 ESR = 18m Ohm

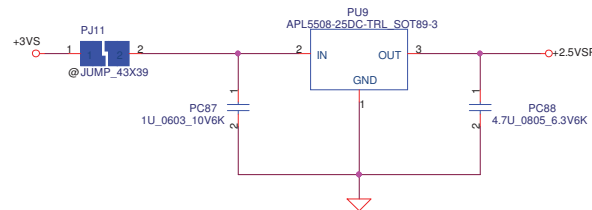
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				LA-6032P	
				Date	Tuesday, March 23, 2010
				Sheet	38 of 45
				Rev	1.0



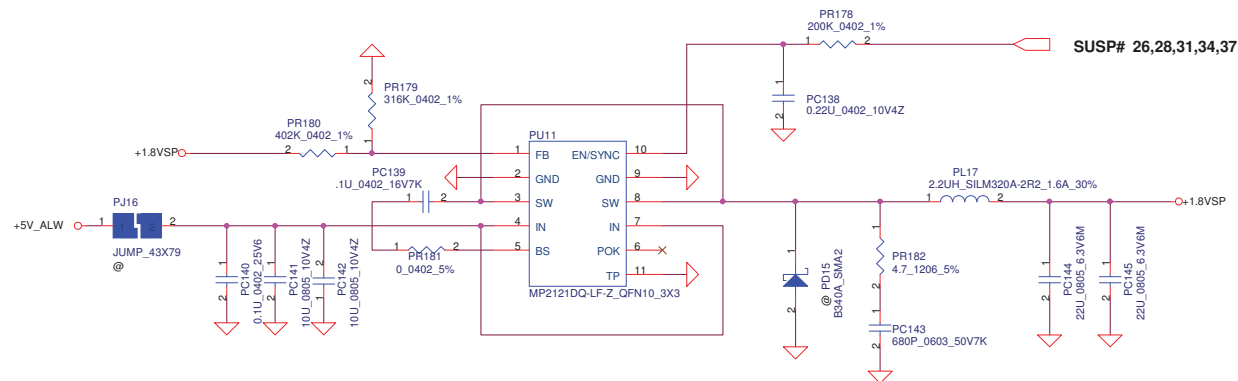
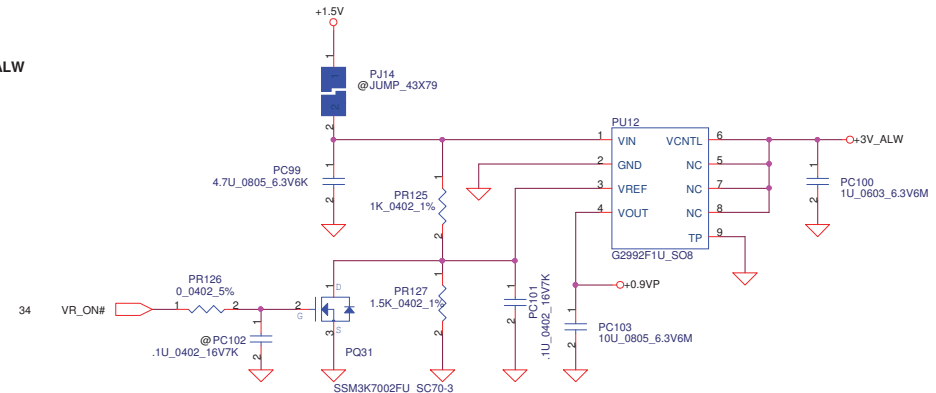
DENIAL OF R&D NS	Document Number	Rev
	LA6032P	1.0
Date:	Tuesday, March 23, 2010	Sheet 39 of 45



$I_{peak} = 8A$
 $I_{max} = 5.6A$
 $F = 313kHz$
 Total Capacitor = 880 uF
 $ESR = 5.67m\ \Omega$

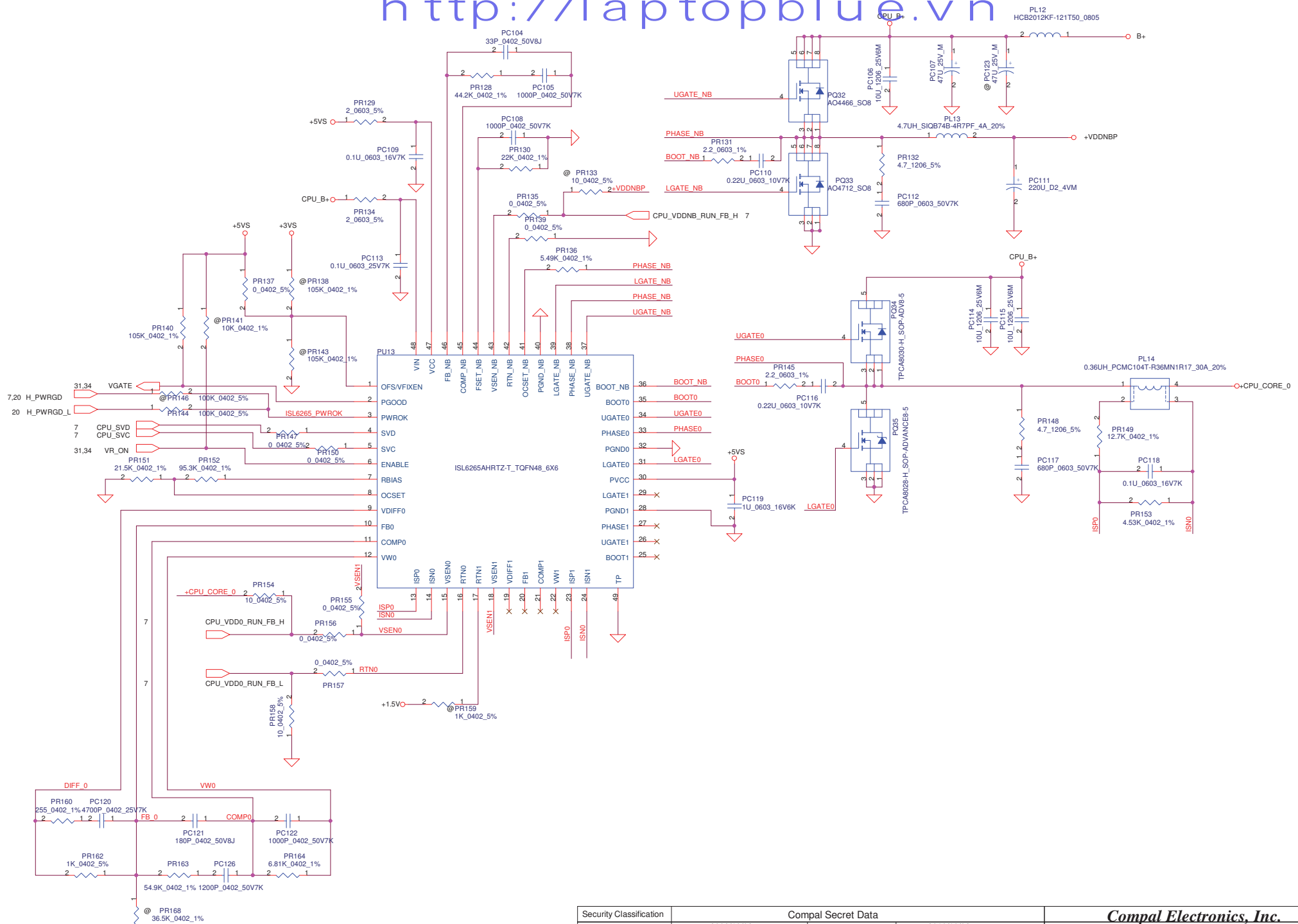


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				LA6032P	1.0
				Date: Tuesday, March 23, 2010	Sheet 40 of 45



ESR = 2.5m Ohm

Security Classification		Compal Secret Data		Compal Electronics, Inc. 0.75VSP/0.9VP/1.8VSP	
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				Document Number	1.0
				LA6032P	
Date: Tuesday, March 23, 2010				Sheet 41 of 45	



Security Classification		Compal Secret Data		Title	
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				LA6032P	1.0
Date: Tuesday, March 23, 2010				Sheet	42 of 45

+CPU_CORE

LA6032P

Rev 1.0

Page#	Title	Date	Request Owner	Issue Description	Solution Description
		2009/11/10	POWER		Release
P38	BATTERY CONN / OTP	2009/12/03	POWER	PR31 change to 34.8k	DVT
P38	BATTERY CONN / OTP	2009/12/03	POWER	PR32 change to 15.4k	DVT
P38	BATTERY CONN / OTP	2009/12/03	POWER	PR37 change to 22k	DVT
P38	BATTERY CONN / OTP	2009/12/03	POWER	PR38 change to 10.2k	DVT
P39	CHARGER	2009/12/03	POWER	PC24,25,26 size change to 4.7uf 0805	DVT
P43	0.75VSP/0.9VP/1.8VSP	2009/12/03	POWER	PR121 change to 300k	DVT
P43	0.75VSP/0.9VP/1.8VSP	2009/12/03	POWER	PC96 change to 0.22uf	DVT
P43	0.75VSP/0.9VP/1.8VSP	2009/12/03	POWER	PR125 change to 1k	DVT
P43	0.75VSP/0.9VP/1.8VSP	2009/12/03	POWER	PR127 change to 1.5k	DVT
P44	+CPU_CORE	2009/12/03	POWER	Delete PR142	DVT
P44	+CPU_CORE	2009/12/03	POWER	PR131, PR145 change to 2.2 ohm	DVT
P44	+CPU_CORE	2009/12/03	POWER	PR132 change to 4.7_1206_5%	DVT
P44	+CPU_CORE	2009/12/03	POWER	PC112 change to 680P_0603_50V7K	DVT
P39	CHARGER	2010/01/29	POWER	Add PC47,68,69,127 10U_1206_25V6M	PVT
P41	+1.1VALWP/+NB_COREP	2010/02/03	POWER	Add PC70 4.7U_0805_25V6-K	PVT
P41	+1.1VALWP/+NB_COREP	2010/02/03	POWER	PL9 change to 1.8UH_9.5A_30%	PVT
P44	+CPU_CORE	2009/12/03	POWER	PL13 change to 4.7UH_4A_20%	PVT
P37	CHARGER	2009/02/08	POWER	Move PR18,PR19 to connect PBJ1	PVT2

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Item	Reason for change	PG#	Modify List	Date	Phase
1	Update JSATA1, JHDMI1 and JREAD1 footprint		ME request	2009/12	EVT->DVT
2	Update DDR_CS0_DIMMB#, DDR_CS1_DIMMB# net	P06	Net contact error on DIMMB	2009/12	EVT->DVT
3	Update DDR_CKE0_DIMMA, DDR_CKE1_DIMMA net	P06	Net contact error on DIMMA	2009/12	EVT->DVT
4	R41~R44 SMT-->@	P07	Fine tune HDT debug pull high R	2009/12	EVT->DVT
5	Del R46 and add R850-R854	P07	For ESD request	2009/12	EVT->DVT
6	Add RS15 RS16 for NBGFX_CLK,NBGFX_CLK#	P12	For internal clock gen	2009/12	EVT->DVT
7	Fine tune RS880M clock	P12	For internal clock gen	2009/12	EVT->DVT
8	Del external clock gen	P16	For internal clock gen	2009/12	EVT->DVT
9	Fine tune pin define JP4 Pin1 Pin2 Pin8-->GND	P17	Add more GND pin	2009/12	EVT->DVT
10	Add R855 R856 for HDMI_SDATA,HDMI_SCLK pull high R	P19	Solve HDMI can not detect	2009/12	EVT->DVT
11	U6 pin5 +5VL-->+5VS and HDMI Dual NMOSx2(Q6 Q7)->Single NMOS (Q6)	P19	Cost down plan	2009/12	EVT->DVT
12	Add RS1~RS14 near SB820M and TP34 TP35	P20	For internal clock gen	2009/12	EVT->DVT
13	C640 @-->22P on CLK_PCI_EC	P20	EMI request	2009/12	EVT->DVT
14	C705 C705 @-->SMT on Y6	P20		2009/12	EVT->DVT
15	R152 R153 R154 pull +3VALW-->pull GND	P21	Follow AMD check list 1.03	2009/12	EVT->DVT
16	Add device clock request pin on SB820M	P21	For internal clock gen	2009/12	EVT->DVT
17	C632 @-->33P on AZ_BITCLK_HD	P21	EMI request	2009/12	EVT->DVT
18	Add WLAN_PWR_EN# and WWAN_PWR_EN# net on SB820M	P22	Power saving request	2009/12	EVT->DVT
19	U47 +3VL-->+3VALW and Y3 R164 C246 C247 SMT->@	P22	25MHz by default	2009/12	EVT->DVT
20	Reaserved R859 C707 on CLK net	P22	EMI request	2009/12	EVT->DVT
21	Fine tune SB820M strap pin	P24	For internal clock gen	2009/12	EVT->DVT
22	Add C706 0.1u on CLK_PCI_EC	P24	EMI request	2009/12	EVT->DVT
23	Del R193 and Add R858 PH on USB_OC#2	P25	Solve the USB hang up issue	2009/12	EVT->DVT
24	Reserved RM5 RM6 CM17 QM1 RM9 for +3V_WWAN power saving	P26	Power saving request	2009/12	EVT->DVT
25	Reserved RM7 RM8 CM18 QM2 RM10 for +3V_WLAN power saving	P26	Power saving request	2009/12	EVT->DVT
26	Reserved CM19 QM3 RM11 for +1.5V_WLAN power saving	P26	Power saving request	2009/12	EVT->DVT
27	RL21 pin2 +3V_LAN-->GND	P27	LAN vender request	2009/12	EVT->DVT
28	Del RA4 RA5	P28	Fine tune Audio HP out voltage	2009/12	EVT->DVT
29	Reserved RA27 CA26 on AZ_RST_HD#	P28	ESD request	2009/12	EVT->DVT
30	Add Q37 R860 R861 and PD# net	P28	Solve Audio PD# control issue	2009/12	EVT->DVT
31	Fine tune JP5 pin define	P29	Solve the USB hnag up issue	2009/12	EVT->DVT
32	Fine tune SPK_L1,SPK_L2,SPK_R1 and SPK_R2 for SPK	P29	Solve SPK pin issue	2009/12	EVT->DVT
33	Add R857 PH USB_OC#0 net	P29	Solve the USB hnag up issue	2009/12	EVT->DVT
34	Add C708 on +5VS	P29	ESD request	2009/12	EVT->DVT
35	Fine tune card reader pin define	P30	ME use new card reader connector	2009/12	EVT->DVT
36	Add EC_MUTE# on KBC926 (U12) 83pin	P31	Solve Audio PD# control issue	2009/12	EVT->DVT
37	Q8 Q9 R258 R259-->@, R790 R791-->SMT	P33	Cost down plan	2009/12	EVT->DVT
38	C386 @-->0.1u on ON/OFFBTN#	P33	EMI request	2009/12	EVT->DVT
39	C410 0.01u_0402_16V-->0.1u_0603_25V and R267 330k->1M	P34	SMT memo	2009/12	EVT->DVT
40	SYSON#-->SUSP on Q26 Pin2	P34	+0.75VS discharge control pin	2009/12	EVT->DVT
41	RA26 0ohm-->Bead (SM010017710) on INT_MIC_CLK	P28	EMI request	2009/12/18	EVT->DVT
42	C632 @-->33P on AZ_BITCLK_HD	P21	EMI request	2009/12/18	EVT->DVT
43	R788 @-->100ohm and C634 @-->100P on SPI_CLK	P32	RF request	2009/12/18	EVT->DVT
44	R789 @-->100ohm and C635 @-->100P on AZ_BITCLK_HD	P28	RF request	2009/12/18	EVT->DVT
45	Add CA63 on INT_MIC_CLK_R	P28	RF request	2009/12/18	EVT->DVT
46	RA1 0ohm-->Bead on Audio power	P28	RF request	2009/12/18	EVT->DVT
47	Add CM20 1000P on +3V_WWAN	P26	RF request	2009/12/18	EVT->DVT
49	Add C709 on 27M_SEL	P16	RF request (EXT only)	2009/12/19	EVT->DVT
49	Fine tune R133 R value 11.8K-->8.2K	P21	Fine tune USB signal	2009/12/22	EVT->DVT
50	<BOM>RA22 RA25 4.7K-->2.2K and CA16 10u-->@	P28	Audio vender request	2009/12/22	EVT->DVT
51	Add BT_PWR# net contact to JWLAN1 pin5	P26	Follow common design	2009/12/23	EVT->DVT
52	Del R161 and SLP_CHG on SB	P22	Follow common design	2009/12/23	EVT->DVT
53	Add SLP_CHG on pin115 and add R862	P31	Follow common design	2009/12/23	EVT->DVT
54	Add UA2 CA67 CA68 CA69	P28	Audio power reserved	2009/12/23	EVT->DVT
55	Add F2 for card reader proetct	P30	H/W request	2009/12/24	EVT->DVT
56	Reserved RA28 CA70	P28	Reserved for fin tune aduio power control	2009/12/24	EVT->DVT
57	Add R863 PH on CIR_EN#	P21	Follow common design	2009/12/24	EVT->DVT
58	Add R864 on LID_SW#	P33	Reserved for ESD protect	2009/12/24	EVT->DVT
59	Modify TP26 TP27-->EVENT#_A and EVENT#_B	P08 P10	Solve layout test point issue	2009/12/25	EVT->DVT
60	C497 SMT-->@	P08	Fine tune CPU_CORE cap	2009/12/25	EVT->DVT

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Doc# 1 Date: 2005/03/10 1 Rev: 44 of 45					

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Item	Reason for change	PG#	Modify List	Date	Phase
1	Add D17 and Q38 for BT power control	P26	Follow common design	2010/1/20	DVT->PVT
2	Change net name SLP_CHG->SLP_CHG#	P25 P31	Follow net rule	2010/1/20	DVT->PVT
3	Need to fine tune R783 and R784	P18	VB function	2010/1/20	DVT->PVT
4	<BOM> SB use 2MB SPI ROM SA00002TO00	P22	Non share ROM	2010/1/20	DVT->PVT
5	<BOM> Update LAN P/N for LAN VB P/N	P27	Vender update P/N	2010/1/20	DVT->PVT
6	<BOM> EC SPI use 256KB SPI ROM SA00003GK00	P32	Non share ROM	2010/1/20	DVT->PVT
7	BT part SMT-->@	P29	IUR no BT device	2010/1/20	DVT->PVT
8	Update JREAD1 footprint (Same as EVT)t	P30	ME request	2010/1/20	DVT->PVT
9	Update JSATA1 footprint TAIWI_EU114-117CRL-TW_11P-T	P25	ME request	2010/1/20	DVT->PVT
10	Update JHDD1 pin4 +5VS-->GND	P25	HW request	2010/1/20	DVT->PVT
11	Del DC to DC +NB_CORE part	P34	HW request	2010/1/20	DVT->PVT
12	Change USB port10 to USB port5 on WWAN	P21	Follow common design	2010/1/20	DVT->PVT
13	Add R865 R866 for SLP_CHGX_M3/M4 on SB	P21	Follow common design	2010/1/20	DVT->PVT
14	Add R867 R868 for SLP_CHGM3/M4 on EC	P31	Follow common design	2010/1/21	DVT->PVT
15	UA2 pin5 +PVDD1--->+AVDD	P28	Reserved for Audio analog power	2010/1/21	DVT->PVT
16	<BOM> U48 SA000008G00-->SA00003DR00 (Same as intel)	P29	HW request	2010/1/21	DVT->PVT
17	Del R164 Y3 C246 C247 and add TP36 TP37	P22	HW request	2010/1/22	DVT->PVT
18	JLVDS1 pin24 +LCD_INV-->NG	P18	Follow common design	2010/1/22	DVT->PVT
19	U9 pin1 +5VALW-->+5V_ALW for USB charge	P25	Follow common design	2010/1/22	DVT->PVT
20	Add C900~C908,R900~R906 Q40 Q41 U49 U50 for power save	P34	Follow common design	2010/1/22	DVT->PVT
21	Update JTP1 footprint--> E-T_6916-Q06N-00R_6P	P33	ME request	2010/1/25	DVT->PVT
22	Update USB20_P10-->USB20_P5,USB20_N10-->USB20_N5	P21 P26	Follow common design	2010/1/25	DVT->PVT
23	Update JHDMI1 footprint-->SUYIN_100042GR019M23BZR_19P-T	P19	ME request	2010/1/25	DVT->PVT
24	R900 pin 1 and R904 pin1 +B-->+VSB	P34	HW request	2010/1/27	DVT->PVT
25	Add J2 J3 for +3V_ALW and +5V_ALW	P34	HW request	2010/1/27	DVT->PVT
26	R808 pin 1,R809 pin2 +3VALW-->+3V_ALW and +5VALW-->+5V_ALW	P33	HW request	2010/1/27	DVT->PVT
27	Add R907 for USB_EN# PH	P29	HW request	2010/1/27	DVT->PVT
28	Del R808 R809 R811 R810 R258 Q8 R259 Q9	P33	HW request	2010/1/27	DVT->PVT
29	R238 pin1 +3VALW-->+3V_ALW	P31	HW request	2010/1/29	DVT->PVT
30	JTP1 pin1 +3VALW-->+3V_ALW	P33	Follow common design	2010/1/29	DVT->PVT
31	Del R246	P32	HW request	2010/1/29	DVT->PVT
32	Add LPC_FRAME#, LPC_AD, LPC_AD1,LPC_AD2,LPC_AD3 JWAN1	P26	HW request	2010/1/29	DVT->PVT
33	Update JPB1 footprint P-TWO_161011-04021_4P-T	P33	ME request	2010/1/29	DVT->PVT
34	Add JHDD2 ACES_87036-1001-CP_10P	P25	HW request	2010/1/29	DVT->PVT
35	Fine tune JP4 pin define for EMI request	P17	EMI request	2010/1/29	DVT->PVT
36	<BOM> Update UA1 P/N for Audio VB version	P28	Vender update P/N	2010/1/29	DVT->PVT
37	Update JP5 pin define and 20pin-->22pin	P29	HW request	2010/1/30	DVT->PVT
38	<BOM> R133 8.2K-->11.8K same as EVT	P21	HW request	2010/1/31	DVT->PVT
39	Add C909 C910	P17	EMI request	2010/1/31	DVT->PVT
40	Add D18 and R908 on RTC circuit	P20	Follow common design	2010/1/31	DVT->PVT
41	JHDD1 10pin-->12pin	P29	Add more power and GND pin on HDD conn	2010/1/31	DVT->PVT
42	Add R909 R910 for ADAPTOR_SEL	P31	Follow common design	2010/1/31	DVT->PVT
43	Add L41 L42 L43 C911 C912 C913 for EMI request	P12	EMI request	2010/2/2	DVT->PVT
44	C240 C244 22P to 18P	P20	Solve RTC fiaf issue	2010/2/2	DVT->PVT
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Doc# 1, Monday, March 24, 2010 1:38pm 45 of 45					