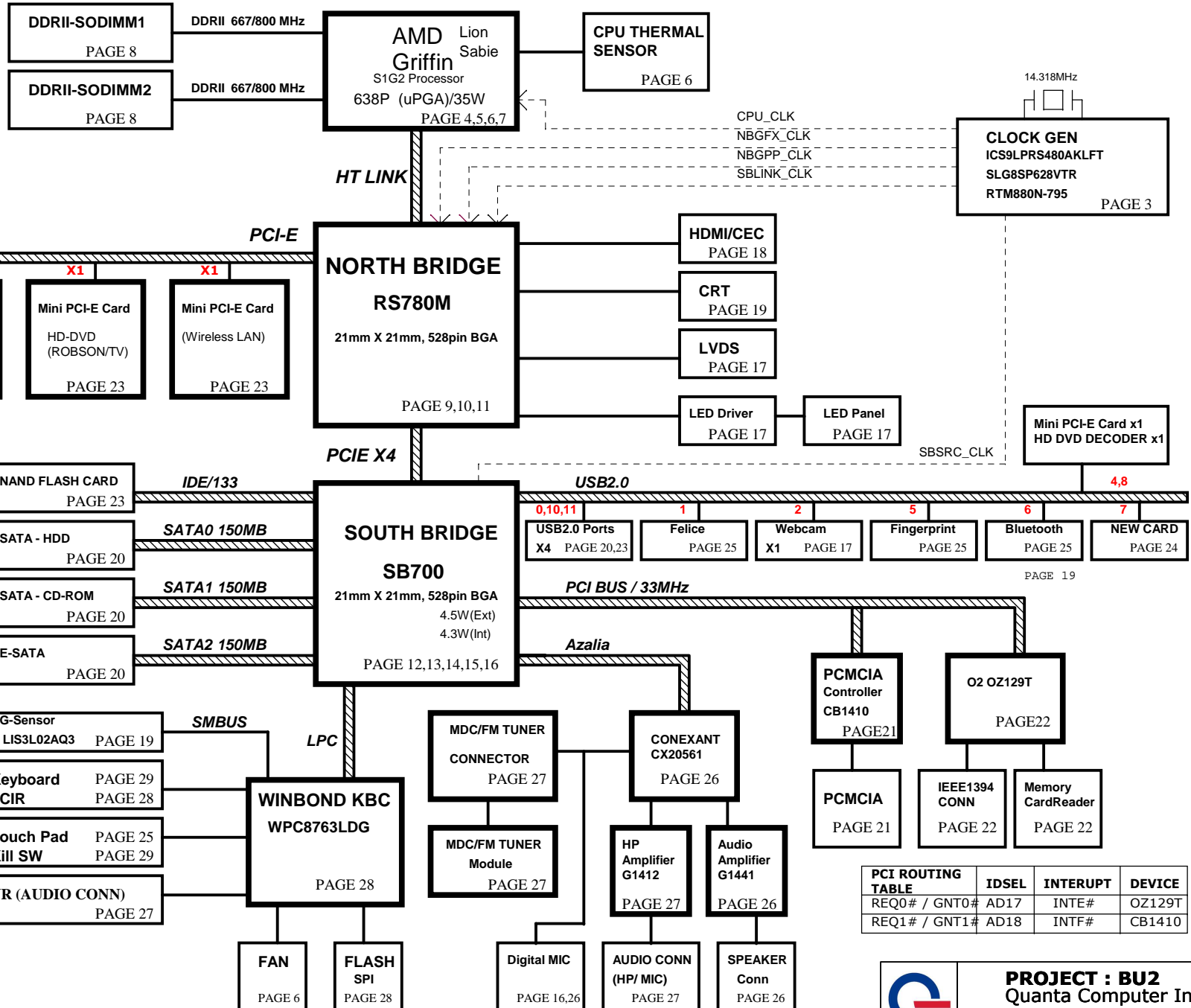



PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT



PCI ROUTING TABLE	IDSEL	INTERRUPT	DEVICE
REQ0# / GNT0#	AD17	INTE#	OZ129T
REQ1# / GNT1#	AD18	INTF#	CB1410



PROJECT : BU2
Quanta Computer Inc.

Size Custom

Document Number
BLOCK DIAGRAM

Date: Wednesday, January 30, 2008 | Sheet 1 of 35

Rev 1A

PAGE#	DESCRIPTION	NOTE
1	SCHEMATIC BLOCK DIAGRAM	
2	SYSTEM INFORMATION	
3	CLOCK GENERATOR_SLG8SP628	
4	S1G2 HT I/F 1/4	
5	S1G2 DDRII MEMORY I/F 2/4	
6	S1G2 CTRL & DEBUG 3/4	
7	S1G2 PWR & GND 4/4	
8	DDR2 SODIMMS: A/B CHANNEL	
9	RS740/RS780-HT LINK/PCIE I/F 1/4	
10	RS740/RS780-SYSTEM I/F 3/5	
11	RS740/RS780-POWER5/5	
12	SB700-PCIE/PCI/CPU/LPC 1/4	
13	SB700-ACPI/GPIO/USB 2/4	
14	SB700-ACPI/GPIO/USB 2/4	
15	SB700-PWR/DECOUPLING 4/4	
16	SB700-STRAPS & PWRGD	
17	LCD/LED PANEL/LID/CAMERA	
18	HDMI/HDMI-CEC(R5F211A)	
19	CRT & G-SENSOR(LIS3L02A)	
20	SATA HDD/ODD & ESATA/USB	
21	PCMCIA(CB1410) -OPTION	
22	OZ129T(5IN1/1394)	
23	MINI CARD & NAND FLASH CARD	
24	NEW CARD & RJ45 BOARD/BEEP	
25	TP/FP/BT/PB/FELICA/MMB CONN	
26	CONEXANT(CX205601)/SPK/AMP	
27	JACK/VR/FM/MIC/MDC/AMPLIFIER	
28	EC(KBC)-WPCPC8763/WPC8769	
29	KEYBOARD/LED/KILL SW/HOLE	
30	CHARGER (ISL6251A)	
31	SYSTEM 5V/3V (ISL6237)	
32	AMD GRIFFIN (ISL6265)	
33	+NB_CORE (RT8202)	
34	DDR 1.8V(TPS51116)	
35	DISCHARGE (1.25V/1.5V)	

AC IN

3V/5VPCU

NBSWON#

DNBSWON#

S5_ON/S5

RSMRST#

PCIE_WAKE#

SUSC

SUSB

SUSON

MAINON

VR_ON

CPU_CORE

VRM_PWRGD

1.2_ON

NB_CORE

HWPG

ECPWROK

NB_PWRGD_IN

SB_PWRGD_IN

CPU CLK IN

CPU RESET

CPU POWER OK

CPU_LDTSTOP#

SB700 SM BUS

SB700 SMBUS	SMBUS Function Define
SMBCLK0 SMBDAT0	DDR / DDR THER / CLOCK GEN (+3V)
SMBCLK1 SMBDAT1	Mini Card/New Card (+3VS5)
SMBCLK2 SMBDAT2	HDMI CEC (+3VS5)

KBC(EC) SM BUS

KBC SMBUS	SMBUS Function Define
MBCLK MBDAT	BATTERY (+3VPCU)
2ND_MBCLK 2ND_MBDATA	CPU THER / SENSOR/EC (+3V/PCU)
3ND_MBCLK 3ND_MBDATA	HDMI CEC / TOUCH SEN(+3VS5)

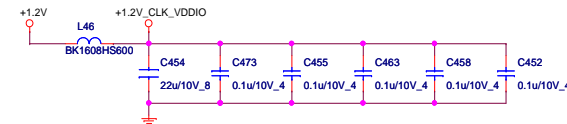
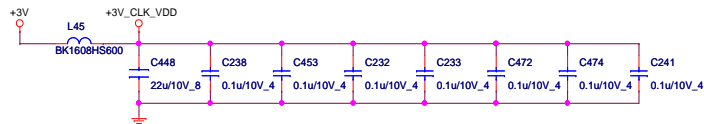


NB4

PROJECT : BU2
Quanta Computer Inc.

Size
CustomDocument Number
SYSTEM INFORMATIONRev
1A

Date: Thursday, November 08, 2007 Sheet 2 of 35



ICS9LPRS480

P/N :

SLG8SP628

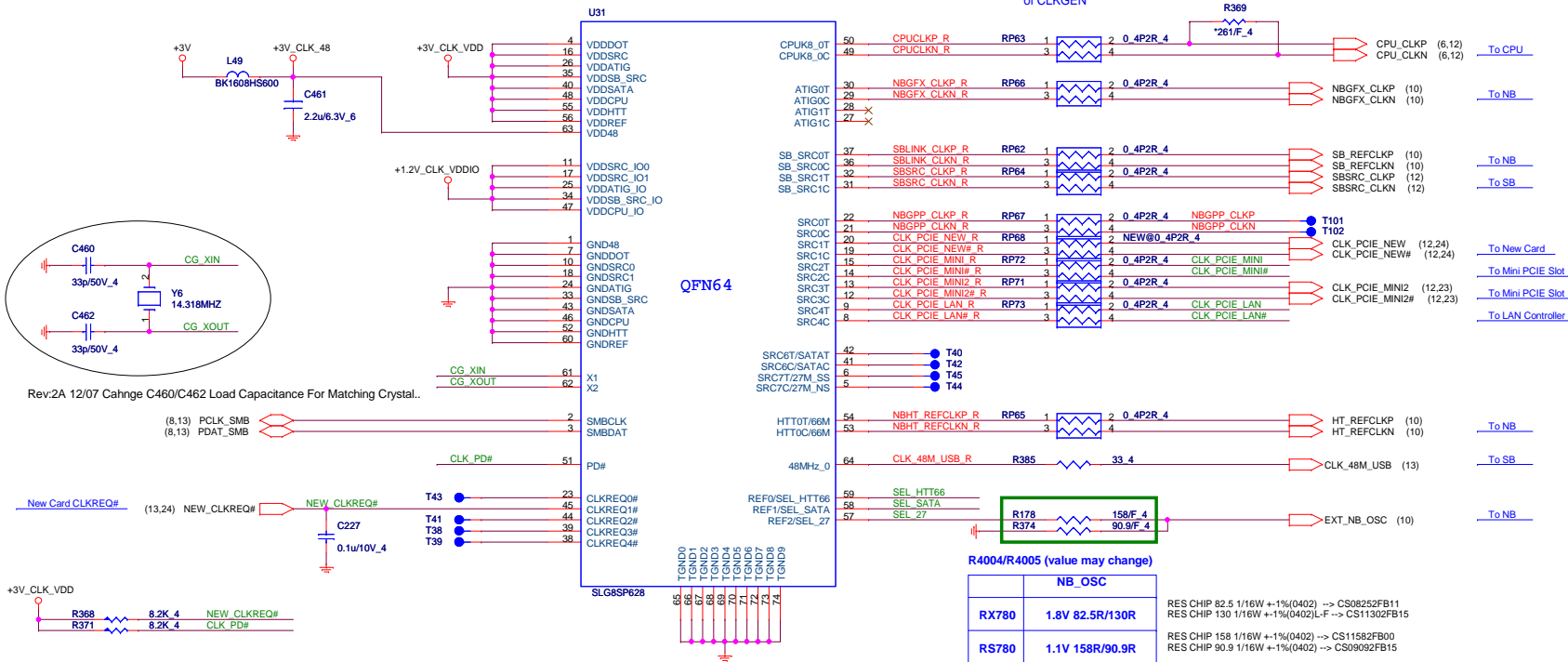
P/N : AL8SP628000

RTM880N-796

P/N : AL000880000

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

Place within 0.5" of CLKGEN



NB CLOCK INPUT TABLE

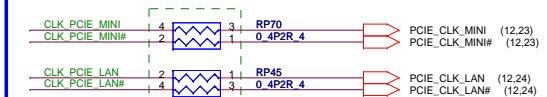
NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT	
GPPSB_REFCLK	100M DIFF	100M DIFF

R4004/R4005 (value may change)

	NB_OSC
RX780	1.8V 82.5R/130R
RS780	1.1V 158R/90.9R

RES CHIP 82.5 1/16W +/-1%(0402) -> CS08252FB11
 RES CHIP 130 1/16W +/-1%(0402)L-F -> CS11302FB15
 RES CHIP 158 1/16W +/-1%(0402) -> CS11582FB00
 RES CHIP 90.9 1/16W +/-1%(0402) -> CS09092FB15

FOR EXTERNAL/INTERNAL CLOCK



Place Close to Drivers Side

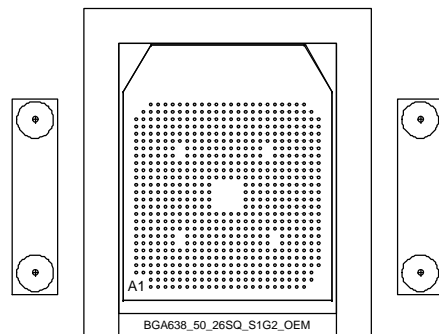
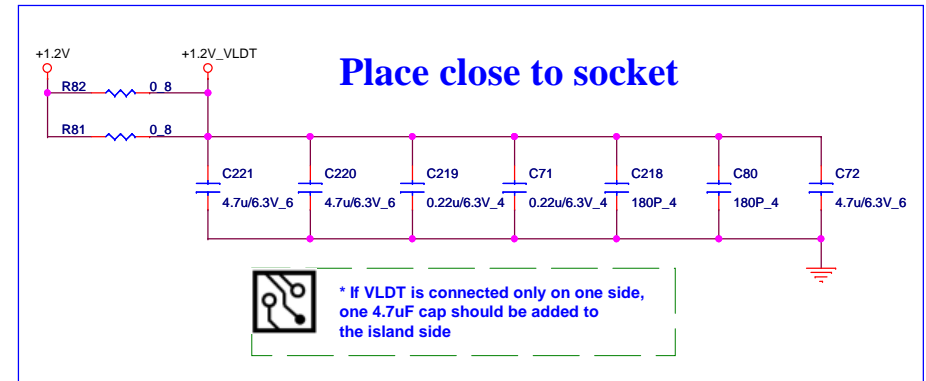
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default



PROJECT : BU2
Quanta Computer Inc.

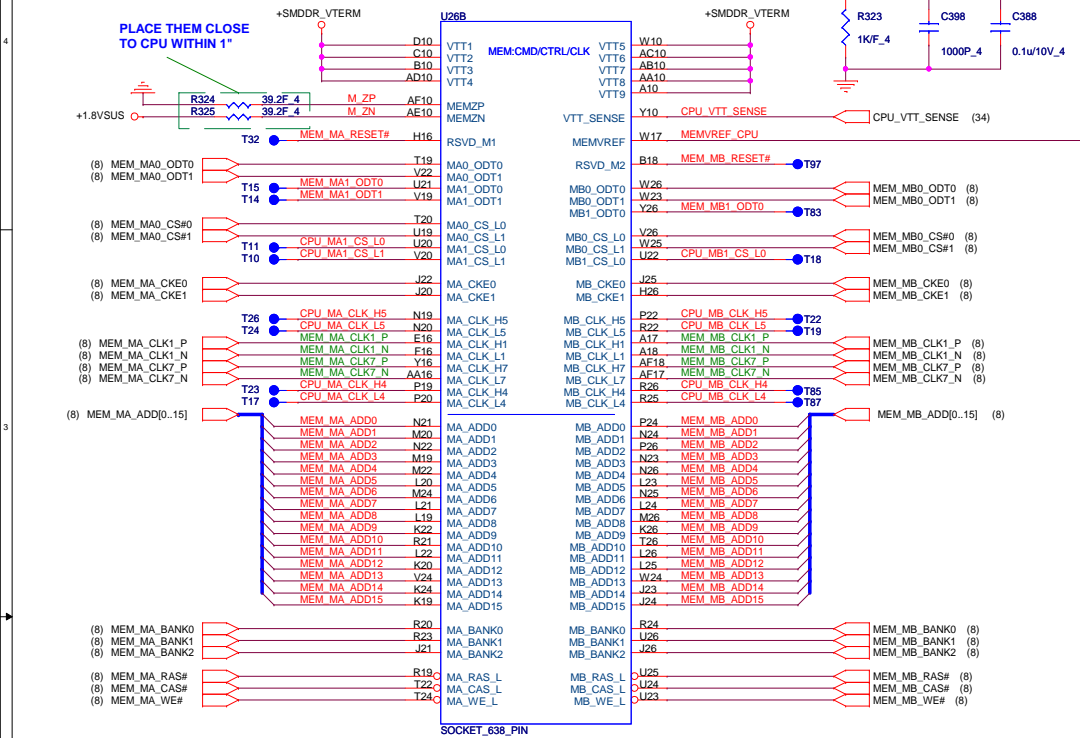
Size Custom Document Number
CLK GENERATOR_SLG8SP628 Rev 1A
 Date: Thursday, July 24, 2008 Sheet 3 of 35



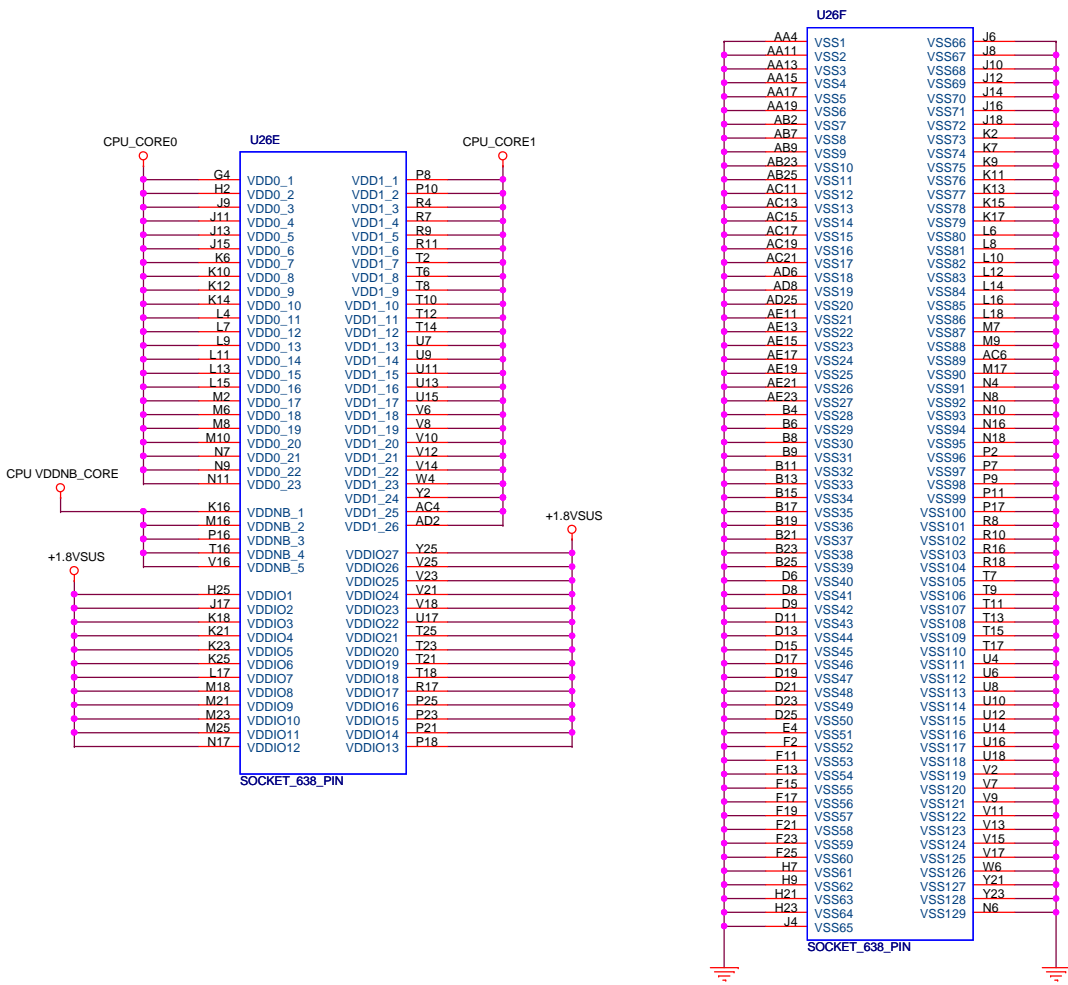
PROJECT : BU2
Quanta Computer Inc.

Size B	Document Number S1G2 HT I/F 1/4	Rev 1A
Date: Thursday, July 24, 2008		Sheet 4 of 35

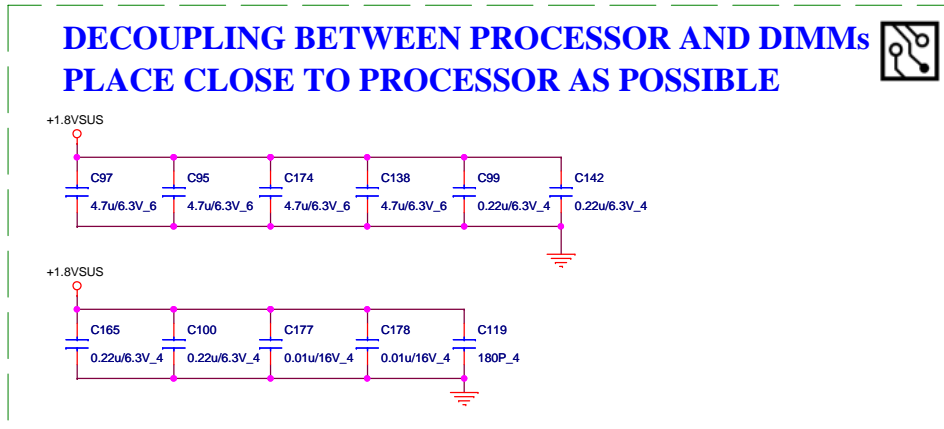
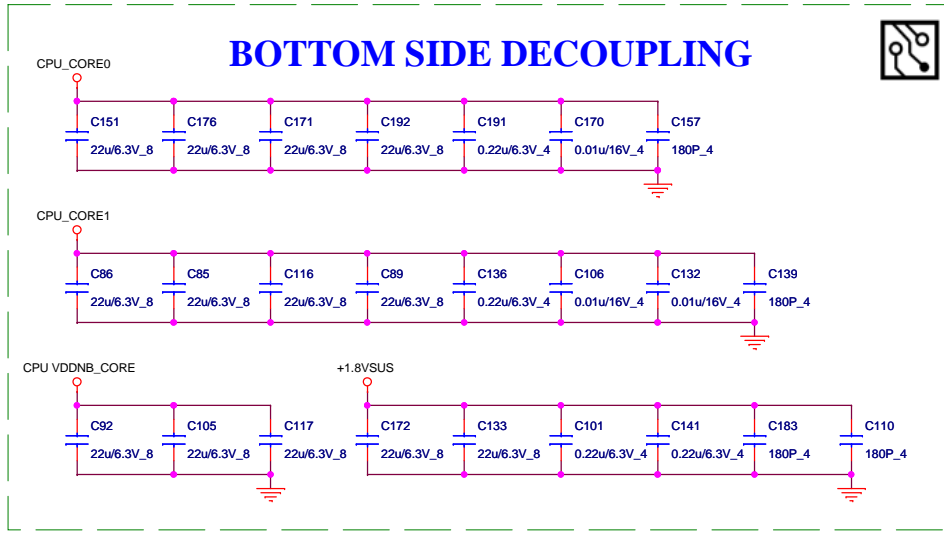
Processor Memory Interface



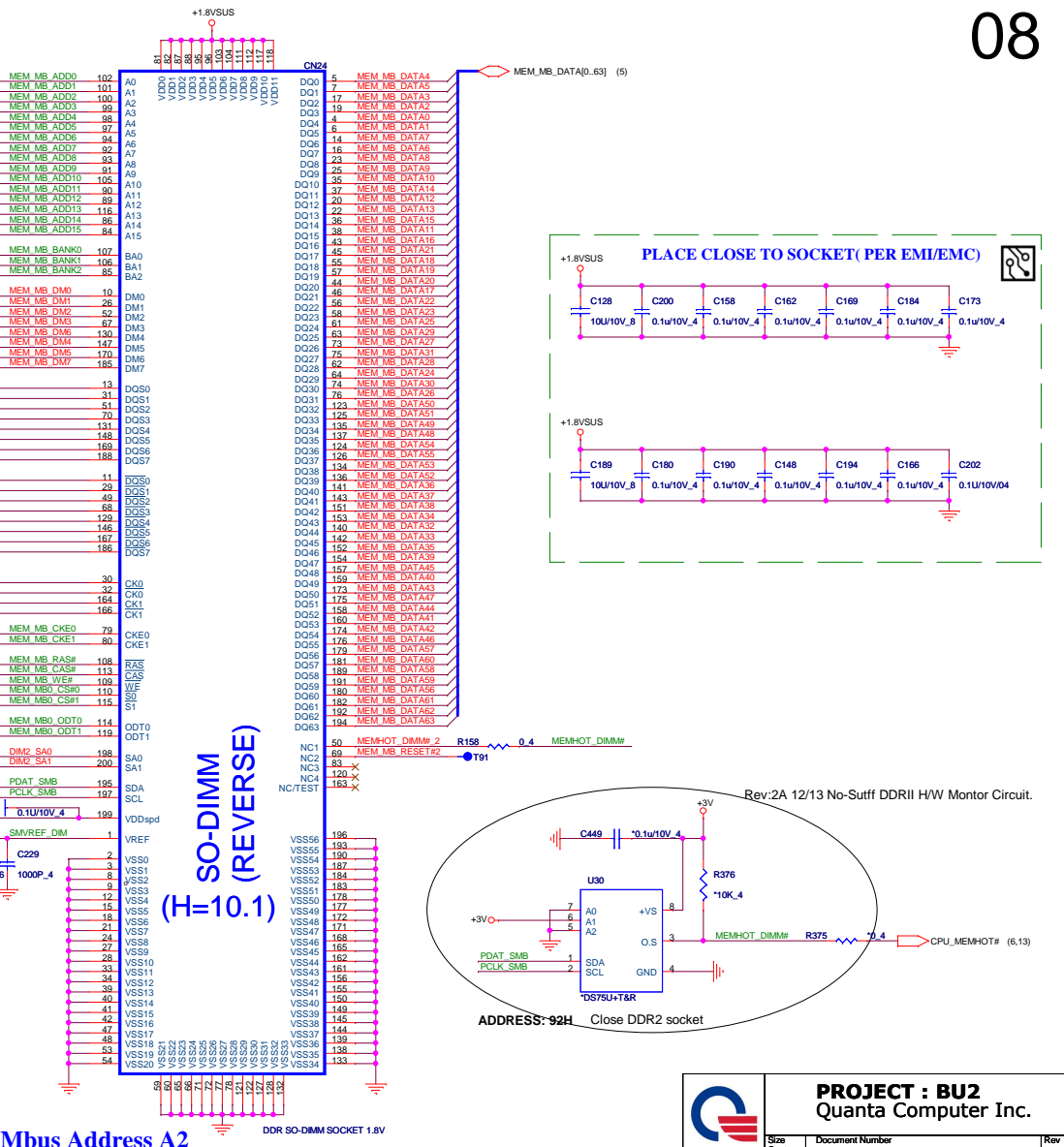
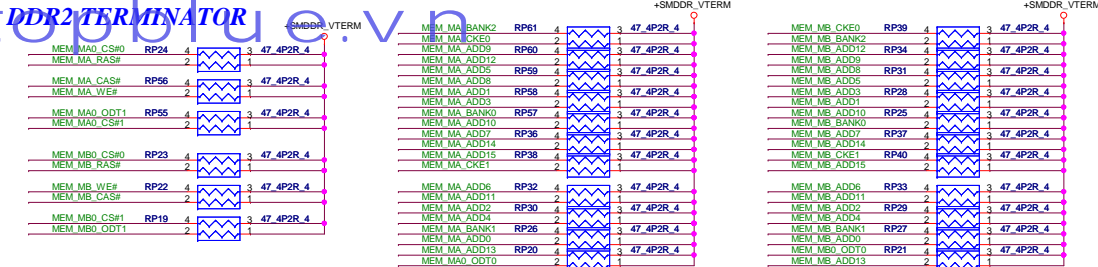
CPU



PROCESSOR POWER AND GROUND



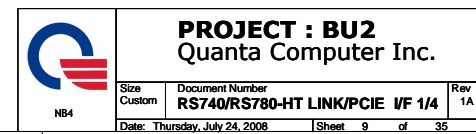
...*DDR2 TERMINATOR*



tor Circuit.

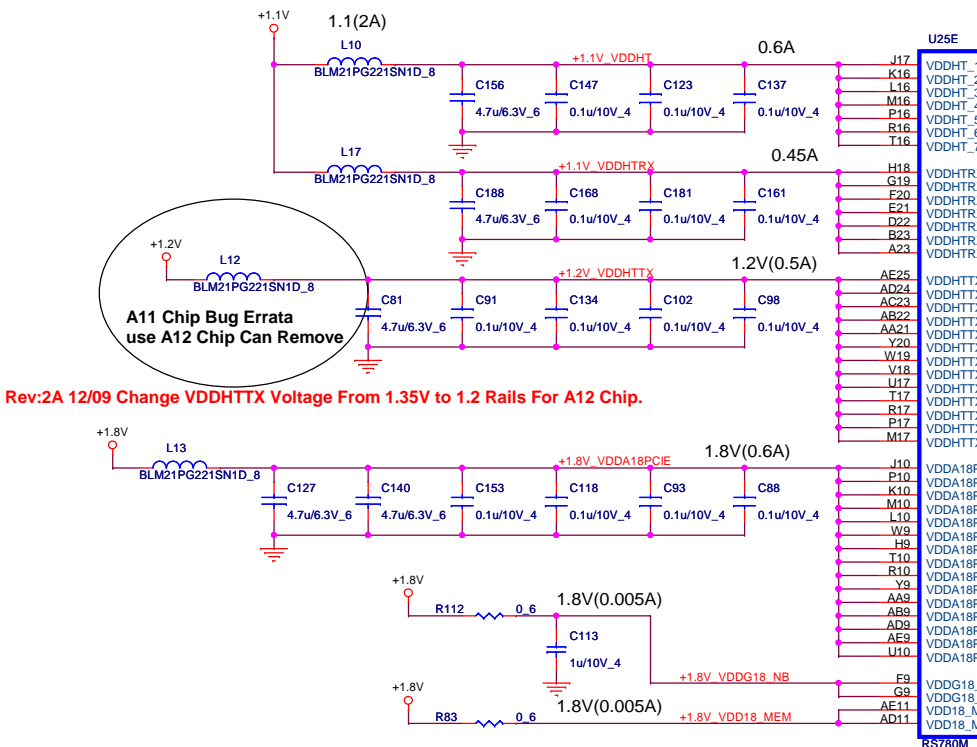
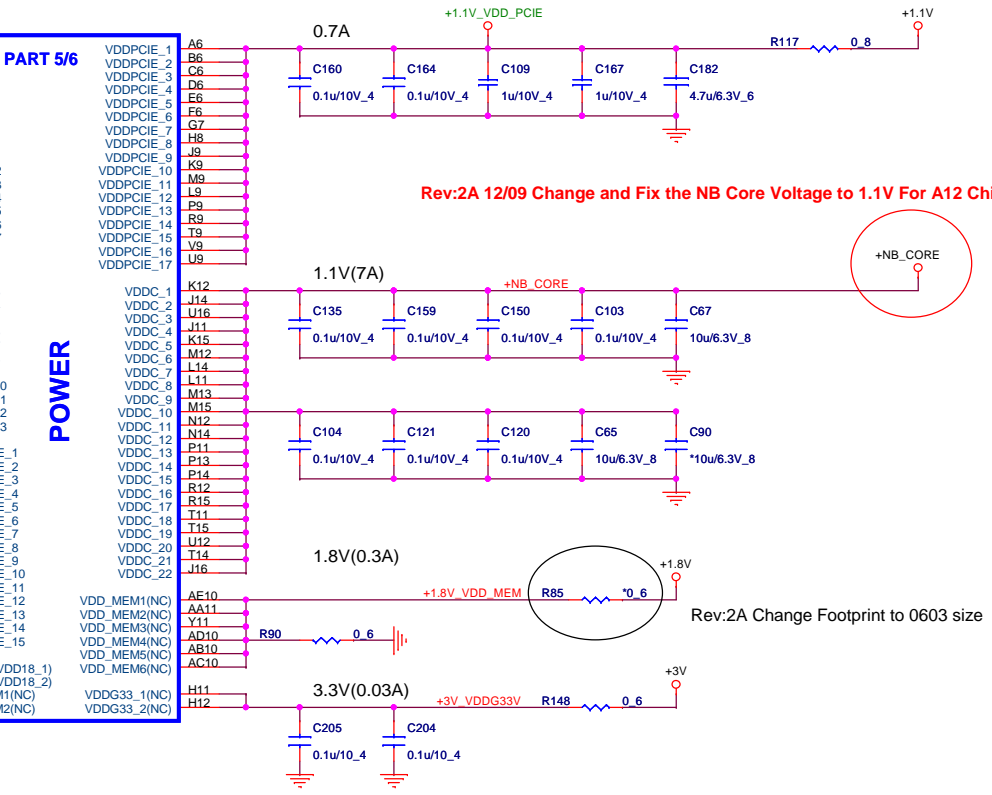
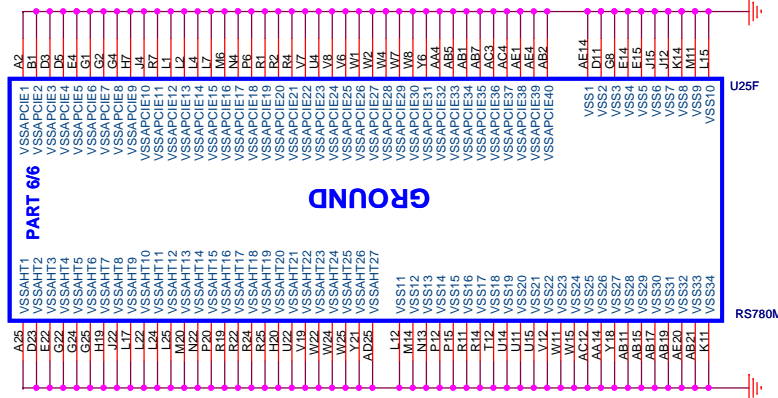
NB4

Size Custom	Document Number DDR2 SODIMMS: A/B CHANNEL	R
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RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDDG18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDDG33	+3.3V	NC	+3.3V	VDDL18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDL18	+3.3V	NC	NC



Rev:2A 12/09 Change VDDHTTX Voltage From 1.35V to 1.2V Rails For A12 Chip.

Rev:2A 12/09 Change VDDHTTX Voltage From 1.35V to 1.2V Rails For A12 Chip.

Rev:2A 12/09 Change VDDHTTX Voltage From 1.35V to 1.2V Rails For A12 Chip.

Rev:2A 12/09 Change VDDHTTX Voltage From 1.35V to 1.2V Rails For A12 Chip.

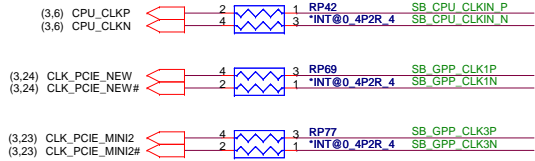
RS780



PROJECT : BU2
Quanta Computer Inc.

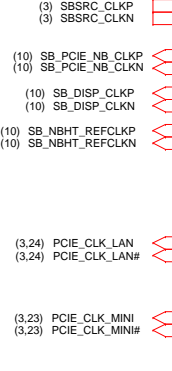
Size Custom	Document Number RS740/RS780-POWER5/5	Rev 1A
Date: Thursday, April 10, 2008	Sheet 11 of 35	

FOR INTERNAL CLOCK

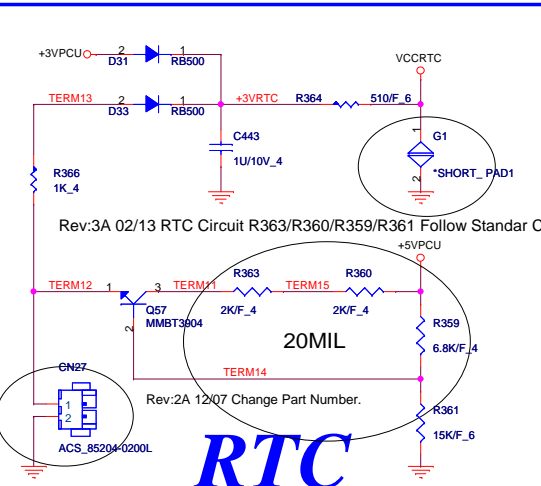


Place close to CLK GEN

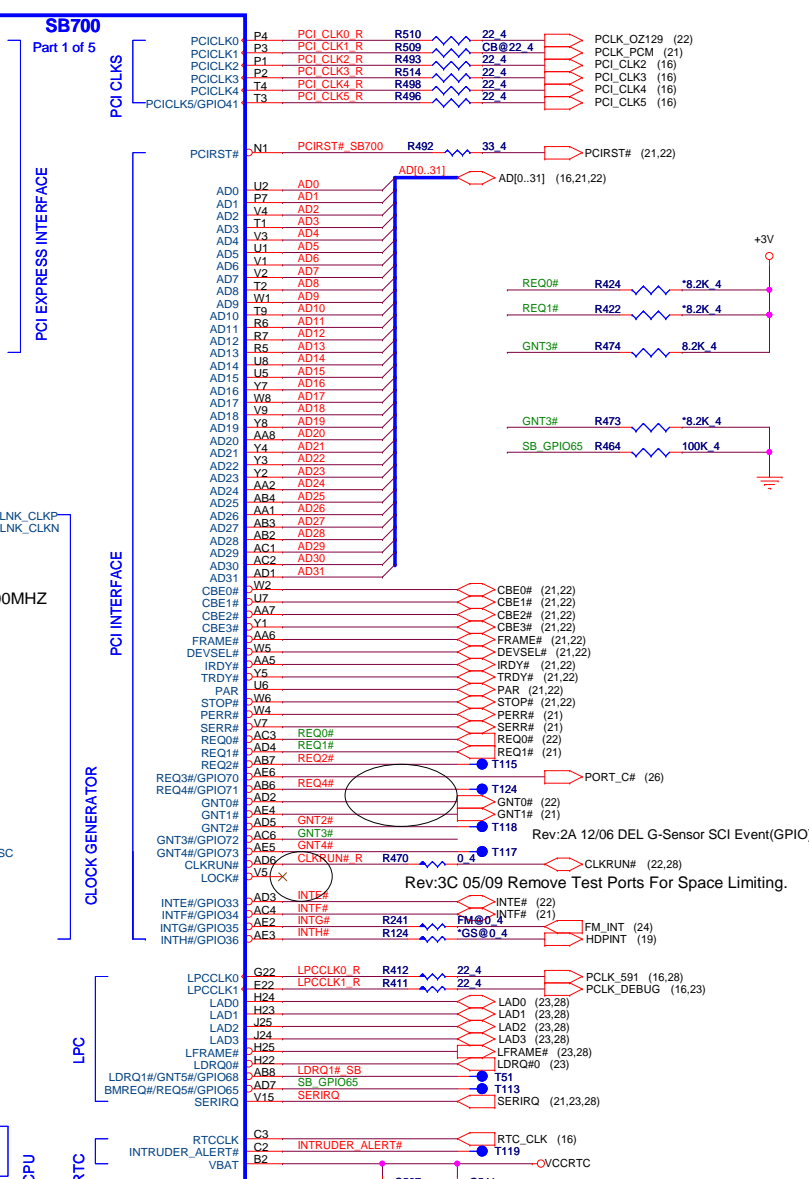
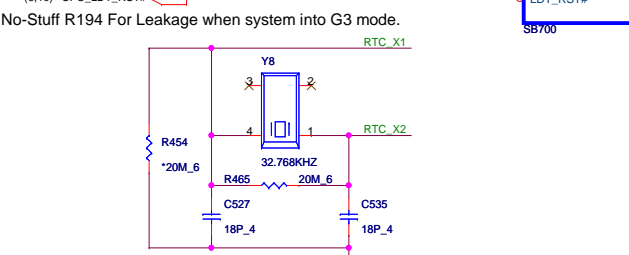
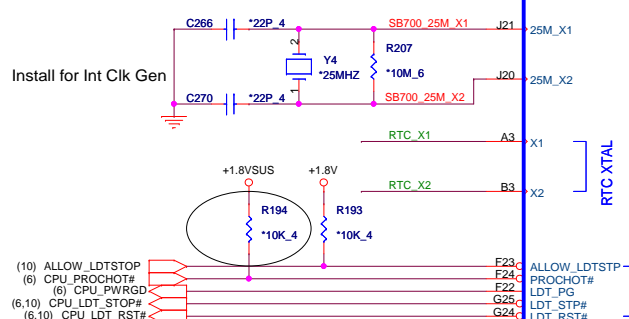
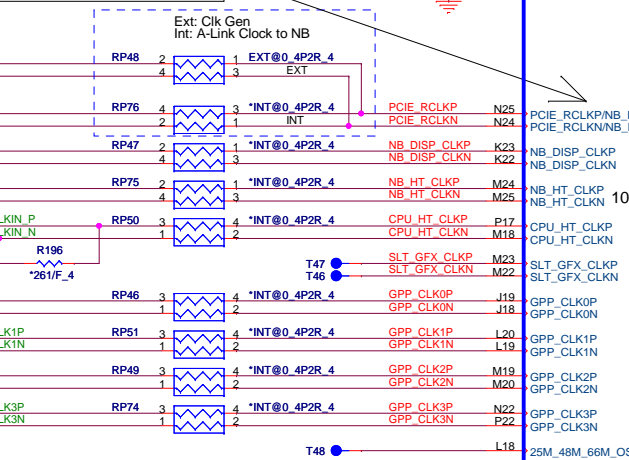
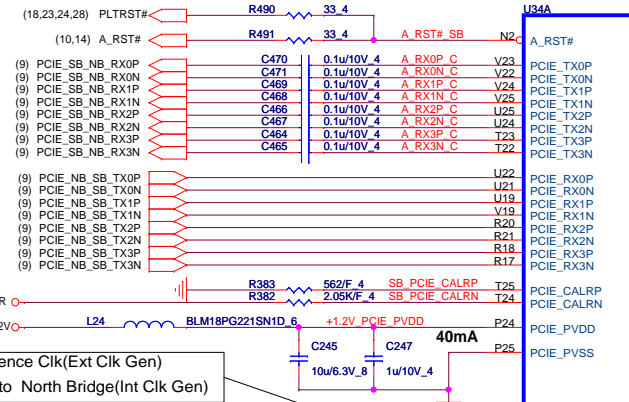
From Clk Gen Input
To NB A-Link CLK
For North Bridge
For North Bridge
For CPU Host Clk

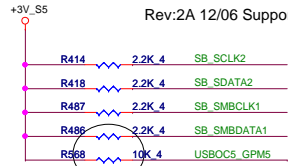
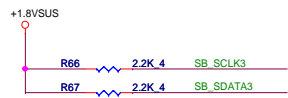


Rev:3B 04/02 As the same location Name(G1) For Toshiba Service Team Request.

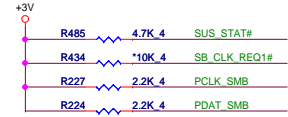


RTC



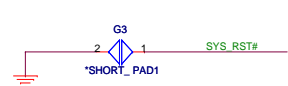


Rev:3B 04/07 USB Overcurrent 5 Pull-up 10K For Open Drain.



Rev:2A 12/06 Support the New Card Hot Plug Function.

Rev:3A 02/05 Move Board ID4 Pin Name From GPIO66 to GPIO3.



Rev:3B 04/07 Added the USB Overcurrent 3 to Support USB 2.0 Ports.

Rev:3A 02/05 Move Hot Plug Pin Name From GEVENT5# to GPM1#.

HD Audio Interface

To Azalia



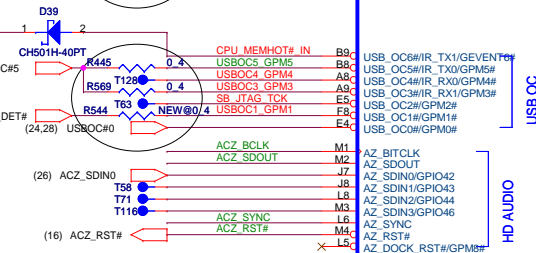
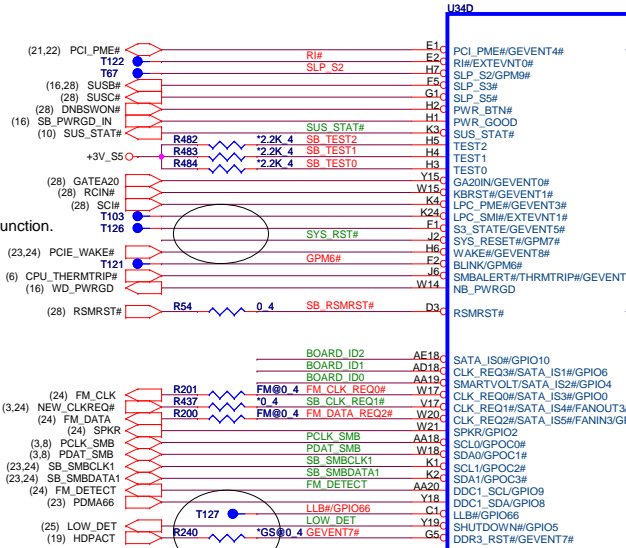
To Azalia



To Azalia



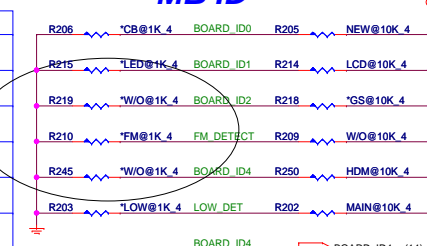
To Azalia



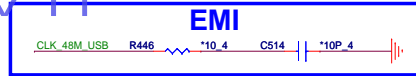
MB ID Selection Table

BOARD_ID	BOARD_ID0	BOARD_ID1	BOARD_ID2	FM_DETECT	BOARD_ID4	LOW_DET
W/ New Crad W/ Crad Bus	H	L				
W/ CCFL Panel W/ LED Panel		H	L			
W/ G-Sensor W/O G-Sensor			H	L		
W/O FM W/FM				H	L	
W/ HDMI W/O HDMI					H	L
Main Stream Low Cost						H

MB ID



Rev:3B 04/18 There is internal 8.2K of I/O Balls So Change Pull-Down Resistors From 10K to 1K.



48MHz

CLK_48M_USB (3)

USB_RCOMP SB R238 11.8K/F 6

Rev:3C 04/08 Reserve the 0hm to USB7 Controller.

Rev:3A 03/03 Swap USB CONN From USB11 to USB7 For Controller ESATA Certification.

Rev:2A 12/11 Swap the New Card From USB7 to USB3 For OHCI Controllers.

USB_FSD13P E6 X

USB_FSD13N E7 X

USB_FSD12P F7 X

USB_FSD12N E8 X

USB_HSD11P H11 X

USB_HSD11N J10 X

USB_HSD10P E11 X

USB_HSD10N E11 X

USB_HSD9P A11 X

USB_HSD9N B11 X

USB_HSD8P C10 X

USB_HSD8N D10 X

USB_HSD7P G11 X

USB_HSD7N H12 X

USB_HSD6P E12 X

USB_HSD6N E14 X

USB_HSD5P C12 X

USB_HSD5N D12 X

USB_HSD4P B12 X

USB_HSD4N A12 X

USB_HSD3P G12 X

USB_HSD3N G14 X

USB_HSD2P H14 X

USB_HSD2N H15 X

USB_HSD1P A13 X

USB_HSD1N B13 X

USB_HSD0P B14 X

USB_HSD0N A14 X

IMC_GPIO18 A18 X

IMC_GPIO19 B18 X

IMC_GPIO20 D21 X

IMC_GPIO21 F19 X

IMC_GPIO22 E20 X

IMC_GPIO23 E21 X

IMC_GPIO24 E19 X

IMC_GPIO25 E18 X

IMC_GPIO26 B24 X

IMC_GPIO27 B23 X

IMC_GPIO28 A23 X

IMC_GPIO29 A22 X

IMC_GPIO30 B22 X

IMC_GPIO31 B21 X

IMC_GPIO32 A21 X

IMC_GPIO33 D20 X

IMC_GPIO34 C20 X

IMC_GPIO35 A20 X

IMC_GPIO36 B19 X

IMC_GPIO37 B18 X

IMC_GPIO38 A19 X

IMC_GPIO39 D18 X

IMC_GPIO40 C18 X

IMC_GPIO41 C18 X

Input

E-SATA and USB Connector

TV/HD DECODER Min-Card

USB Connector

BLUETOOTH

FINGERPRINT

Min-Card

NEW CARD

CAMERA USB

Felica

USB Connector(RJ45 USB BOARD)

SPI/LPC define



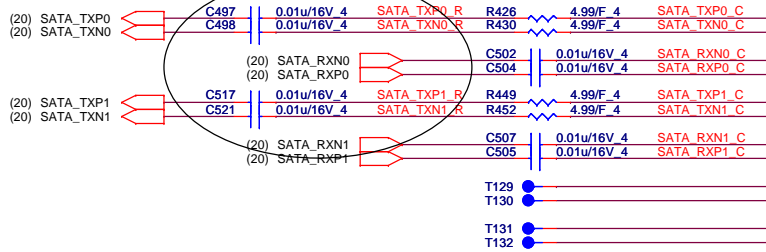
PROJECT : BU2
Quanta Computer Inc.

Size Custom Document Number
SB700-ACPI/GPIO/USB 2/4 Rev 1A
Date: Thursday, July 24, 2008 Sheet 13 of 35

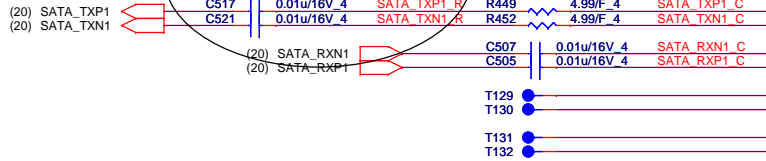
SB700

PLACE SATA AC COUPLING CAPS CLOSE TO SB700

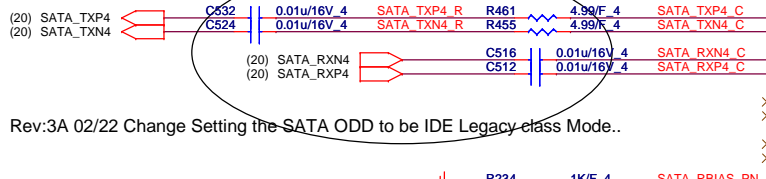
SATA HDD



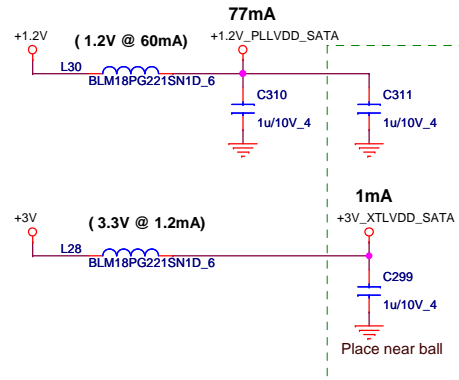
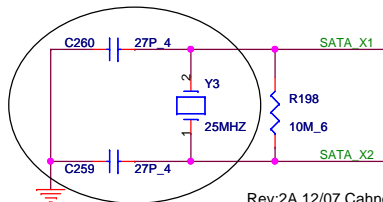
E-SATA



SATA ODD



NOTE:
R635 IS 1K 1% FOR 25MHZ XTAL, 4.99K 1% FOR 100MHZ INTERNAL CLOCK



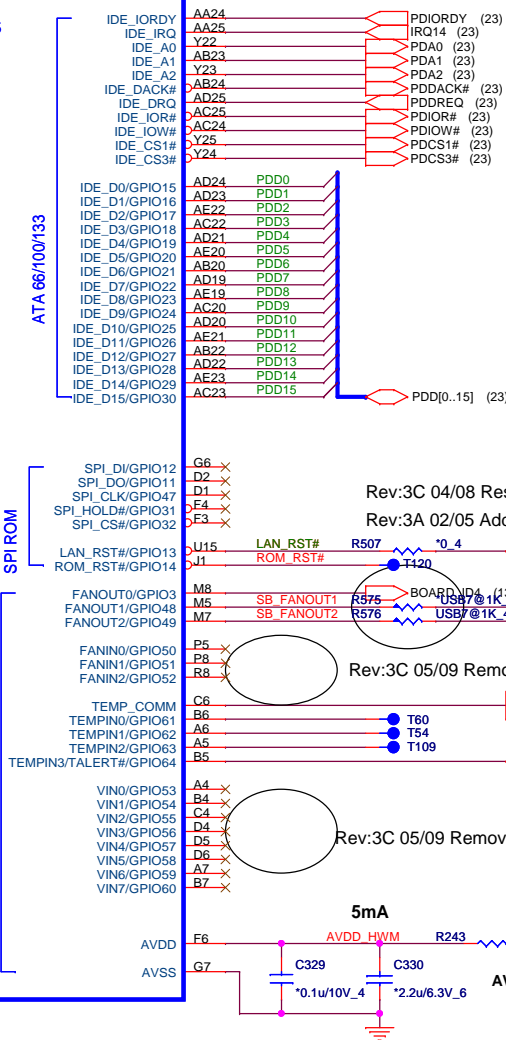
U34B

SB700 Part 2 of 5

SERIAL ATA

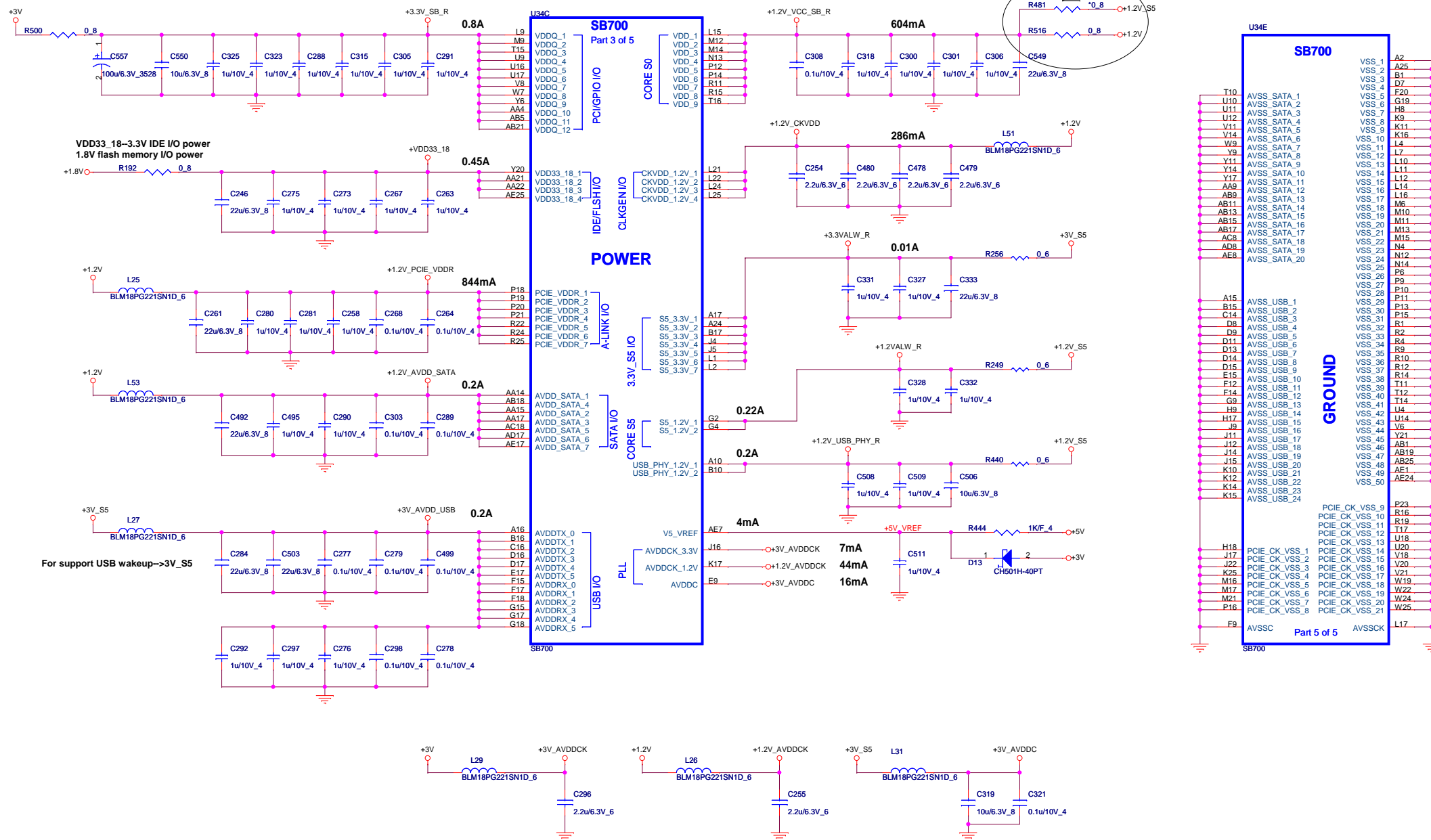
SATA PWR

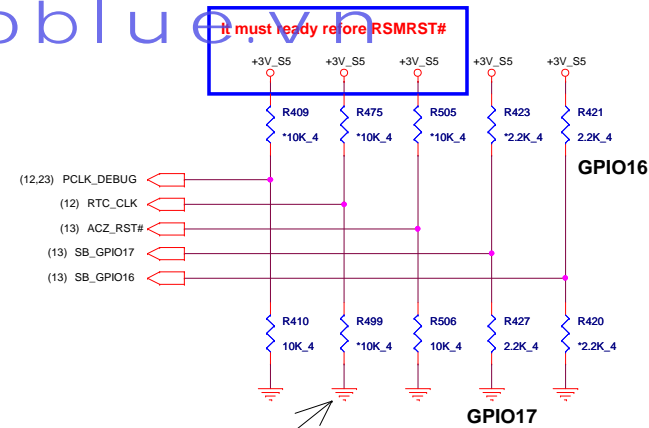
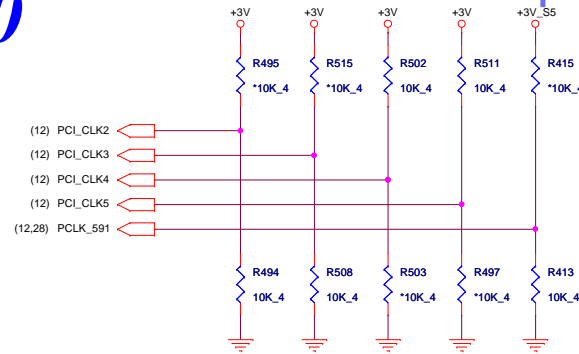
HW MONITOR



PROJECT : BU2
Quanta Computer Inc.

Size Custom	Document Number SB700-ACPI/GPIO/USB 2/4	Rev 1A
Date: Thursday, July 24, 2008	Sheet 14 of 35	



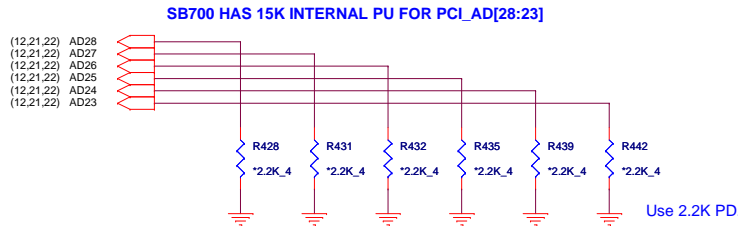


REQUIRED STRAPS

PULL HIGH	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0
	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT

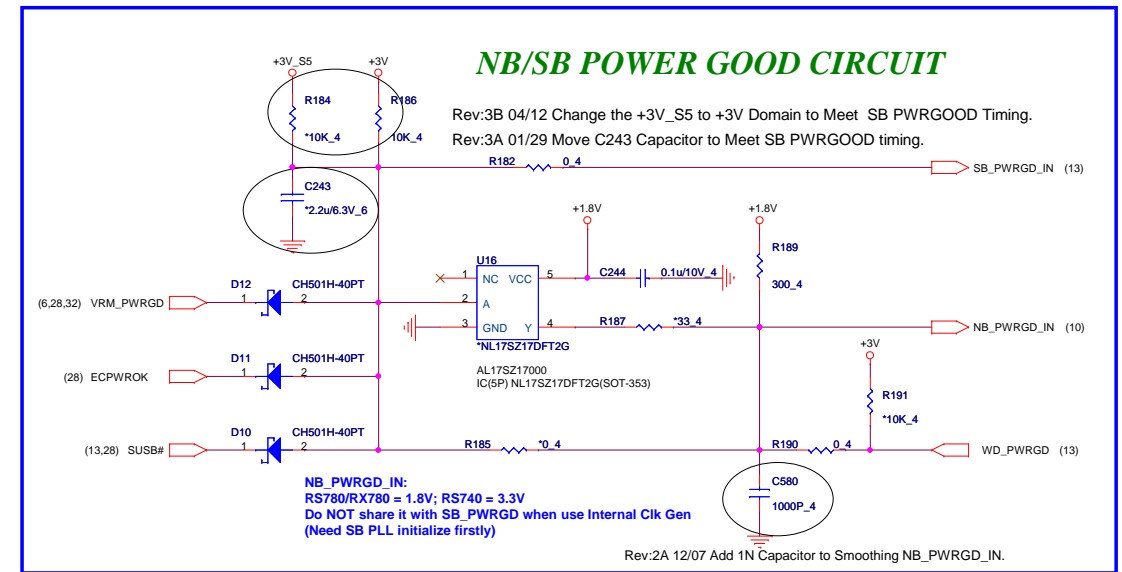
PULL HIGH	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17	GP16
	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED		ROM TYPE: H, H = Reserved H, L = SPI ROM
PULL LOW	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L, H = LPC ROM L, L = FWH ROM DEFAULT

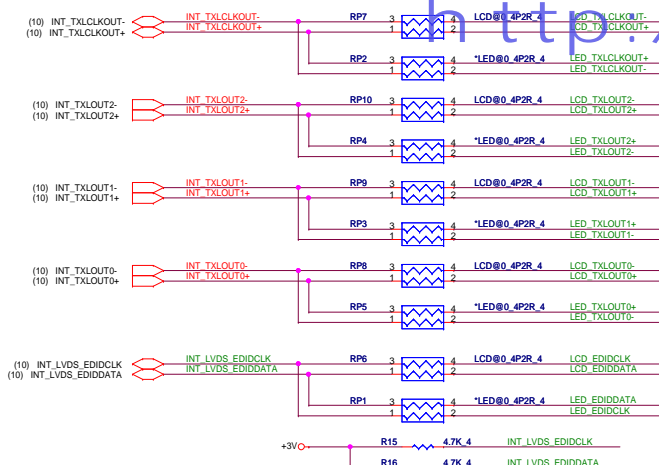
DEBUG STRAPS

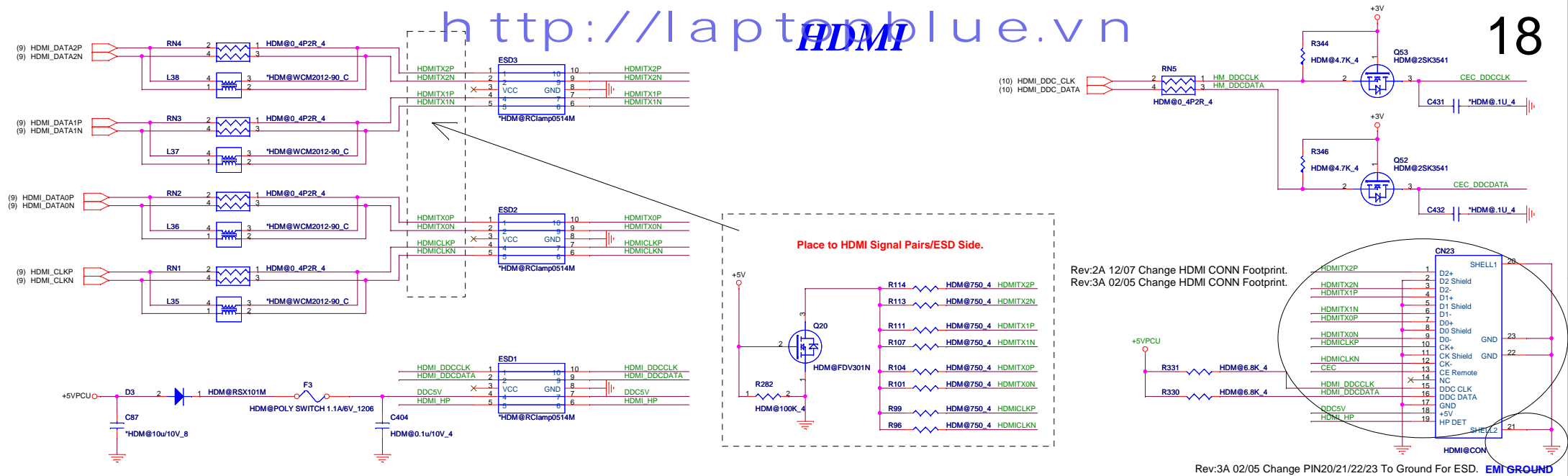


REQUIRED STRAPS

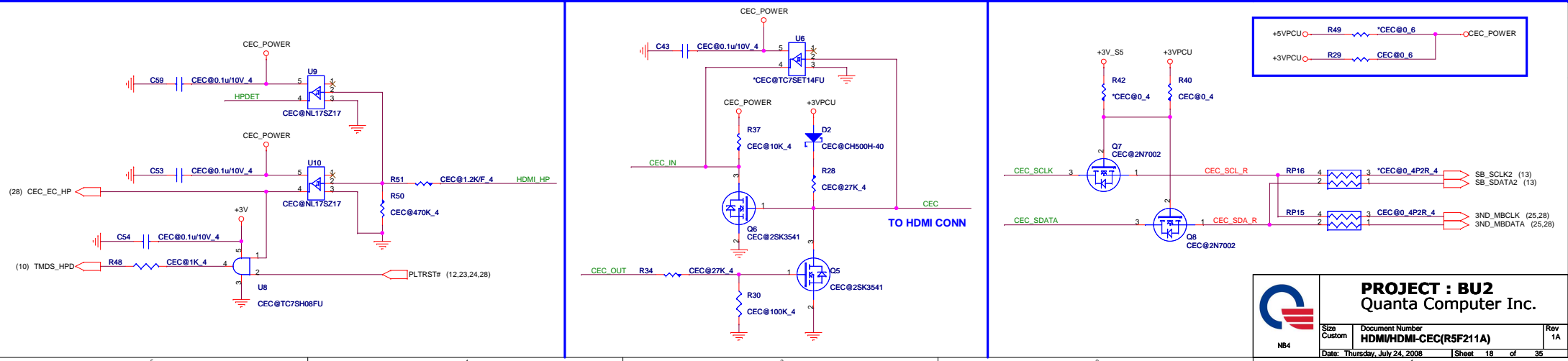
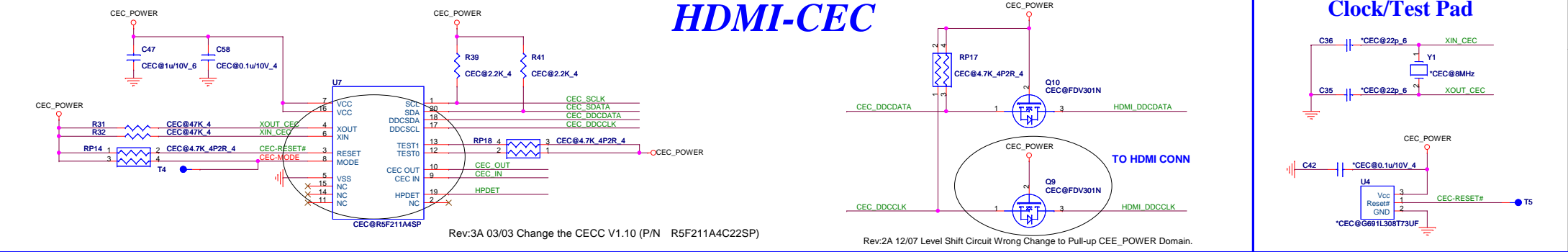
PULL HIGH	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

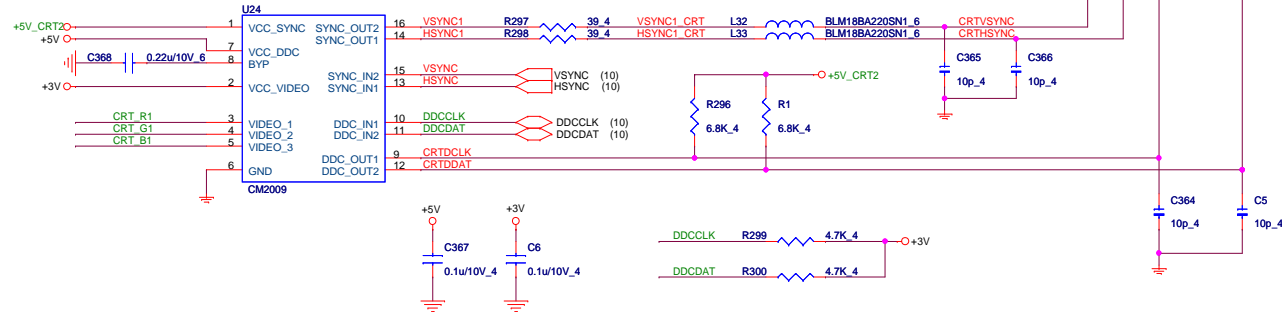




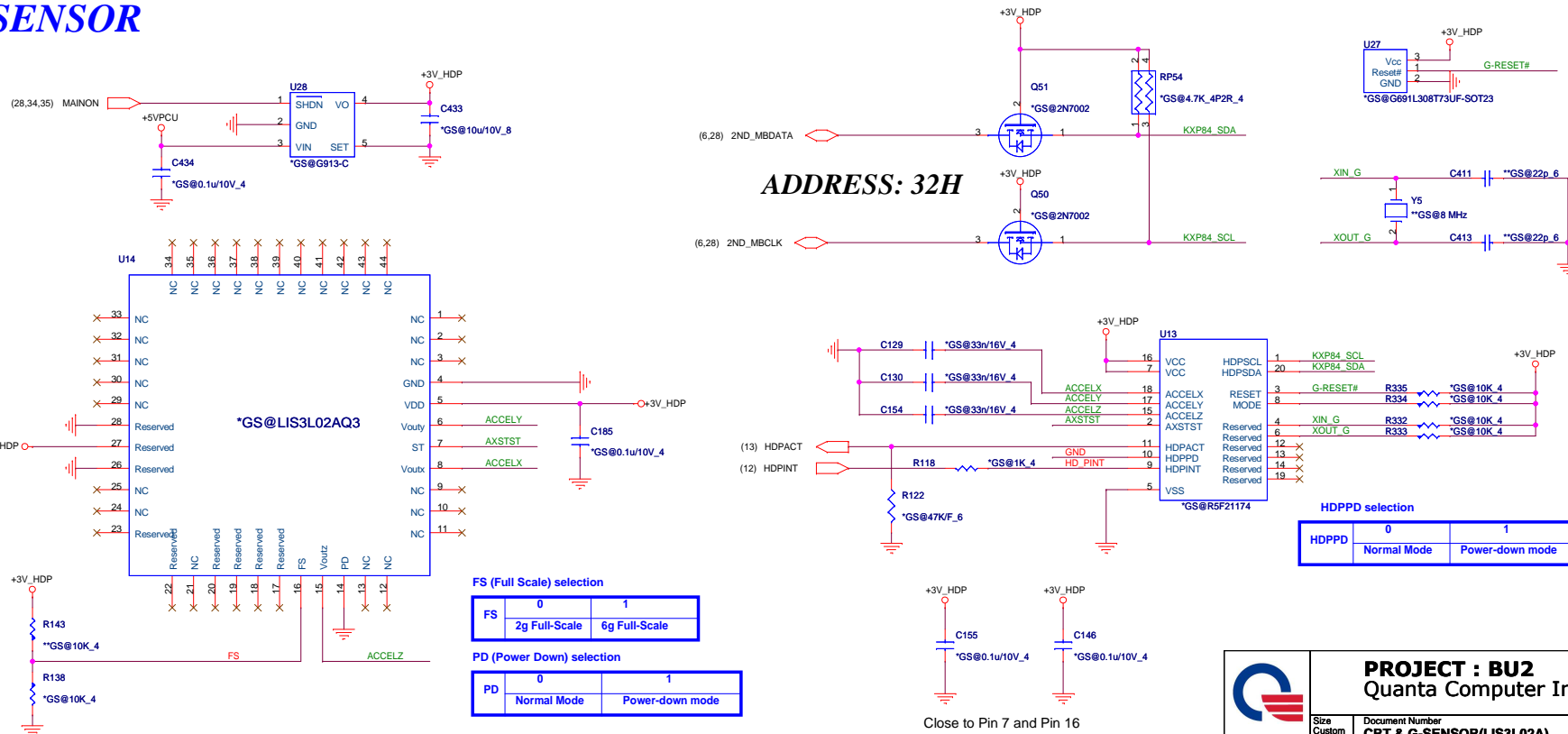


HDMI-CEC

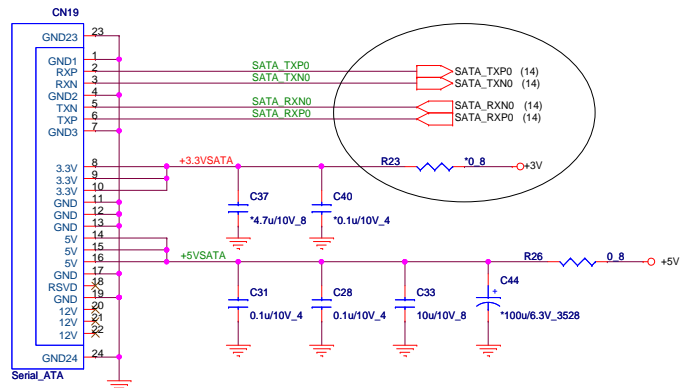




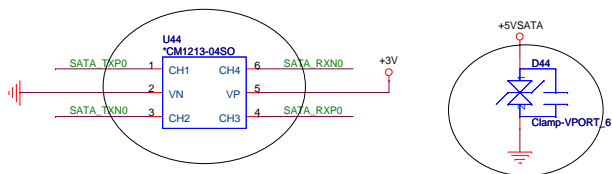
G-SENSOR



SATA HDD

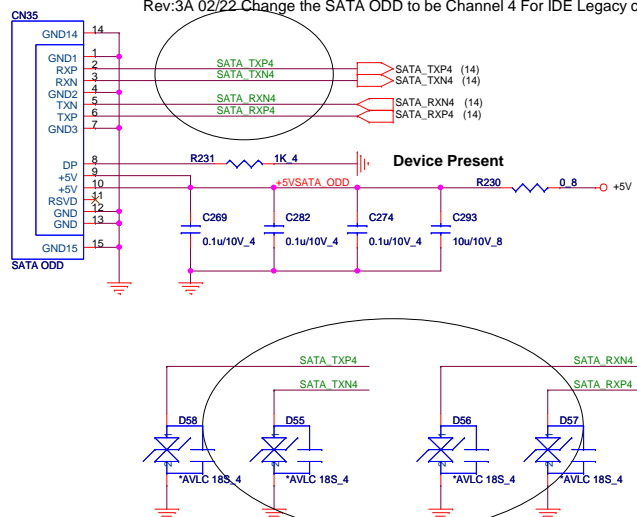


Rev:3B 04/18 Change HDD Control From Channel/2 to Channel/0 For Spin Down Issue.

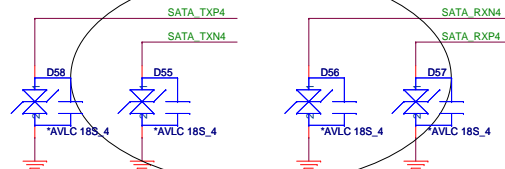


Rev:3B 04/18 Remove D51/D52/D53/D54 Varistor And Change to U44 CM1213-04SO ESD Protection Arrays.

SATA ODD

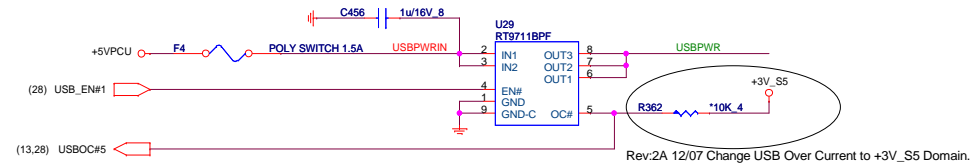


Rev:3A 02/22 Change the SATA ODD to be Channel 4 For IDE Legacy class Mode..



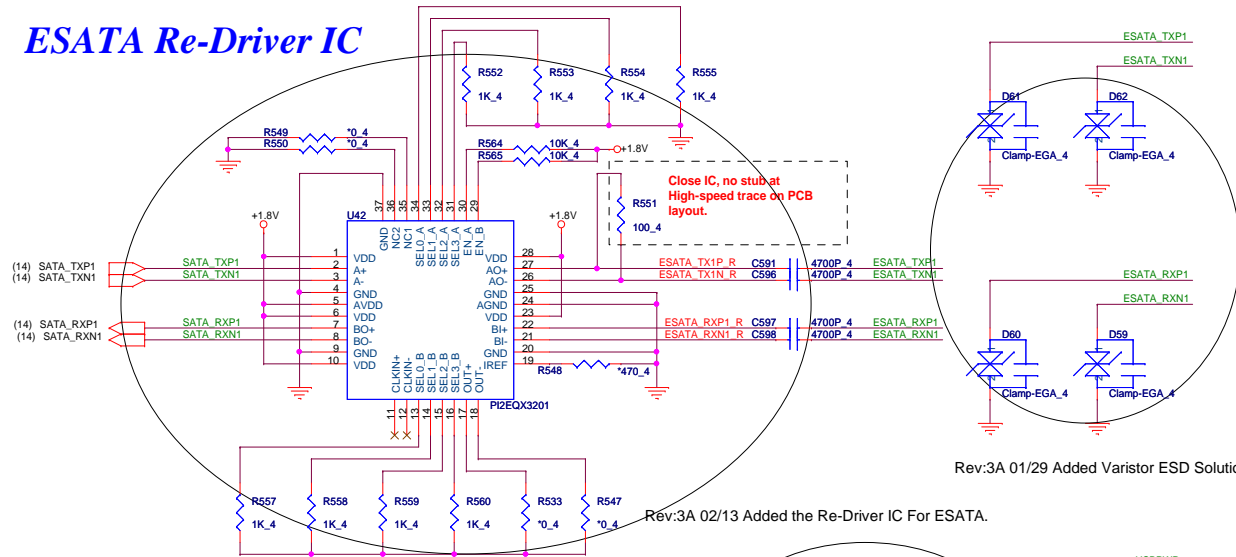
Rev:3A 01/29 Added Varistor ESD Solution.

USB & ESATA



Rev:2A 12/07 Change USB Over Current to +3V_S5 Domain.

ESATA Re-Driver IC



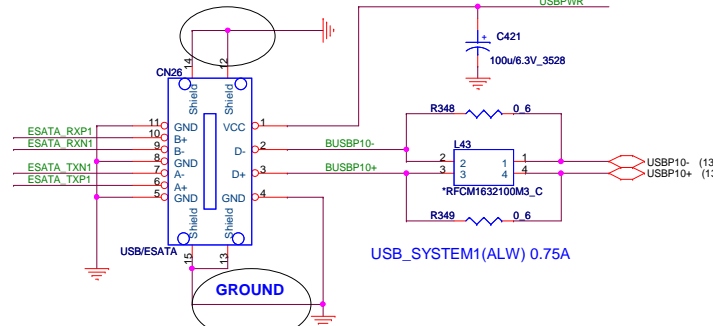
Rev:3A 01/29 Added Varistor ESD Solution.

Rev:3A 02/13 Added the Re-Driver IC For ESATA.

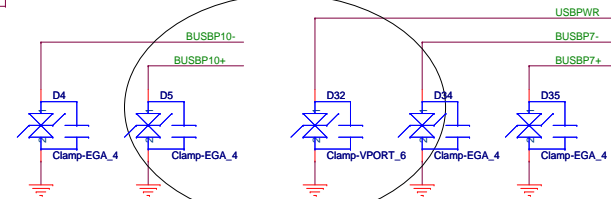
SEL0_X	SEL1_X	E _q	SEL2_X	Swing	SEL3_X	De-Emphasis
0	0	0dB	0	1.0X	0	0dB
0	1	2.5dB	1	1.2X	1	-3.5dB
1	0	4.5dB				
1	1	6.5dB				



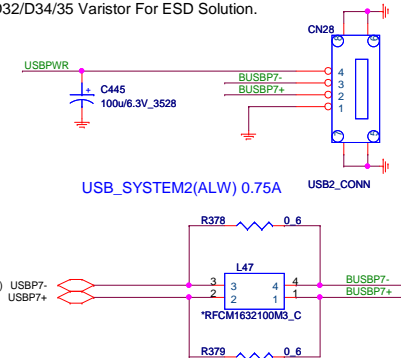
Rev:3A 02/05 Added PIN12/14 To Ground For ESD.

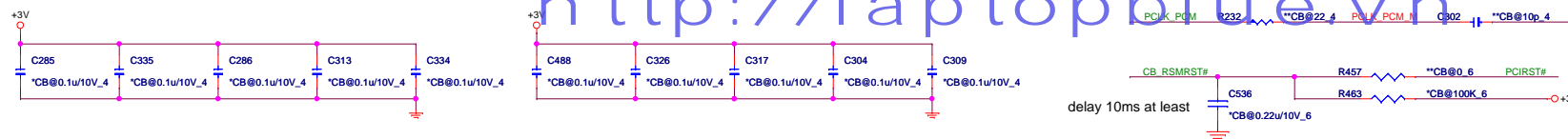


Rev:3A 01/29 Delete R133 For ESD Solution.

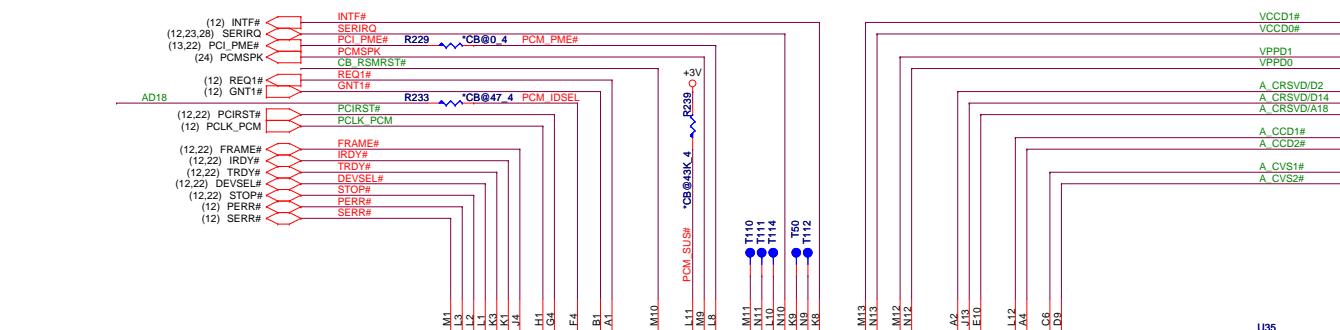


Rev:3A 03/03 Stuff the D4/D5/D32/D34/35 Varistor For ESD Solution.



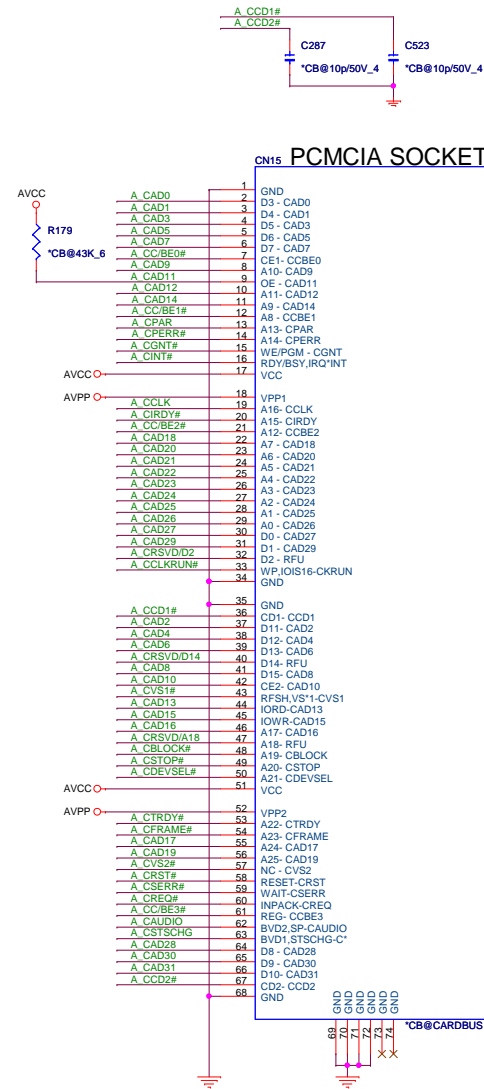
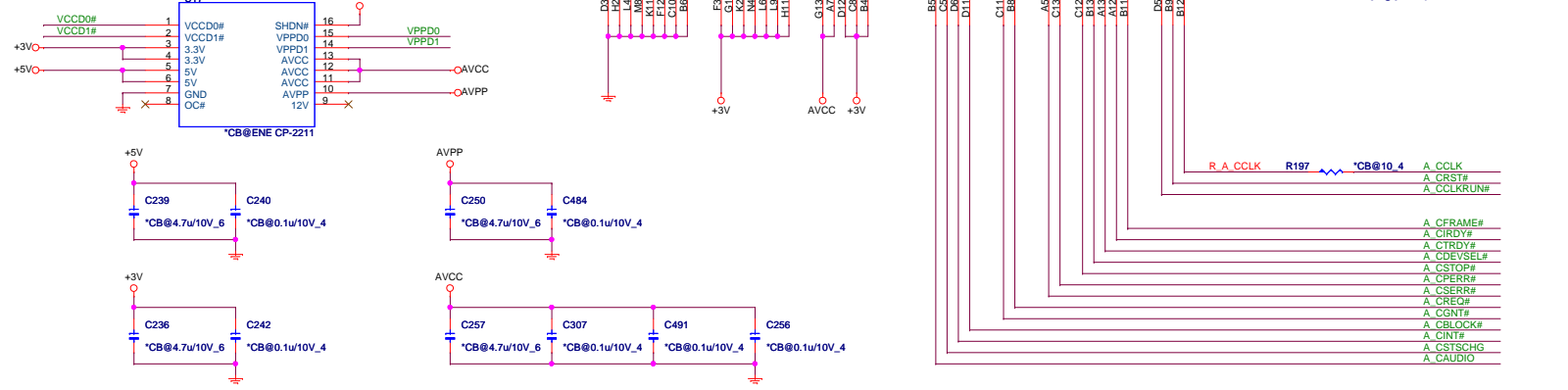
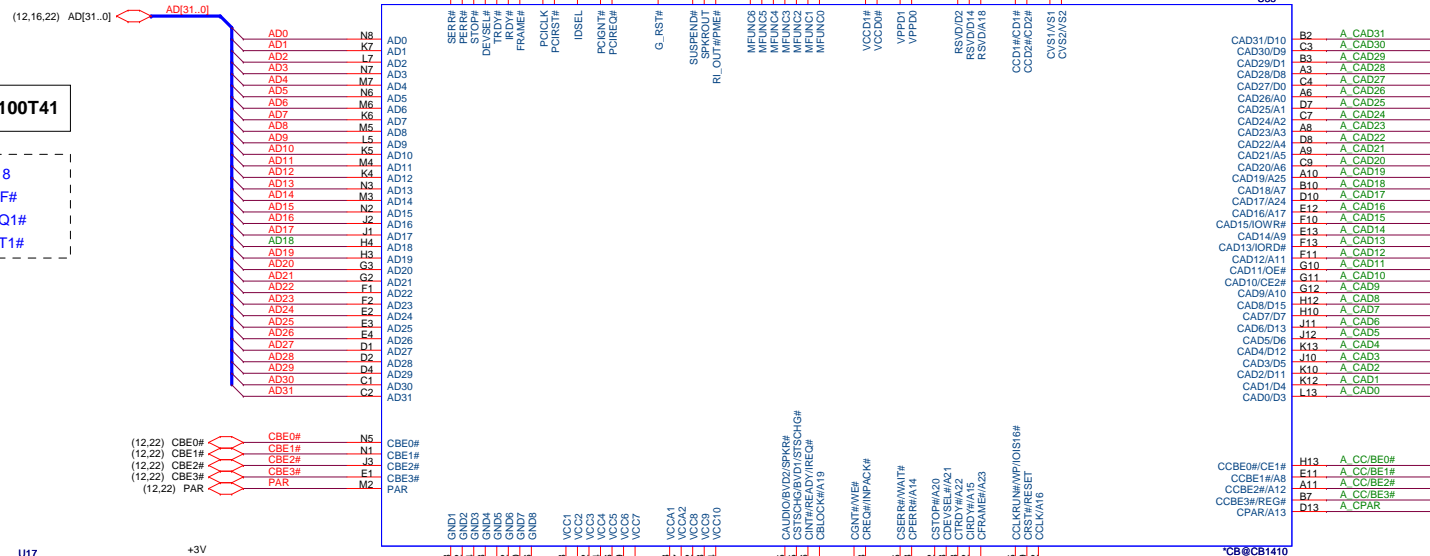


delay 10ms at least



ENE1410 AJ014100T41

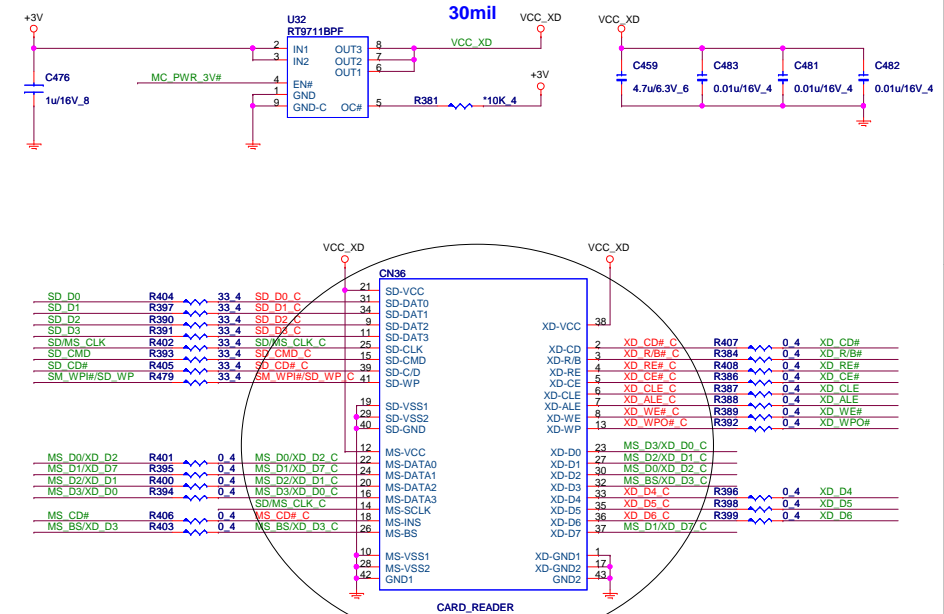
ID Select : AD18
Interrupt Pin : INTF#
Request Indicate : REQ1#
Grant Indicate : GNT1#



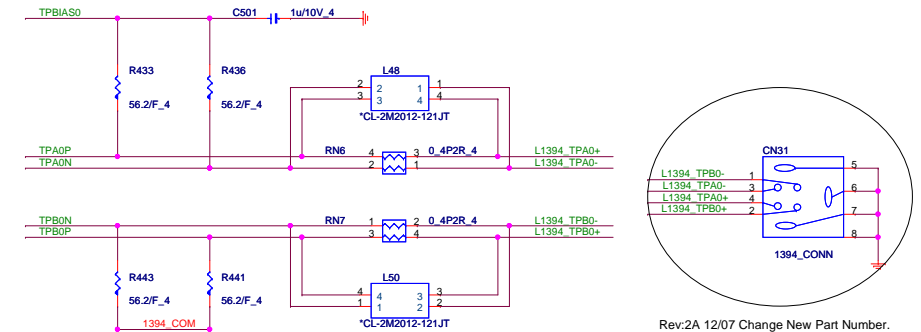
CARDBUS

http://laptopblue.com

ID Select : AD17
Interrupt Pin : INTE#
Request Indicate : REQ0#
Grant Indicate : GNT0#



1394



Rev:2A 12/07 Change New Part Number.

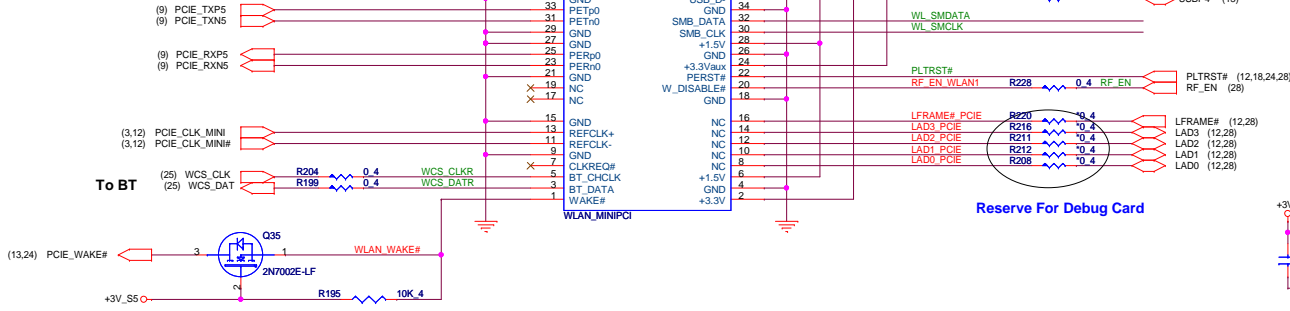


Size Custom	Document Number OZ129T(5IN1/1394)	Rev 1A
Date: Thursday, July 24, 2008		Sheet 22 of 35

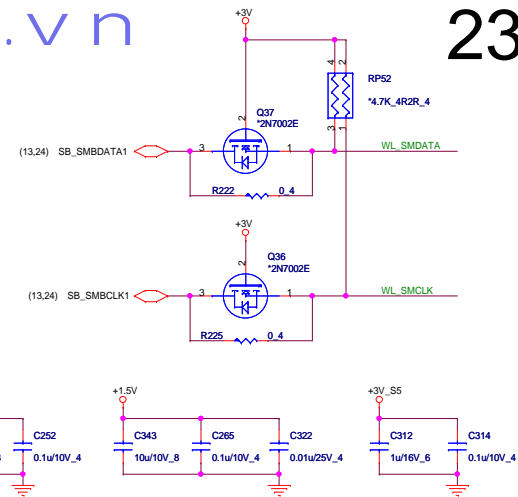
MINI CARD 1 5.6H_WLAN

Reserve For Debug Card

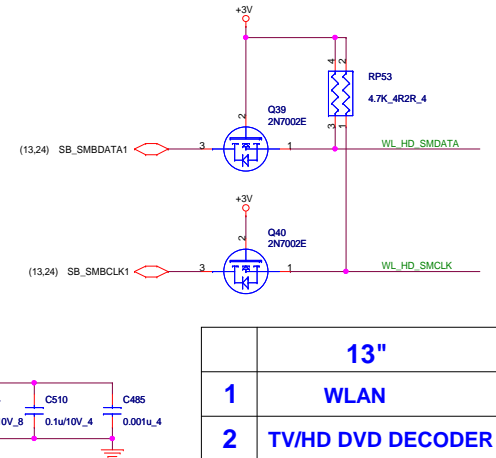
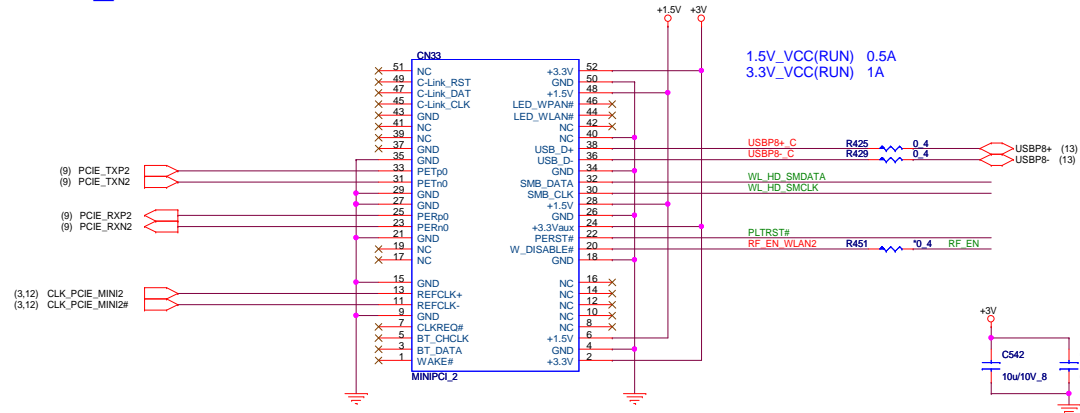
Rev:3A 03/03 Reserve the 39/41Pin to +3.3Vaux For Support WiMax.



Reserve For Debug Card

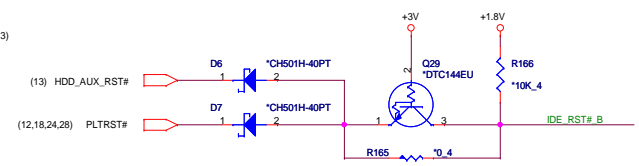
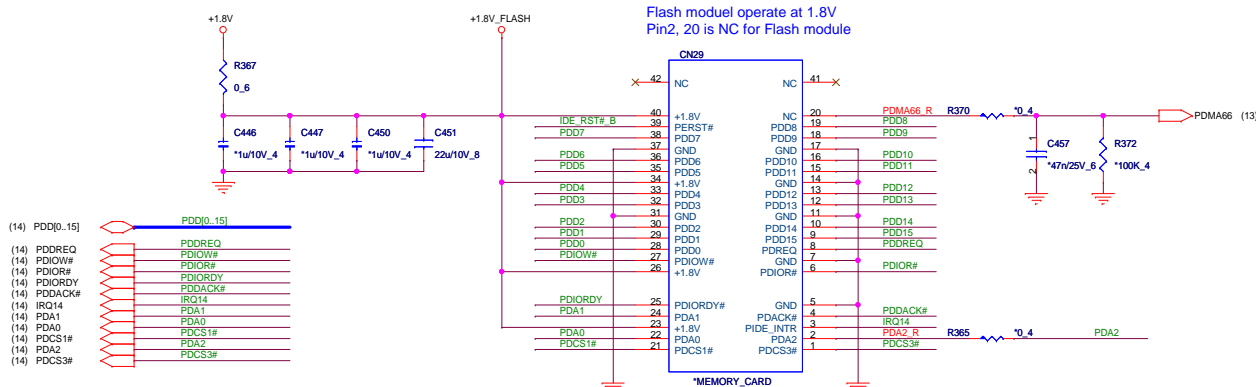


MINI Card 2 5.6H_TV/HD DVD DECODER



	13"
1	WLAN
2	TV/HD DVD DECODER

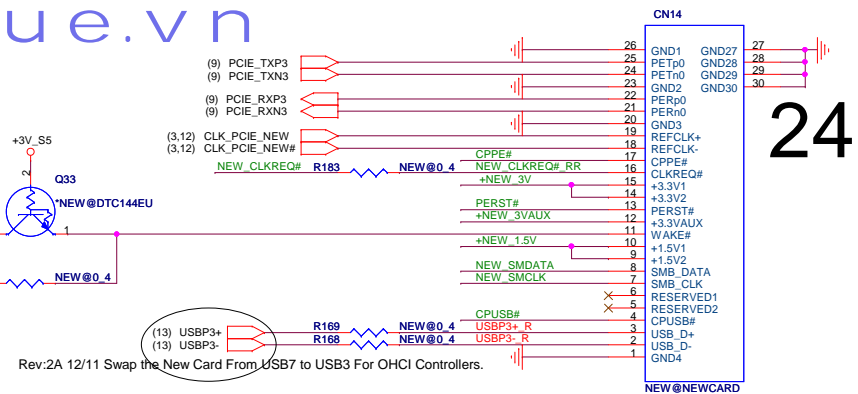
NAND FLASH MEMORY CARD



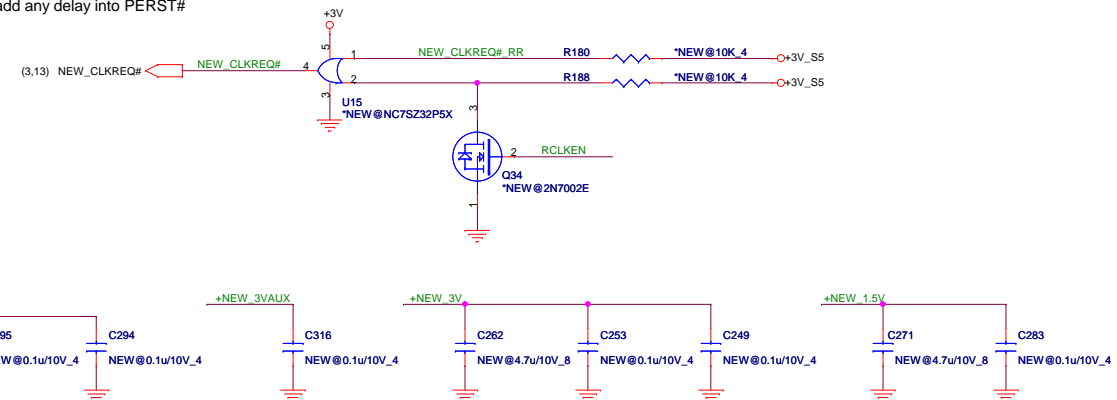
PROJECT : BU2
Quanta Computer Inc.

Size Custom	Document Number MINI CARD & NAND FLASH CARD	Rev 1A
Date: Thursday, July 24, 2008	Sheet 23 of 35	

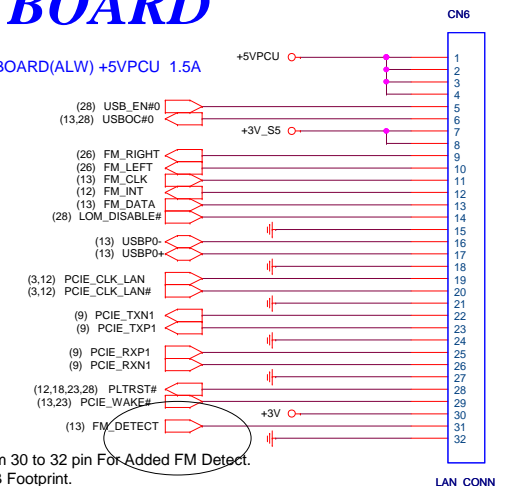
<http://laptopblue.vn>



Rev:3A 03/03 As check with AE regarding to PERST# do not add any delay into PERST#



RJ45/USB BOARD



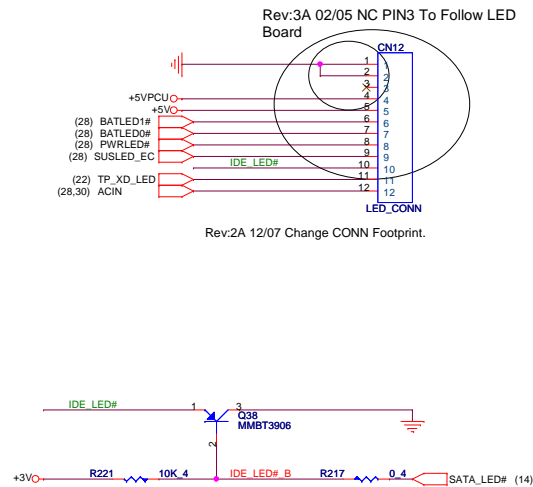
Rev:2A 12/07 Change Connector From 30 to 32 pin For Added FM Detect.
Rev:3A 02/05 Change Connector PCB Footprint.



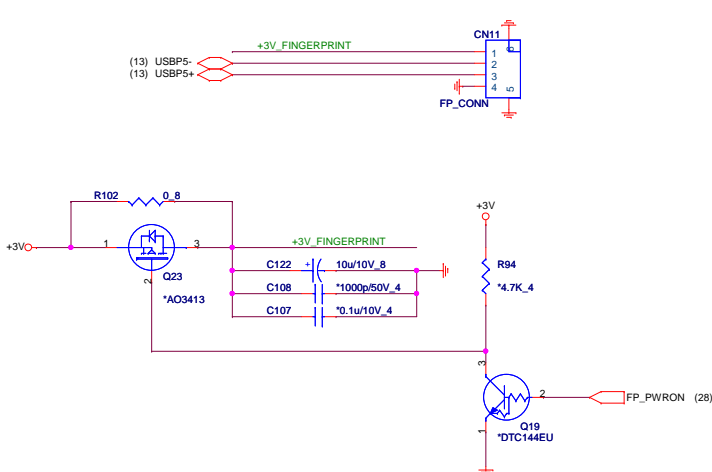
PROJECT : BU2
Quanta Computer Inc.

Size Custom	Document Number NEW CARD & RJ45 BOARD/BEEP	Rev 1A
Date: Thursday, July 24, 2008		Sheet 24 of 35

LED BOARD

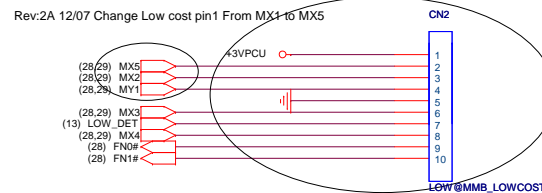


FINGER-PRINT



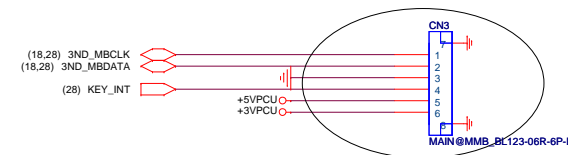
MMB

Low cost

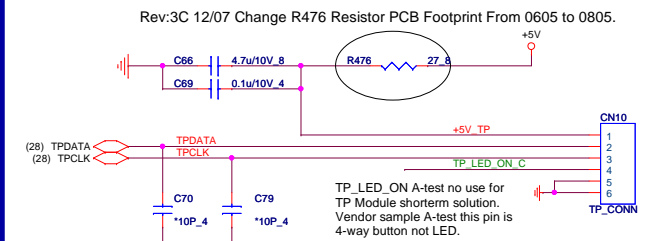


Rev:2A 12/07 Change CONN Footprint.

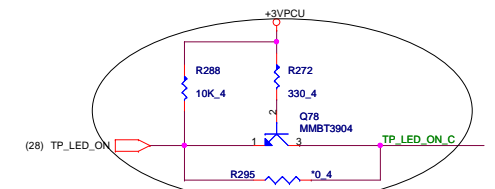
Main stream



TP BOARD

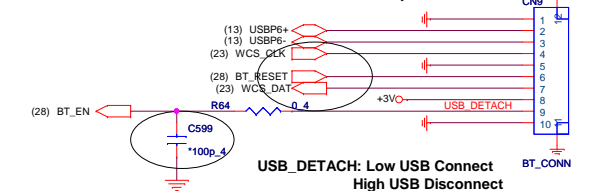


Rev:2A 12/07 Apply isolate TP_LED_ON From EC to Mainstream TP



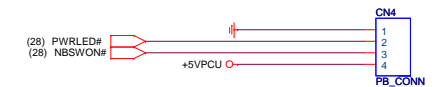
Bluetooth Module


Rev:3D 07/23 Remove R59 and Added control BT Reset by EC GPIO77

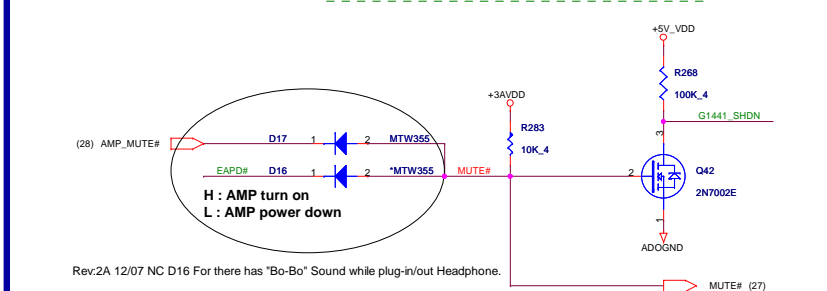
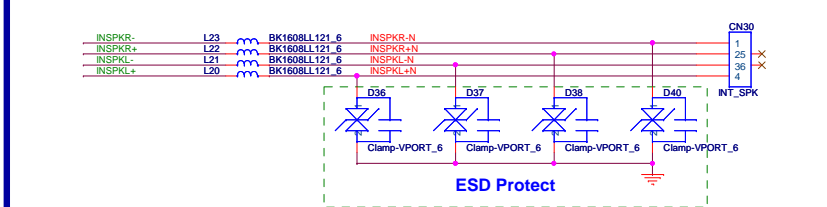
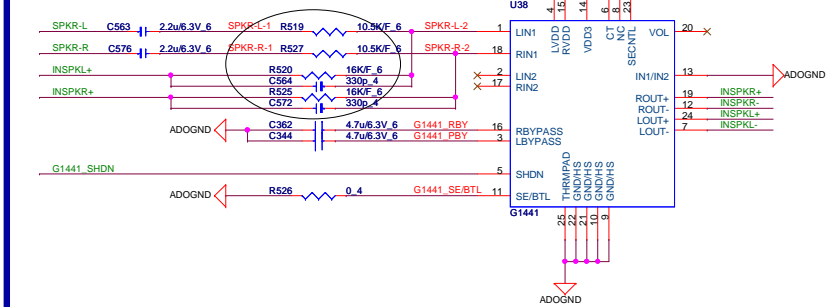
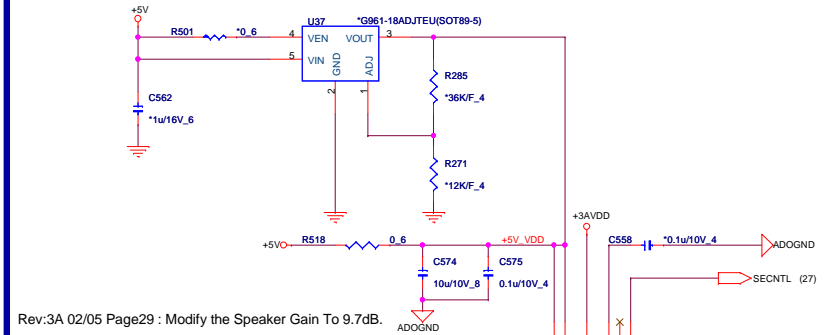
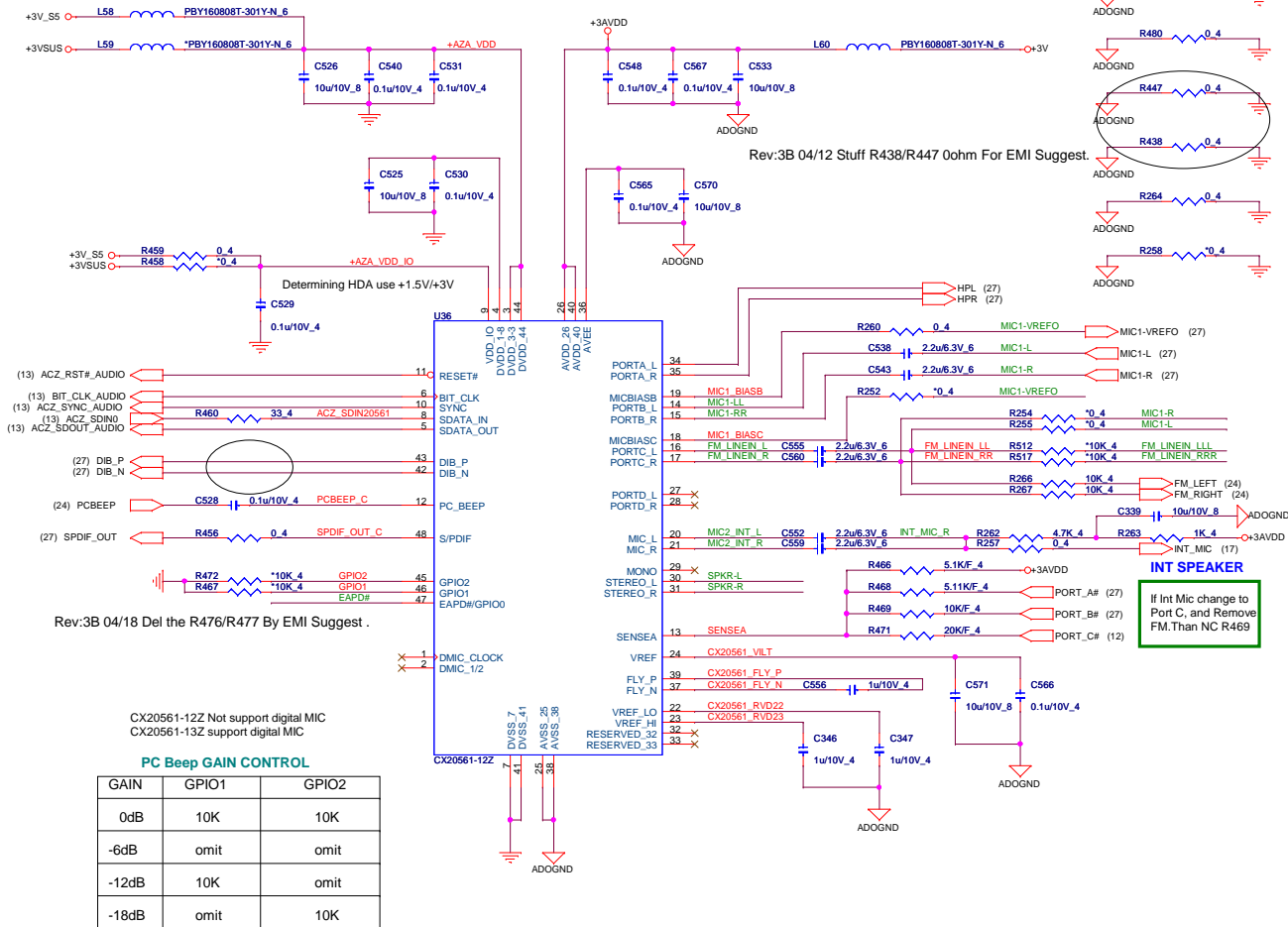


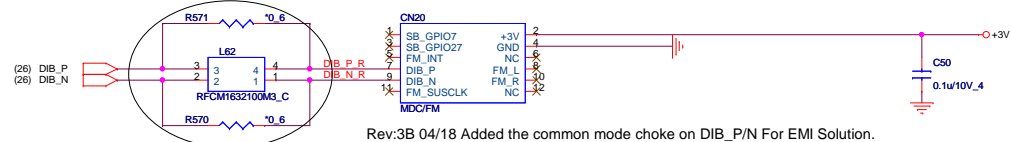
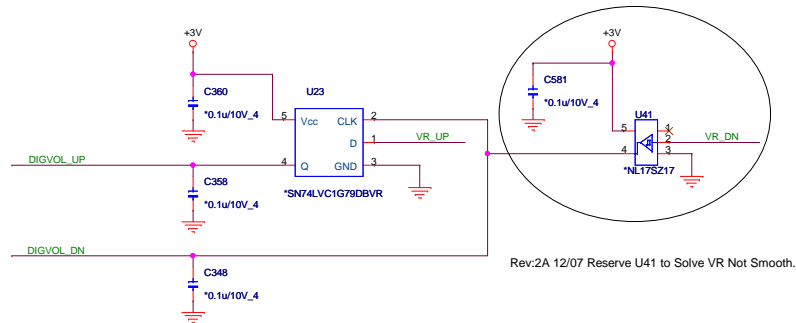
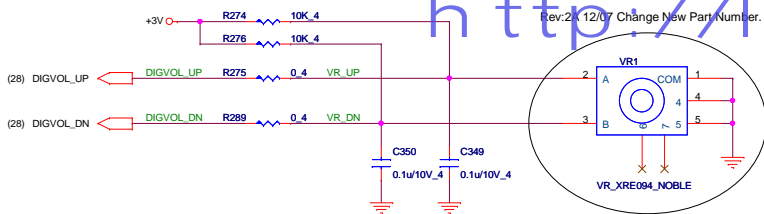
Rev:3A 03/03 Reserve C599 Capacitors to Bluetooth Enable For EMI..

POWER BOARD

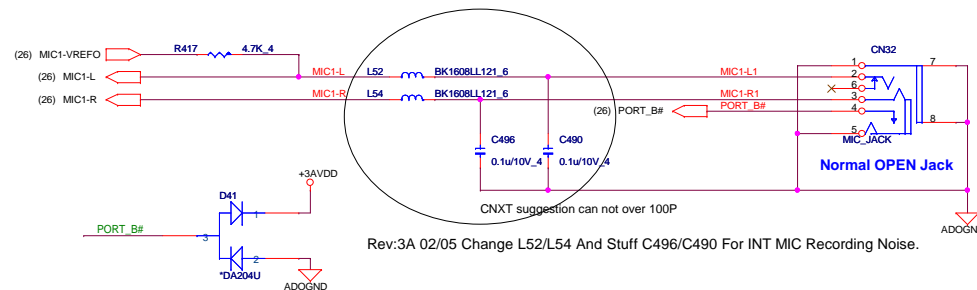


	PROJECT : BU2		
	Quanta Computer Inc.		
Size Custom	Document Number	Rev 1A	
	TP/FP/BT/PC/FELICA/MMB CONN		
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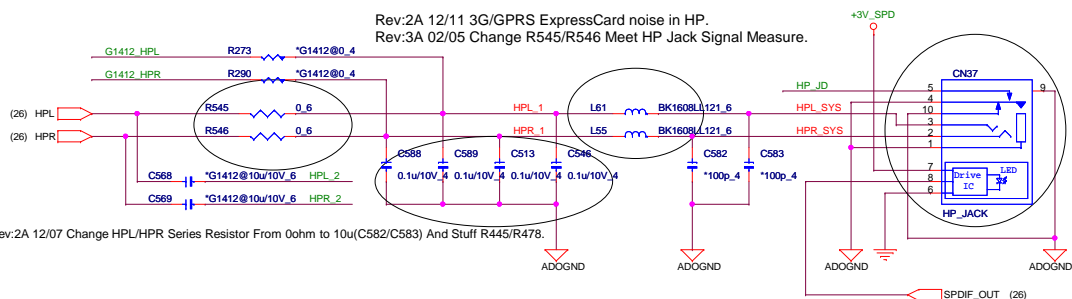


SYSTEM MIC

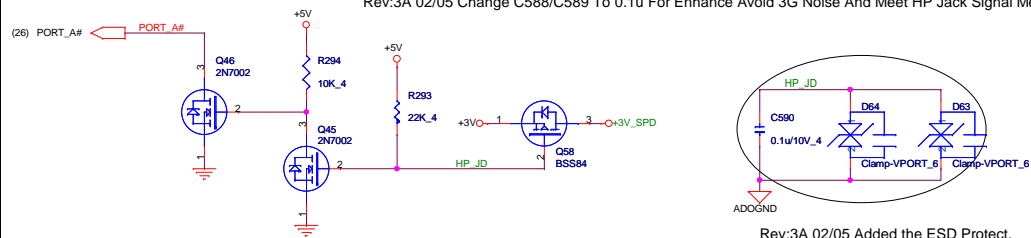


HP JACK

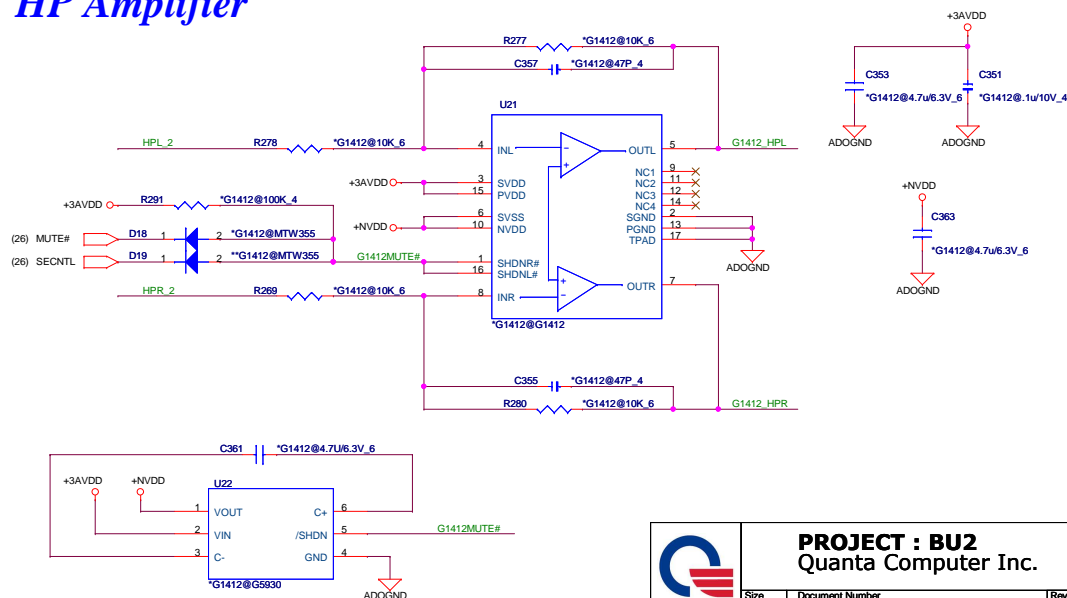
Rev:2A 12/11 3G/GPRS ExpressCard noise in HP.
Rev:3A 02/05 Change R545/R546 Meet HP Jack Signal Measure.

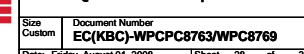


Rev:2A 12/13 CN37 9/10# Shield Pin to ADGND For ESD issue.
Rev:3A 02/05 Change C588/C589 To 0.1u For Enhance Avoid 3G Noise And Meet HP Jack Signal Measure



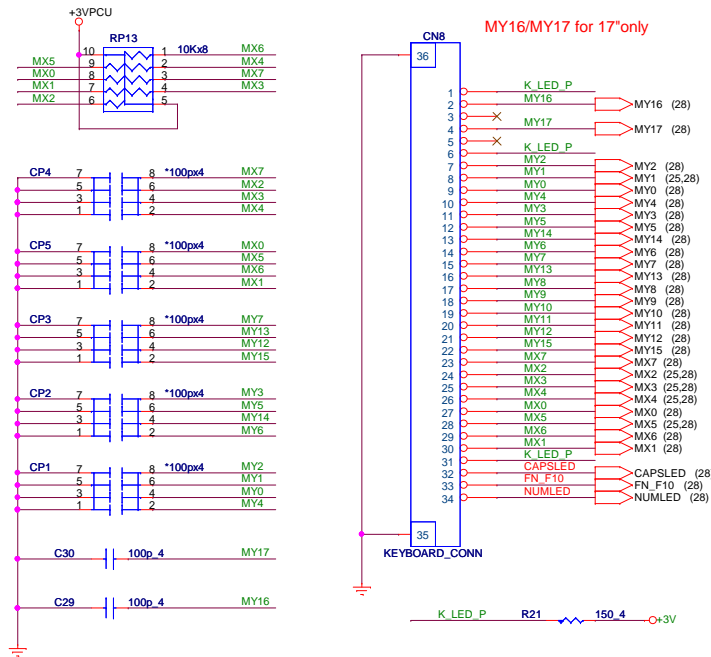
HP Amplifier



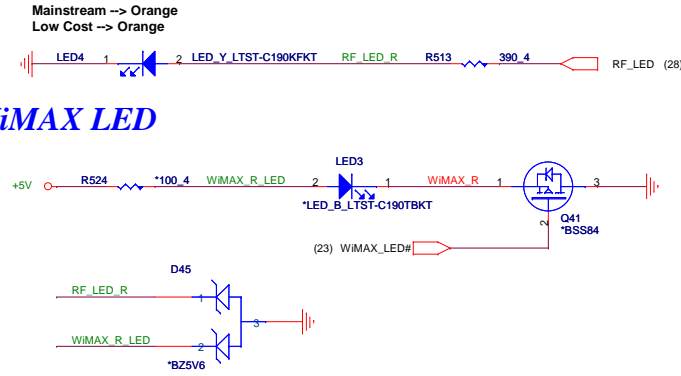


Rev:3D 07/23 Add D68 to Avoid +3V Voltage Leakage

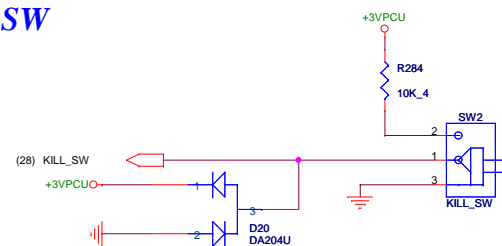
INT KEYBOARD



WiMAX LED

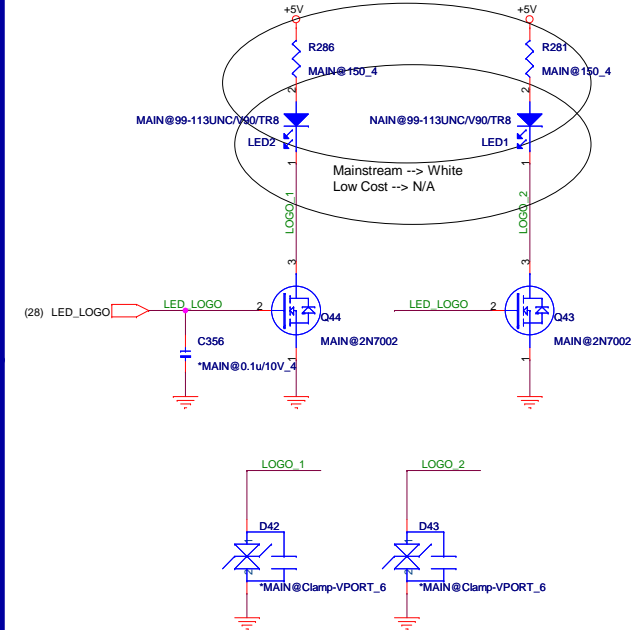


KILL SW



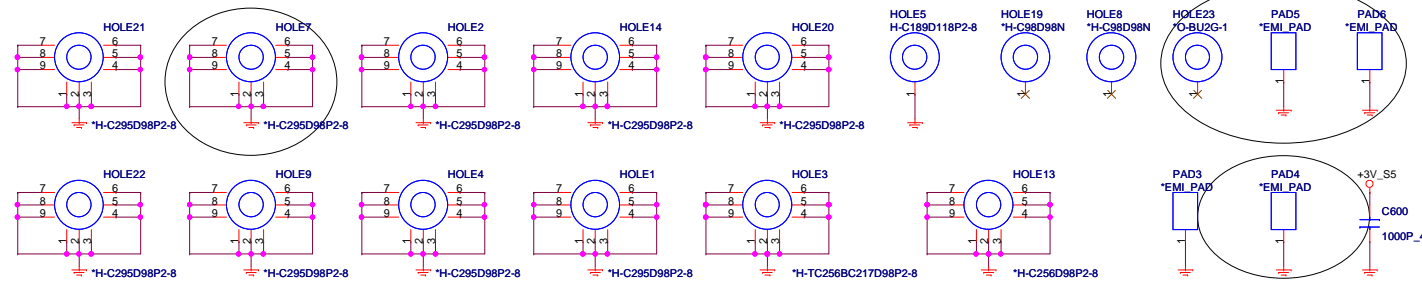
Satellite LED

Rev:2A 12/07 Updated the LED1/LED2 Footprint And Part Number.
Rev:3A 02/05 Change R281/R286 and R375 To 150ohm For LED Light Not Enough

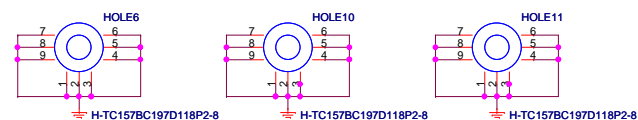


HOLE

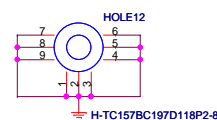
Rev:2A 12/09 Modified the Footprint.



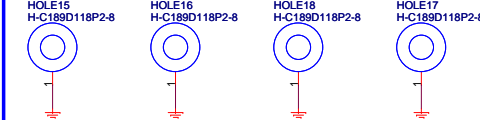
CPU



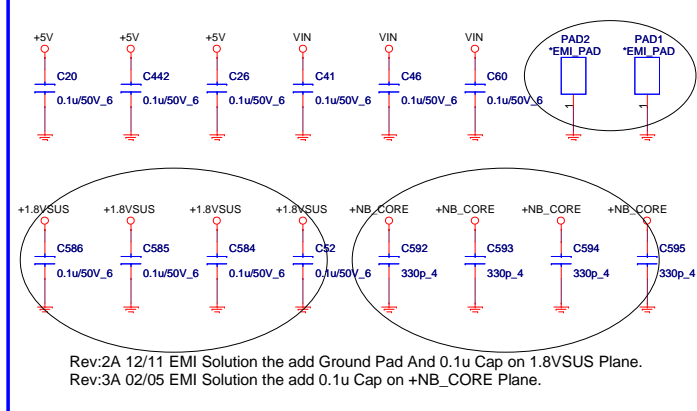
NB



MINI CARD



EMI

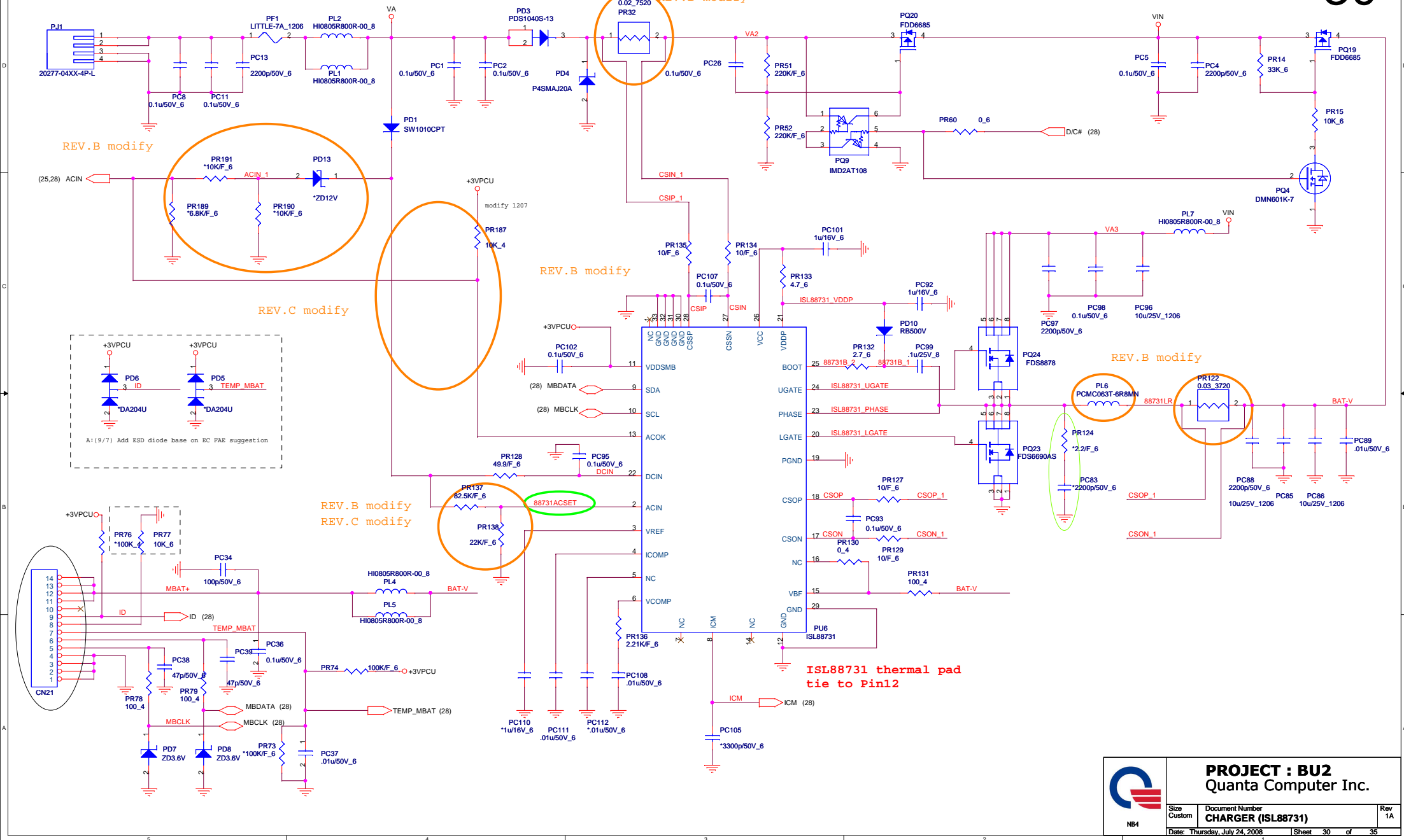


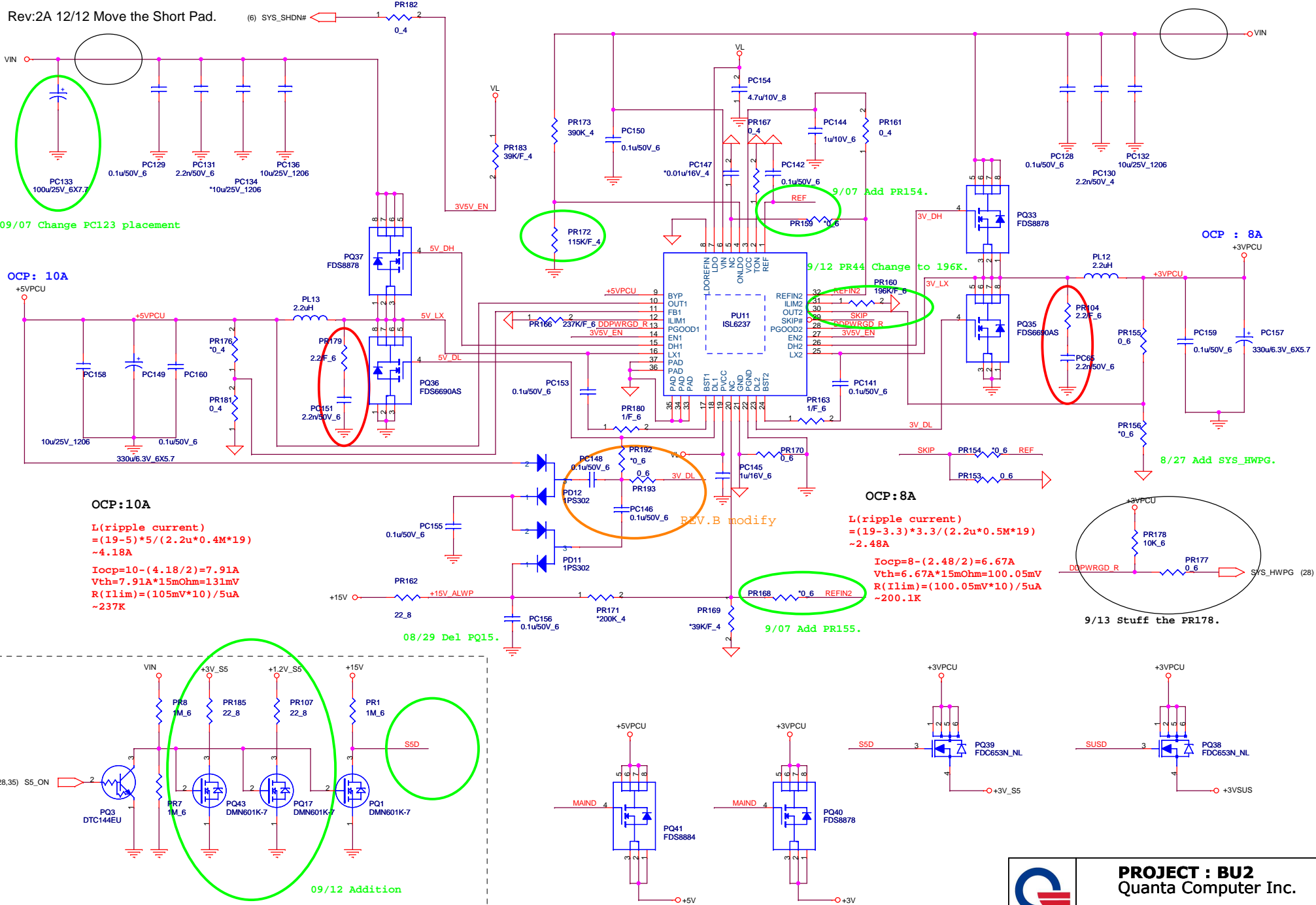
Rev:2A 12/11 EMI Solution the add Ground Pad And 0.1u Cap on 1.8VSUS Plane.
Rev:3A 02/05 EMI Solution the add 0.1u Cap on +NB_CORE Plane.

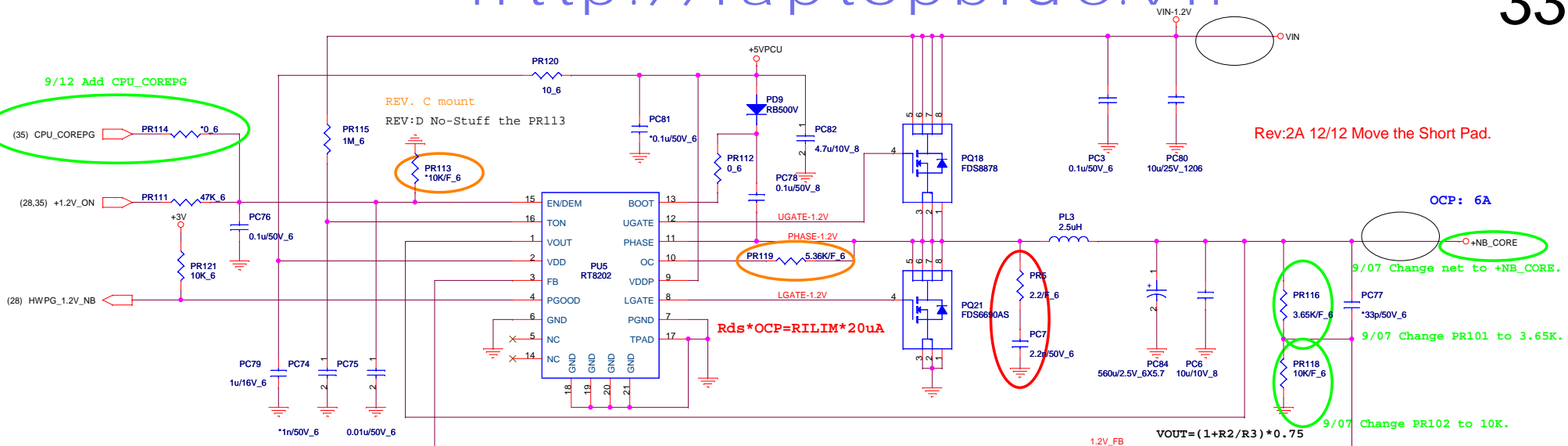


PROJECT : BU2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KEYBOARD/LED/KILL SW/HOLE	1A
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$$TON = 3.85p \cdot R_{TON} \cdot V_{out} / (V_{in} - 0.5)$$

$$Frequency = V_{out} / (V_{in} \cdot TON)$$

$$6A \text{ OCP} \text{ --- } OC = 4.53K$$

$$FDS6690AS \text{ Rds} = 15m\Omega$$

REV. C PR119 change to 5.36Kohm

1/30 modify

