

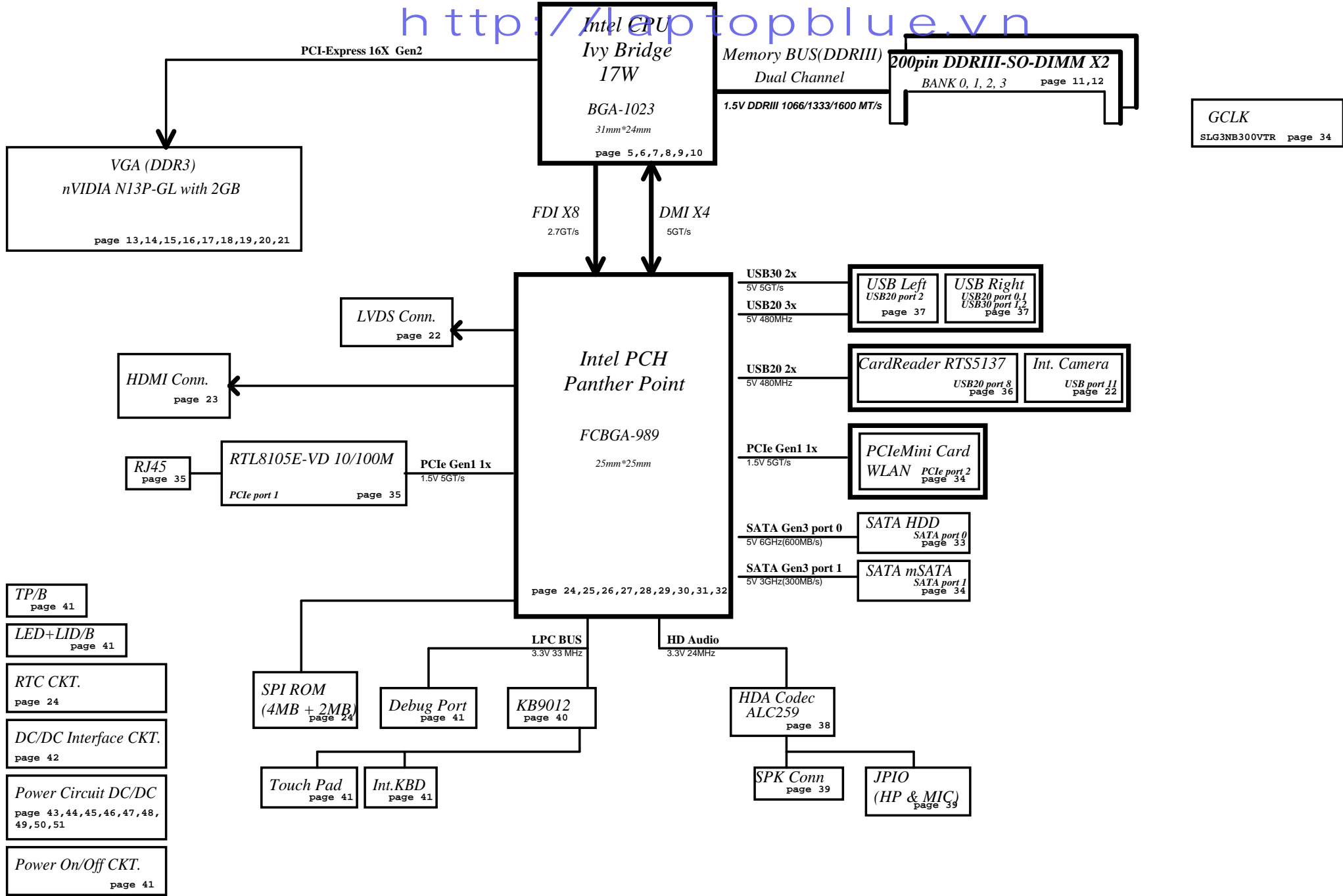
# VCUAA

## *Metis 10F/10FG*

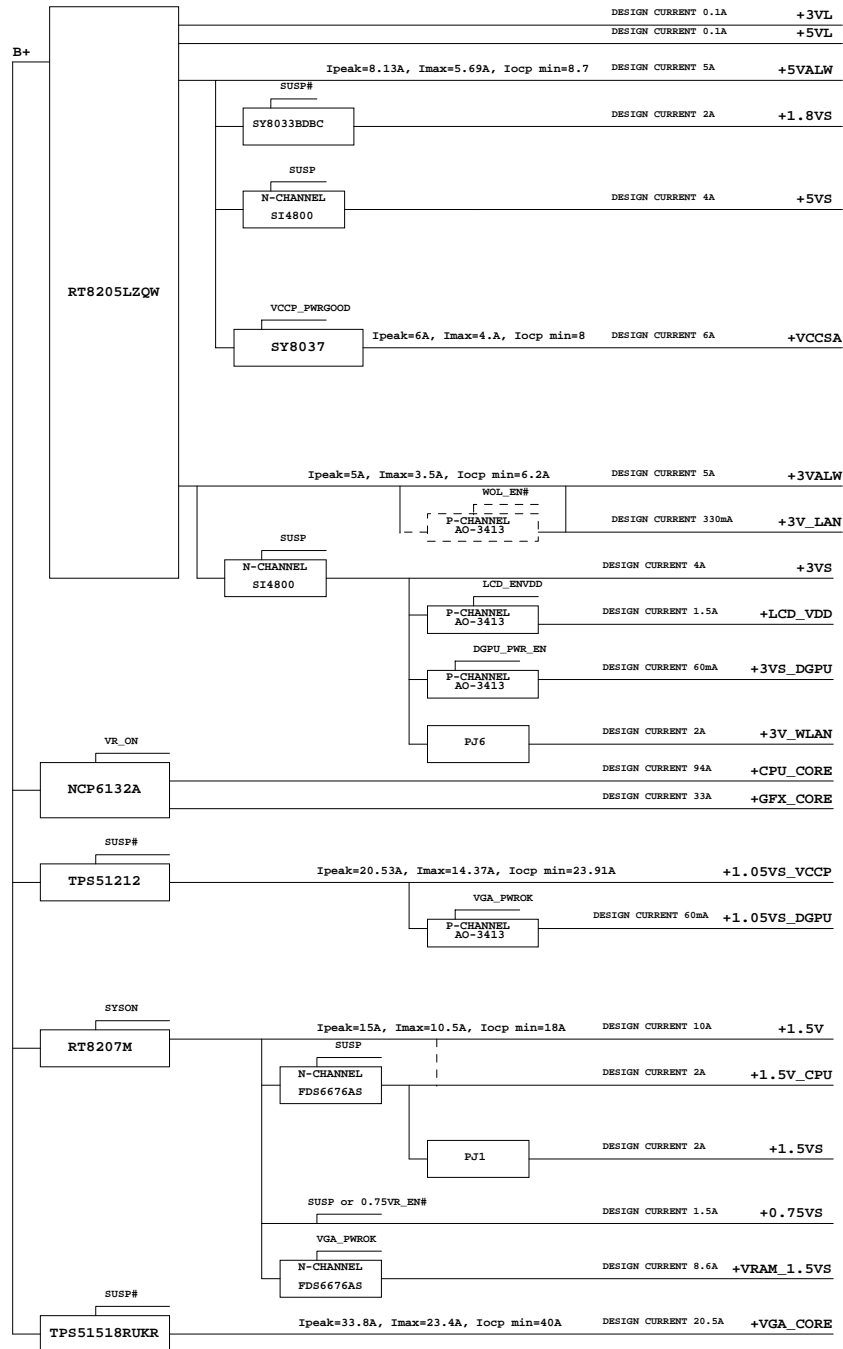
# LA-9161P REV 1.0 Schematic

Intel Processor (Ivy Bridge) / PCH(Panther Point)  
2012-08-07 Rev 1.0

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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	Cover Page
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				VCUAA	1.0
				Date: Tuesday, October 16, 2012	Sheet 1 of 53



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				Date:	Tuesday, October 16, 2012
				Sheet	2 of 53
				Rev	1.0



Voltage Rails						
( O MEANS ON X MEANS OFF )						
power plane	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
State						
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address			
Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b

EC SM Bus1 Address				EC SM Bus2 Address			
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b	+3VS	NVIDIA GPU	9E H	1001 1010 b
Power	Device	HEX	Address				

Platform	SKU	CPU	PCH	VGA
Chief River		Ivy Bridge i3 (CPUI3@) Ivy Bridge i5 (CPUI5@)	HM77C1 (HM77@) HM77C1_R1 (HM77R1@) HM77C1_R3 (HM77R3@)	nVIDIA N13P-GL (N13PGL@)

BTO Option Table

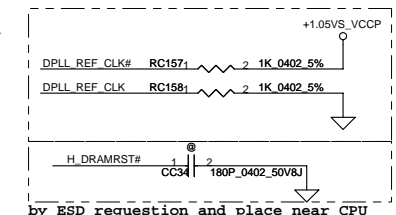
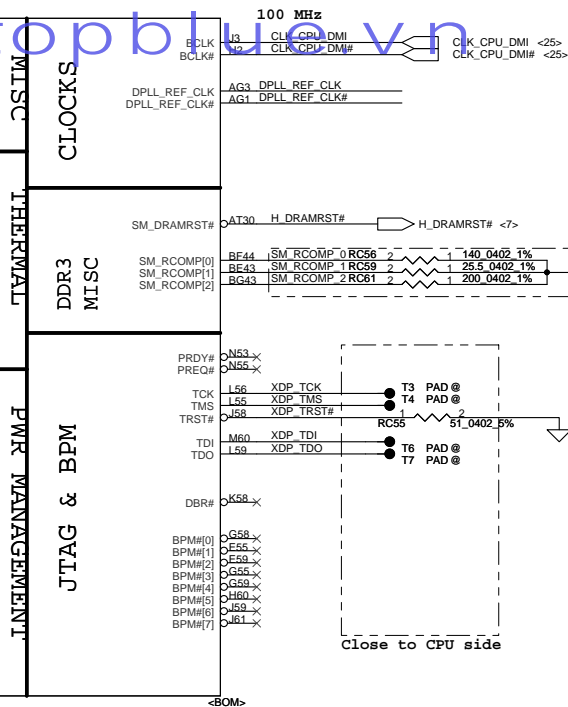
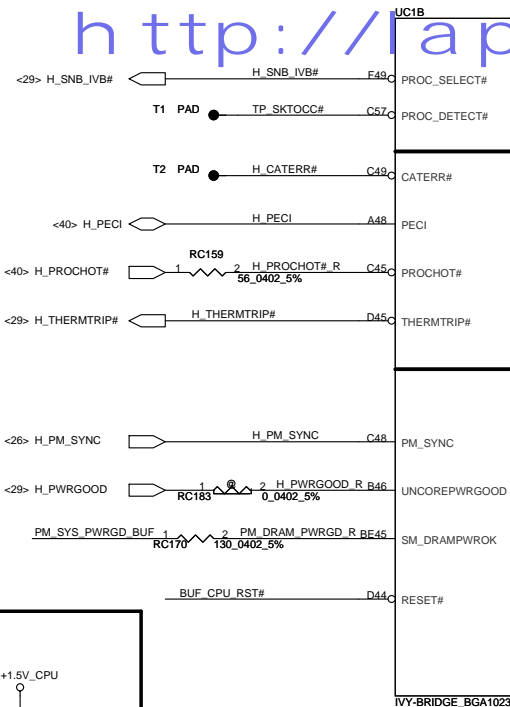
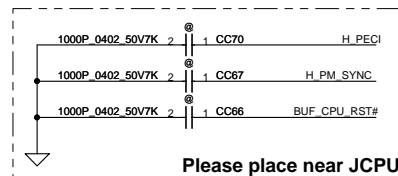
Function	SKU	MIC	LAN			
description						
explain						
BTO						

Function						
description						
explain						
BTO						

Function						
description						
explain						
BTO						

Function		
description		
explain		
BTO		

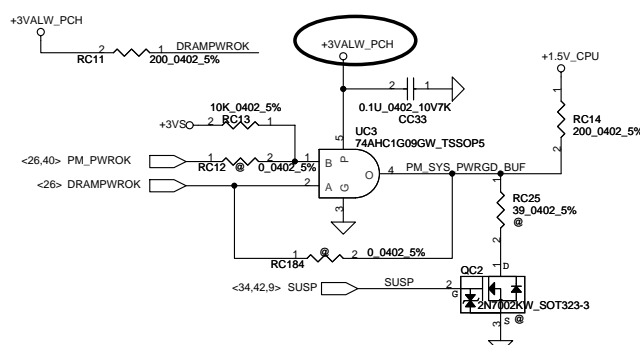
STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW



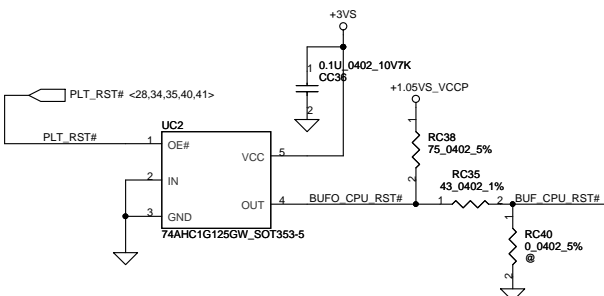
by ESD requestion and  
DDR3 Compensation Signals  
Layout Note: Place these  
resistors near Processor

| Routed as a single daisy chain

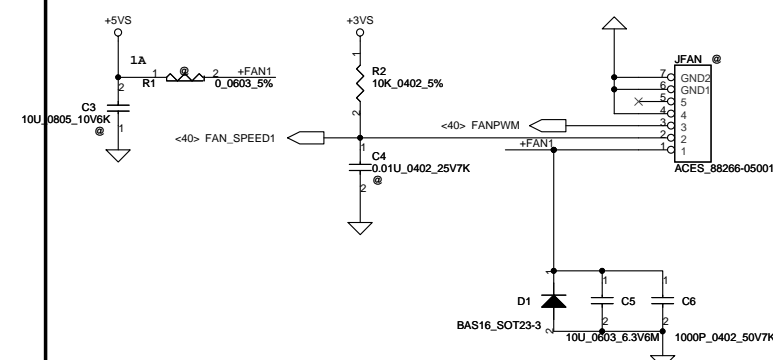
Close to CPU side



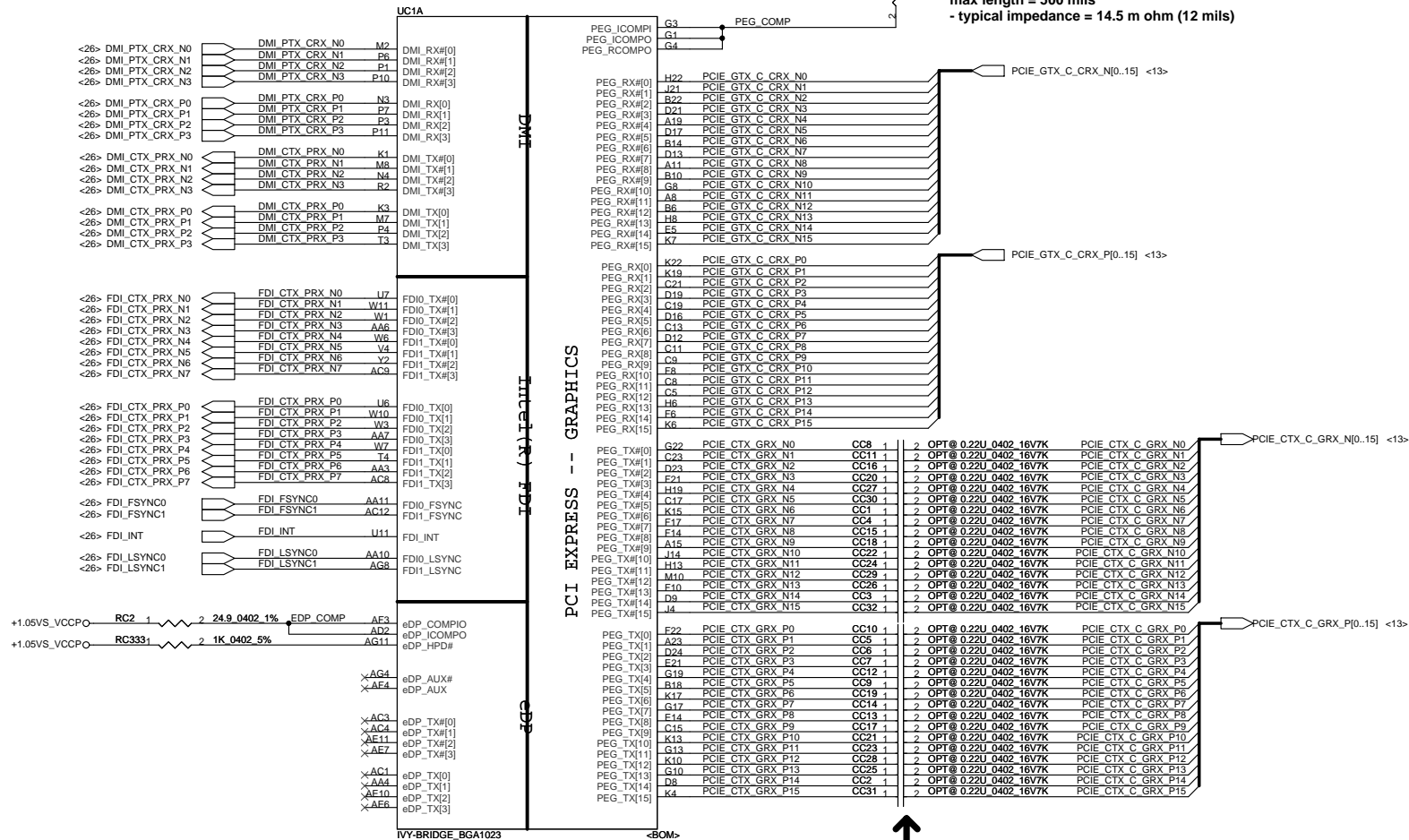
### Buffered Rest to CPU



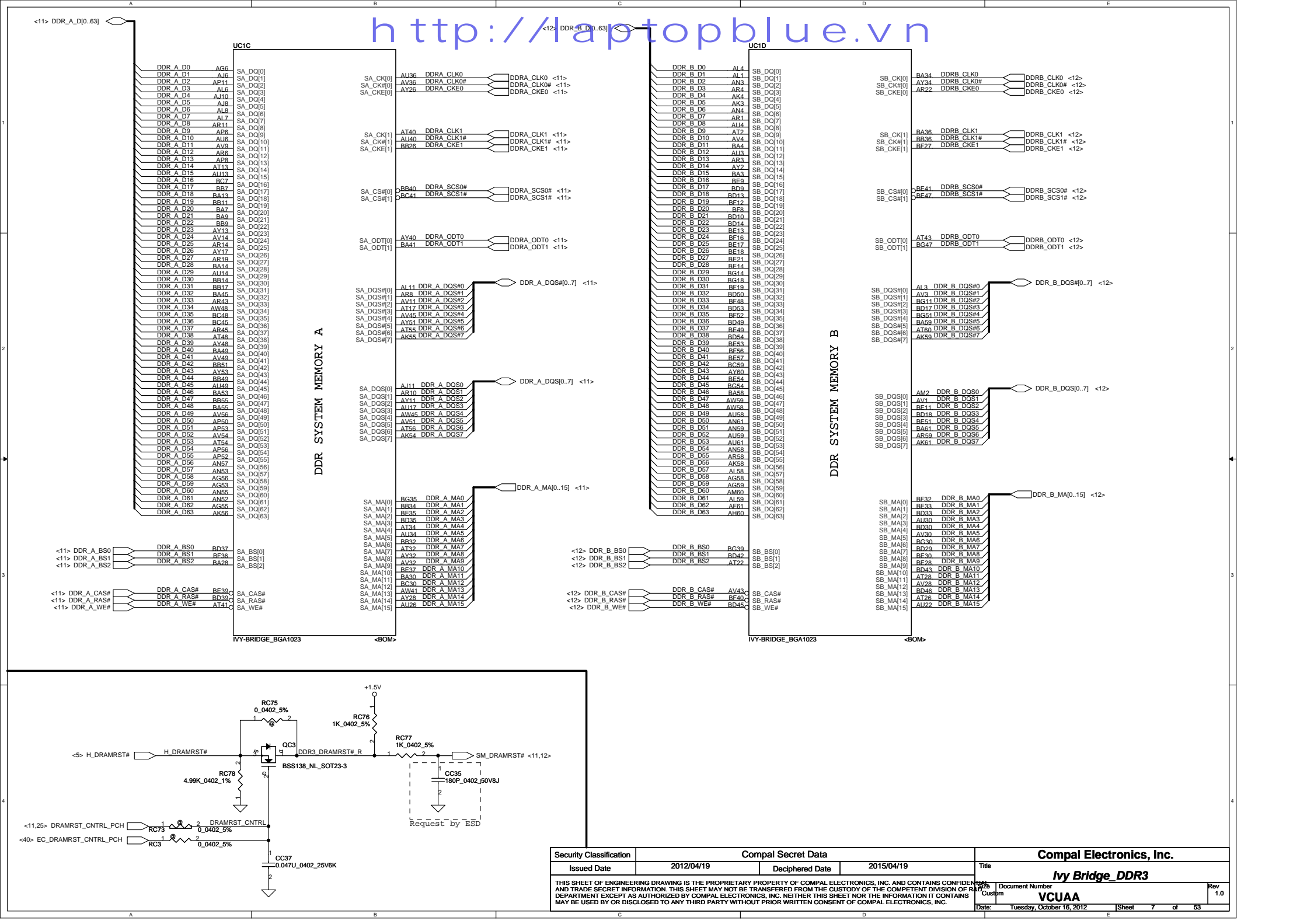
## XDP Connector



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				Document Number	
				VCUAA	
Date:				Tuesday, October 16, 2012	Sheet 5 of 53



	PEG	DG suggest AC cap
IVY Bridge	Gen1/Gen2	75 nF~265 nF
	Gen3	180 nF~265 nF
SANDY Bridge	Gen1/Gen2	180 nF~265 nF
NV N13X	Gen1/2/3	Suggest 220 nF



# POWER

8.5A

+CPU CORE

UC1F  
33A

+1.05V\_VCCP

- A26 VCC[1]
- A31 VCC[2]
- A34 VCC[3]
- A35 VCC[4]
- A38 VCC[5]
- A39 VCC[6]
- A42 VCC[7]
- C26 VCC[8]
- C27 VCC[9]
- C32 VCC[10]
- C34 VCC[11]
- C37 VCC[12]
- C39 VCC[13]
- C42 VCC[14]
- D27 VCC[15]
- D32 VCC[16]
- D34 VCC[17]
- D39 VCC[18]
- D42 VCC[19]
- E26 VCC[20]
- E28 VCC[21]
- F32 VCC[22]
- F34 VCC[23]
- F37 VCC[24]
- F38 VCC[25]
- F25 VCC[26]
- F26 VCC[27]
- F28 VCC[28]
- F34 VCC[29]
- F37 VCC[30]
- F38 VCC[31]
- G42 VCC[32]
- H25 VCC[33]
- H26 VCC[34]
- H28 VCC[35]
- H29 VCC[36]
- H32 VCC[37]
- H34 VCC[38]
- H35 VCC[39]
- H37 VCC[40]
- H38 VCC[41]
- H40 VCC[42]
- J25 VCC[43]
- J26 VCC[44]
- J28 VCC[45]
- J29 VCC[46]
- J32 VCC[47]
- J34 VCC[48]
- J35 VCC[49]
- J37 VCC[50]
- J38 VCC[51]
- J40 VCC[52]
- J42 VCC[53]
- K26 VCC[54]
- K27 VCC[55]
- K29 VCC[56]
- K32 VCC[57]
- K34 VCC[58]
- K35 VCC[59]
- K37 VCC[60]
- K39 VCC[61]
- K42 VCC[62]
- L25 VCC[63]
- L28 VCC[64]
- L33 VCC[65]
- L36 VCC[66]
- L40 VCC[67]
- N26 VCC[68]
- N30 VCC[69]
- N34 VCC[70]
- N38 VCC[71]

CORE SUPPLY

PEG IO AND DDR IO

- AF46 VCCIO[1]
- AG48 VCCIO[3]
- AG50 VCCIO[4]
- AG51 VCCIO[5]
- AJ17 VCCIO[6]
- AJ21 VCCIO[7]
- AJ25 VCCIO[8]
- AJ43 VCCIO[9]
- AJ47 VCCIO[10]
- AK50 VCCIO[11]
- AK51 VCCIO[12]
- AL14 VCCIO[13]
- AL15 VCCIO[14]
- AL16 VCCIO[15]
- AL20 VCCIO[16]
- AL22 VCCIO[17]
- AL26 VCCIO[18]
- AL45 VCCIO[19]
- AL48 VCCIO[20]
- AM16 VCCIO[21]
- AM17 VCCIO[22]
- AM21 VCCIO[23]
- AM43 VCCIO[24]
- AM47 VCCIO[25]
- AN20 VCCIO[26]
- AN42 VCCIO[27]
- AN45 VCCIO[28]
- AN48 VCCIO[29]

For DDR

For PEG

1mA

VCCIO\_SEL

QUIET RAILS

SVID

SENSE LINES

IVY-BRIDGE\_BGA1023

+1.05V\_VCCP

VCCIO50

VCCIO51

RC22

+1.05V\_VCCP

VCCPQE[1]

VCCPQE[2]

CC71

1U\_0402\_6.3V6K

RC91

130\_0402\_5%

RC89

75\_0402\_5%

RC90

43\_0402\_1%

RC88

2\_0402\_5%

RC92

0\_0402\_5%

RC93

100\_0402\_1%

RC94

0\_0402\_5%

RC95

0\_0402\_5%

RC96

10\_0402\_1%

RC97

100\_0402\_1%

RC98

10\_0402\_1%

RC99

10\_0402\_1%

RC100

10\_0402\_1%

RC101

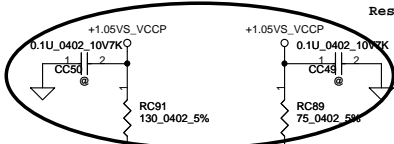
10\_0402\_1%

RC102

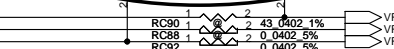
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RC103

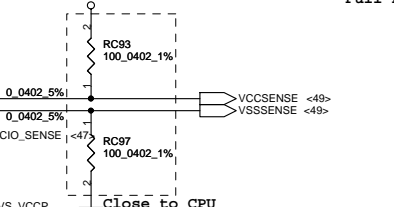
10\_0402\_1%



Reserve 0.1u to avoid noise



Pull high resistor on VR side



Close to CPU

Close to CPU

Close to CPU

Close to CPU

Close to CPU

Close to CPU

Close to CPU

Close to CPU

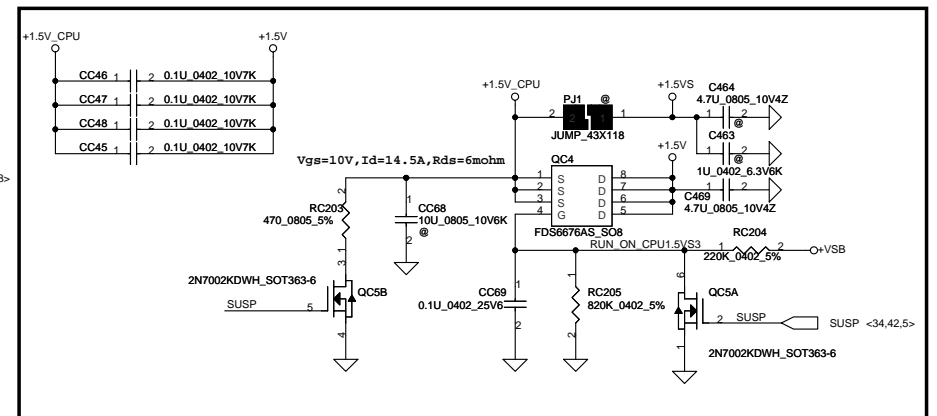
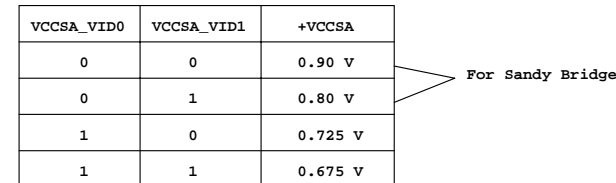
Close to CPU

Close to CPU

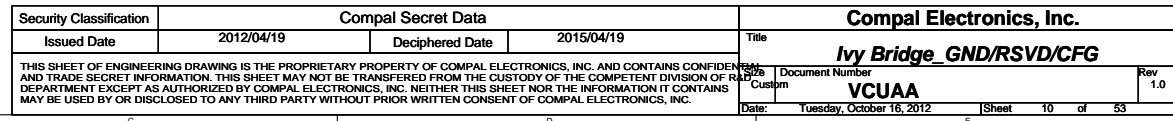
Close to CPU

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Document Number				VCUAA				Rev			
Date				Tuesday, October 16, 2012				Sheet 8 of 53			

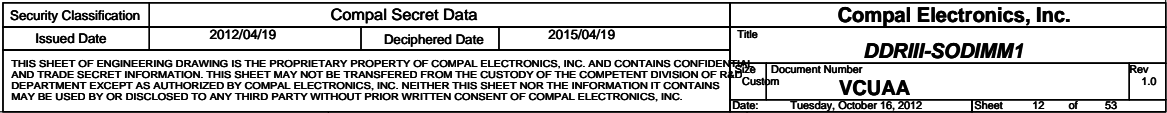


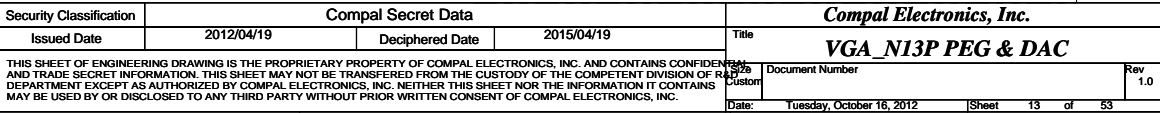


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				Custlsm	1.0	
				VCUAA		
Date:	Tuesday, October 16, 2012	Sheet	9	of	53	



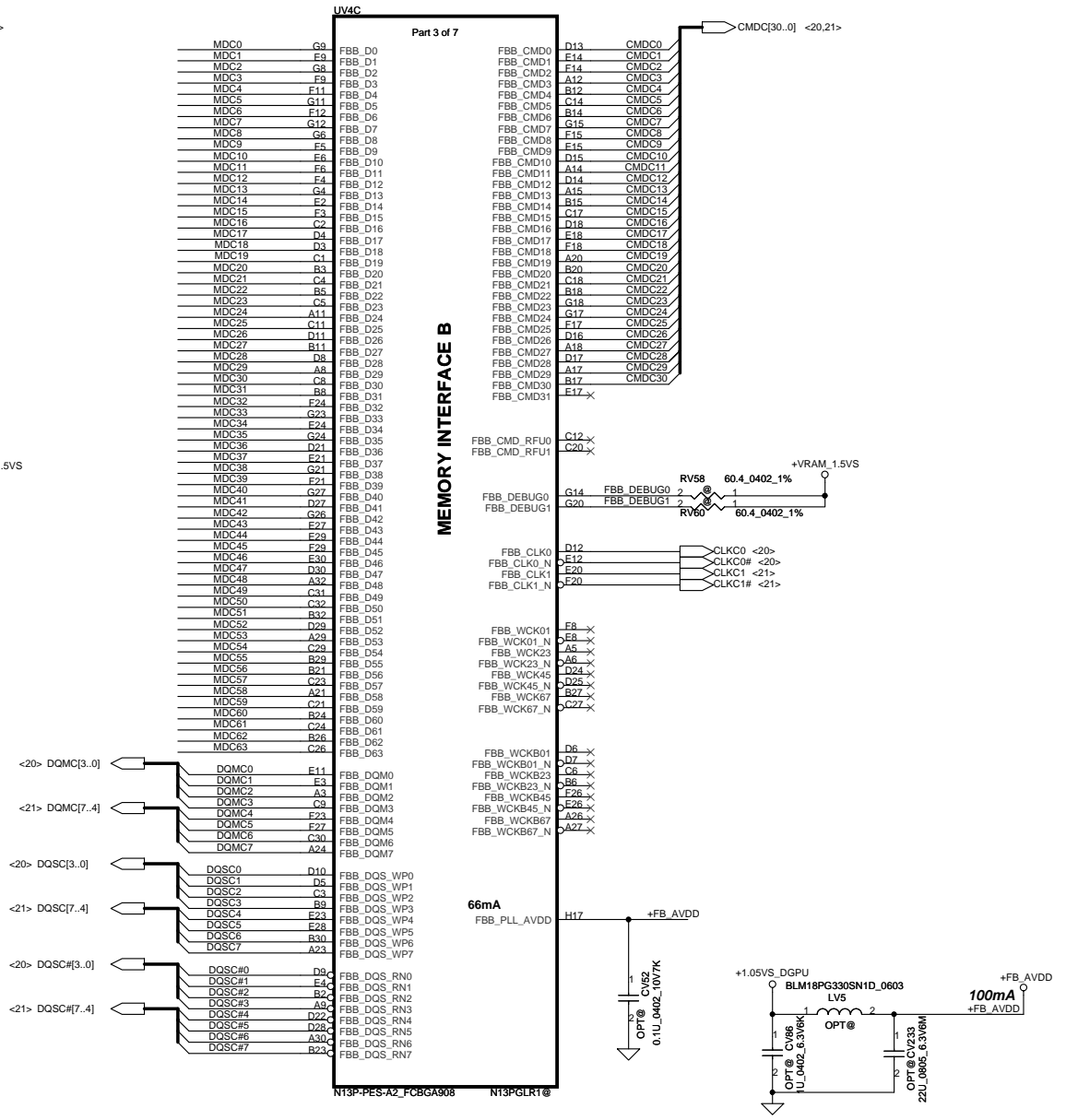
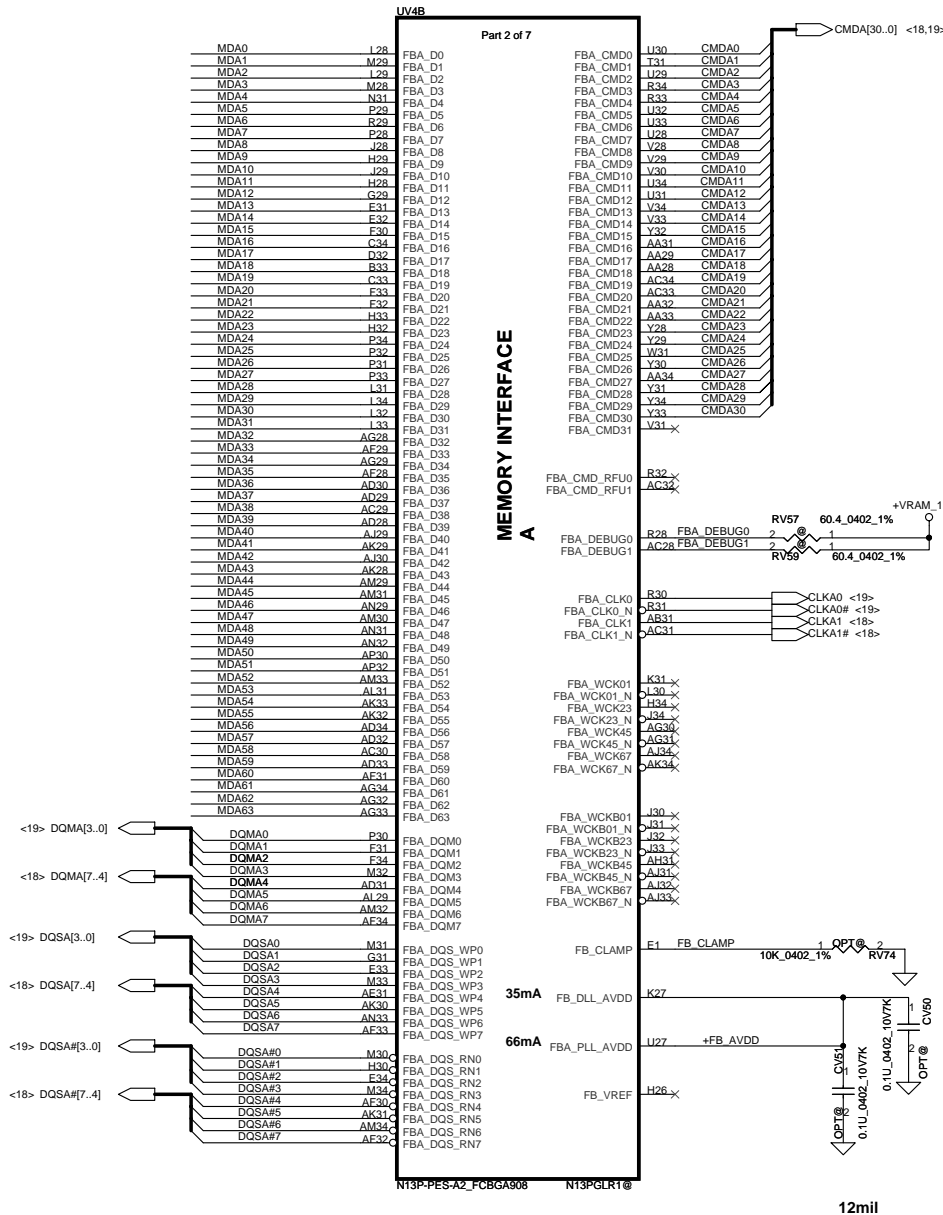
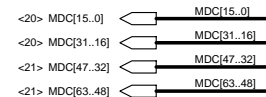
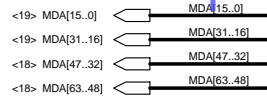








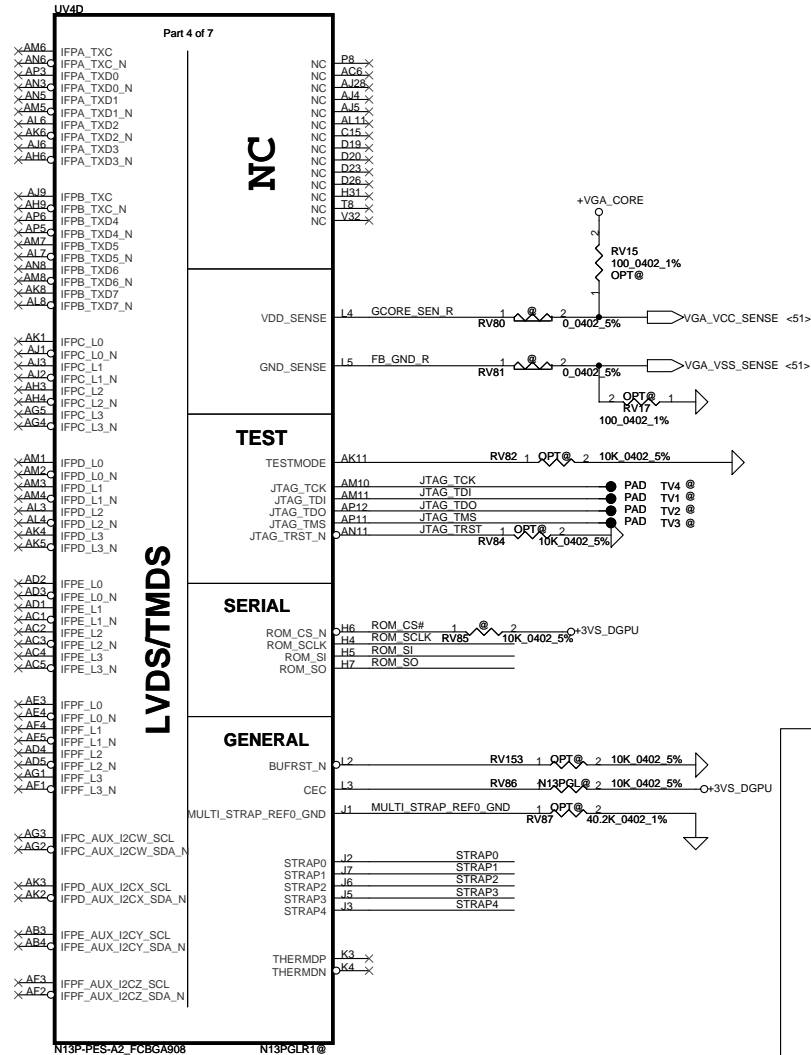
# VRAM Interface



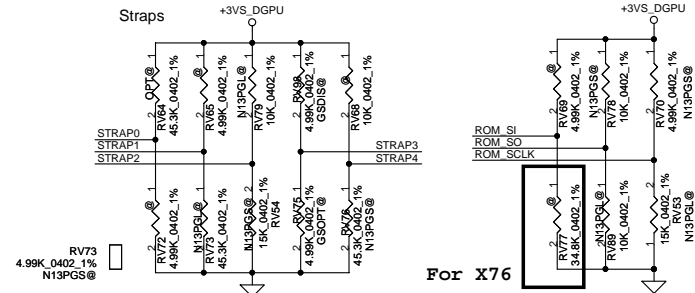
Physical Strapping Pin	Power Pin	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417 for GL, FB[1]	FB_0_BAR_SIZE for GL, FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG for GL, PCI_DEVID[5]	PEX_PLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_DGPU	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_DGPU	RESERVED	PCIE_SPEED_CHANGE_GEN	PCIE_MAX_SPEED	DP_PLL_VDD33V

SKU	Device ID	bit5 to bit0
N13P-GL ES2	0x0DE9	101001
N13P-GS ES1	0x0FDB	011011
N13P-GS QS	0x0FD2	010010

Resistor Values	Pull-up to +3VS_DGPU	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



## MULTI LEVEL STRAPS



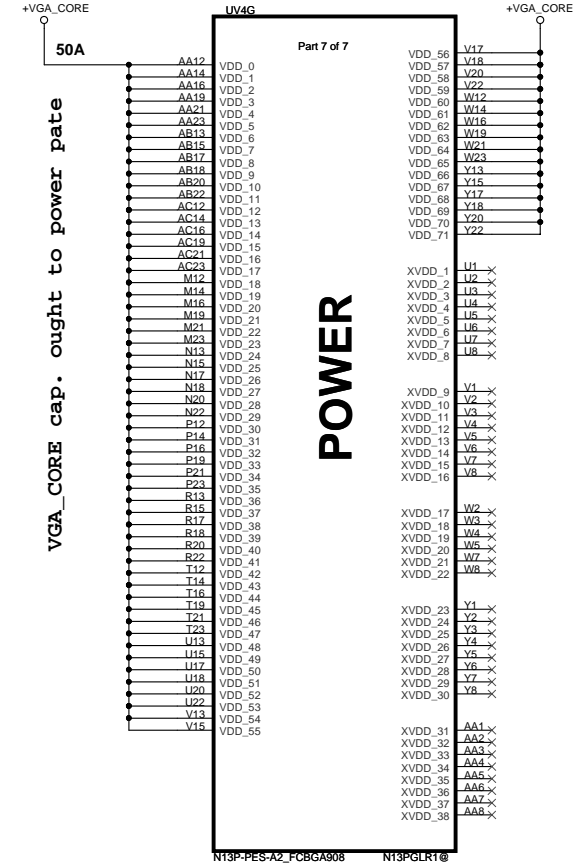
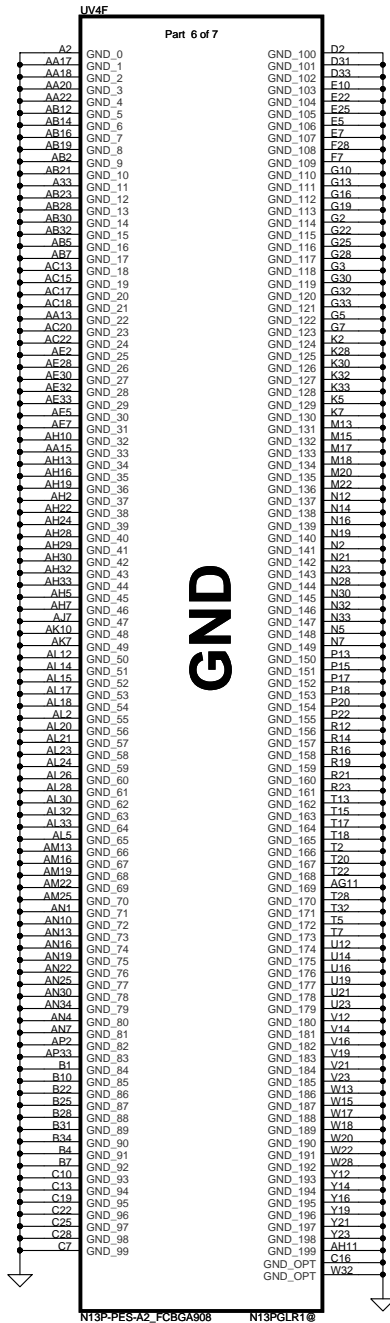
For X76

N13P-GL ROM_SI	Hynix (900MHZ) 64MX16 H5TQ1G63DFR-11C SA000041S20	1GB	0010	RV77 PD 15K (SD034150280)
	Hynix (900MHZ) 128MX16 H5TQ2G63BFR-11C SA00003Y000	2GB	0110	RV77 PD 34.8k (SD034348280)
	Hynix (900MHZ) 128MX16 H5TQ2G63DFR-11C SA00003Y070	2GB	0101	RV77 PD 30k (SD034300280)
	Samsung (900MHZ) 64MX16 K4W1G1646G-BC11 SA00004GS00	1GB	0011	RV77 PD 20K (SD034200280)
	Samsung (900MHZ) 128M16 K4W2G1646C-HC11 SA000047Q00	2GB	0111	RV77 PD 45.3K (SD034453280)
	Samsung (900MHZ) 128M16 K4W2G1646E-BC11 SA00005SH00	2GB	0001	RV77 PD 10K (SD028100280)

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Date: Tuesday, October 16, 2012				Sheet	15 of 53



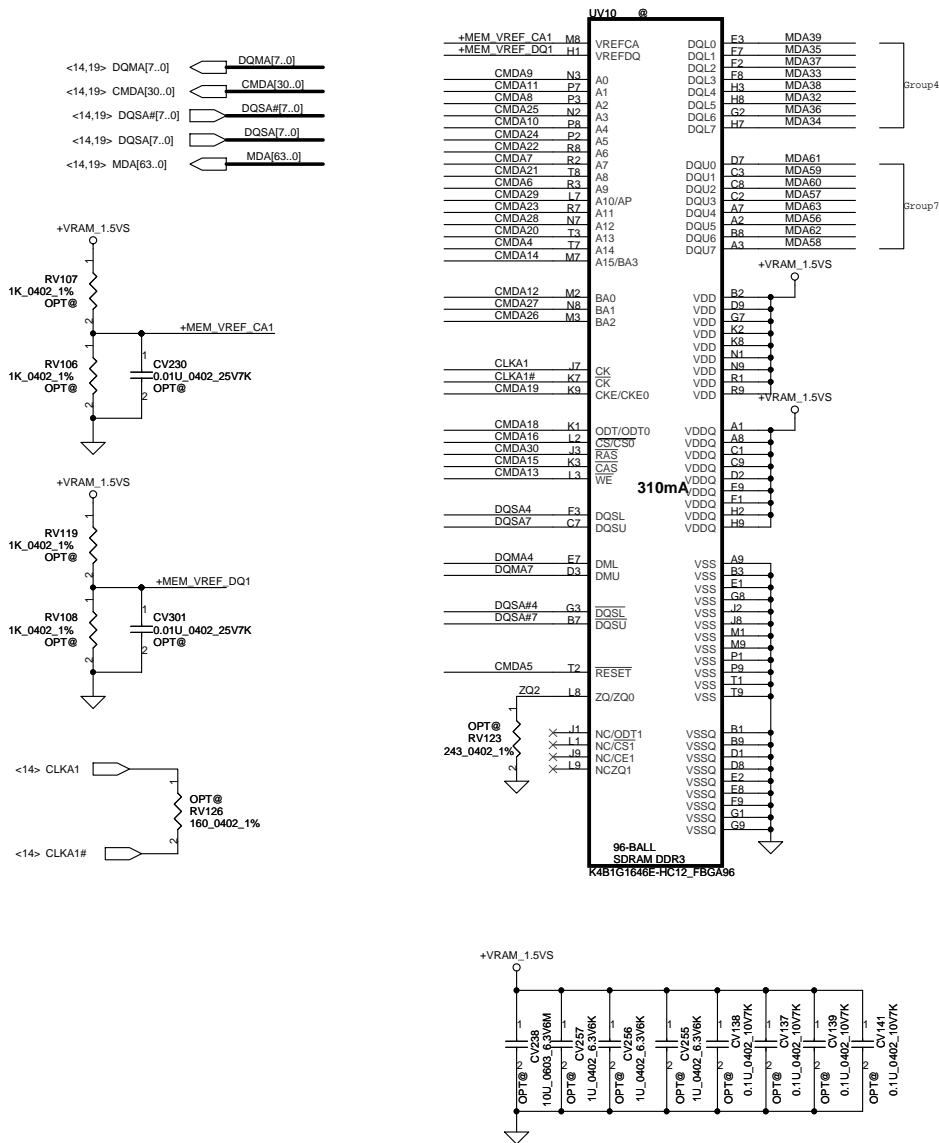




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Date: Tuesday, October 16, 2012				Sheet	17 of 53

# VRAM DDR3 chips (1GB)

64Mx16 DDR3 \*8==>1GB



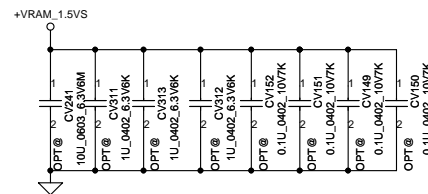
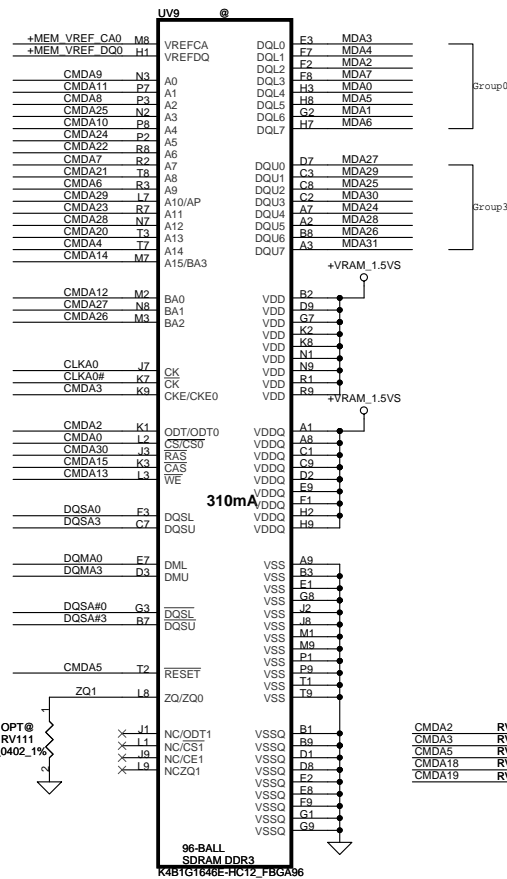
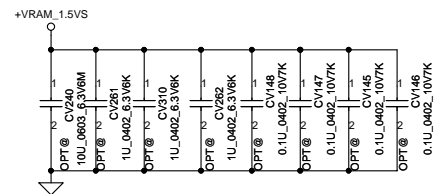
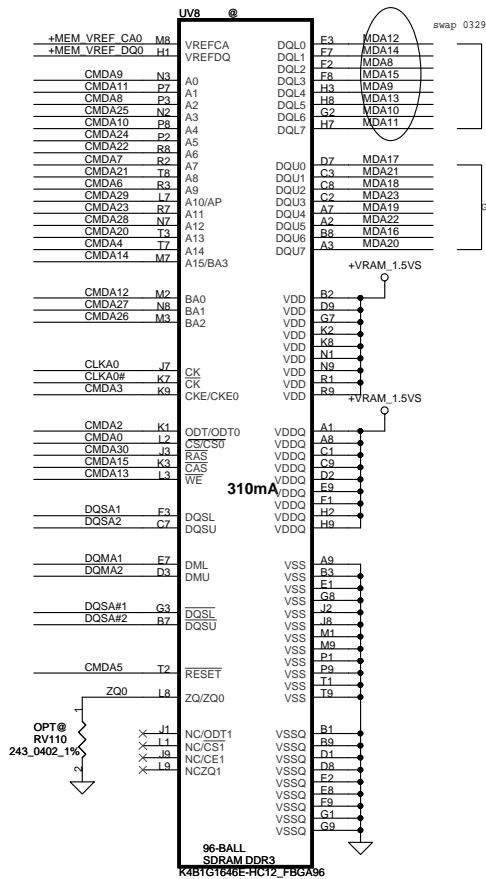
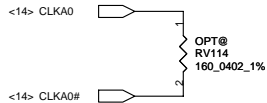
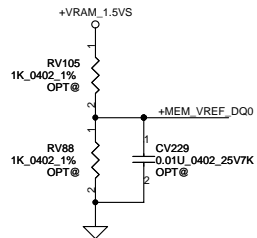
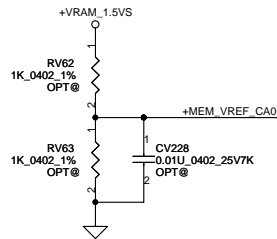
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*

LOW HIGH

# VRAM DDR3 chips (1GB)

64Mx16 DDR3 \*8==>1GB

<14,18> DQSA[7..0] DQSA[7..0]  
<14,18> DQSA# [7..0] DQSA# [7..0]  
<14,18> DQMA[7..0] DQMA[7..0]  
<14,18> MDA[63..0] MDA[63..0]  
<14,18> CMDA[30..0] CMDA[30..0]



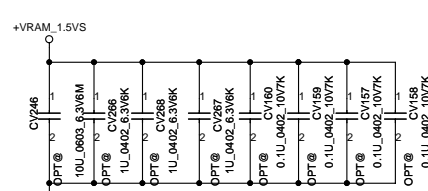
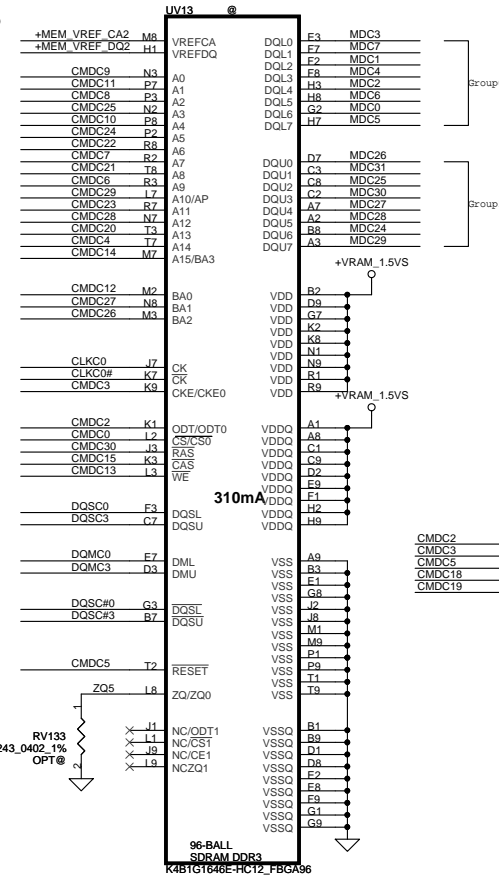
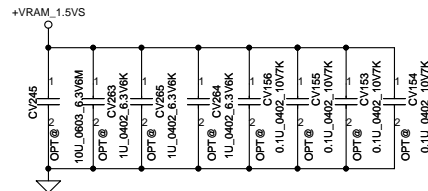
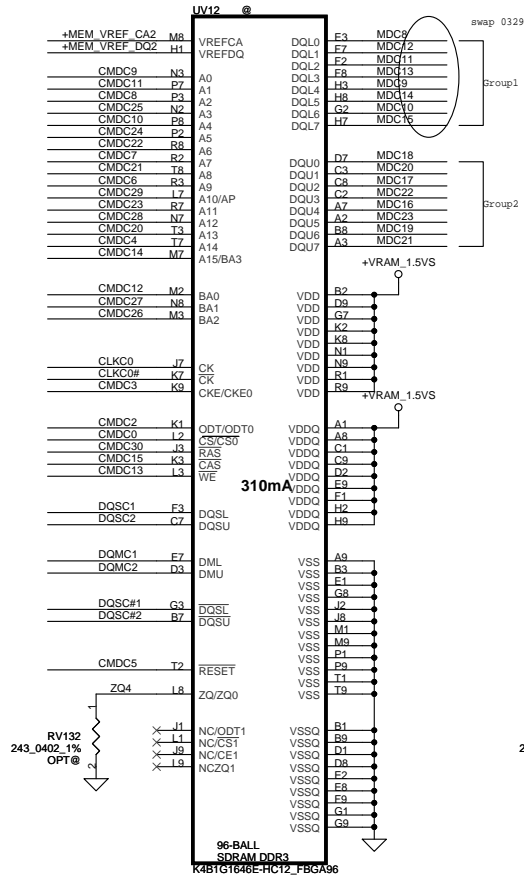
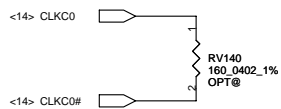
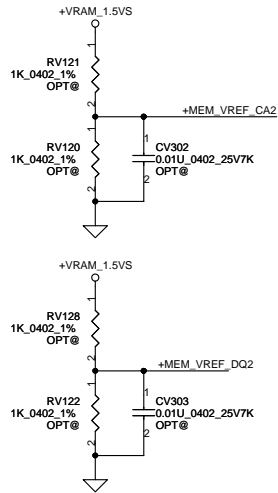
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CAS*	No Termination

# VRAM DDR3 chips (1GB)

64Mx16 DDR3 \*8==>1GB

<14,21> DQSC[7..0] DQSC[7..0]  
 <14,21> DQSC# [7..0] DQSC# [7..0]  
 <14,21> DQMC[7..0] DQMC[7..0]  
 <14,21> MDC[63..0] MDC[63..0]  
 <14,21> CMDC[30..0] CMDC[30..0]

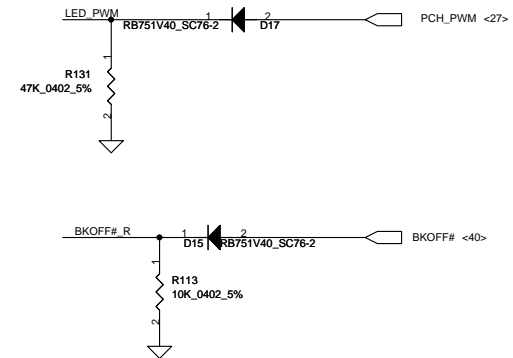
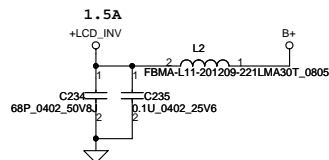
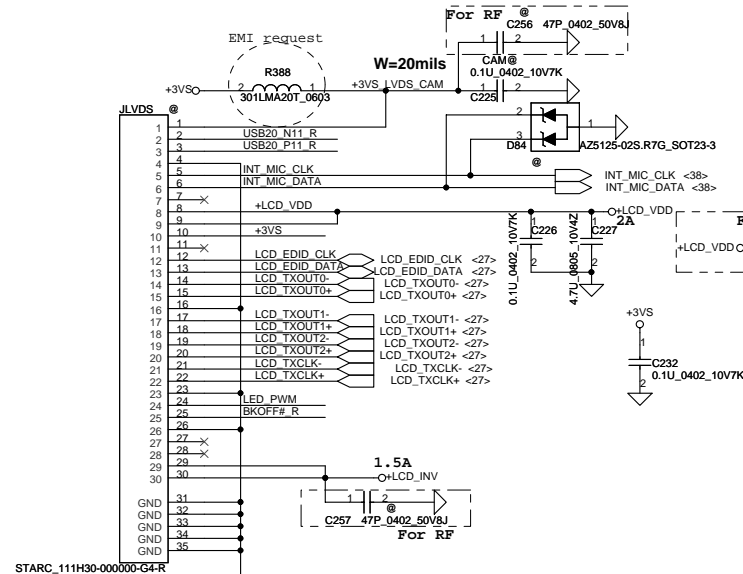
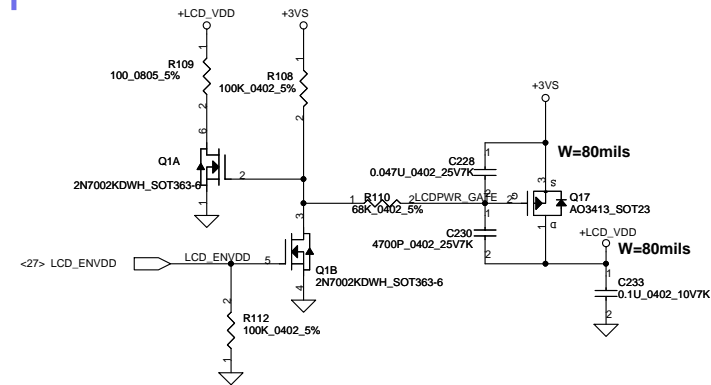
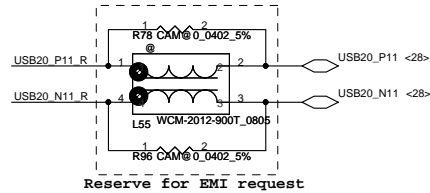


CMDC2 RV134 2 10K 0402 5%  
 CMDC3 RV135 2 10K 0402 5%  
 CMDC5 RV136 2 10K 0402 5%  
 CMDC18 RV137 2 10K 0402 5%  
 CMDC19 RV138 2 10K 0402 5%

Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination





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								Rev		Document Number		Rev	
								Customer		VCUAA		1.0	
Date:		Tuesday, October 16, 2012		Sheet		22		of		53			

<27> UMA_HDMI_TXC+	CV336	1	2	0.1U_0402_10V7K	UMA_DVI_TXC+
<27> UMA_HDMI_TXC-	CV337	1	2	0.1U_0402_10V7K	UMA_DVI_TXC-
<27> UMA_HDMI_TXD0+	CV338	1	2	0.1U_0402_10V7K	UMA_DVI_TXD0+
<27> UMA_HDMI_TXD0-	CV339	1	2	0.1U_0402_10V7K	UMA_DVI_TXD0-
<27> UMA_HDMI_TXD1+	CV340	1	2	0.1U_0402_10V7K	UMA_DVI_TXD1+
<27> UMA_HDMI_TXD1-	CV341	1	2	0.1U_0402_10V7K	UMA_DVI_TXD1-
<27> UMA_HDMI_TXD2+	CV342	1	2	0.1U_0402_10V7K	UMA_DVI_TXD2+
<27> UMA_HDMI_TXD2-	CV343	1	2	0.1U_0402_10V7K	UMA_DVI_TXD2-

HDMI Royalty

JHDMI1 45@

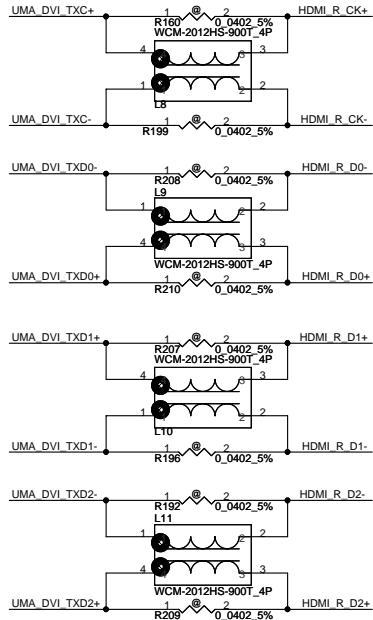
RO0000003HM

HDMI W/Logo + HDCP

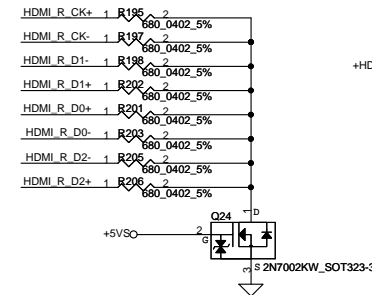
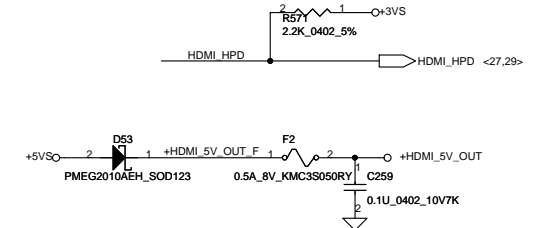
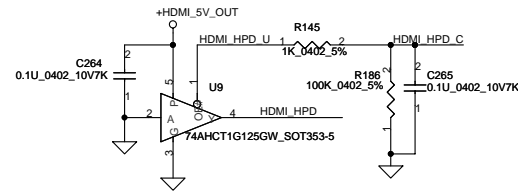
HDMI W/O Logo: RO0000001HM

HDMI W/Logo: RO0000002HM

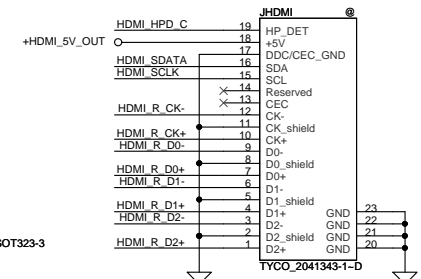
HDMI W/Logo + HDCP: RO0000003HM



common CHOKE use 67ohm  
5/30 change to 90ohm EMI request

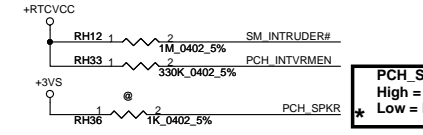
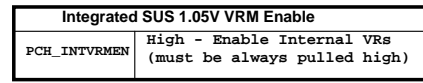
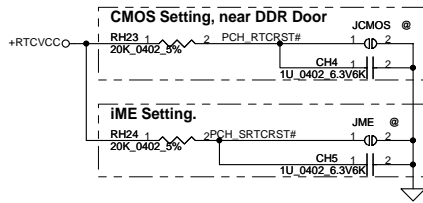


## HDMI Connector



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				1.0	VCUAA	1.0
				Date:	Tuesday, October 16, 2012	Sheet 23 of 53





**HDA\_SDO**

ME debug mode, this signal has a weak internal pull down

\*Low = Disable (default)

High = Enable (flash descriptor security override)

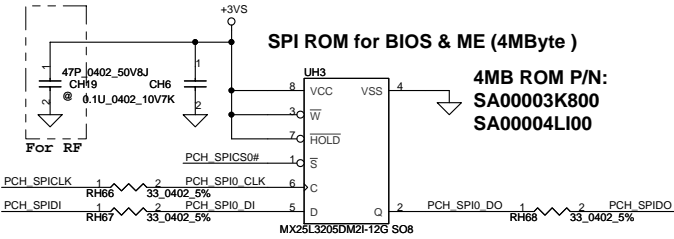
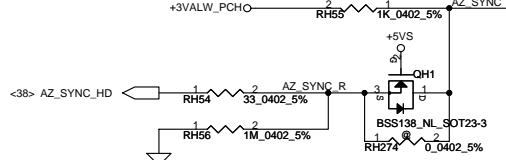
**HDA\_SYNC**

\*This signal has a weak internal pull down

H=>On Die PLL is supplied by 1.5V

L=>On Die PLL is supplied by 1.8V

Need to pull high for Chief River Mobile platform



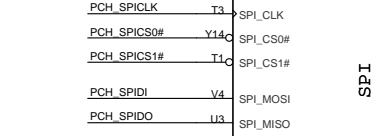
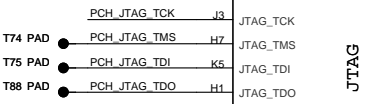
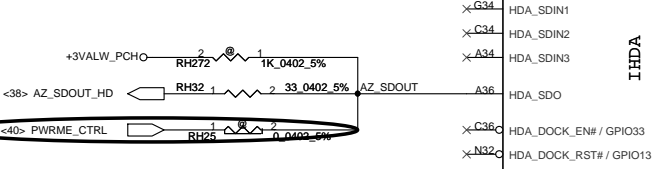
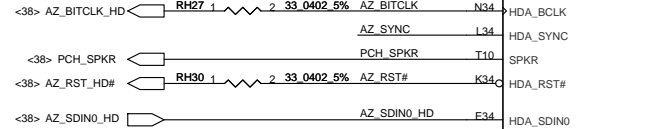
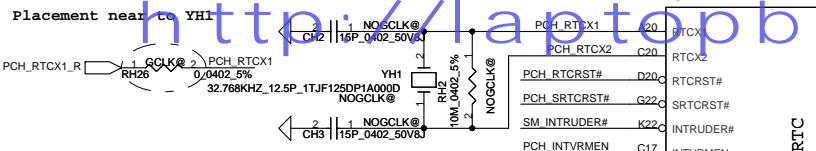
Socket: SP07000F500/SP07000H900

Please place U13 & U4 close to U2 PCH,

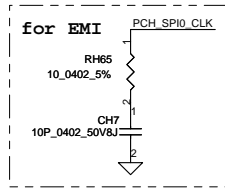
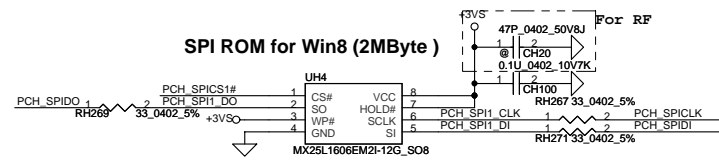
please place RH66, RH67, RH68 near UH3

Please place RH267 near RH66, Please place RH271 near RH67,

Please place RH269 near RH68.



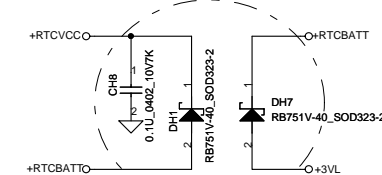
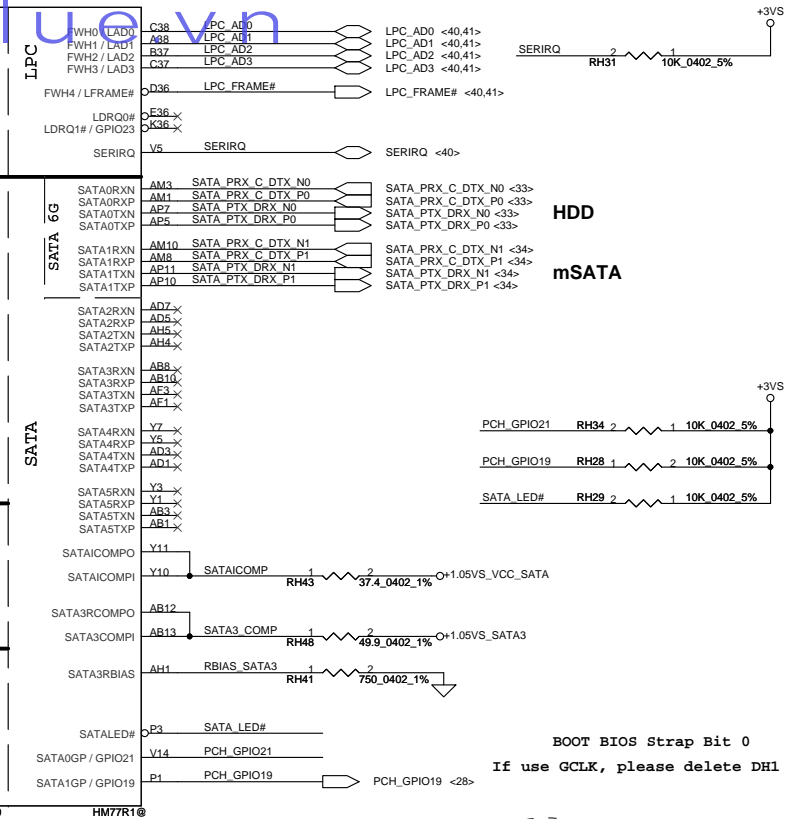
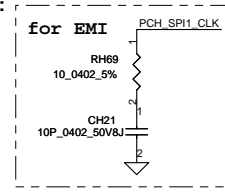
**SPI ROM for Win8 (2MByte)**



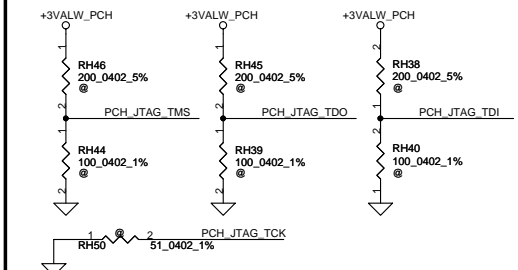
**2MB ROM P/N:**

SA000041N00

SA00003FO10

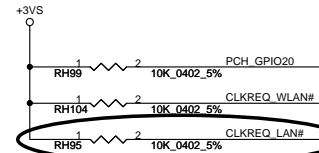
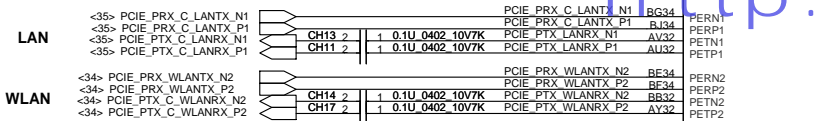


Un-mount for reduce power consumption at S0, S3 state

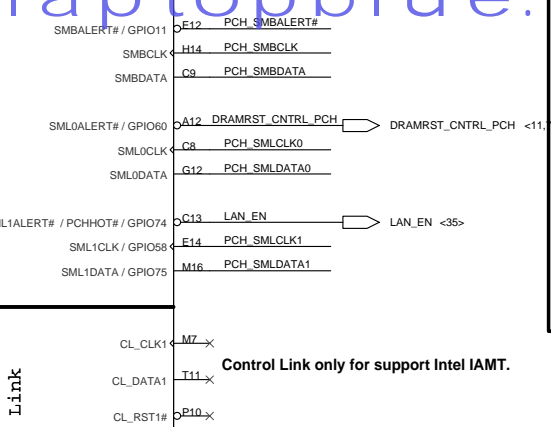
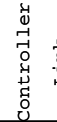
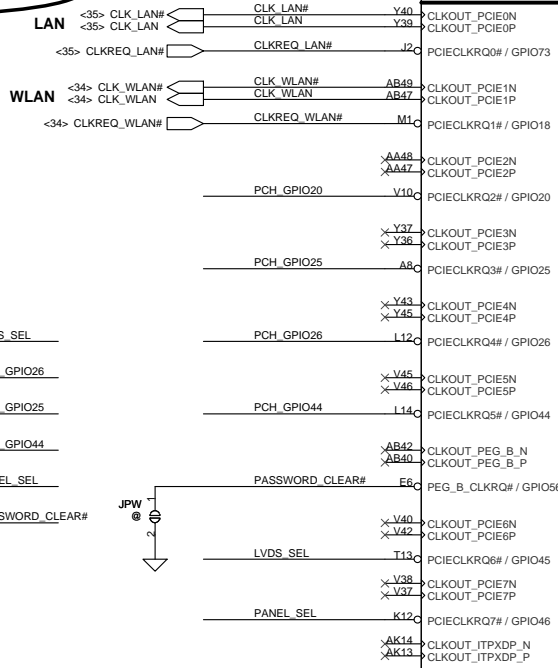
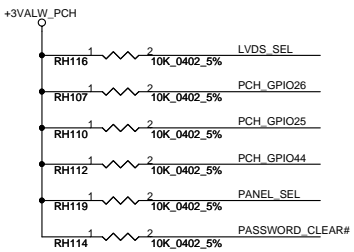


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								VCUAA			
								Date: Tuesday, October 16, 2012			
								Sheet 24 of 53			

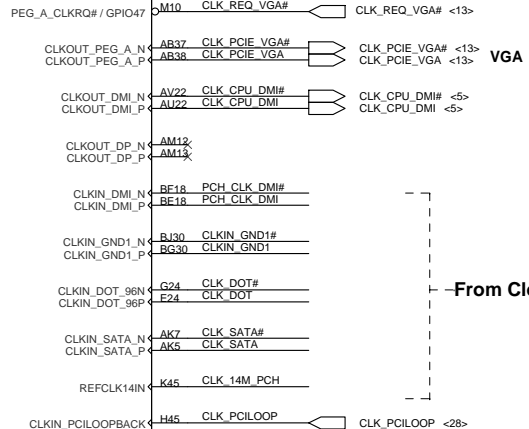




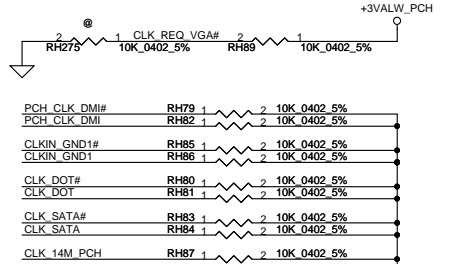
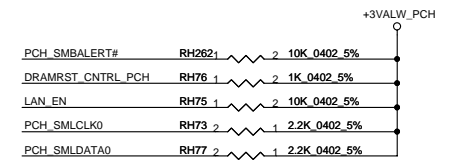
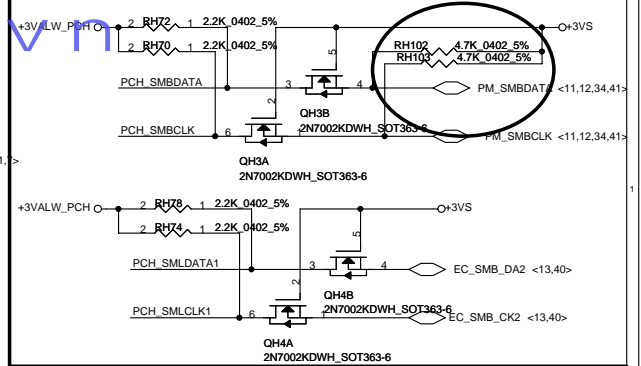
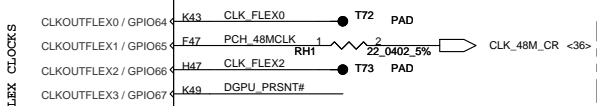
Intel Spec.  
PCIECLK\_RQ0# is suspend well,  
but we pull high to +3VS  
for LAN en/disable function



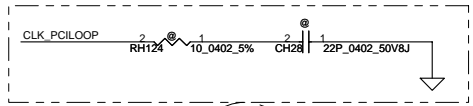
Control Link only for support Intel IAMT



–From Clock Gen.

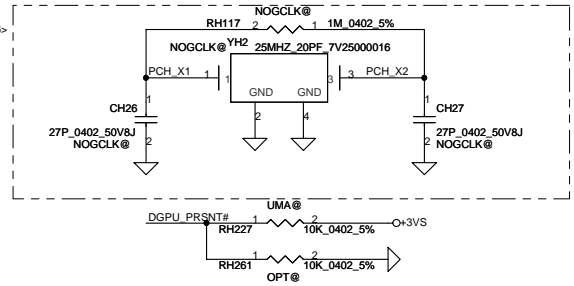


For EMI



<34> PCH\_X1\_R

Placement near to YH2

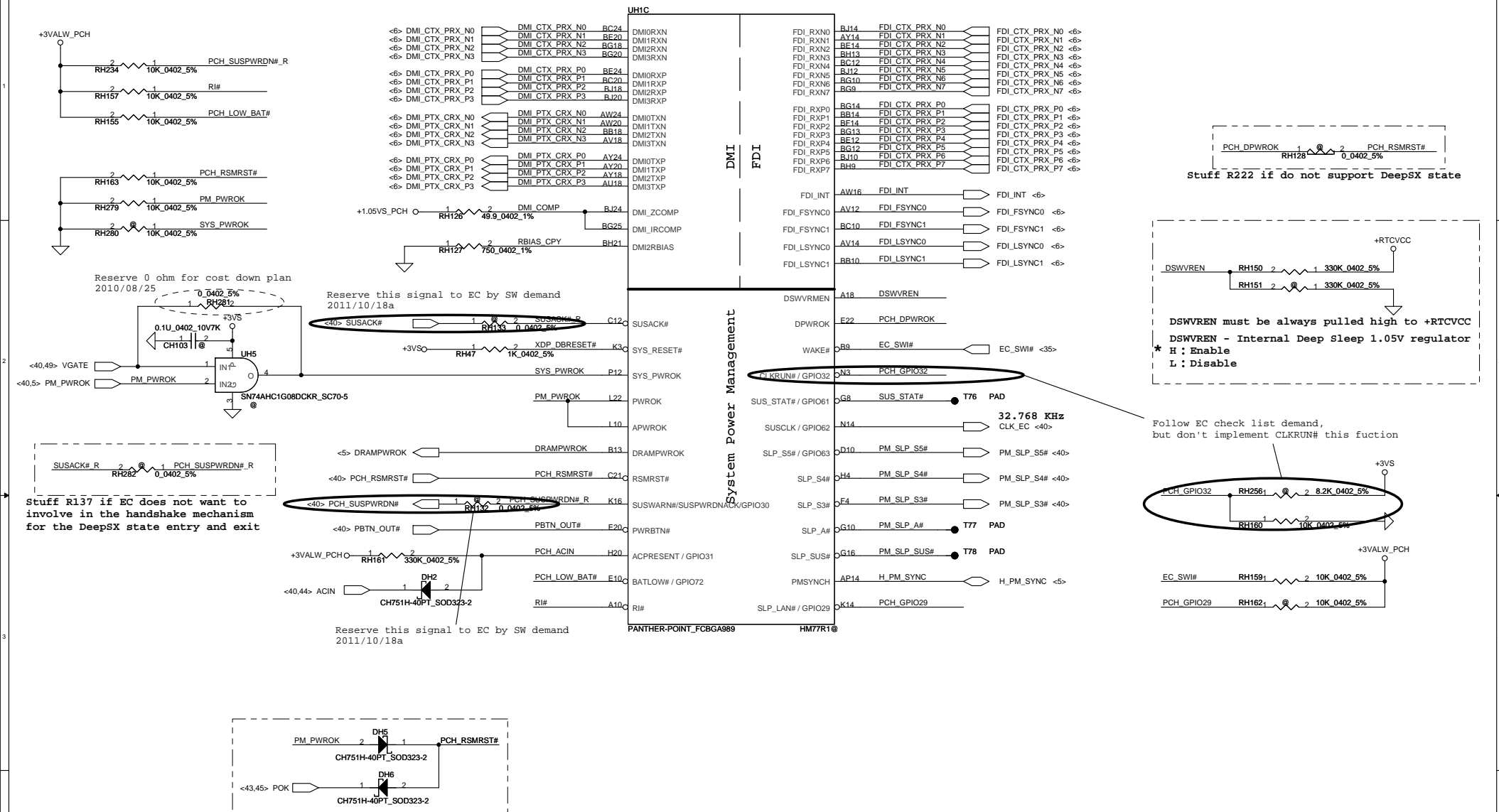


LVDS_SEL		
LVDS_SEL	H	L
Channel	Single (Default)	Dual

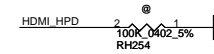
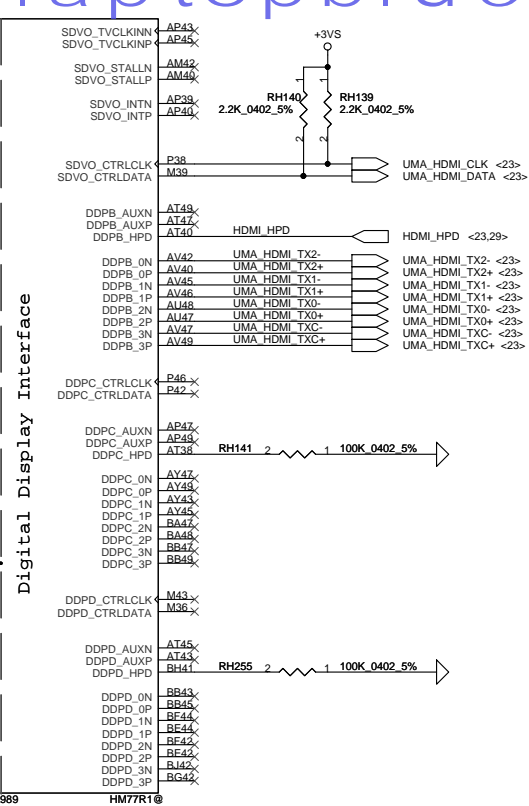
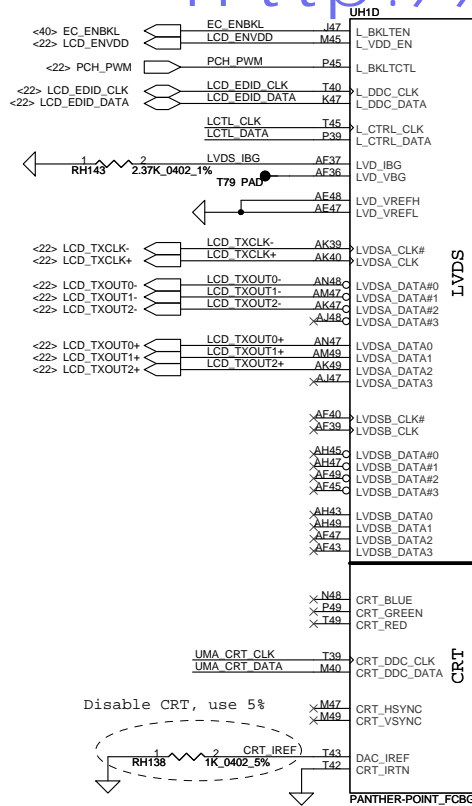
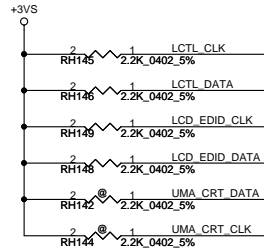
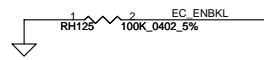
PANEL_SEL		
PANEL_SEL	H	L
Channel	LVDS	EDP

DGPU_PRSENT#		
DGPU_PRSENT#	H	L
M/B SKU	UMA	DIS/OPT

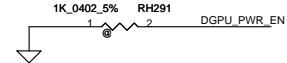
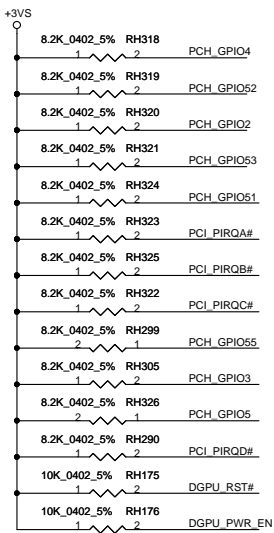
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	PCH_PCI-E/SMBUS/CLK	
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				VCUAA		
Date: Tuesday, October 16, 2012				Sheet	25	of 53



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					Docu- ment Number		Rev	
					VCUAA		1.0	
					Date: Tuesday, October 16, 2012		Sheet 26 of 53	



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Date:				Tuesday, October 16, 2012				Sheet 27 of 53			



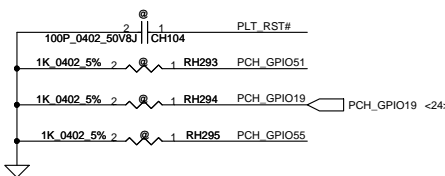
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 <37> U3RXDN2 U3RXDN2 BC30 USB3Rn2  
 <37> U3RXDN1 U3RXDN1 BE32 USB3Rn3  
 <37> U3RXDN2 U3RXDN2 B132 USB3Rn4  
 <37> U3RXDP1 U3RXDP1 BC28 USB3Rp1  
 <37> U3RXDP2 U3RXDP2 BE30 USB3Rp2  
 <37> U3TXDN1 U3TXDN1 BE32 USB3Rp3  
 <37> U3TXDN2 U3TXDN2 BC32 USB3Rp4  
 <37> U3TXDN1 U3TXDN1 AV28 USB3Tn1  
 <37> U3TXDN2 U3TXDN2 BB26 USB3Tn2  
 <37> U3TXDP1 U3TXDP1 AU28 USB3Tn3  
 <37> U3TXDP2 U3TXDP2 AY28 USB3Tn4  
 <37> U3TXDP1 U3TXDP1 AU28 USB3Tp1  
 <37> U3TXDP2 U3TXDP2 AY28 USB3Tp2  
 <37> U3TXDP1 U3TXDP1 AY28 USB3Tp3  
 <37> U3TXDP2 U3TXDP2 AW30 USB3Tp4

PCI\_PIRQA# K40C PIRQA#  
 PCI\_PIRQB# K38C PIRQB#  
 PCI\_PIRQC# H38C PIRQC#  
 PCI\_PIRQD# G38C PIRQD#  
 DGPU\_RST# C46C REQ1# / GPIO50  
 PCH\_GPIO52 C44C REQ2# / GPIO52  
 DGPU\_PWR\_EN E40C REQ3# / GPIO54  
 PCH\_GPIO51 D47C GNT1# / GPIO51  
 PCH\_GPIO53 E42C GNT2# / GPIO53  
 PCH\_GPIO55 F46C GNT3# / GPIO55

PCH\_GPIO2 G42C PIRQE# / GPIO2  
 PCH\_GPIO3 G40C PIRQF# / GPIO3  
 PCH\_GPIO4 C42C PIRQG# / GPIO4  
 PCH\_GPIO5 D44C PIRQH# / GPIO5

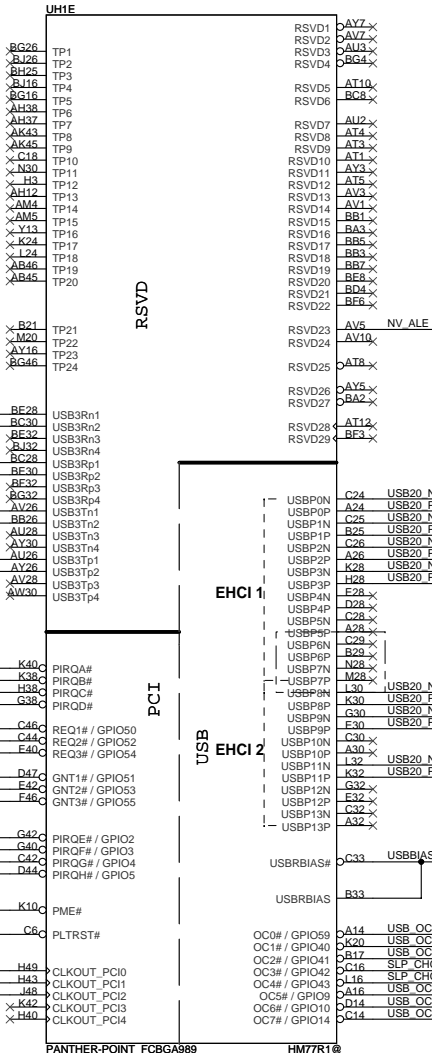
T80 PAD# PCI\_PME# K10C PME#  
 <34,35,40,41,5> PLT\_RST# C6C PLTRST#

<40> CLK\_PCI\_EC 22\_0402\_5% 1 RH167 CLK\_EC\_R H49 CLKOUT\_P00  
 <26> CLK\_PCILoop 22\_0402\_5% 1 RH166 CLK\_PCIL H43 CLKOUT\_P01  
 <41> CLK\_PCI\_DDR 22\_0402\_5% 1 RH294 CLK\_SIO J48 CLKOUT\_P02  
 <42> CLKOUT\_P03 X442 CLKOUT\_P03 X440 CLKOUT\_P04  
 <43> CLKOUT\_P04 X440 CLKOUT\_P04 X440 CLKOUT\_P04



Boot BIOS Strap			
RE_OFF#	PCH_GPIO19	Boot BIOS Location	
0	0	LPC	
0	1	Reserved	
1	0	PCI	
1	1	SPI *	

A16 Swap Override Strap	
WL_OFF#	
	Low= A16 swap override Enable
*	High= A16 swap override Disable



EHCI 1

EHCI 2

USB

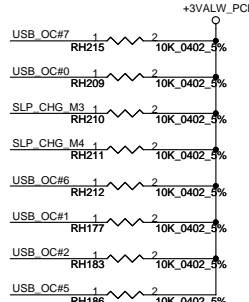
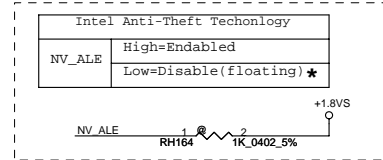
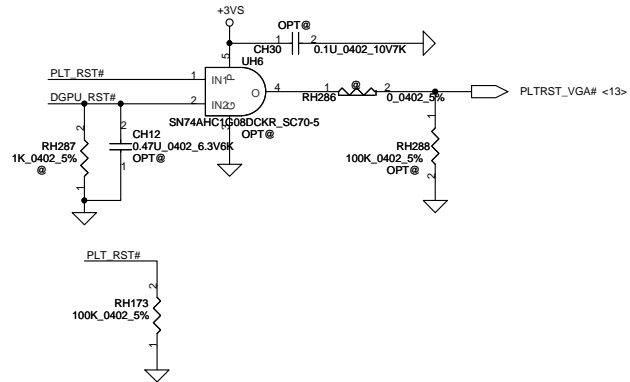
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HM77R1

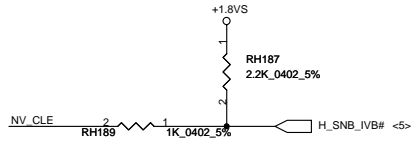
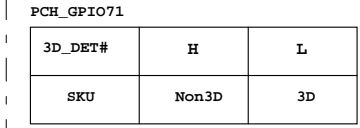
USB-Right1  
 USB-Right2  
 USB-Left  
 CardReader

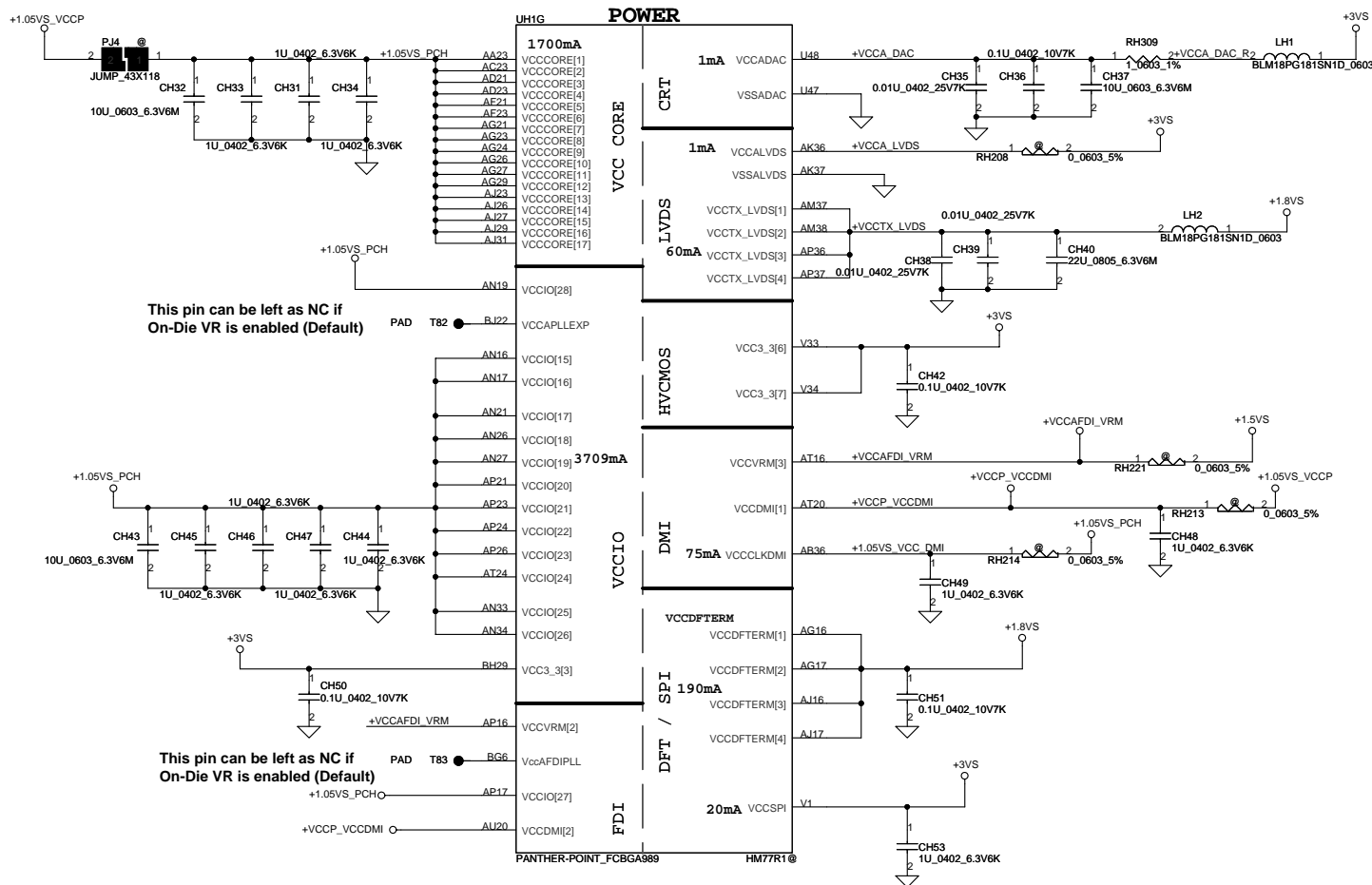
BT  
 Int. Camera

USB-Right Front  
 USB-Right Rear  
 USB-Left



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								Document Number		Rev 1.0	
								VCUAA			
Date:		Tuesday, October 16, 2012		Sheet		28 of 53					

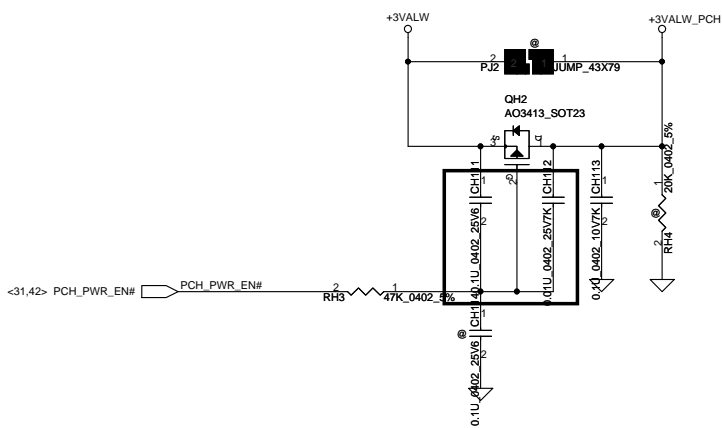




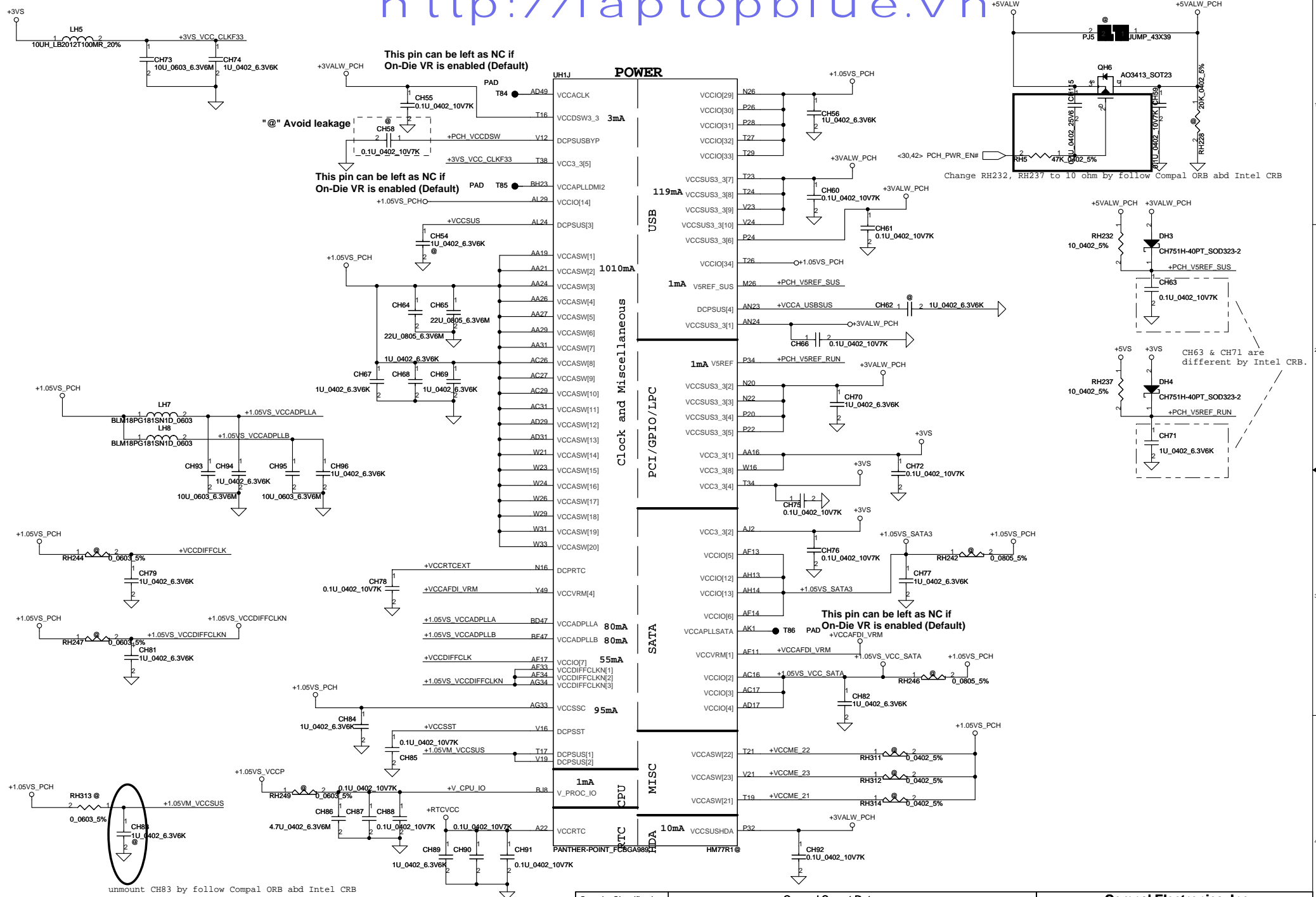
PCH Power Rail Table  
Refer to PCH EDS R1.0

Voltage Rail	Voltage	S0 Iccmax Current (mA)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	N/A
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKLN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

**+3VALW to +3V\_PCH**

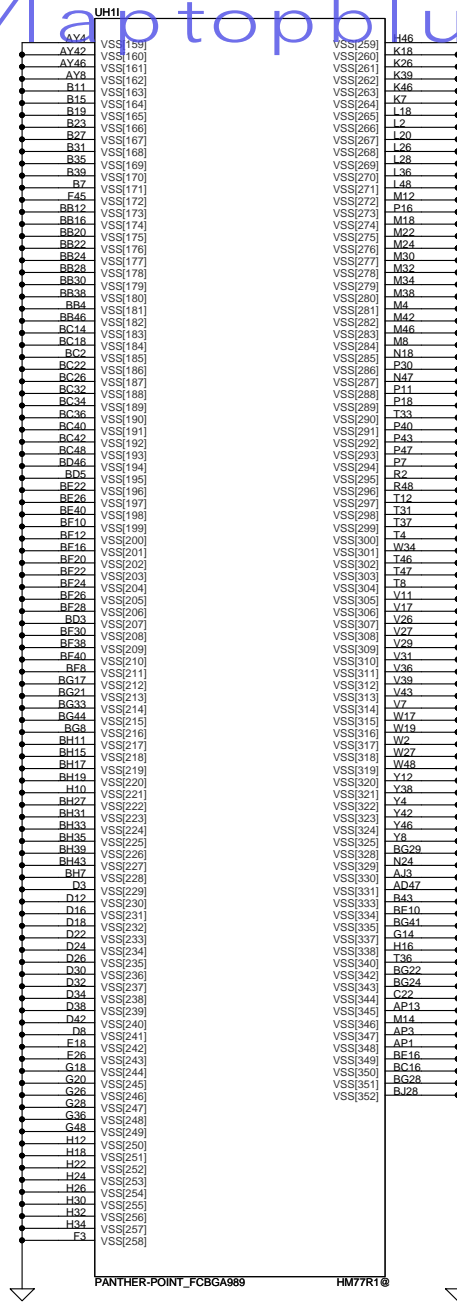
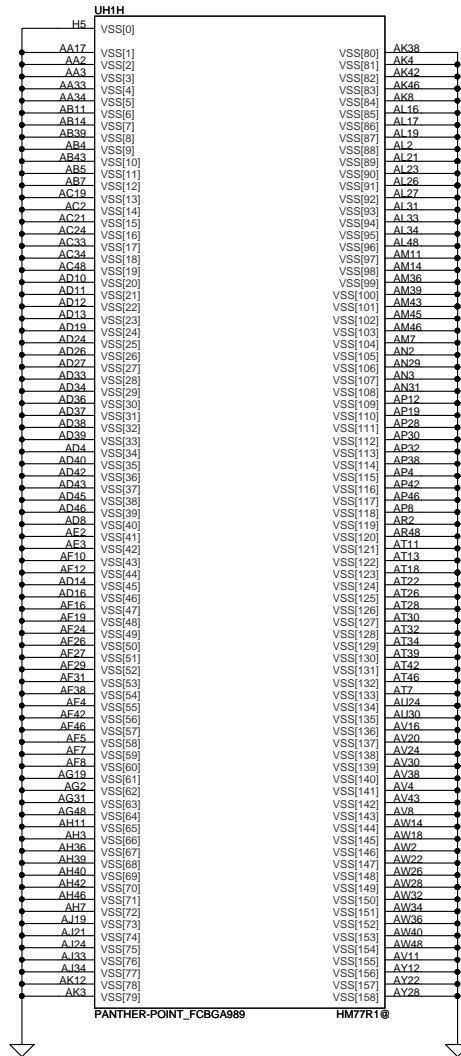


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				Custom	1.0
Date:	Tuesday, October 16, 2012	Sheet	30	of	53



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				Custom	1.0
Date:	Tuesday, October 16, 2012	Sheet	31	of	53

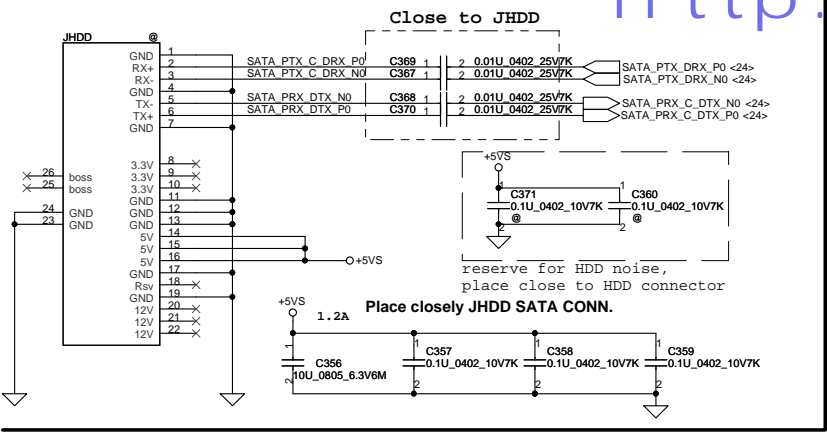




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				Rev	1.0
				Date:	Tuesday, October 16, 2012
				Sheet	32 of 53



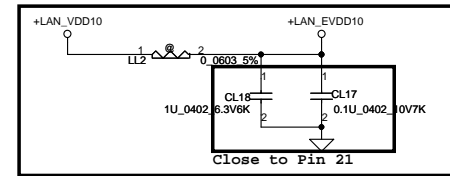
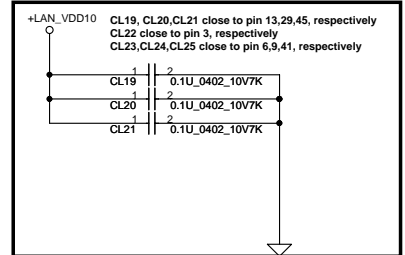
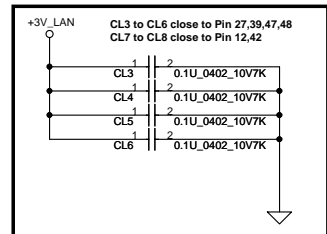
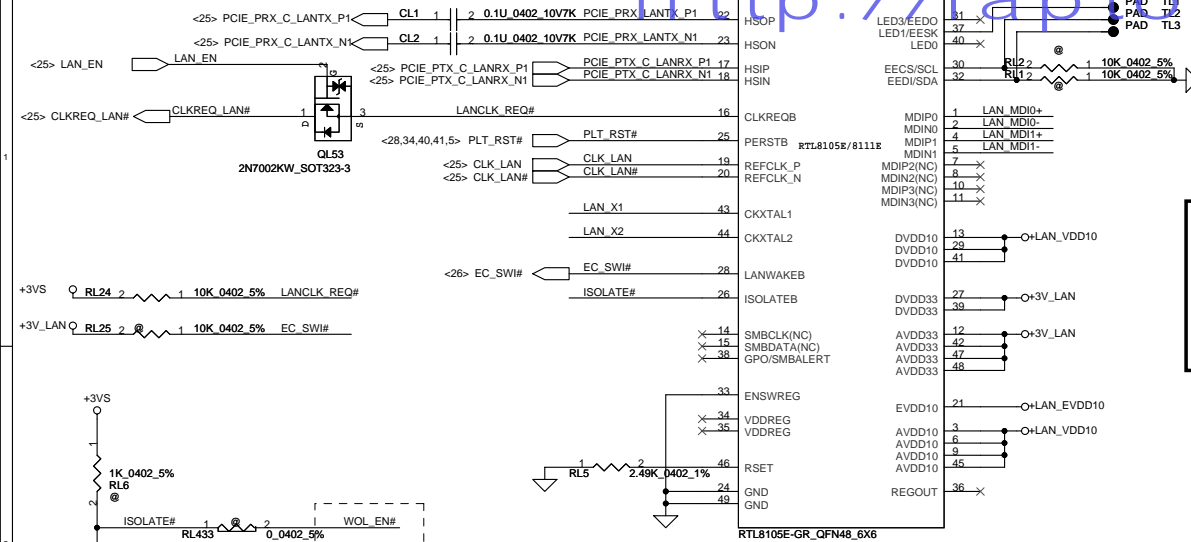
SATA HDD Conn.



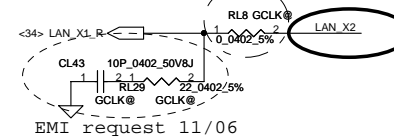
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Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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										Rev	
										1.0	
										Date: Tuesday, October 16, 2012	
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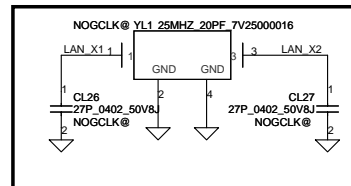




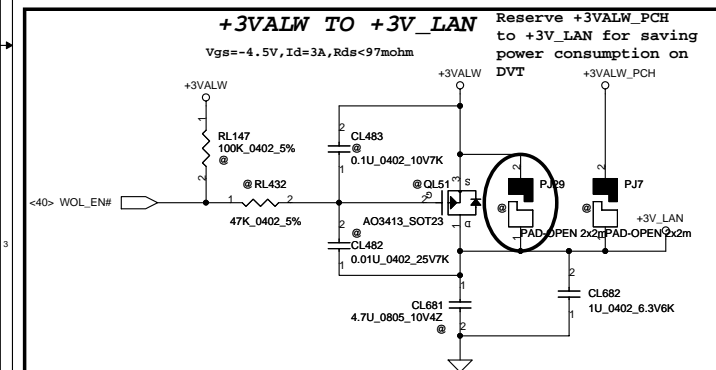
Placement near to YL1



	Sx Enable Wake up	Sx Disable Wake up	S0		RTL8105E	RTL8111E/F
				Pin14	NC	NC
WOL_EN#	LOW	HIGH	HIGH	Pin15	NC	10K ohm PD
				Pin38	NC	1K ohm PH



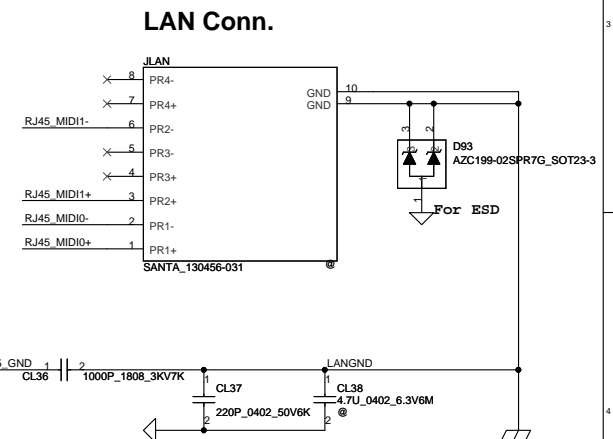
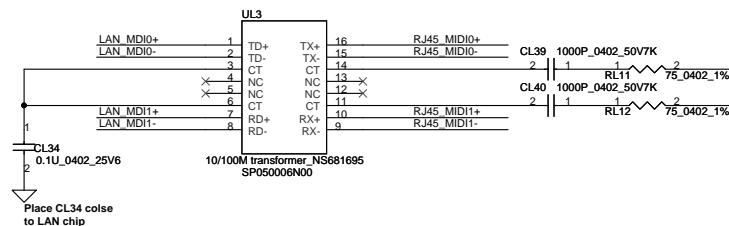
	8105E-VL/VD 8111F/F-VB PWM Mode	8105E-VL/VI LDO Mode
RL4	0 ohm (Pull High)	NC
RL23	NC	0 ohm (Pull Down)



**+3V\_LAN rising time (10%~90%) need > 1ms and <100ms.**

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

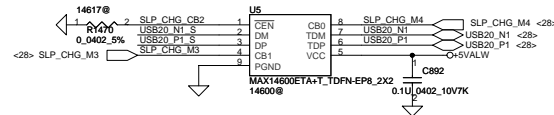
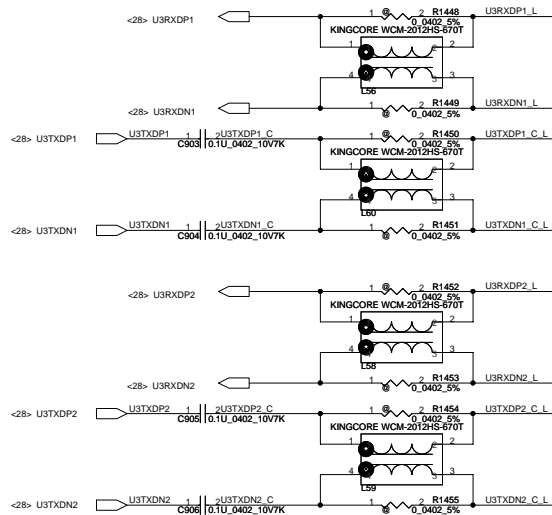
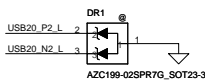
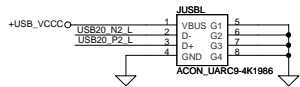
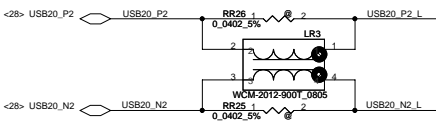
```
*
S3:  after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms
```



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				VCUAA		1.0	
				Date:	Tuesday, October 16, 2012	Sheet	35 of 53



# Left USB 2.0 x 1

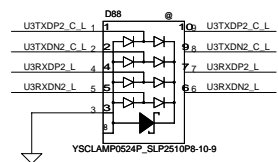
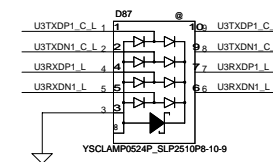
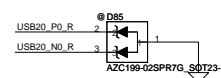
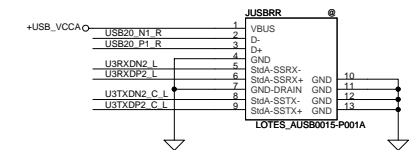
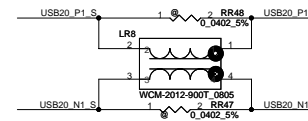
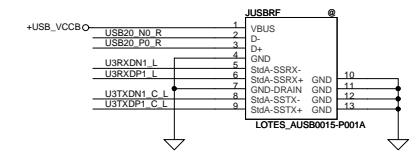
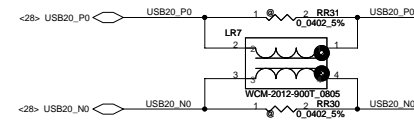
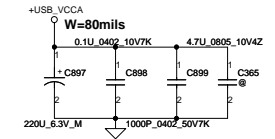
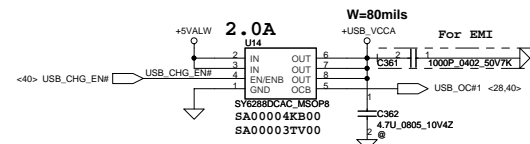
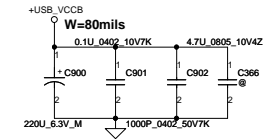
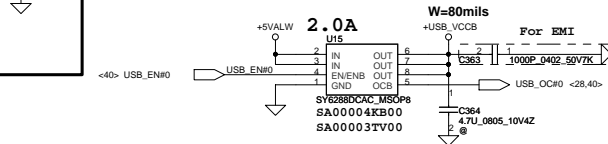
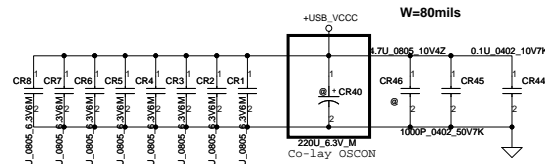
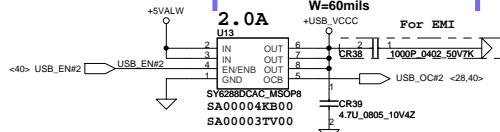


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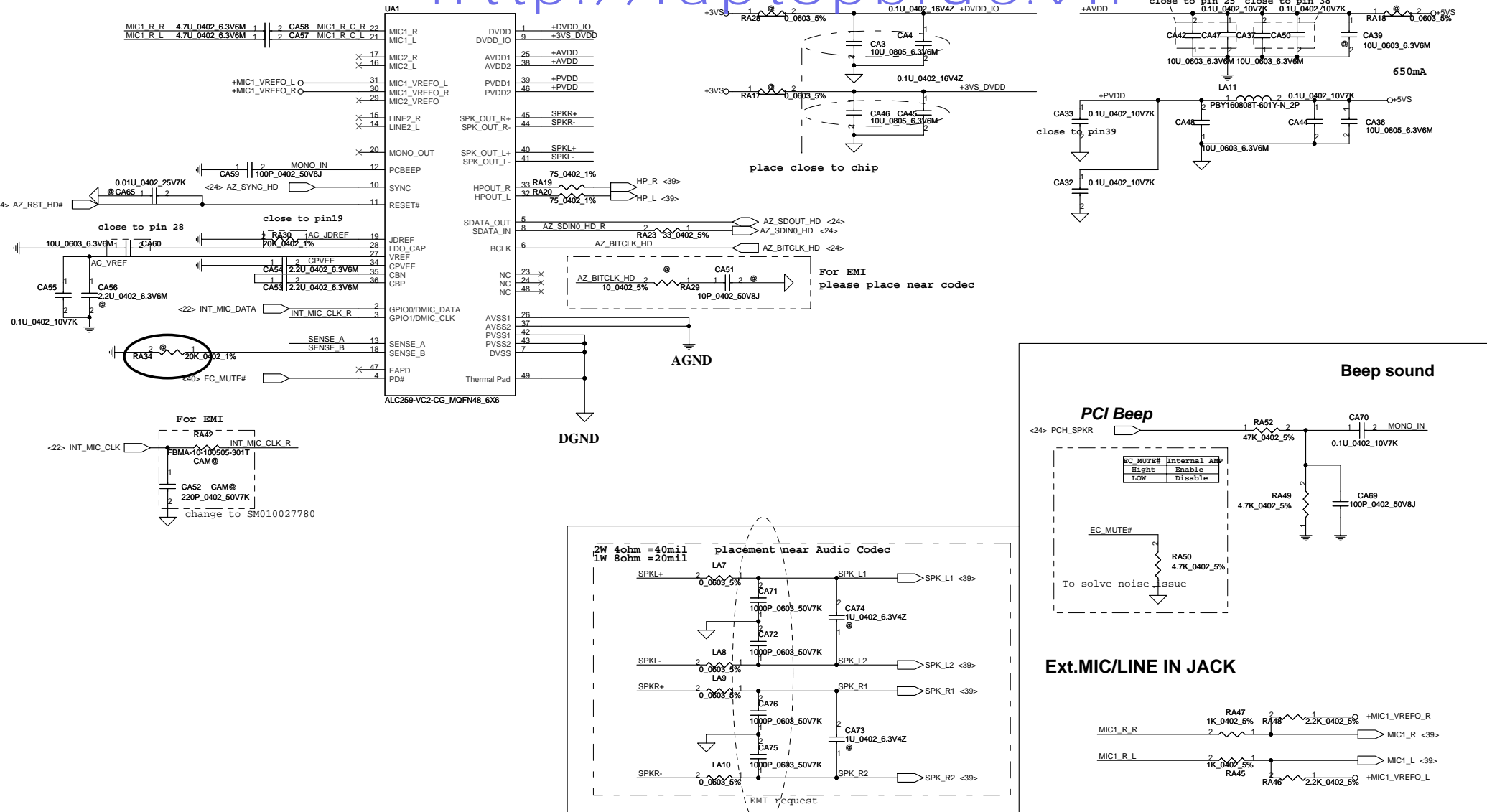
# Right side USB 3.0 x 2/ Sleep&Charge

## USB Sleep & Charge Auto-Mode/Mode3

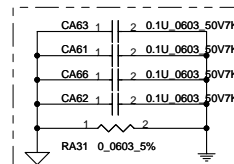
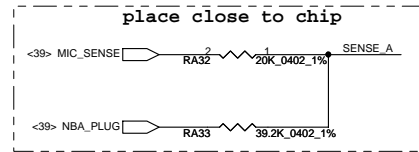
MAX14600 & MAX14617			
CB0 SLP_CHG_M4	CB1 SLP_CHG_M3	CB2 (14617 only)	STATUS
0	0	0	AUTO MODE
0	1	0	Force Dedicated charger mode (MODE3)
1	0	0	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM
1	1	0	Pass-Through (USB) Mode with CDP Emulation: Auto Connect DP/DM to TDP/TDM depending on CDP status
X	X	1	Force Apple 2A Charger Mode: Apple 2A resistor dividers



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Customer			Document Number	
Date: Tuesday, October 16, 2012			Sheet 37 of 53	



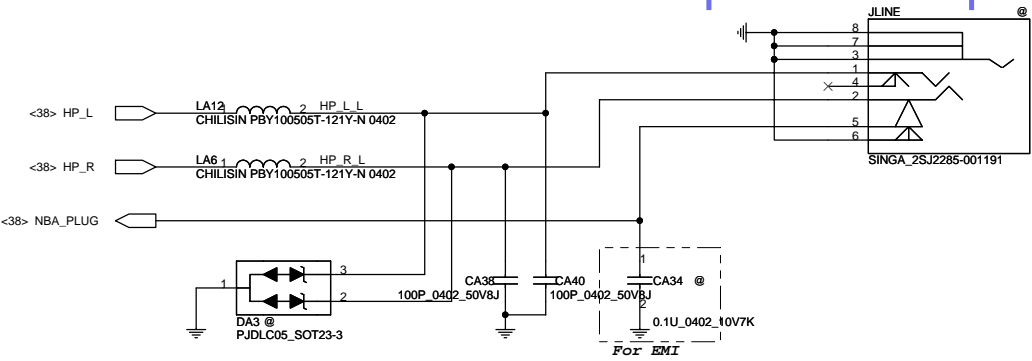
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



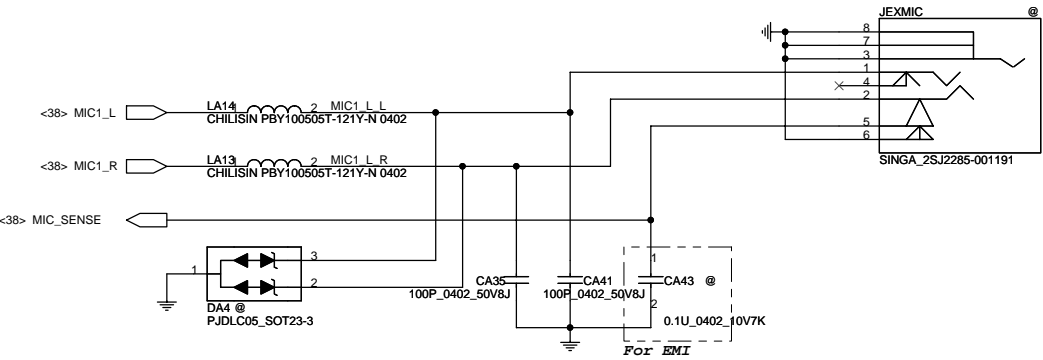
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Date: Tuesday, October 16, 2012				Sheet 38 of 53

HeadPhone/LINE OUT JACK

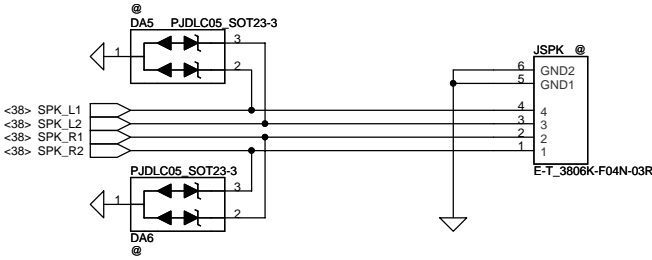
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EXT.MIC/LINE IN JACK



SPK CONN.



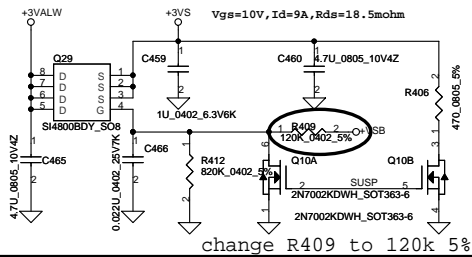
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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	AUDIO CONN	
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				Date:	Tuesday, October 16, 2012	Sheet 39 of 53



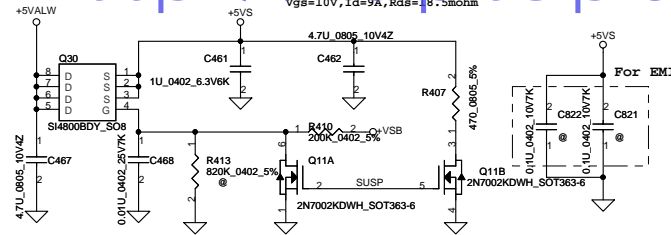




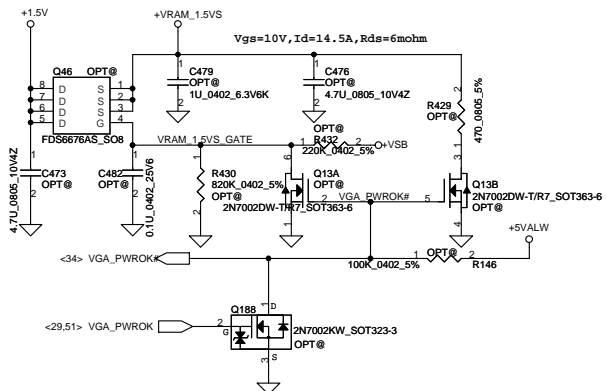
### +3VALW TO +3VS



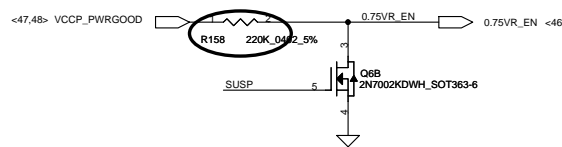
### +5VALW TO +5VS



### +1.5V to +VRAM\_1.5VS



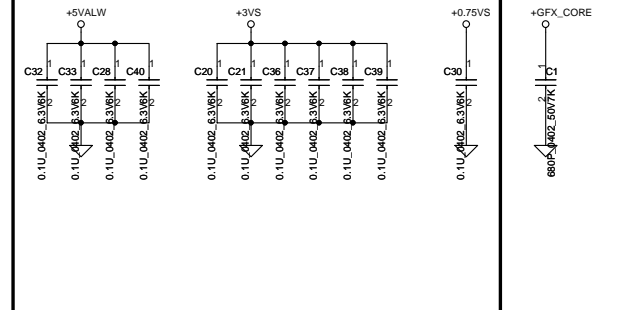
### For S3 CPU Power Saving



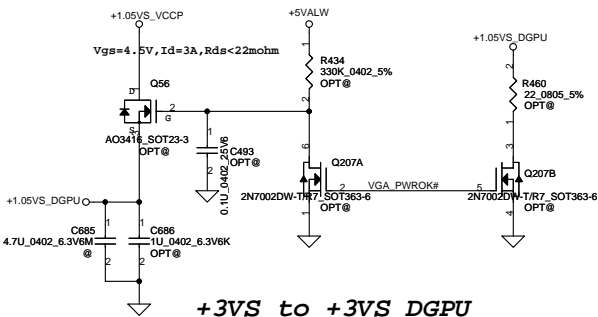
Reserve CAP to avoid Power Noise

ESD Cap., please keep original location

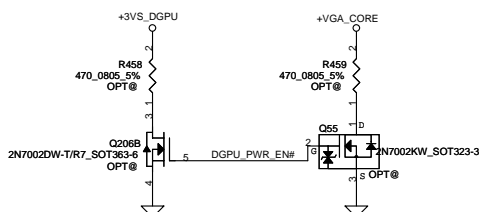
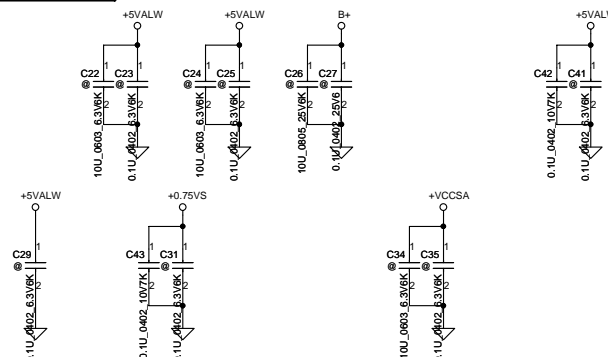
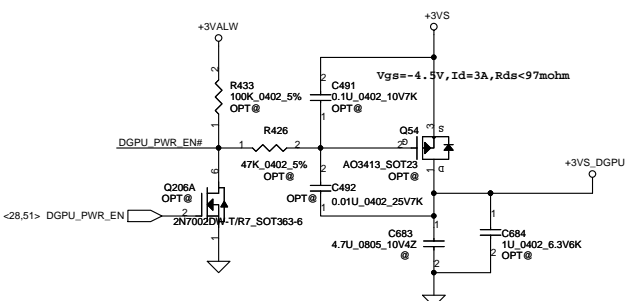
EMI request



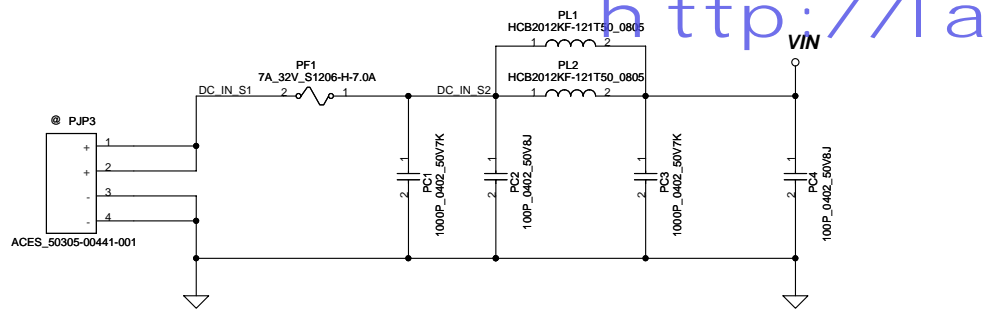
### +1.05VS\_VCCP to +1.05VS\_DGPU



### +3VS to +3VS\_DGPU

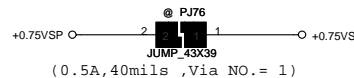
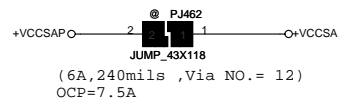
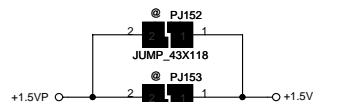
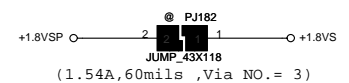
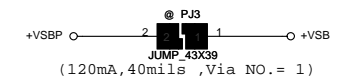
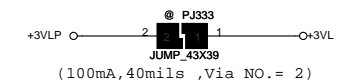
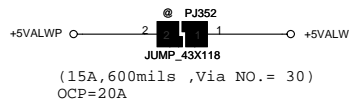
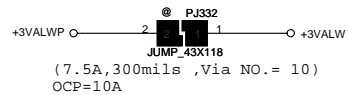
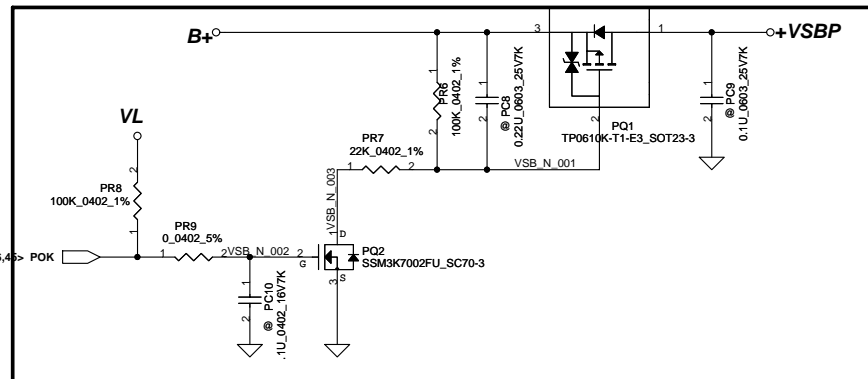
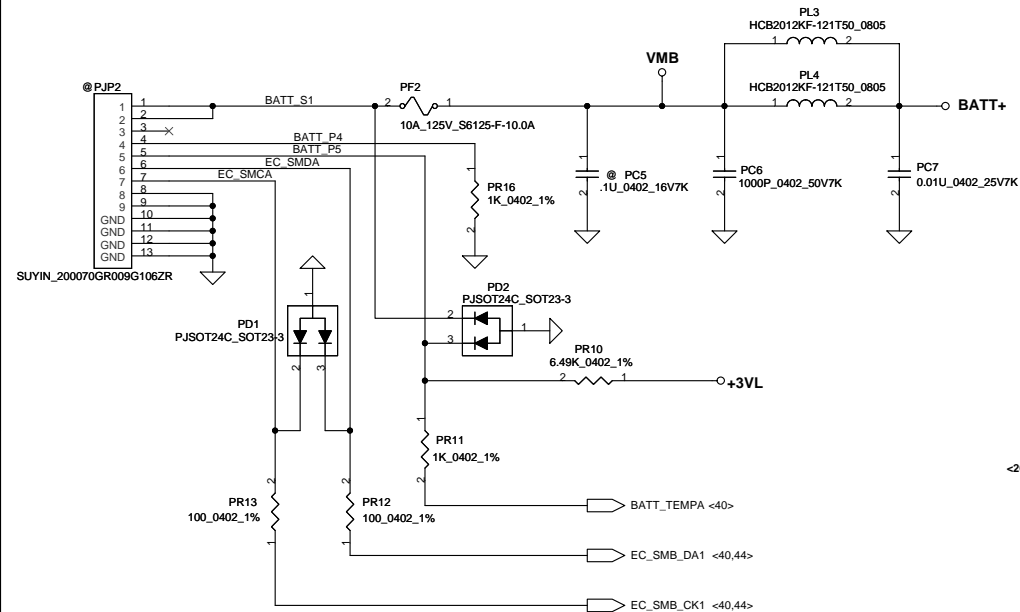
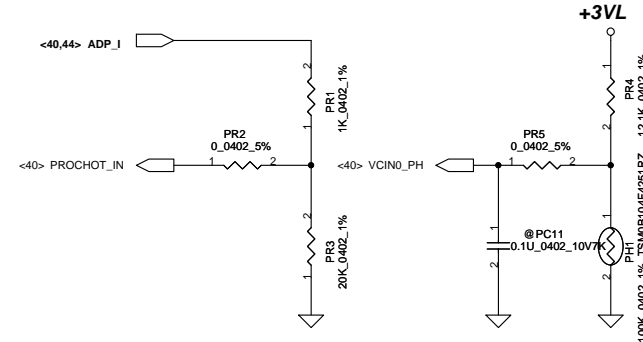


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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	DC-DC INTERFACE
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				Date	Tuesday, October 16, 2012
				Sheet	42 of 53

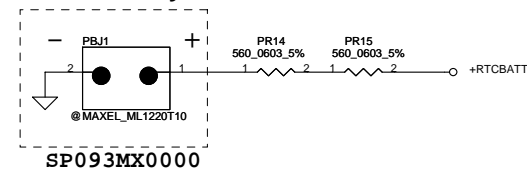


**PJ11 under CPU bottom side:**  
**CPU thermal protection at 93 +3 degree C**  
**Recovery at 56 +3 degree C**

Please locate these parts  
 Near EC chip



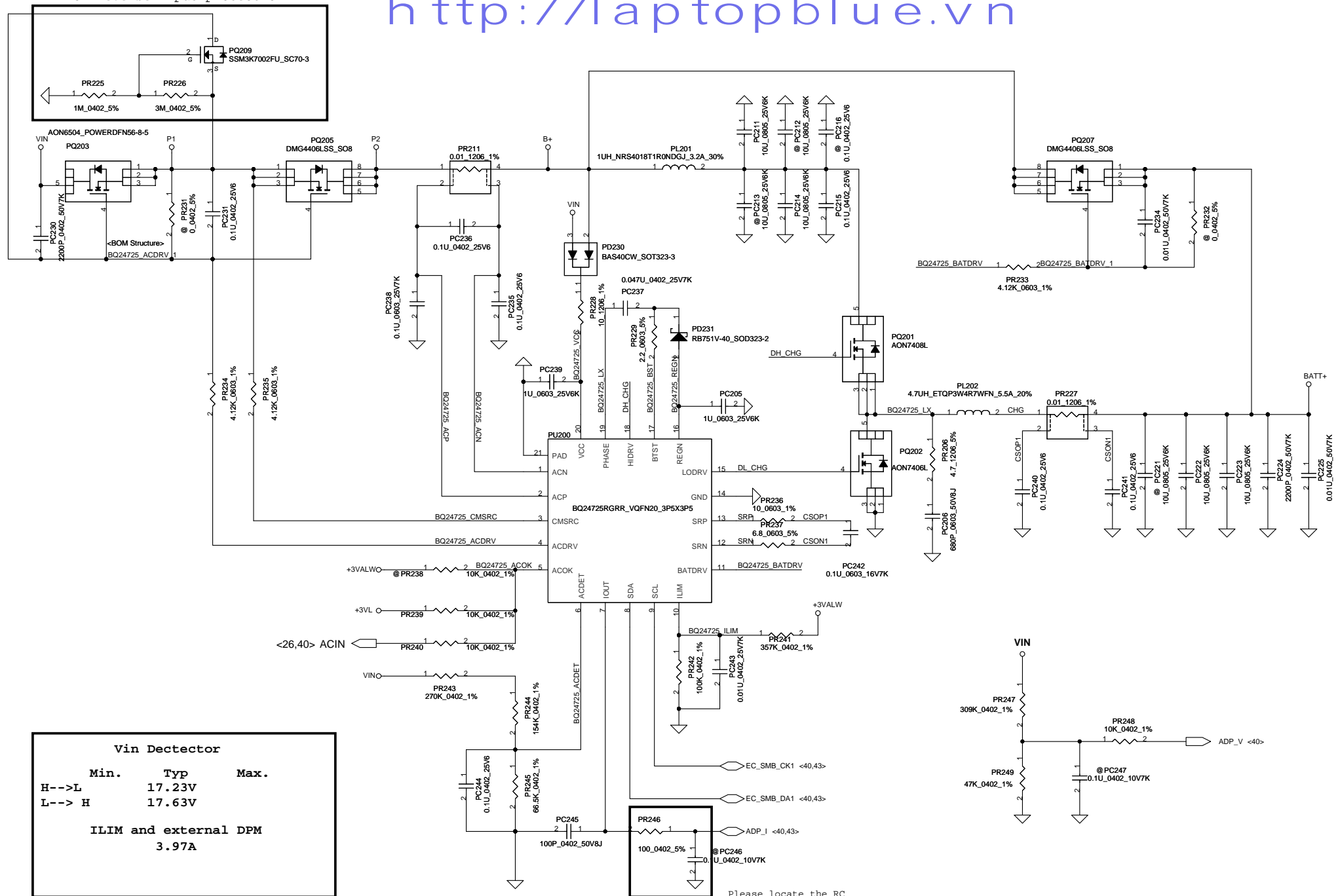
**RTC Battery**



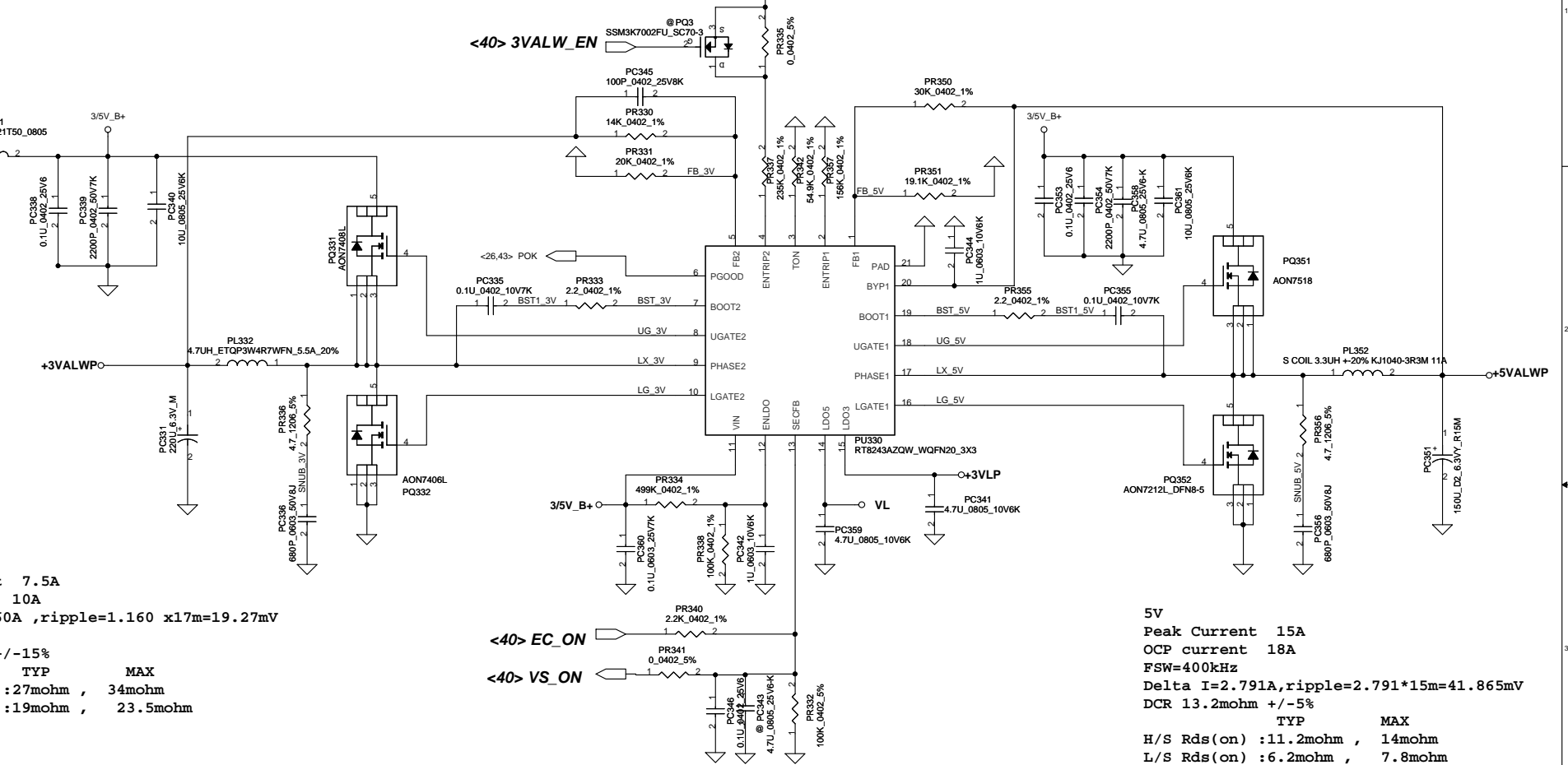
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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	<b>PWR-DCIN / BATT CONN / OTP</b>
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				Date:	Tuesday, October 16, 2012
				Sheet	43 of 53
				Rev	1.0

for reverse input protection

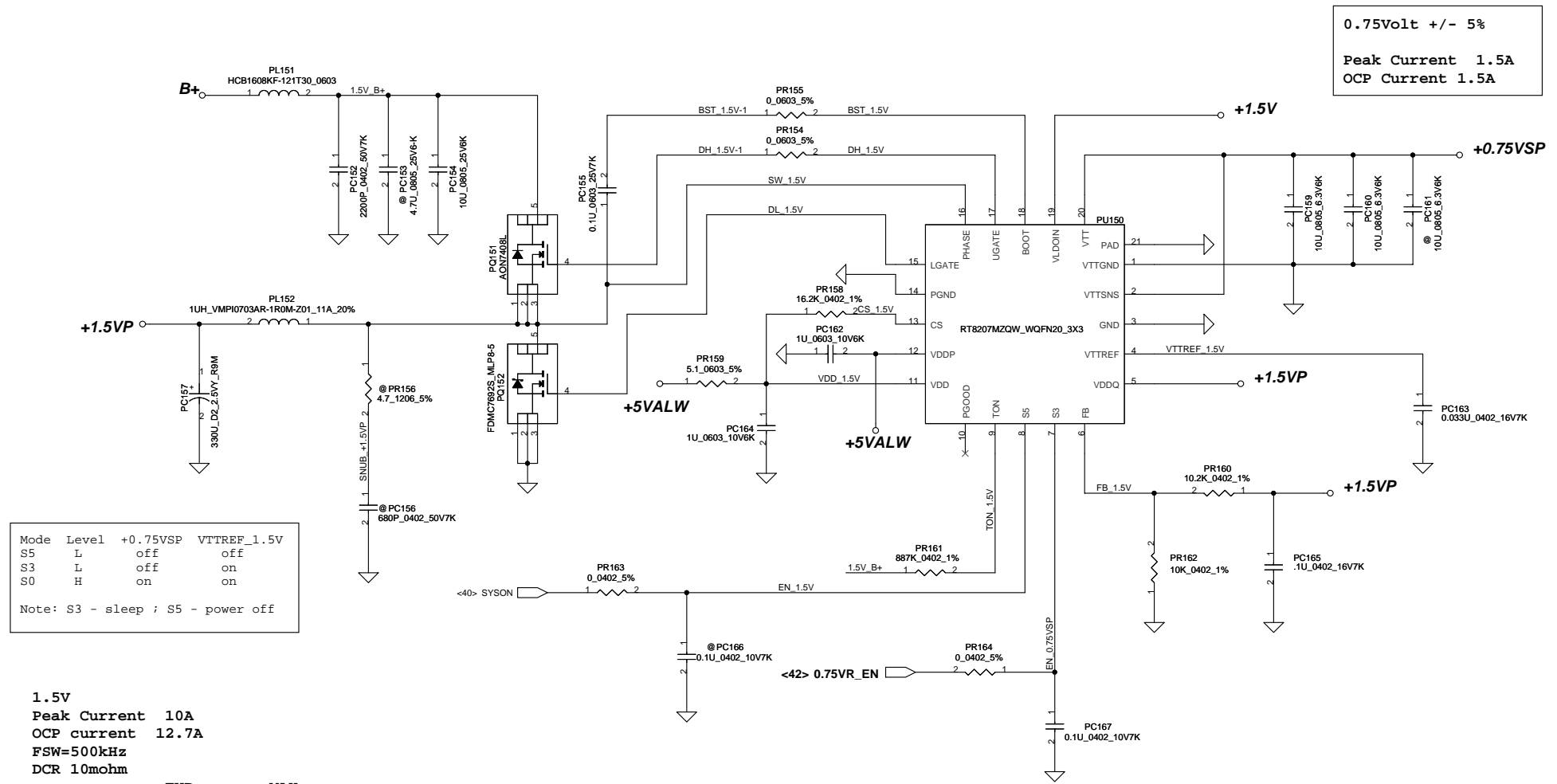
http://laptopblue.vn



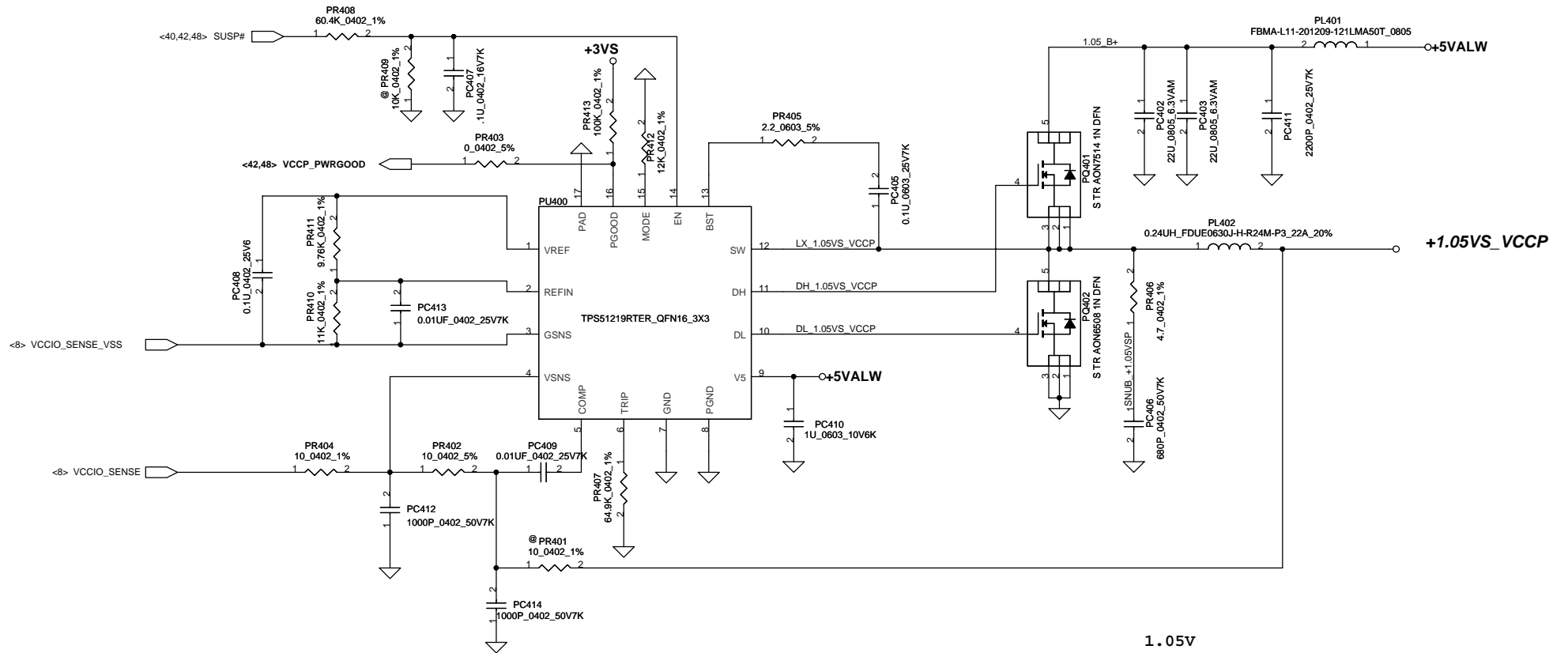
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	PWR-CHARGER
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				Rev	1.0
				Date:	Tuesday, October 16, 2012
				Sheet	44 of 53



Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	<b>PWR-3.3VALWP/SVALWP</b>	
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				Date:	Tuesday, October 16, 2012	Sheet



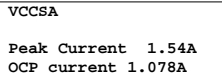




1.05V  
 Peak Current 14A  
 OCP current 15.08A  
 FSW=300kHz  
 Delta I=5.883A, Rippe=5.883x 4.5m=26.473Mv  
 DCR 3.7ohm +  
 TYP MAX  
 H/S Rds(on) :5.6mohm , 6.8mohm  
 L/S Rds(on) :3.7mohm , 5mohm

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	PWR-V1.05SP/16V
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				Date:	Tuesday, October 16, 2012
				Sheet	47 of 53

output voltage adjustable network



123

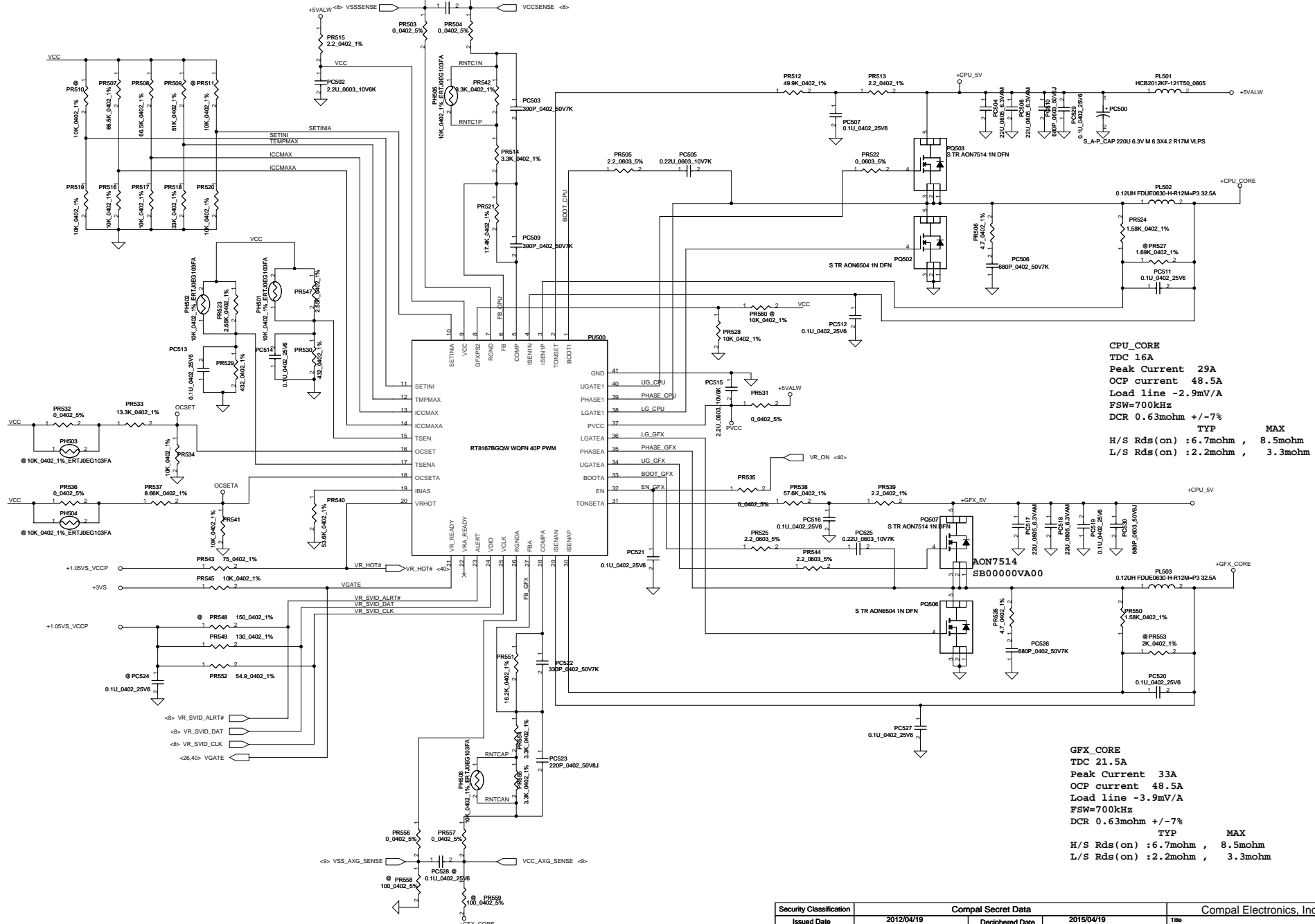
## PWR-VCCSAP/1.8VSF

PWR-VCC

VCUAA

# 1.0

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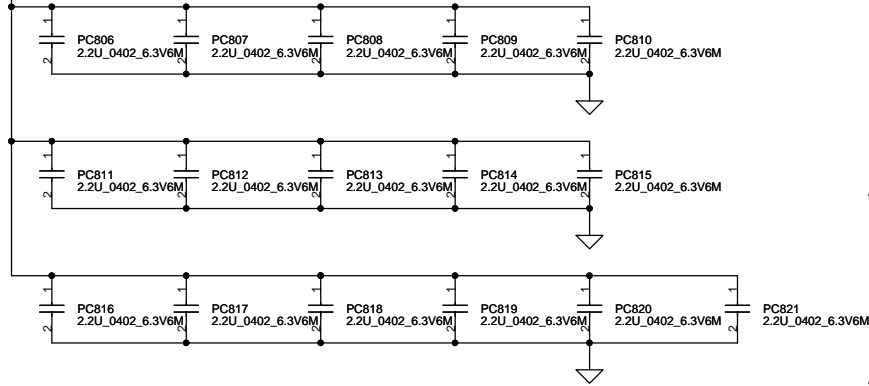


**CPU\_CORE**  
TDC 16A  
Peak Current 29A  
OCP current 48.5A  
Load line -2.9mV/A  
FSW=700kHz  
DCR 0.63mohm +/-7%  
TYP  
H/S Rds(on) : 6.7mohm , 8.5mohm  
L/S Rds(on) : 2.2mohm , 3.3mohm

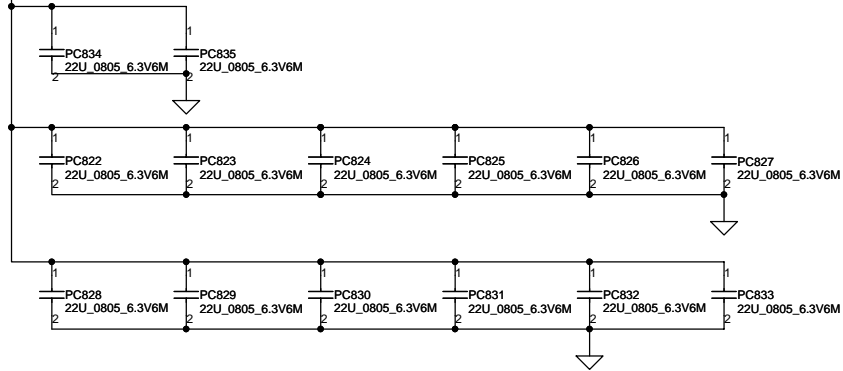
**GFX\_CORE**  
TDC 21.5A  
Peak Current 33A  
OCP current 48.5A  
Load line -3.9mV/A  
FSW=700kHz  
DCR 0.63mohm +/-7%  
TYP  
H/S Rds(on) : 6.7mohm , 8.5mohm  
L/S Rds(on) : 2.2mohm , 3.3mohm

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
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				LA-8551P
				Rev 1.0
				Date: Tuesday, October 16, 2012
				Sheet 49 of 53

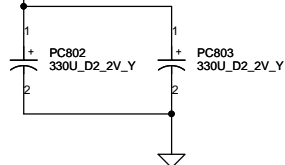
### +CPU\_CORE



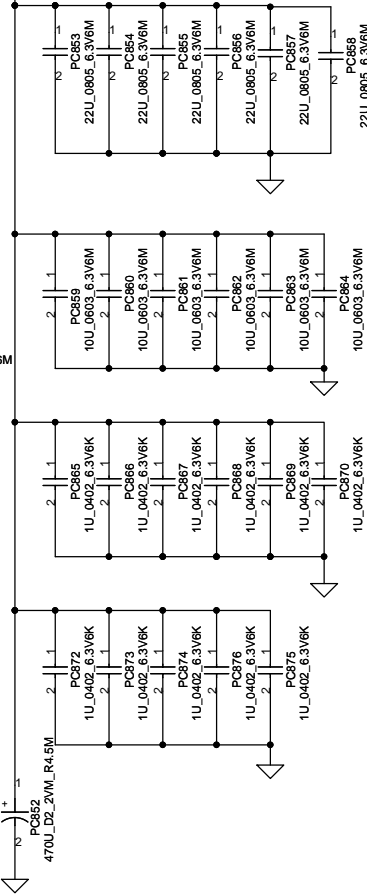
### +CPU\_CORE



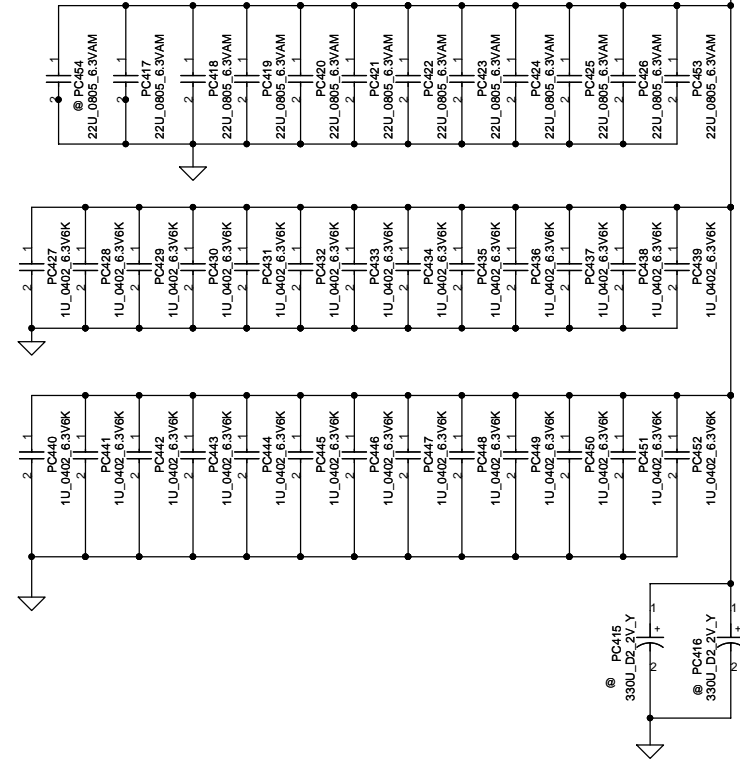
### +CPU\_CORE



### +GFX\_CORE



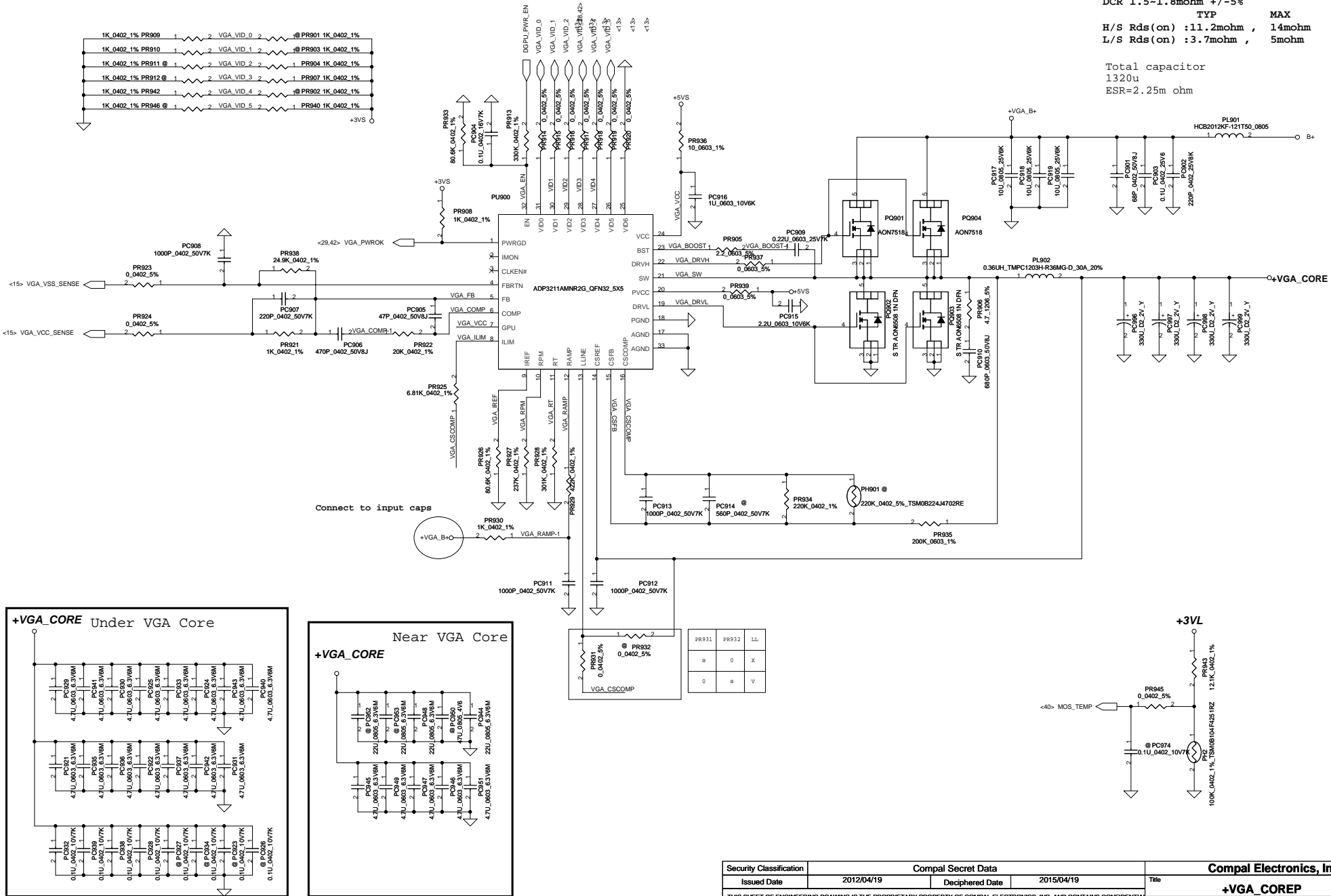
### +1.05V\_VCCP



Chief River ULV	330uF*9m	22uF	10uF	2.2uF	1uF
CPU	2	14		16	
GFX_CORE	1	6	6		11
1.05V_VCCP	2		11		26

VGA\_Core  
TDC 35A  
Peak Current 42A  
OCP current 65A  
Load line -  
FSW=300kHz  
DCR 1.5~1.8mohm +/-5%  
TYP MAX  
H/S Rds(on) :11.2mohm , 14mohm  
L/S Rds(on) :3.7mohm , 5mohm

Total capacitor  
1320u  
ESR=2.25m ohm



Item	Reason for change	PG#	Modify List	Date	Phase
1	HW command (Follow QFKAA)	45	change PR330 13K to 14K	2012/5/17	DVT
2	HW command (Follow QFKAA)	45	change PR351 20K to 19.1K	2012/5/17	DVT
4	fine tune 1.5V ocp =12.6A	46	change PR158 13.3K to 16.2K	2012/5/17	DVT
5	fine the 1.05V vout volatge=1.059V	47	change PR411 10.5K to 9.76K	2012/5/17	DVT
6	fine tune the CPU load line =2.7mV	49	change PR521 14.3K to 17.4K	2012/5/17	DVT
7	fine tune the GFX load line =3.7mV	49	change PR551 10.5K to 16.2K	2012/5/21	DVT
8	fine tune the GFX load line =3.7mV	49	change PC522 560P to 330P	2012/5/21	DVT
9	fine tune the GFX OCP setting	49	change PR537 13.3K to 8.66K	2012/5/21	DVT
10	purchaser command for cost down plane	48	change PU460 SY8037D to TPS51463	2012/5/22	DVT
11	for 1.05V high frequence change to remote sense	47	add PR402 reserve PR401	2012/5/24	DVT
12	for 1.05V high frequence	47	change PR412 100k to 12K	2012/5/24	DVT
13	change the same solution for 2nd sourced	44	change PQ203 TPCA8057 to AON6504	2012/5/24	DVT
14	change the same solution for 2nd sourced	44	change PR227 with the same PR211	2012/5/25	DVT
15	change the same solution for 2nd sourced	46	change PC157 with the same PC996	2012/5/25	DVT
16	fine tune 1.05V vout volatge=1.059V	47	change PR410 12K to 11K	2012/5/25	DVT
17	fine tune the CPU DCR sense	49	change PR538 49.9K to 57.6K	2012/5/25	DVT
18	fine tune the CPU DCR sense	49	change PR550 1.13K to 1.58K	2012/5/25	DVT
19	fine tune the 5V OCP=18A	45	change PR357 120K to 133K	2012/5/25	DVT
20	fine tune 3.3V OCP =10A	45	change PR337 120K to 200K	2012/5/25	DVT
21	for 1.05V high frequence	47	change PL402 0.47u to 0.24u	2012/5/25	DVT
22	for 1.05V high frequence	47	Reserve the PC415 and PC416	2012/5/25	DVT
23	change the 3v/5v IC version	45	change the PU330 RT8243B to RT8243A	2012/5/25	DVT
24	change 1.5V chokethe same part number with PL462	46	change the PL152 SH00000GJ00 to SH00000KS00	2012/5/25	DVT
25	change 1.05V high frequence OCP=16.5A	47	change the PR407 75K to 64.9K	2012/5/25	DVT
26	change charger current =3.46A	48	change the PR241 150 Kto 357K		
27	change the PF2 for design change	43	change the PF2 8A to 10A		

Security Classification	Compal Secret Data		Title	
Issued Date	2012/04/19	Deciphered Date	2015/04/19	PIR (PWR)
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			Date:	Tuesday, October 16, 2012
			Sheet	52 of 53
			Rev	1.0

HW PIR (Product Improve Record)

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VCUAA LA-9161P SCHEMATIC CHANGE LIST  
REVISION CHANGE: 0.3 TO 1.0

Item	Page	Date	Request	Solution
1)	24	2012/7/23A	Change RTCBATT power rail from GCLK to original design	DH1 mount always
2)	24	2012/7/23A	remove BIOS socket	UH3 mount always
3)	41	2012/7/23A	remove debug SW	Change SW2 to @
4)	38	2012/7/26A	EMI request	CA71,CA72,CA75,CA76 mount SE025102K80/1000pF
5)	41	2012/8/3A	Update JBLG footprint	Change JBLG footprint to E-T_7182K_F04N-00R_4P
6)	41	2012/8/3A	Update H20	Change H20 from 3P8 to 3P3 size
7)	05	2012/8/6C	remove JTAG for ESD request	remove T5, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17
8)	42	2012/8/6D	ESD request	mount C20,C21,C28,C30,C32,C33,C36,C37,C38,C39,C40; add C44 on SUSP
9)		2012/8/6D	Change footprint of 0ohm to Short_pad	Change location: LL2, R1, R16, R17, R388, RA17, RA18, RA28, RB1,RB32, RB34, RC119, RC183, RC73, RC88, RC92, RC94, RC95, RH128, RH208, RH213, RH214, RH221, RH242, RH244, RH246, RH247, RH249, RH25, RH286, RH311, RH312, RH314, RL433, RV182, RV80, RV81
10)	41	2012/8/6D	Change PCB PN	Change to DAZ0T700100
11)	34	2012/8/6D	EMI request	Change CM18 from 47pF to 680pF
12)	42	2012/8/6D	EMI request	Add C1(680pF) on +GFX_CORE, place close to CPU

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				Custom		1.0
				Date:	Tuesday, October 16, 2012	Sheet 53 of 53