

Schematics Page Index (Title / Revision / Change Date)

Page	Title of Schematics Page	Rev.	Page	Title of Schematics Page	Rev.	Page	Title of Schematics Page	Rev.
01	Schematics Page Index	SA	43	Express Card	SA	85	History(2)	SA
02	Block Diagram	SA	44	Mini-PCIE Card (WLAN)	SA	86	History(3)	SA
03	ARD (DMI,PEG,FDI)	SA	45	LAN (88E8057) 1/2	SA	87	History(4)	SA
04	ARD (CLK,MISC,JTAG)	SA	46	LAN (Transformer) 2/2	SA	88	History(5)	SA
05	ARD (DDR3)	SA	47	SATA HDD	SA	89	History(6)	SA
06	ARD (POWER)	SA	48	SATA CD-ROM	SA	90	History(7)	SA
07	ARD (GRAPHICS POWER)	SA	49	eSATA COMBO	SA	91	History(8)	SA
08	ARD (GND)	SA	50	PCIE (MS) 1/2	SA	92	History(9)	SA
09	ARD (RESERVED)	SA	51	PCIE (SD) 1/2	SA	93	History(10)	SA
10	PCH (HDA,JTAG,SAT)	SA	52	Camera Connector	SA			
11	PCH (PCI-E,SMBUS,CLK)	SA	53	Bluetooth Connector	SA			
12	PCH (DMI,FDI,GPIO)	SA	54	Felica Connector	SA			
13	PCH (LVDS,DDI)	SA	55	Status LED & LID	SA			
14	PCH (PCI,USB,NVRAM)	SA	56	FAN	SA			
15	PCH (GPIO,VSS NCTF,RSVD)	SA	57	Touch Pad	SA			
16	PCH (POWER) 1/2	SA	58	Thermal Sensor	SA			
17	PCH (POWER) 2/2	SA	59	Switch DB Conn.	SA			
18	PCH (VSS)	SA	60	AUDIO SPEAKER CONNECTOR	SA			
19	CLOCK GEN	SA	61	Audio/USB DB Conn.	SA			
20	DDRIII(SO-DIMM 0) 1/3	SA	62	Switch (Botton & KB LED)	SA			
21	DDRIII(SO-DIMM 1) 2/3	SA	63	Audio (CODEC)	SA			
22	VGA (PCI-E) 1/6	SA	64	Audio (MUTE)	SA			
23	VGA (Strap) 2/6	SA	65	Audio (Power)	SA			
24	VGA (I/O) 3/6	SA	66	Audio (Audio & USB Conn.)	SA			
25	VGA (Memory BUS) 4/6	SA	67	Audio (Head Phone Jack)	SA			
26	VGA (LVDS) 5/6	SA	68	Audio (Ext MIC Jack)	SA			
27	VGA (Power) 6/6	SA	69	Audio (USB Port)	SA			
28	VRAM(DDR3) # 1/4	SA	70	Power Design Diagram	SA			
29	VRAM(DDR3) # 2/4	SA	71	DCIN&Charger	SA			
30	VRAM(DDR3) # 3/4	SA	72	Discharge Circuit	SA			
31	VRAM(DDR3) # 4/4	SA	73	Identify IC	SA			
32	VRAM(BYPASS) 1/2	SA	74	SYS Power (+3 3V/+5V)	SA			
33	VRAM(BYPASS) 2/2	SA	75	VTT&PCH Power(+1 1/1 05V)	SA			
34	CRT	SA	76	DDR3 Power(+1 5V/+0 75V)	SA			
35	LVDS	SA	77	SYS Power(+1 8V)	SA			
36	Inverter CONNECTOR	SA	78	CPU Power VHCORE	SA			
37	LVDS CONNECTOR	SA	79	CPU Power VID	SA			
38	HDMI	SA	80	VGA Power(ATI VDD)	SA			
39	EC+KBC (NPCE783L)	SA	81	Others power plane	SA			
40	KB Connector	SA	82	OVP protection	SA			
41	SPI Flash ROM	SA	83	HOLE & AMI LABEL	SA			
42	Debug Port	SA	84	History(1)	SA			

Project Code & Schematics Subject: M960&M970 H Model

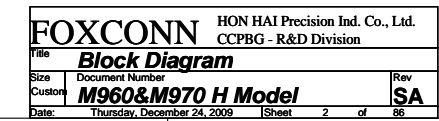
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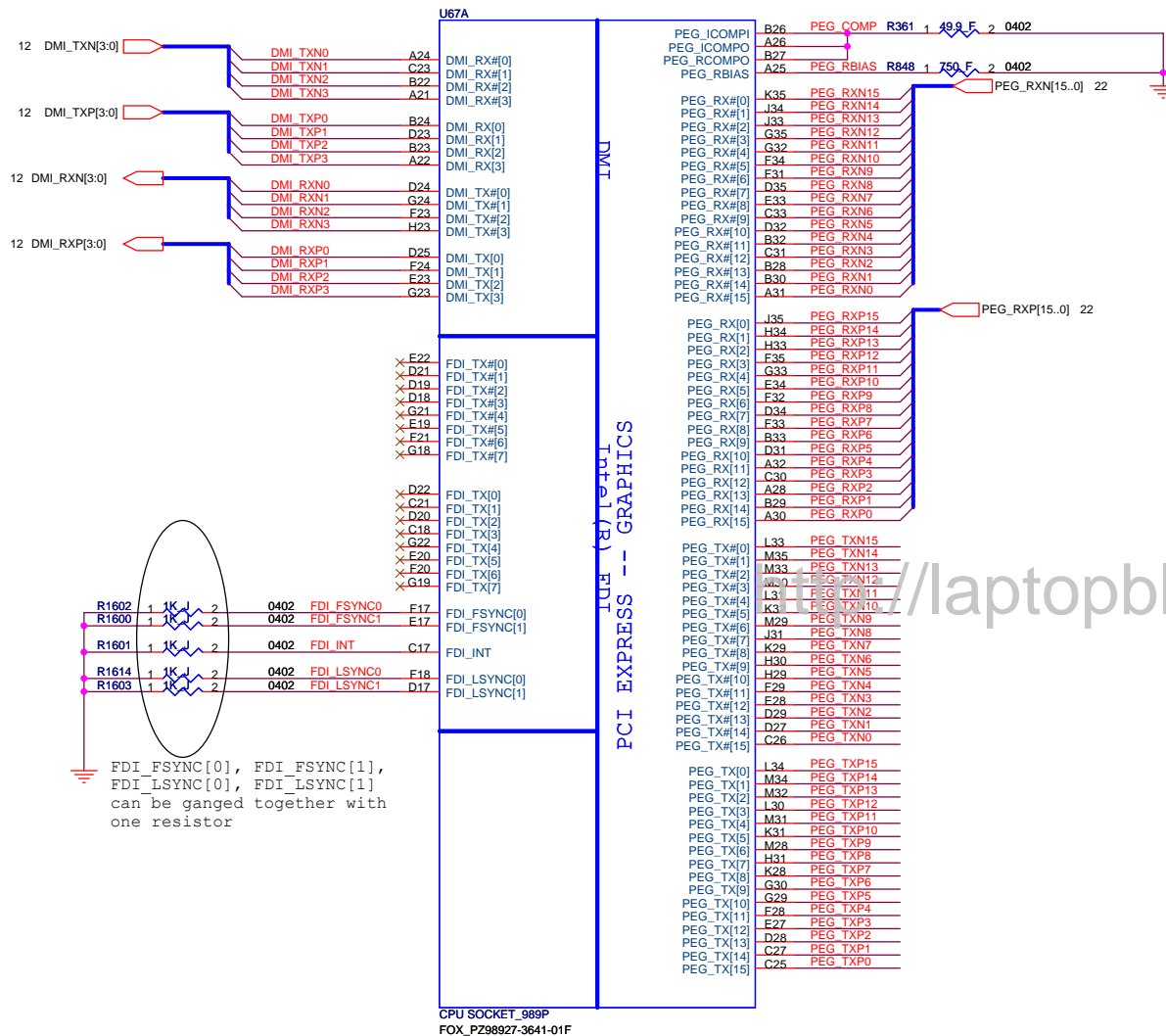
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 1P-1099J00-80SB (IRIS AUDIO)
 1P-1099J01-80SB (IRIS PWR)
 1P-0099500-80SB (HANNSTAR MB)
 1P-1099500-80SB (HANNSTAR Audio)
 1P-1099501-80SB (HANNSTAR PWR)

P. Leader	Check by	Design by

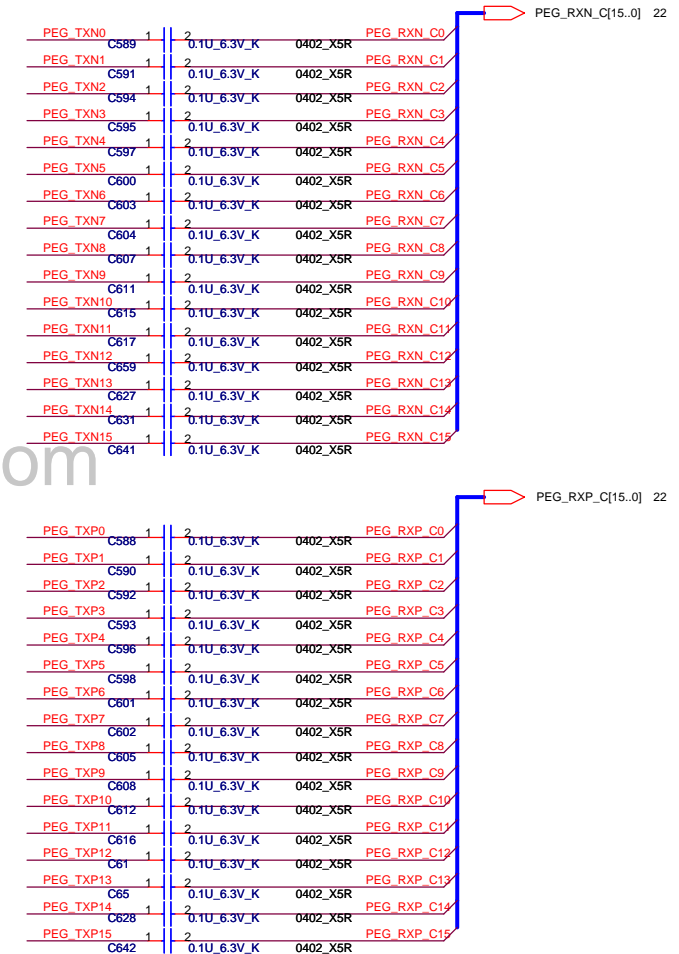
FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Index Page			
Size A3	Document Number M960&M970 H Model		Rev SA
Date: Thursday, December 24, 2009	Sheet 1	of 86	

Calpella Platform+ AMD Madison/P





If PCIe Graphics is not implemented, the TX/RX pairs can be left as No Connect.



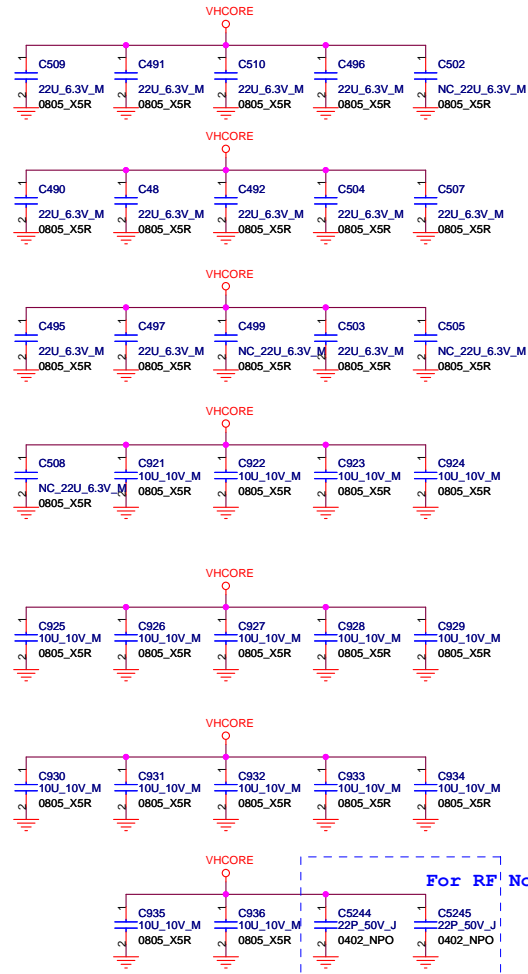
For Disable Arrandale Graphic

In addition, FDI_RXN[7:0] and FDI_RXP[7:0] can be left floating on the PCH. FDI_TX[7:0] and FDI_TX# [7:0] can be left floating on the Arrandale. The GFX_IMON, FDI_FSYN[0], FDI_FSYN[1], FDI_LSYN[0], FDI_LSYN[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors). FDI_FSYN[0], FDI_FSYN[1], FDI_LSYN[0], FDI_LSYN[1] can be ganged together with one resistor.



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48A (SV)



For RF Noise

VH CORE

CPU SOCKET_989P
FOX_PZ98927-3641-01F

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

VTT0_1
VTT0_2
VTT0_3
VTT0_4
VTT0_5
VTT0_6
VTT0_7
VTT0_8
VTT0_9
VTT0_10
VTT0_11
VTT0_12
VTT0_13
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VTT0_25
VTT0_26
VTT0_27
VTT0_28
VTT0_29
VTT0_30
VTT0_31
VTT0_32

VTT0_33
VTT0_34
VTT0_35
VTT0_36
VTT0_37
VTT0_38
VTT0_39
VTT0_40
VTT0_41
VTT0_42
VTT0_43
VTT0_44

```

PSI#
VID[0]
VID[1]
VID[2]
VID[3]
VID[4]
VID[5]
VID[6]
DPRSLPVR
TT_SELECT

```

```

ISENSE
CC_SENSE
SS_SENSE

VTT_SENSE
SENSE_VTT

```

18A (SV) (VTT)

EVT

+1_05V_VTT

+1_05V_VTT

18A (SV) (VTT)

EVT

+1_05V_VTT

+1_05V_VTT

MP

CORE

F

—

1

F

2

5

1

1

1

2

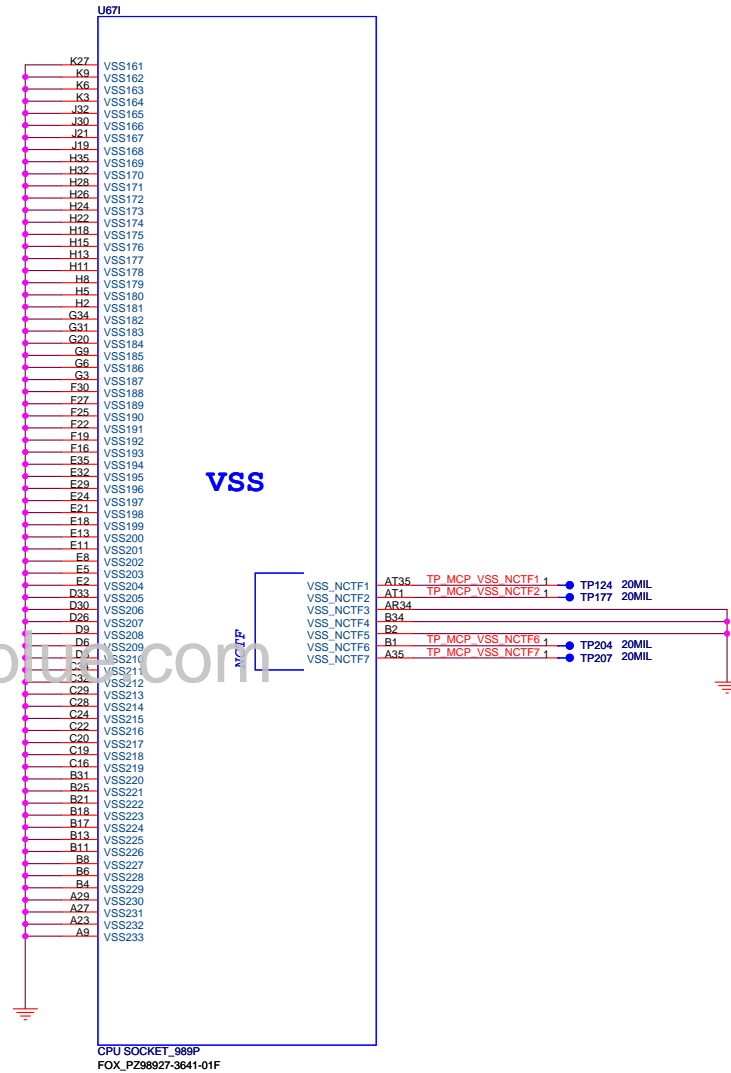
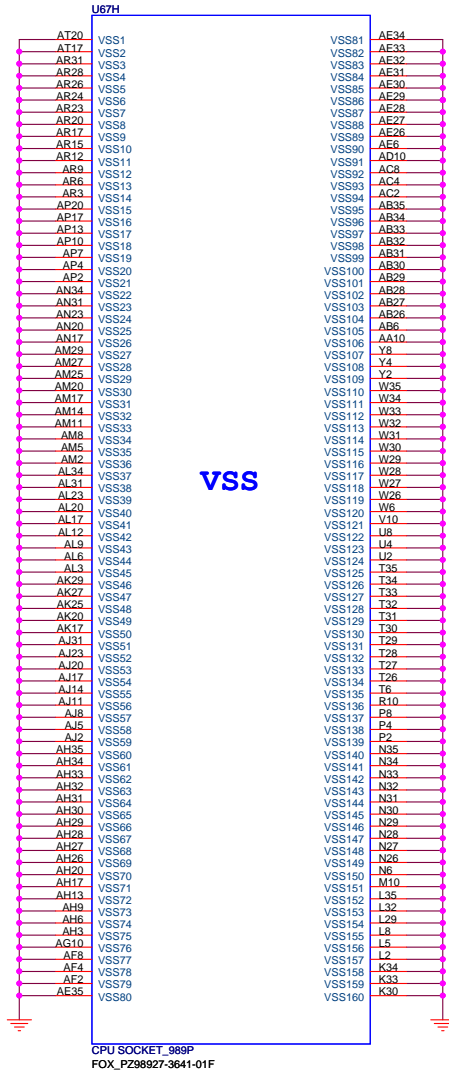
FOXCONN

Title **ARD (POWER)**

Size	Document Number
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Date:	Tuesday, December 29, 2009	Sheet	6	of	86
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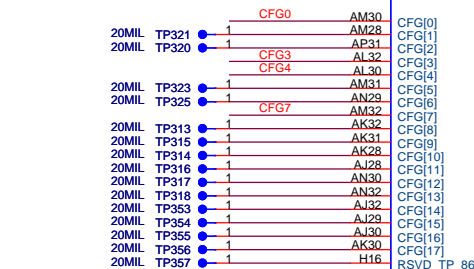


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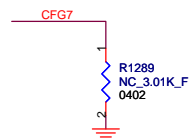
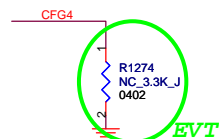
The diagram shows the pinout for the U67E component. The pins are arranged in a 2x14 grid. The top row of pins is labeled 1 through 14, and the bottom row is labeled 15 through 28. The test points are labeled as follows:

Pin	Test Point	Test Point Name
1	TP305	AP25
2	TP307	AL25
3	TP306	AL24
4	TP308	AL22
5	TP310	AJ33
6	TP309	AG9
7	TP311	M27
8	TP312	L28
9	TP1220	J17
10	TP1221	H17
11	TP300	G25
12	TP302	G17
13	TP303	E31
14	TP304	E30

The diagram also shows the connections for the EVT and DVT test points. The EVT test point is connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, and 14. The DVT test point is connected to pins 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, and 28.



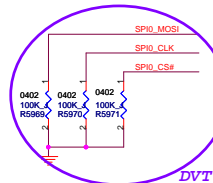
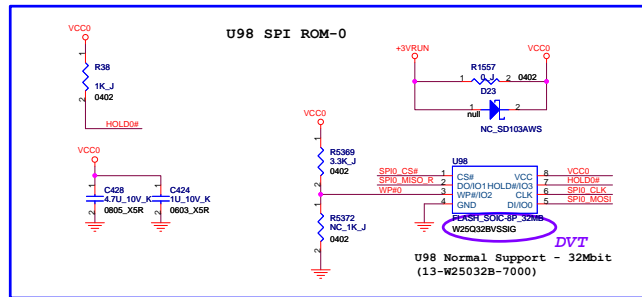
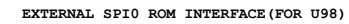
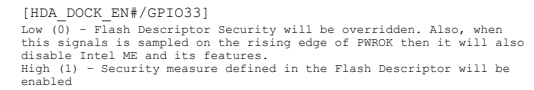
A circuit diagram showing a resistor labeled R1273 with a value of 3.01K_F and a 0402 package. The resistor is connected between a pin labeled CFG3 and a ground symbol.



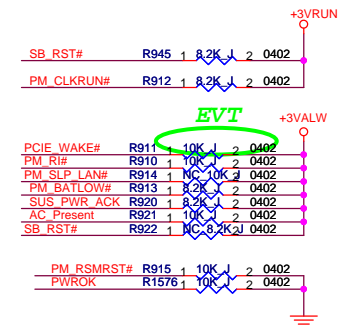
Intel has determined that the workaround (3.01K pull down to Vss on signal CFG[7]) is not robust. Intel recommends not implementing this workaround at this time (CFG[7] should not be pulled down). Intel recommends not to test for PCI-E Express 2.0 Jitter specification compliance for the affected steppings.

VSS (AP34) can be left NC is
CRB implementation; EDS/DG
recommendation to GND

The traces inside this block should be wider.

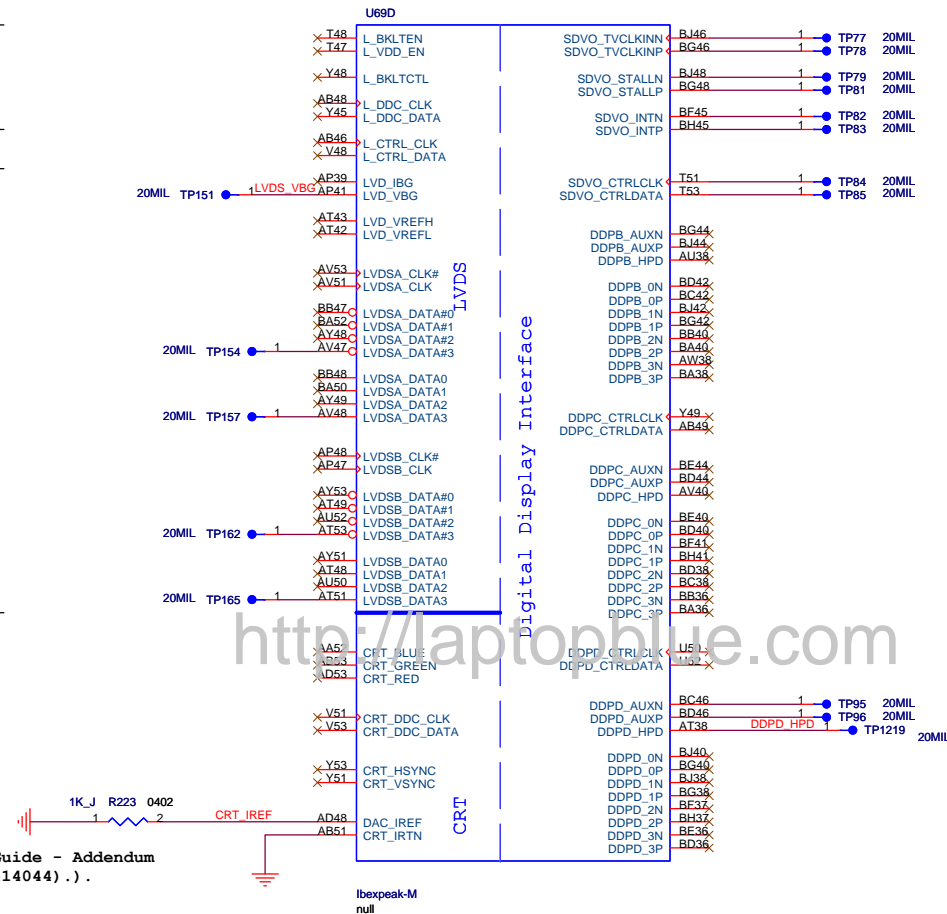


For Disable Arrandale Graphic
In addition, FDI_RXN[7:0] and FDI_RXP[7:0] can be left floating on the PCH.
FDI_TX[7:0] and FDI_TX# [7:0] can be left floating on the Arrandale. The
GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT
signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

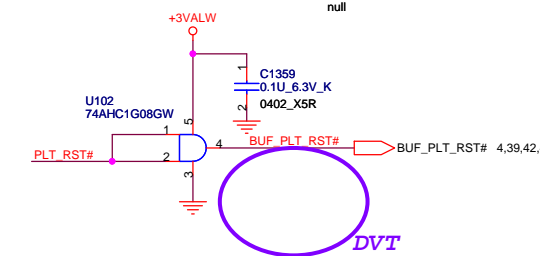
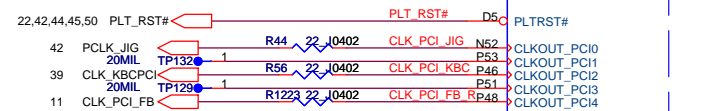
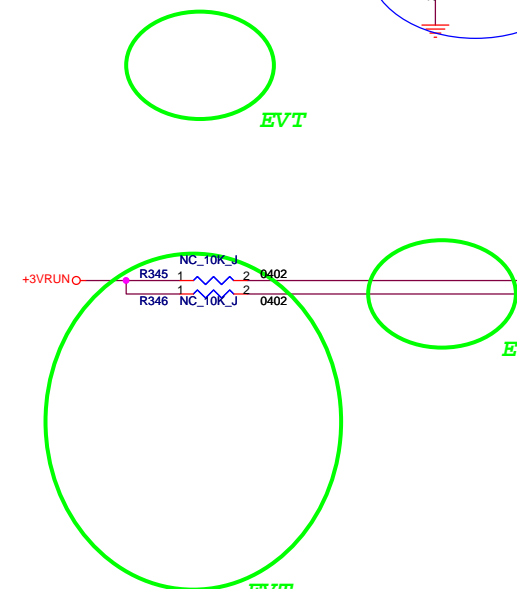
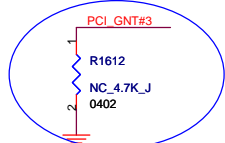
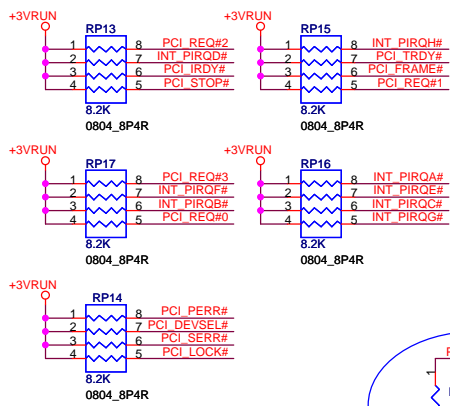


NC for disable LVDS

NC for disable LVDS



Calpella Platform - Design Guide - Addendum
/ Update - Rev. 1.52 (Doc #414044).).



20MIL	TP182	1	H40
20MIL	TP167	1	N34
20MIL	TP186	1	C44
20MIL	TP194	1	A38
20MIL	TP187	1	C36
20MIL	TP199	1	J34
20MIL	TP201	1	A40
20MIL	TP200	1	D45
20MIL	TP202	1	E36
20MIL	TP319	1	H48
20MIL	TP227	1	E40
20MIL	TP322	1	M48
20MIL	TP363	1	I43
20MIL	TP324	1	M45
20MIL	TP426	1	F53
20MIL	TP428	1	M40
20MIL	TP427	1	M43
20MIL	TP429	1	J36
20MIL	TP431	1	K48
20MIL	TP430	1	F40
20MIL	TP432	1	C42
20MIL	TP434	1	K46
20MIL	TP433	1	M51
20MIL	TP435	1	J52
20MIL	TP437	1	L34
20MIL	TP436	1	K51
20MIL	TP438	1	F42
20MIL	TP440	1	J40
20MIL	TP439	1	G46
20MIL	TP441	1	F44
20MIL	TP443	1	M47
20MIL	TP442	1	H36

20MIL	TP446	1	J50
20MIL	TP445	1	G42
20MIL	TP447	1	H47
20MIL	TP444	1	G34

INT_PIRQA#	G38
INT_PIRQB#	H51
INT_PIRQC#	B37
INT_PIRQD#	A44
PCI_REQ#0	F51
PCI_REQ#1	A46
PCI_REQ#2	B45
PCI_REQ#3	M53
PCI_GNT#0	F48
PCI_GNT#1	K45
PCI_GNT#2	F36
PCI_GNT#3	H53

INT_PIRQ#	E41
INT_PIRQF#	K33
INT_PIRQG#	A36
INT_PIRQH#	A48
PCI_RST#	K6
PCI_SERR#	E44
PCI_PERR#	E50
PCI_IRDY#	A42
PCI_PAR#	H44
PCI_DEVSEL#	F46
PCI_FRAME#	C46
PCI_LOCK#	D49

PCI_STOP#	D41
PCI_TRDY#	C48
PME#_ICH	M7
PLT_RST#	D5
CLKOUT_PCIO	N52
CLKOUT_PC1	P53
CLKOUT_PC2	P46
CLKOUT_PC3	P51
CLKOUT_PC4	P48

U69E	AD0	NV_CE#0
U69E	AD1	NV_CE#1
U69E	AD2	NV_CE#2
U69E	AD3	NV_CE#3
U69E	AD4	NV_DQS0
U69E	AD5	NV_DQS1
U69E	AD6	NV_DQ0 / NV_I00
U69E	AD7	NV_DQ1 / NV_I01
U69E	AD8	NV_DQ2 / NV_I02
U69E	AD9	NV_DQ3 / NV_I03
U69E	AD10	NV_DQ4 / NV_I04
U69E	AD11	NV_DQ5 / NV_I05
U69E	AD12	NV_DQ6 / NV_I06
U69E	AD13	NV_DQ7 / NV_I07
U69E	AD14	NV_DQ8 / NV_I08
U69E	AD15	NV_DQ9 / NV_I09
U69E	AD16	NV_DQ10 / NV_I10
U69E	AD17	NV_DQ11 / NV_I11
U69E	AD18	NV_DQ12 / NV_I12
U69E	AD19	NV_DQ13 / NV_I13
U69E	AD20	NV_DQ14 / NV_I14
U69E	AD21	NV_DQ15 / NV_I15

C/BE0#	J50
C/BE1#	G42
C/BE2#	H47
C/BE3#	G34

PIRQA#	G38
PIRQB#	H51
PIRQC#	B37
PIRQD#	A44
REQ0#	F51
REQ1# / GPIO50	A46
REQ2# / GPIO52	B45
REQ3# / GPIO54	M53

GNT0#	F48
GNT1# / GPIO51	K45
GNT2# / GPIO53	F36
GNT3# / GPIO55	H53

PRO# / GPIO2	E41
PRO# / GPIO3	K33
PIRQ# / GPIO4	A36
PIRQH# / GPIO5	A48

PCI_RST#	K6
SERR#	E44
PERR#	E50
IRDY#	A42
PAR#	H44
FRAME#	C46
LOCK#	D49
STOP#	D41
TRDY#	C48
PME#	M7
PLTRST#	D5

CLKOUT_PCIO	N52
CLKOUT_PC1	P53
CLKOUT_PC2	P46
CLKOUT_PC3	P51
CLKOUT_PC4	P48

NV_CE#0	BD
NV_CE#1	BD
NV_CE#2	BD
NV_CE#3	BD
NV_DQS0	BD
NV_DQS1	BD
NV_DQ0 / NV_I00	BD
NV_DQ1 / NV_I01	BD
NV_DQ2 / NV_I02	BD
NV_DQ3 / NV_I03	BD
NV_DQ4 / NV_I04	BD
NV_DQ5 / NV_I05	BD
NV_DQ6 / NV_I06	BD
NV_DQ7 / NV_I07	BD
NV_DQ8 / NV_I08	BD
NV_DQ9 / NV_I09	BD
NV_DQ10 / NV_I10	BD
NV_DQ11 / NV_I11	BD
NV_DQ12 / NV_I12	BD
NV_DQ13 / NV_I13	BD
NV_DQ14 / NV_I14	BD
NV_DQ15 / NV_I15	BD

NV_ALE	BD
NV_CLE	BD
NV_RCOMP	BD
NV_RB#	BD
NV_WR#0_RE#	BD
NV_WR#1_RE#	BD
NV_WE#_CK0	BD
NV_WE#_CK1	BD

USB_PN0	H18
USB_PP0	J18
USB_PN1	A18
USB_PP1	C18
USB_PN2	N20
USB_PP2	P20
USB_PN3	J20
USB_PP3	L20
USB_PN4	F20
USB_PP4	G20
USB_PN5	A20
USB_PP5	C20
USB_PN6	M2
USB_PP6	J2
USB_PN7	E2
USB_PP7	S2
USB_PN8	J22
USB_PP8	E22
USB_PN9	F22
USB_PP9	A22
USB_PN10	C22
USB_PP10	G24
USB_PN11	J24
USB_PP11	L24
USB_PN12	M24
USB_PP12	A24
USB_PN13	C24
USB_PP13	E24

USB_OC#0	N16
USB_OC#1	J16
USB_OC#2	E16
USB_OC#3	L16
USB_OC#4	E14
USB_OC#5	G16
USB_OC#6	F12
USB_OC#7	I15

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USB_PP1	61
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USB_PP2	43
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USB_PP3	43
USB_PN4	61
USB_PP4	61
USB_PN5	61
USB_PP5	61
USB_PN6	52
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USB_OC#7	61

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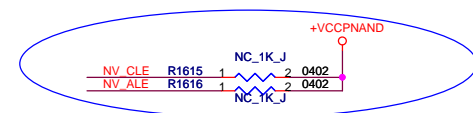
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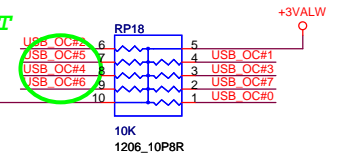
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AY18	BD
AY19	BD
AY20	BD
AY21	BD
AY22	BD
AY23	BD
AY24	BD
AY25	BD
AY26	BD
AY27	BD
AY28	BD
AY29	BD
AY30	BD
AY31	BD

DMI Termination Voltage	
NV_CLE	Set to Vss when LOW
NV_CLE	Set to Vcc when HIGH

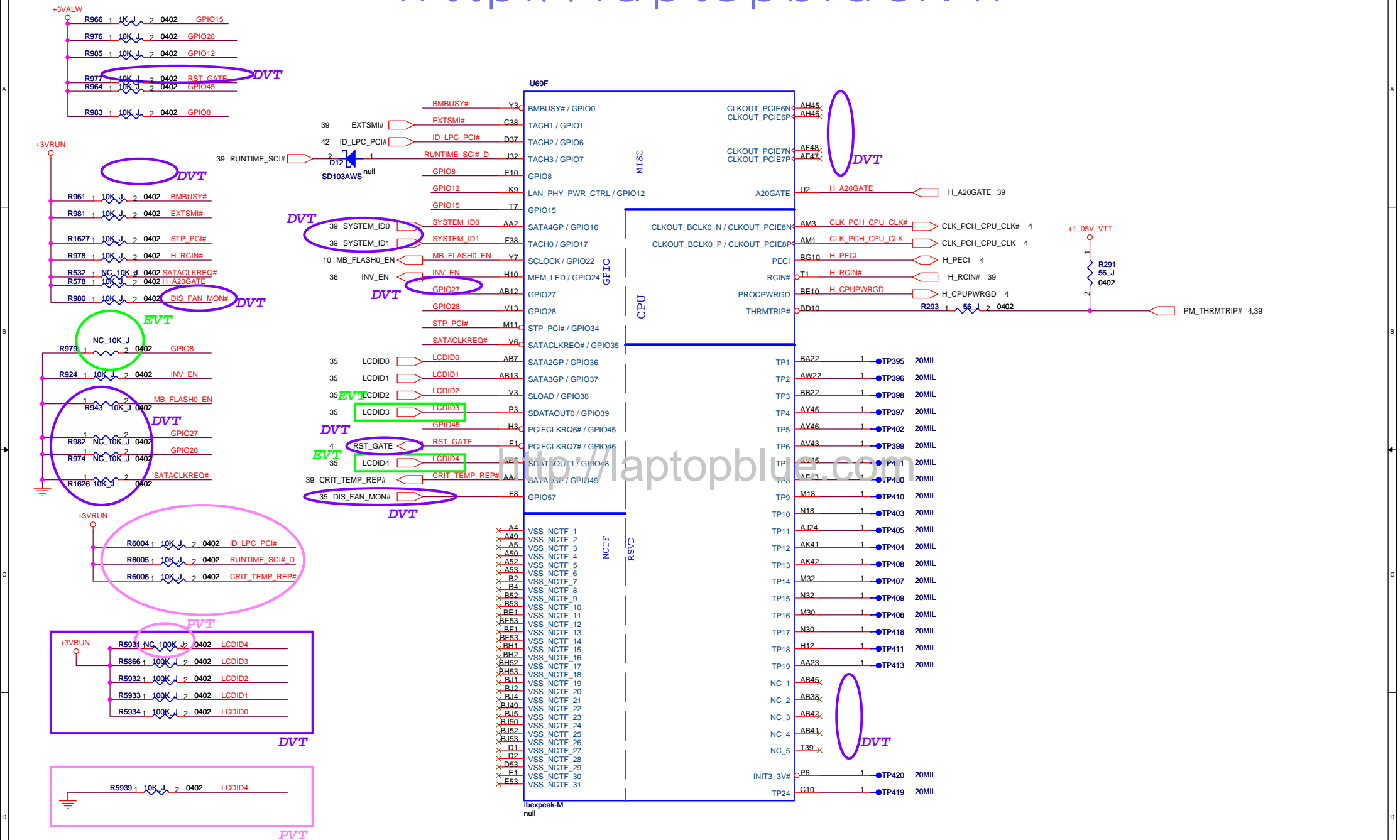


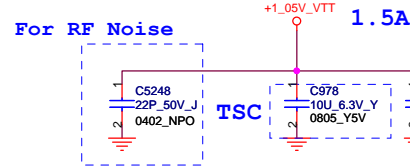
Danbury Technology
Disabled when Low
Enabled when High

USB PORT	Function
PORT-0	eSATA
PORT-1	External Port-2
PORT-2	
PORT-3	ExpressCard/34 (USB)
PORT-4	External Port-3
PORT-5	External Port-1
PORT-6	
PORT-7	
PORT-8	
PORT-9	Camera
PORT-10	
PORT-11	Felica
PORT-12	WLAN
PORT-13	Bluetooth



Buffer to reduce loading on PLT_RST#.

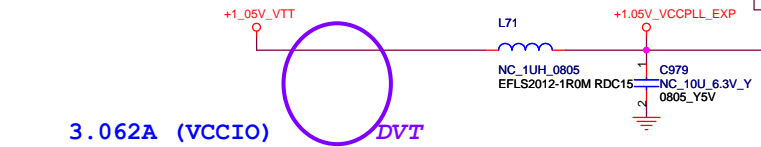




3.062A (VCCIO)

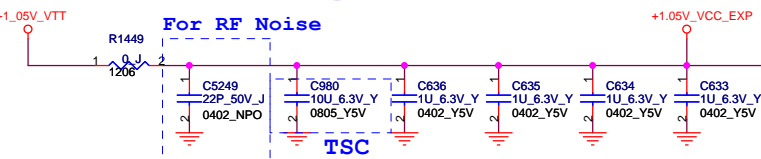
Default is use Internal VRM

For Disable Arrandale Graphic
GPIO27 floating as Internal VRM and there is no need external supply



3.062A (VCCIO)

For RF Noise

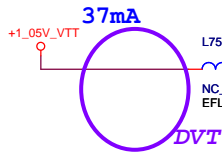


TSC

357mA

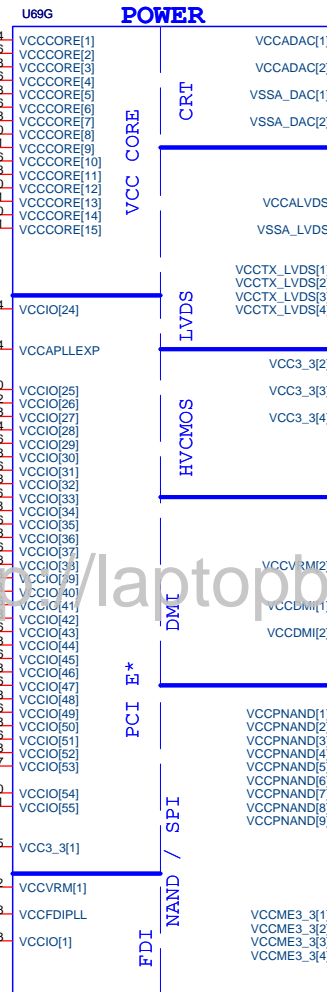
200mA

37mA



Default is use Internal VRM

For Disable Arrandale Graphic
GPIO27 floating as Internal VRM and there is no need external supply



VCCALVDS, VCCTX_LVDS to GND
VSSA_LVDS NC
For disable LVDS

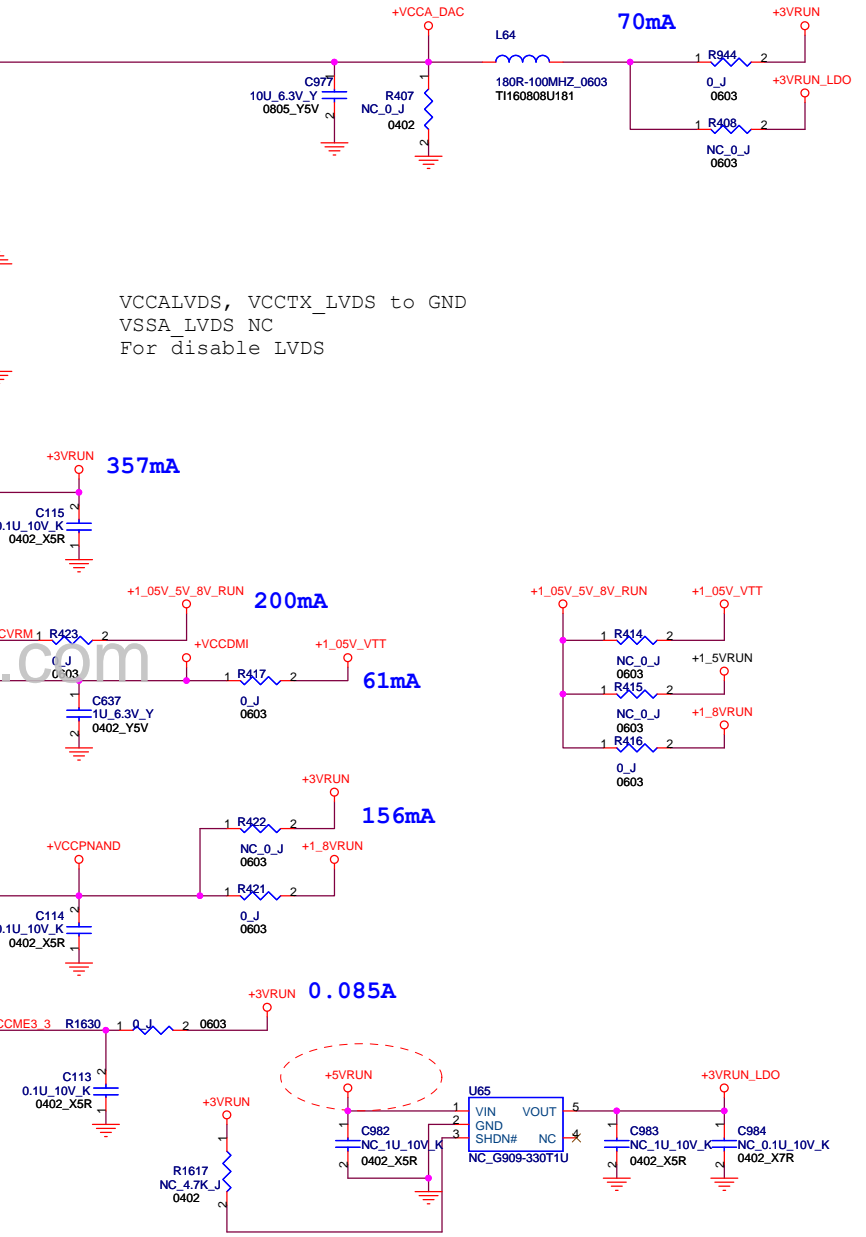
357mA

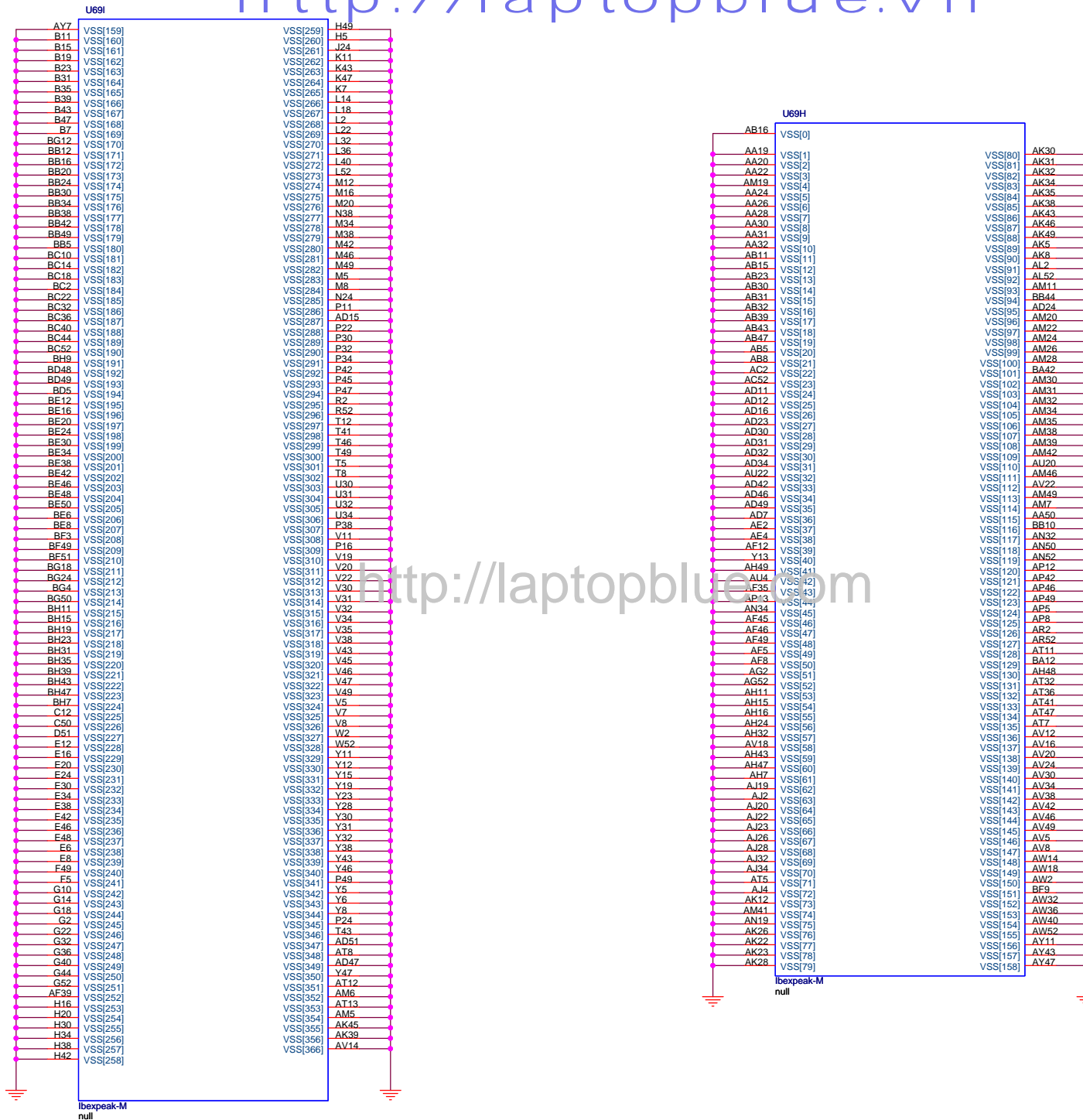
200mA

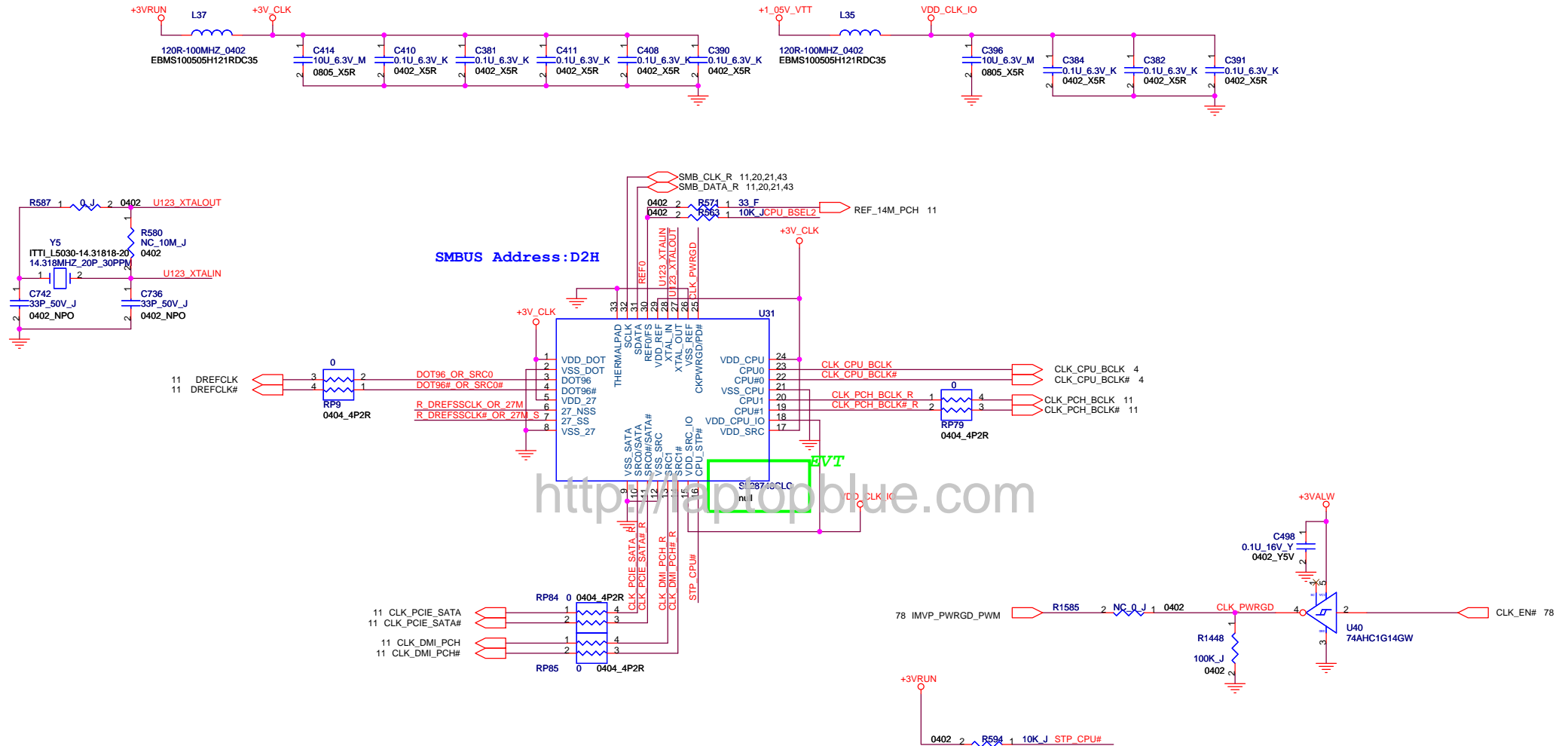
61mA

156mA

0.085A

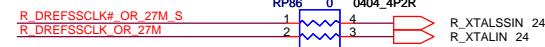
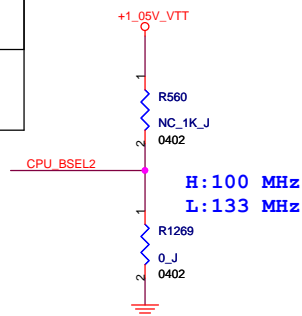






Frequency Select Pin (FS)

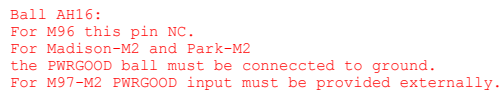
FS	CPU	Power On	SRC	SATA	DOT96	27MHz	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						



09/11/17 R_XTALSSIN be Connect a stable clock source (from clock gen SS 27MHz) to GPIO26_TCK.







EVT

EVT

Strap for DDR3 VRAM
ATI_DVDPDATA[3 : 0]

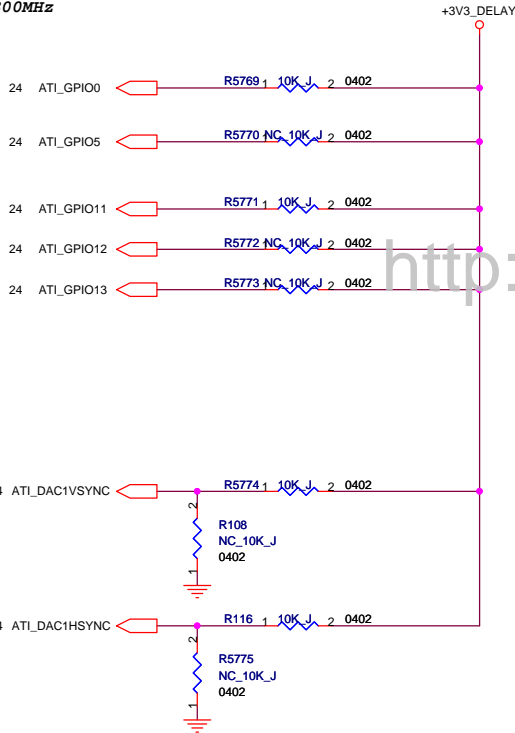
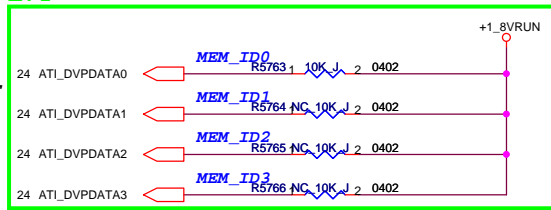
For M960/M970 M92-M2 XTX / Park-XT
0001 64Mx16 Reserve x4pcs
0010 64Mx16 Hynix * x4pcs
0011 64Mx16 Samsung** x4pcs
0101 64Mx16 Reserve x4pcs
0110 64Mx16 Elpida*** x4pcs
0111 64Mx16 AMD**** x4pcs

For M960/M970 Madsion-LP
0001 64Mx16 Reserve x8pcs
0010 64Mx16 Hynix * x8pcs
0011 64Mx16 Samsung** x8pcs
0101 64Mx16 Reserve x8pcs
0110 64Mx16 Elpida*** x8pcs
0111 64Mx16 AMD**** x8pcs
P.S. * means Hynix H5TQ1G63BFR-12C,800MHz
**means Samsung K4W1G1646E-HC12T00,800MHz
***means Elpida EDJ1116DBSE-DJ-F,1333MHz
****means AMD 23EY2387MA-12,800MHz

If no ROM attached, GPIO[13:12:11]
CONFIG{2:0}
controls the memory aperture size.
64MB 010
128MB 000
256MB 001
512MB 001

1 Enable HD Audio
0 Disable HD Audio

1 Enable HDMI
0 Disable HDMI

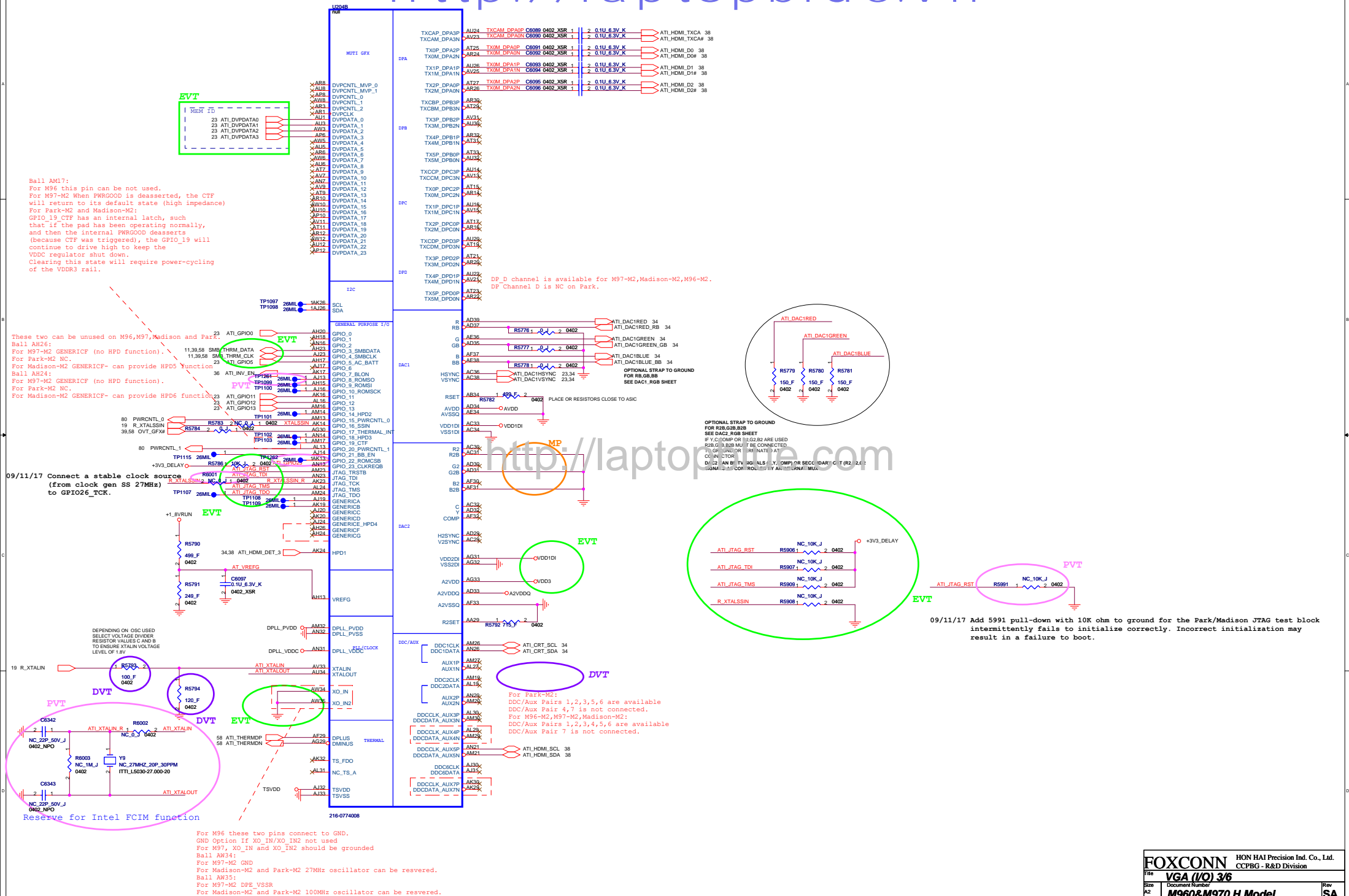


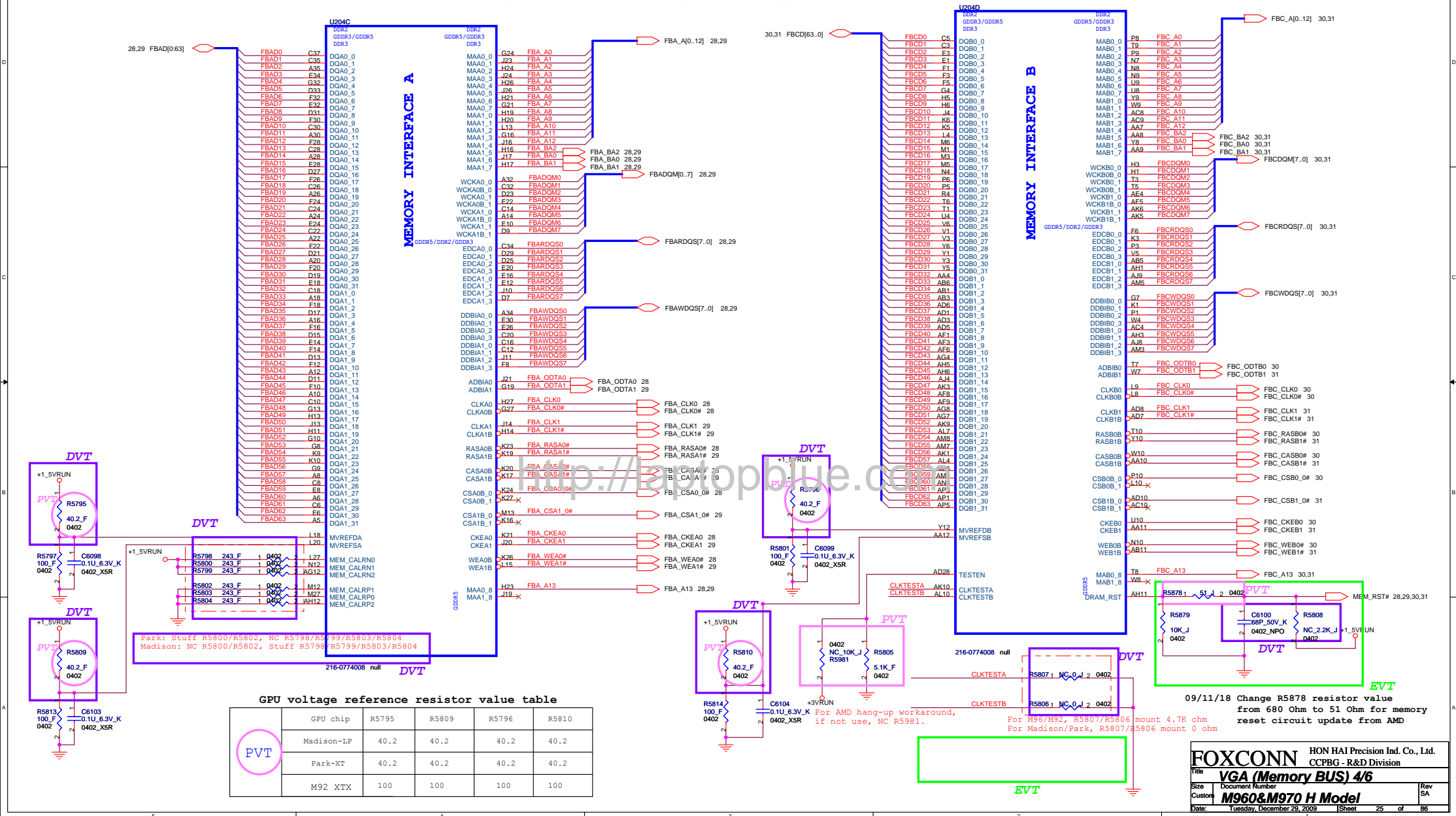
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED,
THEY MUST NOT CONFLICT DURING RESET

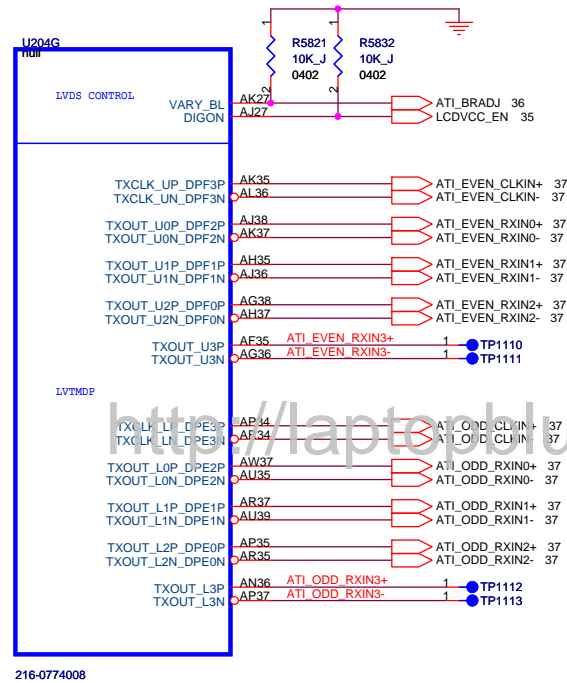
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN name	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO_0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	
TX_DEEMPH_EN	GPIO_1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	
AC_BATT	GPIO_5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
PWRCNTL_0 PWRCNTL_1	GPIO_6 GPIO_15 GPIO_20	Power Control signals control the core voltage regulator. At Reset, these signals will be inputs with weak internal pull-down resistors. VBios can define these signals to be either 3.3-V outputs or open drain outputs. The output state (high/low) of these signals is programmable for each PowerPlay state.	
BB_EN	GPIO_21	Back Bias (BB) control: When GPIO_21_BB_EN = 0 V, then back bias is disabled on the PCB (i.e. BPP = VDDC). When GPIO_21_BB_EN = 3.3 V, then back bias is enabled on the PCB (i.e. BPP = VDDC + Offset). Can function as a GPIO if not required for BB control.	
BLON	GPIO_7	Controls Backlight On/Off. Active high. If not needed as the backlight enable signal, it can alternatively be used as a GPIO or an open drain type output. Note: External pull-down recommended	
VGA_DIS	GPIO_9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	
CONFIG[0] CONFIG[1] CONFIG[2]	GPIO_11 GPIO_12 GPIO_13	If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	
BIOS_ROM_EN	GPIO_22	Enable external BIOS ROM device 0: Disable external BIOS ROM device 1: Enable external BIOS ROM device	
SSIN	GPIO_16	Spread Spectrum clock input for memory clock and/or engine clock (maximum down spread of -2.5%). Requires a spread version of 27 MHz(The modulation rate is 30-50 KHz.)	
THERMAL_INT	GPIO_17	Thermal monitor interrupt Can be set as either: 1) An input from an external temperature sensor (ALERTb) , or 2) An output signaling that the ASIC temp (measured by the internal sensor) is above the high threshold or below the low threshold.Output can be open drain or 3.3-V output.(active low by default)	
CLKREQB	GPIO_23	Reserve	

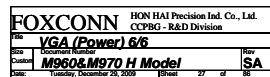


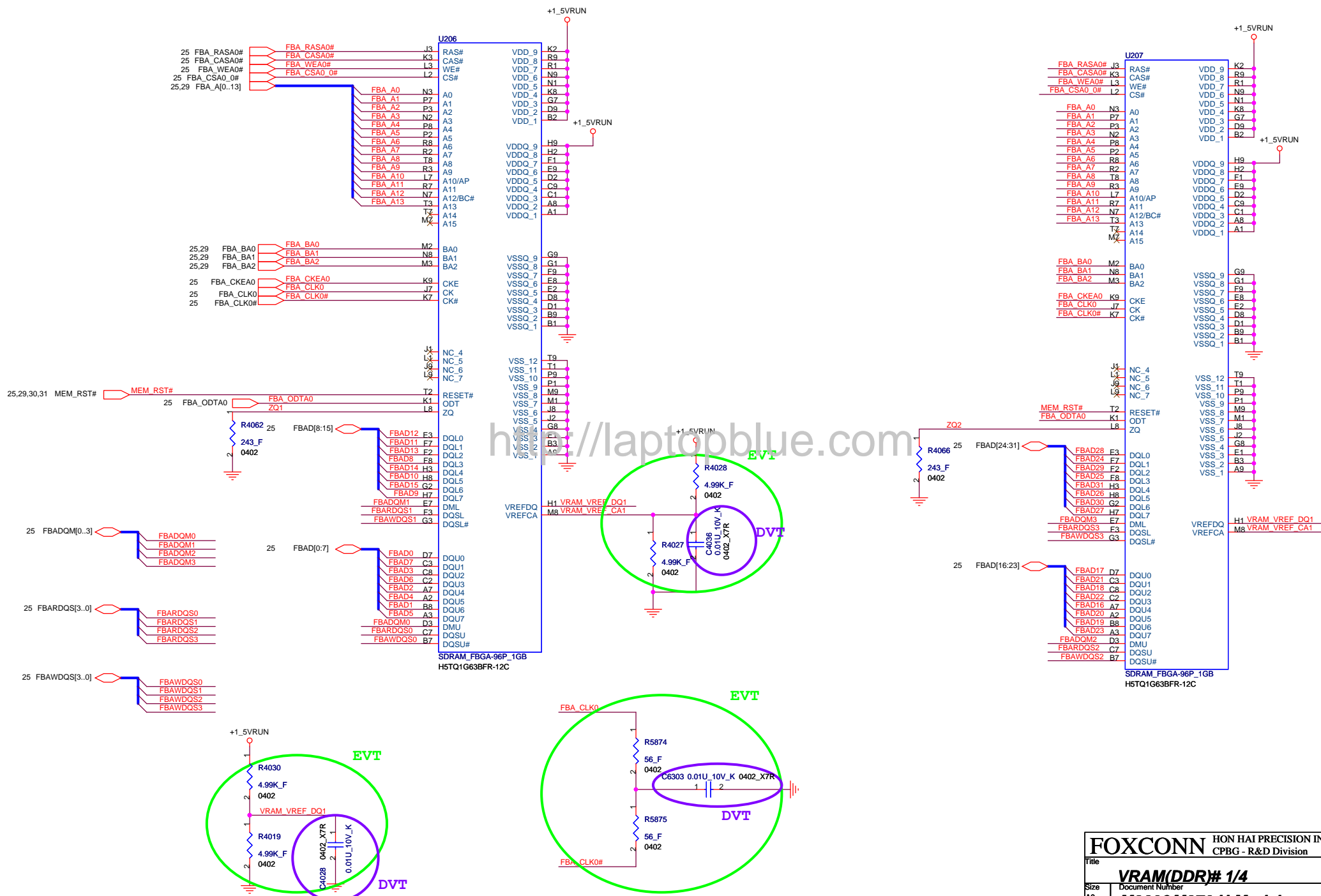


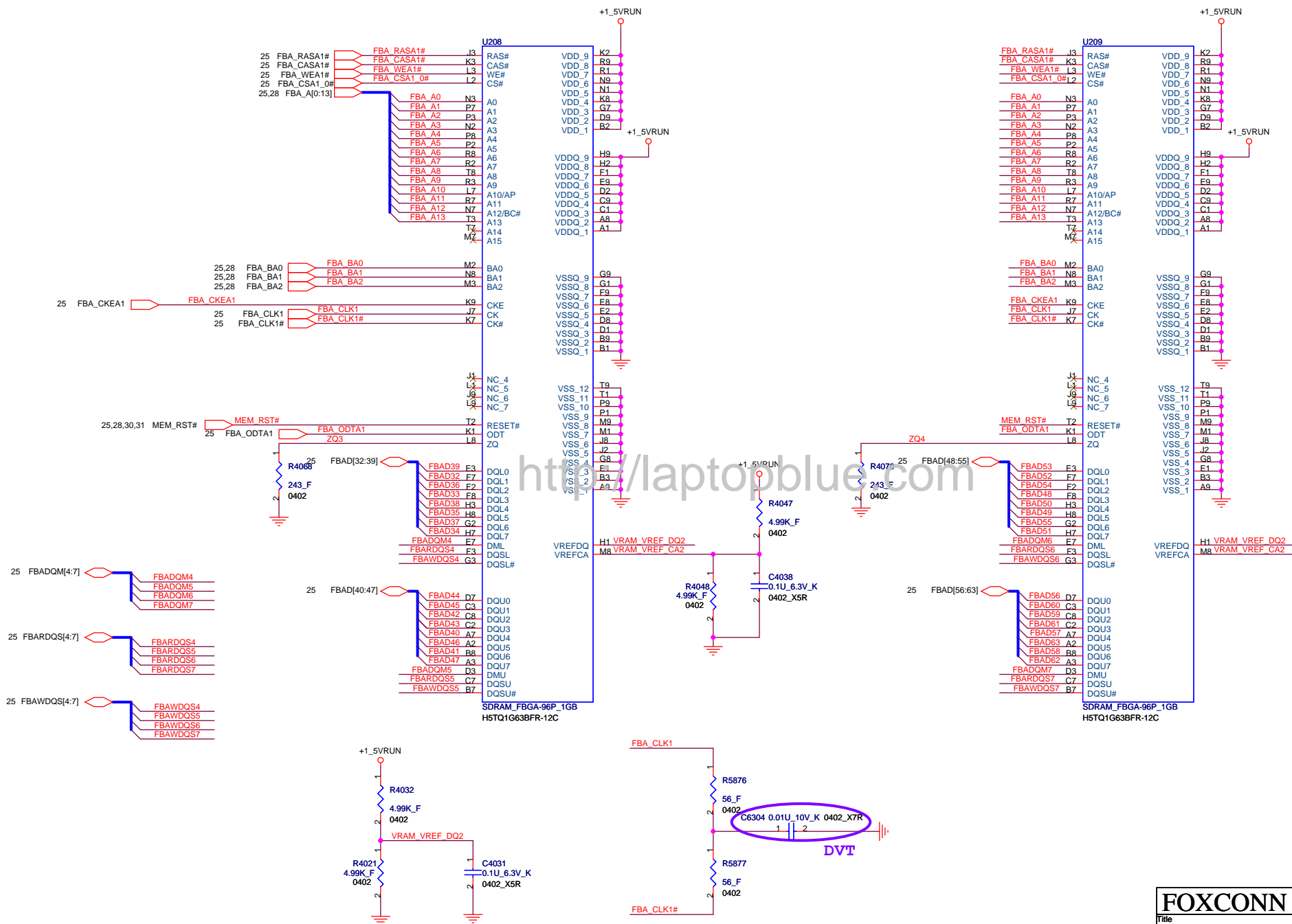
http://laptopblue.vn

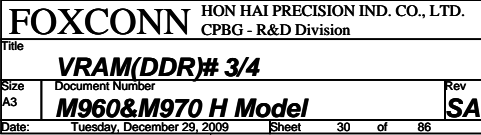


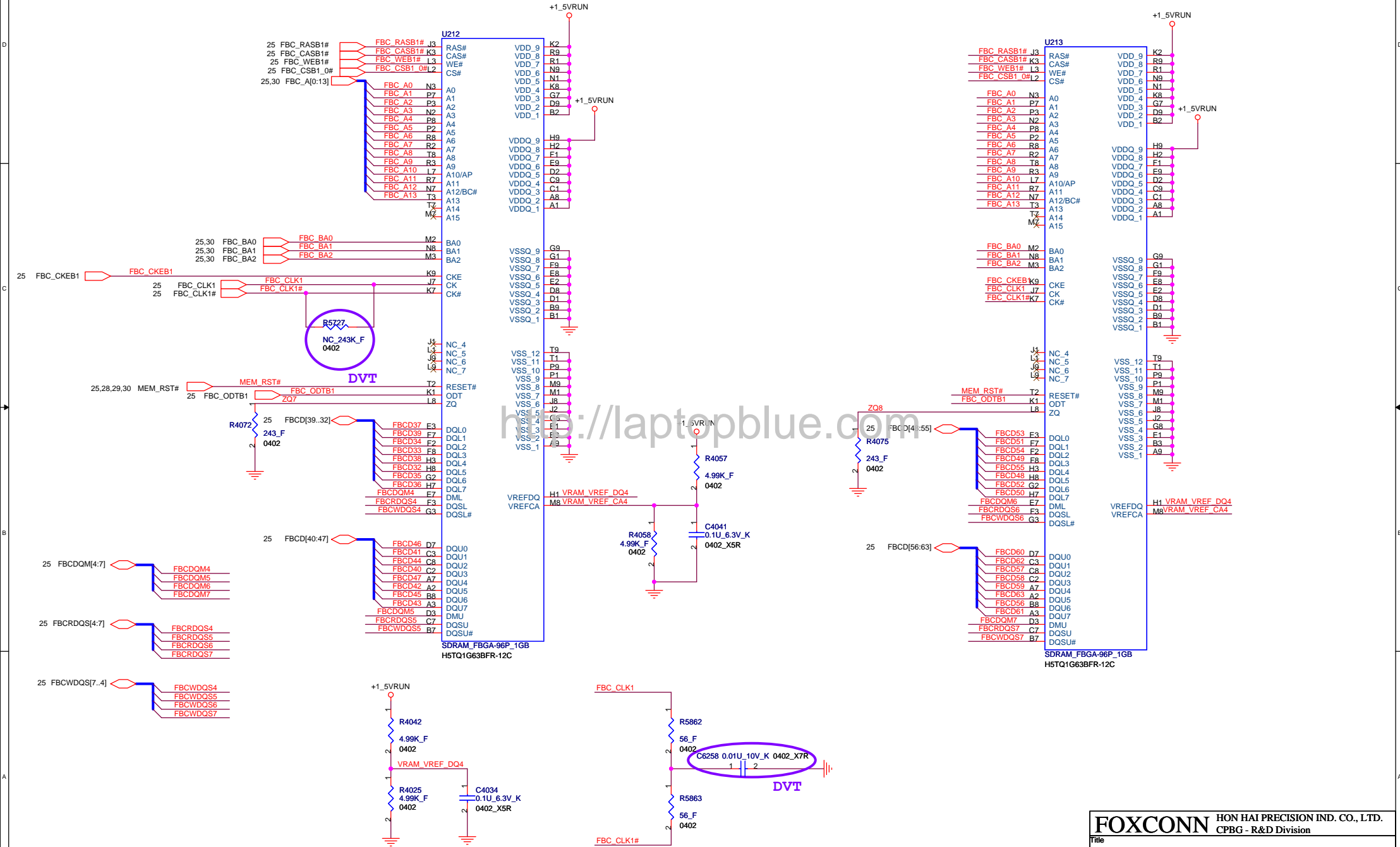
TXCLK =U=EVEN
TXOUT=U=EVEN
TXCLK =L=ODD
TXOUT=L=ODD



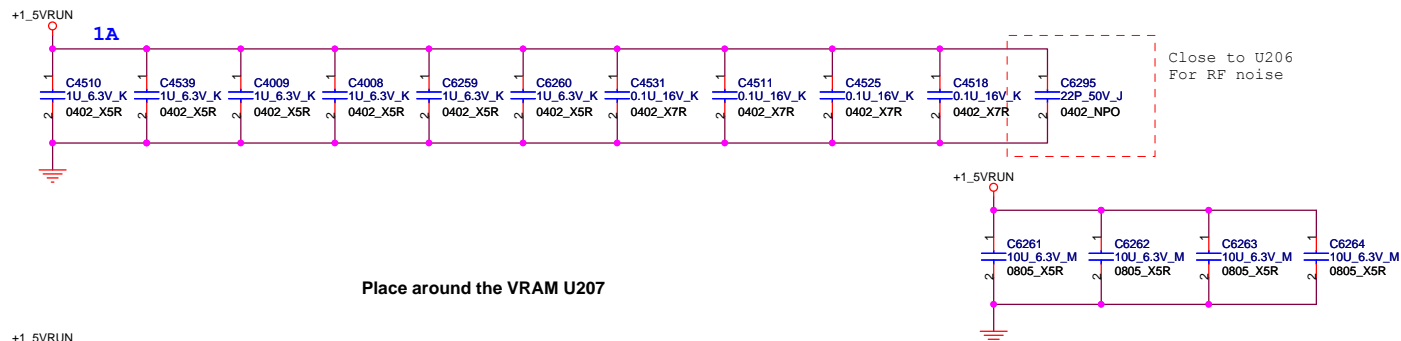




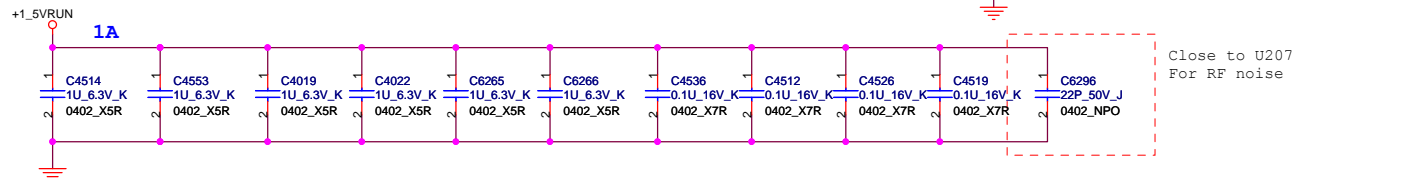




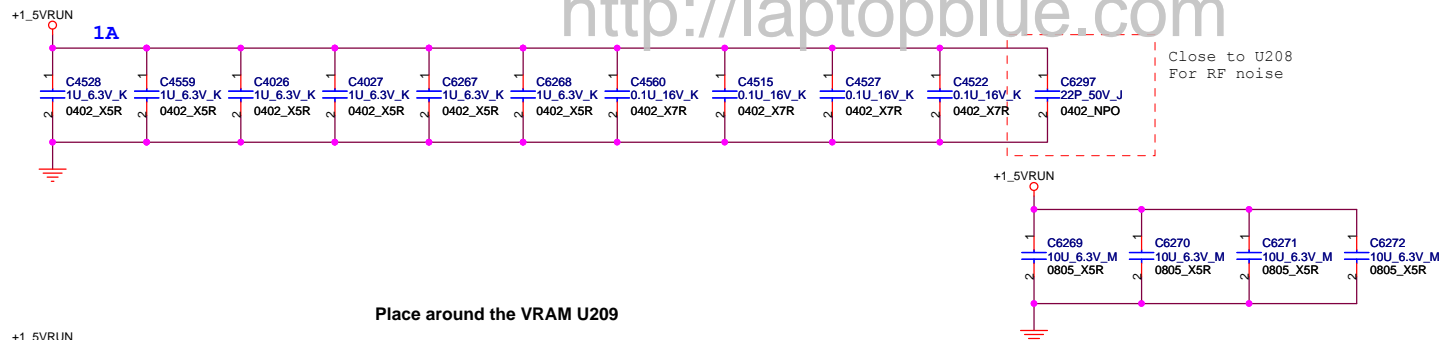
Place around the VRAM U206



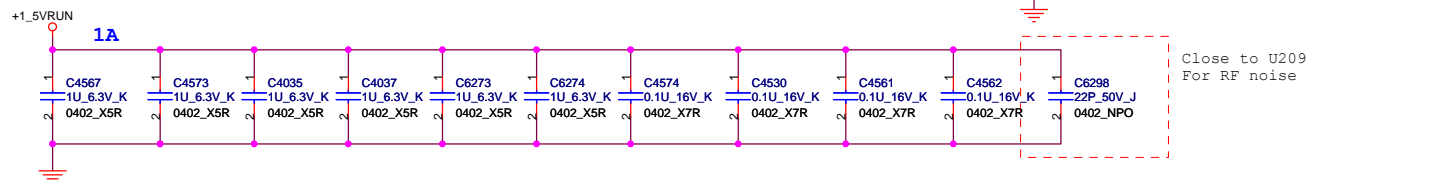
Place around the VRAM U207



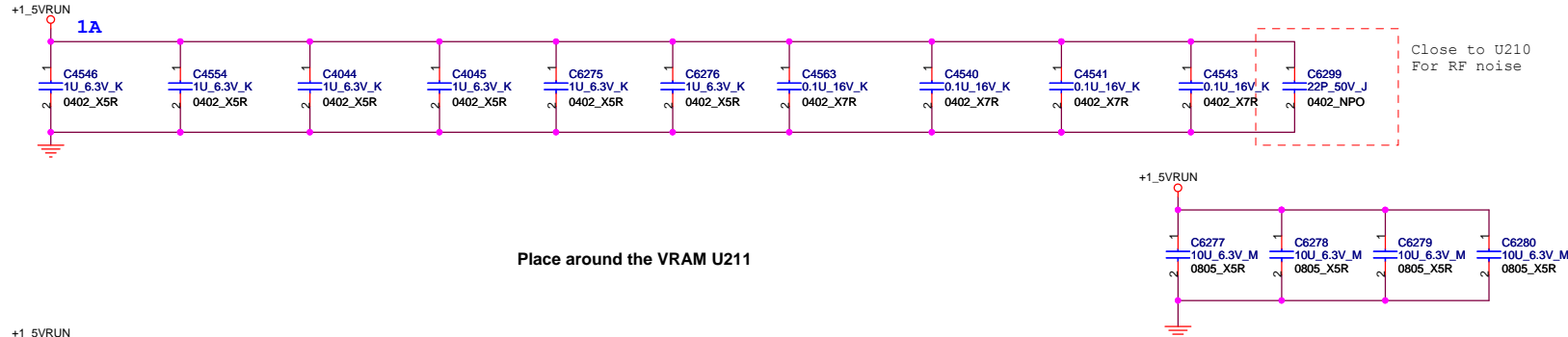
Place around the VRAM U208



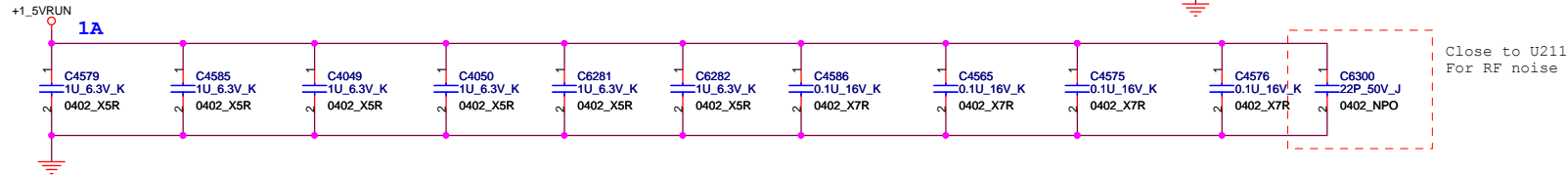
Place around the VRAM U209



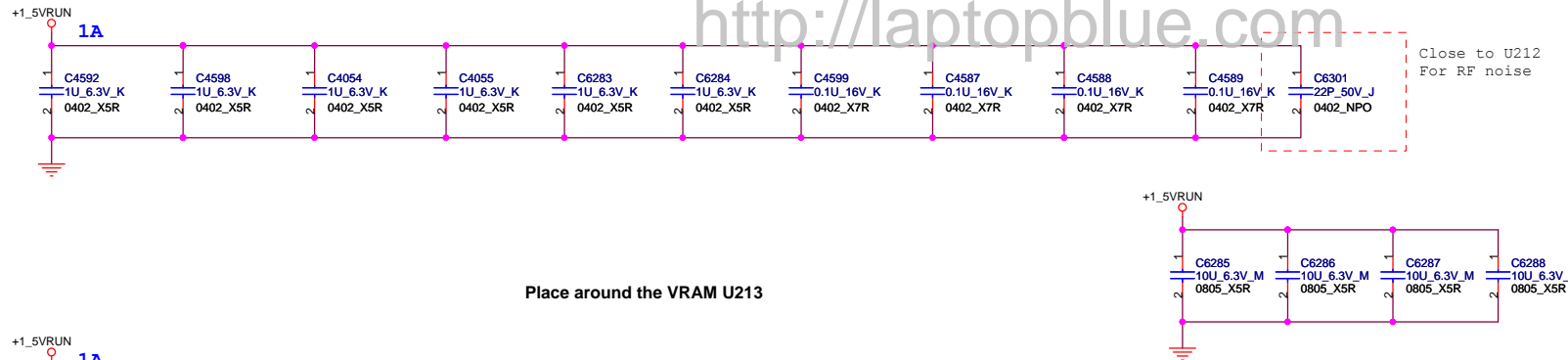
Place around the VRAM U210



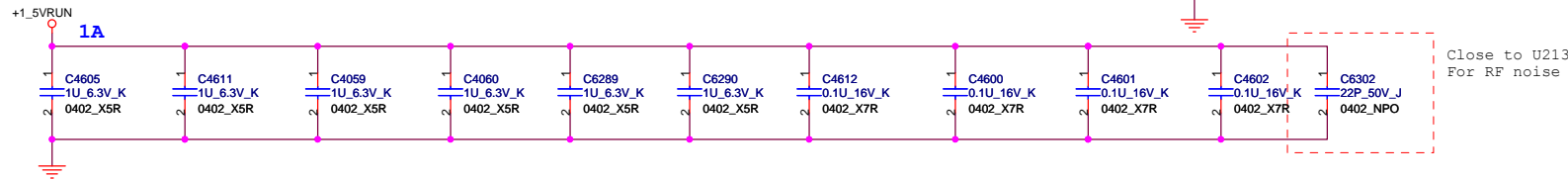
Place around the VRAM U211

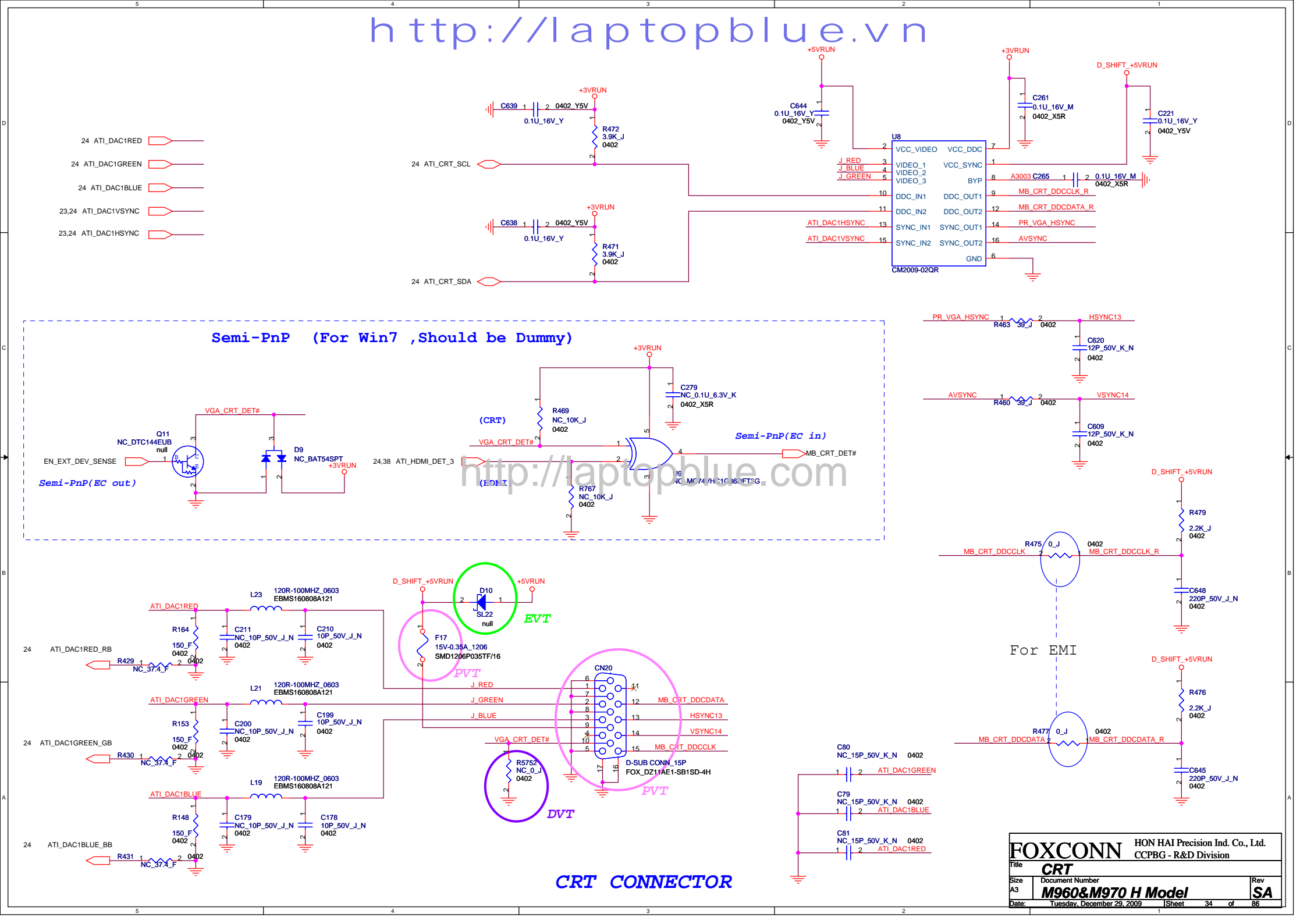
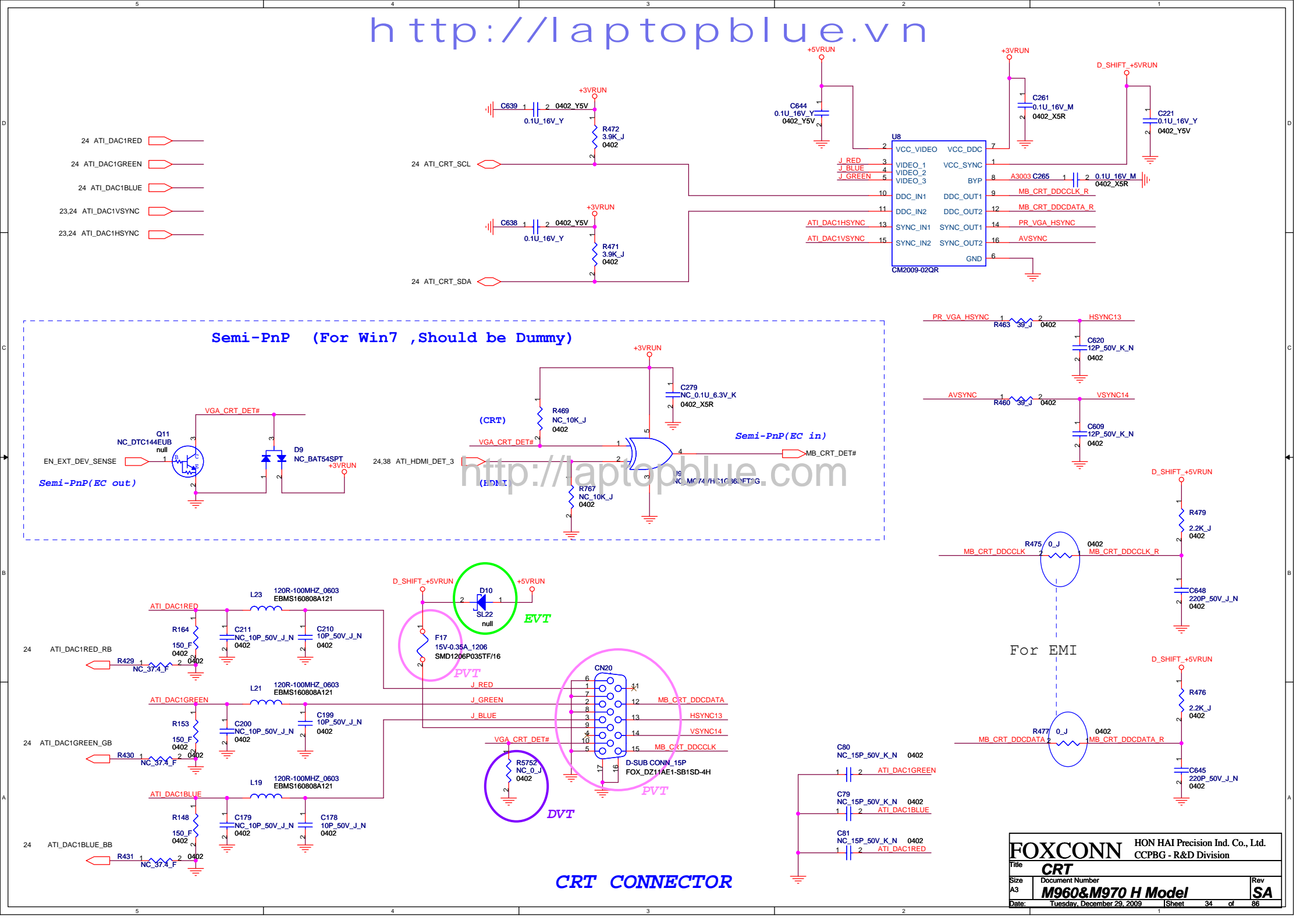
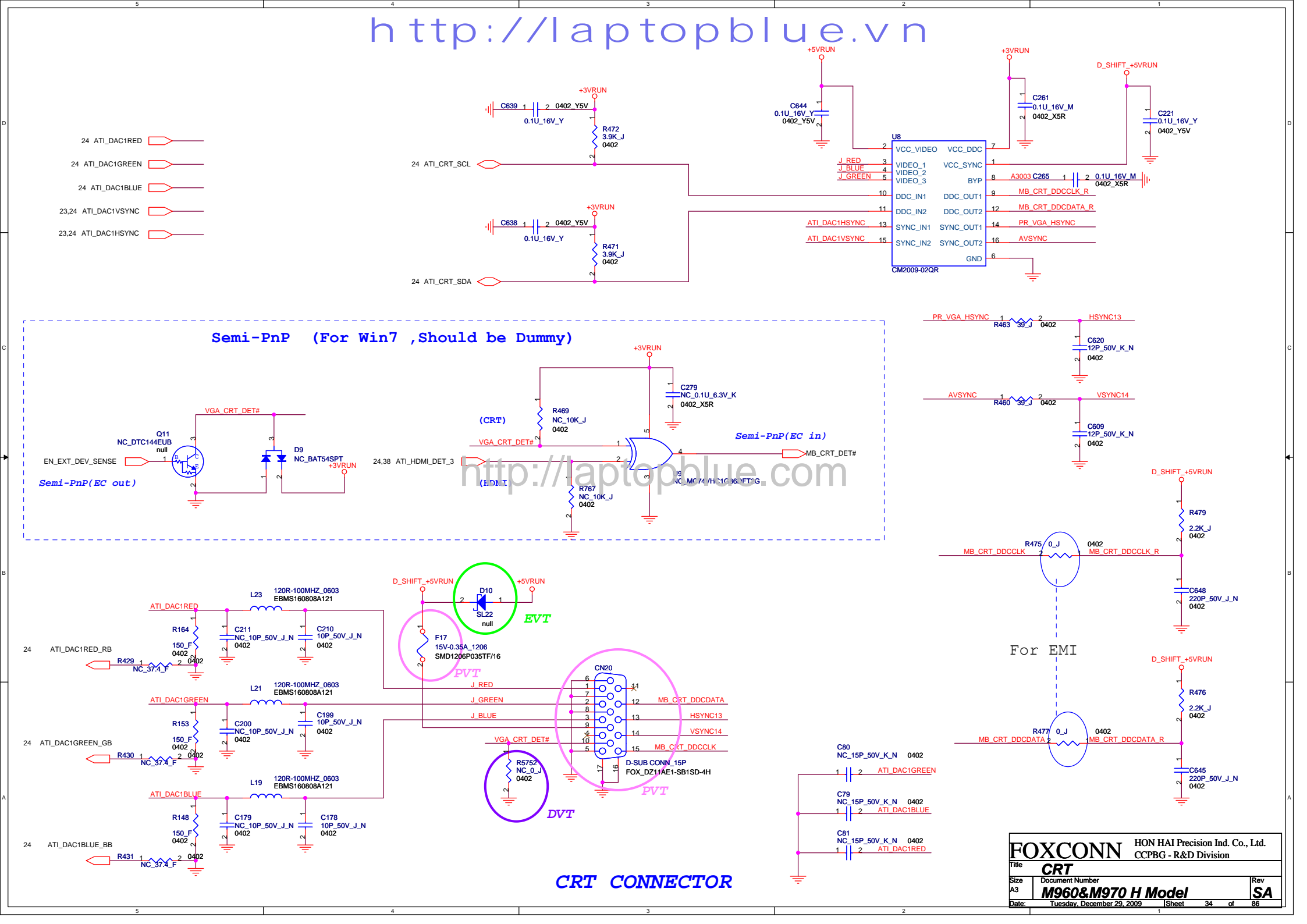
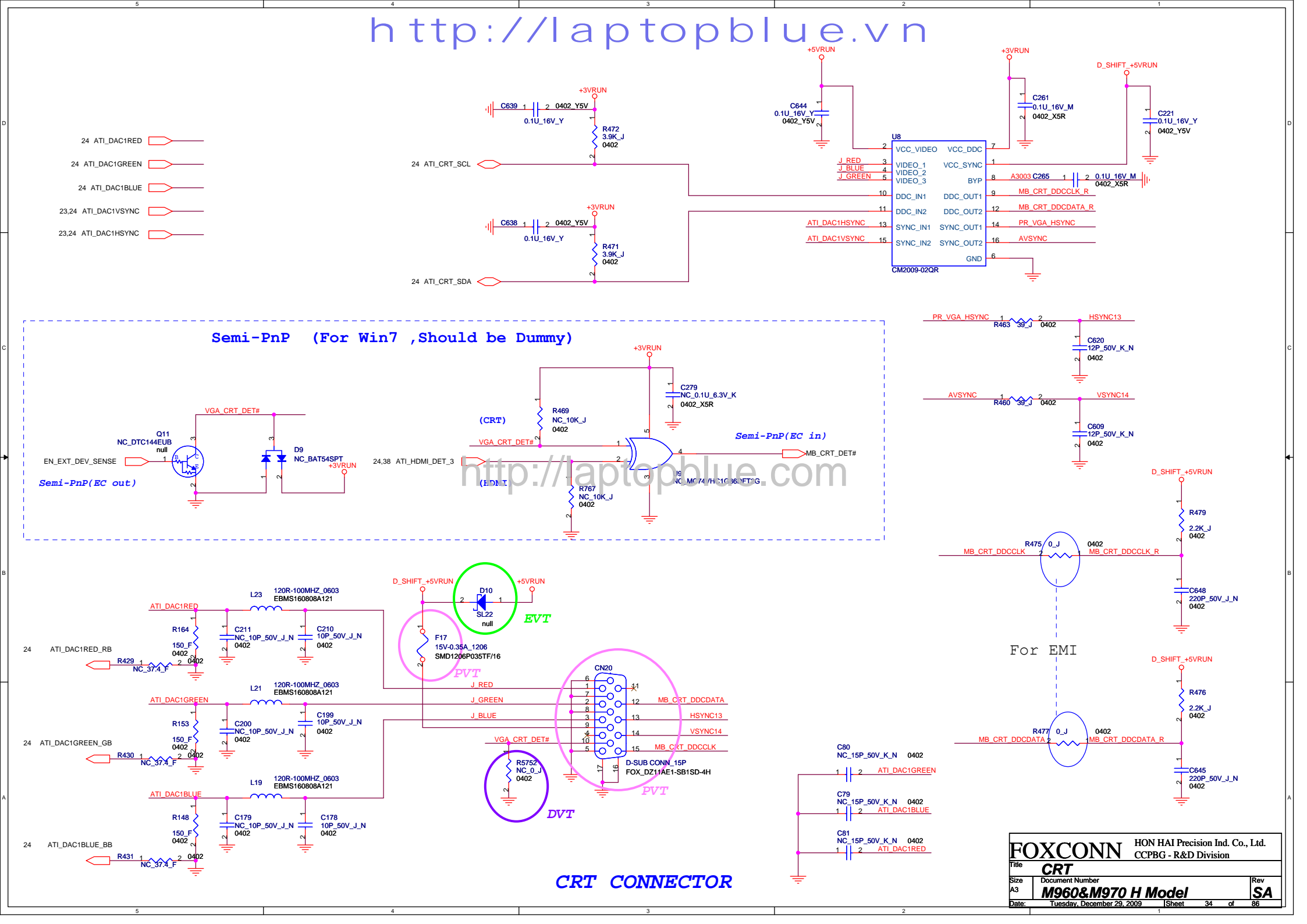
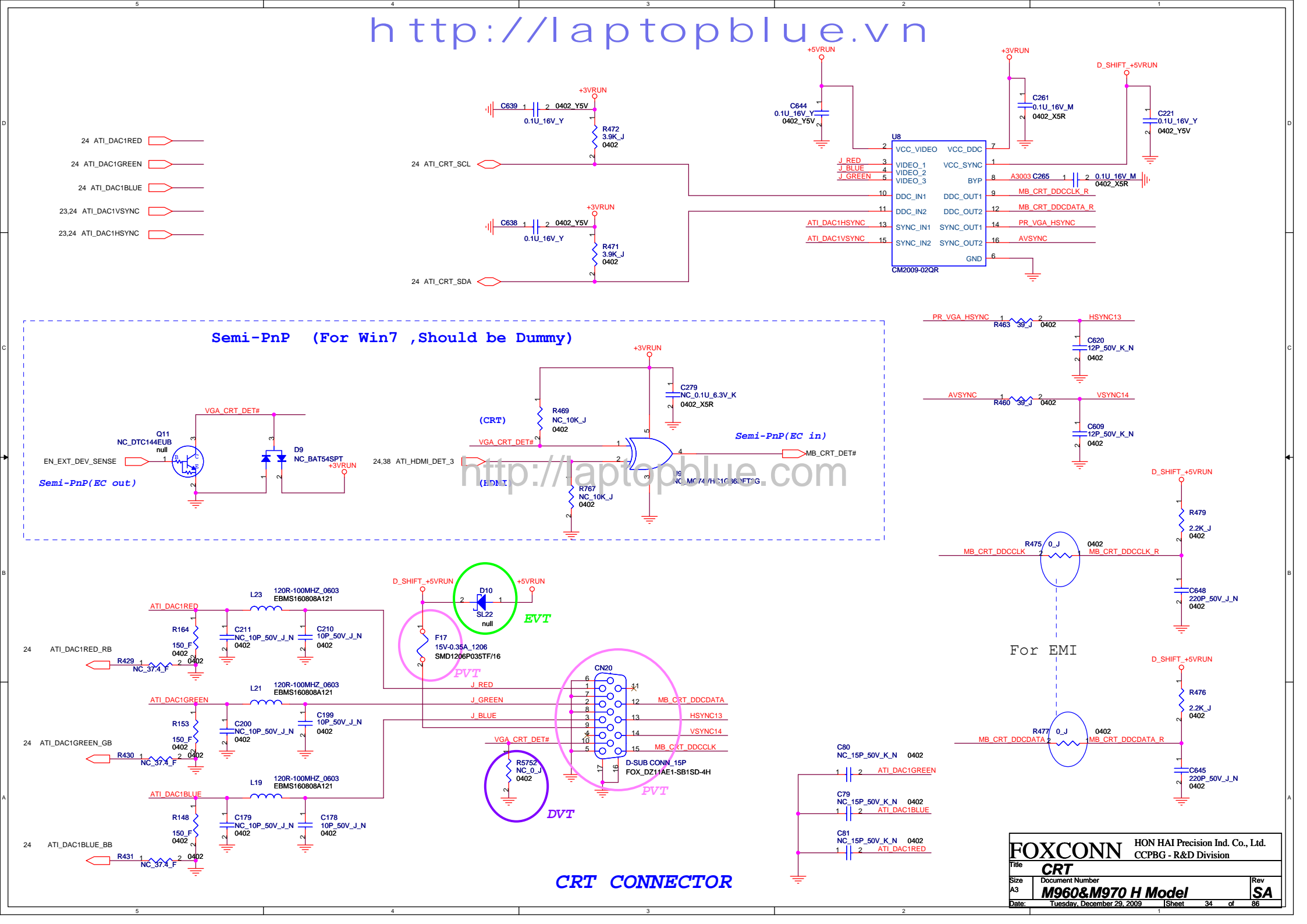
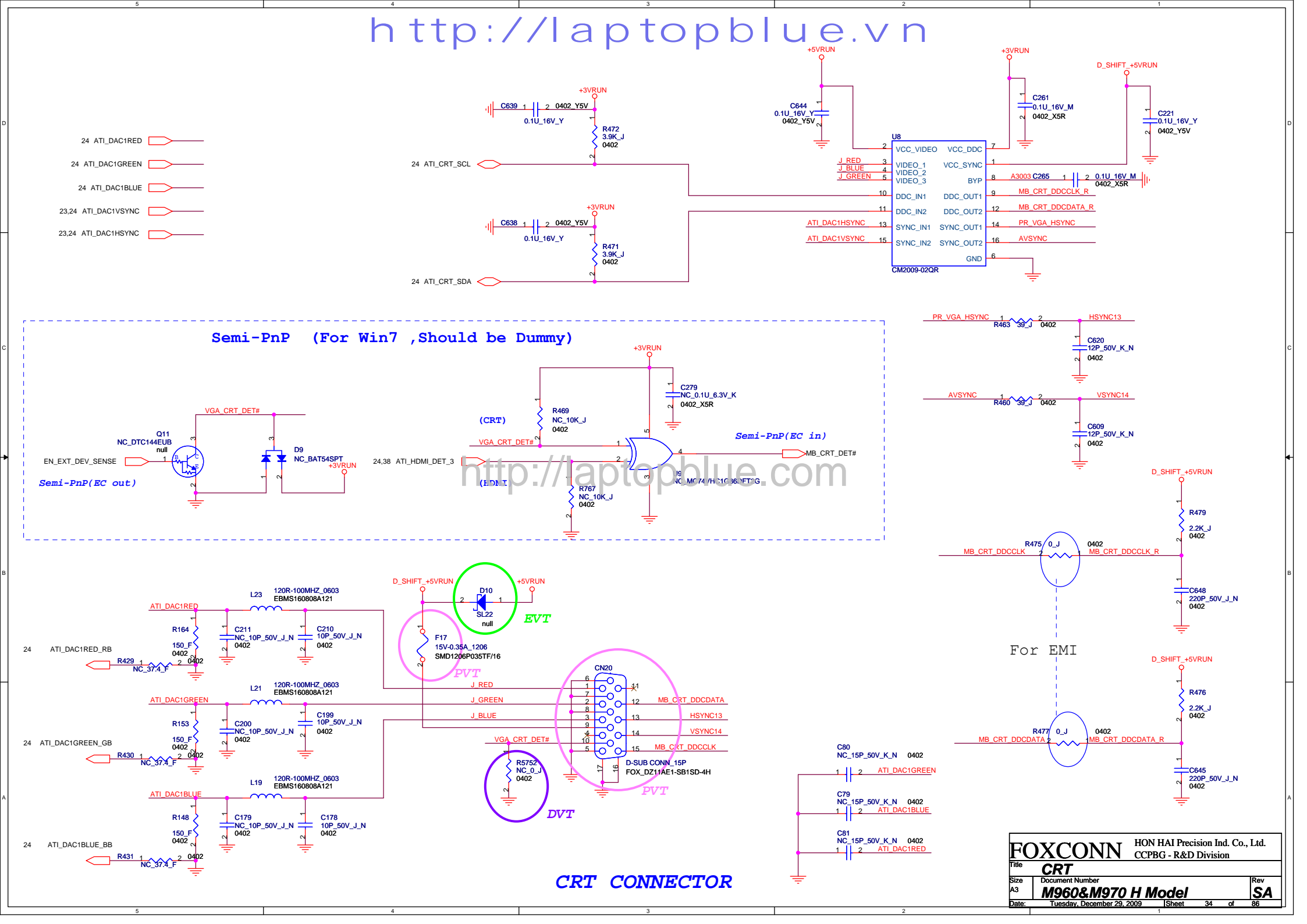
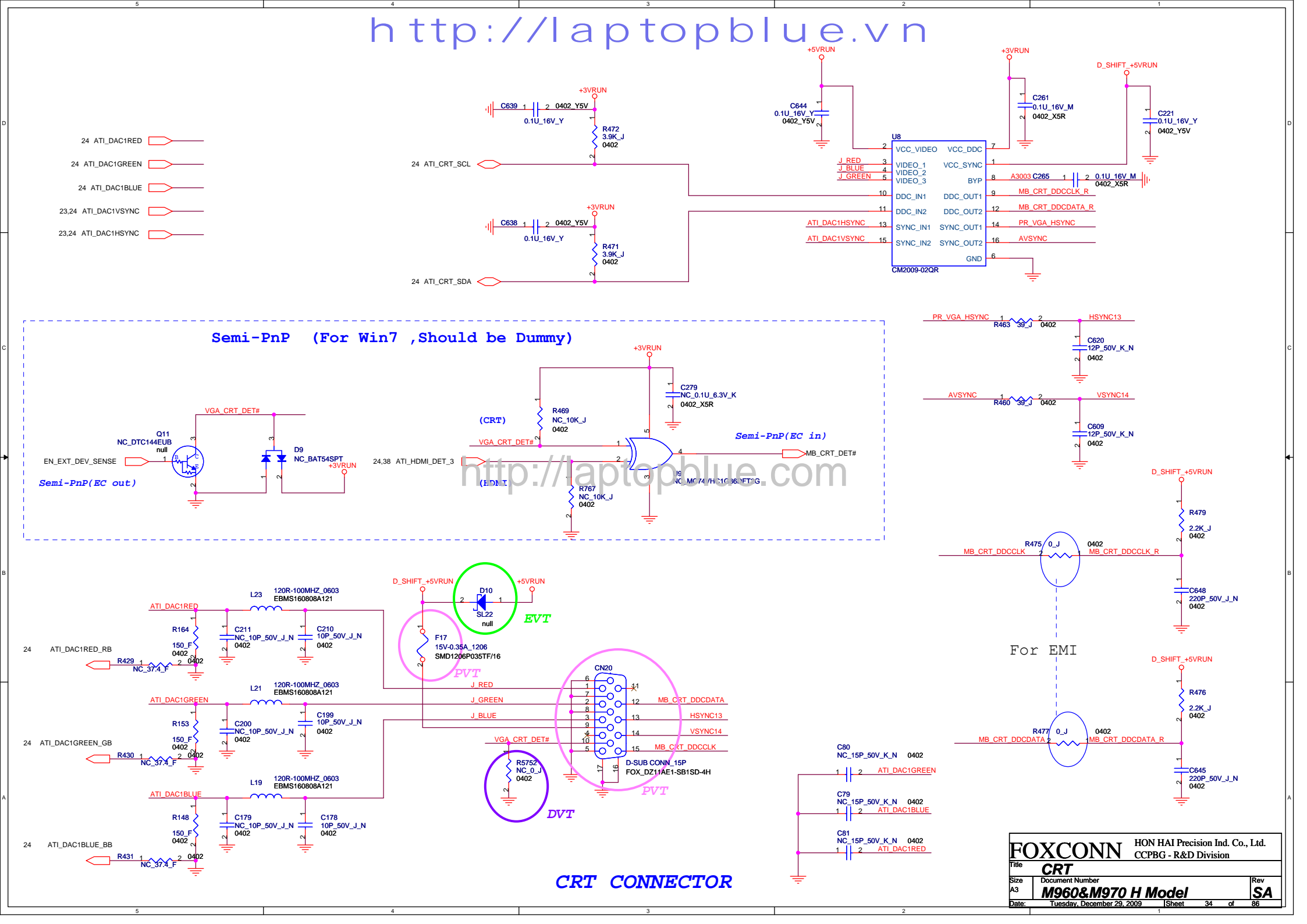


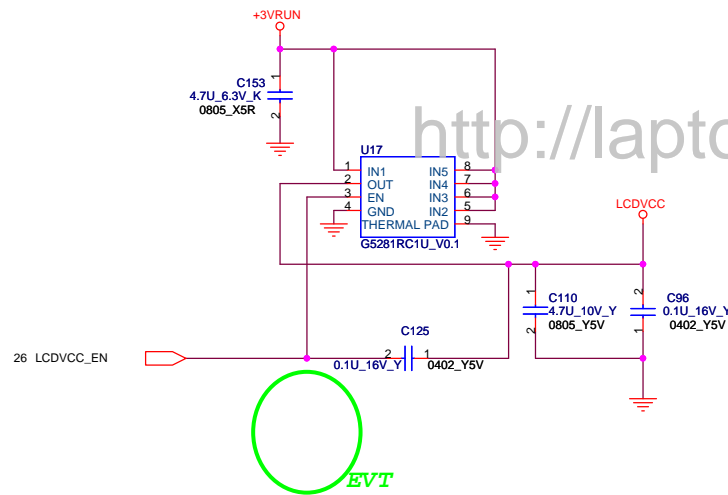
Place around the VRAM U212



Place around the VRAM U213



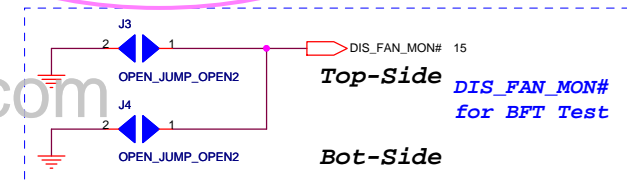
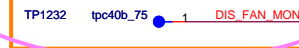
[illegible]



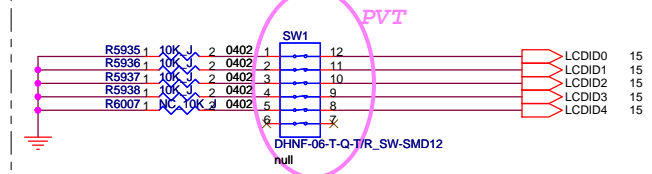
BFT Test Pad(Top)



BFT Test Pad(Bottom)



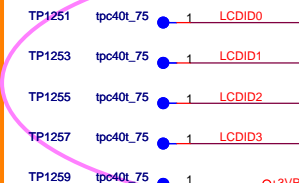
PANEL ID



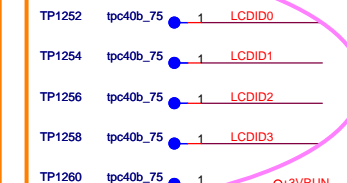
PANEL ID

Type		LED	LED	LED	LED	1	1	1	LED	LED	LED
Size	14	14	14	14	14	15.5	15.5	15.5	15.5	17.3	17.3
Vendor	No LCD	AUO	Samsung	LGD	AUO	LGD	CPT	Samsung	LGD	CPT	AUO
Model Name		B140XW02	LTN140AT08	LP140WH2	B140RW02	LP156WH1	CLAA156WA01A	LTN156AT01	LP156WF1	CLAA173UA01A	B173HW01
Panel ID [4.3.2.1.0]	00000	00001	00010	00011	00100	00110	00111	01000	01001	01011	01100

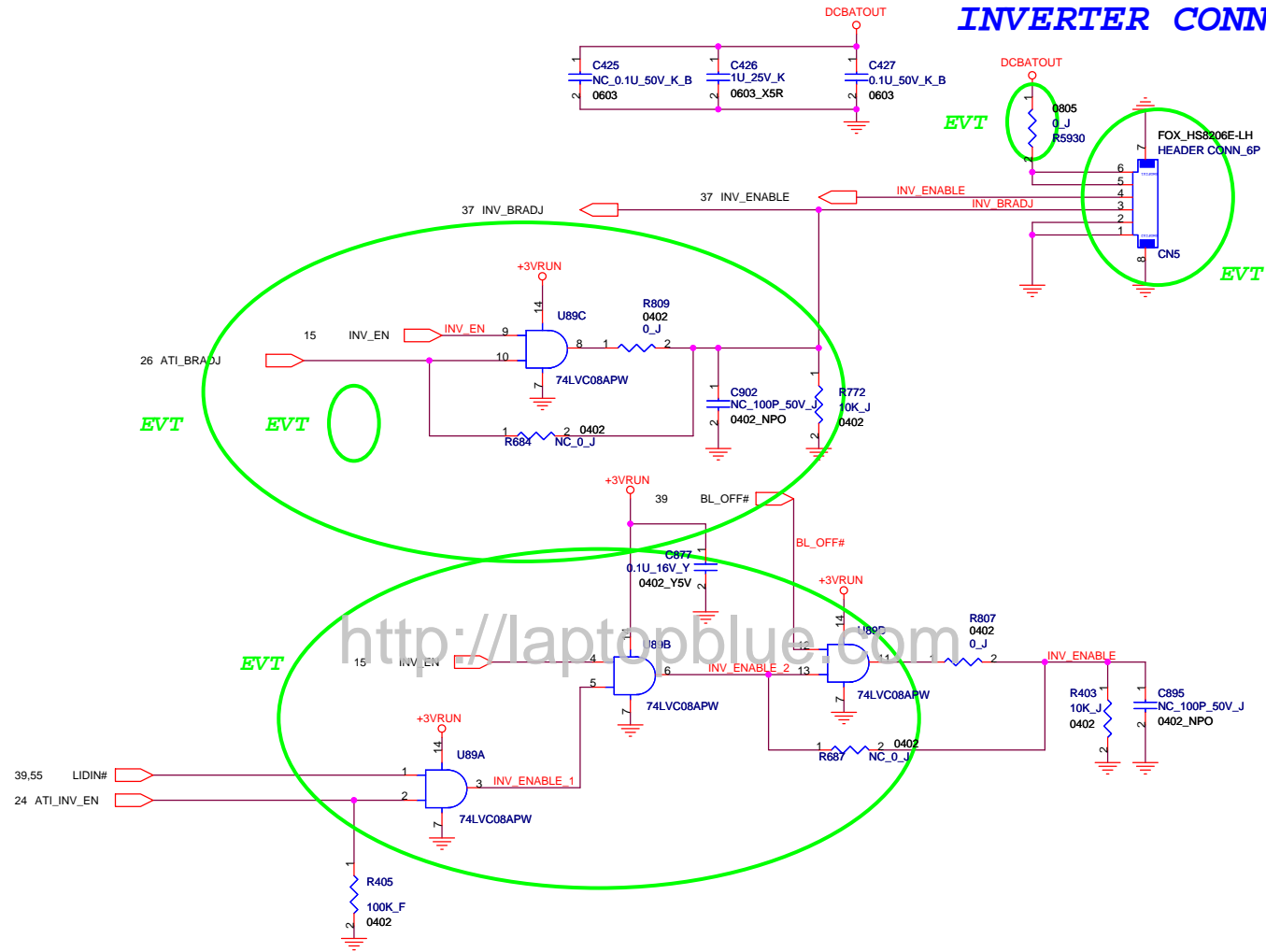
BFT Test Pad(Top)



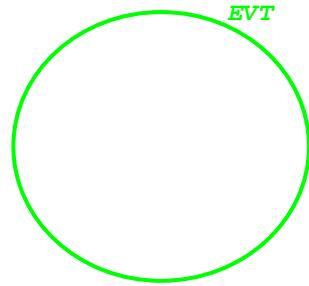
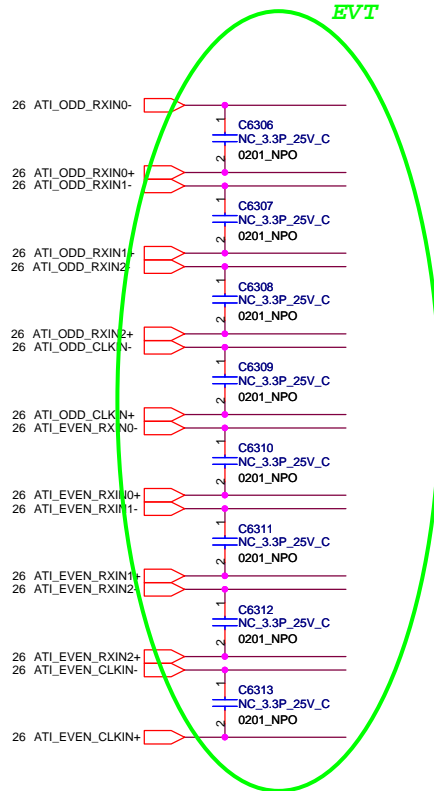
BFT Test Pad(Bottom)



INVERTER CONNECTOR

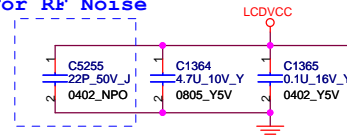


For RF verification, del these cap. in DVT if these cap. do not use.



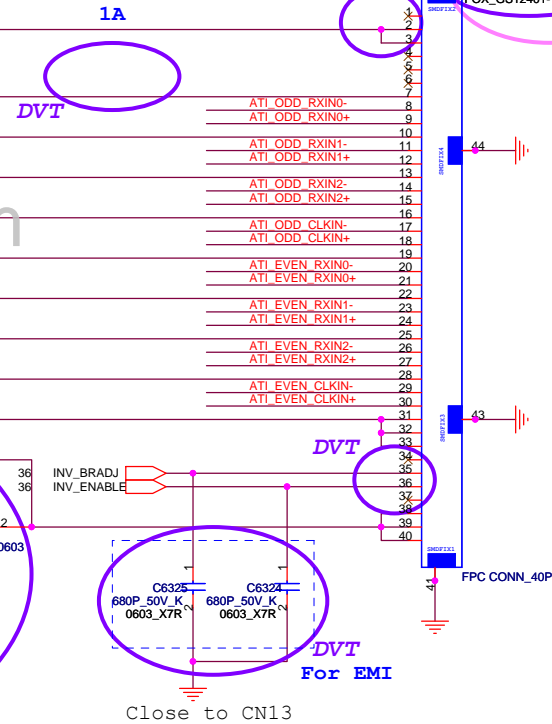
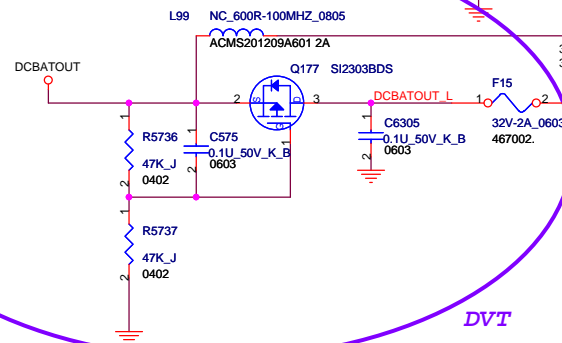
LVDS CONNECTOR

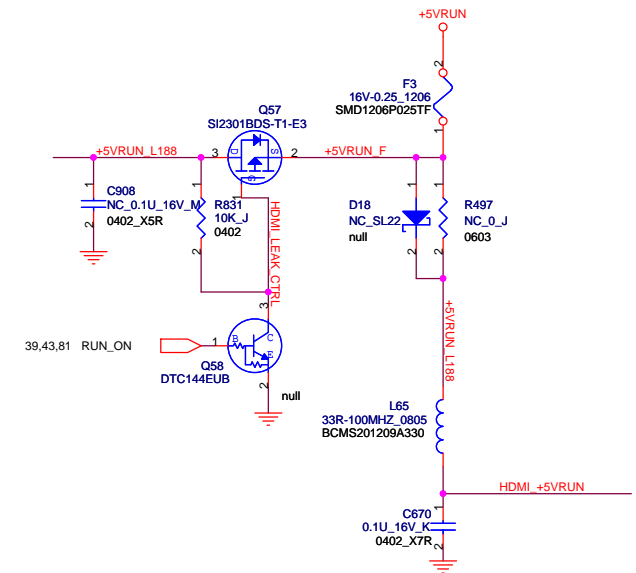
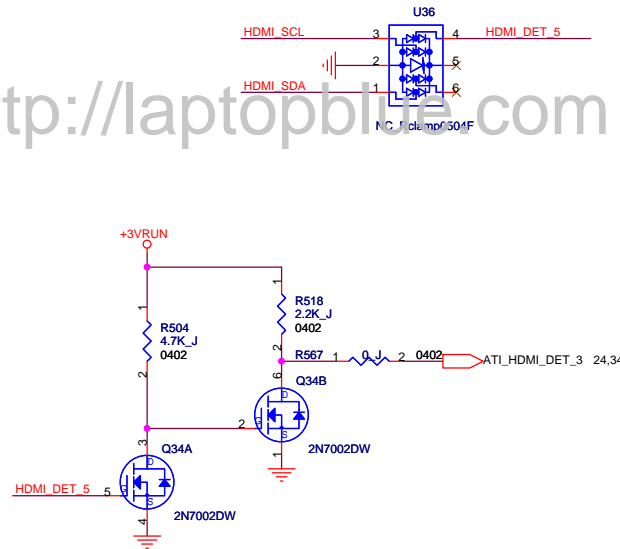
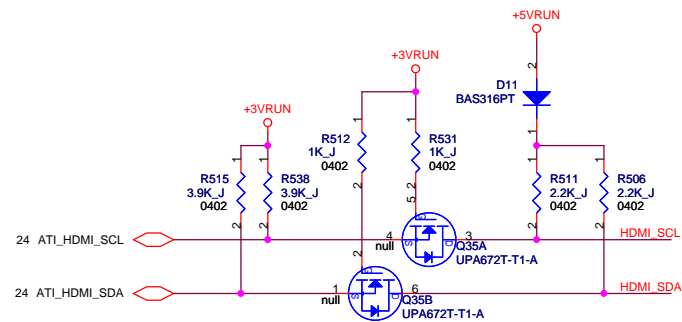
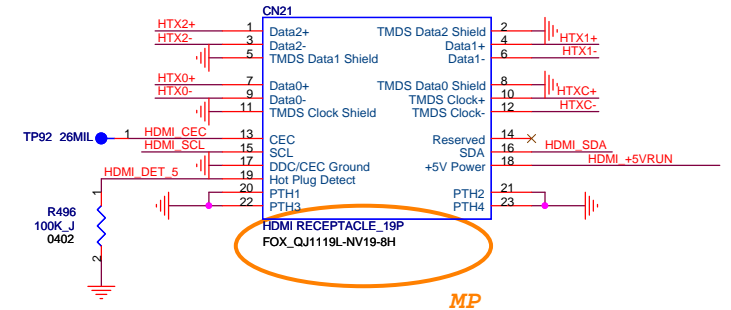
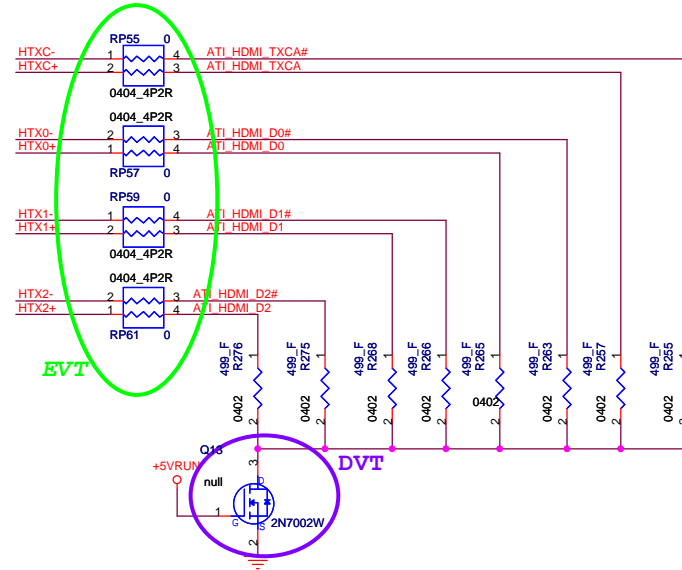
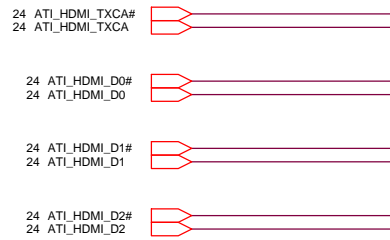
For RF Noise

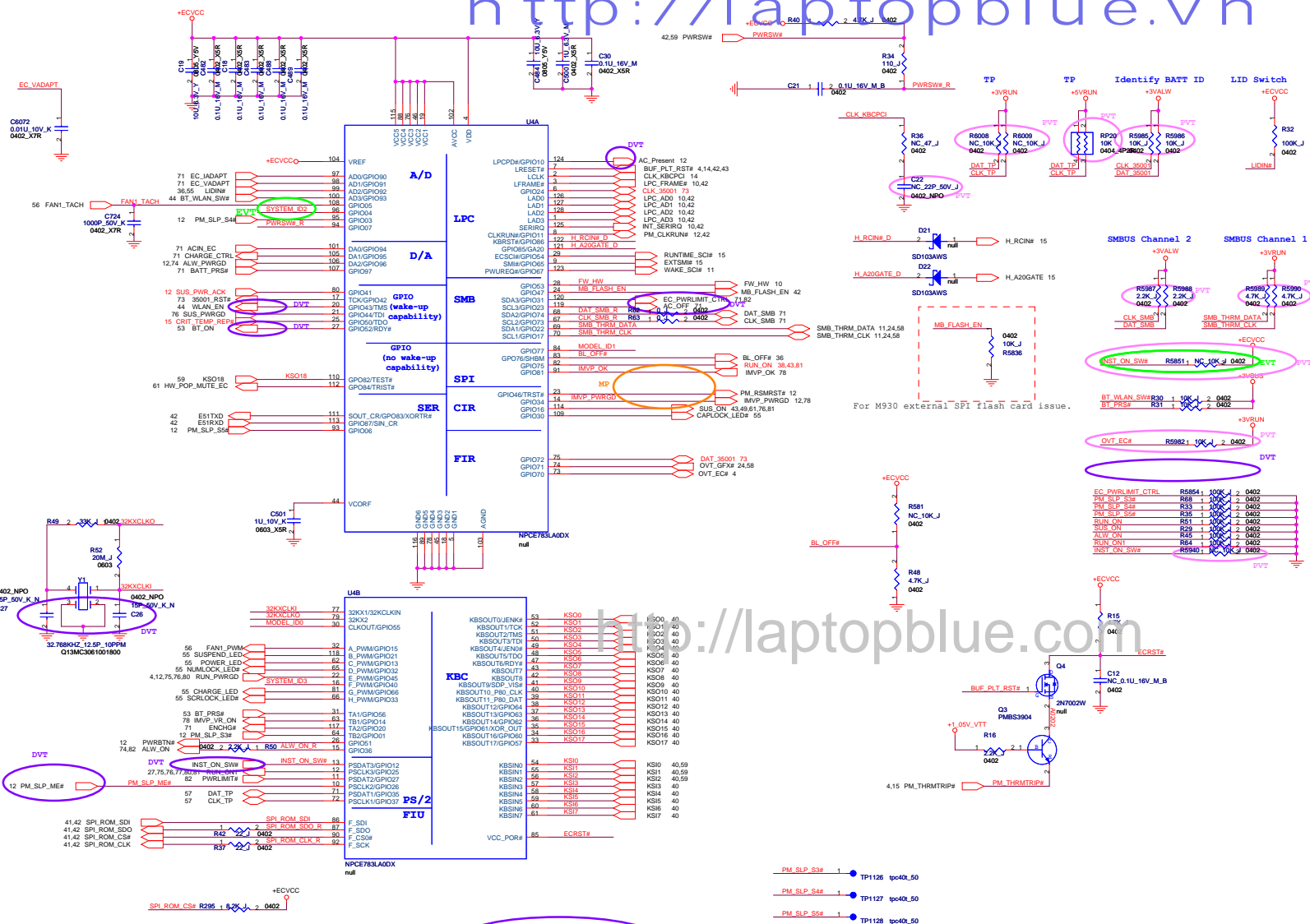


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For rush current issue







MODEL ID0-1

ECVCC	KBQVCC	NPCE783L_VADAPT
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
10	10	10
11	11	11
12	12	12
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100	100	100

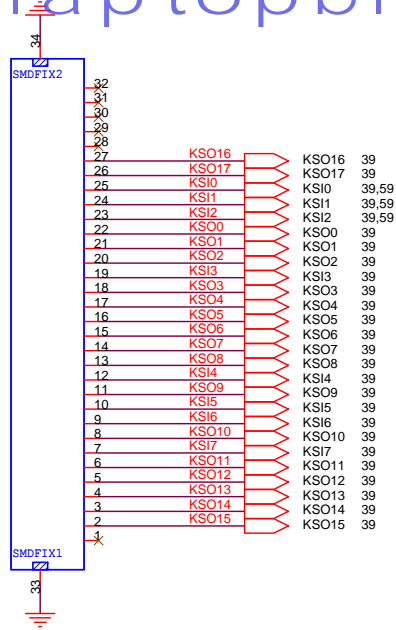
SYSTEM ID0-2

ECVCC	KBQVCC	NPCE783L_VADAPT
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95	95	95
96	96	96
97	97	97
98	98	98
99	99	99
100	100	100

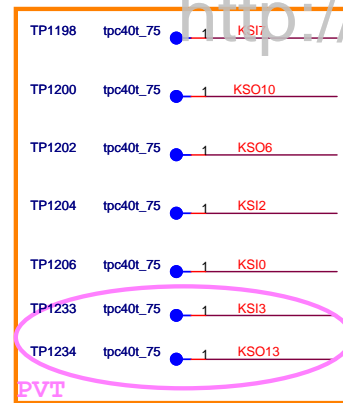
http://laptopblue.vn

KBC Conn

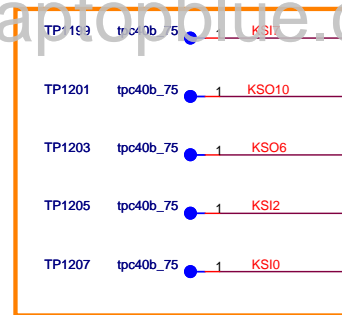
CN38
FPC CONN_32P
FOX_GB1SH320-1280-7H



BFT Test Pad(Top)



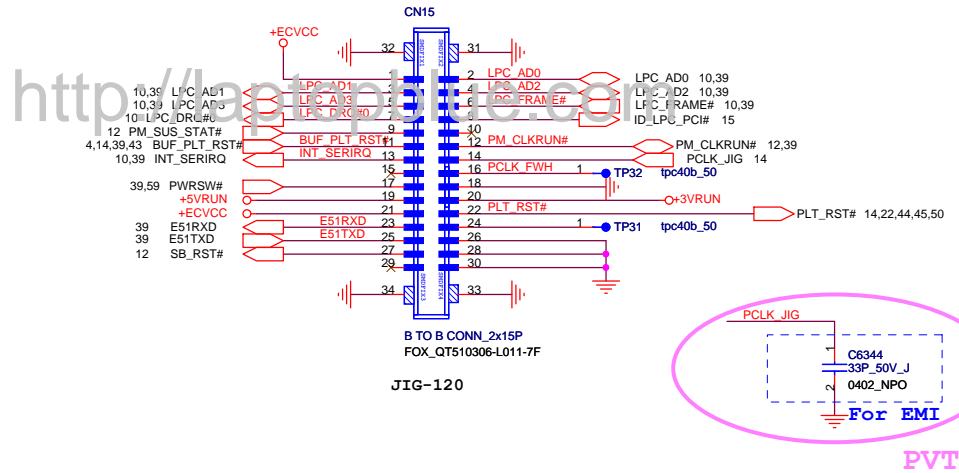
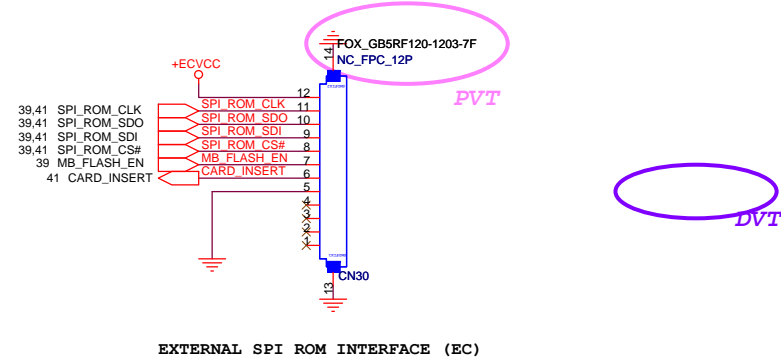
BFT Test Pad(Bottom)

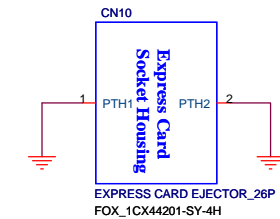
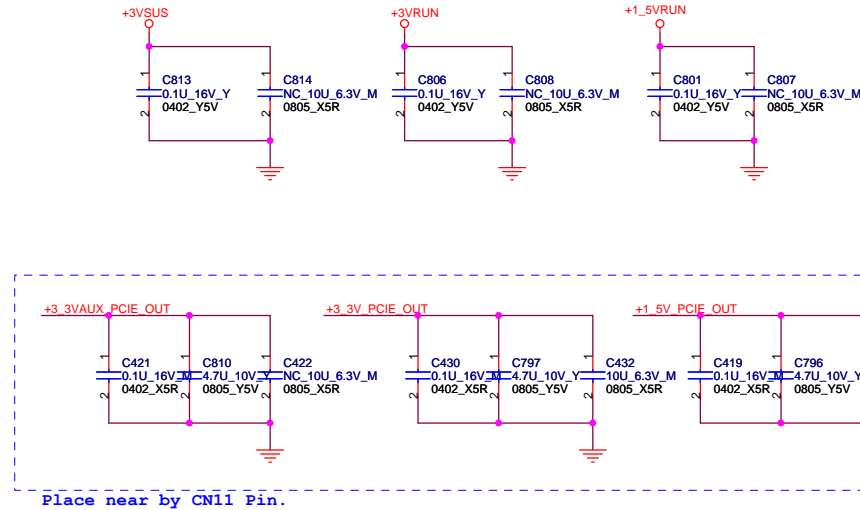
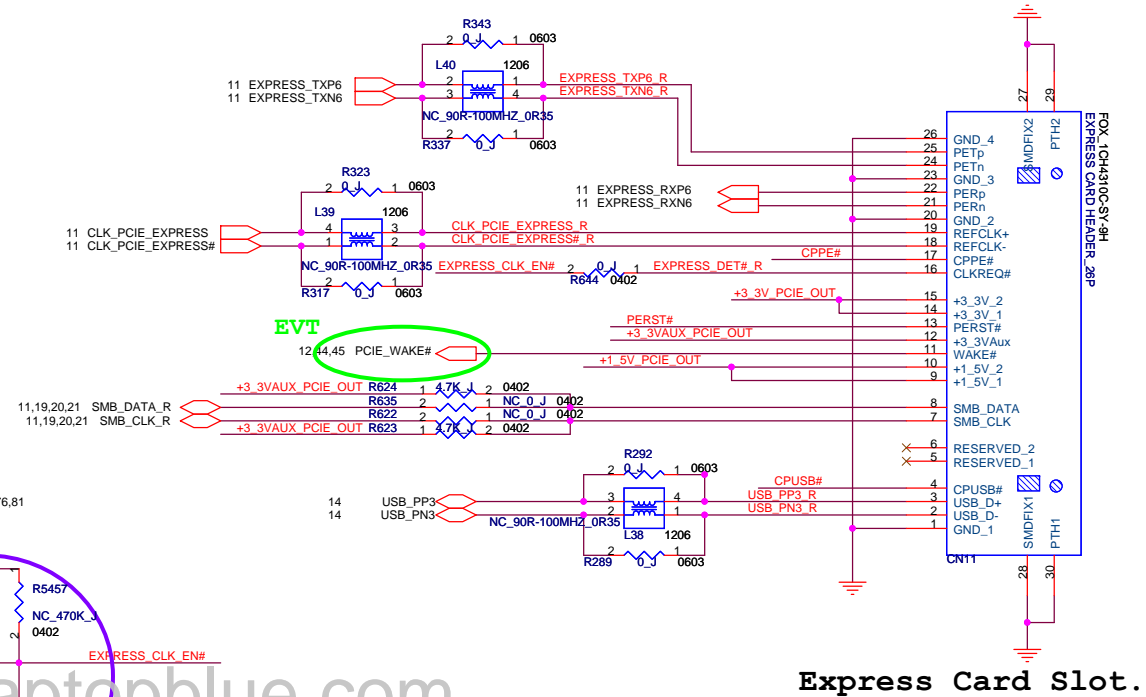
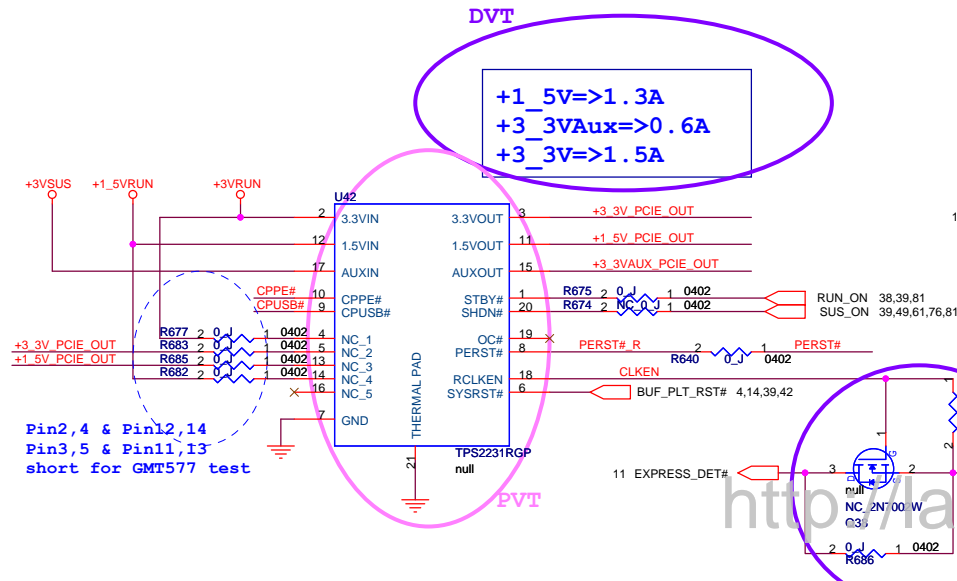


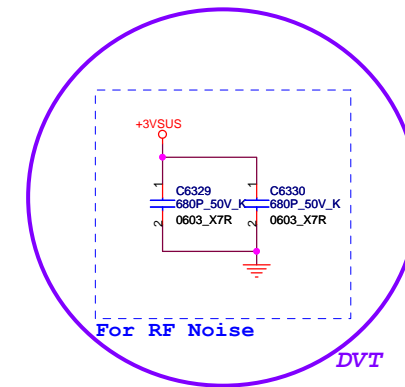
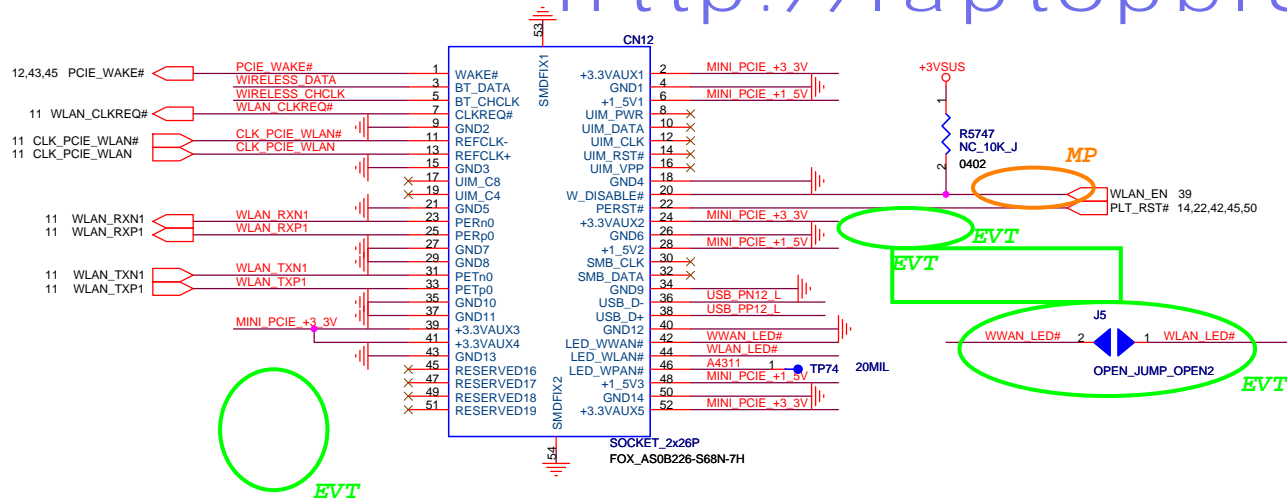
EVT

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title KB Connector			
Size	Document Number		Rev
B	M960&M970 H Model		SA
Date:	Tuesday, December 29, 2009	Sheet	40 of 86

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	<i>SPI Flash ROM</i>		
Size A3	Document Number <i>M960&M970 H Model</i>	Rev <i>SA</i>	
Date:	Tuesday, December 29, 2009	Sheet	41 of 86

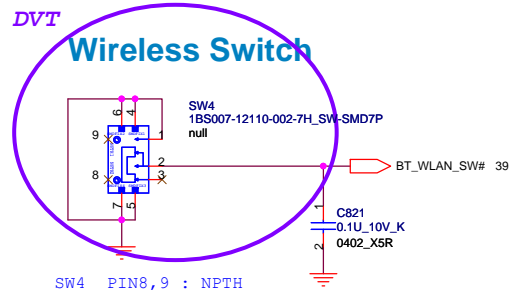




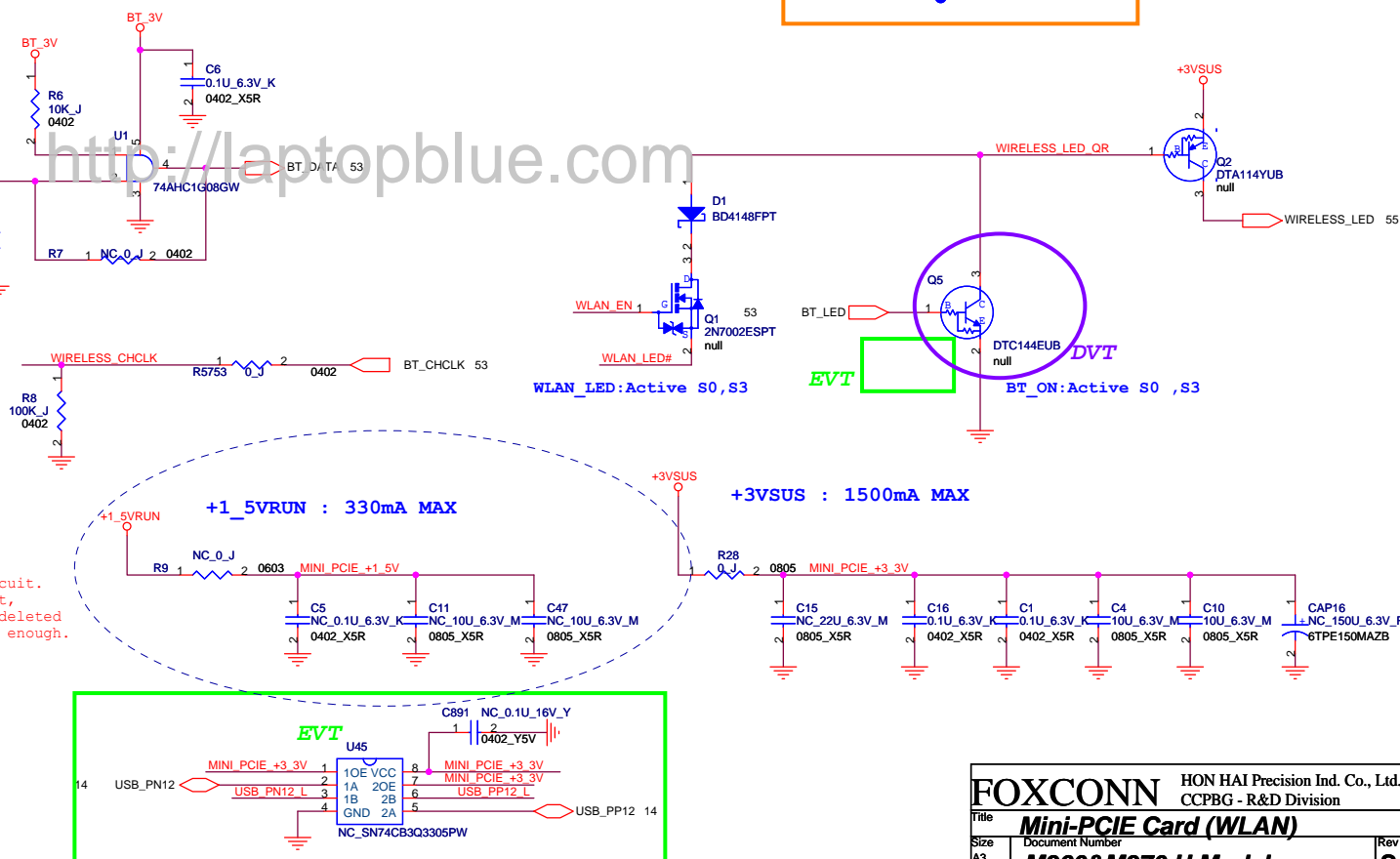


Power Test Test Point (Top)

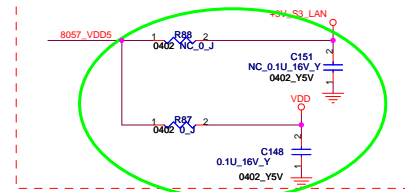
TP1223 tpc60t_100 1 WIRELESS_LED_QR



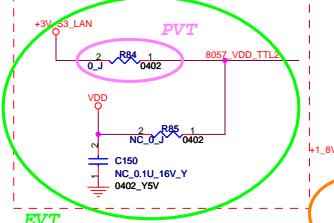
This is a reserved circuit.
According to RF comment,
this circuit could be deleted
if Layout space is not enough.



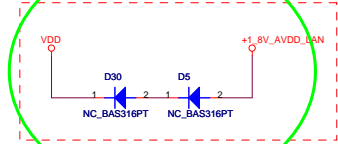
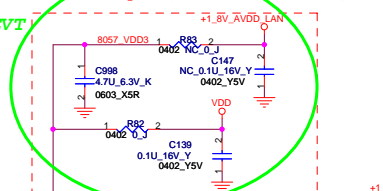
For 8059 Dummy R88 ,C151, and Stuff R87 ,C148
For 8057 Dummy R87, C148 and Stuff R88 ,C151



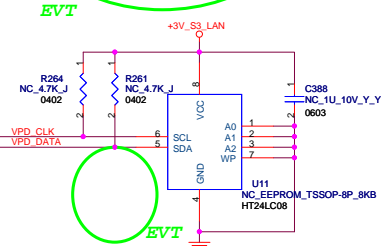
For 8059 Dummy R85 ,C150, and Stuff R84
For 8057 Dummy R84 and Stuff R85 ,C150



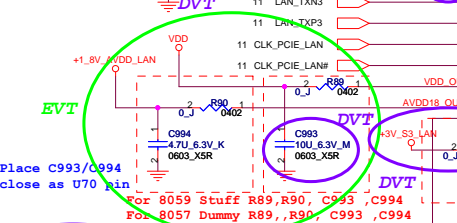
For 8059 Dummy R83 ,C147, and Stuff R82 ,C139
For 8057 Dummy R82, C139 and Stuff R83 ,C147



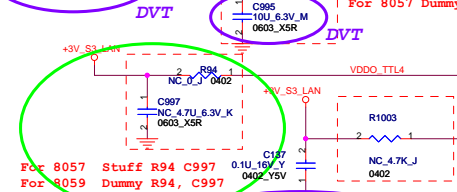
For 8059 Z0 version ONLY,
It's LDO Power-Up Issue workaround.



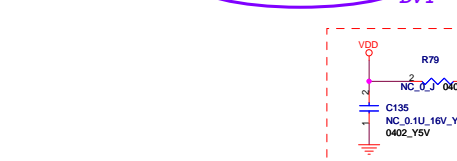
For 8059 Stuff C6341
For 8057 Dummy C6341



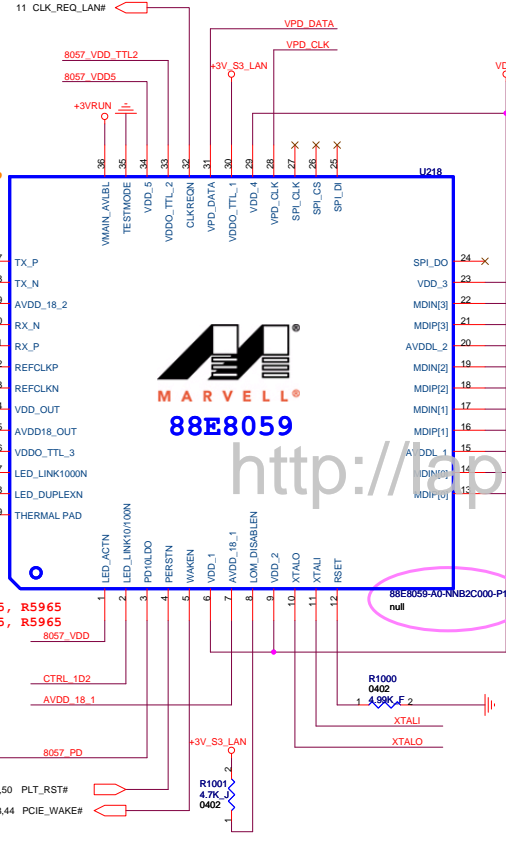
Place C993/C994
close as U70 pin



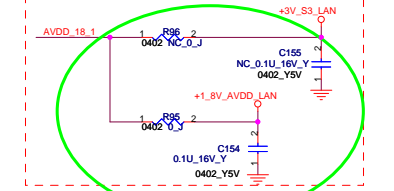
For 8059, Dummy R1003
For 8057, Stuff R1003

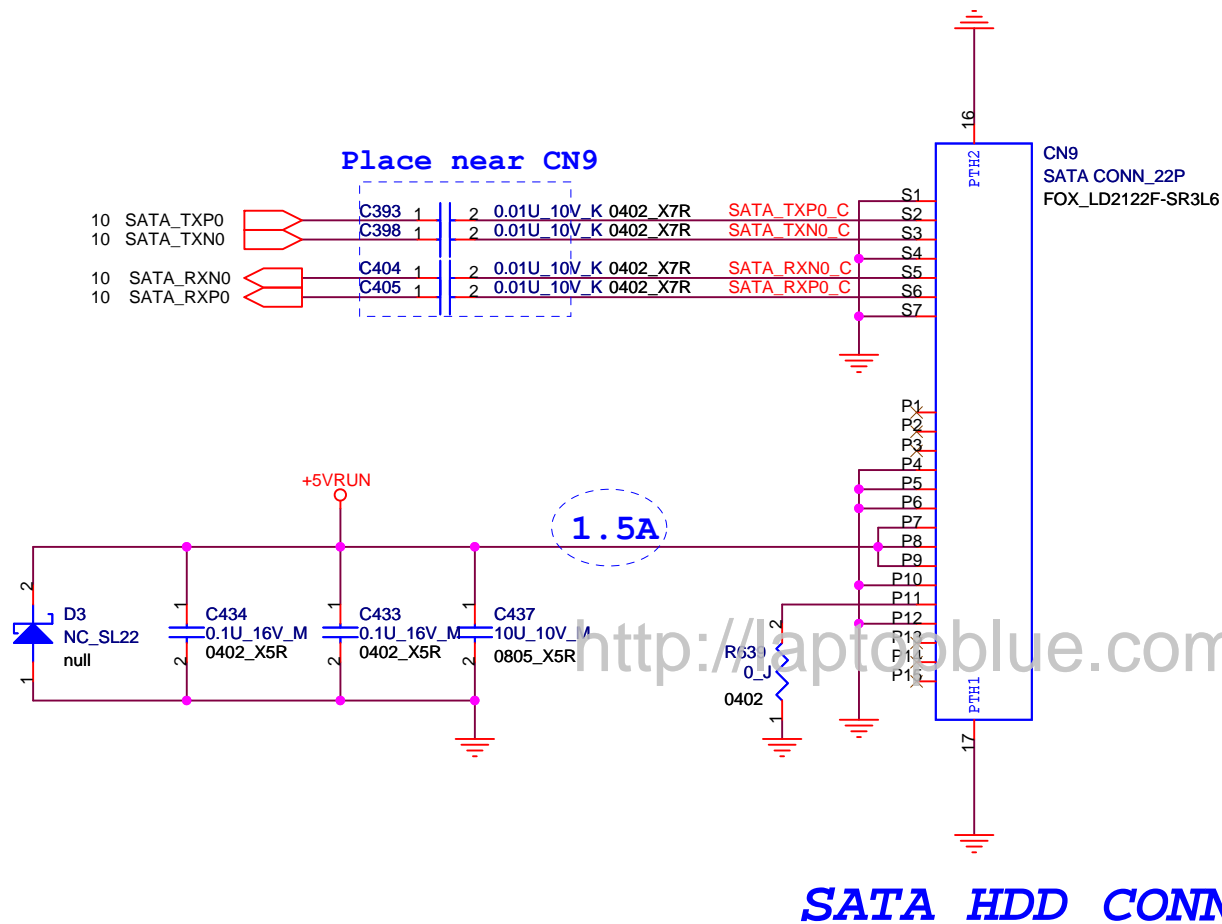


Dummy all when use 88E8059 (A0/Z0)

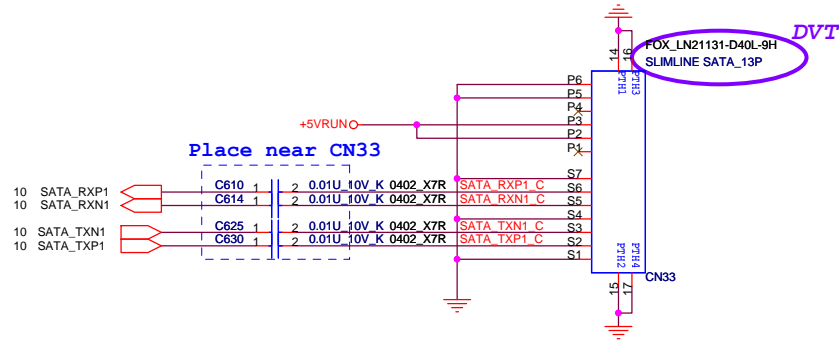


For 8059 Dummy R96 ,C155, and Stuff R95 ,C154
For 8057 Dummy R95, C154 and Stuff R96 ,C155

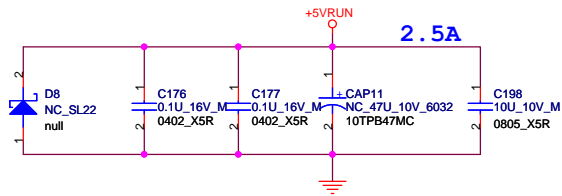




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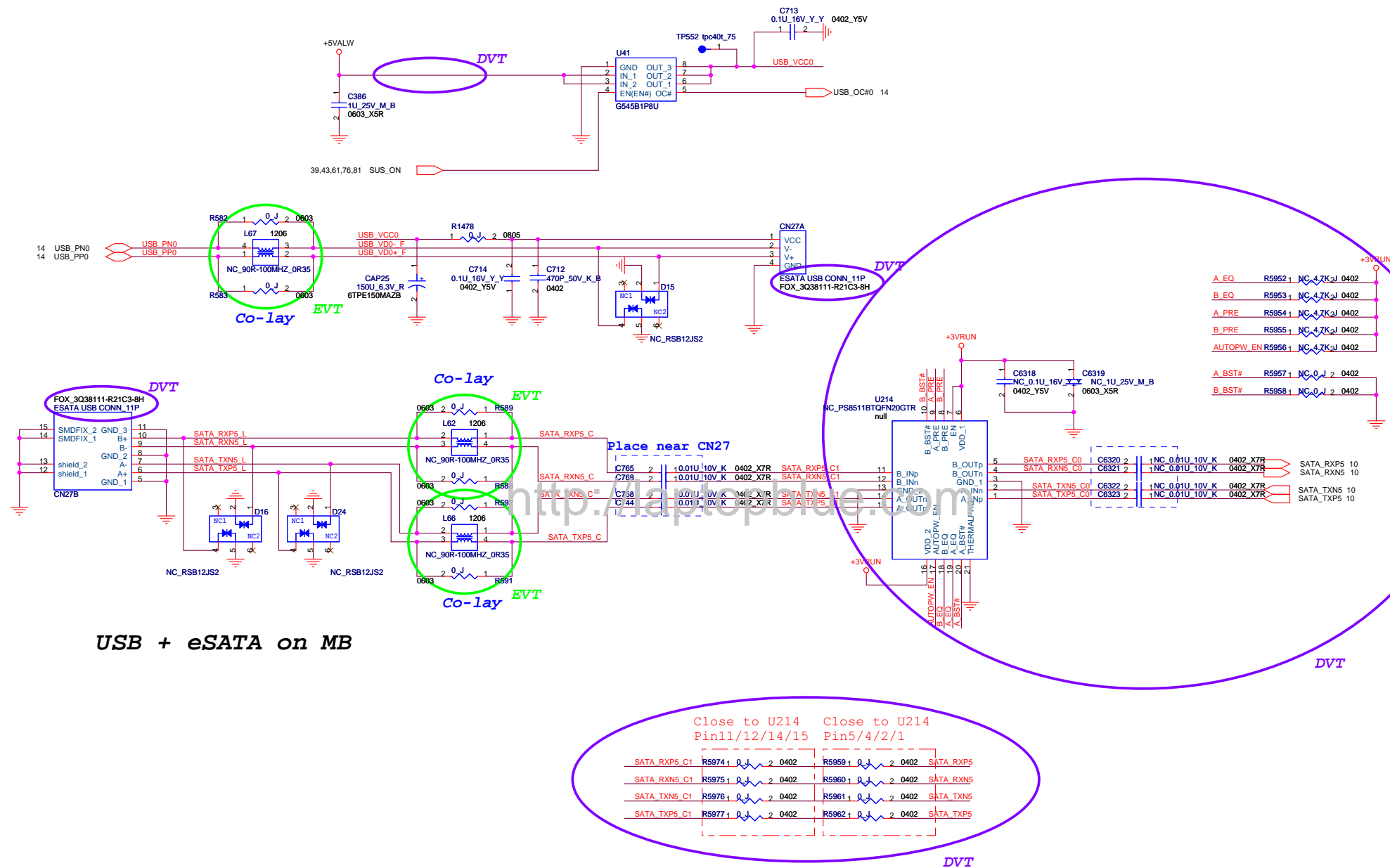


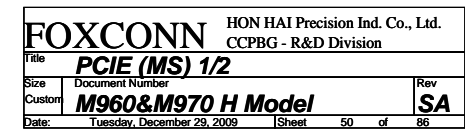
SATA ODD CONN



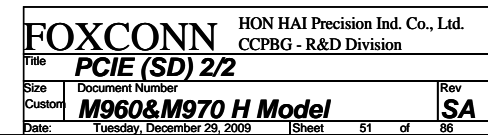
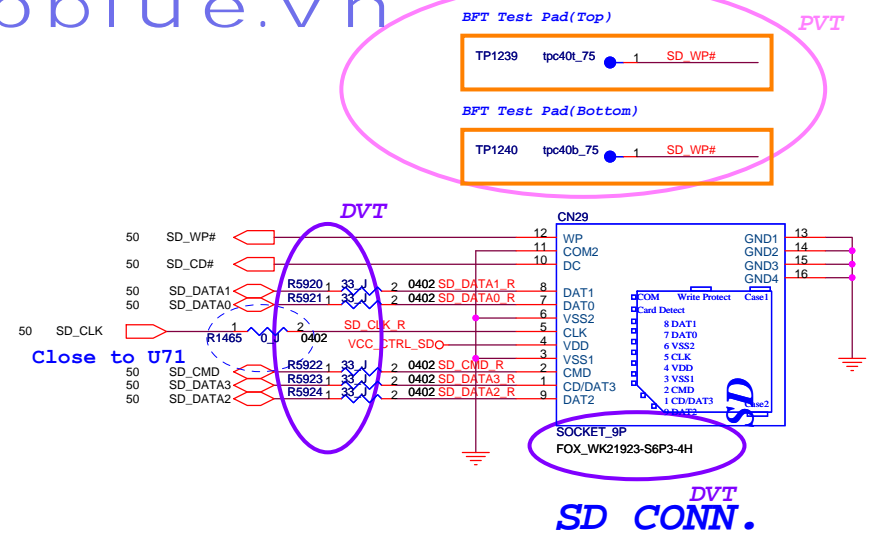
http://laptopblue.com

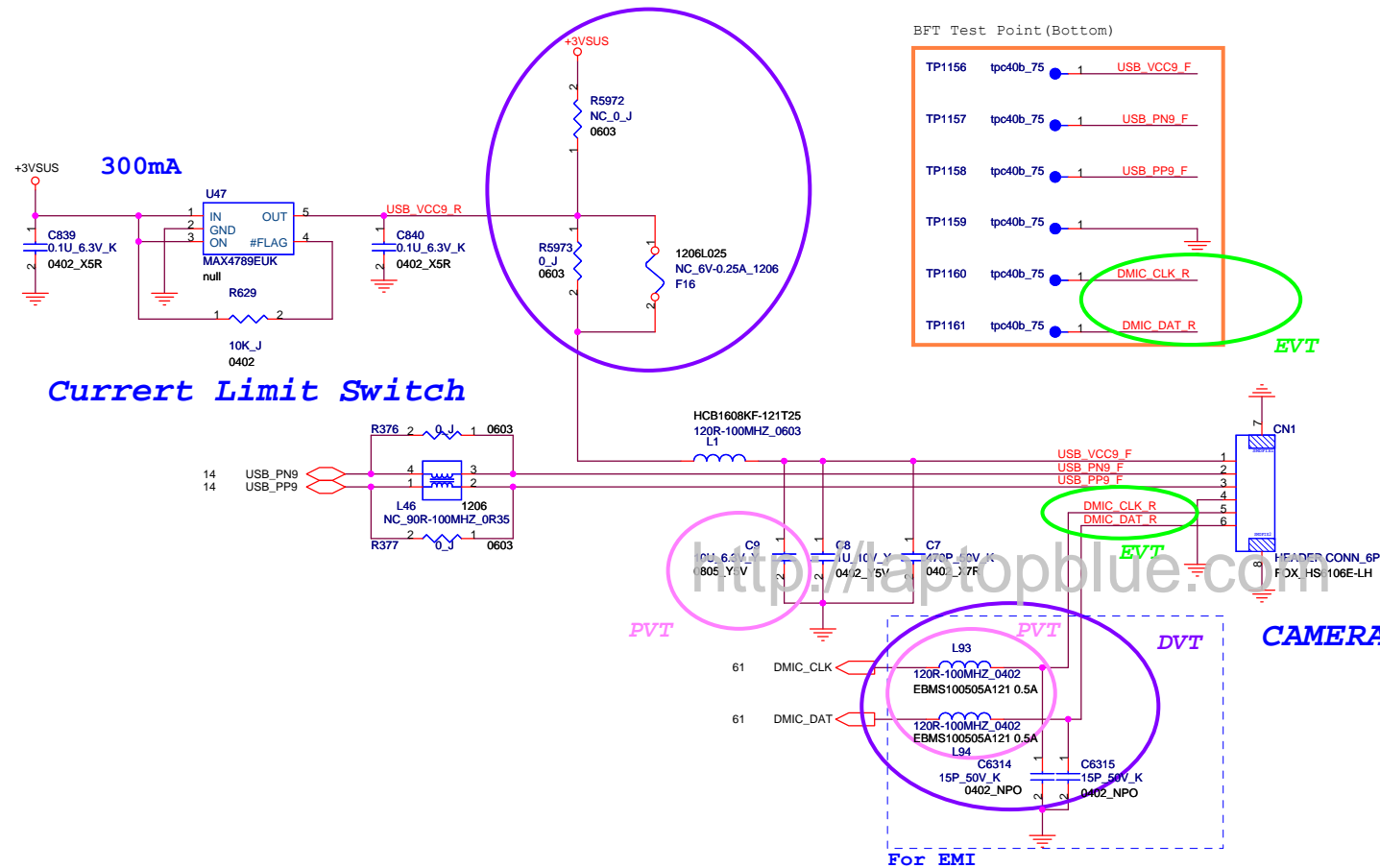




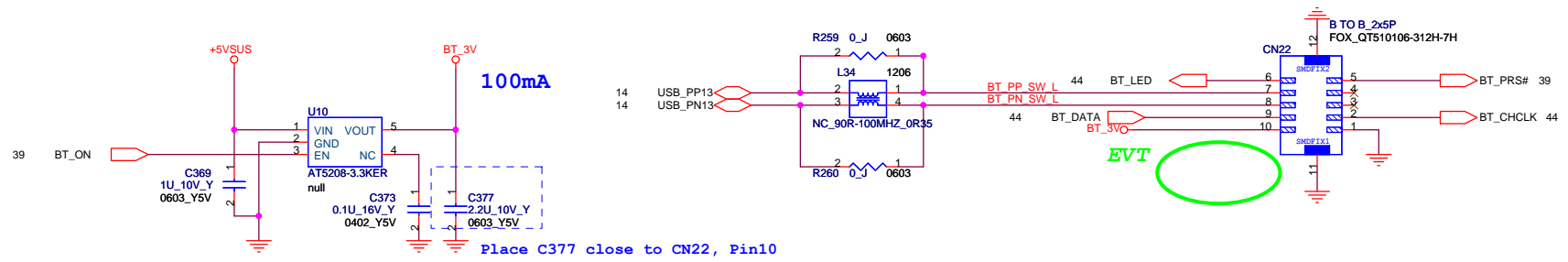


<http://laptopblue.com>





<http://laptopblue.vn>



Bluetooth CONN.

<http://laptopblue.com>

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		CCPBG - R&D Division	
Size		Document Number	
Custom		M960&M970 H Model	
Date:		Tuesday, December 29, 2009	Sheet 53 of 86
		Rev SA	

Power Test Test Point (Top)

Power Test Test Point (Top)

Power Test Test Point (Top)

PVT

BFT Test Point (Top)

PVT

TP1227 tpc60t_100 1 WIRELESS_LED_TP

TP1224 tpc60t_100 1 CHARGE_LED
TP1228 tpc60t_100 1 CHARGE_LED_TP

TP1225 tpc60t_100 1 SATA_LED#
TP1229 tpc60t_100 1 SATA_LED#_TP

TP1226 tpc60b_100 1 SD_MS_LED#
TP1230 tpc60b_100 1 SD_MS_LED#_TP

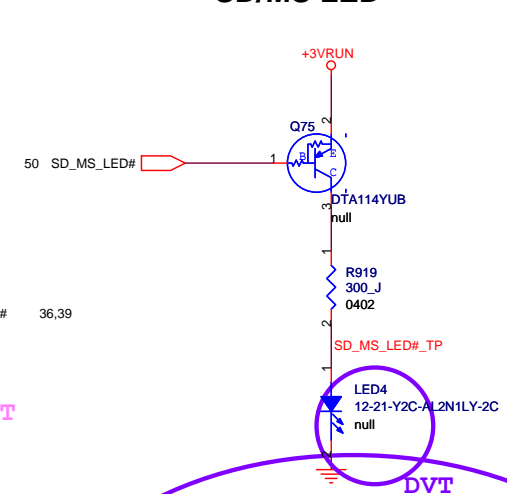
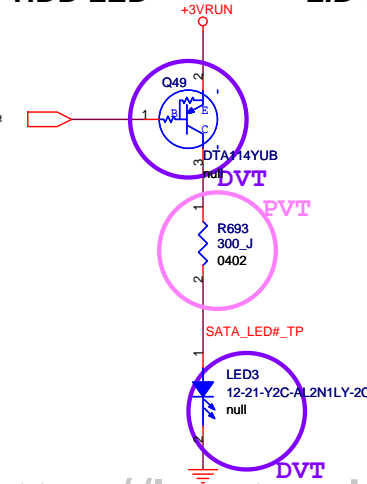
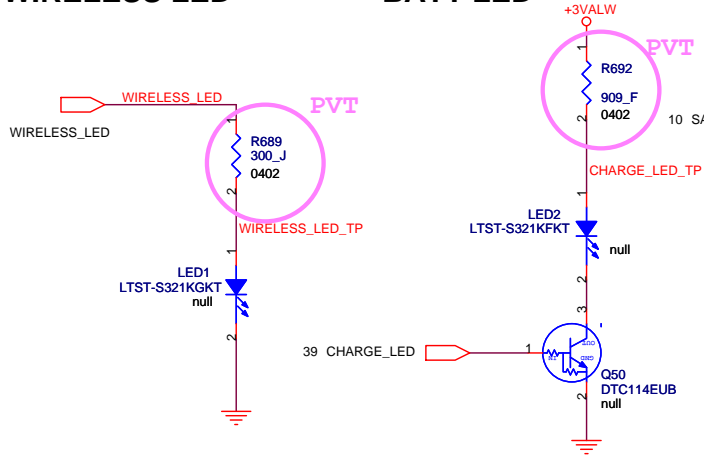
WIRELESS LED

BATT LED

HDD LED

LID Switch

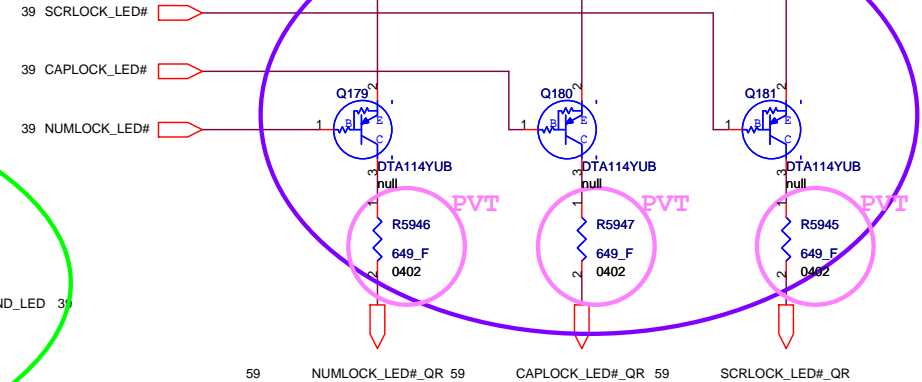
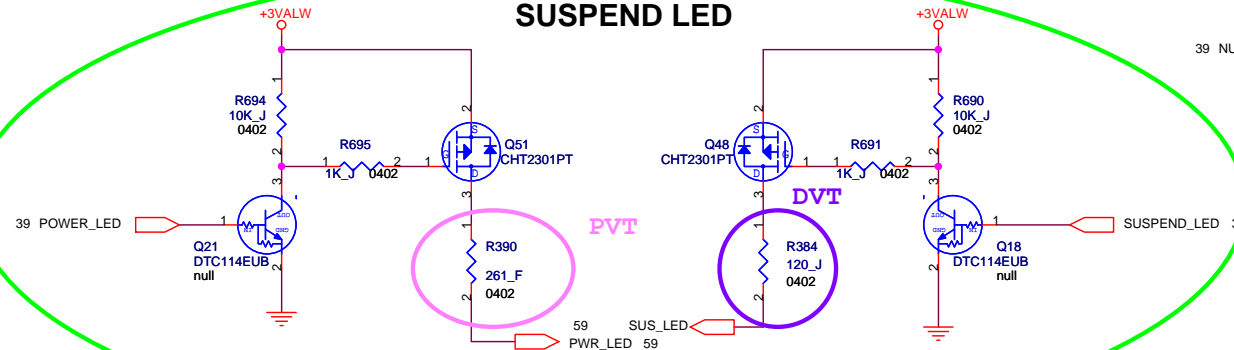
SD/MS LED



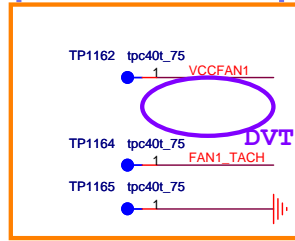
http://laptopblue.com

EVT

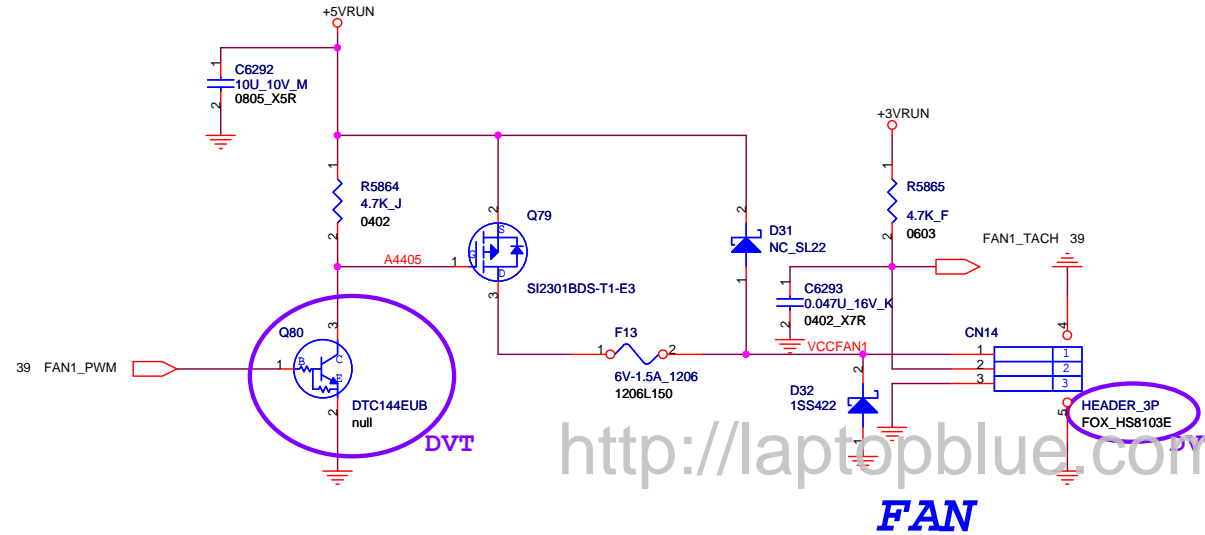
POWER LED SUSPEND LED



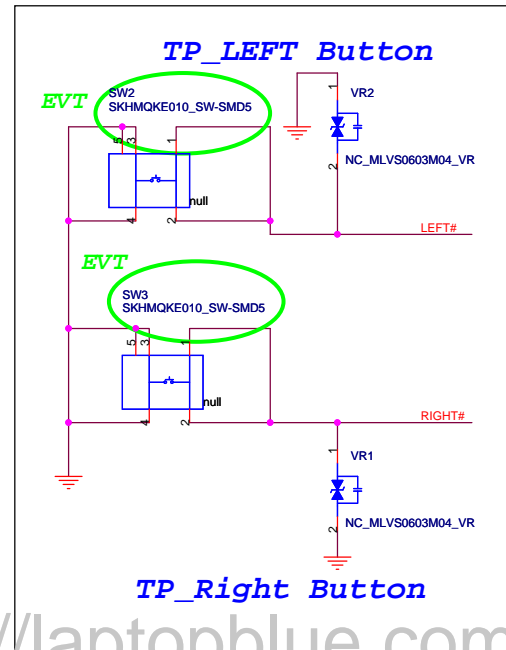
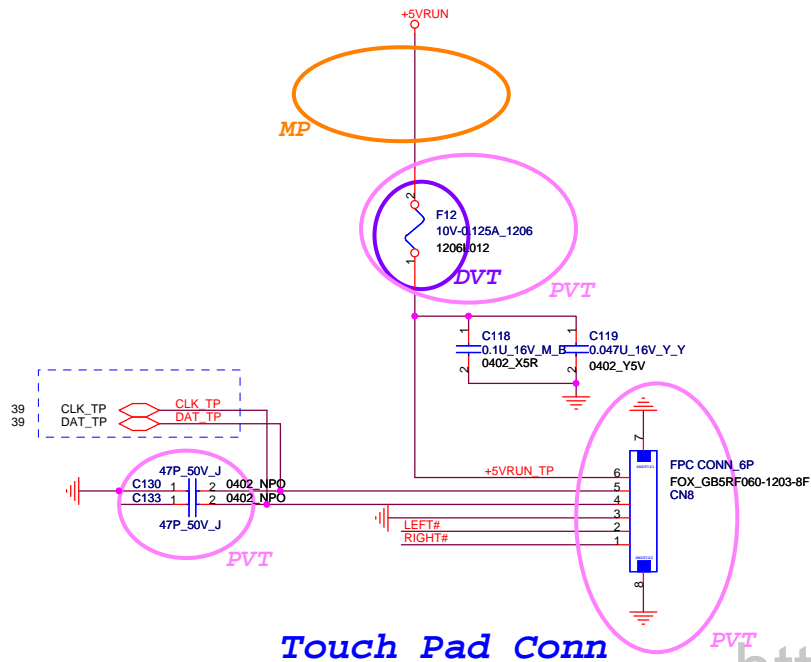
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		CCPBG - R&D Division	
Size		Document Number	
Date		Tuesday, December 29, 2009	
Sheet		55 of 86	
Rev		SA	



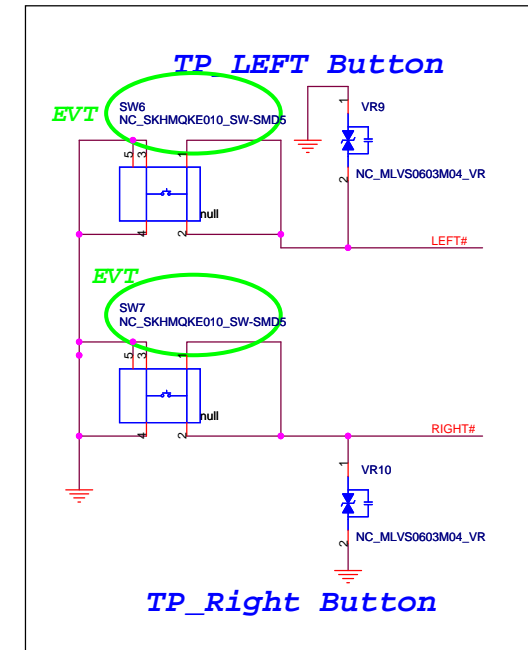
BFT Test Point(TOP)



FAN



For M960 Only



For M970 Only

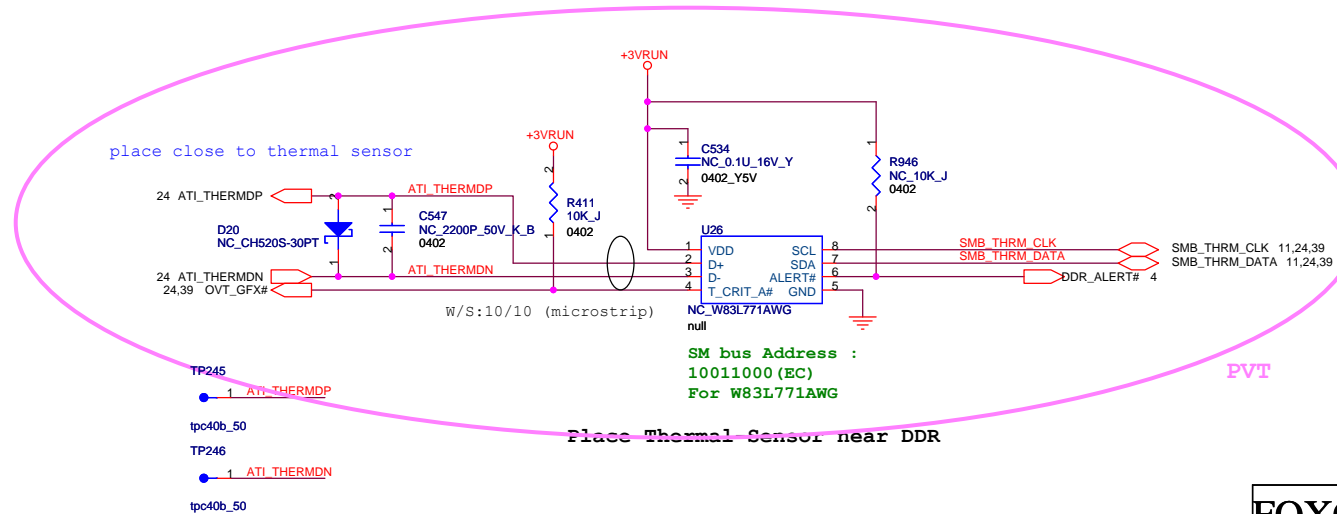
M960/M970 T/P Control Table

	SW2	SW3	SW6	SW7				
M960	Stuff	Stuff	Dummy	Dummy				
M970	Dummy	Dummy	Stuff	Stuff				

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VGA Thermal SENSOR W83L771AWG



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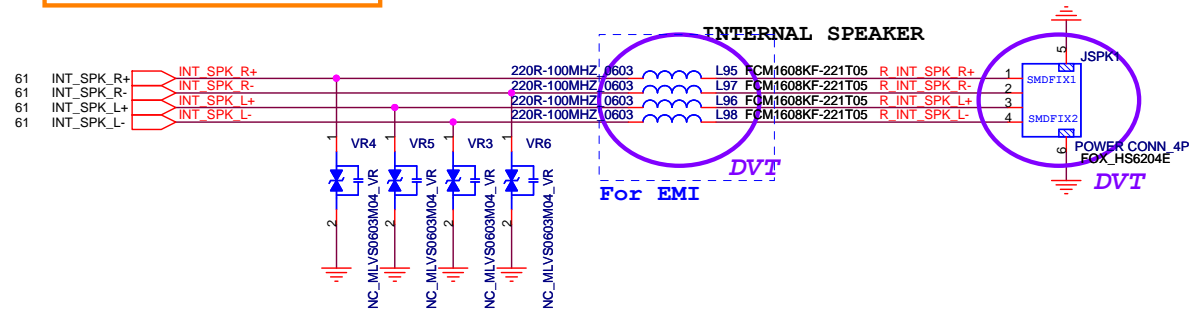


Switch DB Conn.

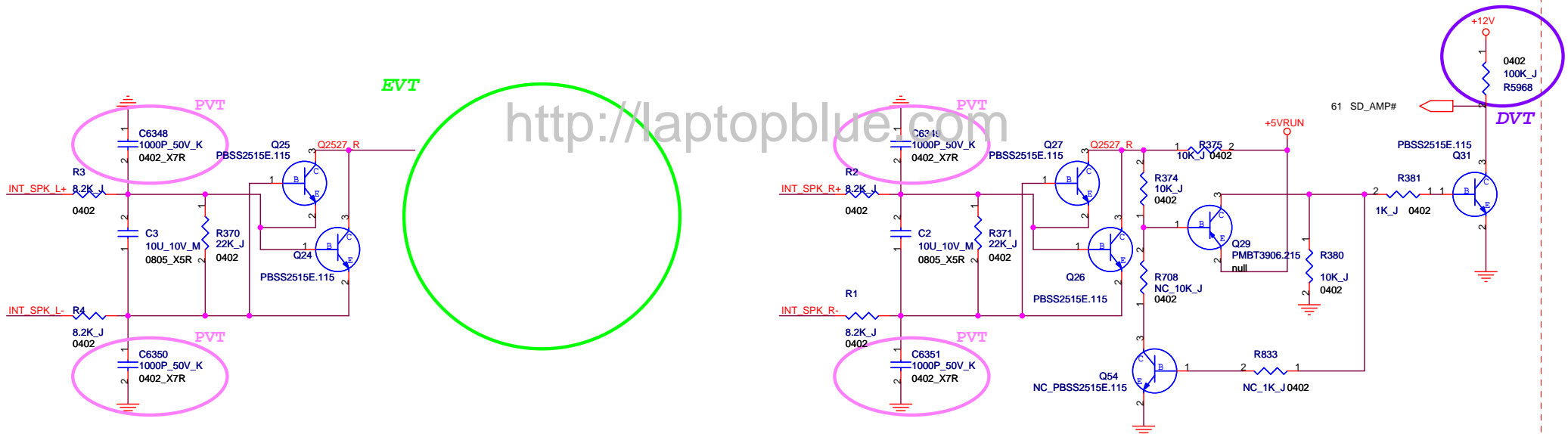
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	SWITCH DB Connector		
Size	Document Number		Rev
Custom	M960&M970 H Model		SA
Date:	Tuesday, December 29, 2009	Sheet	59 of 86

BFT Test Pad(Bottom)

TP1194	tpc40b_75	1	R_INT_SPK_R-
TP1195	tpc40b_75	1	R_INT_SPK_R+
TP1196	tpc40b_75	1	R_INT_SPK_L-
TP1197	tpc40b_75	1	R_INT_SPK_L+

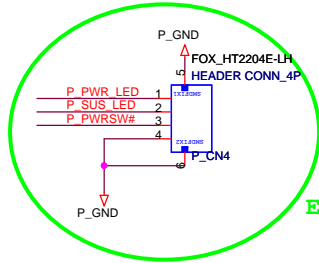


If use ALC275 Codec, for Shut-down Codec Amp. power (PVDD1 and PVDD2)

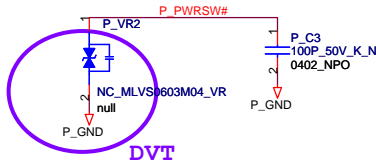


For Mor request,add the speaker cable short protection circuit

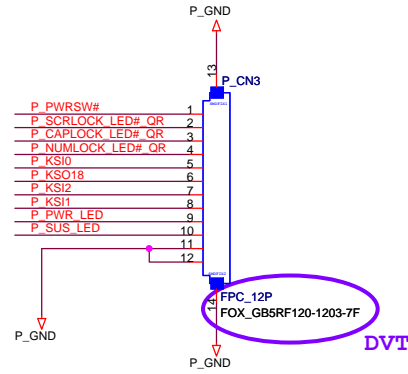
POWER BUTTON



EVT

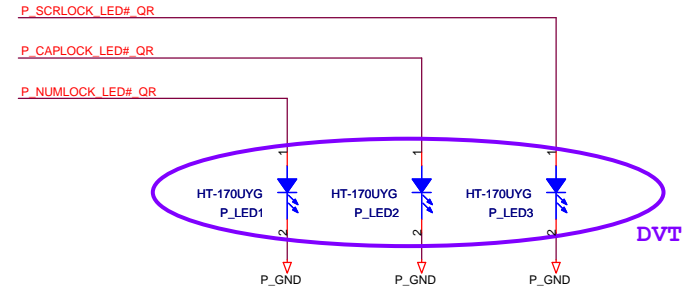


DVT

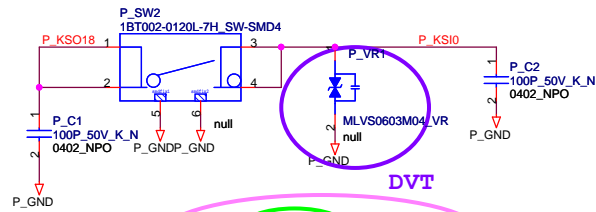


DVT

NUM LOCK LED CAP LED SCROLL LOCK LED



DVT

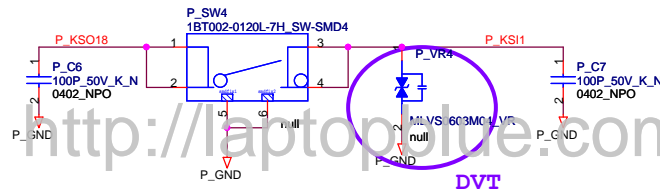


DVT

Assist

EVT

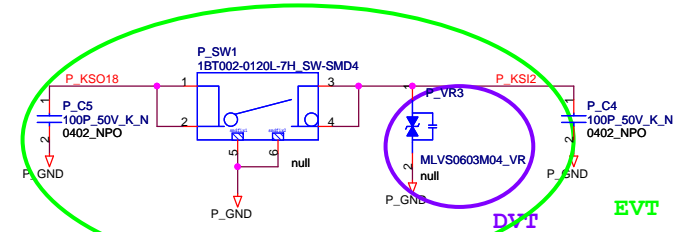
PVT



DVT

VAIO

EVT



DVT

Web(Instant On)

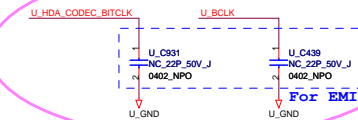
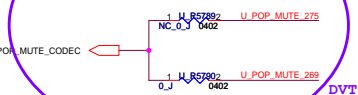
PVT

DVDD_IO can be either 1.5V or 3.3V. Resume well power, regardless iHDMI is implemented or not. However, external codec/MDC must have the same voltage level as PCH VCCSUSDA power.

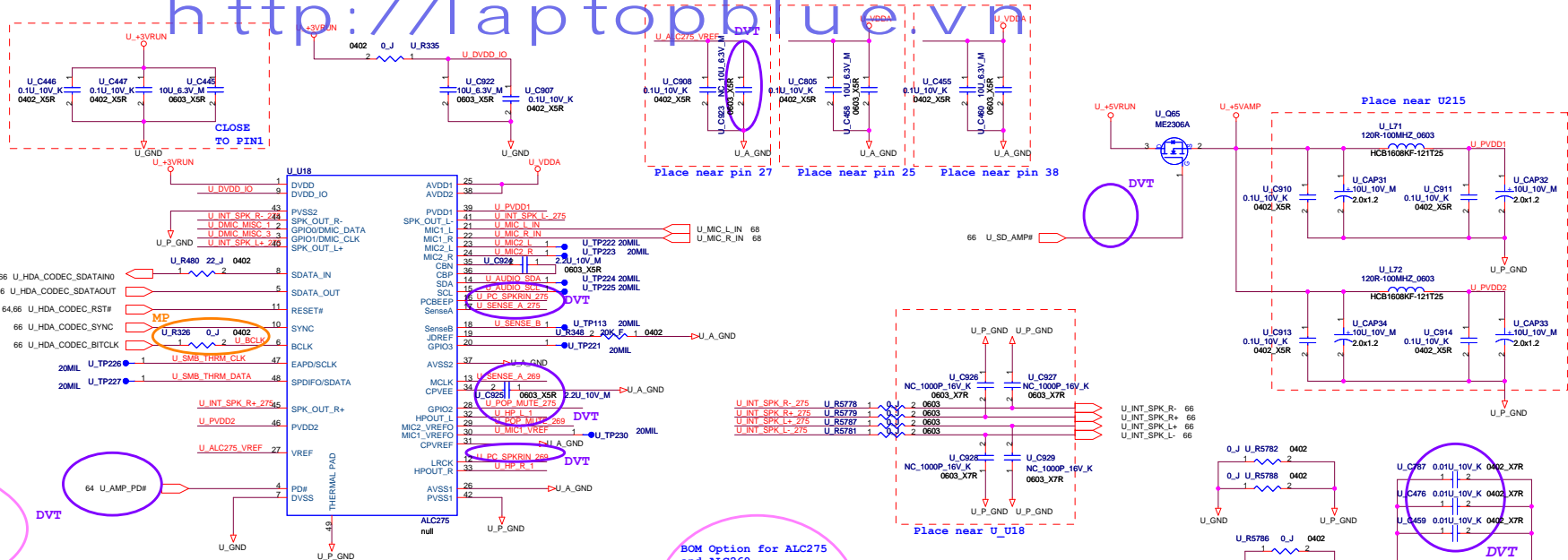
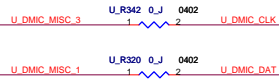
http://laptopblue.vn



BOM Option for ALC275 and ALC269 (Default is ALC269.)

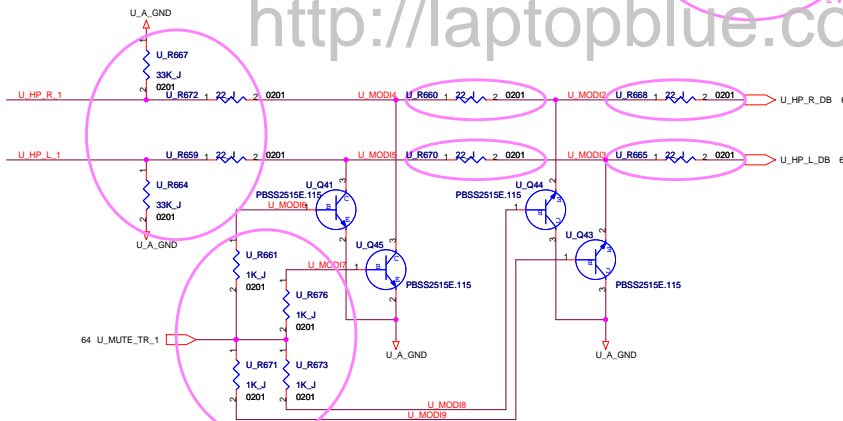


PVT

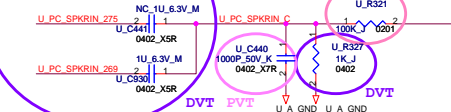


<<Attention>>
For power on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on, please let EC_MUTE# High first.
2. When you want to exit your Bios Programming Code, please let the EC_MUTE# Low. (The programming is different from before.)

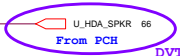
http://laptopblue.com

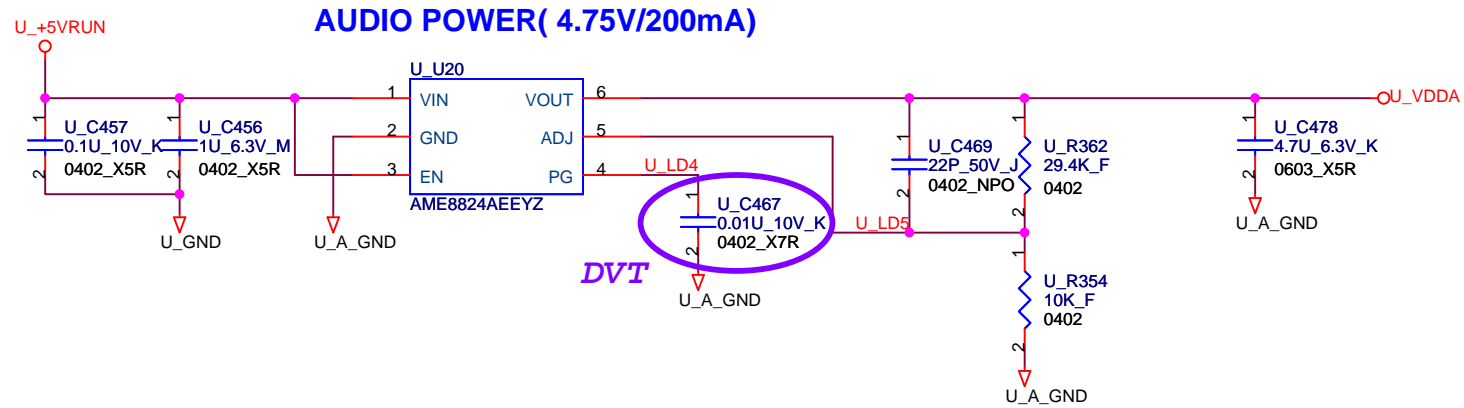


BOM Option for ALC275 and ALC269 (Default is ALC269.)



PC BEEP





The diagram illustrates a PCB layout for a laptop, showing various components and their connections. The layout is divided into two main sections: a top section for the main board and a bottom section for a sub-board.

Top Section (Main Board):

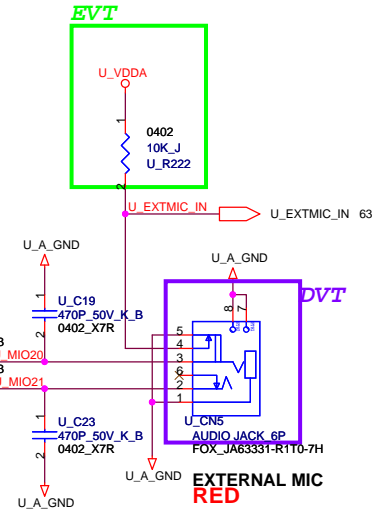
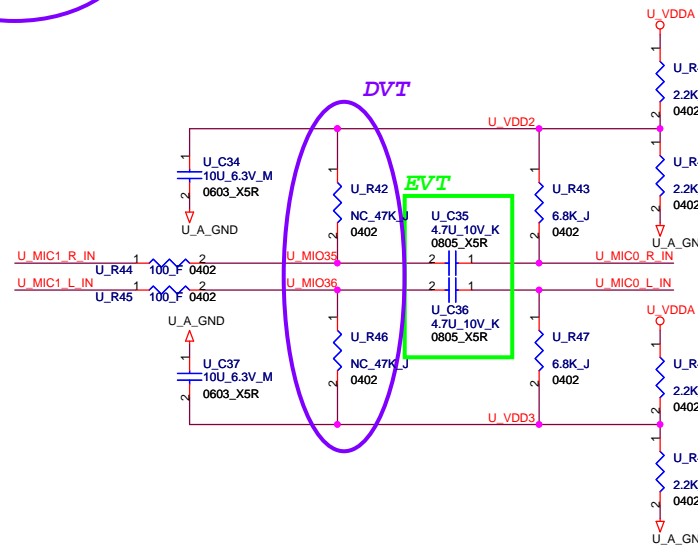
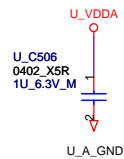
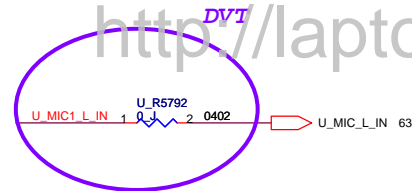
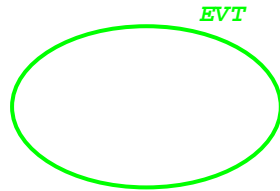
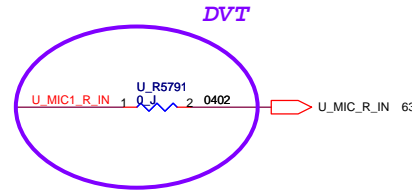
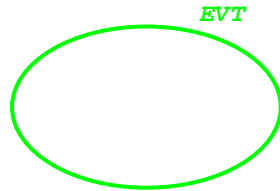
- Left Side:** Labeled with "DVT" and "EVT". It shows various pins and components, including:
 - U_+5VALW_IN (DVT)
 - U_GND
 - U_USB_PN5
 - U_USB_PP5
 - U_USB_PN1
 - U_USB_PP1
 - U_USB_PN4
 - U_USB_PP4
 - U_USB_OC#1
 - U_USB_OC#2
 - U_USB_OC#3 (DVT)
 - U_SUS_ON (EVT)
 - U_+3VALW
 - U_+3VRUN
 - U_GND
 - U_INT_SPK_R
 - U_INT_SPK_R+
 - U_GND
 - U_INT_SPK_L
 - U_INT_SPK_L+
 - U_GND
 - U_DMIC_DAT
 - U_DMIC_CLK
 - U_GND
 - U_HDA_CODEC_BITCLK
 - U_GND
 - U_SD_AMP#
 - U_HW_POP_MUTE_EC
 - U_HDA_SPKR
 - U_HDA_CODEC_SYNC
 - U_HDA_CODEC_RST#
 - U_HDA_CODEC_SDATAOUT
 - U_HDA_CODEC_SDATAIN0
 - U_+5VRUN
- Right Side:** Labeled with "PVT". It shows a vertical strip of pins and components, including:
 - U_GND
 - SN0FTX1
 - 51
 - 50
 - 49
 - 48
 - 47
 - 46
 - 45
 - 44
 - 43
 - 42
 - 41
 - 40
 - 39
 - 38
 - 37
 - 36
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 - 13
 - 12
 - 11
 - 10
 - 9
 - 8
 - 7
 - 6
 - 5
 - 4
 - 3
 - 2
 - 1
 - SN0FTX2
 - 52
 - U_GND

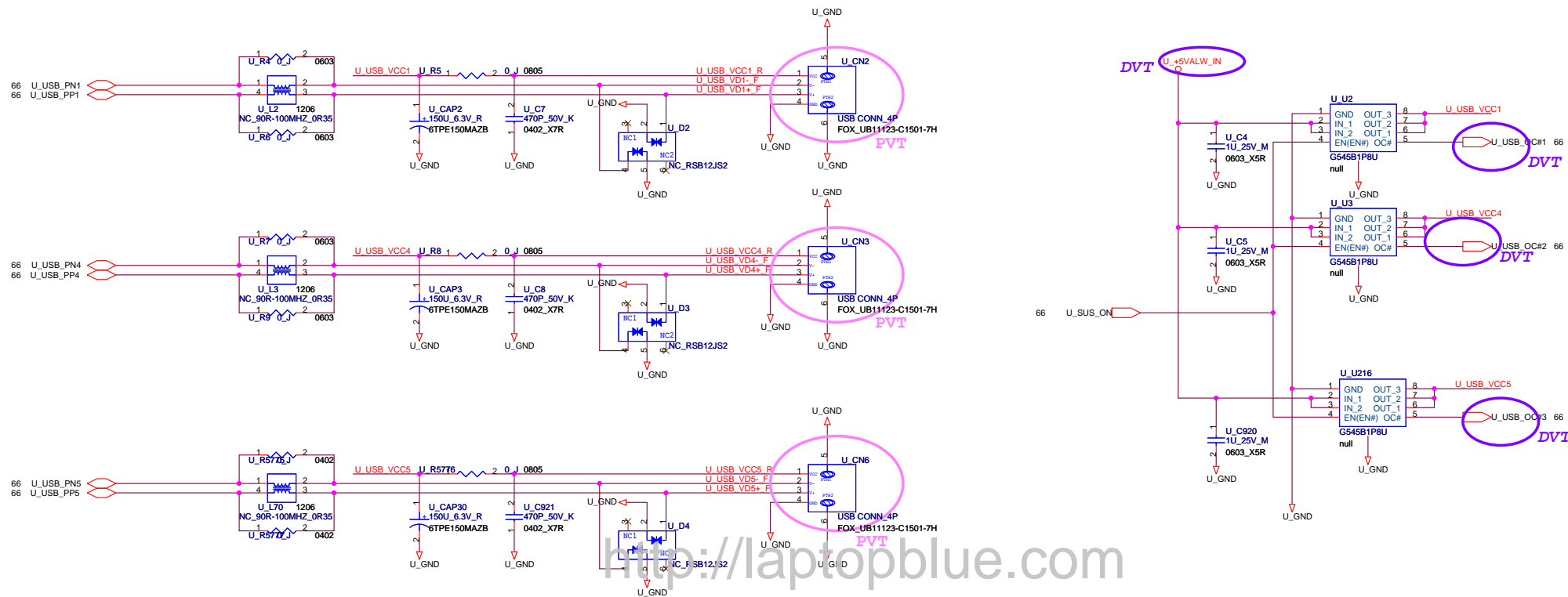
Bottom Section (Sub-board):

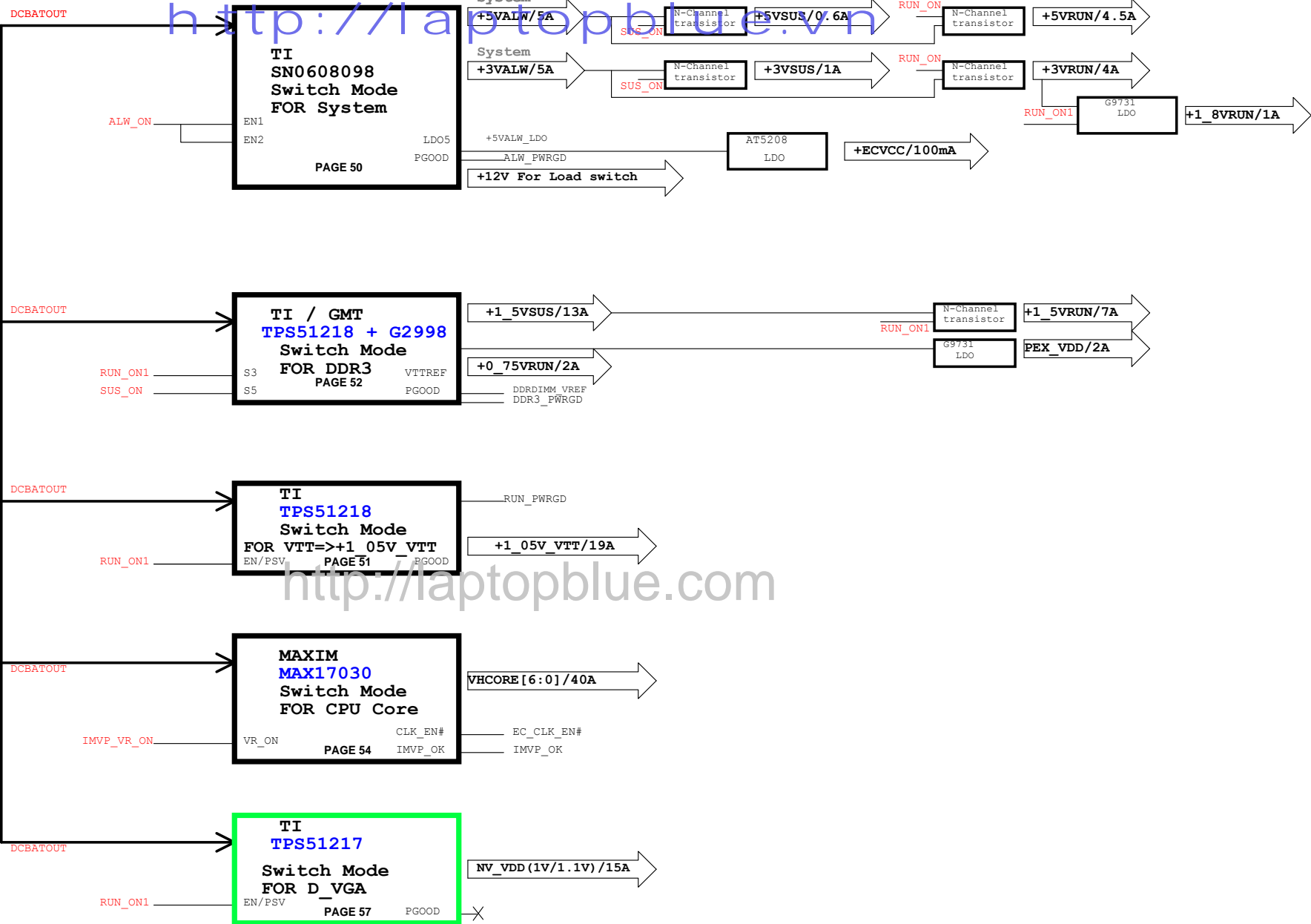
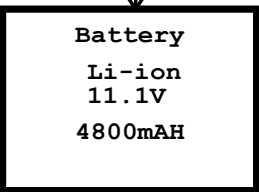
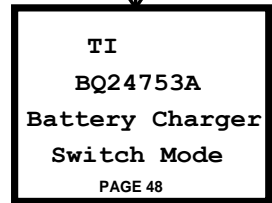
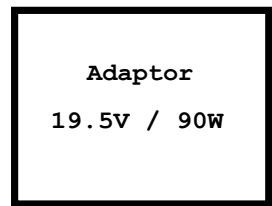
- Labeled with "PVT". It shows a smaller rectangular area with a few components, including:
 - U_+5VRUN
 - C6345
 - 0.1U_16V_M
 - 0402_X5R
 - For EMI
 - U_GND

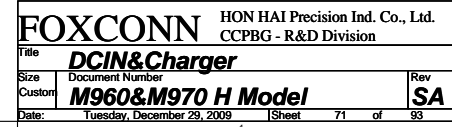
A large watermark "http://laptop" is visible across the center of the diagram.

[illegible]





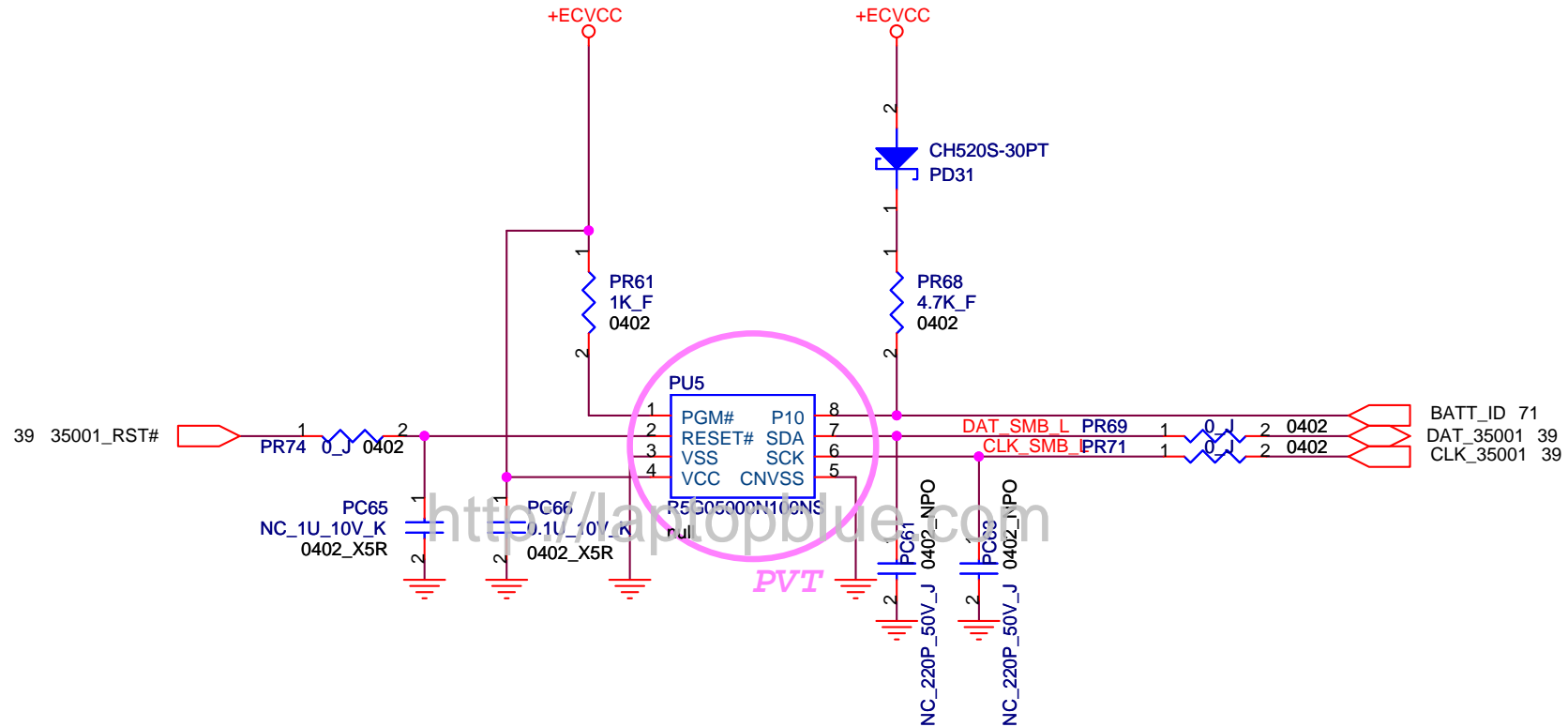




h t t p : // l a p t o p b l u e . v n

h t t p : // l a p t o p b l u e . c o m

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title		DISCHARGE CIRCUIT	
Size	Document Number		Rev
A	M960&M970 H Model		SA
Date:	Thursday, December 24, 2009	Sheet	72 of 93



FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Identify IC			
Size A	Document Number M960&M970 H Model		Rev SA
Date:	Tuesday, December 29, 2009	Sheet 73 of 93	

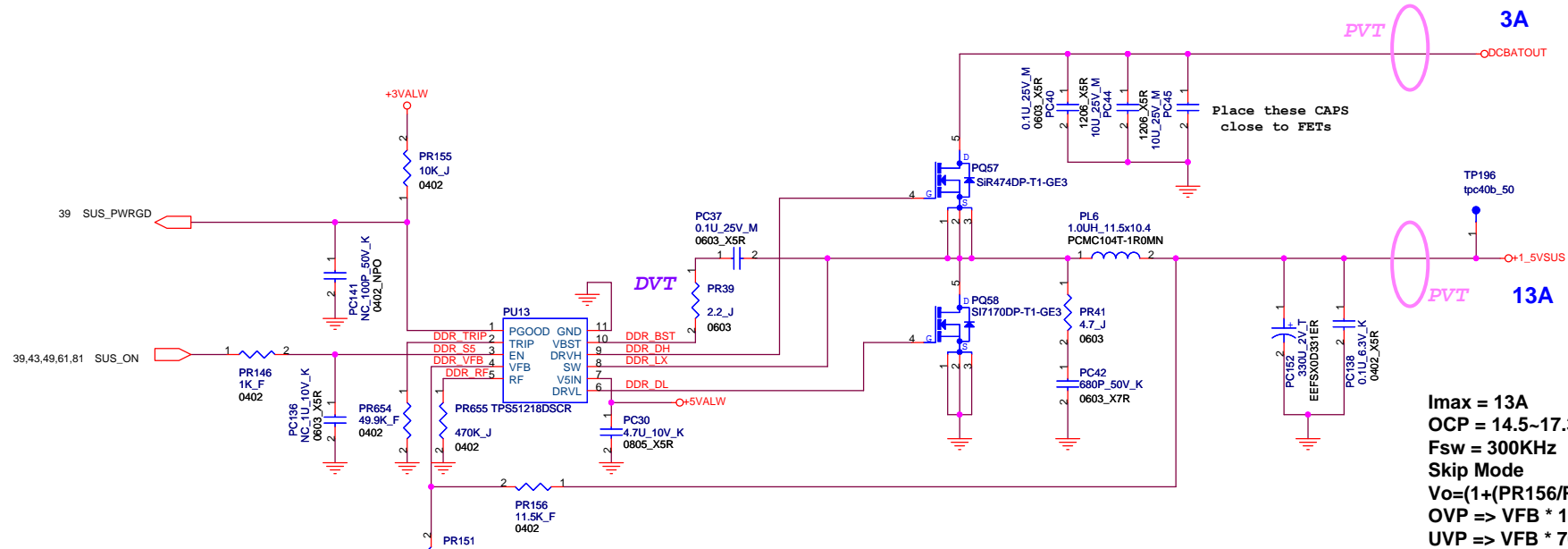
09/10/22 delete PJ22 and PJ23

PVT 3A
Place these CAPS close to FETs

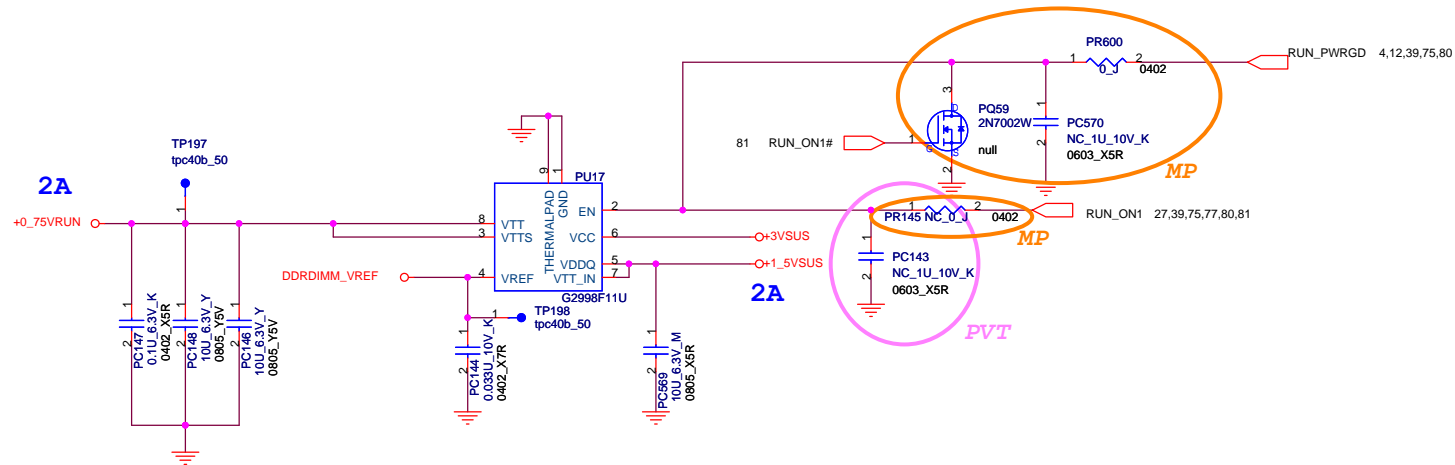
19A
PVT

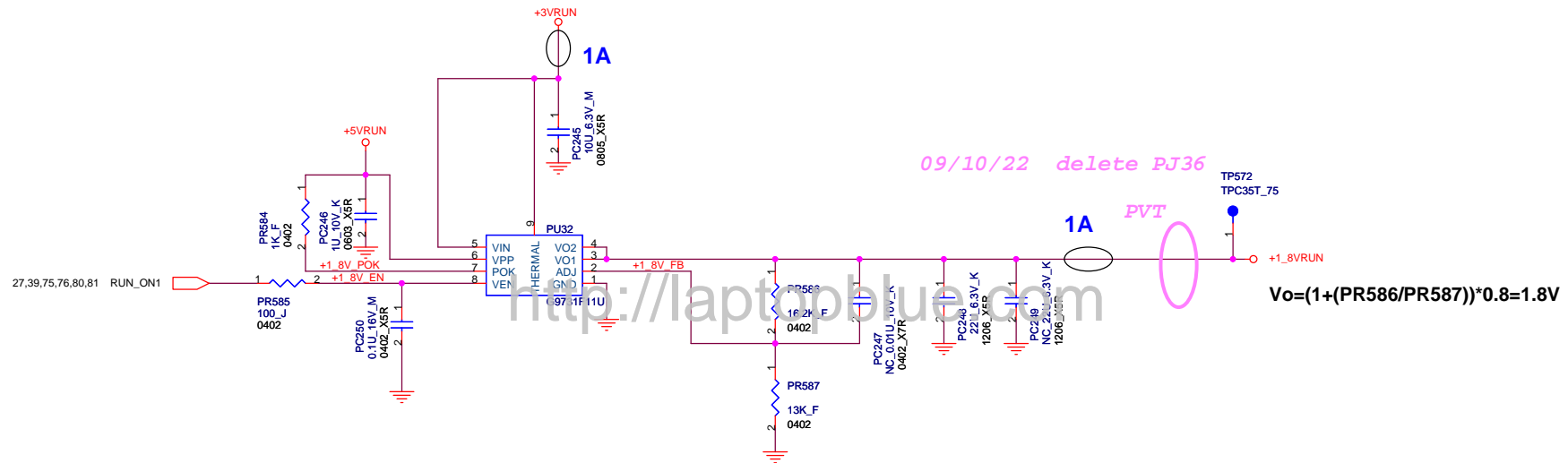
Imax = 19A
Fsw = 390KHz
Skip Mode
 $V_o = (1 + (PR187/PR208)) * 0.704 = 1.05V$
OVP => VFB * 120%
UVP => VFB * 70%

RF=470Kohm ,300KHz
200Kohm ,350KHz
100Kohm ,390KHz
47Kohm ,450KHz

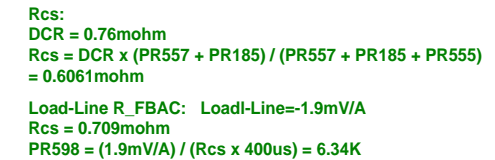


RF=470Kohm ,300KHz
 200Kohm ,350KHz
 100Kohm ,390KHz
 47Kohm ,450KHz

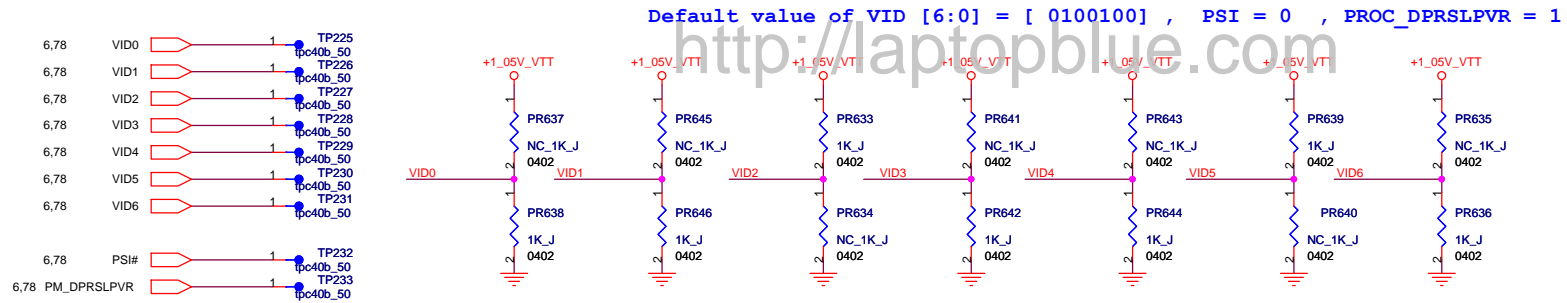




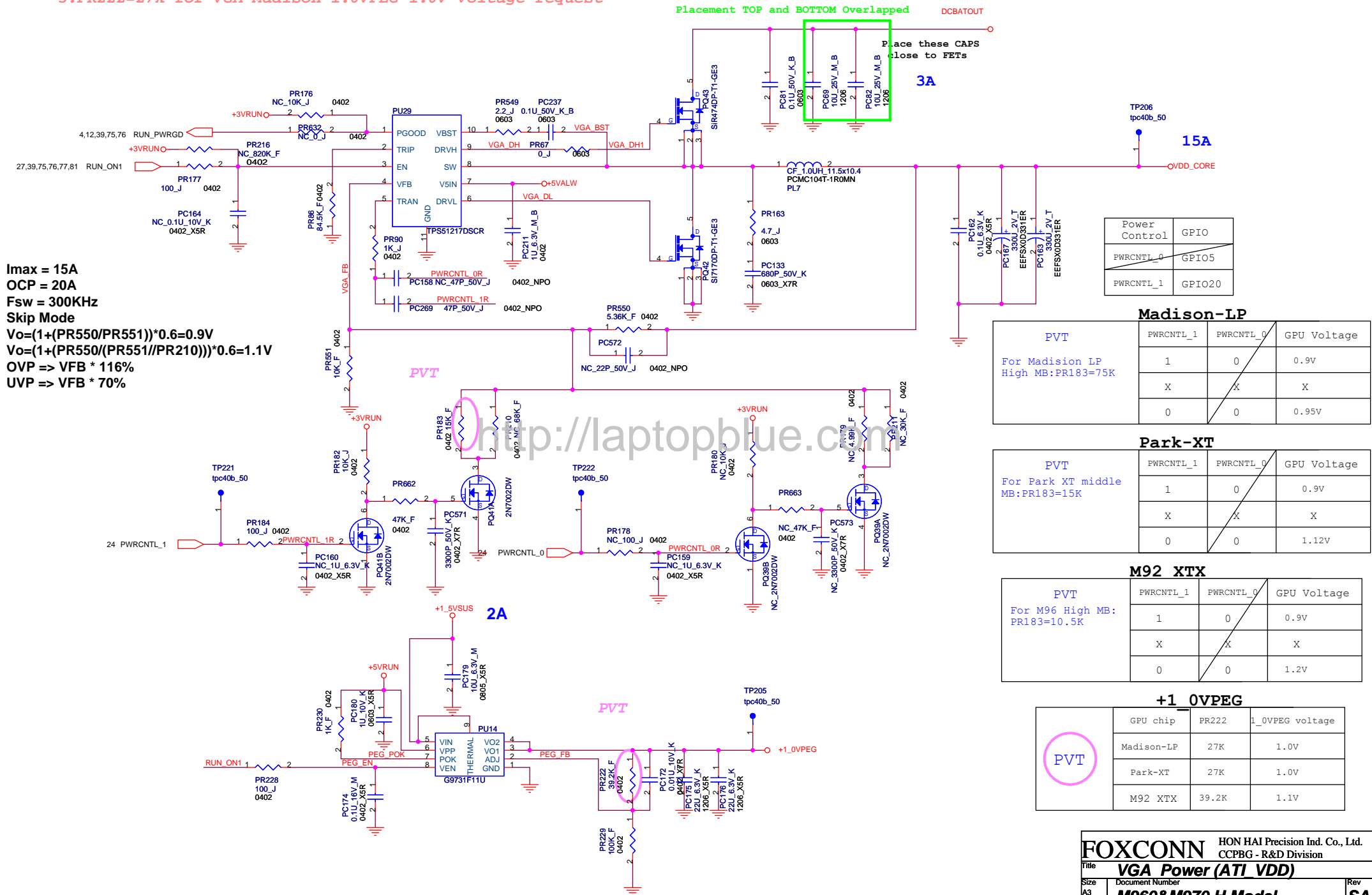
Place these CAPS
close to FETs



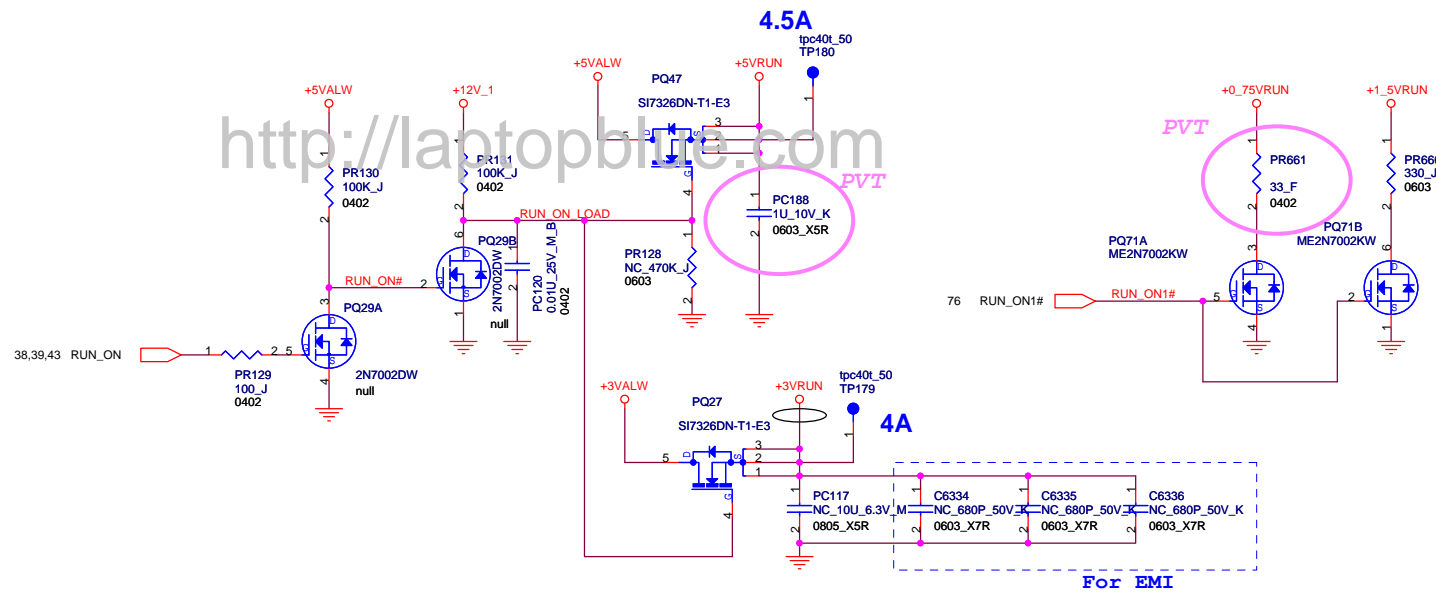
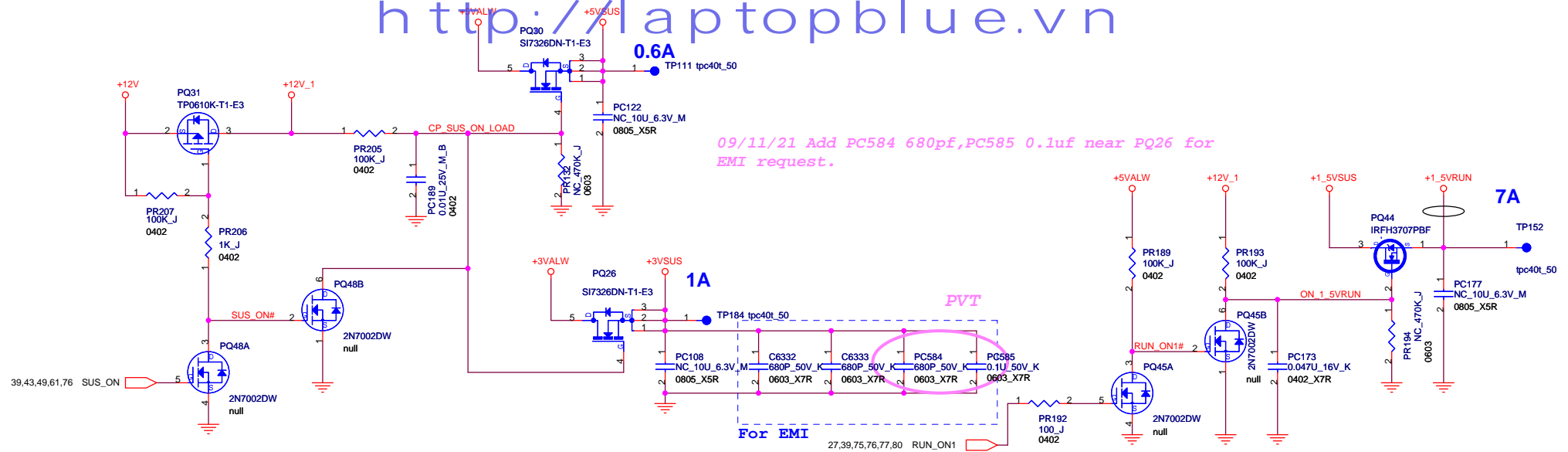
09/11/13 change pc253 from 1000P_16V_0402_X7R to
1000pF_50V_0402_X7R for MOR request

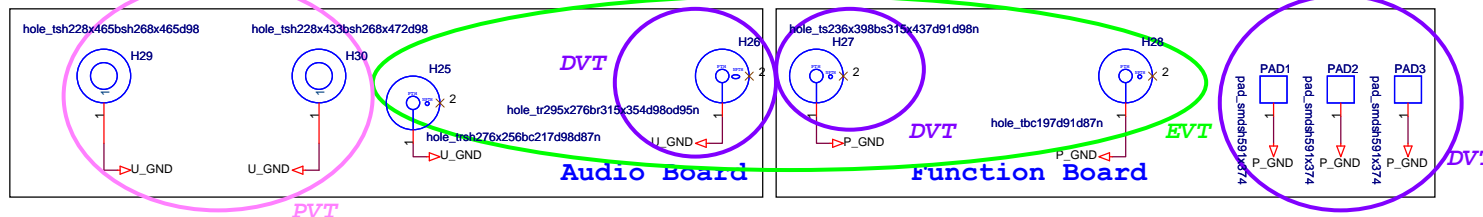
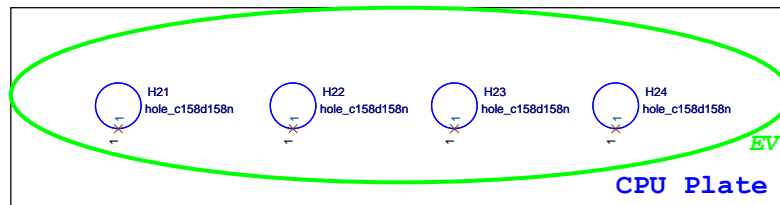
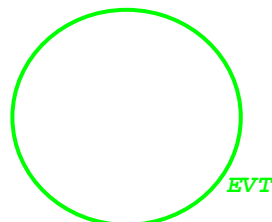
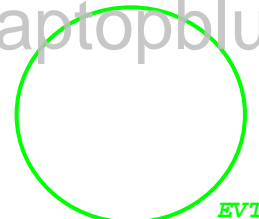
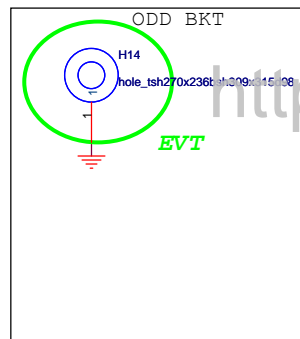
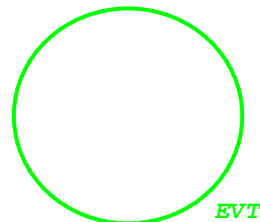
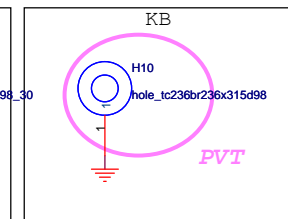
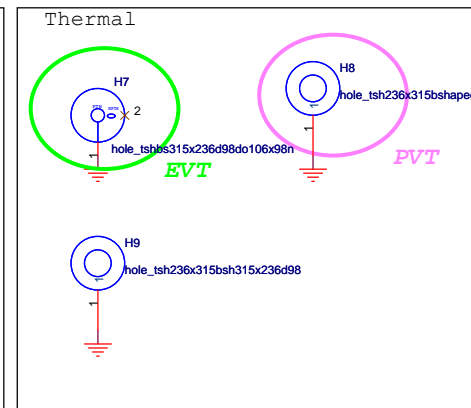
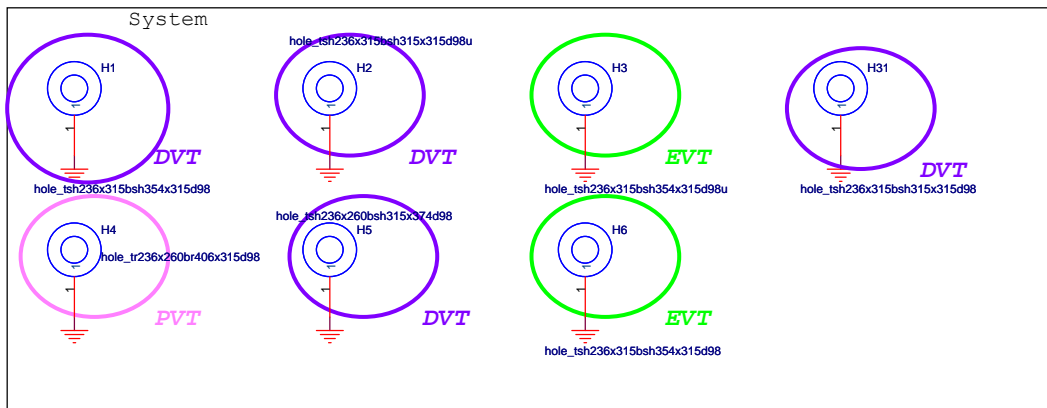
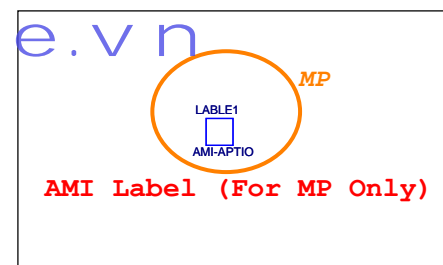
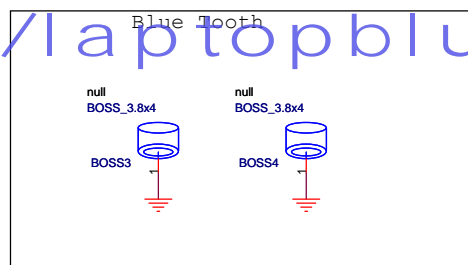
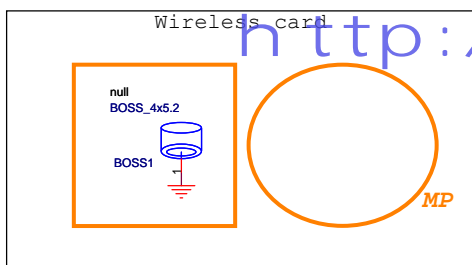
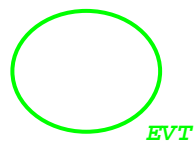


09/12/08 1.PR222=39.2k for VGA M92 XTX 1.0VPEG 1.1V voltage request
2.PR222=27k for VGA Park 1.0VPEG 1.0V voltage request
3.PR222=27k for VGA Madison 1.0VPEG 1.0V voltage request



http://laptopblue.vn





M960/M970 EVT

(2009/06/22)

- P.25 [VGA(I/O)]Delete R5858 and R5859 for needless from AMD suggestion.
- P.25 [VGA(I/O)]Connect VDD2DI to +1_8VRUN directly and delete.
- P.28 L98,C[6254:6256] for AMD suggestion.
- P.25 [VGA(I/O)]Connect A2VDD to +3V3_DELAY directly and delete.
- P.28 L12,C529,C91,C85 for AMD suggestion.
- P.28 [VGA(Power)]Delete net BIF_VDDC and C6156,C6157 for needless from AMD suggestion.
- P.28 [VGA(Power)]Change VDD3 power plan from +1_8VRUN to +3V3_DELAY from AMD suggestion.
- P.28 [VGA(Power)]Connect Ball AH29 to GND from AMD suggestion.
- P.28 [VGA(Power)]The power for DPB can be shared with DPA from AMD suggestion.
- P.28 [VGA(Power)]DPC and DPD can be powered directly without filters from AMD suggestion.
- P.40 [EC]Add R5877,R5878 for SYSTEM_ID2 used from SW's requested.

(2009/06/23)

- P.25 [VGA(I/O)]Delete R5846, R5847, R5848, R5849, R5838, R5839, R5840, C6188, C6189, U215 for needless from AMD suggestion.
- P.73 [DCIN & Charger]Add test points TP1148~TP1155 for BFT test.
- P.53 [Camera Connector]Add test points TP1156~TP1161 for BFT test.
- P.57 [FAN]Add test points TP1162~TP1165 for BFT test.
- P.35 [LAN]Add test points TP1166~TP1181 for BFT test.
- P.43 [Debug Port]Add test points TP1186~TP1193 for BFT test.
- P.61 [AUDIO Speaker Conn]Add test points TP1194~TP1197 for BFT test.
- P.41 [KB Connector]Add test points TP1198~TP1207 for BFT test.
- P.60 [SWITCH DB Conn.]Add test points TP1208~TP1211 for BFT test.
- P.73 [DCIN&Charger]Add test points TP1212~TP1218 for BFT test.
- P.41 [KB Connector]Del CN4 because M960 and M970 KB connectors are decided to co-use.
- P.67 [AUDIO Speaker AMP]Del this page because AMP is combined with ALC275
- P.39 [PCIE (MS&LINK)]Change the net name from "SDMS_VCC" to "VCC_MS" because this net is for MS power only.
- P.26 [VGA (Memory BUS) 4/6]Change the power source from +1_8VRUN to +1_5VRUN because the power source of DDR3 VRAM is +1_5VRUN.

(2009/06/24)

- P.23 [CRT]Add and NC Q11,D9,R469,C279,R767,U9 for Semi-PNP.
- P.39 [HDMI]Del C100,C107,C105,C106,C108,C109,C111,C112 for redundant design.
- P.10 [PCH (HDA,JTAG,SAT)]Del R302 for redundant design.
- P.24 [VGA (Strap) 2/6]Change net name "ATI_DVPDATA[23:20]" to ATI_DVPDATA[3:0] for AMD recommend.
- P.24 [VGA (Strap) 2/6]Del R5767,R5768 for AMD recommend.
- P.25 [VGA (I/O) 3/6]Del R5837 for AMD recommend.
- P.26 [VGA (Memory BUS) 4/6]Add C6105,C6106,R5871,R5872 for AMD recommend.
- P.13 [PCH (LVDS,DDI)]Del R1571 and place TP1219 on DDPD_HPDI because this pin is not necessary for pull-low to GND.
- P.55 [Felica Connector]Del F14,R5874,R5875 because the F14 related circuit is out of Felica spec.
- P.55 [Felica Connector]Stuff C869,U48,R630,C845 because F14 related circuit is out of Felica spec.
- P.72 [DCIN&CHARGE]Change DC-IN current form 8A to 5A.
- P.72 [DCIN&CHARGE]Change PD7 from SMD15C to TVS2315PT.
- P.74 [Identify ID]Change PC61 from 1uF 10V k to 220Pf 50v J, then NC PC61.
- P.76 [VTT&PCH Power(+1_05V)]Change PR116 from 100k to 470k.
- P.77 [DDR3 Power(+1_5V/+0_75V)]Change PR655 from 100k to 470k.
- P.79 [CPU Power_VHCORE]Delete PC67,PC155.
- P.82 [Other plane power]Change PQ29,PQ45,PQ48: from 2N7002DW to 2N7002SPT.
- P.93 [OVP protection]Change PC41 from 0.01uF to 1000Pf.

(2009/06/25)

- P.46 [Mini-PCIE Card (WLAN)]Add R5901 on WLAN_EN for RF VEDS test.
- P.23 [VGA (PCI-E) 1/6]NC R5831 for AMD M96.
- P.26 [VGA (Memory BUS) 4/6]NC R5798,R5800,R5799,R5802,R5803,R5804 for AMD M96.
- P.26 [VGA (Memory BUS) 4/6]NC R5779,R5880 for AMD M96.
- P.28 [VGA (Power) 6/6]NC L90,C6196,C6194,C6195,C6192,C6193 for AMD M96.
- P.28 [VGA (Power) 6/6]NC L91,C6197,C6194,C6199,C6200 for AMD M96.
- P.28 [VGA (Power) 6/6]NC L26 for AMD M96.
- P.28 [VGA (Power) 6/6]Add L30 and connect between VDD_CORE and SPV10 for AMD M96.
- P.28 [VGA (Power) 6/6]NC L92,C6233,C6234,C6236 for AMD comment.
- P.28 [VGA (Power) 6/6]NC L96,L97,C6248,C6251,C6249,C6252,C6250,C6253 for AMD comment.
- P.26 [VGA (Memory BUS) 4/6]Change C6100 from 2200P to 1U for AMD comment.
- P.28 [VGA (Power) 6/6]NC R5833,R5834 because M96 not support for PowerXpress.
- P.28 [VGA (Power) 6/6]Add R587 and connect to GND for PowerXpress function of Park and Madison.
- P.29 [VRAM(DDR3)# 1/4]Change R4030,R4019,R4027,R4028 from 1.33K to 4.99K for AMD comment.
- P.29 [VRAM(DDR3)# 1/4]Add R5874,R5875,C6303 for AMD comment.
- P.63 [SWITCH (Bottom & KB LED)*]Change P_VR1,P_VR2,P_VR3,P_VR4,P_VR5 for EMC team request.
- P.20 [DDRIII(SO-DIMM_0) 1/2]Del SPRI,J1.
- P.20 [DDRIII(SO-DIMM_0) 1/2]Connect CN34 207 Pin to GND.
- P.21 [DDRIII(SO-DIMM_0) 2/2]Connect CN35 G2 Pin to GND.
- P.46 [LAN (88E8057) 1/2]Del R1462 for Marvell comment.
- P.46 [LAN (88E8057) 1/2]NC C997,R94 for Marvell comment.
- P.37 [Inverter Connector]Add U89C,R809,R684,C902,R772 for MOR's request.
- P.37 [Inverter Connector]Change the off-page from "BL_OFF#" to "INV_EN" for MOR's request.
- P.37 [Inverter Connector]Add U89A,U89B,C877,R687 for MOR's request.
- P.37 [Inverter Connector]Add an off-page of BL_OFF# on U89D for MOR's request.
- P.38 [LVDS Connector]Change the off-page of 35/36 pin of CN13 to INV_BRADJ/INV_ENABLE for MOR's request.
- P.10 [PCH (HDA,JTAG,SAT)]Add R5905 to let JTAG_TCK pull down for MOR's request.
- P.11 [PCH (PCI-E,SMBUS,CLK)]Add R539,R540 to let PCIECLKRQ3#,PCIECLKRQ4# to pull high to +3VVRUN for MOR's request.
- P.11 [PCH (PCI-E,SMBUS,CLK)]Add R579 to connect WLAN_CLKREQ# to +3VSUS for MOR's request.
- P.11 [PCH (PCI-E,SMBUS,CLK)]NC R577 for MOR's request.
- P.14 [PCH (PCI,USB,NVRAM)]Change Bluetooth function from port 13 to port10 to meet Freedom Project Product Specifications.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Del GPIO39 related circuit because this pin is for LCDID3
- P.51 [PCIE (MS&LINK) 1/2]Delete i-Link function from Freedom_specV0.6.

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title History(1)			
Size A3	Document Number M960&M970 H Model		Rev SA
Date:	Thursday, December 24, 2009	Sheet 84 of 86	

M960/M970 EVT

(2009/06/26)

- P.19 [CLOCK GEN]Change U31 from SL28748ALC to SL28748CLC.
- P.14 [PCH (PCI,USB,NVRAM)]Del USB_PN12,USB_PP12 off-page and add TP365,TP452 on tha same ports.
- P.45 [Mini-PCIE Card (WLAN)]Del U45,C891 for disable WIMAX function
- P.45 [Mini-PCIE Card (WLAN)]NC 36pin,38pin of CN12 for disable WIMAX function
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Add an off-page "LCDID4" on GPIO48 and change the net name to LCDID4 for LCDID[4:0].
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Del R5867 for LCDID[4:0].
- P.63 [SWITCH (Botton & KB LED)*]Del "VAIO" button from Freedom Project Product Specifications V0.6.
- P.63 [SWITCH (Botton & KB LED)*]Change the button names "Web" and "Display Off" to "Instant On" and "VAIO" from Freedom Project Product Specifications V0.6.
- P.51 [PCIE (MS&iLINK) 1/2]Connect TPB+/- to GND and NC TPA0/TPAN0/TPBIAS0 to disable i-Link function for Realtek comment.
- P.51 [PCIE (MS&iLINK) 1/2]Add R1468 and NC it to disable i-Link function for Realtek comment.
- P.12 [PCH (DMI,FDI,GPIO)]Connect SYS_PWROK line to ALW_PWRGD through D33 for MOR's request.
- P.44 [Express Card]Add R5457 between the gate and the source of Q38 for MOR's request.
- P.68 [AUDIO (Head Phone Jack)*]Add U_R220 pull-high to U_VDDA on U_HP_IN_5 for Realtek comment.
- P.68 [AUDIO (Head Phone Jack)*]Change U_GND ground to U_A_GND for Realtek comment.
- P.69 [AUDIO (Ext MIC Jack)*]Add U_R221 pull-high to U_VDDA on U_EXTMIC_IN for Realtek comment.
- P.69 [AUDIO (Ext MIC Jack)*]Change U_C35/U_C36 to 4.7u X5R for Realtek comment.
- P.84 [HOLE & AMI LABEL]Add H1~H20 for ME request.
- P.25 [VGA (I/O) 3/6]Add 10K ohm resistors to let ATI_JTAG_TFSTE,ATI_JTAG_TDI,ATI_JTAG_TCLK,ATI_JTAG_TMS,ATI_JTAG_TDO pull up to +3V3_DELAY.

(2009/06/29)

- P.68 [AUDIO (Head Phone Jack)*]Change U_A_GND which is connected to U_C9 pin2 to U_GND.
- P.72 [DCIN&Charger]Change PCN1 connector to BP91071-B51E3-7H for ME request.
- P.50 [eSATA Combo Conn.]Change CN27 connector to 3Q38111-R21C3-8H for ME request.
- P.58 [Touch Pad]Change SW2/SW3/SW6/SW7 to 19-SKRPABE-1000 for ME request.
- P.22 [Braidwood Connector]Change NC39 to 1N-0078002-F1G0 for ME request.
- P.51 [PCIE (MS&iLINK) 1/2]Del R1468 and connect XOUT to U71 A2 for Ricoh's comment.
- P.28 [VGA (Power) 6/6]NC AH29 U204E for AMD's comment.
- P.16 [PCH (POWER) 1/2]Change R366,R325 to 100 ohm for Intel'comment.
- P.16 [PCH (POWER) 1/2]Change C141 to 1U for Intel'comment.
- P.09 [ARD (RESERVED)]Change R1274 to 3.3K for Intel's comment.

(2009/06/30)

- P.25 [VGA (I/O) 3/6]Change JTAG_TCK to pull-low to GND through a 10K ohm resistor for MOR's request.
- P.25 [VGA (I/O) 3/6]Del R5910 for MOR's request.
- P.25 [VGA (I/O) 3/6]NC R5906,R5907,R5908,R5909 for MOR's request.
- P.26 [VGA (Memory BUS) 4/6]Del C6105,C6106,R5879,R5880 for MOR's request.
- P.28 [VGA (Power) 6/6]Del R5802,R5803 and connect DPE_VDD18/DPE_VDD10 to DPF_VDD18 [2:1]/DPF_VDD10 [2:1] for MOR's request.
- P.28 [VGA (Power) 6/6]Del L96/C6248/C6249/C6250/L97/C6251/C6252/C6253 for MOR's request.
- P.80 [CPU Power_VID]Stuff PR638,PR646 for Power request.
- P.80 [CPU Power_VID]NC PR637,PR645 for Power request.
- P.28 [VGA (Power) 6/6]Del L80/C859/C858/C860/L81/C862/C861/C6291/L82/C6165/C6164/C866 for MOR's comment.

- P.45 [Mini-PCIE Card (WLAN)]Del R824 for MOR's request.
- P.12 [PCH (DMI,FDI,GPIO)]Change R911 to 10K for MOR's request.
- P.54 [Bluetooth Connector]Del C378 for MOR's request.
- P.28 [VGA (Power) 6/6]Del L6,Q7,Q9,R5828,R5829,R5830 because M960/M970 do not use BBP function.
- P.45 [Mini-PCIE Card (WLAN)]NC CN12 15pin and del R18 for RF request.
- P.56 [Status LED & LID]Add LED6/LED7/LED8/LED9 for M970 only.
- P.45 [Mini-PCIE Card (WLAN)]Add R17 and NC it for MOR's request.

(2009/07/01)

- P.25 [VGA (I/O) 3/6]Del TP1104,TP1105,TP1106,TP1230 because these test points are redundant.
- P.28 [VGA (Power) 6/6]Change net name DPE_VDD18/DPE_VDD10 to DPEF_VDD18/DPEF_VDD10 for the co-use power DPE_VDD/DPF_VDD.
- P.84 [HOLE & AMI LABEL]Del BOSS9,BOSS10 for ME request.
- P.84 [HOLE & AMI LABEL]Add CPU hole H21,H22,H23,H24 for CPU socket.
- P.50 [eSATA Combo Conn.]Del eSATA repeater schematic (U214,C766,C776,C759,C745,R5754,R5835,R5756,R5755,R5757,R5758,R5759,C718,C387) for over-design.
- P.10 [PCH (HDA,JTAG,SAT)]Change SPI_CLK_SW/SPI_MOSI_SW/SPI_MISO_SW to SPI_CLK_L/SPI_MOSI_L/SPI_MISO_L for modifying the SW reserve design.
- P.28 [VGA (Power) 6/6]Del R5833,R5834,R5837 and connect U204F AL21 to GND because M960/M970 do not have PowerXpress function.
- P.25 [VGA (I/O) 3/6]Add two connection ATI_LVDS_SCL/ATI_LVDS_SDA to CN13 5/6 pin and pull-high 4.7K to +3V3_DELAY for SW request to add EDID function.

(2009/07/02)

- P.38 [LVDS Connector]Connect CN13 Pin1 to LCDVCC for LCD power supply.
- P.38 [LVDS Connector]Connect CN13 Pin34 to GND for LCD power supply.
- P.51 [PCIE (MS&iLINK) 1/2]NC R820/C868/R817/C865/R818/C864 because SD_CD#/SD_WP#/MS_CD# has an internal pull-up resistor and the debouching circuit.
- P.36 [LVDS]Update Panel ID and related information.

(2009/07/03)

- P.10 [PCH (HDA,JTAG,SAT)]Del TP119/TP123/TP133/TP136/TP137/TP138 and R442 because this is SW reserve design.
- P.14 [PCH (PCI,USB,NVRAM)]Del Q39/Q37/R5456/SW5/R300 for changing GNT1#/GNT0# control method.
- P.14 [PCH (PCI,USB,NVRAM)]Add R345/R346 pull-high to +3VRUN for controlling GNT1#/GNT0#.
- P.14 [PCH (PCI,USB,NVRAM)]Change R344/R392/R345/R346 to 10K ohm.
- P.45 [Mini-PCIE Card (WLAN)]Del R17 and change the net name "MINI_PCIE_+3_3V_R" to "MINI_PCIE_+3_3V" to del RF reserve circuit.
- P.70 [AUDIO (USB)*]Change U_CN2/U_CN3/U_CN6 to 2N-0004009-MKG0 for ME request.
- P.64 [AUDIO (CODEC)*]Change U_R5774 to 100K ohm and change the power source on it from U_VDDA to U_+12V because Gate voltage of U_Q55 is too low.
- P.67 [AUDIO (AUDIO & USB Conn)*]Move U_SUS_ON to U_CN1 Pin22 and add U_+12V on Pin7.
- P.62 [AUDIO/USB DB Conn.]Move SUS_ON to CN31 Pin29 and add +12V on Pin44.
- P.37 [Inverter Connector]Del R400 for MOR's request.
- P.38 [LVDS Connector]Add Q177/Q178/R5736/R5737/C575 and change L98 for rush current issue.
- P.36 [LVDS]Del R136 for redundant design.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Add a NC resistor R979 to let GPIO8 pull-low to GND.
- P.14 [PCH (PCI,USB,NVRAM)]Change Bluetooth USB port to port13.
- P.14 [PCH (PCI,USB,NVRAM)]Change USB External Port-1 to USB port5 and eSATA change to port0.

(2009/07/04)

- P.45 [Mini-PCIE Card (WLAN)]Restore U45,C891 for WIMAX function.
- P.45 [Mini-PCIE Card (WLAN)]Connect 36pin,38pin of CN12 to USB PN12 L/USB PP12 L for WIMAX function.
- P.45 [Mini-PCIE Card (WLAN)]Add J5 to connect Pin42 and Pin44 of CN12 for MOR's request.

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Document Number		CCPBG - R&D Division	
Title	History(2)		
Size	A3		Rev
M960&M970 H Model		SA	
Date:	Thursday, December 24, 2009	Sheet	85 of 86

M960/M970 EVT

(2009/07/07)

- P.54 [Bluetooth Connector]Add C378 pull-low to GND refer to M930.
- P.56 [Status LED & LID]Del POWER/SUSPEND LED and its related circuit for ID changing.
- P.12 [PCH (DMI,FDI,GPIO)]Change R973 to 2.2K ohm for MOR's requirement.
- P.28 [VGA (Power) 6/6]Add R5816 between GND to PX_EN and set N.C for MOR's request.
- P.38 [LVDS Connector]Add Q177 and related RC for protecting rush current.
- P.61 [AUDIO Speaker Conn]Del Q28/Q30/Q53 and connect Q25 and Q27 because short protection circuit can marge L channel and R channel.
- P.04 [ARD (CLK,MISC,JTAG)]Add Q72 for Intel S3 Power Reduction issue.
- P.72 [DCIN&Charger]Delete PR17.
- P.75 [SYS Power (+3_3V/+5V)]Delete close_jump GP2.
- P.77 [DDR3 Power(+1_5V/+0_75V)]Change 1.5VSUS full load from 12A to 13A.
- P.77 [DDR3 Power(+1_5V/+0_75V)]Change PR654 from 46.4k to 49.9k
- P.82 [Others power plane]Change 1.5VRUN full load form 6A to 7A.
- P.82 [Others power plane]Add 1.5VRUN discharge circuit (add PR660 330ohm,PQ71 2N7002EPT).
- P.38 [LVDS Connector]Del R474/R473 and related EDID circuit for disabling EDID.

(2009/07/08)

- P.56 [Status LED & LID]Add Q18/Q21/Q48/Q51/R384/R390/R690/R691/R694/R695 for POWER/SUSPEND LED location changing.
- P.54 [Bluetooth Connector]Del C378 because C377 has the same function.
- P.40 [EC+KBC(NPCE783L)]Add SYSTEM_ID3 (R5891/R5900) for SKU control.
- P.25 [LVDS Connector]NC CN13 Pin3 because EDID is disabled.
- P.63 [SWITCH (Botton & KB LED)*]Del P_SW3 and add P_CN4 for POWER/SUSPEND LED location changing.
- P.56 [Status LED & LID]Change Q18/Q21/Q50 to DTC114EUB for MOR's request.
- P.07 [ARD (GRAPHICS POWER)]Change VDDQ power source from +1_5VSUS to +1_5VRUN for Intel S3 Power Reduction issue.
- P.60 [SWITCH DB Conn.]Change CN2 to 14pin type for POWER/SUSPEND LED location changing.
- P.63 [SWITCH (Botton & KB LED)*]Change P_CN3 to 14pin type for POWER/SUSPEND LED location changing.
- P.51 [PCIE (MS&iLINK) 1/2]Change CN36 type for ME request.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Set GPIO27 as RST_GATE for Intel S3 Power Reduction issue.
- P.75 [SYS Power (+3_3V/+5V)]Change NC PR118 to NO NC PR118 and NC PR234,PR235.
- P.83 [OVP protection]Delete reserved Power limit circuit(delete PU2,PU11,PD22 ,PR22,PR24,PR142,PR143,PR149,PR153,PR159,PR213,PR214,PC26,PC27,PC28).
- P.83 [OVP protection]change PR218 from 37k to 45.3k.
- P.11 [PCH (PCI-E,SMBUS,CLK)]Del R1590/R1591/R1592/Q73/Q74 and rename SMB_DATA_SB/SMB_CLK_SB to SMB_DATA_R/SMB_CLK_R.
- P.10 [PCH (HDA,JTAG,SAT)]Del R1552/R1554 and rename SPI_CLK_L/SPI_MOSI_L to SPI0_CLK/SPI0_MOSI for redundant design.
- P.10 [PCH (HDA,JTAG,SAT)]Add R5910 on SATA_LED# which is pull-high to +3VRUN for Intel comment.
- P.04 [ARD (CLK,MISC,JTAG)]NC R1451/R1452 and stuff R1450/R1453 refer to M930.
- P.52 [PCIE (SD) 2/2]Change CN29 type for ME request.
- P.58 [Touch Pad]Change SW2/SW3/SW6/SW7 type for ME request.

(2009/07/09)

- P.24 [VGA (Strap) 2/6]Change memory aperture size description for SW request.
- P.68 [AUDIO (Head Phone Jack)*]Change Pin7/Pin8 of U_CN4 to U_A_GND for Layout request.
- P.14 [PCH (PCI,USB,NVRAM)]Change USB_OC#5/USB_OC#4 to Pin7/Pin8 of RP18 for Layout request.
- P.07 [ARD (GRAPHICS POWER)]Add a Open-Jump PJ43 between +1_5VRUN to VDDQ.
- P.06 [ARD (POWER)]Del R856/R857 for MOR's request.

- P.07 [ARD&CD (GRAPHICS POWER)]Del R864/R866/R868/R869/R871 for MOR's request.
- P.51 [PCIE (MS&iLINK) 1/2]Add damping resistors (R5911~R5919) on each MS signal.
- P.52 [PCIE (SD) 2/2]Change C518/C522 to X5R type for MOR's request.
- P.52 [PCIE (SD) 2/2]Add damping resistors (R5920~R5924) on each SD signal.
- P.52 [PCIE (SD) 2/2]Change C767 to 10pF for MOR's request.
- P.56 [Status LED & LID]Del LED7/LED8/LED10 for ME request.
- P.38 [LVDS Connector]Add NC Cap. (C6306~C6313) between each LVDS differential lane.
- P.46 [LAN (88E8057) 1/2]Modify R94/R97/C997 description.
- P.46 [LAN (88E8057) 1/2]Change all resistors and caps to 88E8059 setting.
- P.84 [HOLE & AMI LABEL]Add H25/H26/H27/H28 for ME request.
- P.35 [CRT]Change CN20 type for ME request.
- P.70 [AUDIO (USB)*]Change U_CN2/U_CN3/U_CN6 type for ME request.
- P.84 [HOLE & AMI LABEL]Del H11/H12/H13/H15/H16/H17/H18/H19/H20 for ME request.
- P.44 [Express Card]Rename PCIE_EXPRESS_WAKE# to PCIE_WAKE# to del reserve design.
- P.12 [PCH (DMI,FDI,GPIO)]Del R290 and PCIE_EXPRESS_WAKE# off-page to del reserve design.
- P.82 [Others power plane]Add 0.75V RUN discharge circuit(add PR661 330ohm).
- P.82 [Others power plane]Change PQ71 from 2N7002EPT to ME2N7002KW.
- P.04 [ARD (CLK,MISC,JTAG)]Del the description of RST_GATE and add a 1k ohm resister R5925 between +1_5VSUS and DDR3_DRAMRST#.
- P.04 [ARD (CLK,MISC,JTAG)]Add R5926/R5927/U217 for Intel S3 Power Reduction issue.
- P.04 [ARD (CLK,MISC,JTAG)]Del R928/R929 and related description for Intel S3 Power Reduction issue.
- P.53 [Camera Connector]Add R5928/R5929/C6314/C6315 For EMI verification.
- P.37 [Inverter Connector]Add R5930 For EMI verification.

(2009/07/10)

- P.22 [Braidwood Connector]Del P.22 and change the page number from 23~87 to 22~86 for removing Braidwood function.
- P.14 [PCH (PCI,USB,NVRAM)]Del all Braidwood-related off-page for removing Braidwood function.
- P.49 [SATA Combo]Swap L62/L66/L67 for layout request.
- P.62 [SWITCH (Botton & KB LED)*]Change the description "Instant On" to "Web(Instant On) for SW request".
- P.50 [PCIE (MS&iLINK) 1/2]Del R820/C868/R817/C865/R818/C864 for Ricoh's FAE suggest.
- P.50 [PCIE (MS&iLINK) 1/2]Add description of C794/C771/C774/C992 for Ricoh's FAE suggest.
- P.50 [PCIE (MS&iLINK) 1/2]Add description of C790/C769/C770/C772/C799 for Ricoh's FAE suggest.
- P.50 [PCIE (MS&iLINK) 1/2]Add description of C716/C717 for Ricoh's FAE suggest.
- P.38 [HDMI]Connect Q57 D/S to +5VRUN_L188/+5VRUN_F.
- P.37 [LVDS Connector]Connect Q177 D/S to DCBATOUT_L/DCBATOUT.
- P.39 [EC+KBC(NPCE783L)]Change net name "KB_PRESENCE#" to "INST_ON_SW#" for SW request.
- P.71 [DCIN&Charger]Delete NC PR12.
- P.71 [DCIN&Charger]Change charge voltage form 12.48V to 12.465V for MOR request (change PR25 form 200k_F to 210K_F, change PR27 from 100K_F to 100K_D).
- P.73 [Identify IC]Change PC66 from 0.1u 16v 0402_Y5V to 0.1u 10v 0402_X5R.
- P.73 [Identify IC]Change NC PC65 1u 10v 0603_X5R to NC PC65 1u 10v 0402_X5R.
- P.78 [CPU Power_VHOCORE]Change PC112 from 100U_25V_M_φ6.3*7.7mm to 68uF_25V_M_φ6.3*5.8mm.

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	History(3)		
Size	Document Number		Rev
A3	M960&M970 H Model		SA
Date:	Thursday, December 24, 2009	Sheet	86 of 93

M960/M970 EVT

(2009/07/11)

- P.36 [Inverter Connector]Reverse CN5.
- P.62 [SWITCH (Botton & KB LED)*]Reverse P_CN3.
- P.37 [LVDS Connector]Add description on the circuit for inrush current issue of M870.
- P.34 [CRT]Change F2 type for PUR request.
- P.63 [AUDIO (CODEC)*]Change U_C459/U_C476/U_C787 type for PUR request.
- P.07 [ARD (GRAPHICS POWER)]Add net name "+1_5VRUN_J".
- P.14 [PCH (PCI,USB,NVRAM)]Del R344/R392 and the description about Boot-BIOS for SW request.
- P.52 [Camera Connector]Add net name DMIC_CLK R/DMIC_DAT R and connect TP1160/TP1161 to the new net for TE request.
- P.20 [DDRIII(SO-DIMM_0) 1/2]Reconnect SPR2/J2 to CN34 and CN35 for EMC request.
- P.10 [PCH (HDA,JTAG,SAT)]Reverse CN26.
- P.38 [HDMI]Change CN21 type for ME request.
- P.60 [AUDIO Speaker Conn]Swap JSPK1 for ME request.

(2009/07/13)

- P.51 [PCIE (SD) 2/2]Change U22 to G553E1P11U to meet MOR's request for SD.
- P.57 [Touch Pad]Reverse CN8 for ME request.
- P.62 [SWITCH (Botton & KB LED)*]NC P_VR2 for EMC reserve.
- P.50 [PCIE (MS) 1/2]Del all i-Link related description.
- P.36 [Inverter Connector]Reverse CN5.
- P.83 [HOLE & AMI LABEL]Change H2/H3/H4/H5/H6/H7/H10/H14 type for ME request.
- P.25 [VGA (Memory BUS) 4/6]Change C6100 type for PUR request.
- P.71 [DCIN&Charger]Delete EC3 and C907.
- P.79 [CPU Power VHCORE]Change PC566 from 0.1U_6.3V_K to 0.1U_16V_K (HH PN:1C-2B20104-K300).
- P.82 [OVP protection]Change PQ3 from IRLML5103TRPbF to SI2303BDS.
- P.04 [ARD (CLK,MISC,JTAG)]Change U217 SUS_PWRGD to RUN_PWRGD.
- P.63 [AUDIO (CODEC)*]Paste the schematic from P.48 of L model for MOR's request and Layout concern.
- P.64 [AUDIO (MUTE)*]Paste the schematic from P.49 of L model for MOR's request and Layout concern.
- P.65 [AUDIO (Power)*]Paste the schematic from P.50 of L model for MOR's request and Layout concern.
- P.66 [AUDIO (AUDIO & USB Conn)*]Paste the schematic from P.51 of L model for MOR's request and Layout concern.
- P.67 [AUDIO (Head Phone Jack)*]Paste the schematic from P.52 of L model for MOR's request and Layout concern.
- P.68 [AUDIO (Ext MIC Jack)*]Paste the schematic from P.53 of L model for MOR's request and Layout concern.
- P.69 [AUDIO (USB)*]Paste the schematic from P.54 of L model for MOR's request and Layout concern.
- P.04 [ARD (CLK,MISC,JTAG)]Change R5926/R5927 to 1.5K/750 ohm for intel's comment.
- P.81 [Others power plane]Change PR661 from 330ohm to 33ohm.

(2009/07/14)

- P.38 [HDMI]Swap RP55/RP57/RP59/RP61 for Layout request.
- P.49 [eSATA Combo]Swap L62/L66/L67 for Layout request.
- P.37 [LVDS Connector]Swap Pin1 CN13 to Pin3 CN13 for cable design.
- P.83 [HOLE & AMI LABEL]Change H4/H5/H7 footprint for ME request.
- P.71 [DCIN&Charger]NC PR76 and PR77.
- P.78 [CPU Power_VHCORE]Change PR555 and PR569 from 2.7K to 2.21K.
- P.78 [CPU Power_VHCORE]NC PC260 ,NC PC261.
- P.39 [EC+KBC(NPCE783L)]Pull-high INST_ON_SW# to +ECVCC for SW request.
- P.76 [DDR3 Power(+1.5V/+0.75V)]Add PQ59(2N7002EPT)/PR600(100K)/PC570(1U_10V_K), then NC PQ59/PR600/PC570.

(2009/07/15)

- P.49 [SATA Cd-ROM]NC CN37 for ME request.
- P.39 [EC+KBC(NPCE783L)]Del R5858 for redundant design.
- p.78 [CPU Power_VHCORE]change PC112 from NOCHICON to Panasonic.
- P.24 [VGA (I/O) 3/6]Connect GPIO_3/GPIO_4 to SMB_THRM_DATA/SMB_THRM_CLK for MOR's request.
- P.09 [ARD (RESERVED)]Del RP83 and DQ_VREF off-page and add two test point to CPU for Intel's comment.
- P.20 [DDRIII(SO-DIMM_0) 1/2]Del C35/C45/R1283 and DQ_VREF0 off-page for Intel's comment.
- P.20 [DDRIII(SO-DIMM_0) 1/2]Connect VREF_DQ ato VREF_CA for Intel's comment.
- P.21 [DDRIII(SO-DIMM_1) 2/2]Del C37/C44/R1284 and DQ_VREF1 off-page for Intel's comment.
- P.21 [DDRIII(SO-DIMM_1) 2/2]Connect VREF_DQ ato VREF_CA for Intel's comment.
- P.83 [HOLE & AMI LABEL]Add H29/H30/PAD1/PAD2/PAD3 for EMC request.
- P.83 [HOLE & AMI LABEL]Change H28/H25 type for ME request.

(2009/07/16)

- P.83 [HOLE & AMI LABEL]Change PAD1/PAD2/PAD3 for CIS request.
- P.23 [VGA (Strap) 2/6]Modify description of VRAM.
- P.20 [DDRIII(SO-DIMM_0) 1/2]Restore C35/C41 for MOR's request.
- P.21 [DDRIII(SO-DIMM_1) 2/2]Restore C37/C44 for MOR's request.

(2009/07/17)

- P.78 [CPU Power_VHCORE]Change PR565 from 10k to 1.8k, change PC566 from 0.1u to 0.022u.

M960/M970 DVT

(2009/07/21)

- p.1~88 [Page Data]Update all page data.

(2009/07/24)

- P.84 [Braidwood Connector]Add CN39 and its related schematic for layout estimation.
- P.4 [PCH (PCI,USB,NVRAM)]Add Braidwood related schematic for layout estimation.

(2009/07/30)

- P.84 [Braidwood Connector]Del CN39 and its related schematic for layout estimation.
- P.78 [CPU Power_VHCORE]Delete PJ42.
- P.80 [VGA Power(ATI_VDD)]Delete PJ30, NC PR210, Change PR183 from 20K to 15.4K, Change PR550 from 2.7k to 5.36k.

(2009/08/13)

- P.39 [EC+KBC(NPCE783L)]Del R5852 for OVT_EC# double pull-high.
- P.13 [PCH (LVDS,DDI)]Change R223 from 0.5% to 5% for RGB disable guide.
- P.60 [AUDIO Speaker Conn]Change JSPK1 to 1N-0004003-MIT0 for ME request.
- P.66 [AUDIO (AUDIO & USB Conn)*]Reverse U_CN1 for moving U_CN1 from TOP to BOT side.
- P.67 [AUDIO (Head Phone Jack)*]Changen U_CN4 to 2N-000600N-FKG0.
- P.68 [AUDIO (Ext MIC Jack)*]Change U_CN5 to 2N-000600C-FRG0.
- P.69 [AUDIO (USB)*]Change U_USB_OC#1/2/3 to U_USB_OC#0/2.
- P.66 [AUDIO (AUDIO & USB Conn)*]NC U_USB_OC#3 and Change U_USB_OC#1/2 to U_USB_OC#0/2.
- P.61 [AUDIO/USB DB Conn.]NC U_USB_OC#3 and Change U_USB_OC#1/2 to U_USB_OC#0/2.
- P.14 [PCH (PCI,USB,NVRAM)]Del off-page USB_OC#1/3.
- P.27 [VGA (Power) 6/6]Change Q77 to 17-2N7002W-0000 for PUR request.
- P.04 [ARD (CLK,MISC,JTAG)]Change Q72 to 17-2N7002W-0000 for PUR request.
- P.38 [HDMI]Change Q13 to 17-2N7002W-0000 for PUR request.
- P.78 [CPU Power_VHCORE]Delete NC_PC260, NC_PC261.

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
History(4)			
Title	Document Number		Rev
Size	M960&M970 H Model		SA
A3	Date: Thursday, December 24, 2009		Sheet 87 of 93

M960/M970 DVT

(2009/08/18)

- P.34 [CRT]Change F2 to 0.35A.
- P.83 [HOLE & AMI LABEL]Add H31 and change H1/H27/PAD1/PAD2/PAD3 for ME request.
- P.49 [eSATA Combo]Swap CN27B.
- P.43 [Express Card]Change R5457 to 470K and add NC R686 for MOR request.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Change RST_GATE from GPIO27 to GPIO46 , Stuff R982,NC R977.
- P.46 [LAN (Transformer) 2/2]Change L70 for cost down.
- P.51 [AUDIO (CODEC)*]Change U_U215.
- P.25 [VGA (Memory BUS) 4/6]Change R5795,R5809,R5796,R5810 from 1R-000402X-F200 to 1R-0000101-F200 for vendor request.
- P.27 [VGA (Power) 6/6]Stuff R5816 for vendor request.
- P.24 [VGA (I/O) 3/6]Change R5793 from 1R-0000000-J200 to 1R-0000101-F200 and change R5794 from 1R-0000000-J200 to 1R-0000121-F200 for vendor request.
- P.31 [VRAM(DDR3)# 4/4]NC R5727 for vendor request.
- P.55 [Status LED & LID]Change U21 to 15-EC2648B-0000 for cost down.
- P.71 [DCIN&Charger] Change PQ5,PQ16,PQ34 to 17-2N7002W-0000 for materials shortage.
- P.76 [DDR3 Power(+1.5V/+0.75V)] Change PQ59 to 17-2N7002W-0000 for materials shortage.
- P.82 [OVP protection] Change PQ9,PQ17 to 17-2N7002W-0000 for materials shortage.
- P.81 [Others power plane] Change PQ29,PQ45,PQ48 to 17-2N7002D-W001 for materials shortage.
- P.83 [HOLE & AMI LABEL]Change H29/H30 for ME request.

(2009/08/24)

- P.69 [AUDIO (USB)*]Change U_CN2/U_CN3/U_CN6 for ME request.
- P.60 [AUDIO Speaker Conn]Change JSPK1 for ME request.
- P.34 [CRT]Change CN20 for ME request.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Change R977 from NC to Stuff and change R982 from Stuff to NC.

(2009/08/25)

- P.83 [HOLE & AMI LABEL]Change H26 for ME request.

(2009/08/27)

- P.83 [HOLE & AMI LABEL]Change H30 for ME request.

(2009/08/31)

- P.71 [DCIN&Charger]Change PCN1 to BP92071-B81E2-7H for ME request.
- P.48 [SATA HDD]Change CN33 to LN21131-D40L-9H for ME request.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Add R5931/R5932/R5933/R5934 and change R5866 to 100K to pull-high LCDID for PE request.
- P.35 [LVDS]Add R5935/R5936/R5937/R5938/R5939/R5940 to pull-low LCDID for PE request.

(2009/09/01)

- P.56 [FAN]Del TP1163.
- P.63 [AUDIO (CODEC)*]Add ALC269 co-lay schematic and del U_TP229, U_TP231, U_TP228.
- P.14 [PCH (PCI,USB,NVRAM)]Del R1575 for redundant design (double pull-low).
- P.64 [AUDIO (MUTE)*]Add ALC265 co-lay schematic.
- P.10 [PCH (HDA,JTAG,SAT)]NC R5910 for redundant design (double pull-high).
- P.74 [SYS Power (+3.3V/+5V)]Move TP215 from +5VALW_PWM to +5VALW for power test.
- P.74 [SYS Power (+3.3V/+5V)]Move TP219 from +3VALW_PWM to +3VALW for power test.
- P.75 [SYS Power(+1.05V_VTT)]Add TP504 for +1.05V_VTT power test.
- P.78 [CPU Power_VHCORE]Add TP507,TP223,TP224 for VHCORE power test.
- P.79 [CPU Power_VID]Add TP225~ TP233 for power test.
- P.80 [VGA Power (ATI_VDD)]Change PR184 rome 1K to 100ohm, NC PC160 for vendor suggest.
- P.80 [VGA Power (ATI_VDD)]Add TP221,TP222 for power test.
- P.80 [VGA Power (ATI_VDD)]Add PR662 and PC571 for vendor suggest.
- P.80 [VGA Power (ATI_VDD)]Add PC572(NC) for vendor suggest.

(2009/09/03)

- P.25 [VGA (Memory BUS) 4/6]Stuff R5798, R5800, R5799, R5802, R5803, R5804 for Madison/Park only.
- P.25 [VGA (Memory BUS) 4/6]Change R5806, R5807 to 0 ohm for Madison/Park only.
- P.27 [VGA (Power) 6/6]Stuff L89,C6187,C6186,C6185 for Madison/Park only.
- P.27 [VGA (Power) 6/6]Stuff R5811 for Madison/Park only.
- P.22 [VGA (PCI-E) 1/6]Stuff R5831 for Madison/Park only.
- P.27 [VGA (Power) 6/6]NC L76,L77,C6155,C6158 for Madison/Park only.
- P.27 [VGA (Power) 6/6]Stuff L92, C6233, C6234, C6236, R5812 for Madison/Park only.
- P.27 [VGA (Power) 6/6]Stuff L26, NC L30 for Madison/Park only.
- P.27 [VGA (Power) 6/6]Stuff L90, C6192, C6193, C6194, C6195, C6196 for Madison/Park only.
- P.27 [VGA (Power) 6/6]Stuff L91, C6197, C6199, C6200 for Madison/Park only.
- P.27 [VGA (Power) 6/6]NC R5815 for Madison/Park only.
- P.55 [Status LED & LID]Move R390/R384 to Drain side of Q51/Q48 for MOR comment.
- P.37 [LVDS Connector]Change CN13 to M870 type (1N-0040000-FWG0).
- P.59 [SWITCH DB Conn.]Change CN2 to 12pin type (1N-0012002-F0T0).
- P.62 [SWITCH (Botton & KB LED)*]Change P_CN3 to 12pin type (1N-0012002-F0T0).
- P.62 [SWITCH (Botton & KB LED)*]Move NUM LOCK LED/CAP LED/SCROLL LOCK LED driving circuit to MB for MOR comment.
- P.55 [Status LED & LID]Add NUM LOCK LED/CAP LED/SCROLL LOCK LED driving circuit for MOR comment.
- P.09 [ARD (RESERVED)]Del test points for MOR comment.
- P.11 [PCH (PCI-E,SMBUS,CLK)]Del test points for MOR comment.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Del test points for MOR comment.
- Test Points[TP109/TP193/TP181/TP208/TP209/TP211/TP210/TP212/T213/TP214/TP235/TP236/TP265/TP266/TP237/TP239/TP327/TP328/TP329/TP256/TP257/TP259/TP260/TP262/TP263/TP264/TP284/TP287/TP288/TP289/TP290/TP291/TP292/TP293/TP294/TP295/TP296/TP297/TP298/TP425/TP1116/TP1117/TP1118/TP1119/TP140/TP147/TP148/TP149/TP148/TP145/TP144/TP134TP1120/TP1121/TP1122/TP1123/TP1124/TP188/TP183/TP88/TP91/TP93/TP101/TP412/TP416/TP415/TP417/TP414/TP421/TP422/TP423/TP424]
- P.09 [ARD (RESERVED)]Del RP87 for MOR and Intel comment.
- P.15 [Status LED & LID]Add LED test points TP1223/TP1224/TP1225/TP1226/TP1227/TP1228/TP1229/TP1230.
- P.10 [PCH (HDA,JTAG,SAT)]Change U98 to W25Q32BVSSIG.
- P.63 [AUDIO (CODEC)*]Del U_U7 and U_C155 for Realtek suggestion.
- P.16 [PCH (POWER) 1/2]Del R897, R989 for MOR comment.
- P.17 [PCH (POWER) 2/2]Del R428, R958 for MOR comment.
- P.04 [ARD (CLK,MISC,JTAG)]Add R5950, C6316, R5951, R5949, R5948, C6317 for Intel S3 issue.

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title History(5)			
Size	Document Number		Rev
A3	M960&M970 H Model		SA
Date:	Thursday, December 24, 2009	Sheet	88 of 93

M960/M970 DVT
(2009/09/08)

- P.63 [AUDIO (CODEC)*]Change U_R327 to 1K.
- P.71 [DCIN&Charger]NC PR33 for costdown.
- P.80 [VGA Power (ATI VDD)]Add PR663(NC) and PC573(NC) for vendor suggest.
- P.82 [OVP protection]PR167 change to 26.1K, PR169 change to 80.6K , PR171 change to 18.2K for OVP Adjust
- P.82 [OVP protection]Use SW PWRLIMIT function replaced HW PWRLIMIT circuit for costdown.(NC PU31,PC567,PR223,PR629,PR219,PR218,PR78,PC46.)
- P.62 [SWITCH (Botton & KB LED)*]Change P_VR1/P_VR2/P_VR3/P_VR4 to 19-MLVS060-5000.
- P.39 [EC+KBC(NPCE783L)]Change C27/C26 to 15p for Crystal vendor comment.
- P.10 [PCH (HDA,JTAG,SAT)]Change C727/C702 to 15p for Crystal vendor comment.
- P.50 [PCIE (MS) 1/2]Change C785/C786 to 22p for Crystal vendor comment.
- P.49 [eSATA Combo Conn.]Add eSATA reperator schematic and NC it.
- P.10 [PCH (HDA,JTAG,SAT)]Change CN18 to GB5RF120-1203-7F for Halgen Free.
- P.42 [Debug Port]Change CN30 to GB5RF120-1203-7F for Halgen Free.
- P.54 [Felica Connector]Add Felica power supply schematic as Pokerman type for MOR request.
- P.14 [PCH (PCI,USB,NVRAM)]Change USB OC# signal to EVT type for MOR request.
- P.41 [SPI Flash ROM]Change U23 to W25X10BVSNIQ for SW comment.
- P.63 [AUDIO (CODEC)*]Move U_R5774 to P.60 and rename to R5968.
- P.61 [AUDIO/USB DB Conn.]NC +12V and add a +5VALW pin for USB VEVS test.
- P.66 [AUDIO (AUDIO & USB Conn)*]NC U_+12V to a U_+5VALW pin for USB VEVS test.
- P.61 [AUDIO/USB DB Conn.]Change CN31 to 1N-0050004-F0T0 for ME request.
- P.66 [AUDIO (AUDIO & USB Conn)*]Change U_CN1 to 1N-0050004-F0T0 for ME request.
- P.45 [LAN (88E8057) 1/2]Add R5965/R5966/R5967 for 88E8057/88E8059 co-lay.
- P.61 [AUDIO/USB DB Conn.]Change CN31 Pin 43 to GND.
- P.66 [AUDIO (AUDIO & USB Conn)*]Change U_CN1 Pin 43 to GND.
- P.55 [Status LED & LID]Change Q49/Q179/Q180/Q181 to 17-DTA114Y-UB00 for PUR suggest.
- P.44 [Mini-PCIE Card (WLAN)]Change Q5 to 17-DTC144E-UB00 for PUR suggest.
- P.56 [FAN]Change Q80 to 17-DTC144E-UB00 for PUR suggest.
- P.71 [DCIN&Charger]Change TP1148,TP1149,TP1150,TP1151 from DC_IN_1 to P+ for power test.
- P.71 [DCIN&Charger]Change PQ16,PR76,PR77 from NC to mount for EC PWRLIMIT function.
- P.71 [DCIN&Charger]Change PR79 from 0 to 3.48K, change PR11 from 20K to 12K for EC PWRLIMIT function.
- P.73 [Identify IC]Add PD31 and change PR68 from 10K to 4.7K for MOR request.
- P.81 [Others power plan]Delete TP189,TP203 for power test.

(2009/09/09)

- P.42 [Debug Port]Del TP1186~TP1193.
- P.24 [VGA (I/O) 3/6]Add ATI_LVDS_SCL/ATI_LVDS_SDA for EDID function.
- P.37 [LVDS Connector]Add ATI_LVDS_SCL/ATI_LVDS_SDA for EDID function.
- P.74 [SYS Power (+3.3V/+5V)]Change PR652,PR245 from NC to mount 4.7ohm. Change PC568,PC272 from NC to mount 680pF for EMI suggest.
- P.75 [SYS Power(+1.05V_VTT)]Change PR188 from NC to mount 4.7ohm, Change PC170 from NC to 680pF for EMI suggest.
- P.76 [DDR3 Power(+1.5V/+0.75V)]Change PR41 from NC to mount 4.7ohm, Change PC42 from NC to mount 680pF for EMI suggest.
- P.80 [VGA Power (ATI VDD)]Change PR163 from NC to mount 4.7ohm, Change PC133 from NC to mount 680pF for EMI suggest.
- P.52 [Camera Connector]Del R5928/R5929 and add L93/L94 for EMC request for DMIC noise.
- P.52 [Camera Connector]Mount C6314/C6315 for EMC request for DMIC noise.
- P.60 [AUDIO Speaker Conn]Del R5870, R5871, R5872, R5873 and Add L95, L96, L97, L98 for EMC request to filtrate SPK noise.
- P.37 [LVDS Connector]Add C6324/C6325 for EMC request for 150MHz powerbase issue.

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- P.42 [Felica Connector]Change Felica power supply from +5VSUS to +3VSUS.
- P.41 [PCIE (SD) 2/2]Change R991 to 100K for MOR request.
- P.43 [Express Card]NC Q38, R5457 and mount R686 for MOR comment.

(2009/09/10)

- P.37 [LVDS Connector]Add CN13 Pin40 for EDID function.
- P.44 [Mini-PCIE Card (WLAN)]Add C6329/C6330 for EMI request.
- P.16 [PCH (POWER) 1/2]Add C6326/C6327/C6328 for EMI request.
- P.62 [SWITCH (Botton & KB LED)*]Change P_LED1/P_LED2/P_LED3 to HT-170UYG.
- P.81 [Others power plane]Add C6332/C6333 on +3VSUS for EMI request.
- P.81 [Others power plane]Add C6334/C6335/C6336 on +3VRUN for EMI request.
- P.45 [LAN (88E8059) 1/2]Del R97 and add C6341 for Marvell FAE request.
- P.45 [LAN (88E8059) 1/2]Del R5966, R5967 for Marvell FAE request.
- P.45 [LAN (88E8059) 1/2]Change C993 to 10u for Marvell FAE request.
- P.43 [Express Card]Correct Express Card SPEC.
- P.48 [SATA CD-ROM]Del CN37 for MOR request.
- P.61 [AUDIO/USB DB Conn.]Add F1 for MOR comment.
- P.66 [AUDIO (AUDIO & USB Conn)*]rename U_+5VALW to U_+5VALW_IN for MOR comment.
- P.69 [AUDIO (USB)*]Del U_F1 and rename U_+5VALW to U_+5VALW_IN for MOR comment.
- P.83 [HOLE & AMI LABEL]Del BOSS2 for MOR request.
- P.63 [AUDIO (CODEC)*]Change U_R321 to 100K for MOR request.
- P.64 [AUDIO (MUTE)*]NC U_C472 for MOR comment.
- P.68 [AUDIO (Ext MIC Jack)*]NC U_R42, U_R46 for MOR comment.
- P.68 [AUDIO (Ext MIC Jack)*]Del U_C26, U_C31 and add U_R5791, U_R5792 for MOR comment.
- P.68 [AUDIO (Ext MIC Jack)*]NC U_R42, U_R46 for MOR comment.
- P.63 [AUDIO (CODEC)*]NC U_C923.
- P.67 [AUDIO (Head Phone Jack)*]Change U_GND to U_A_GND for Realtek FAE suggest.
- P.37 [LVDS Connector]NC CN13 Pin7.

(2009/09/11)

- P.71 [DCIN&Charger]Change PR15 to RLM12FTSR020 for PUR request.
- P.71 [DCIN&Charger]Change PF1 to 0437007.WR for PUR request.
- P.37 [LVDS Connector]Change CN13 for Halgen-free.
- P.60 [AUDIO Speaker Conn]Swap JSPK1 for layout concern.
- P.44 [Mini-PCIE Card (WLAN)]Change SW4 to 1BS007-12110-002-7H for ME request.
- P.55 [Status LED & LID]Change LED3/LED4 vendor to Everlight.
- P.67 [AUDIO (Head Phone Jack)*]Change U_A_GND to U_GND for Realtek FAE suggest.
- P.63 [PCIE (SD) 2/2]Change CN29 to WK21923-S6P3-4H for ME request.
- P.10 [PCH (HDA,JTAG,SAT)]Change CN18 to No Halgen-free.
- P.42 [Debug Port]Change CN30 No Halgen-free.
- P.62 [SWITCH (Botton & KB LED)*]Change P_CN3 to No Halgen-free.
- P.59 [SWITCH DB Conn.]Change CN2 to No Halgen-free.
- P.56 [FAN]Change CN14 to No Halgen-free.
- P.60 [AUDIO Speaker Conn]Change JSPK1 to No Halgen-free.
- P.83 [HOLE & AMI LABEL]Change H2/H4/H5 for ME request.
- P.39 [EC+KBC(NPCE783L)]NC U216 Pin8 and del R575.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Connect DIS_FAN_MON# to U69F GPIO57 and pull-high to +3VRUN.
- P.39 [EC+KBC(NPCE783L)]NC U4A Pin20 and add SYSTEM_ID1 off-page.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Connect SYSTEM_ID1 to U69F GPIO17 and del R965.
- P.39 [EC+KBC(NPCE783L)]NC U4A Pin27 and add SYSTEM_ID0 off-page.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Connect SYSTEM_ID0 to U69F GPIO16 and NC RP19 Pin7.
- P.39 [EC+KBC(NPCE783L)]NC U216 Pin9.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Connect PM_SLP_ME# to U4B GPIO26.
- P.39 [EC+KBC(NPCE783L)]Del R5853 and connect INST_ON_SW# to GPIO12.
- P.39 [EC+KBC(NPCE783L)]NC U216 Pin3 and connect WLAN_EN to U4A Pin20.
- P.39 [EC+KBC(NPCE783L)]NC U216 Pin4 and connect BT_ON to U4A Pin27.

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	History(6)		
Size	Document Number	Rev	
A3	M960&M970 H Model	SA	
Date	Thursday, December 24, 2009	Sheet	89 of 93

M960/M970 DVT

(2009/09/11)

- P.39 [EC+KBC(NPCE783L)]NC U216 Pin5/Pin6 and connect AC_OFF/EC_PWRLIMIT_CTRL to U4A Pin119/Pin120.
- P.39 [EC+KBC(NPCE783L)]Del R5855/R5856/C6201/C6202.
- P.39 [EC+KBC(NPCE783L)]Connect AC_Present to U4A Pin124.
- P.39 [EC+KBC(NPCE783L)]Del U216/R5857/C6203.
- P.25 [VGA (Memory BUS) 4/6]Change C6100 to UMK105CH680KW-F for PUR request.
- P.34 [CRT]Del F2 for MOR comment.
- P.63 [AUDIO (CODEC)*]Del U_R5773/U_Q64/U_R5771/U_R5783/U_U215/U_R5784 for MOR comment.
- P.63 [AUDIO (CODEC)*]Move U_AMP_PD# to U_U18 Pin4.
- P.64 [AUDIO (MUTE)*]Mount U_R352/U_R351/U_Q17/U_R349/U_Q15/U_R341 for MOR comment.
- P.25 [VGA (Memory BUS) 4/6]Change R5795/R5796/R5809/R5810 to 40.2 ohm for AMD comment.
- P.34 [CRT]NC R5752 for no need of semi-PNP function.

(2009/09/12)

- P.80 [VGA Power (ATI_VDD)] Change PC159/PC160 to 1C-2B20105-K100(NC) for more stability.
- P.01 [Index page]Update information.
- P.02 [BLOCK DIAGRAM]Update information.
- P.10 [PCH (HDA,JTAG,SAT)]Update SPI ROM information.
- P.49 [eSATA Combo Conn.]Del F10 for no need.
- P.49 [LVDS Connector]Add F15/L99 to follow M870.
- P.10 [PCH (HDA,JTAG,SAT)]Add 100K pull-low resistors R5969/R5970/R5971 on SPI0_MOSI/SPI0_CLK/SPI0_CS# for Intel EDS request.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Change R943/R974/R982/R1626 to 1R-0000103-J200.
- P.63 [AUDIO (MUTE)*]Change U_R340/U_R350/U_R663 to 1R-0000103-J200.
- P.62 [AUDIO (CODEC)*]Change U_R652/U_R662 to 1R-0000103-J200.
- P.52 [Camera Connector]Add R5972/F16 for adding fuse solution.
- P.25 [LVDS Connector]NC CN13 Pin1/Pin5/Pin6 for del EDID function.
- P.24 [VGA (I/O) 3/6]NC U204B ATI_LVDS_SCL/ATI_LVDS_SDA for del EDID function.
- P.20 [DDRIII(SO-DIMM_0) 1/2]NC CAP13 for no need.
- P.21 [DDRIII(SO-DIMM_1) 2/2]NC CAP22 for no need.
- P.25 [VGA (Memory BUS) 4/6]Change Madison/Park description.
- P.25 [VGA (Memory BUS) 4/6]NC R5806/R5807/R5808 for AMD comment.
- P.63 [AUDIO (CODEC)*]Change the setting to ALC269 (NC: U_C441/R5943/U_R5789, Stuff U_C930/R5944/U_R5790).
- P.71 [DCIN&Charger]Change PL3 to NC for costdown.
- P.75 [VTT&PCH Power(+1_05V)]Change PR44 from 0ohm to 2.2ohm for vendor suggest.
- P.76 [DDR3 Power (+1_5V/+0_75V)]Change PR39 from 0ohm to 2.2ohm for vendor suggest.
- P.80 [VGA Power (ATI_VDD)]Change PR549 from 0ohm to 2.2ohm for vendor suggest.

- P.57 [Touch Pad]Del F12 for no need.
- P.35 [LVDS]Update Panel ID information.
- P.51 [AUDIO (CODEC)*]Change U_C787/U_C476/U_C459 to 1C-2B20103-K200.
- P.28 [VRAM(DDR3)# 1/4]Change C6303 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
- P.29 [VRAM(DDR3)# 2/4]Change C6304 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
- P.30 [VRAM(DDR3)# 3/4]Change C6257 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
- P.31 [VRAM(DDR3)# 4/4]Change C6258 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
- P.28 [VRAM(DDR3)# 1/4]Change C4028/C4036 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
- P.80 [VGA Power(ATI_VDD)]Change PC172 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
- P.77 [SYS Power(+1_8V)]Change PC247 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.

- P.65 [AUDIO (Power)*]Change U_C467 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
- P.50 [PCIE (MS) 1/2]Change R5912/R5913/R5914/R5911/R5915/R5916/R5917/R5918/R5919 to 33ohm for correcting SI test fail.
- P.51 [PCIE (SD) 2/2]Change R5920/R5921/R5922/R5923/R5924 to 33ohm for correcting SI test fail.

(2009/09/13)

- P.34 [CRT]Change CN20 to DZ11A91-SB281-4H for different package.
- P.68 [AUDIO (Ext MIC Jack)*]Change U_CN5 to JA63331-R1T0-7H for ME request.

(2009/09/14)

- P.45 [LAN (88E8059) 1/2]Change C995 to 10uF for Marvell comment.
- P.74 [SYS Power (+3_3V/+5V)] Change PR122/PR201 to 2.2 ohm for RF noise.
- P.78 [CPU Power VHCORE] Change PR563 to NC, change PU28 pin25 connect to PROCHOT# for design change.
- P.04 [ARD (CLK,MISC,JTAG)]Add off-page PROCHOT#.
- P.54 [Felica Connector]NC R5963/F14, stuff C869/U48/R630/C845/R5964 for Felica fuse solution fail.
- P.49 [eSATA Combo Conn.]Add R5974/R5975/R5976/R5977 to reduce the trace length on U214 for vendor request.

(2009/09/15)

- P.11 [PCH (PCI-E,SMBUS,CLK)]Make R902/R903 from +3VRUN pull-high to +3VALW pull-high for Intel recommendation.
- P.38 [HDMI]Change CN21 to DF03-577-1931.

(2009/09/16)

- P.14 [PCH (PCI,USB,NVRAM)]NC R1466 for Intel Braidwood disable guideline.

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	History(7)		
Size	Document Number		Rev
A3	M960&M970 H Model		SA
Date:	Thursday, December 24, 2009	Sheet	90 of 93

M960/M970 PVT

(2009/09/19)

- P.25 [VGA (Memory BUS) 4/6]Change R5805 to 10k for AMD comment.
- P.25 [VGA (Memory BUS) 4/6]Add R5981 pull-high to +3VRUN on TESTEN for AMD hang-up workaround.
- P.24 [VGA (I/O) 3/6]Add R5978 pull-low to GND on ATI_JTAG_RST for AMD hang-up workaround.
- P.24 [VGA (I/O) 3/6]Add R5979 pull-high to +3VRUN on ATI_JTAG_TMS for AMD hang-up workaround.
- P.24 [VGA (I/O) 3/6]Add R5980 between R_XTALSSIN and ATI_JTAG_TCLK for AMD hang-up workaround.

(2009/11/04)

- P.07 [ARD (GRAPHICS POWER)] Delete PJ43 for redundant design of EVT & DVT
- P.34 [CRT] Add F17 for current limit by MOR comment
- P.74 [SYS Power (+3_3V/+5V)] Delete PJ11 and PJ12 for redundant design of EVT & DVT
- P.75 [VTT&PCH Power(+1_05V)] Delete PJ22 and PJ23 for redundant design of EVT & DVT
- P.76 [DDR3 Power(+1_5V/+0_75V)] Delete PJ26 and PJ27 for redundant design of EVT & DVT
- P.77 [SYS Power(+1_8V)] Delete PJ36 for redundant design of EVT & DVT
- P.78 [CPU Power_VHOCORE] Change PC112 from 68u_25V to OS_Con cap 47u 25V by MOR request
- P.80 [VGA Power(ATI_VDD)] Delete PJ31 and PJ37 for redundant design of EVT & DVT

(2009/11/12)

- P.25 [VGA (Memory BUS)] Change R5805 to NC & Mount R5981 for AMD suggestion
- P.39 [EC+KBC(NPCE783L)] Add R5982 on OVT_EC# for GPIO70 need pull high
- P.62 [SWITCH (Botton & KB LED)*] Exchange function name for Assist & Web button
- P.35 [LVDS] No mount R5940 to cancell Instant_On function by MOR request
- P.39 [EC+KBC(NPCE783L)] No mount R5851 to cancell Instant_On function by MOR request
- P.55 [Status LED & LID] R689 change resistor value to 300 Ohm, R692 change resistor value to 909 Ohm, R693 change value to 300 Ohm, R5945~R5947 change resistor value to 392 Ohm for LED brightness by MOR request
- P.37 [LVDS Connector] Change CN13 to 1N-004000E-FKG0 for better L6 process
- P.40 [KB Connector] Add TP1233,TP1234 for BFT test
- P.35 [LVDS] Add TP1231,TP1232 for BFT test
- P.51 [PCIE(SD) 2/2] Add TP1239,TP1240 for BFT test
- P.57 [Touch Pad] Add TP1245~TP1250 for BFT test
- P.54 [Felica Connector] Add TP1241~TP1244 for BFT test

(2009/11/16)

- P.71 [DCIN&Charger] Change pcl26 from 1000P_50V_0603_X7R to 1000pF_50V_0402_X7R for MOR request
- P.78 [CPU Power VHOCORE] Change pc253 from 1000P_16V_0402_X7R to 1000pF_50V_0402_X7R for MOR request
- P.82 [OVP protection] Change pc41 from 1000P_16V_0402_X7R to 1000pF_50V_0402_X7R for MOR request
- P.10 [PCH (HDA,JTAG,SAT)] Update U43 schematic symbol
- P.73 [Identify IC] Update PU5 schematic symbol
- P.52 [Camera Connector] L93,L94 change to Bead,MAX ECHO,EBMS100505A121 0.5A, 120ohm/100MHz,25%,0402(1005mm) by MOR request
- P.67 [Audio] U L4,U L5 change to Bead,MAX ECHO,EBMS100505A121 0.5A, 120ohm/100MHz,25%,0402(1005mm) by MOR request
- P.45 [LAN (88E8059) 1/2] C6077 change to SMD,MLCC,X7R,1000pF,50V,10%,0402 by MOR request

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- P.63 [AUDIO (CODEC)*] U_C440 change to SMD,MLCC,X7R,1000pF,50V,10%,0402 by MOR request
- P.46 [LAN (Transformer) 2/2] C568 change to SMD,MLCC,X7R,1000pF,50V,10%,0402 by MOR request
- P.57 [Touch Pad] C130,C133 change to SMD,MLCC,NPO,47pF,50V,5%,0402 by MOR request
- P.39 [EC+KBC(NPCE783L)] C22 change to SMD,MLCC,NPO,22pF,50V,5%,0402 by MOR request
- P.50 [PCIE (MS) 1/2] C544,C785,C786 change to SMD,MLCC,NPO,22pF,50V,5%,0402 by MOR request
- P.63 [AUDIO (CODEC)*] U_C439 change to SMD,MLCC,NPO,22pF,50V,5%,0402 by MOR request
- P.64 [AUDIO (MUTE)*] U_R351 change to SMD,RES,200K,1/16W,5%,0402 by MOR request
- P.64 [AUDIO (MUTE)*] U_R352 change to SMD,RES,33K,1/16W,5%,0402 by MOR request
- P.64 [AUDIO (MUTE)*] U_R341,U_R349, change to SMD,RES,10K,1/16W,5%,0402 by MOR request
- P.10 [PCH (HDA,JTAG,SAT)] R5905, change to SMD,RES,51ohm,1/16W,5%,0402 by MOR request
- P.39 [EC+KBC(NPCE783L)] RP1,RP20,RP90 change to SMD,RES,10K,1/16W,5%,0402 and locations are R5991~R5996 by MOR request
- P.39 [EC+KBC(NPCE783L)] RP21, change to SMD,RES,2.2K,1/16W,5%,0402 and locations are R5987,R5988 by MOR request
- P.39 [EC+KBC(NPCE783L)] RP22, change to SMD,RES,4.7K,1/16W,5%,0402 and locations are R5989,R5990 by MOR request
- P.43 [Express Card] Update U42 Schematic symbol
- P.55 [Status LED & LID] Change TP1224~TP1230 to top for BFT test

(2009/11/17)

- P.33 [HCLK & AM LABEL] Add BOSS2 for M960 wireless card use only
- P.44 [Mini-PCIE Card (WLAN)] Add TP1235~TP1238 on BT_WLAN_SW# & GND for BFT test
- P.45 [LAN (88E8059) 1/2] LAN chip 88E8059 change packing method to tapping for better L6 process
- P.24 [VGA (I/O) 3/6]Connect a stable clock source (from clock gen SS 27MHz) to GPIO26_TCK. Add 5991 pull-down with 10K ohm to ground for the Park/Madison JTAG test block intermittently fails to initialize correctly. Incorrect initialization may result in a failure to boot.
- P.35 [LVDS] SW1 change from 12-pin to 8-pin panel ID SW
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)] NC_R5931 & move R5939 from P.35 to P.15
- P.39 [EC+KBC(NPCE783L)] Move R5940 from P.35 to P.39

(2009/11/18)

- P.57 [Touch Pad] Add F12 for cable short test fail
- P.35 [LVDS] Add test point from TP1251~TP1260 for panel ID switch BFT test
- P.58 [Thermal Sensor] Delete VGA thermal sensor function, NC_U26, NC_R946, NC_C534, NC_C547 because GPU support DTS function
- P.25 [VGA (Memory Bus) 4/6] Change R5878 resistor value from 680 Ohm to 51 Ohm for memory reset circuit update from AMD
- P.55 [Status LED & LID] Change U21 to E-CMOS EC2618NLB1GR for distance can't meet MOR spec

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title History(8)			
Size A3	Document Number M960&M970 H Model		Rev SA
Date: Thursday, December 24, 2009	Sheet 91	of 93	

M960/M970 PVT

(2009/11/19)

- P.24 [VGA (I/O) 3/6] Add TP1261,TP1262 on GPIO8 & GPIO 22 for reserve AMD errata solution
- P.11 [PCH (PCI-E,SMBUS,CLK)] Reserve R5992~R6000 for Intel FCIM function
- P.78 [CPU Power_VHCORE] Change PR554 and PR558 from 0ohm to 2.20hm for EMI request
- P.80 [VGA Power(ATI_VDD)] Change PR183 from 15.4k to 15k for VGA Park high level request
change PR210 from NC_7.15K to 68k for VGA Madison high level request

(2009/11/20)

- P.24 [VGA (I/O) 3/6]Delete R5978,R5979,R5980 for needless
- P.24 [VGA (I/O) 3/6]NC R5991 and add R6001(NC) for AMD Errata suggestion
- P.25 [VGA (Memory BUS)]NC R5981 for AMD Errata suggestion
- P.15 [PCH]Change R5939 to mount for Panel ID setting requirement
- P.64 [Audio(Mute)]Change U_R364 from 33kohm to 3.3kohm for satisfy hFE under 100 as MOR's suggestion.
- P.45 [LAN]Change R84 from 4.7kohm to 0ohm for vendor modification

(2009/11/21)

- P.24 [VGA]Add R6002,R6003,Y9,C6342,C6343 and NC them, it reserve for Intel FCIM function.
- P.69 [Audio (USB)*]Change the footprint of U_CN2,U_CN3,U_CN6 as SMT suggestion.
- P.42 [Debug Port]Add C6344 for EMI request.
- P.66 [AUDIO]Add C6345 for EMI request.
- P.46 [LAN]Change L47 from 100R to 300R for EMI request.
- P.71 [DCIN&Charger]: Dcbatout Add PC574 0.1uf,PC575 0.1uf,PC576 4700pf , PC577 4700pf for EMI request
- P.74 [SYS Power (+3 3V/+5V)]:Add PC578 and PC579 680pf near PQ70 for EMI request
- P.78 [CPU Power_VHCORE]:change PC151 and PC156 from NC to mount 0.1uf for EMI request
- P.81 [Others power plane]:Add PC584 680pf,PC585 0.1uf near P226 for EMI request.

(2009/11/22)

- P.60 [Audio]Add C6348~C6351 for speaker noise issue.
- P.10 [PCH]Add C6352,C6353 and NC them, reserve for EMI request.
- P.63 [AUDIO]NC U_C439 and add U_C931(NC) for EMI request.
- P.55 [LED]Change R5945,R5946,R5947 from 392ohm to 649ohm and R390 from 120ohm to 261ohm as DQA&ME request.
- P.63 [Audio]Change U_R668,U_R665,U_R660,U_R670,U_R672,U_R659(22ohm) from 0402 to 0201 for implement ME solution and layout space is not enough. And change U_R667,U_R664(33kohm), and R5943(NC),R5944(0ohm), and U_R339(20kohm), and U_R338(39.2kohm), and U_R652,U_662(10kohm) from 0402 to 0201 for implement ME solution and layout space is not enough.

(2009/11/23)

- P.39 [EC]Delete R5983,R5984 and add RP20 for layout space concern
- P.81 [Other power plane]Change PR661 from 0603 to 0402 for MOR request to cost down.
- P.15 [PCH]Delete RP19 and add R6004,R6005,R6006 for MOR request to cost down.
- P.52 [Camera]Change C9 from 1C-2Y70106-Y001 to 1C-2Y70106-Y000 for MOR request to cost down.
- P.64 [Audio]Change U_Q20 form 2N7002W to SRK7002 for ESD issue.
- P.25 [VGA]Change R5805 from NC to mount for AMD suggestion.
- P.83 [HOLE]Change H30,H29,H8,H10,H4 hole size as ME's request.
- P.34 [CRT]Change CN20 from FOX_DZ11A91-SB281-4H to FOX_DZ11AE1-SB1SD-4H as ME's request.
- P.61 [Audio/USB DB CONN]Change CN31 from FOX_GB5RF500-1203-7H to FOX_GB5RF500-1203-8H for ME's request.
- P.66 [Audio (Audio/USB CONN)*]Change U_CN1 from FOX_GB5RF500-1203-7H to FOX_GB5RF500-1203-8H as ME's request.
- P.54 [Felica]Change CN7 from FOX_GB5RF060-1203-7H to FOX_GB5RF060-1203-8F as ME's request.

(2009/11/23)

- P.57 [TouchPad]Change CN8' from FOX_GB5RF060-1203-7H to FOX_GB5RF060-1203-8F as ME's request.
- P.10 [PCH]Change C6352 from 0.1uF to 33pF(mount) and R618 from 33ohm to 47ohm as EMC request.
- P.81 [Other power plan]Change PC188 from 10uF to 1uF(mount) for improve power signal.
- P.63 [Audio]Change U_R661,U_R671,U_R676,U_673,U_R321 from 0402 to 0201 for layout space concern.

(2009/11/24)

- P.25 [VGA]Change R5805 from 10k to 5.1k as AMD's suggestion
- P.35 [LVDS]Change SW1 from DHNF-04-T-Q-T-R_SW-SMD8P to DHNF-06-T-Q-T/R_SW-SMD12 for shortage issue.

(2009/11/28)

- P.74 [SYS Power]Change PC578,PC579 from 1C-2B20681-M000 to 1C-2B20681-K000 for PUR's suggestion.
- P.46 [LAN]Change L47 from 1L-BACMS16-0809 to 1L-BTB1608-080D for PUR's suggestion.
- P.42 [Debug Port]NC CN30 for EMC solution.
- P.41 [SPI Flash ROM]NC U3,R43,C20 and mount R775 for EMC solution.
- P.80 [VGA Power(ATI_VDD)]:
 - 1.PR183=10.5k for VGA M92 XT high voltage level request
 - 2.PR183=10.5k for VGA M92 XTX high voltage level request
 - 3.PR183=34.8k for VGA M96 high level request
 - 4.PR183=75k for VGA madision high level request
 - 5.PR183=15K for VGA Park high level request
 - 6.NC PR210

M960/M970 MP

(2009/12/22)

- P.76 [DDR3 Power(+1_5V/+0_75V)] Mount PQ59, change PR600 resistor to 0 Ohm & no mount PR145 to change the enable signal to RUN_PWRGD by MOR request.
- P.38 [HDMI] Change CN21 symbol from 2N-0019007-MKG0 to 2N-0019003-MKG0 to improve factory process

(2009/12/23)

- P.80 [VGA Power(ATI_VDD)]
 - 1.PR222=39.2k for VGA M92 XTX 1.0VPEG 1.1V voltage request
 - 2.PR222=27k for VGA Park 1.0VPEG 1.0V voltage request
 - 3.PR222=27k for VGA Madison 1.0VPEG 1.0V voltage request
- P.25 [VGA (Memory Bus 4/6)]
 - 1.R5795, R5796, R5809, R5810=100 for VGA M92XTX voltage reference
 - 2.R5795, R5796, R5809, R5810=40.2 for VGA Park voltage reference
 - 3.R5795, R5796, R5809, R5810=40.2 for VGA Madison voltage reference
- P.83 [HOLE & AMI LABEL] Mount AMI label for AMI certificate
- P.10 [PCH (HDA,JTAG,SAT)] No mount CN18, U43, C815, R542 & Mount R1551 for needless in MP
- P.64 [AUDIO (MUTE)*] Change U_Q15 with ESD protection for factory ESD issue

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History(9)			
Title	Document Number		Rev
Size	M960&M970 H Model		SA
A3	Date: Thursday, December 24, 2009		Sheet 92 of 93

M960/M970 MP
(2009/12/24)

- P.83 [HOLE & AMI LABEL]Delete BOSS2 for needless from ME's request
- P.46 [LAN(Transformer)]Change L70 from LANKOM to DELTA for LANKOM transformer issue in PVT
- P.45 [LAN]Add R6010 reserve for 8057 solution
- P.04 [ARD]Delete R937,R930 for MOR's request
- P.06 [ARD]Delete R860 for MOR's request
- P.24 [VGA]Delete R5785,R5788,R5789 for MOR's request
- P.39 [EC]Delete R39,R46 for MOR's request
- P.44 [Mini-PCIE Card]Delete R5901 for MOR's request
- P.57 [Touch Pad]Delete R5869,R5868 for MOR's request

(2009/12/28)

- P.10 [PCH]Change R618 from 47ohm to 68ohm and Change C6353 from NC_0.1uF to mount 22pF for EMC audio FFC issue
- P.63 [Audio]Change U_R326 from 22ohm to 0ohm for EMC audio FFC issue