

# COMPAL CONFIDENTIAL

MODEL NAME : *JAL20*

PCB NO : *LA-4041P (DA800009Y1L)*

BOM NO : *43153231L01(TPM)*

*43153231L02 (Non TPM)*

## M09 Maybach UMA

### uFCPGA Mobile Penryn Intel Cantiga GM + ICH9M

<http://hobi-elektronika.net/>

## 2008-06-16

### REV : 1.0(A00)

@ : Nopop Component

3@ : disable TPM

4@ : enable TPM

Fix Function Field

MB PCB	
Part Number	Description
DA800009Y1L	PCB 03N LA-4041P REV1 M/B

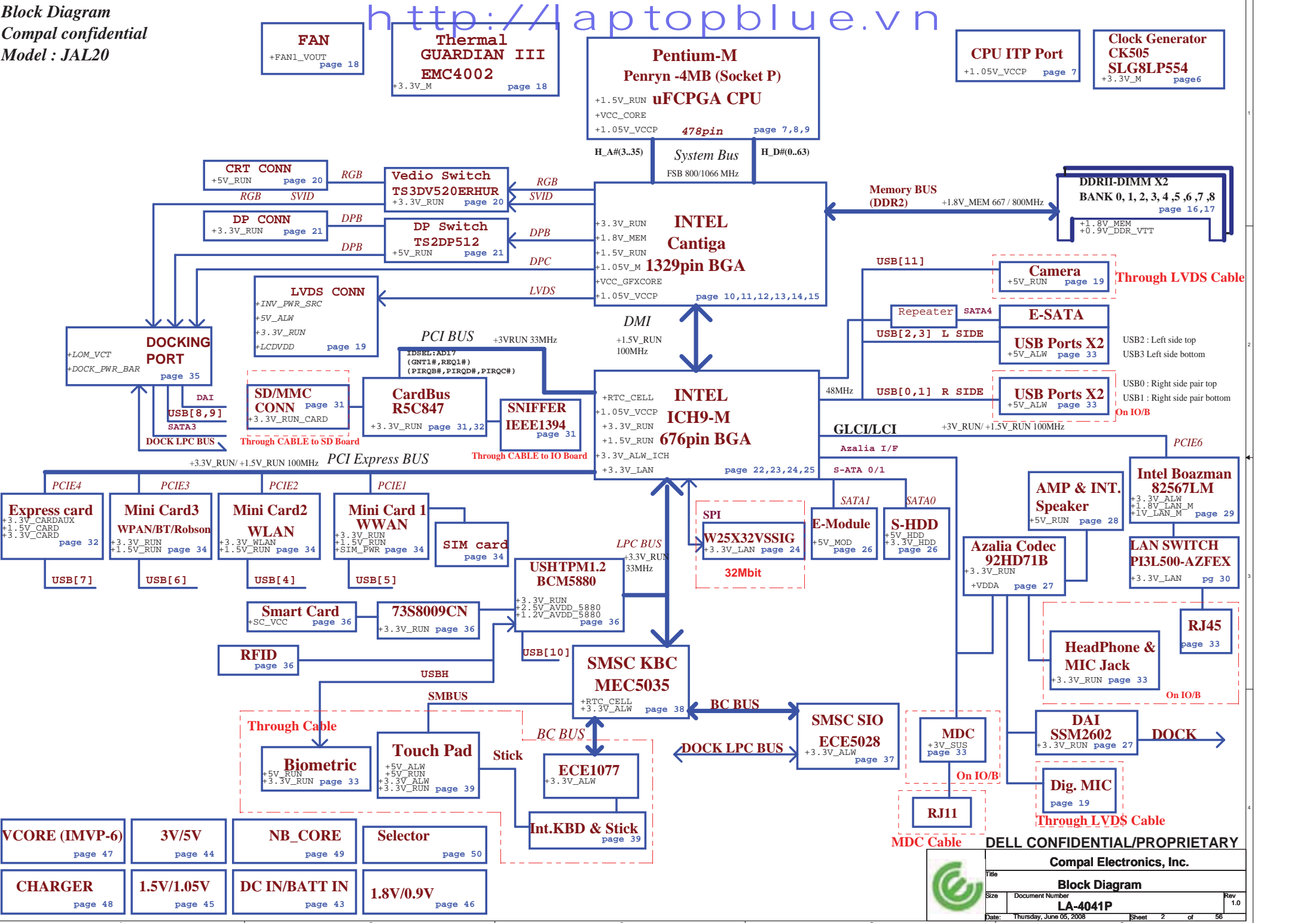
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## POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

## PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_ICH +3.3V_RTC_LDO	+3.3V_SUS +1.8V_MEM	+5V_RUN +3.3V_RUN +2.5V_RUN +1.5V_RUN +0.9V_DDR_VTT +VCC_GFXCORE +VCC_CORE +1.05V_VCCP	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

## PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C847	AD17	REQ#1 / GNT#1	PIRQ[B..D]

ICH9-M	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side Top)
	1	JUSB1 (Ext Right Side Bottom)
	2	JESA1 (Ext Left Side Top)
	3	JESA1 (Ext Left Side Bottom)
	4	WLAN
	5	WWAN
	6	WPAN
	7	Card Bus/Express card
	8	DOCKING
	9	DOCKING
	10	USH->BIO
	11	Camera

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PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 BT/UWB
Lane 4	EXPRESS CARD
Lane 5	None
Lane 6	10/100/1G LAN

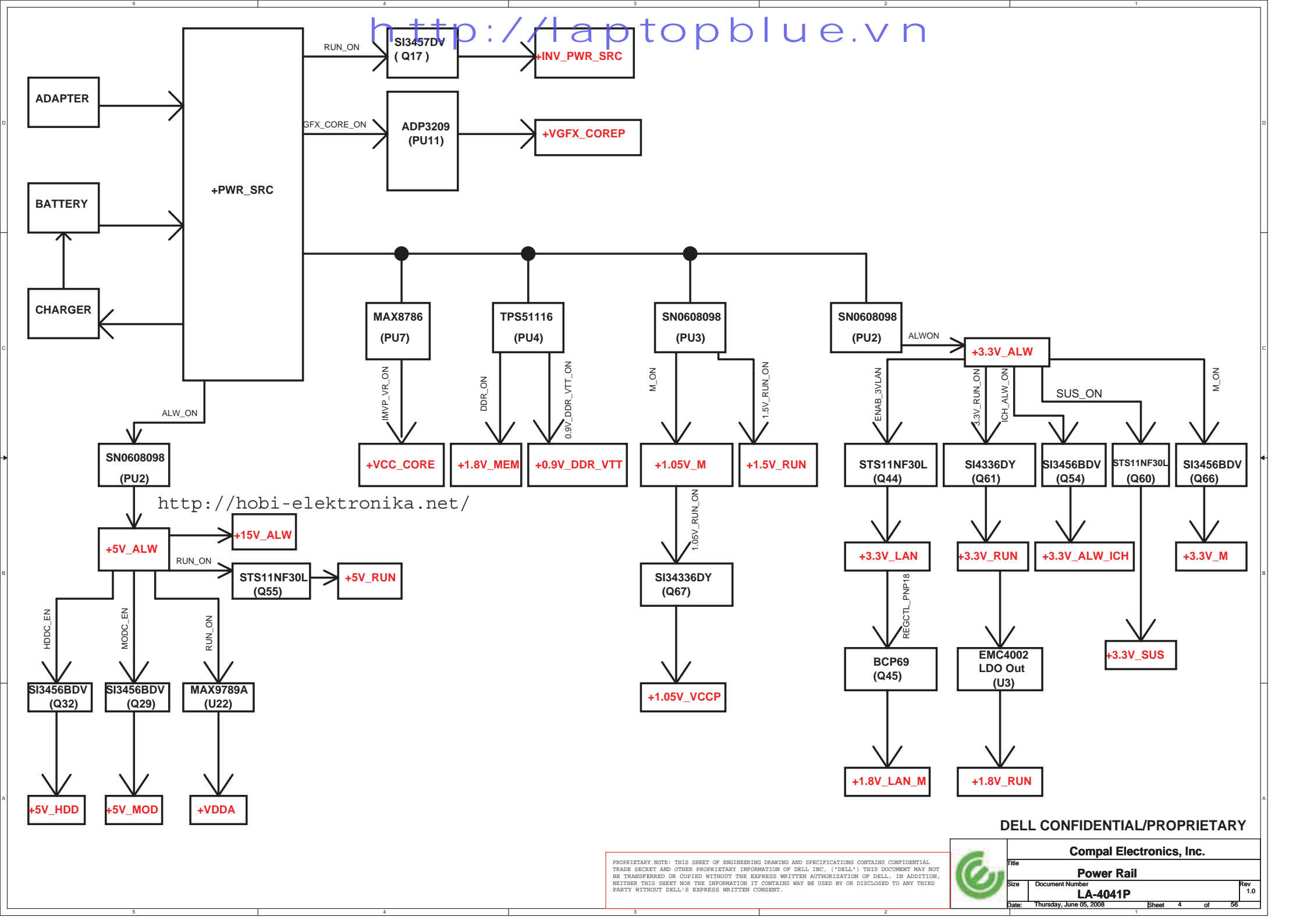
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[illegible][illegible][illegible]

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The diagram illustrates the power rail architecture, starting from external sources (ADAPTER, BATTERY, CHARGER) connected to the main power source (+PWR\_SRC). This source feeds several primary regulators:

- MAX8786 (PU7)**: Controls **+VCC\_CORE**, **+1.8V\_MEM**, and **+0.9V\_DDR\_VTT**.
- TPS51116 (PU4)**: Controls **+1.8V\_MEM** and **+0.9V\_DDR\_VTT**.
- SN0608098 (PU3)**: Controls **+1.05V\_M** and **+1.5V\_RUN**.
- SN0608098 (PU2)**: Controls **+3.3V\_ALW**, **+3.3V\_LAN**, **+3.3V\_RUN**, **+3.3V\_ALW\_ICH**, **+3.3V\_M**, and **+3.3V\_SUS**.

Secondary regulators and outputs include:

- +5V\_ALW** (SN0608098 PU2) leading to **+5V\_HDD**, **+5V\_MOD**, and **+VDDA**.
- +1.05V\_VCCP** (SI34336DY Q67) derived from **+1.05V\_M**.
- +1.8V\_LAN\_M** (BCP69 Q45) derived from **+3.3V\_LAN**.
- +1.8V\_RUN** (EMC4002 LDO Out U3) derived from **+3.3V\_RUN**.

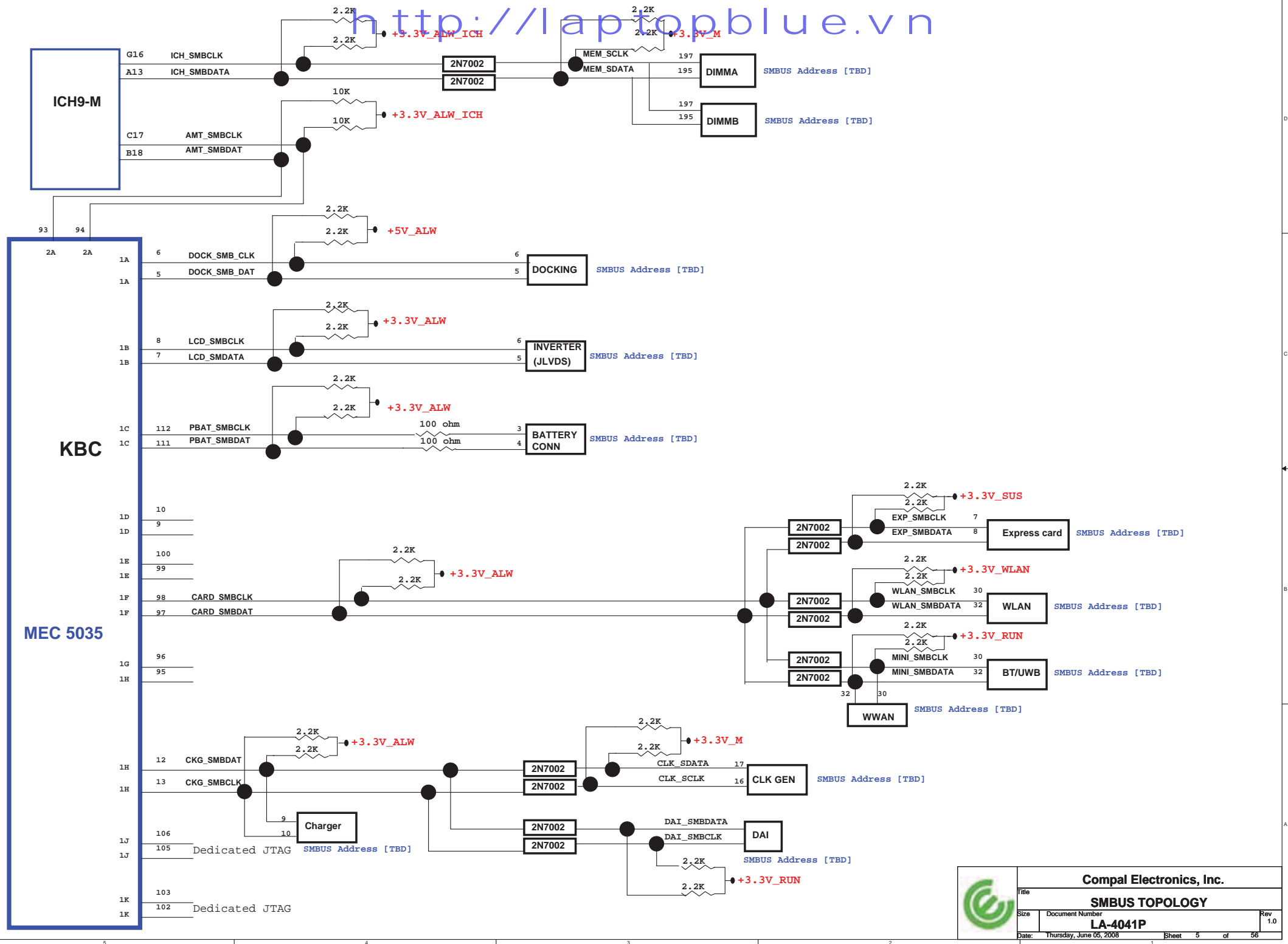
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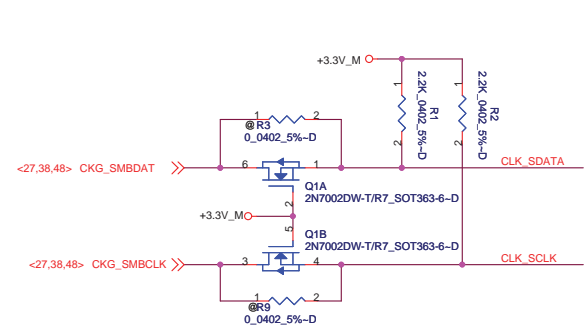
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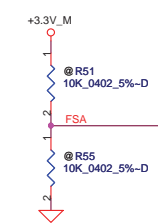
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FSC	CLKSEL2	FSB	CLKSEL1	FSA	CLKSEL0	CPU	MHz	SRC	MHz	PCI	MHz
0	0	0	0	0	0	266	100	33.3			
0	0	1	1	1	1	133	100	33.3			
0	1	0	0	0	0	200	100	33.3			
0	1	1	1	1	1	166	100	33.3			
1	0	0	0	0	0	333	100	33.3			
1	0	1	1	1	1	100	100	33.3			
1	1	0	0	0	0	400	100	33.3			



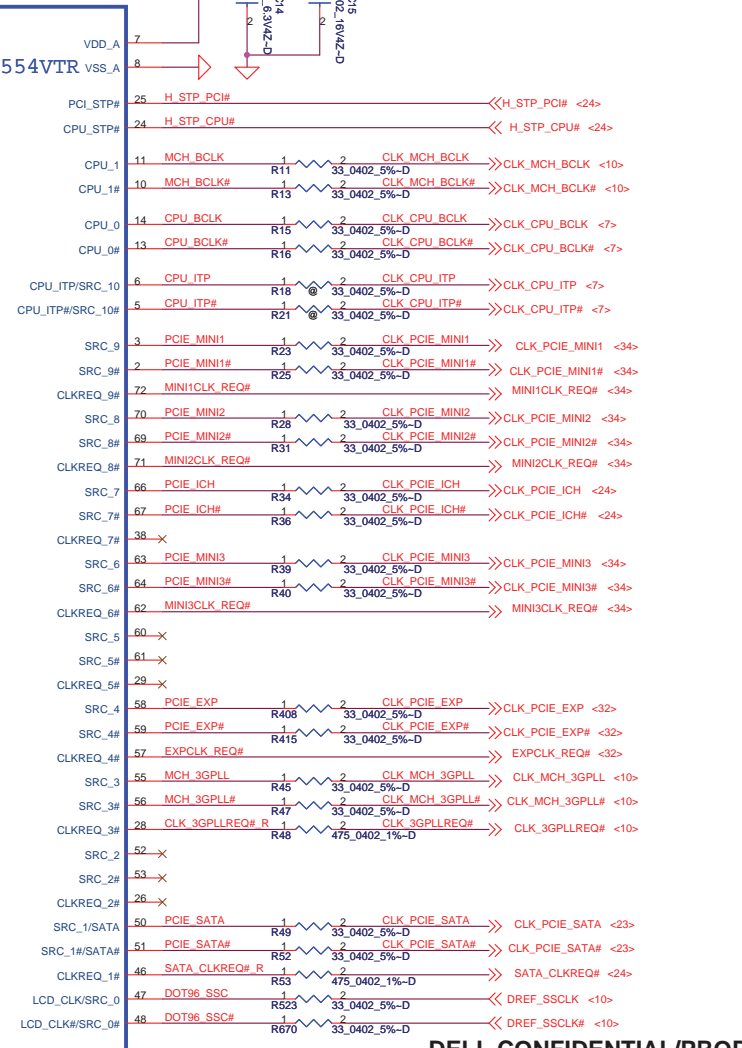
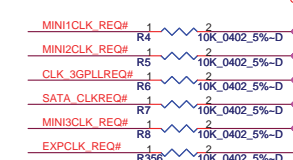
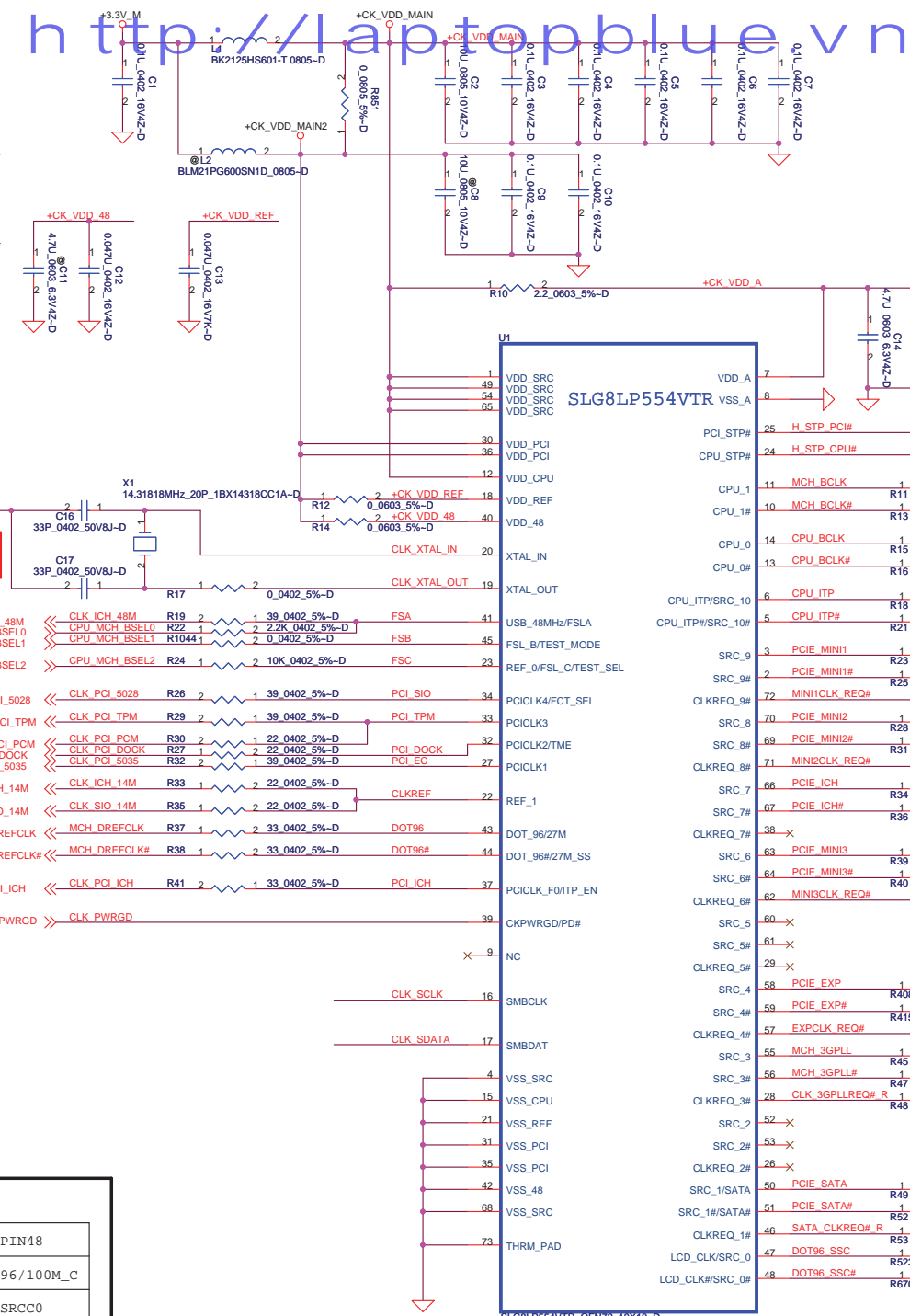
TME	PIN 32
0	overclocking enabled
1	overclocking disabled

ITP_EN	PIN 37
0	Pin 5/6 as SRC_10
1	Pin 5/6 as CPU_ITP

FCTSEL1	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1=DIS	27M_out	27M SSout	SRCT0	SRCC0

0=UMA  
1=Disc. GRFX down

Place crystal within 500 mils of CK505



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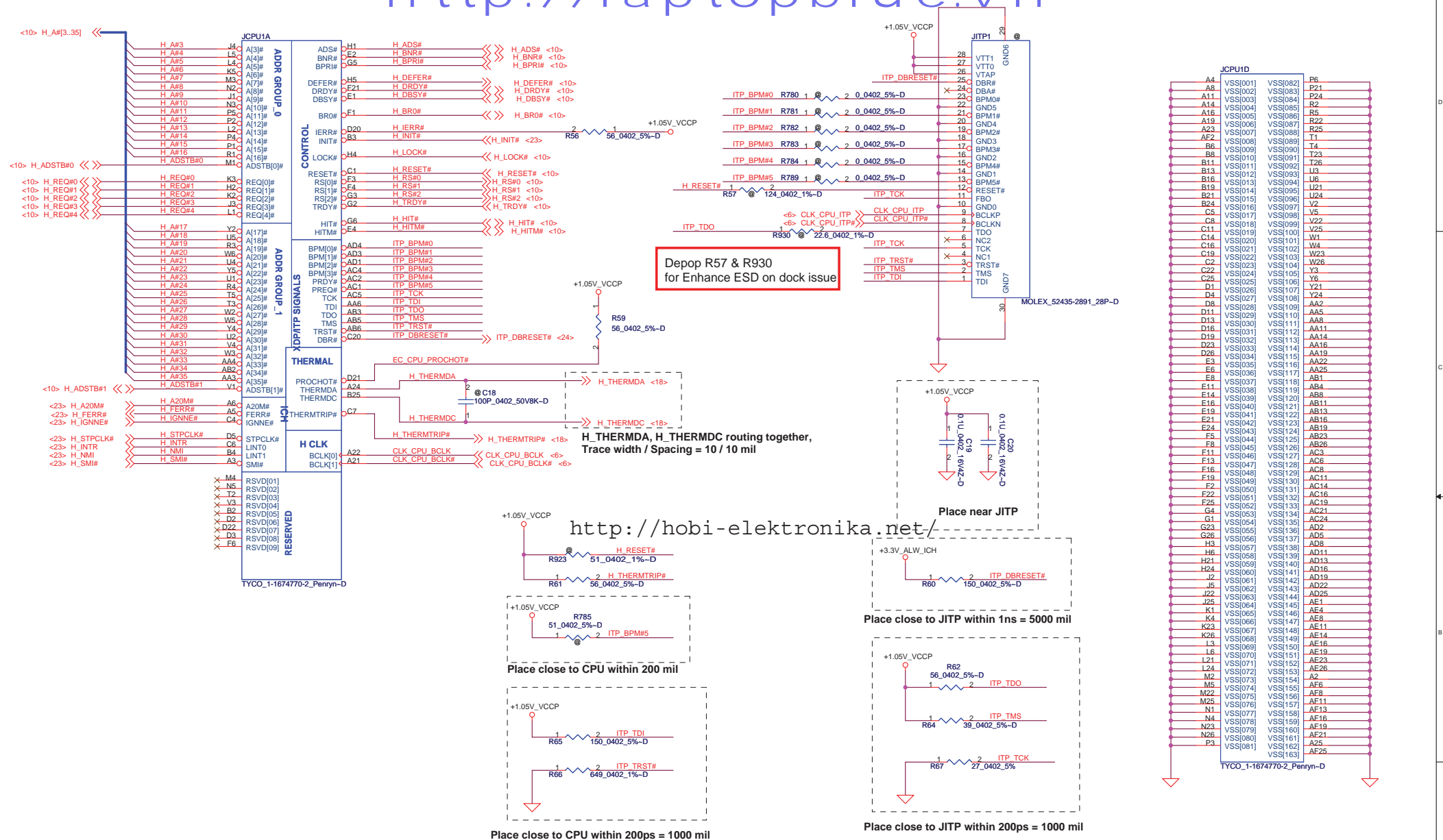
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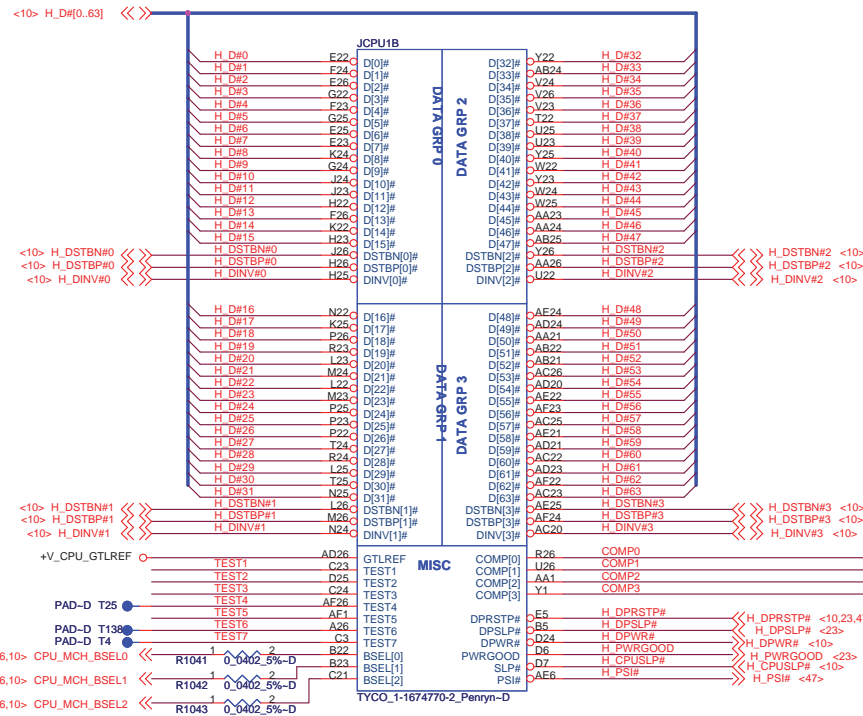
Clock Generator

LA-4041P

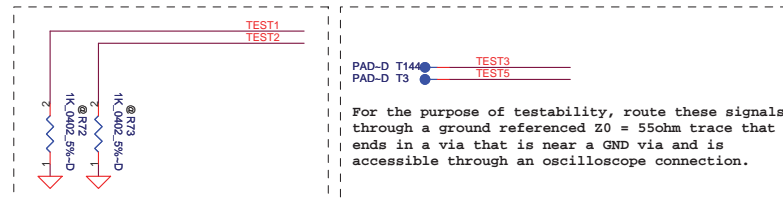
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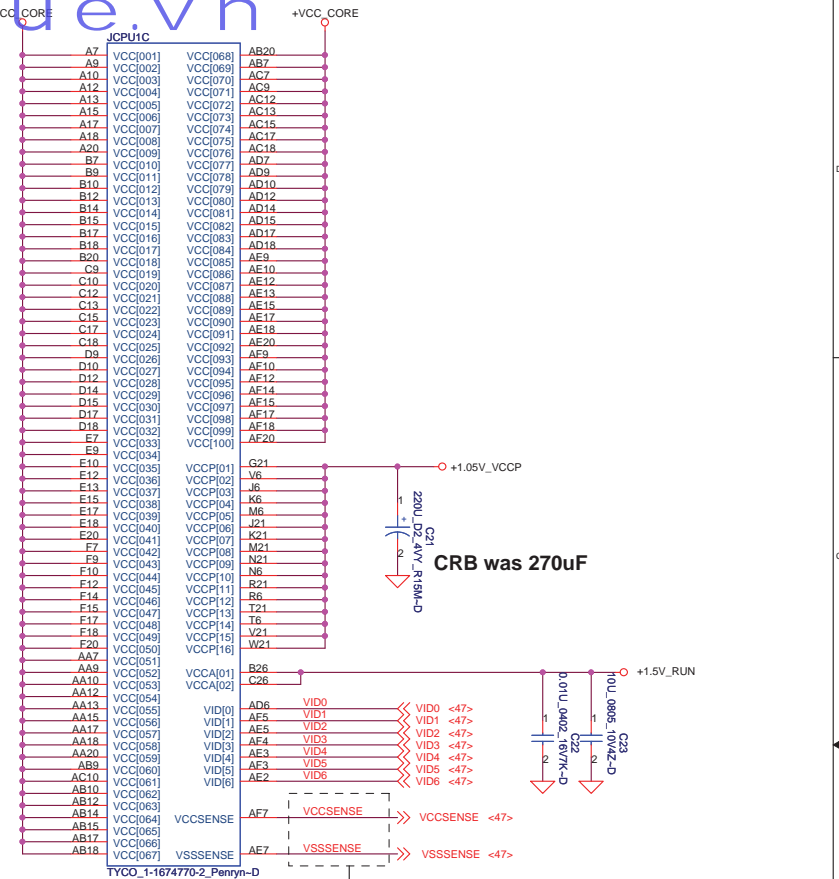
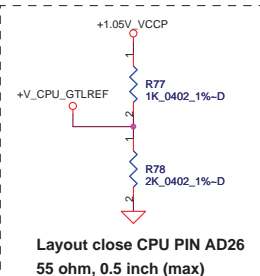




Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP0, COMP2 trace should be 27.4 ohm. COMP1, COMP3 should be 55 ohm.

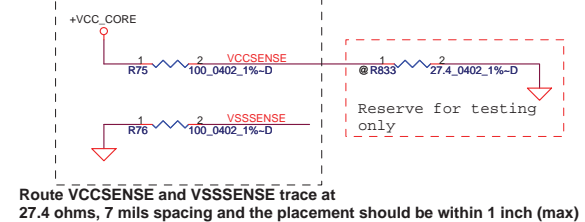


FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0



Length match within 25 mils, Z0=27.4 ohm

Place R75 and R76 near CPU



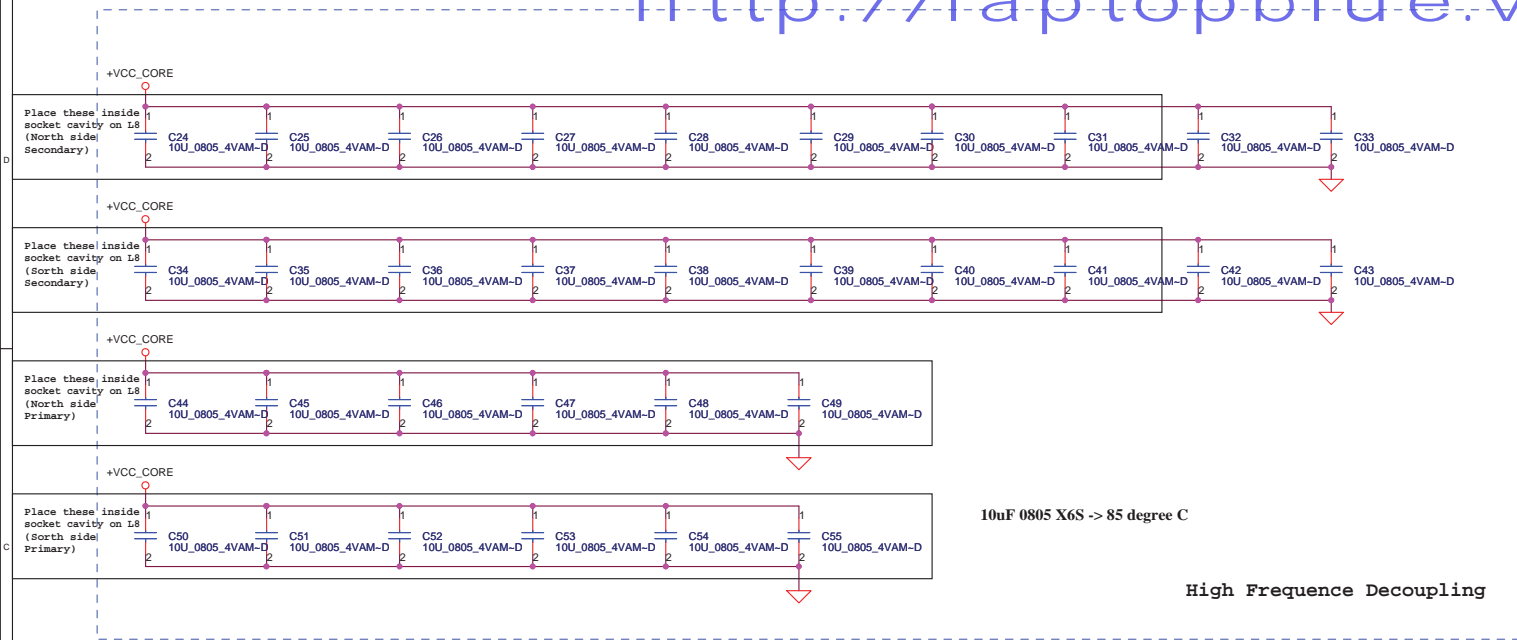
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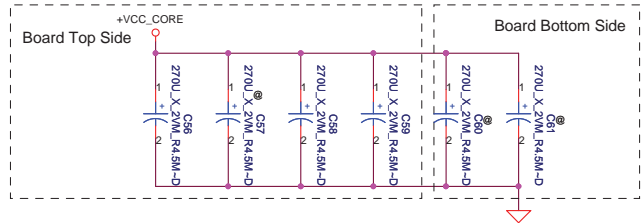
Penryn Processor(2/2)			
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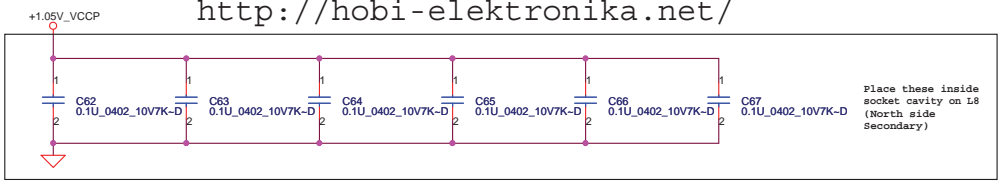


Near VCORE regulator.



ESR <= 1.5m ohm  
Capacitor > 1320uF

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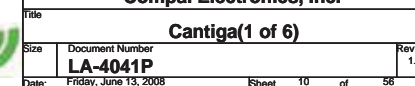
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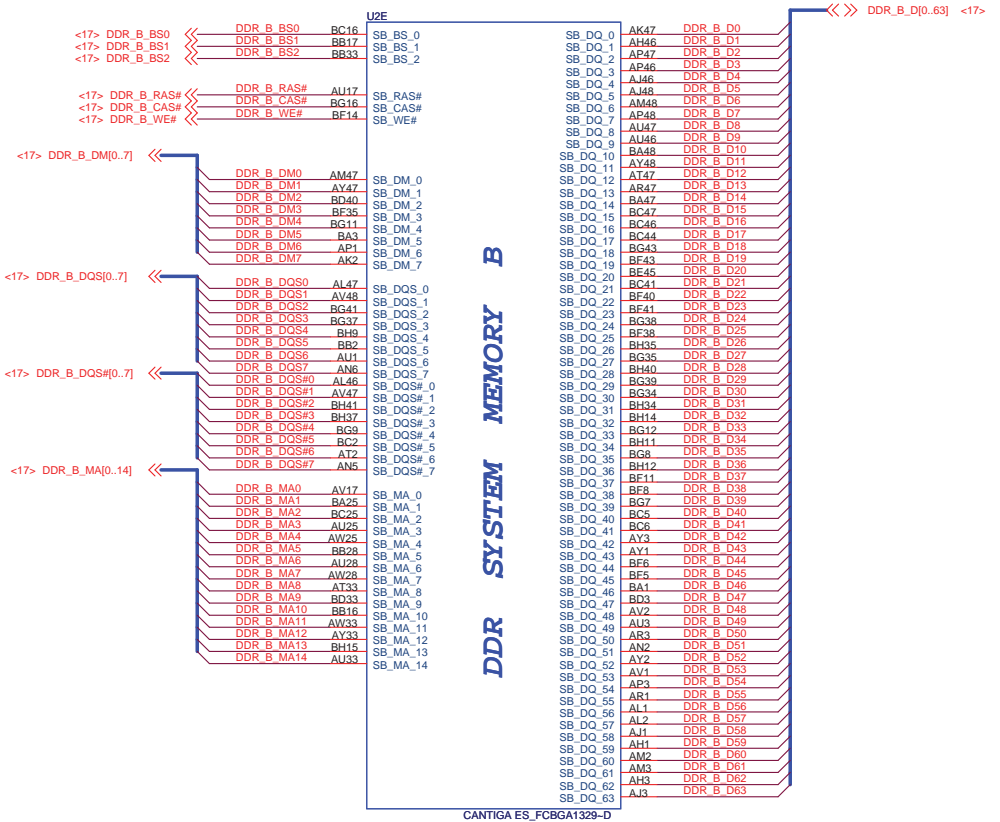
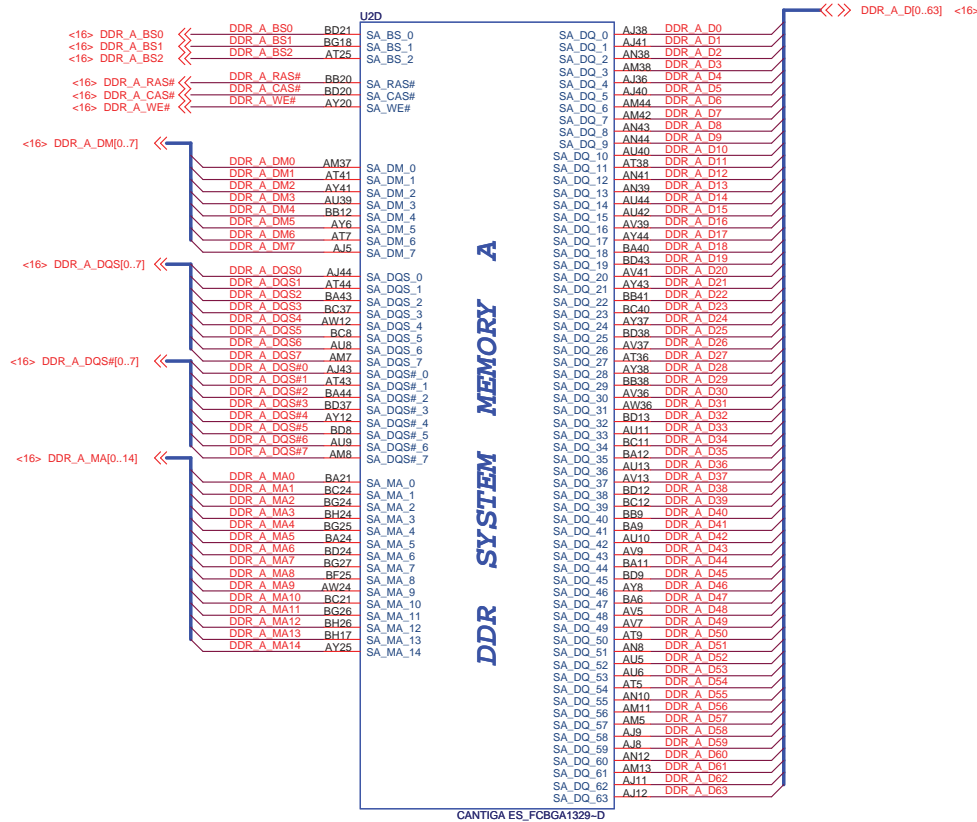
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CPU Bypass

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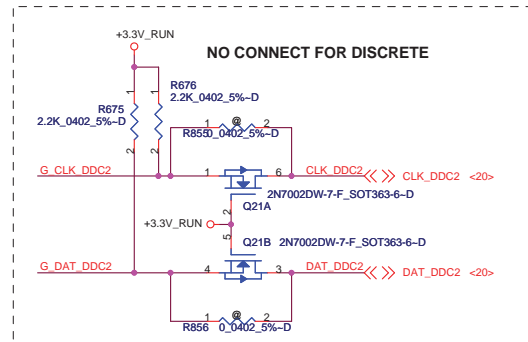


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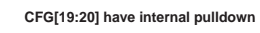
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Cantiga(2 of 6)

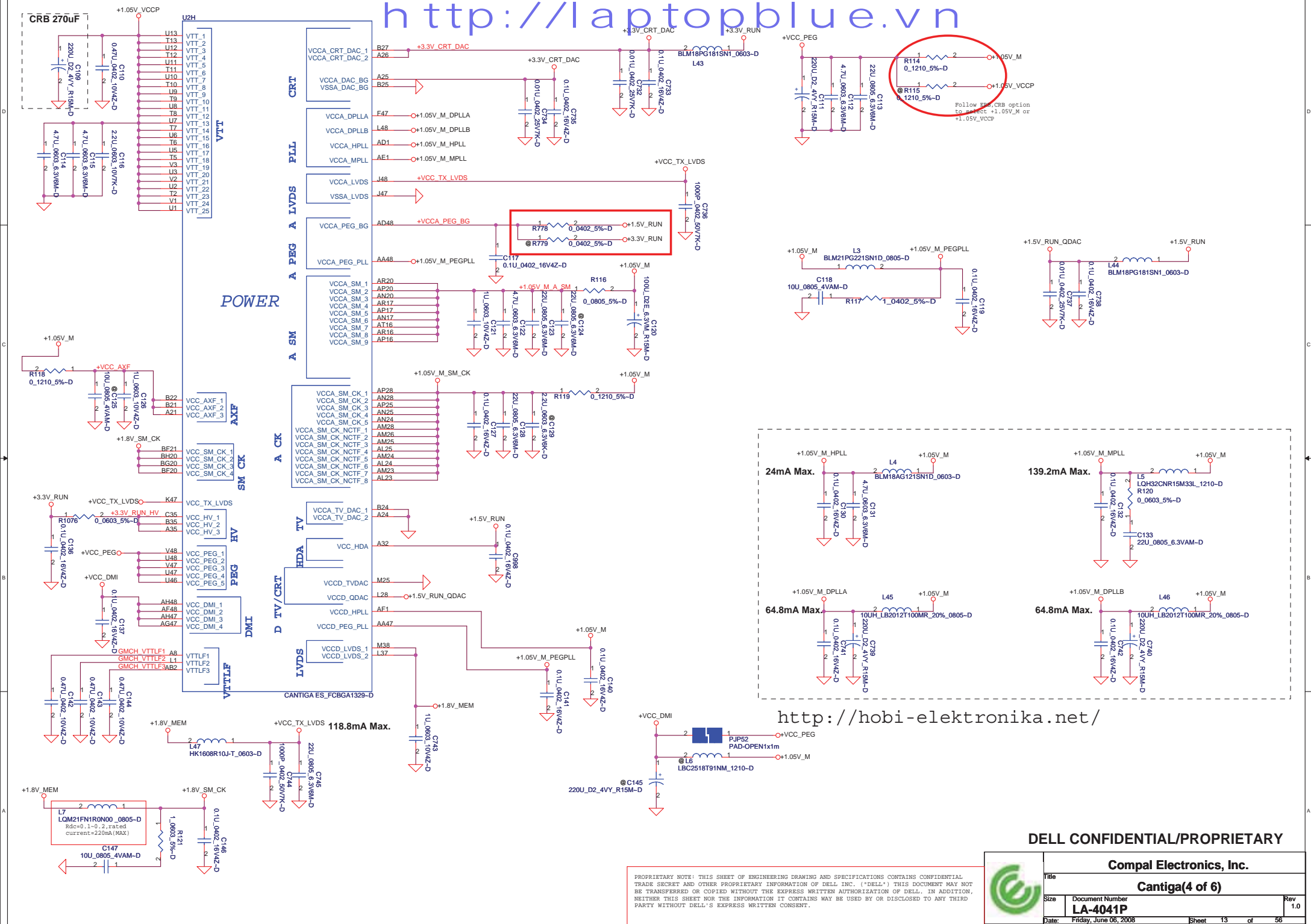
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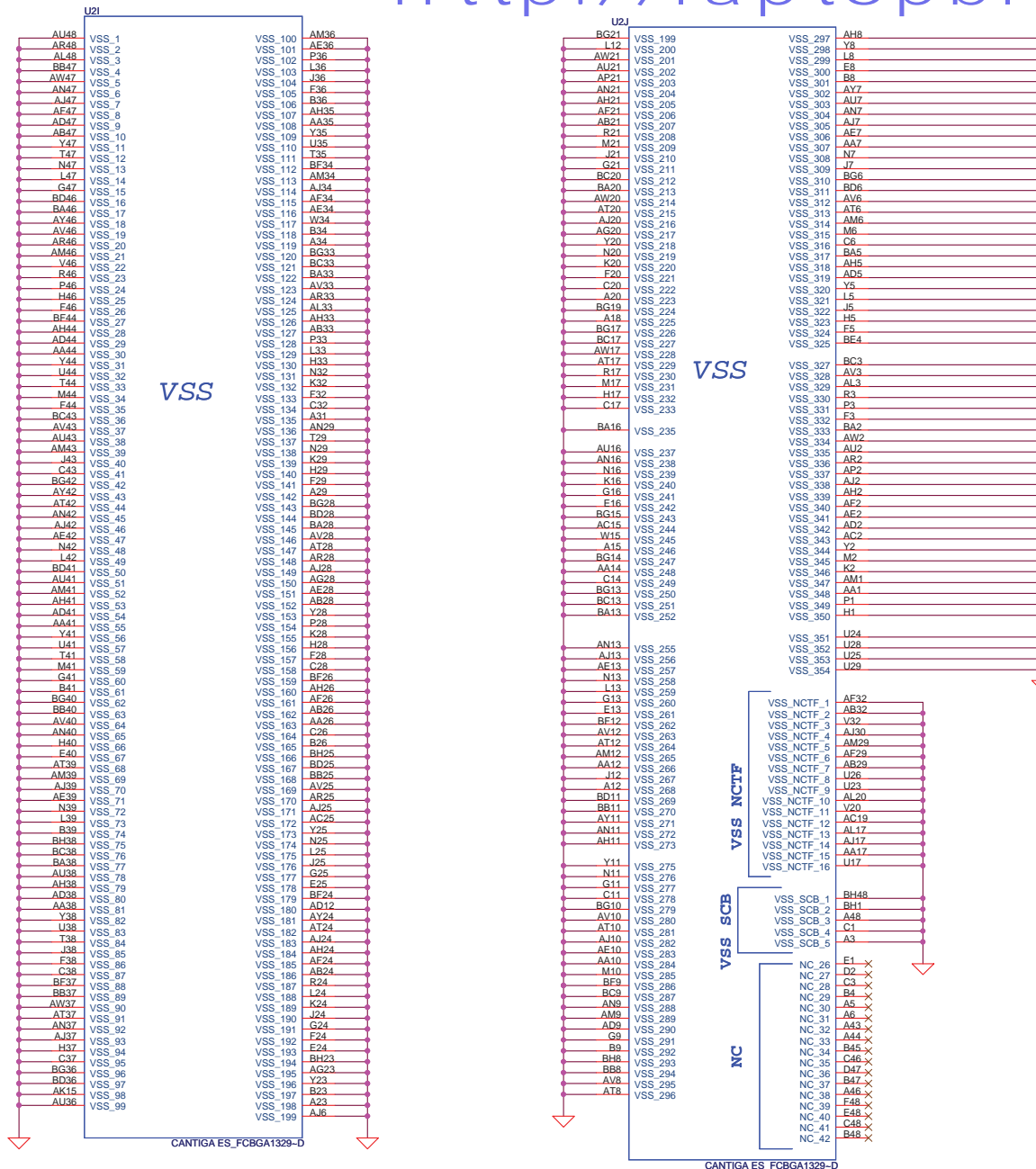
The diagram shows five horizontal signal lines labeled <10> CPG5, <10> CPG6, <10> CPG7, <10> CPG9, and <10> CPG16. Each line has a red arrow pointing right, indicating a signal transition. Below each line, a blue waveform shows a pulse. The pulse width is labeled as 2.21K\_0402 1%-D. The pulse is labeled with @R106, @R107, @R108, @R109, and @R110 respectively. Below the waveforms, the text 'CFG[5:16] have internal pullup' is written, with a red triangle pointing to the right, indicating the pullup configuration.



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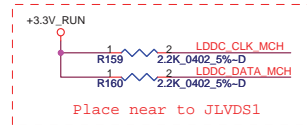
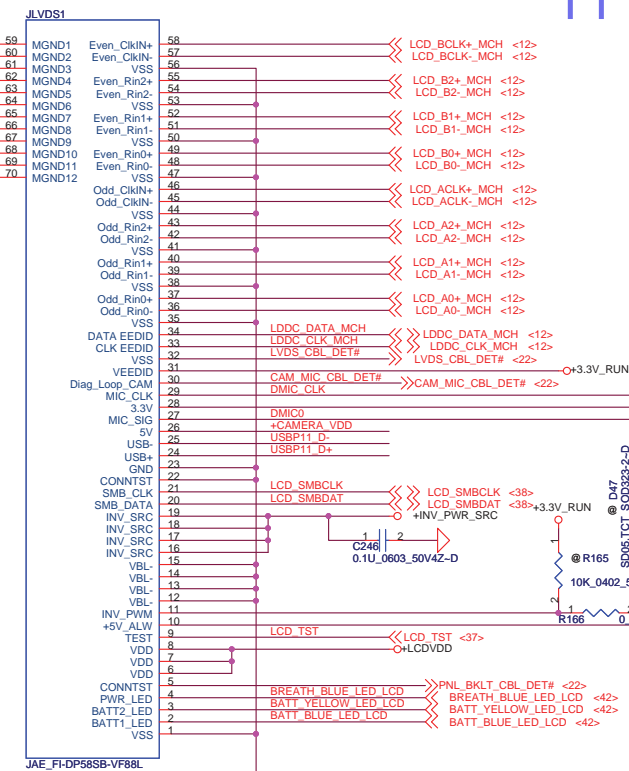




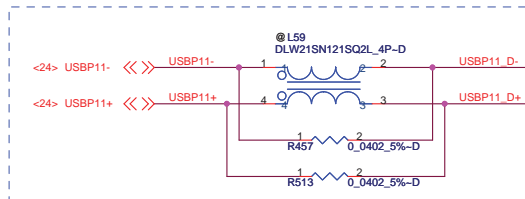
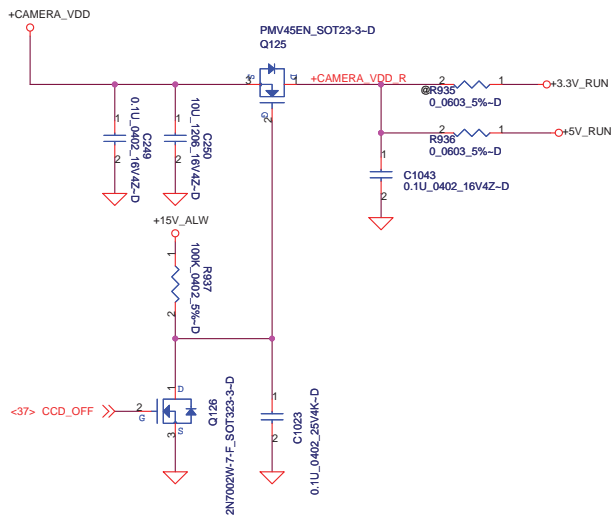
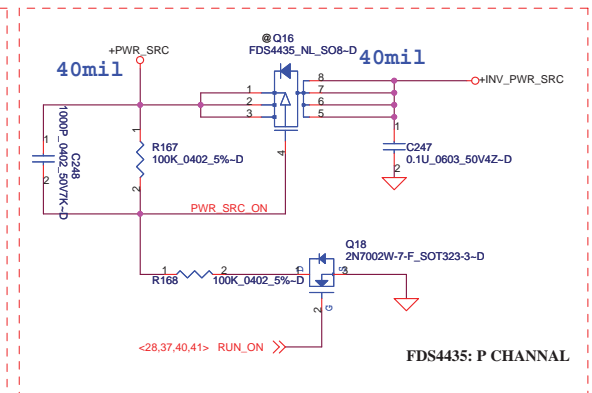
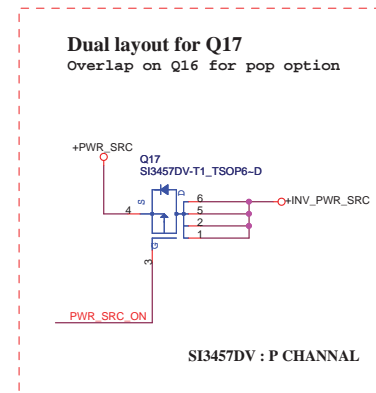
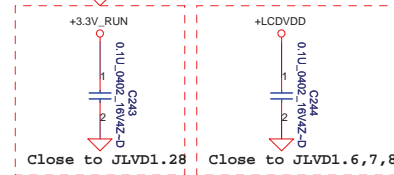
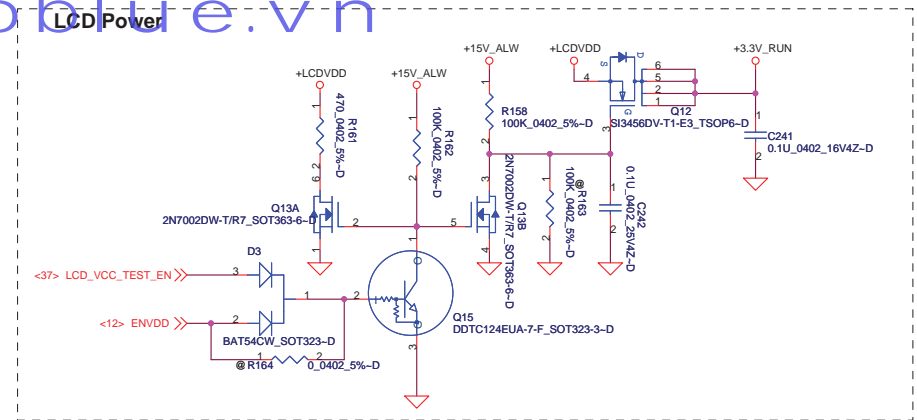
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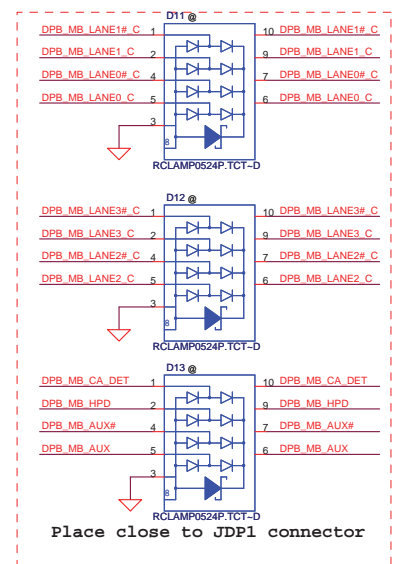
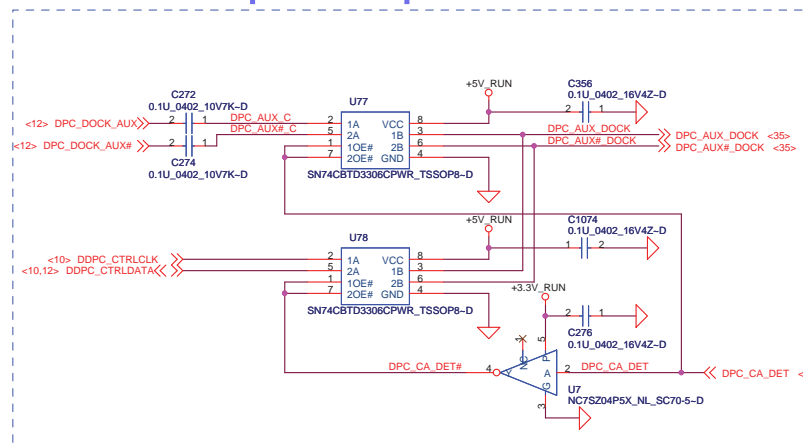


Part Number	Description
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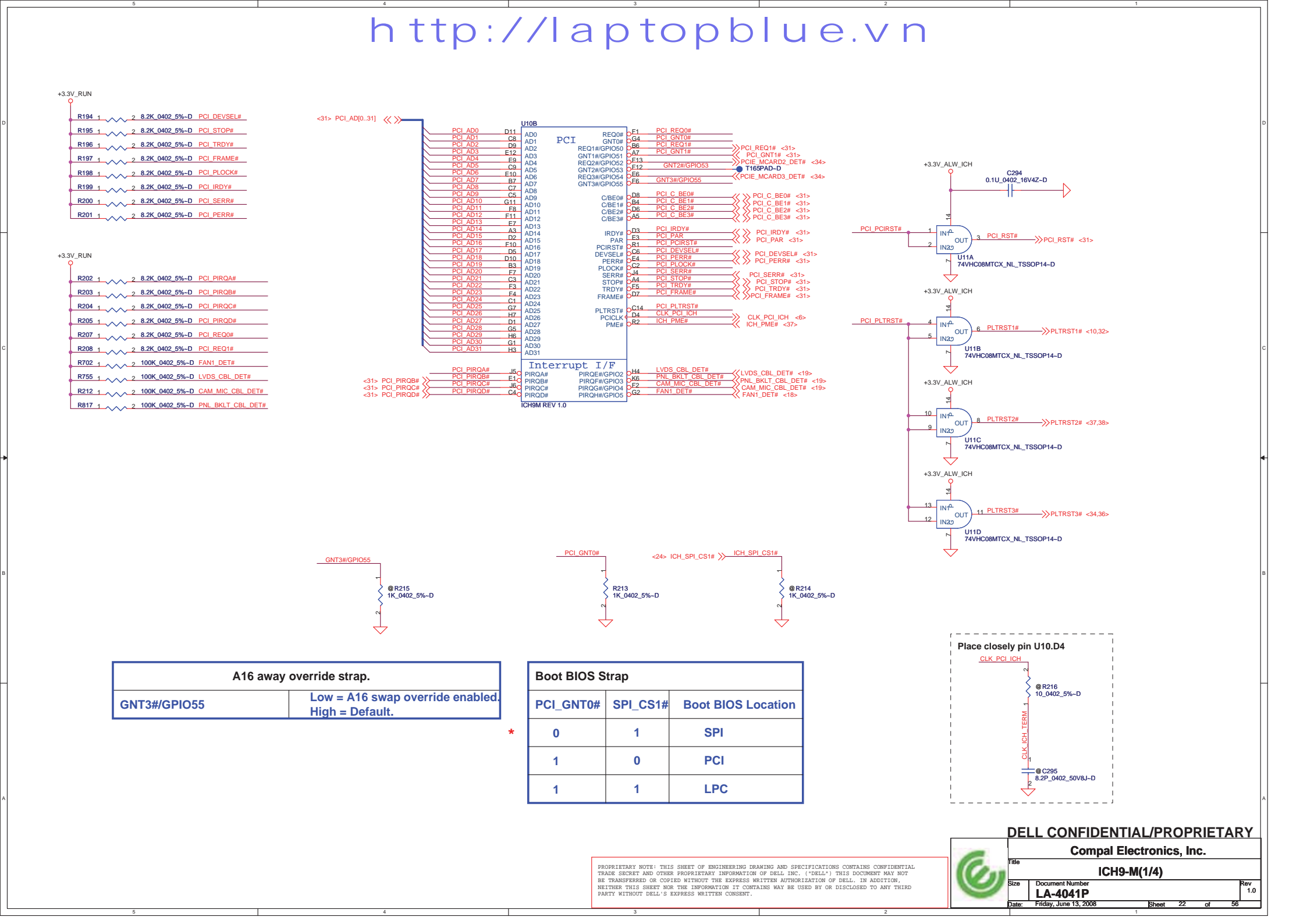


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**A16 away override strap.**

GNT3#/GPIO55	Low = A16 swap override enabled. High = Default.

**Boot BIOS Strap**

PCI_GNT0#	SPI_CS1#	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC

**Place closely pin U10.D4**

CLK_PCI_ICH	CLK_ICH_TERM

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GNT3#/GPIO55	Low = A16 swap override enabled. High = Default.

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PCI_GNT0#	SPI_CS1#	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC

**Place closely pin U10.D4**

CLK_PCI_ICH	CLK_ICH_TERM

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GNT3#/GPIO55	Low = A16 swap override enabled. High = Default.

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PCI_GNT0#	SPI_CS1#	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC

**Place closely pin U10.D4**

CLK_PCI_ICH	CLK_ICH_TERM

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The schematic diagram illustrates the ICH9-M(1/4) chip and its connections. The central component is the ICH9M REV 1.0 chip, which includes a PCI controller (U10B) and an Interrupt I/F (U10B). The chip is connected to various pins, including PCI\_A0# through PCI\_A31#, PCI\_B0# through PCI\_B31#, PCI\_C0# through PCI\_C31#, PCI\_D0# through PCI\_D31#, PCI\_E0# through PCI\_E31#, PCI\_F0# through PCI\_F31#, PCI\_G0# through PCI\_G31#, PCI\_H0# through PCI\_H31#, PCI\_I0# through PCI\_I31#, PCI\_J0# through PCI\_J31#, PCI\_K0# through PCI\_K31#, and PCI\_L0# through PCI\_L31#.

The diagram also shows the connection of the chip to various components, including resistors (R194-R201, R202-R208, R702, R755, R817, R213, R214, R215, R216), capacitors (C294, C295), and integrated circuits (U10B, U11A, U11B, U11C, U11D).

**A16 away override strap.**

GNT3#/GPIO55	Low = A16 swap override enabled. High = Default.
0	Low
1	High

**Boot BIOS Strap**

PCI_GNT0#	SPI_CS1#	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC

**Place closely pin U10.D4**

CLK_PCI_ICH	CLK_ICH_TERM
1	1
2	2

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Size: Document Number  
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Rev: 1.0

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# http://laptopblue.vn

**A16 away override strap.**

GNT3#/GPIO55	Low = A16 swap override enabled. High = Default.

**Boot BIOS Strap**

PCI_GNT0#	SPI_CS1#	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC

**Place closely pin U10.D4**

CLK_PCI_ICH	CLK_ICH_TERM

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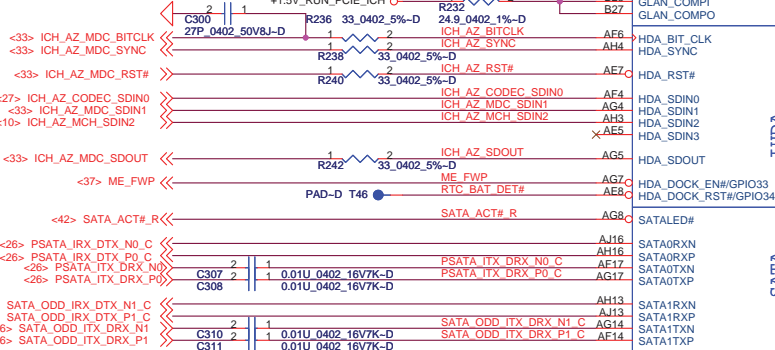
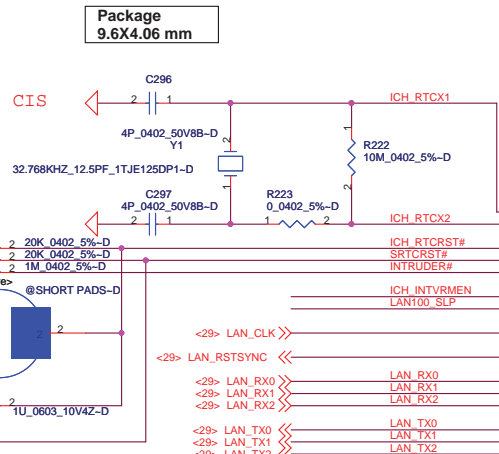
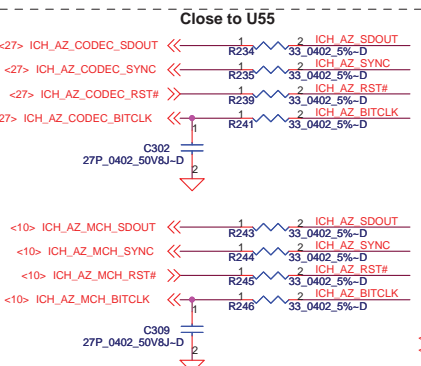
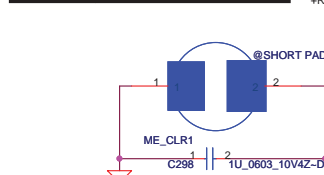
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Size: Document Number  
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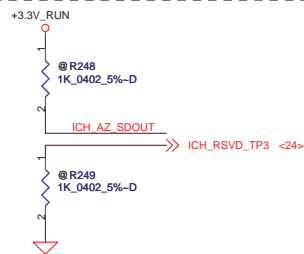
CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



XOR Chain Entrance Strap		
ICH_RSVD_TP3	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1



For WLAN detection issue  
Pin AH4, AG5 has weak internal PD

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ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH9M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

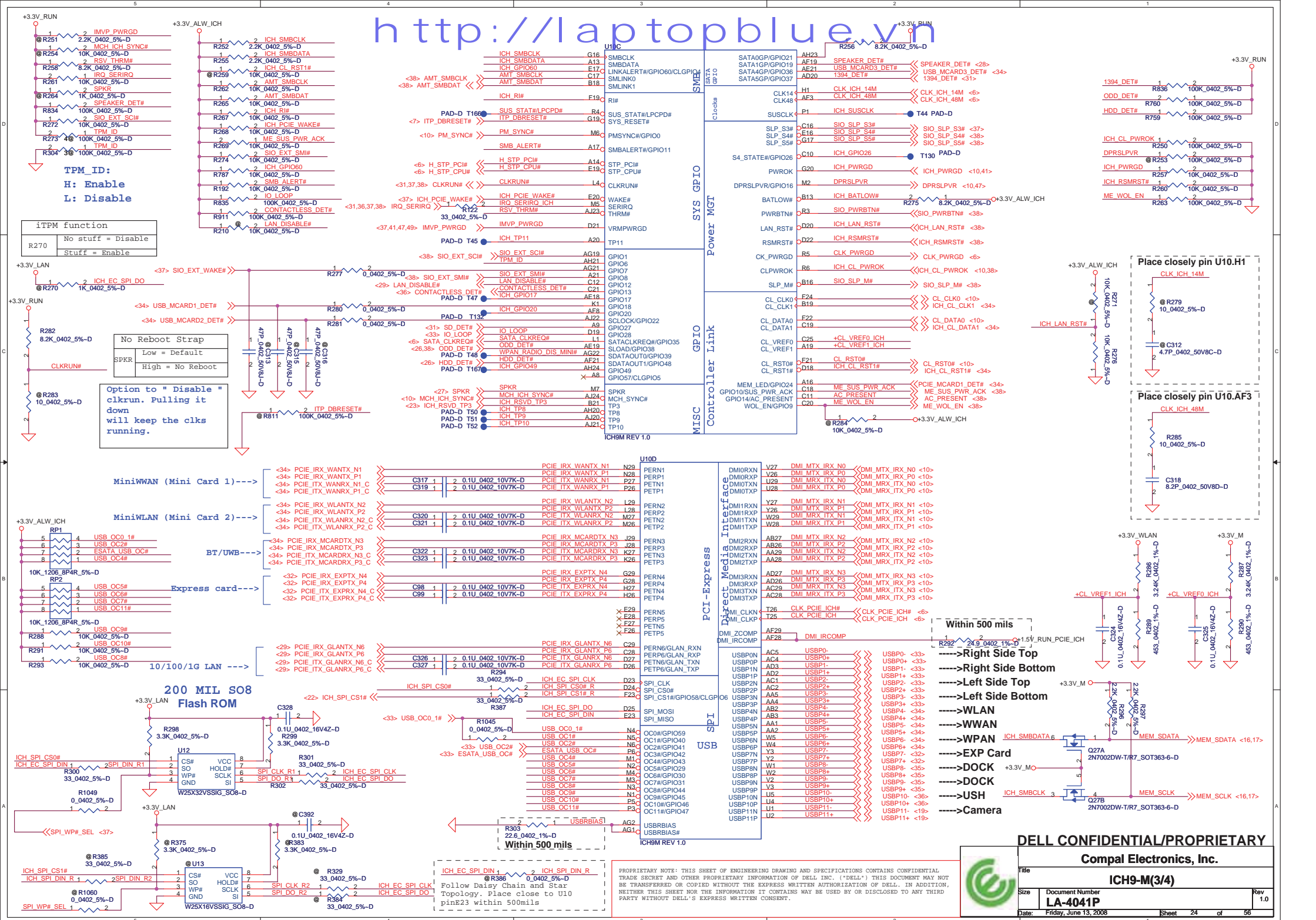


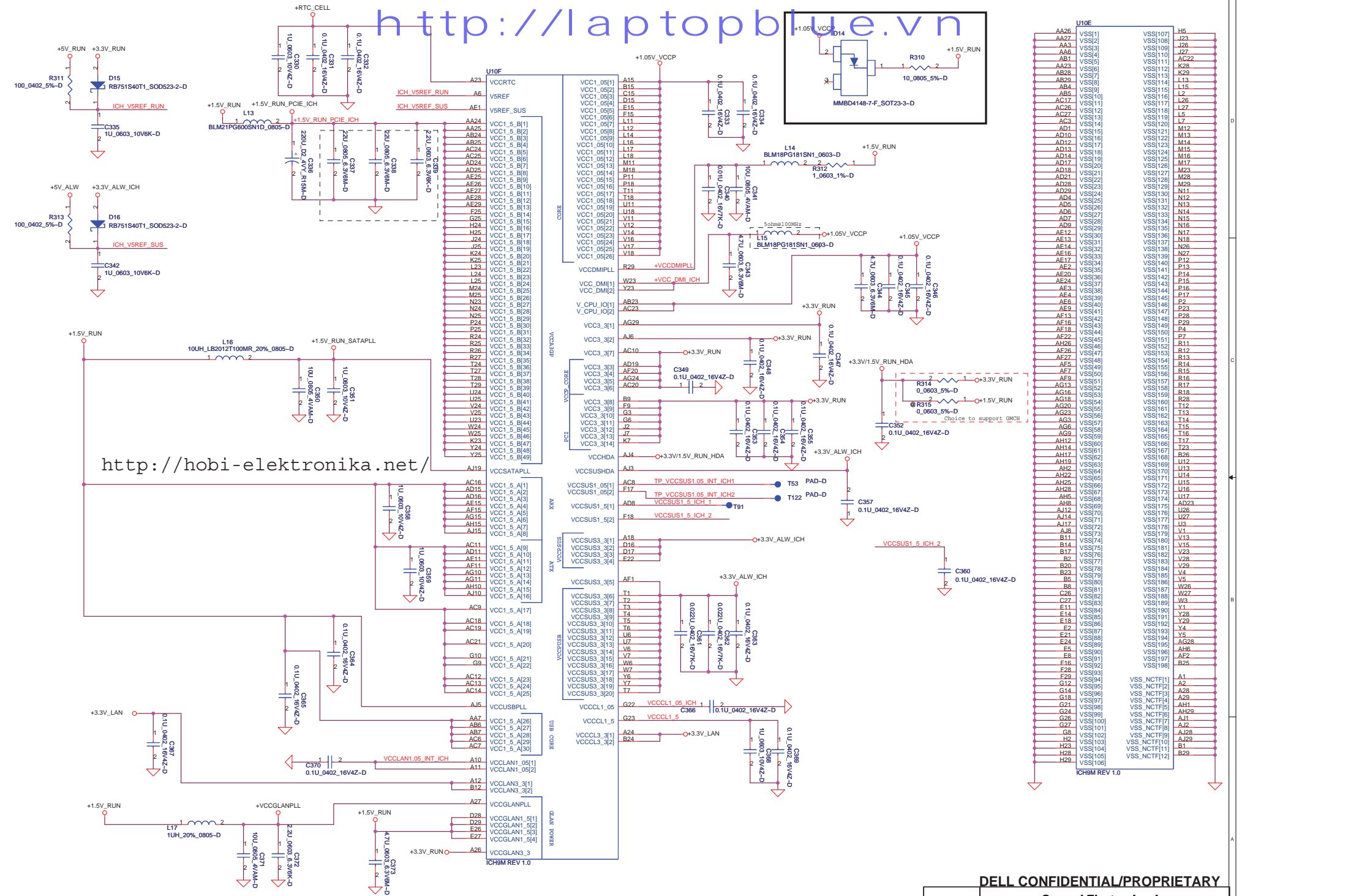
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ICH9-M(2/4)

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Date	Friday, June 13, 2008	Sheet 23 of 56



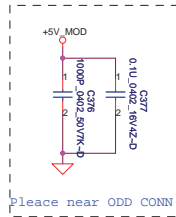


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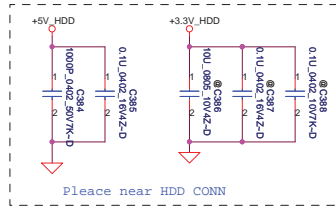
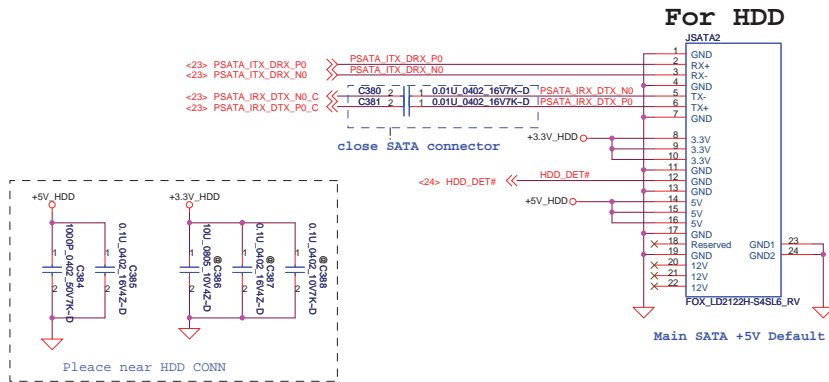
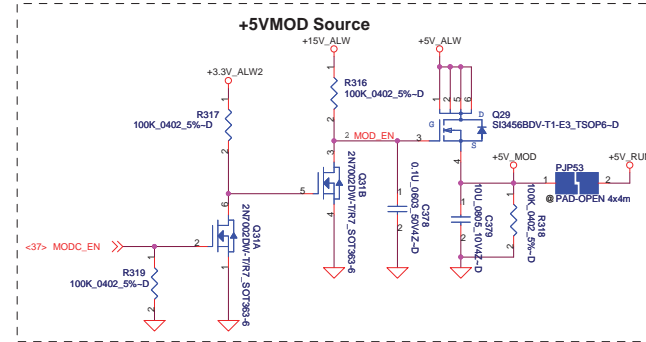
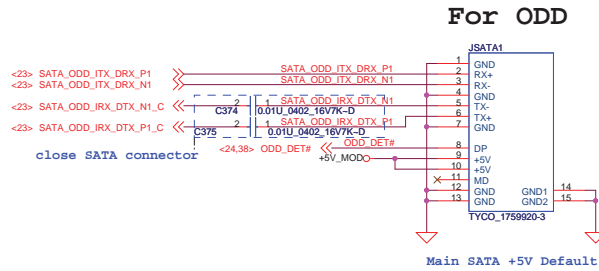
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File	ICH9M(4/4)		
Size	Document Number	LA-4041P	
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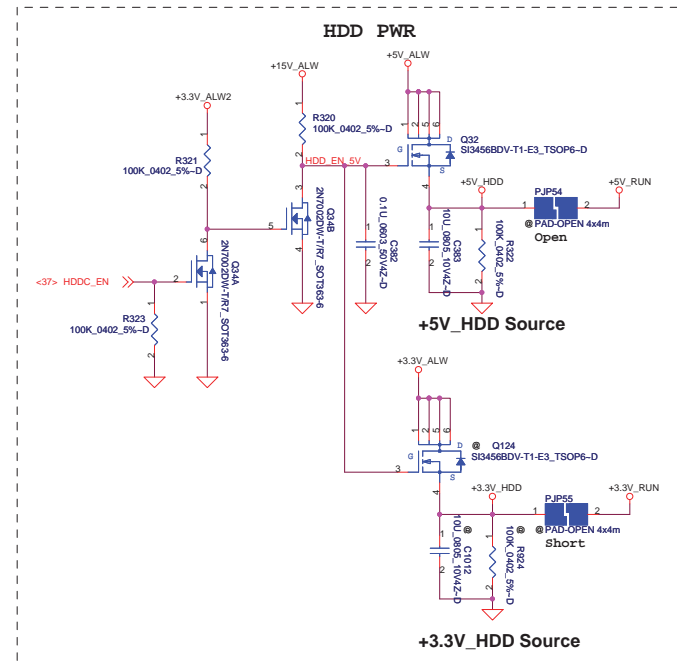
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Please near ODD CONN



Please near HDD CONN



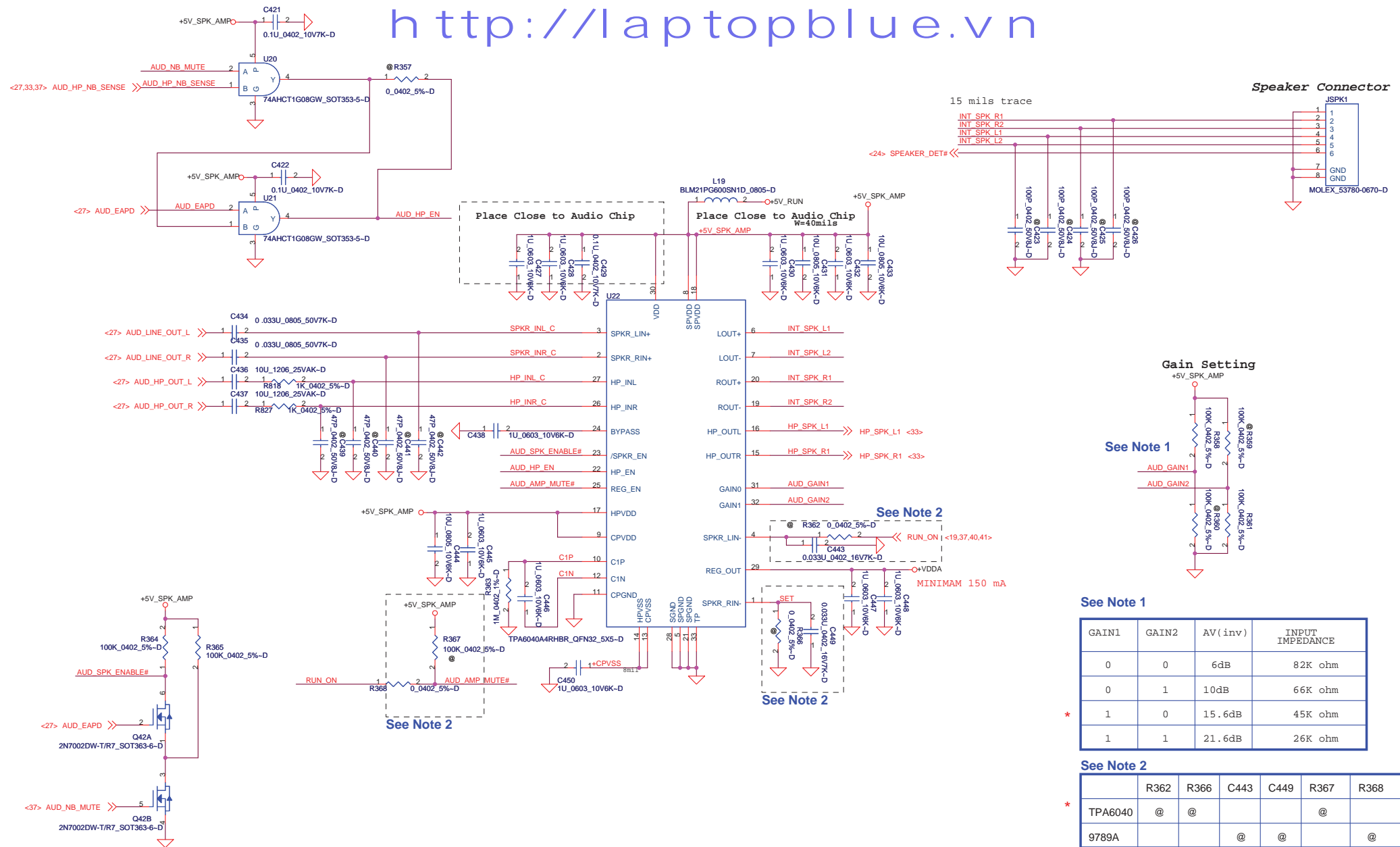
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Title				Rev 1.0
ODD/HDD CONNECTOR				
Size	Document Number			
	LA-4041P			
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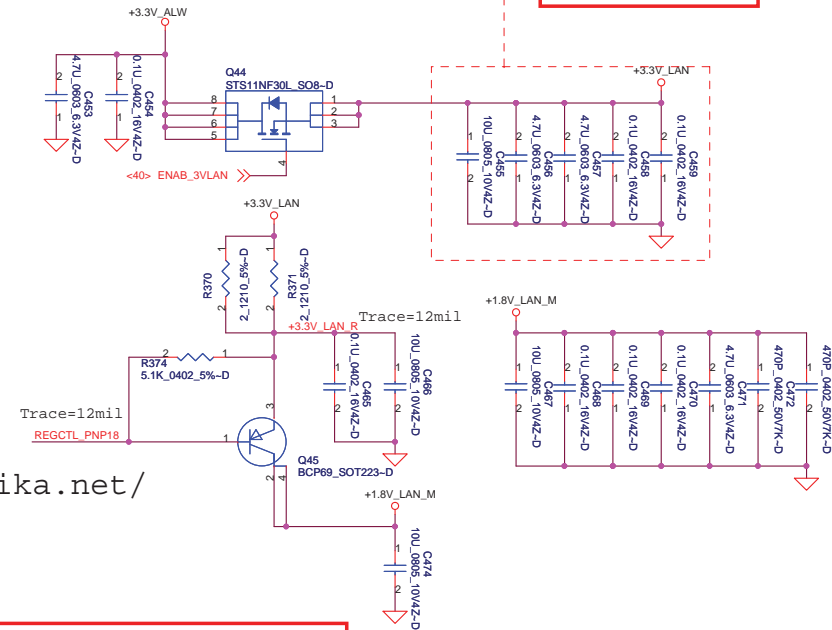
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## AMP and PHONE JACK

**LA-4041P**

Rev	
1.0	

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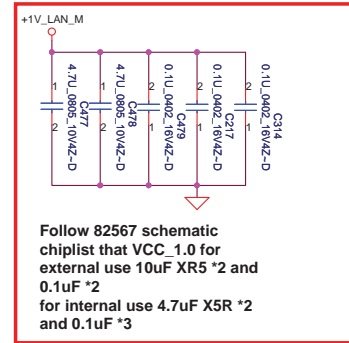
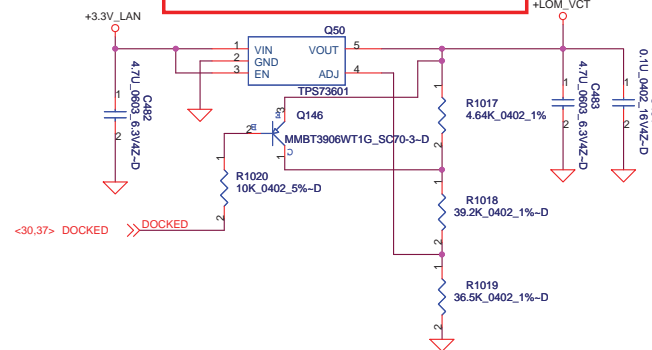


**Need to ensure crystal at least 300uW max power drive-level**

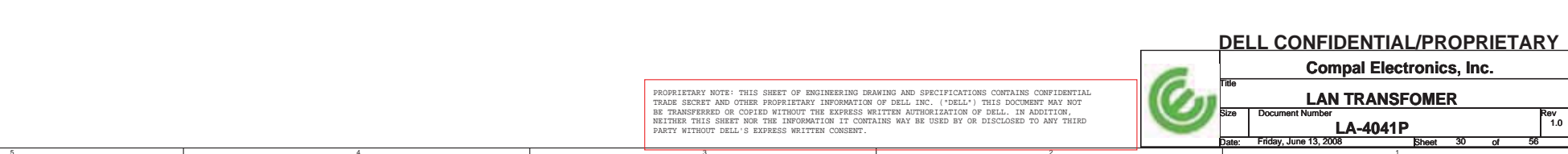
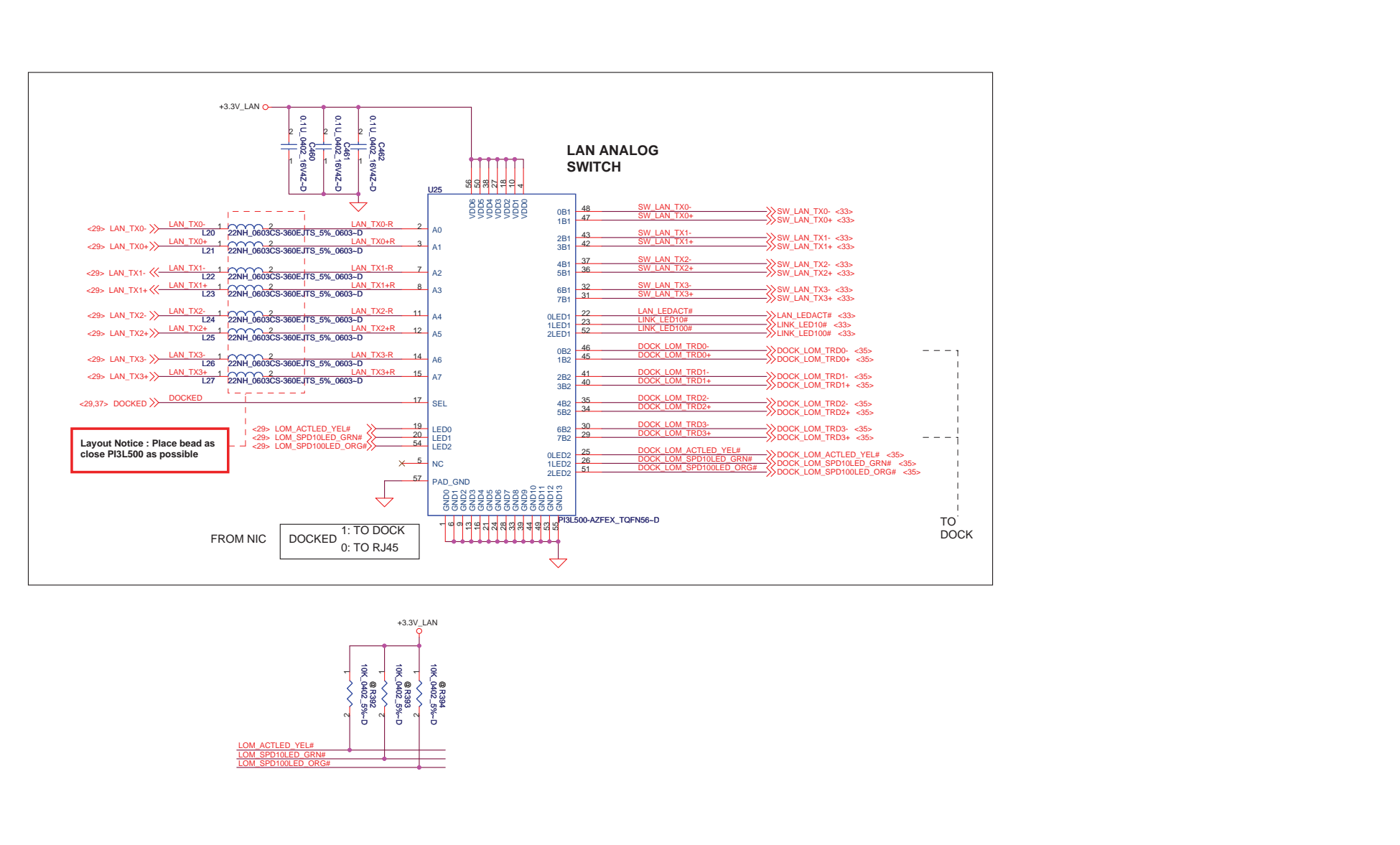
MA use internal 1V,NOT external solutions.  
82567LM:  
B0 version: 1.05V  
A1 version: 1V

+LOM\_VCT = 2.5V (W0/Docking)  
= 2.65V (W/Docking)

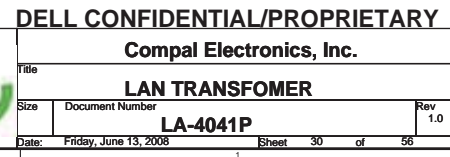
VOUT = 1.204 (1+R1/R2),  
where R1 = R1017 + R1018, R2 = R1019



Follow 82567 schematic  
chiplist that VCC\_1.0 for  
external use 10uF XR5 \*2 and  
0.1uF \*2  
for internal use 4.7uF X5R \*2  
and 0.1uF \*3

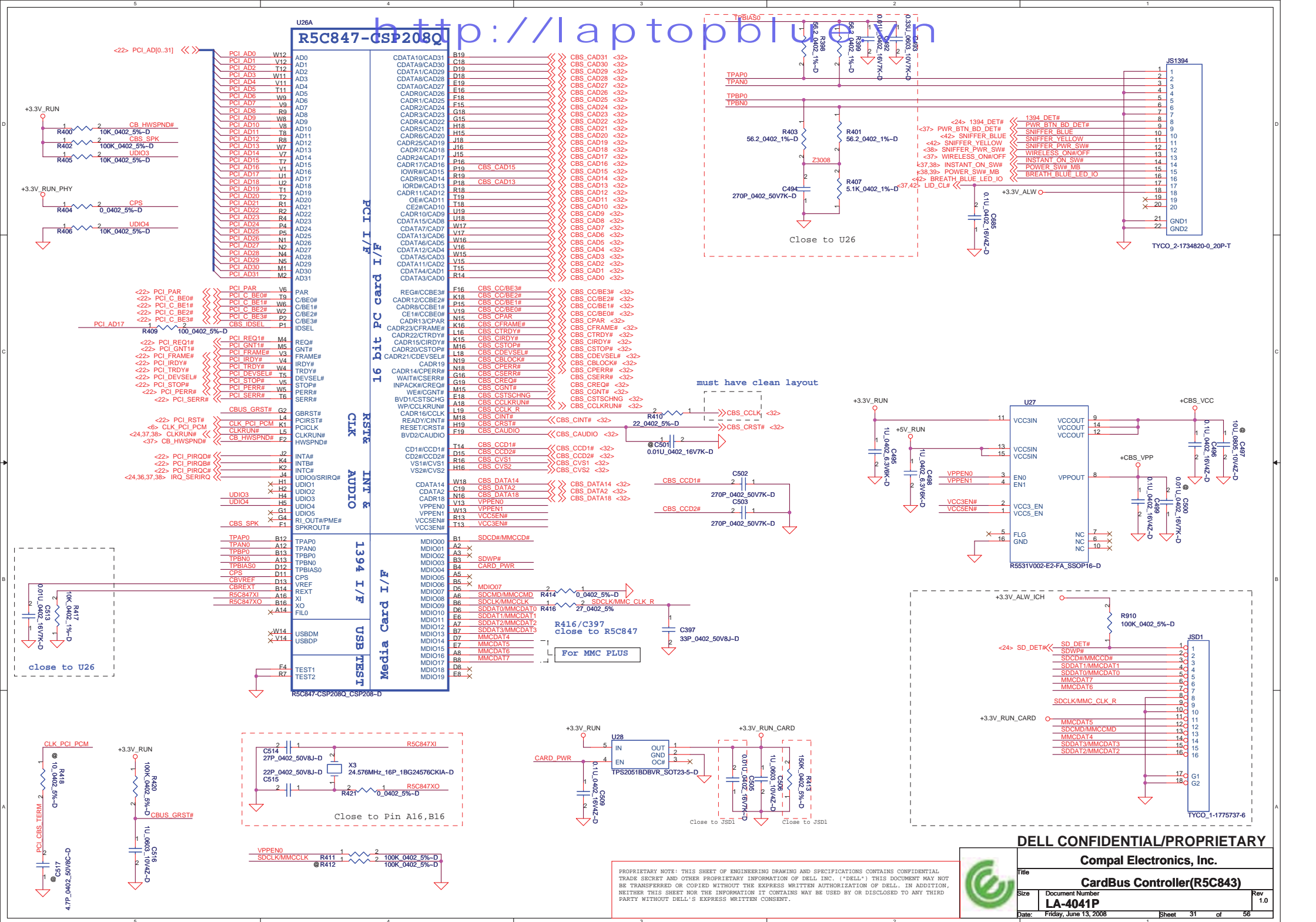


A horizontal number line is shown with tick marks at 0, 5, and 10. A vertical line is drawn at the 5 mark. The segment of the number line from 0 to 5 is labeled with the number 3. The segment of the number line from 5 to 10 is labeled with the number 2.



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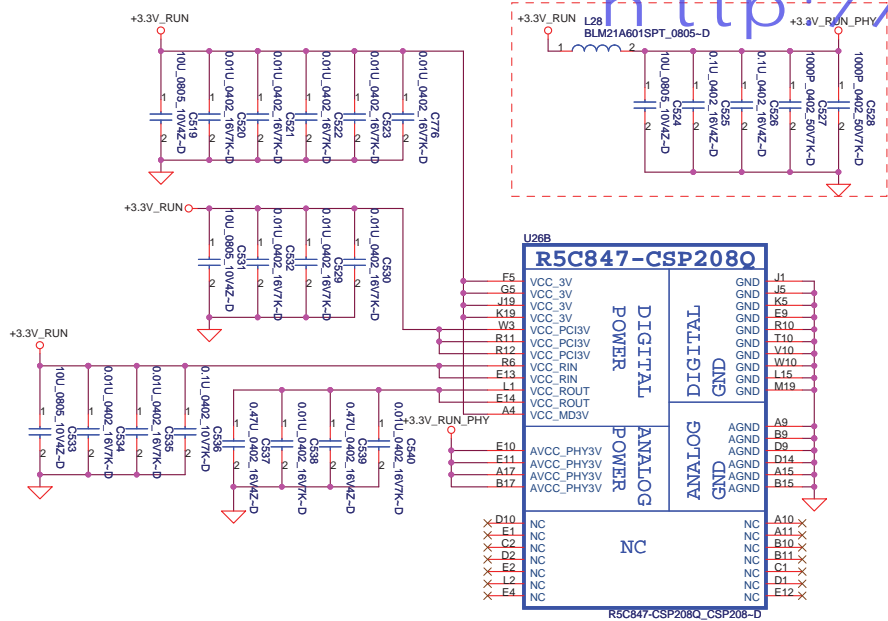
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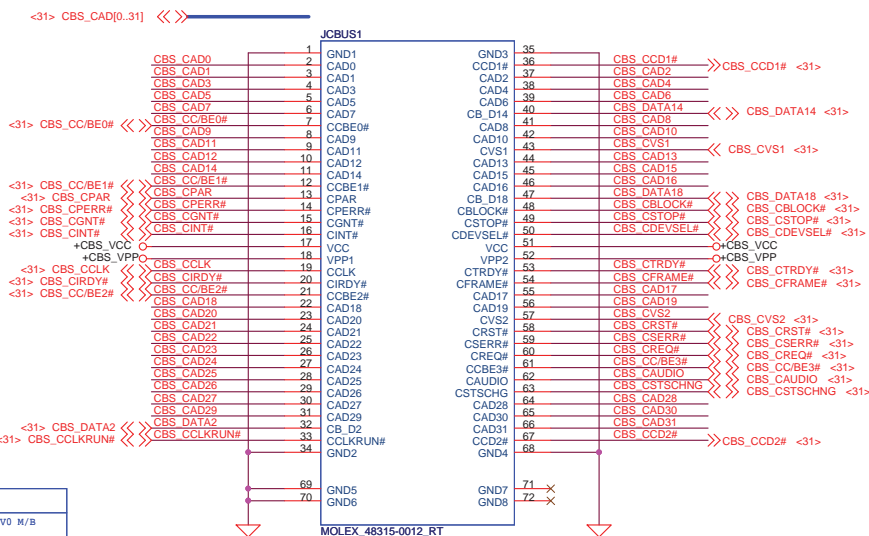
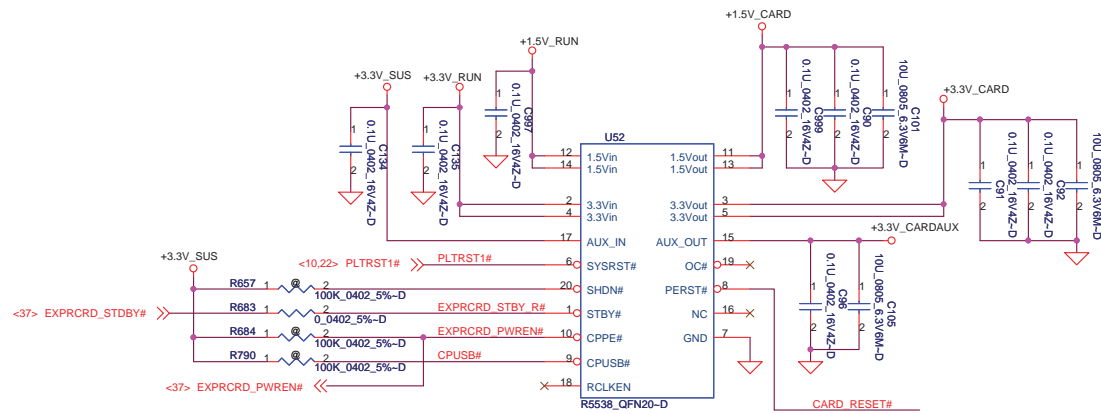
CardBus Controller(R5C843)

LA-4041P  
Date: Friday, June 13, 2008 Sheet 31 of 56

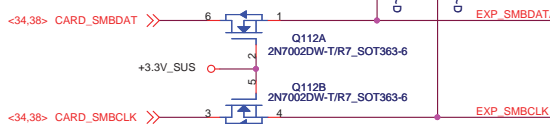
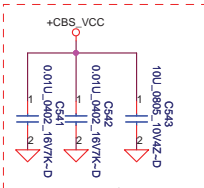
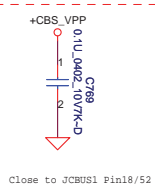


## Express Card

**+1.5V\_CARD: Max. 650mA, Average 500mA**  
**+3.3V\_CARD: Max. 1300mA, Average 1000mA**



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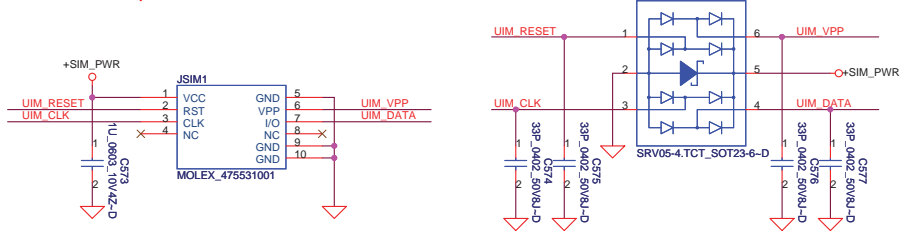
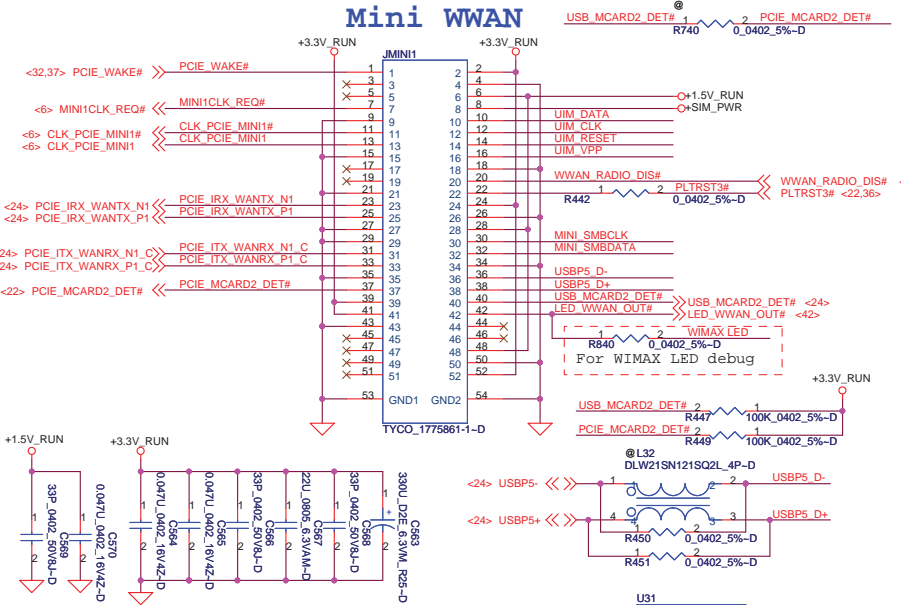
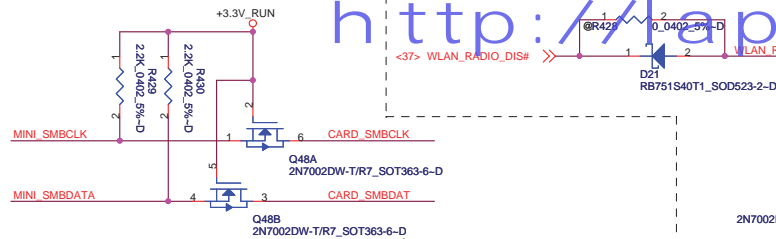
**CardBus/SD card Socket**

**LA-4041P**

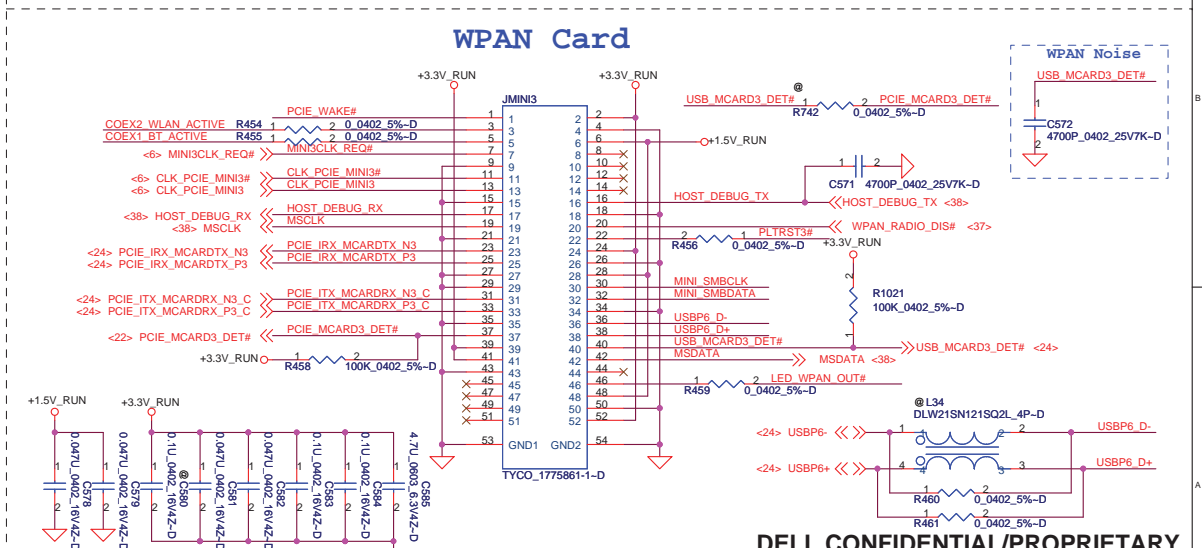
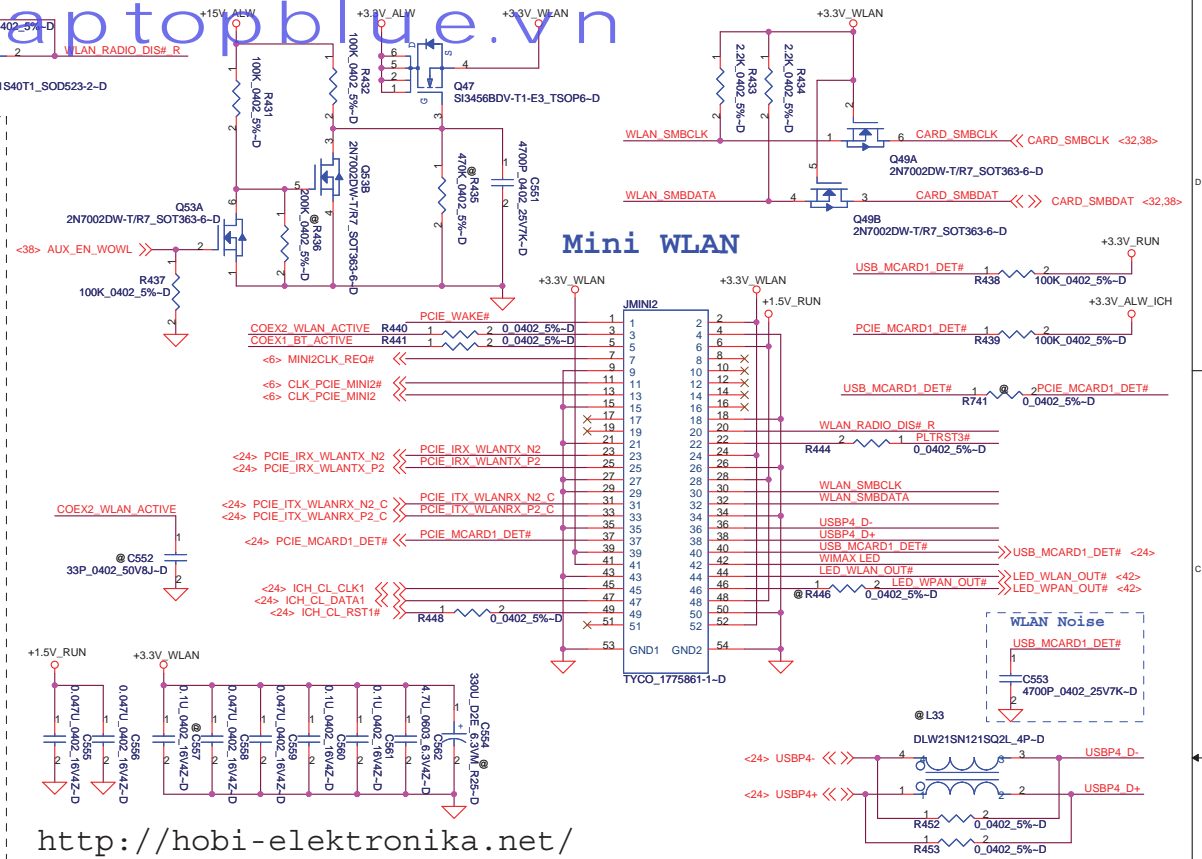
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PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+ -9%	1000	750	
+3.3Vaux	+ -9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+ -5%	500	375	NA



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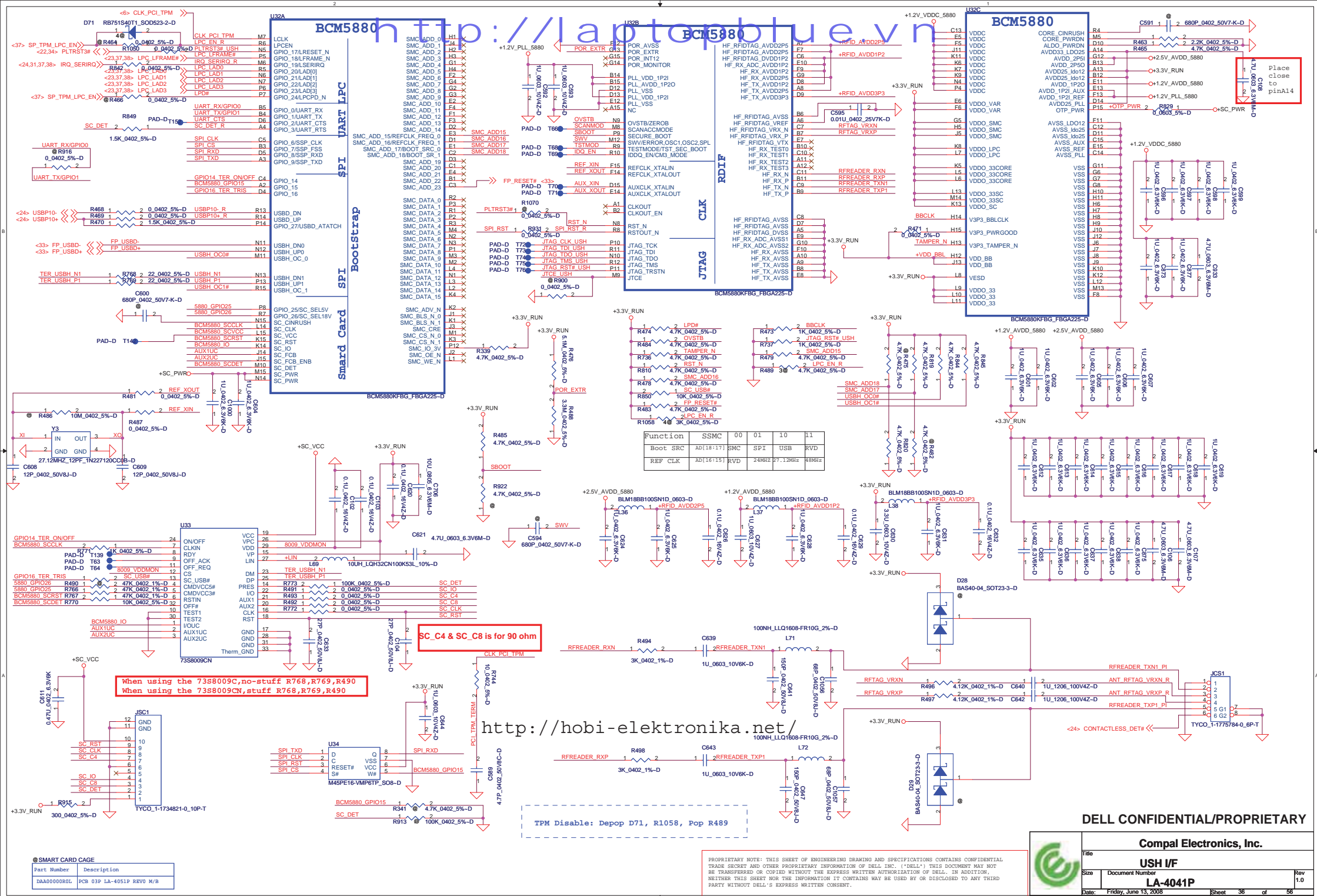
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### Mini Card

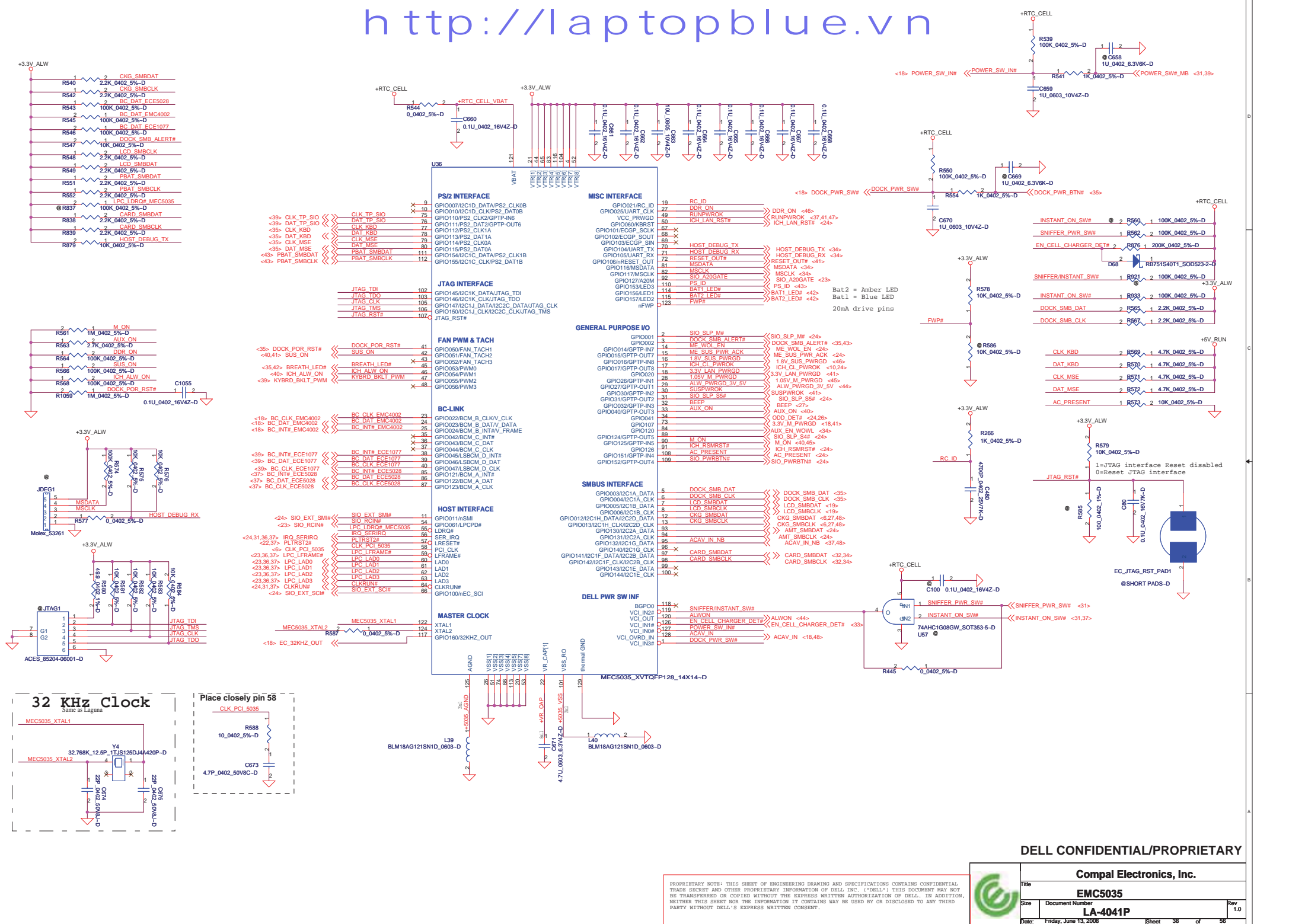
**LA-4041P**

Title			
Mini Card			
Size	Document Number	Rev	
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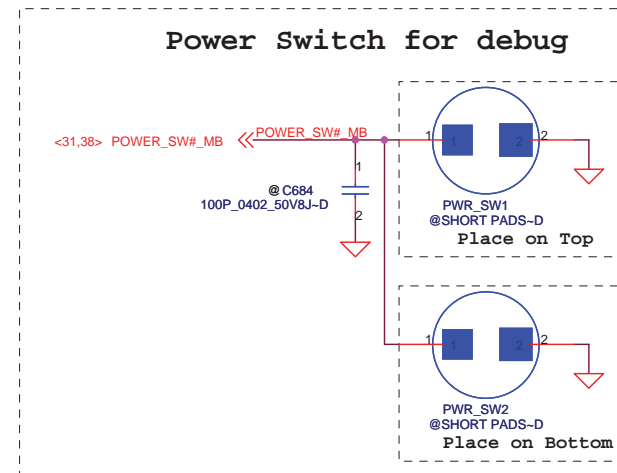
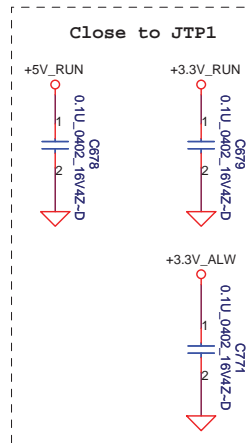
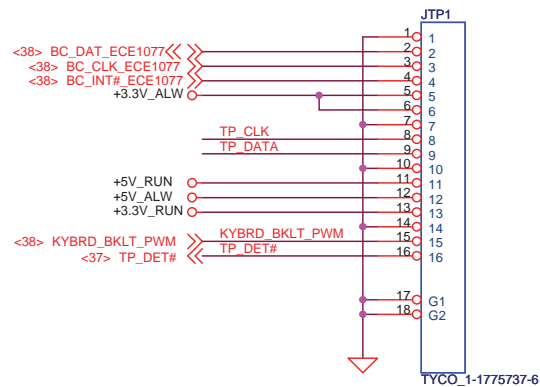
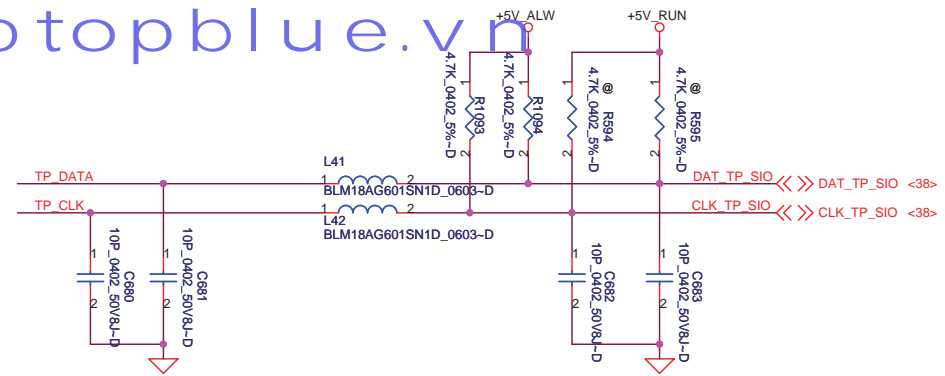
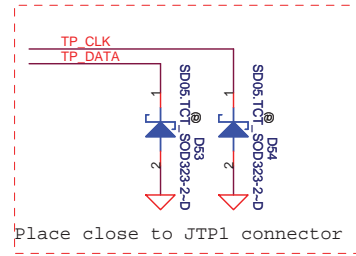
Compal Electronics, Inc.

EMC5035

LA-4041P

Rev 1.0

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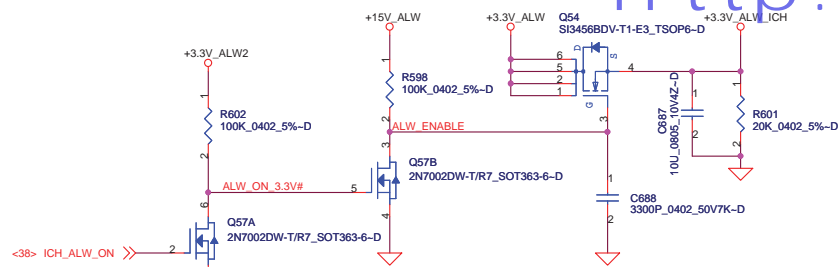
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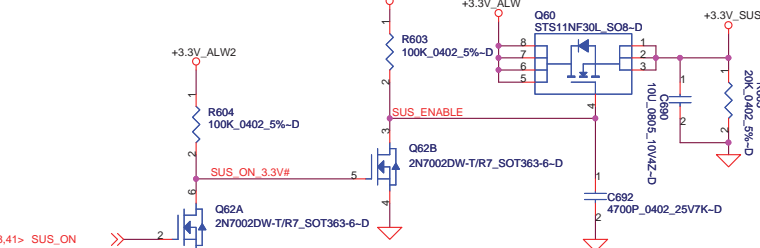
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Touch PAD/Int KB/LID		1.0
Size	Document Number	
	LA-4041P	
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# DC/DC Interface

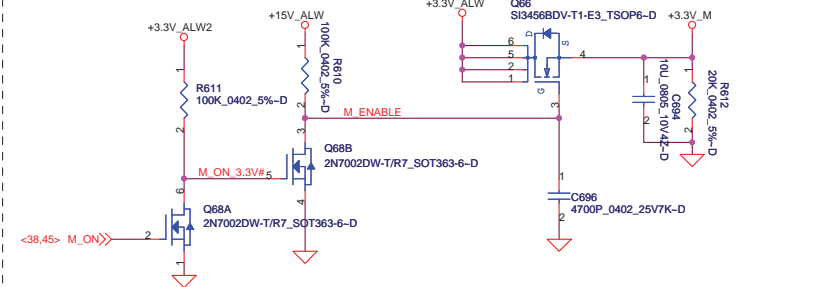
## +3.3V\_ALW\_CH Source



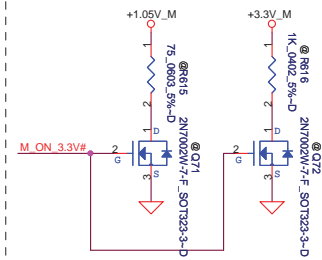
## +3.3V\_SUS Source



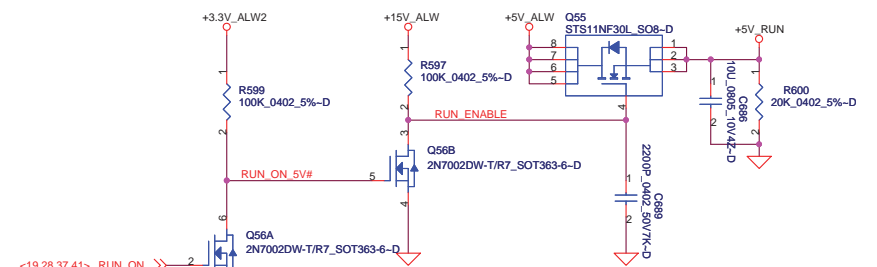
## +3.3VM Source



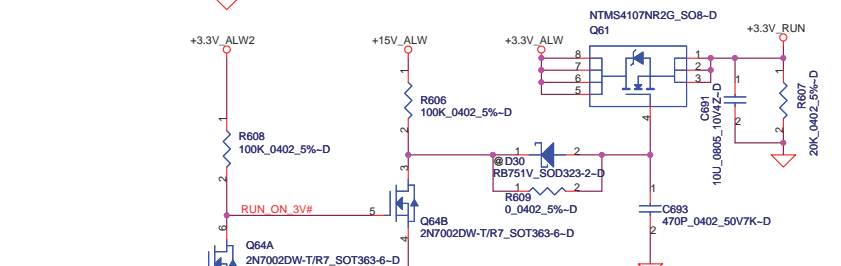
## Discharge Circuit



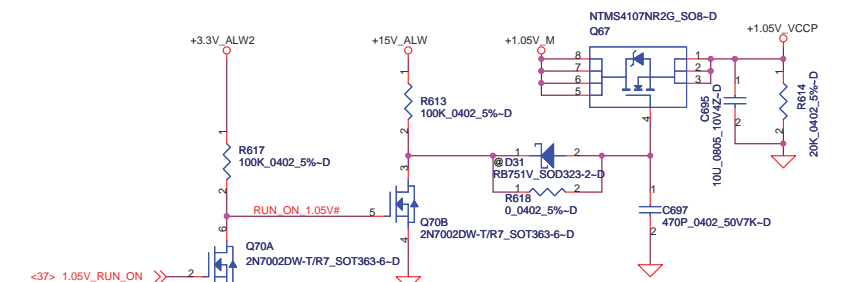
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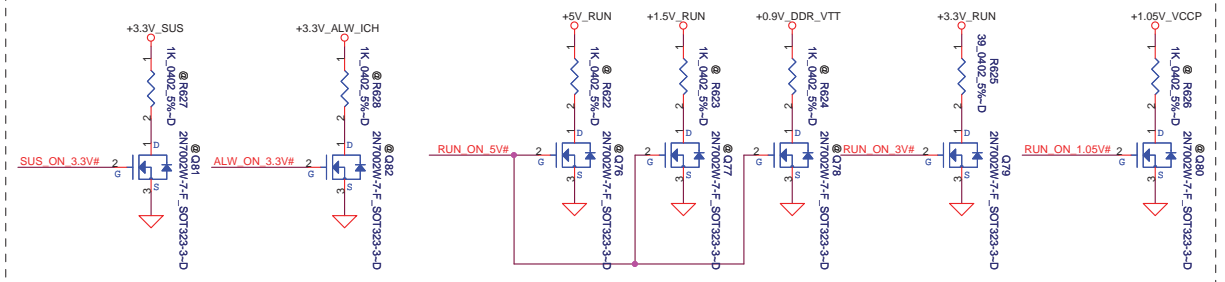
## +3.3V\_RUN Source



## +1.05V\_VCCP Source



## Discharge Circuit



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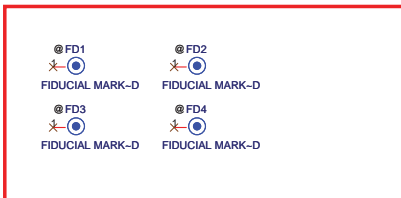
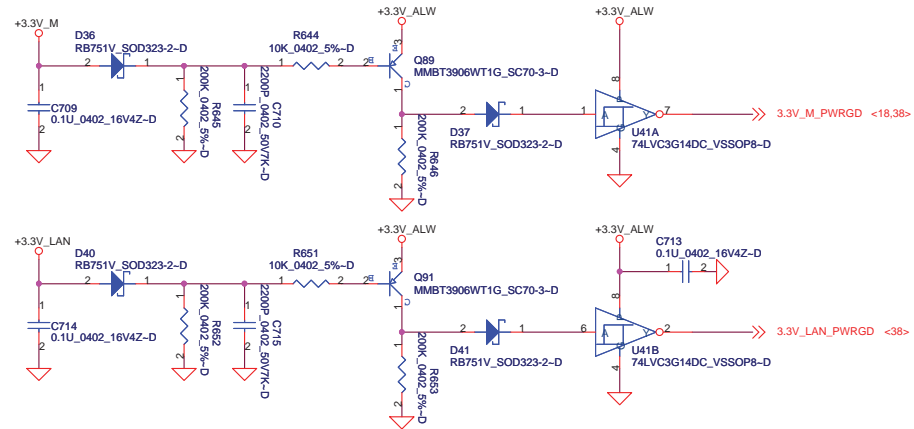
POWER CONTROL

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eDOCK x 2

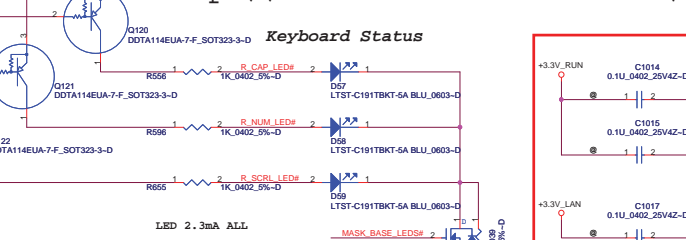
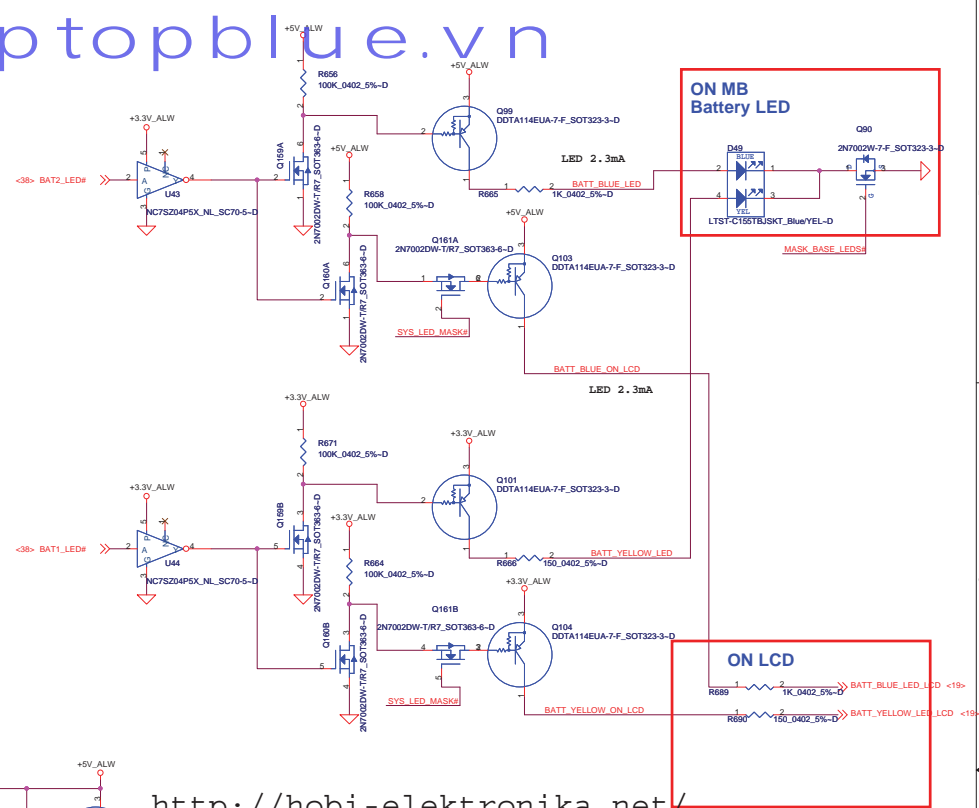
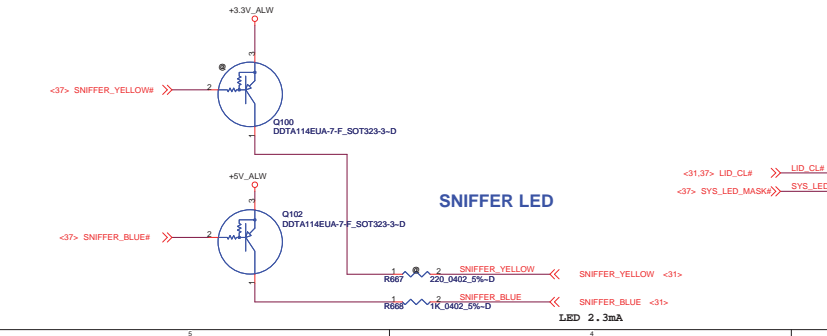
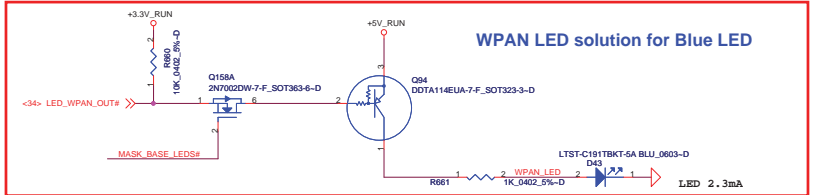
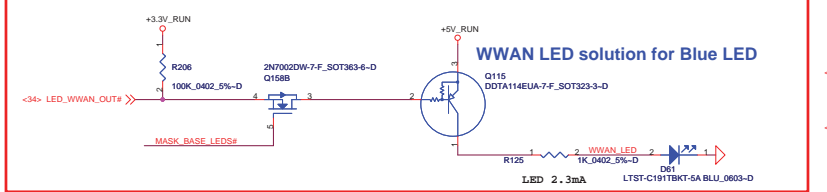
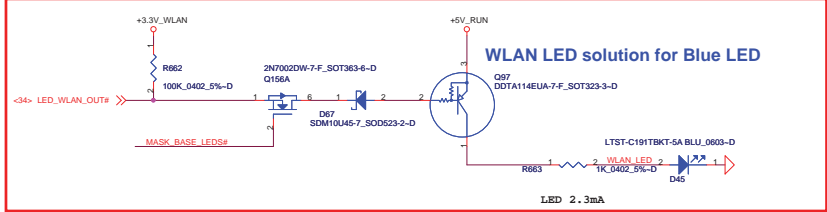
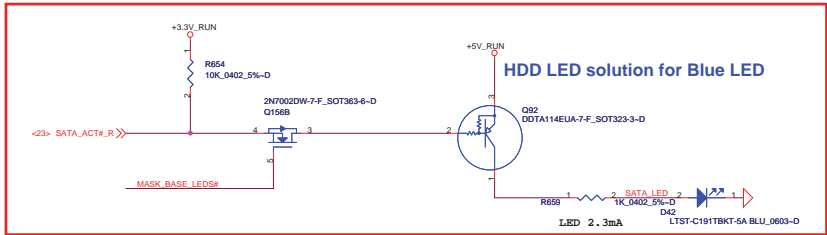
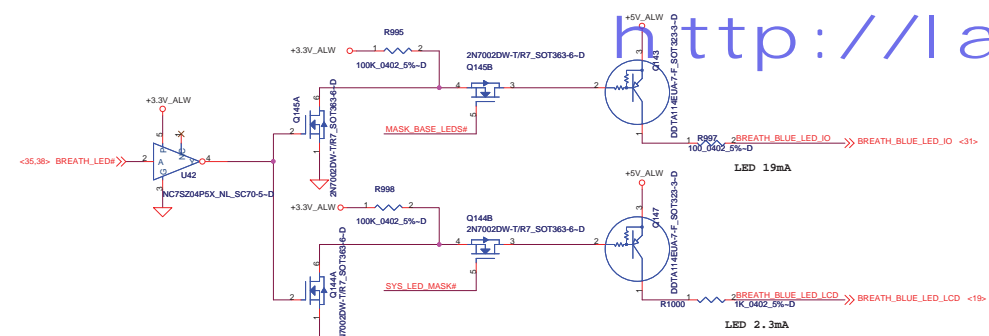
FD2  
FIDUCIAL MARK-D

FD4  
FIDUCIAL MARK-D

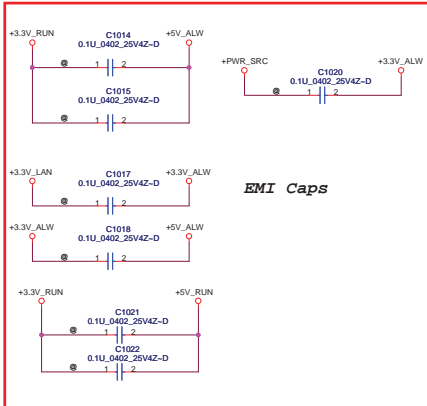
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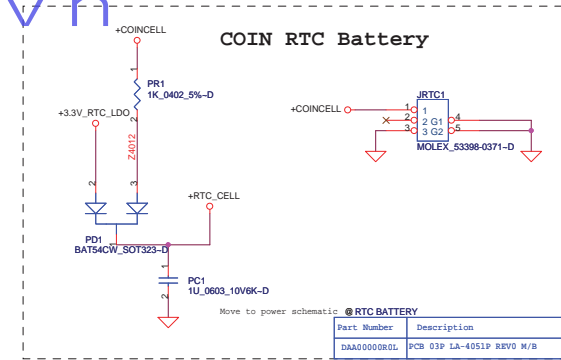
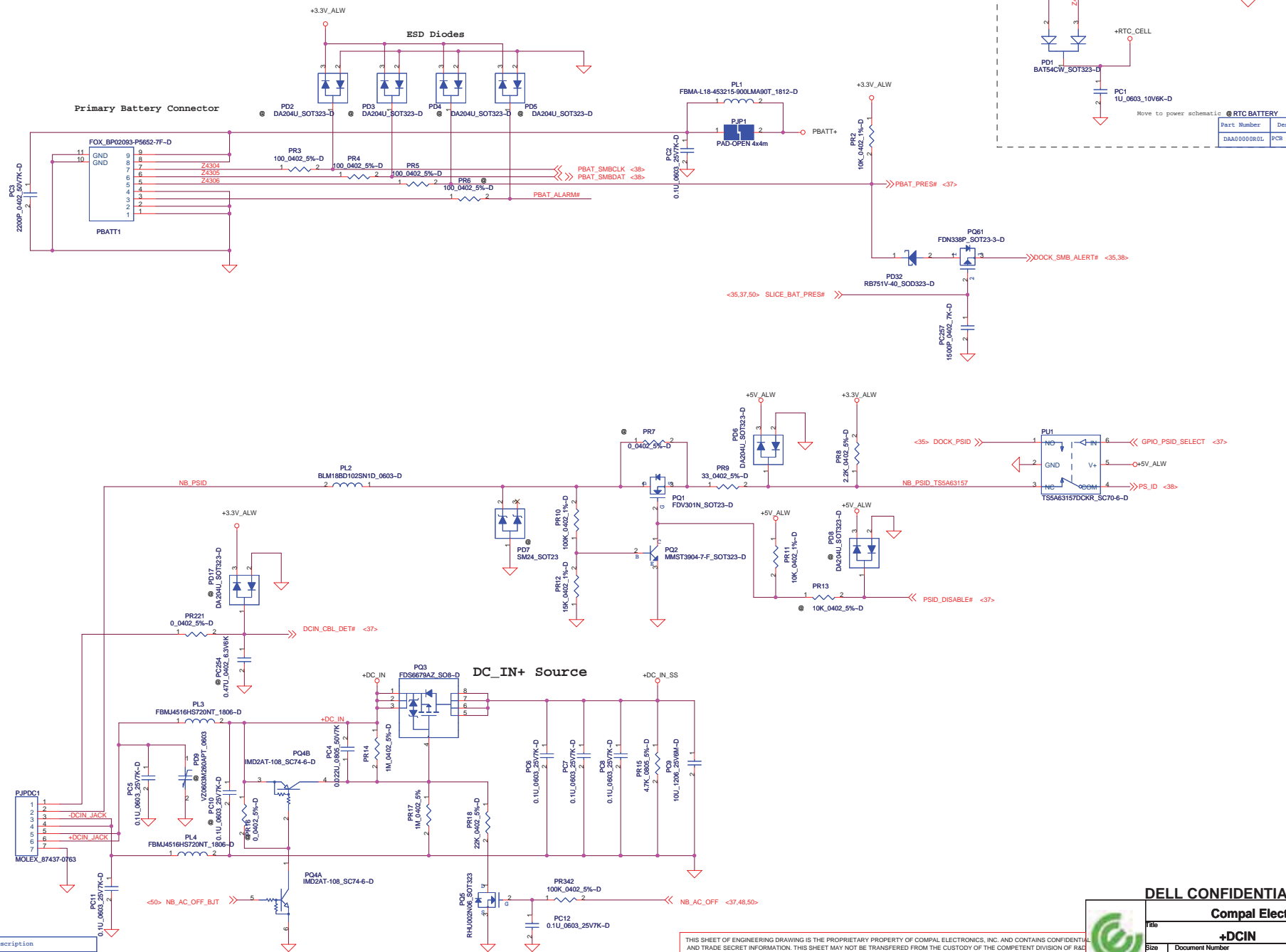
LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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		<b>LED</b>	
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Part Number	Description
DAA00000R0L	PCB 03P LA-4051P REV0 M/B

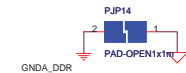
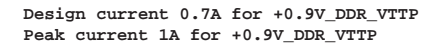




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**+1.8VSUSP/ +0.9V\_DDR\_VTT**  
DDR2 Termination



```
Component select
Input CAP 10uF_1206_25V
Output Cap 330U_D2E_2.5VM_R9*2 (Sanyo2R5TPE330M9)
H_MOSFET FDS6298
L_MOSFET FDS6299S
Inductor 1.4U_
```

**Compal Electronics, Inc.**

### 1.8VSUSP/0.9VDDR

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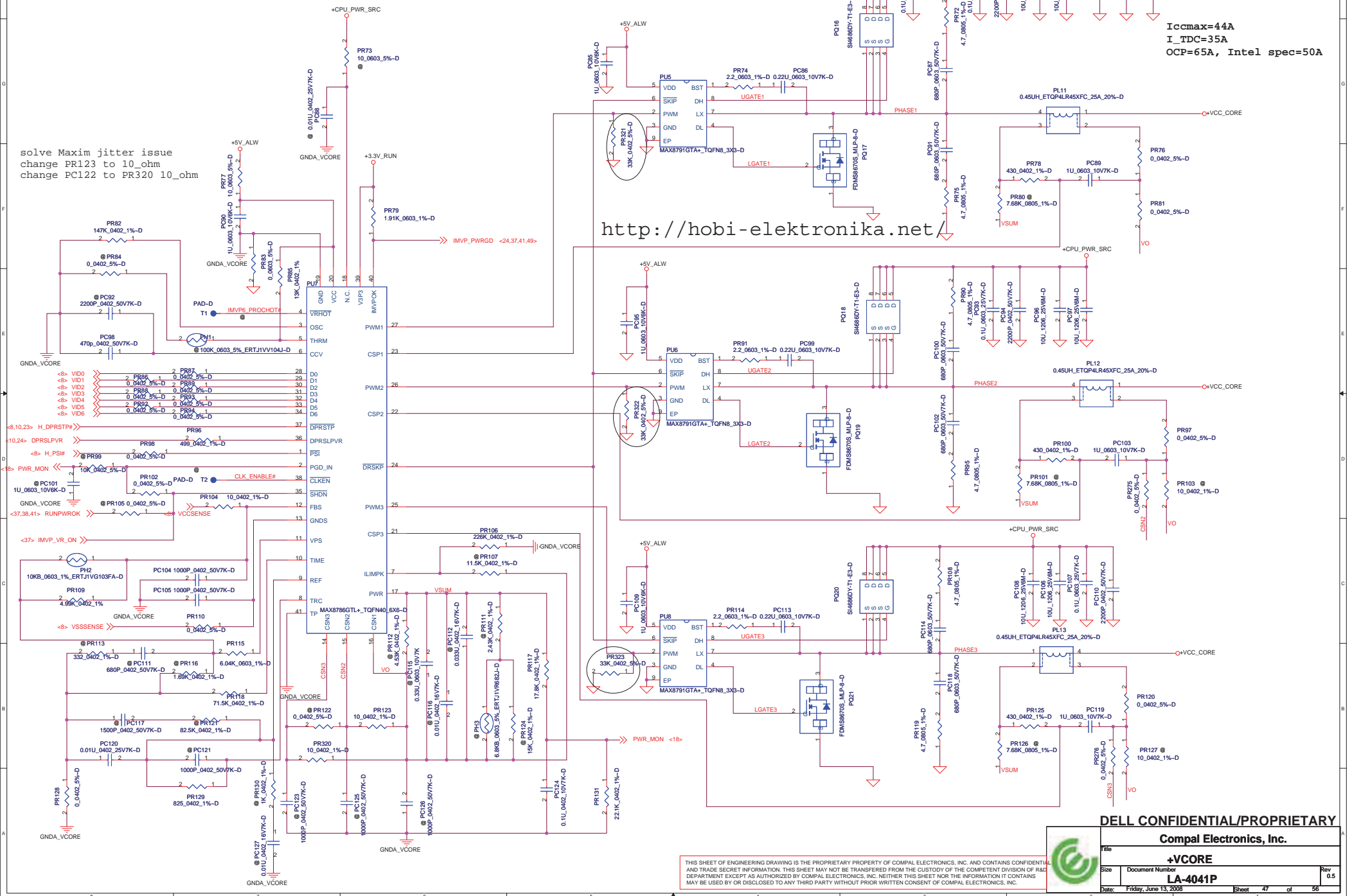
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```
solve Maxim jitter issue
change PR123 to 10_ohm
change PC122 to PR320 10_ohm
```

<http://hobi-elektronika.net>

Iccmax=44A  
I\_TDC=35A  
OCP=65A, Intel spec=50A

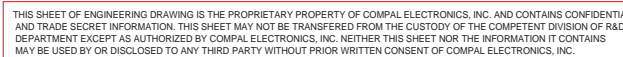


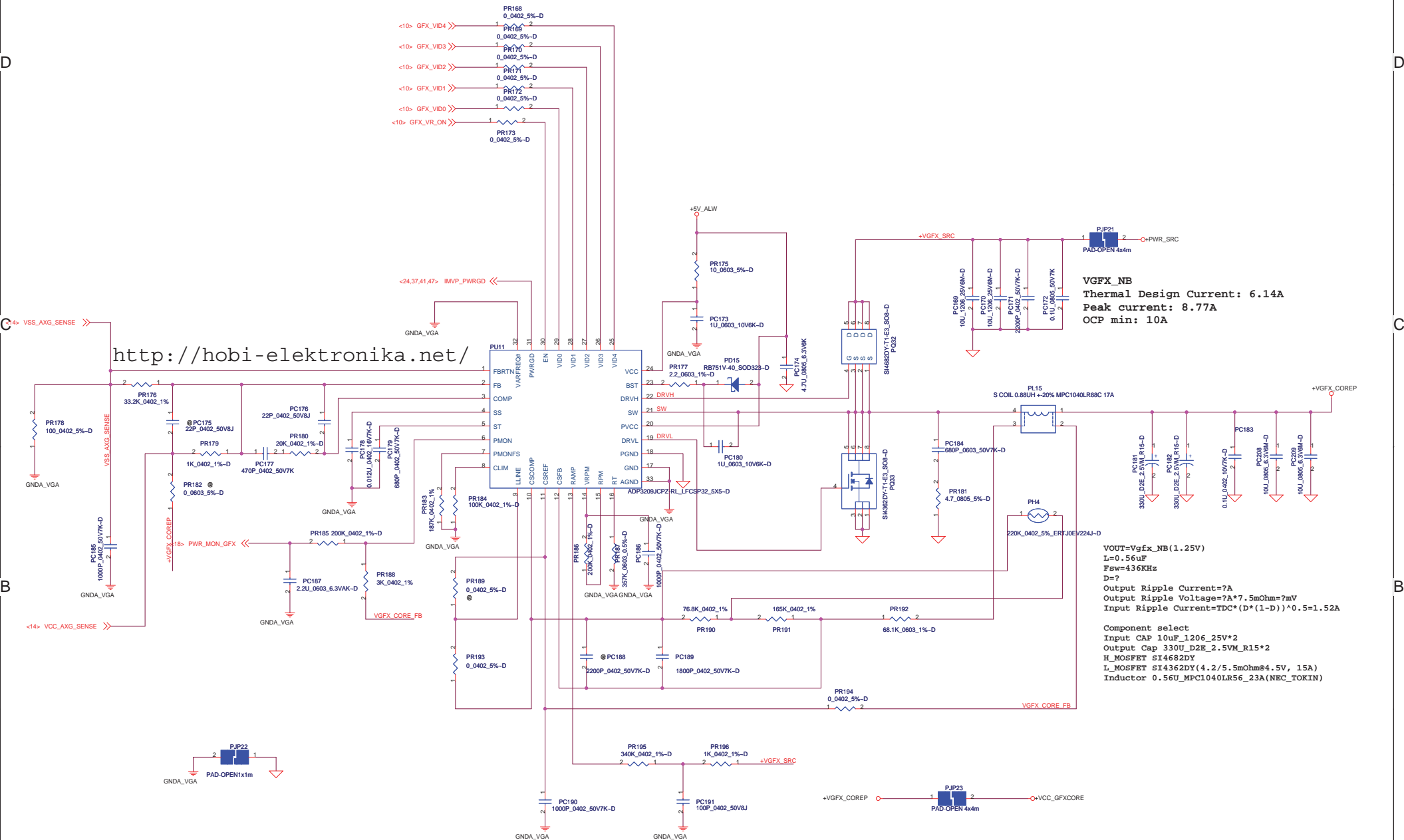
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**+VCORE**

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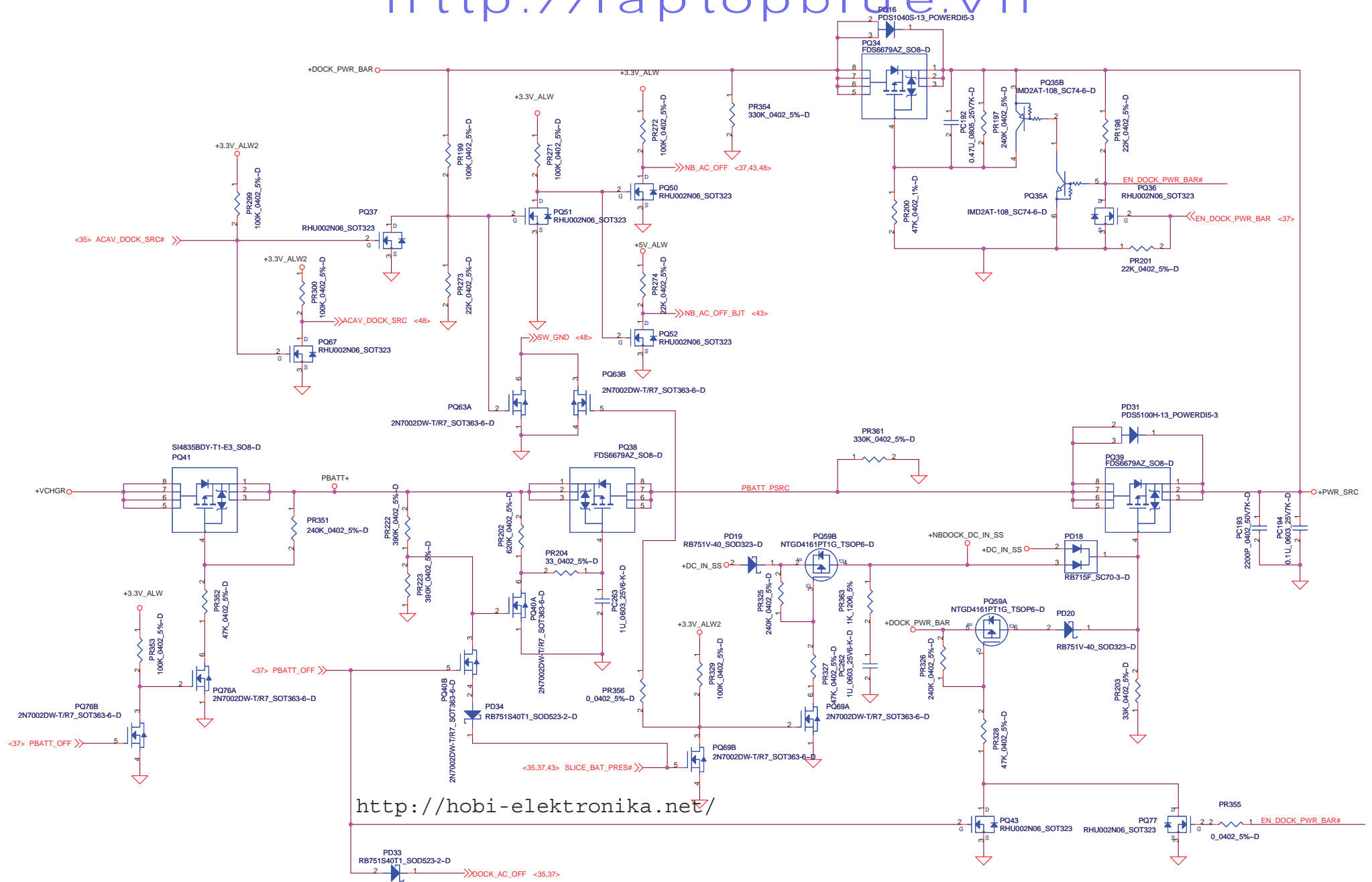


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ADP3209_NB_core			
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## Version Change List ( P. I. R. List)

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	ECE5028	2007/10/08	Compal	SCH165092 : change BID pop option to X01.	R534 (depop) ; R529 ( pop )	X01
2	24	ICH	2007/10/08	Compal	SCH165096 : modify the net "TPM_ID" connection.	change R273 from PD to GND to +3.3V_RUN. (PU = USH ; PD = china TPM)	X01
3	40	PWR CTRL	2007/10/08	Dell	SCH165105 : modify LAN_DISABLE# connection (MH:10/02 email)	Delete U61, add R934 and connect the net to U35(5028) pin 88. All Follow Roush circuit.	X01
4	36	USH	2007/10/08	Compal	SCH165106 : Change Y3 P/N & PCB footprint.	P/N from SJ10000550L to SJ100005X0L(KDS).	X01
5	36	USH	2007/10/11	Dell	SCH165108 : MA schematic Issue list , item 139.	change the connection ; NET" SMC_ADD15 " to GND. NET " SMC_ADD16 " to +3.3VRUN.	X01
6	33	USB	2007/10/11	Compal	SCH165110: (1) Per connector spec of the location JESAL. (2) Per 10/25 GPIO table, modify net name & connection. Also refer to Roush DF174483 issue.	(1)To swap the USB2 & USB3 connection to the JESAL (2)modify connection, U29 pin4 for ESATA_USB_PWR_EN#,U53 pin4 for USB_POWERSHARE_PWR_EN#. (3)Per Roush DF174483, chnage the PU PWR from 3.3VALW to 3.3VALW2 for below, USB_SIDE_EN# ; ESATA_USB_PWR_EN# ; USB_POWERSHARE_EN#.	X01
7	38	5035	2007/10/11	Dell	SCH165113 : Wrong PWR Rail (PU) for DOCK SMBUS.	Modify the PU PWR rail from 5VALW to 3VALW below, DOCK_SMB_DAT ; DOCK_SMB_CLK.	X01
8	19	LVDS Conn	2007/10/11	Dell	SCH165218 : to add webcam control PWR circuit.	Add Q125, Q126 to control Webcam PWR	X01
9	42	LED	2007/10/11	Compal	SCH165219 : Modify LED circuit concept.	Modify LED circuit concept	X01
10	35	eDOCK	2007/10/11	Dell	SCH165220 : ESD solution on DOCK Conn.	Add D65 & D66 , make them pop.	X01
11	12	Cantiga	2007/11/02	Dell	SCH165221 : Remove TV-out on LIO docking.	(1)disconnect TV out signals to U4,delete R674,R677,R678,R669,R762,R763. (2) make U4, pin15,pin19,pin20,pin31,pin22,pin23 all NC. (3) connect U2(MCH), pinF25,H25,K25,H24,A24,M25 to GND. (4) U2(MCH),PinL28 connect to 1.5V filter.	X01
12	21	DP Circuit	2007/11/02	Compal	SCH165222 : Follow Roush to have PD on DPC_CA_DET	Add R377 (100K,PD)	X01
13	22	ICH	2007/11/02	Dell	SCH165223 : Folooow DELL GPIO table, GPIO date code : 1025	Modify U10(ICH), pinF6, net name from MDC_RST_DIS# to GNT3#/GPIO55	X01
14	33	USB 2.0	2007/11/02	Compal	SCH165223 : MDC couldn't be detected issue	R326 needs to PU to +5V_RUN and per GPIO table 10/25, MDC_RST_DIS# should be connected to U35(5028) pin84.	X01
15	23	ICH	2007/11/02	Dell	SCH165224 : To delete RTC detection circuit.	Have discussed with MH, HW needs to provide more spacing for MB structure support. to delete below Locations are: R92,R96,Q123,R913,R914	X01
16	31	CardBus	2007/11/02	Compal	SCH165229 : SD card PWR S/W is not DELL AVL.(U28)	Change U28 to DELL AVL, TI part.	X01
17	34	Mini Card	2007/11/03	Compal	SCH165216 : (1)Follow Roush schematic for R449. (2)follow Roush to pop C553,C572 for EMI noise	(1)make R449 (pop) and change to 100K ohm. (2)make C553 (pop) & C572(pop) for EMI noise concern.	X01
18	34	USH5880	2007/11/03	Compal	SCH165214 : Per BRCM's comments for L69 concern.	Change L69 to 450mA (rated current), They suggest to use 400mA at least.	X01
19	34	USH5880	2007/11/03	Dell	SCH165213 : BIOS no need SC_DET function.	Delete R489,R830, and U35 Pin84 change to MDC_RST_DIS#.	X01
20	34	ECE5028	2007/11/15	Compal	SCH165211 : Follow Roush to add 10K PD on SYS_LED_MASK#	Add R669 (10K , PD to GND)	X01
21	30	LAN Transfomer	2007/11/15	Compal	SCH165209 : Duplicate location for function on MB & IO board.	To delete R395 ~ R397 on MB to get more room for layout.	X01
22	37	ECE5028	2007/11/19	Compal	SCH165206 : ALWON Oscillating issue	To Add D4 & R20 to the 5028 input on the INSTANT_ON_SW# signal	X01
23	37	Intel LAN	2007/11/19	Compal	SCH165207 : To Add Intel LOM LDO for 2.65/2.5V	To Add Q50,Q146,C482,R1020,R1017,R1018,R1019,C483,C484 To Add Q50,Q146,C482,R1020,R1017,R1018,R1019,C483,C484 To pop R42,R44,R685-R687,R243-R246.	X01
24	10	GMCH	2007/11/19	Dell	SCH165208 : To Add level shift circuit for MCH HDA.		X01
25	36	USH5880	2007/11/19	Compal	SCH165205 : To delete R495,R499	Follow Roush schematic, R495 & R499 can be replaced with short.	X01
26	28	Codec AMP.	2007/11/20	Dell	SCH165253 : Dell Roush WLP Results	(1) On MB: C436 & C437; change from 1U 1206 25V to 2.2U 1206 25V (2) On IO : C2 & C3 from 1uF 0603 to 2.2uF 0805	X01
27	39	TP/KB	2007/11/20	Compal	SCH165256 : To remove ECE1088 related circuit	To remove U38(ECE1088), C677,C676,R747,R650,R826 to have more layout room	X01
28	38	MEC5035	2007/11/20	Compal	SCH165257 : To remove SPI ROM related circuit on MEC5035	(1) to delete U37,R591,R589,C672,R590,R592,R593,R558. (2) make U37, Pin67 ~ Pin69,Pin48 for NC.	X01
29	36	USH5880	2007/11/20	Dell	SCH165263 : FP_RESET# signal from USH5880 to BIO connector	(1)Add the connection of FP_RESET# between USH5880(U32), pinC3 to JBI01 pin5. Also add R483(4.7K) PU on the net FP_RESET#. (2) chnage JBI01 connector to TYCO_1734242, same as Roush part. (3) delete the connection of BIO_DET# to the ICH pinA8,and delete R823.	X01

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## Title Changed-List History 1

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## Version Change List ( P. I. R. List )

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
30	18	EMC4002	2007/11/20	DELL	SCH165267 : To add the connection of PWR_MON_GFX	(1) add the net of PWR_MON_GFX, between U3 pin39 and PR185 pin2. (2) Add R938 (0 ohm, pop) and add R999 (270K , depop) (3) change R932 from 0 ohm to 4.7K	X01
31	38	MEC5035	2007/11/20	DELL	SCH165272 : change net name following PWR circuit naming.	(1) From ACAV_IN_DOCK# to ACAV_DOCK_SRC# (2) From ACAV_IN_MB/DOCK to ACAV_IN (3) also remove U59,C101 ; and add U69,C672.	X01
32	21	DP circuit	2007/11/20	Compal	SCH165273 : Per derating data from Roush team to change D10.	to change D10 from SDM10U45 to B0540WS for derating issue	X01
33	33	USB2.0	2007/11/20	Compal	LAY165112 : U54 need to be placed close to ICH.	change the common mode choke connection between SW and connector.	X01
34	30	LAN SW	2007/11/20	DELL	SCH165275 : To change MDI BUS L20 ~ L27 value	Per Roush WI: SCH164889, we have to change the value for L20 ~ L27 from 36nH to 22nH to improve the IEEE return loss margins.	X01
35	30	LAN SW	2007/11/21	Compal	SCH165306 : To remove MDI terminations and caps for LAN TX/RX	Follow Roush schematic to remove R384-R391;C488-C491	X01
36	18	EMC4002	2007/11/21	DELL	SCH165309 : EMC4002 POWER_SW# input - to add AND gate.	To add U68,R169,R170,C1050,R1014,R1015, follow Roush.	X01
37	35	Docking	2007/11/21	DELL	SCH165310 : docking pinout change to support battery slice.	To assign the Pin 41 of the docking connector for +NBDOCK_DC_IN_SS	X01
38	33	USB2.0	2007/11/21	Compal	SCH165312 : Follow Roush team to add a Cap on U54 Pin8.	Follow Roush team to add a Cap on +3.3V_SUS of U54 Pin8.	X01
39	37	ECE5028	2007/11/21	DELL	SCH165313 : To update 5028 GPIO	(1) chnage U35 Pin82, from DELL_ESATA_PWR_EN# to ESATA_USB_PWR_EN# (2) change U35 Pin104, from ESATA_USB_PWR_EN# to USB_POWERSHARE_PWR_EN# (3) delete R489,R830	X01
40	37 38	ECE5028 MEC5035	2007/11/21	DELL	SCH165315 : To update 5035 & 5028 GPIO	For 5035, (1) Pin30, from DEBUG_ENABLE# to SUSPWROK, no more net is called DEBUG_ENABLE# (2) Pin19, from SUSPWROK to RC_ID For 5028, (1) Pin 70, change to NC. (2) Pin 71, follow Roush to be LCD_TST only,remove R517.	X01
41	37	ECE5028	2007/11/21	DELL	SCH165316 : To change SNIFFER_DET# connection	Disconnect SNIFFER_DET# from ICH pin AE18 and connect it toEC5028 pin 33. Rename, SNIFFER_DET# to PWR_BTN_BD_DET#	X01
42	34	Mini Card	2007/11/21	DELL	SCH165320 : To pop R458 and R449.	Follow Roush to pop R458 and R449. R449 change to 100K.	X01
43	24	ICH	2007/11/22	DELL	SCH165338 : To modify the pop option for the net ICH_LAN_RST#	Follow Roush to depop R271, and pop R276	X01
44	7	CPU	2007/11/22	DELL	SCH165342 : To change BOM pop option and value of ITP circuit	(1) R785 change to depop (2) R65,R66,R62,R64,R67, from 51 ohm to 56 ohm. (3) R60 from 10K to 150 ohm	X01
45	7	CPU	2007/11/26	DELL	SCH165380 : voltage step up issue on H_RESET#	To depop the R923 to solve the voltage step up issue on H_RESET#	X01
46	24	ICH	2007/11/27	DELL	SCH165428 : To remove the second SPI ROM on ICH	to delete R295,R304,R305,C329,U13,R306,R308,R309,R307	X01
47	36	USH5880	2007/11/27	Compal	SCH165429 : To delete R846,R847	Per FAE's feedback, we can delete them for more layout room. Those resistors are the snap pin for chip version control. B0: pop R844,R845 ; so remove R846,R847	X01
48	36	Codec	2007/11/27	DELL	SCH165430 : To delete R329	Because we'll fix by PD R331 only. This is for I2C or SPI selection	X01
49	7	CPU	2007/11/28	Compal	SCH165508 : To add 0 ohm resistors for ESD concern.	ESD team require to have some 0 ohm series resistors on the ITP I/F. to add R780 ~ R784,R789.	X01
50	10	GMCH	2007/11/29	Compal	SCH165550 : To change R181 value for DP functional workable	Per Roush PT build result, need to change the R181 from 100K to 4.02K	X01
51	13	GMCH	2007/12/03	Compal	SCH165564 : this is Roush team EE WI	To remove D1 & R122	X01
52	31,32	CardBus	2007/12/06	Compal	SCH165942 : Ricoh review result	(1) CBS_CCD1#/CBS_CCD2# add C502/C503 270PF pull down. (2) U52,+1.5V_CARD add C101,+3.3V_CARDAUX add C105 10uF 0805. (3) R657,R684,R790 deopo,because chip internal have pull up. (4) PinA14, FIL0 add 0402 0.01uF C603	X01
53	10	GMCH	2007/12/07	Compal	SCH165943 : To modify the HDA circuit	change U67 to bi-direction part, and delete U66,C1048,C1049	X01
54	21	Display Port	2007/12/08	Compal	SCH165944 : To Follow Intel suggestion to update DP circuit	Add Q162,Q163 and modify the DP concept to meet Intel suggestion.	X01
55	37,38	5035,5028	2007/12/08	Compal	SCH165945 : To follow Roush team Instant SW circuit	Add R1036,R445,R933,depop R20,depop C100,depop U57, Depop R560	X01

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Item		Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
56	24		ICH	2007/12/08	DELL	SCH165946 : To Follow Schematic, it's feedback from Intel	To add R210 10K(Ⓢ) PU to +3.3V_ALW_ICH on the net"LAN_DISABLE#" (depop)	X01
57	10		GMCH	2007/12/10	Compal	SCH165947 : Intel asks to change R180,R182,R183 value.	R180,R182,R183 from 100K to 4.02K.	X01
58	37		ECES028	2007/12/17	Compal	SCH166250 : To change the BID from X01 to X02	pop R530, depop R535 ; pop R534, depop R529	X02
59	35		Docking	2007/12/17	DELL	SCH166251 : to add PU option for DOCK_DET#	Add R1038, and depop R124	X02
60	12		Cantiga	2007/12/17	DELL	SCH166253 : to change the R672 value	follow Roush team to change the value from 1.02K to 976 ohm.	X02
61	12		Cantiga	2007/12/17	DELL	SCH166255 : To change R688 value	R688 from 2.37K to 2.4K	X02
62	42		LED	2007/12/17	Compal	SCH166258 : to add D67 for backdrive issue	to add D67 to solve backdrive issue in S3 , +3.3VWLAN to +5VRUN via body diode.	X02
63	18		EMC4002	2007/12/17	DELL	SCH166260 : to follow Rosuh to disable the 2.5V from EMC4002	to add R211, depop R149, depop C238,C239	X02
64	21		DP	2007/12/17	DELL	SCH166262 : to follow Roush schematic to pop R875	follow Roush UMA DP circuit to pop R875	X02
65	27		Codec	2007/12/17	DELL	SCH166266 : to follow Roush team to change C408 ~ C411 value	C408 ~ C411 from 1uF to 2.2uF 0805 10V	X02
66	18,21 37,38,42		EMC4002,DP 5028,5035,LED	2007/12/17	DELL	SCH166268 : About 74AHCT1G08GW AND Gate issue	Change U68, U60, U69, U57, and U65 from 74AHCT1G08GW to 74AHC1G08GW	X02
67	38		MEC5035	2007/12/17	DELL	SCH166269 : update the connection of ACAV_DOCK_SRC#	The signal ACAV_DOCK_SRC# can be removed from the 5035	X02
68	42		LED	2007/12/17	DELL	SCH166271 : to follow Roush to add Q150 and R1039(depoy)	to follow Roush to add Q150 and R1039(depoy)	X02
69	33,38		USB,MEC5035	2007/12/17	DELL	SCH166273 : to modify for the connection "CELL_CHARGER_DET#"	add D68,D69,R1040,Delete R926,change C1013 from 0.1u to 1u. follow Roush team.	X02
70	6,8,24		CLK,CPU,ICH	2007/12/17	DELL	SCH166276 : Intel NOA test point compliance	Add R1041-R1045.	X02
71	33		USB2.0	2007/12/17	DELL	SCH166277 : to add esata repeter U72 related circuit	to add U72,C490,C489,R306,R307,R305,C1052,C488 and U72 change to PI2EQX3201BZFE	X02
72	35		Dock	2007/12/21	Compal	SCH166435 : Hot Docking then Docking side Apdater Protect	add D70 and R1057 on docking connector, and add C1055, R1059. MEC5035 pin41 change to "DOCK_POR_RST#" to dock pin140	X02
73	35		Dock	2007/12/28	Compal	SCH166508 : DP function finalize to change DP/DVI circuit	add R1060-R1063 for DDC, R1064/R1065 for CD_DET, R1066-R1069 for pull up an dlow	X02
74	36		USH	2007/12/28	Dell	SCH166328: Add a series resistor on PLTRST3# for the USH RESET_N	Add R1070 for PLTRT3# to USH_RST_N	X02
75	37		IO 5028	2007/12/28	Compal	SCH166510 : DOCK_AC_OFF signals problem	Cause the Battery Slice make the DOCK_AC_OFF always Low, add D72/R1071, PR356 and PD33. But depoy it	X02
76	42		LED	2008/1/2	Compal	SCH166540: DF186056 : ROUSH issues, Maybach have same design and similar ME design. Follow Roush suggest for LED Resistors value	Change the LED resistors value: (1) R997 --> 68ohm (power on LED on IO board) (2) others Blue color LED change to 1K : R125, R556, R596, R655, R659, R663, R665, R661, R668, R689, R1000	X02
77	37		IO 5028	2008/02/13	Compal	SCH168204 : change BID to X03	pop R529, depoy R534	X03
78	37		IO 5028	2008/02/13	Dell	SCH168206 : follow Roush X05 schematic	pop D72, depoy R1072, pop R1071 (33K ohm)	X03
79	36		USH5880	2008/02/13	Dell	SCH168207 : USB EA issue	change R468/R469 from 22ohm to 0ohm	X03
80	33		USB2.0	2008/02/13	Dell	SCH168208 : Follow Roush to add bypass resistors on U54.	add R1082,R1083 (make them depoy)	X03
81	18		EMC4002	2008/02/13	Dell	SCH168209 : change R152 from 0ohm to0.82ohm for LDO input	change R152 from 0ohm to 0.82ohm	X03
82	6		CLOCK	2008/02/13	Dell	SCH168210 : Follow Roush to change L1 (derating problem)	change L1 to DC PWR Part BK2125HS601	X03
83	36		USH5880	2008/02/13	Dell	Schematic : Follow Roush to pop R849 to support USH Low PWR	pop R849	X03
84	35		edock	2008/02/13	Dell	SCH168211 : follow Roush to depoy R1057	depop R1057	X03
85	33		USB2.0	2008/02/13	Dell	SCH168213 : for esata EA to pop R1046	pop R1046	X03
86	10		MCH	2008/02/13	Dell	SCH168215 : follow Roush to add R1088(depoy) for Intel debug	depop R1088	X03
87	24,36		ICH,USH5880	2008/02/13	Dell	SCH168216 : To have disable / enable TPM pop option	3Ⓢ = disable TPM , 4Ⓢ = enable TPM R273(4Ⓢ),D71(4Ⓢ),R1058(4Ⓢ) R304(3Ⓢ),R489(3Ⓢ) change R997 to 82ohm	X03
88	42		LED	2008/02/13	Dell	SCH168217 : to change R997 value, LED current over spec	change R997 to 82ohm	X03
89	33		USB2.0	2008/02/13	Dell	SCH168218 : Follow Roush to update ESATA circuit	Add R1075,R1074,R1079,R1080,R1077,R1078	X03
90	13		MCH	2008/02/13	Dell	SCH168219 : debug +3.3V_RUN backdrive issue in S3	Add R1076	X03
91	27		Codec	2008/02/13	Dell	SCH168220 : Per vendor feedback, change L18 to BLM18EG601SN1D	L18 change to BLM18EG601SN1D	X03
92	27		Codec	2008/02/13	Dell	SCH168221 : Per vendor feedback, update codec circuit	Add L35,delete C392,R328(Depoy),R327 & R828 change to 499K ohm	X03
93	38		MEC5035	2008/02/13	Dell	SCH168223 : Dock SMBUS timing failed	Change R565, R567 to 2.2K ohm	X03
94	10		MCH	2008/02/15	Dell	SCH168224 : Follow Roush to change R180-R183 value	change to 2.2K	X03
95	7		CPU	2008/02/15	Dell	SCH168225 : Follow Roush to update ITP circuit resister value	R65 from 56ohm to 150ohm;R66 from 56ohm to 649ohm;R64 from 56ohm to 39ohm R67 from 56ohm to 27ohm;R57 from 1Kohm to 124ohm	X03
96	27		Codec	2008/02/20	Dell	SCH168336 : Follow Roush to change C406 to 10uF to change C436/C437 from 2.2uF to 10uF for Audio performance	C406 change to 10uF, C436/C437 change to 10uF	X03
97	21		DP	2008/02/20	Dell	SCH168338 : to change R377 value to follow DP spec.	R377 change to 1M ohm.	X03

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98	21	DP	2008/02/20	DELL	SCH168340:To modify DP circuit as Roush schematic	pop R875,R278 ; depop R1066,R674,R650,R1069	X03
99	9	CPU	2008/02/20	DELL	SCH168341:To update CPU Bypass caps value & pop option	(1) change C56 ~ C61 from 220uF to 270uF (2) depop C59.	X03
100	27	Codec	2008/02/20	Compal	SCH168349 : modify codec circuit to have analog GND	To add analog GND to solve noise problems.	X03
101	27	Codec	2008/02/21	Compal	SCH168528 :To modify Audio circuit after discussing with ADI	To improve Audio noise problem. 1. change C401 to 0.1uF 2. change C408/C409 to 0.22uF 3. change C410/C411 to 0.068uF 4. add C77/C78/C79/C81/R308/R309 5. delete C397	X03
102	36	USH5880	2008/02/21	Compal	SCH168529 : to modify RFID circuit for EMI issue.	Add L71,L72,C1056,C1057	X03
103	18	EMC4002	2008/02/25	Compal	SCH168530 : chnge R153 value to meet the formula of Ra.	R153 change to 3.16K	X03
104	33	USB2.0	2008/02/29	Compal	SCH168775 : To pop U51 per ESD testing result	pop U51	X03
105	23,29,36	ICH,USH,LAN	2008/02/29	Compal	SCH168776 : X'tal EA result to change some Caps value	C296/C297 from 15pF to 10pF ; C475/C476 from 27pF to 12pF;C609/C608 from 22pF to 12pF	X03
106	27	Codec	2008/3/3	Compal/IDT	SCH168837 : Follow Roush to add R1091/R1092 for Audio noise	add R1091/R1092 (100 ohm)	X03
107	39	TP/INT KB/LID	2008/3/3	DELL	SCH168840 : M09 S3 backdrive issue	Touch pad vendor use 5VALW for SMBUS,to add R1093,Ro1094, and depop R594/R595	X03
108	23	ICH	2008/3/3	Compal	SCH168842 : 24MHz noise issue (EMI feedback)	pop C300,C302,C309	X03
109	31	CardBus	2008/3/4	Compal	SCH168876 : Modify SD card circuit per EMI's feedback	R416 change to 33ohm and add C397(33pF)	X03
110	40	PWR CTRL	2008/3/5	Compal	SI4336DY will phse out, impact location Q61,Q67	Q61,Q67 from SI4336DY to NTMS4107NR2G	X03
111	20	CRT	2008/3/5	Compal	SCH168968 : modify RGB circuit to pass EMI/HW timing	L61/L62/L63 from BLM18BB750SN1D to ; depop C267/C268 BLM18BB470SN1D; depop C390/C518/C996	X03
112	36	USH5880	2008/3/6	DELL	SCH169090 : Per Roush EE WI SCH167486	L8/L9/L10 change to R830/R831/R832 all for 0 ohm R849 change to 1.5K , R915 change to 300 ohm	X03
113	31	CardBus	2008/3/6	Compal	SCH169116 : X'tal EA result (location: X3)	change C515 to 22pF, C514 to 27pF	X03
114	21	DP circuit	2008/3/11	DELL	SCH169224 : modify DP circuit	(1)To implement the DP S/W as SN74CBTD3306 for MB & Docking side (2)F1, change to 1206L150PR, make it pop, add C485 (10 uF), R184(depoc)	X03
115	12	MCH	2008/3/11	DELL	SCH169225 : follow Roush to add 75 ohm on TV signals	Add R1114 ~ R1116	X03
116	33	USB2.0	2008/3/11	DELL	SCH169226 : to bypass USB S/W	depop U54,C1045 ; pop R1082,R1083	X03
117	27	Codec	2008/3/11	ADI	SCH169231 : to modify Audio circuit	(1) C77,C78,C79,C81 change to 1000pF (2) L35 change to LBR2012T101K (3) add C481(0.1uF) (4) C410/C411 change to 0.22uF (5) C408,C409 change to 1uF (6) R1091,R1092,R340,R342 change to 200 ohm (7) R308,R309 change to 10 M ohm and use AGND	X03
118	6,37,38,36	Clock,50285035, dock	2008/3/12	Compal	SCH169269 : to improve system noise	R19 to 39ohm,R285(pop),C318(pop),R26 to 39ohm,R527(pop),C656(pop) R32 to 39ohm,R588(pop),C673(pop),R29 to 39ohm, R744(pop),C589(pop)	X03
119	24	ICH	2008/3/12	DELL	SCH169282 : add 2nd SPI ROM	add R385,R375,U13,C392,R383,R329.R384,R386,R387	X03
120	24	ICH	2008/3/13	DELL	to delete the change for item 119	to delete R385,R375,U13,C392,R383,R329.R384,R386,R387	X03
121	24	ICH	2008/3/12	DELL	SCH169282 : add 2nd SPI ROM	add R385,R375,U13,C392,R383,R329.R384,R386,R387	X03
122	24	ICH	2008/3/17	DELL	SCH169460 : add connection for SPI ROM selection	add R1049,R1060, add SPI selection connection of SPI_WP#_SEL	X03
123	6	Clock	2008/3/18	DELL	SCH169486 : 33MHz clock shared issue	CLK_PCI_PCM connection change to U1 pin 33. Pin 32 is for dock 33MHZ ONLY.	X03
124	21,35	DF,eDOCK	2008/4/28	Compal	SCH170959 : C985/C984 from 0.1uF to 0.033uF for ESD concern	C985/C984 from 0.1uF to 0.033uF.	X04
125	24	ICH	2008/4/28	DELL	SCH170960 : to depop 2nd SPI ROM	to depop R385,R1060,R375,U13,C392,R383,R329,R384,R386	X04
126	27	Codec	2008/4/28	Compal	SCH170961 : EMI concern for DMIC_CLK	change R338 to L75, and pop C486	X04
127	27	Codec	2008/4/28	DELL	SCH170962 : bypass double inverter of DAI_DI	depop U18,U19,C418,C419 and add R762	X04
128	35	eDOCK	2008/4/28	Compal	SCH170963 : Follow Roush to add R1095,R1096	add R1095,R1096. (0 ohm)	X04
129	37	ECE5028	2008/4/28	Compal	SCH170964 : change BID	depop R539 add R534, depop R530 add R535, add R531 depop R536	X04
130	40	PWR CTRL	2008/4/28	Compal	SCH170965 : add discharge circuit of 3.3VRUN	add R625(39 ohm) and Q79	X04
131	42	LED	2008/5/7	Compal	SCH171234 : SNIFFER LED only support BLUE color	depop Q100,R667	X04
132	18	EMC4002	2008/5/7	Compal	SCH171233 : FAN speed couldn't be detected issue	add D38	X04
133	23	ICH	2008/5/8	Compal	SCH171331 : WLAN detection issue	Follow Roush to add R84,R96 10K PD. (R84 & R96 all depop)	X04
134	40	PWR CTRL	2008/5/26	Compal	SCH172014 : Follow Roush to change C688 value.	C688 from 4700pF to 3300pF.	X04A
135	10	MCH	2008/5/26	Compal	SCH171331 : PCiE detection for WLAN issue	Add Q153-Q155, R1118-R1123 , C1049	X04A
136	24,38	ICH,MEC5035	2008/6/2	DELL	SCH172196 : re-route ODD_DET#	add a connection to MEC5035 pin 34 also.	A00
137	37	ECE5028	2008/6/2	Compal	SCH172197 : BID changed from X04 to A00	POP R529, DEPOP R534	A00
138	29	82567LM	2008/6/6	DELL	SCH172399 : LOM IEEE test result from Intel	C475 & C476 from 12PF to 27PF to pass LOM IEEE test	A00
139	42	LED	2008/6/6	Compal	SCH172401 : Breath LED current issue	R997 from 82 ohm to 100 ohm for current limited	A00
140	24	ICH	2008/6/6	Compal	SCH172404 : SAWTOOTH waveForm on SERIRQ issue	Add R122(33 ohm)	A00
141	36	USH5880	2008/6/13	BRCM	BRCM feedback for PI circuit	C1056/C1057 from 5% to 1% ; C641/C647 from 5% to 1%	A00

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1	43	+DC_IN	11/17	leverage Roush	Battery slice need detect NB battery is insert or not.	Add PQ61 NTR4502PT1G, and PD32 RB751_SOD323 Connect to DOCK_SMB_ALERT# and SLICE_BAT_PRES#	X01
2	43	+DC_IN	11/17	leverage Roush	DCIN_CBL_DET# damage ECE5028	Add ESD diedo PD17 DA204U_SOT323 at DCIN_CBL_DET# Series PR221 1K_0402_5% between PJPDC1, PIN1 and DCIN_CBL_DET# Parallel PC254 0.47uF_0402_6.3V on DCIN_CBL_DET#	X01
3	43	+DC_IN	11/17	leverage Roush	Roush component and rework changes for Dcoking test	PC4 change form 0.47uF_0805_25V to 0.1uF_0805_25V PR14 change form 240K_0402_5% to 1M_0402_5% PR17 change form 47K_0402_1% to 220K_0402_5% PR18 change form 47K_0402_1% to 22K_0402_5% PR342 change form 0_0402_1% to 100K_0402_5%	X01
4	48	Charger	11/17	leverage Roush	NB DC blocking MOSFET won't turn off when Dock AC insert.	Add PQ44 RHU002N06 control NB DC blocking MOSFET. Control singal is NB_AC_OFF Series PR284 200K_0402_1% between PQ44 PIN1 and ACAV_IN Add PD30 B540C parallel PQ34	X01
5	48	Charger	11/17	leverage Roush	Charger of ISL88731 will turn off When ACIN is no power	Add LM393 to replace ISL88731 ACOK function(PU11B)	X01
6	48 50	Charger Selector	11/17	leverage Roush	+PWR_SRC exist on Docking connector through the DOCK_DCIN_IS+ and -	Add PQ62 NTGD4161PT1G series DOCK_DCIN_IS+ and - Add PQ63 RHU002N06 to control PQ62 on/off	X01
7	48 50	Charger Selector	11/17	leverage Roush	A global signal name change for all notebooks	From "ACAV_IN_DOCK" to "ACAV_DOCK_SRC" From "ACAV_IN_DOCK#" to "ACAV_DOCK_SRC#"	X01
8	48	Charger	11/17	leverage Roush	SCH165050: Validate EMC4002 VIN1/VCP1/VCP2 for UMA & Discrete for PT1 SMT	Depop UL circuit.	X01
9	50	Selector	11/17	leverage Roush	PBATT DC blocking MOSFET won't turn off when Docking AC insert. It will cause Battery or adapter protect.	Add PD18 RB715F_SOT323, PD20 and PD19 RB751V_SOD323, PR329 100K_0402_5% PR328 and PR327 47K_0402_5%, PR326 and PR325 240K_0402_5% PQ69 2N7002DW-7-F_SOT363-6, PQ59 NTG6161PT1G_TSOP6 Extra net name add +NBDOCK_DC_IN_SS from Docking connector	X01
10	43	+DCIN	11/20	EE / SCH165224	follow HW change	To delete the RTC detection circuit	X01
11	48 50	Selector charger	11/30	Dell	for slice function implement	change charger output to FB pin15 net name from PBATT+ to +VCHGR Add PQ41 PQ70 PR351 PR352 PR353 between +VCHGR and PBATT+	X01
12	43	+DCIN	12/17	Dell	change DCIN connector for ESD issue of "DCIN_CBL_DET#"	from Molex_87437_0663 to MOLEX_87437-0763	X02
13	50	Selector	12/28	leverage Roush	follow Roush	change PQ63 from RHU002N06 to 2N7002DW ADD PD33 RB751V ADD PR354 ADD PQ77 RHU002N06 and PR355 0 ohm	X02
14	48	Charger	12/28	leverage Roush	follow Roush	Change PC131 from TBD to 0.047uF	X02

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15	47	+Vcore	02/18	Dell / Maxim	Reduce Ring-backwithin 20mV when change bulk caps from 4*220uF to 3*270uF	PR129 change from 909 ohm to 825 ohm	
16	50	Selector	02/18	Merle DELL	Fix BITS CR196131 and CR196130	Add PR363 1K_1206 and PC262 1U_0603_25V from +NBDOCK_DC_IN_SS to ground Add PD35 RB751S40T1_SOD523-2 from NB_AC_OFF# to ACAV_IN_NB	
17	47	+Vcore	02/18	Maxim	Fix Jitter issue	change PR123 to 10_ohm change PC122 to PR320 10_ohm	
18	48/50	charger / selector	02/26	Compal	location change for Charger 2nd source X76 BOM control	change PR141 to PR217      change PR217 to PR141 change PR228 to PR218      change PR218 to PR351 change PR230 to PR219      change PR219 to PR352 change PR229 to PR220      change PR220 to PR353 change PR284 to PR307 change PQ62 to PQ70      change PQ70 to PQ76	
19	48	Charger	03/06	Compal	Delete non-use circuit	delete +DC_IN_SS to PR217 and PR217.	
20	50	Selector	03/06	Compal	For slice battery hot docking issue	Change PQ40 from IMD2AT to 2N7002DW change PR202 from240K_ohm ot 620k_ohm change PR204 from 47K_ohm to 33_ohm add PR222 390K_ohm and PR223 390K_ohm add PD34 RB751S40T1	
21	47	+Vcore	03/11	Maxim	For driver IC power down issue	Add PR321 PR322 PR323 from IC pin 2 to GND	
22	44-50	All	03/19	Compal	EMI solution	Change PR32 PR33 PR57 PR58 PR64 PR74 PR91 PR144 PR177 to 2.2_ohm Add PC198 PR211 PC199 PR212 PC200 PR213 PC201 PR214 PC202 PR215 PC87 PR72 PC91 PR75 PC100 PR90 PC102 PR95 PC114 PR108 PC118 PR119 PC204 PR216 PC184 PR181 PC128 PC130	
23	45	1.5V/1.05v	4/23	Compal	change non-lead free part to lead free part	PR47 change from SD03415830L to SD03415838L	
24	47	Vcore	4/23	Maxim	Driver IC power down issue need change resistor value	change PR321 PR322 PR323 to 33K	
25	49	ADP3209	4/23	Intel Compal	Follow Roush VGFX DC load line slope change to -7.5mOhm	Change PR192 from 75K_0603 to 68.1K_0603	
26	43	DC-IN	6/3	Compal	Glitch issue on SLICE_BAT_PRES#	Add PC257:SE074152K8L(S CER CAP 1500P 50V +-10% X7R 0402) between pin2 of PQ61 and GND.	
27	50	Selector	6/4	Compal	Reserve a pull high resistor between +3.3V_ALW2 and SLICE_BAT_PRES#	Add un-pop PR330:SD02847018L(S RES 1/16W 4.7K +-5% 0402) between +3.3V_ALW2 and PQ40B.5.	