

COMPAL CONFIDENTIAL

MODEL NAME : *QAL81*
PCB NO : *LA-7782P (DAA00002J00)*
BOM P/N : *TBD*
GPIO MAP: E4_VC_GPIO_map_rev_0.8

Dalmore 14 DSC

Ivy Bridge + Panther POINT

2011-05-12

REV : 0.1 (X00)

@ : Nopop Component

CONN@ : Connector Component

MB Type	BOM P/N
TPM	1@ 3@
TCM	2@ 4@
TPM DIS/TCM DIS	2@ 3@

Part Number	Description
DAA00002J00	PCB 0LE LA-7782P REV0 M/B DSC

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DIS Block Diagram

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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

Layer No.	Name	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
		SolderMask	min 0.4	0.50000
		Add Plating		1.45000
1	Top	Copper foil	0.5oz(0.68)	0.65000
		Prepreg	1080	2.75000
2	GND1	Copper foil	1oz(1.35)	1.35000
		Core	4mil	3.89000
3	IN 1	Copper foil	1oz(1.35)	1.35000
		Prepreg	1506	5.50000
4	GND2	Copper foil	1oz(1.35)	1.35000
		Core	3mil	3.09000
5	IN 2	Copper foil	1oz(1.35)	1.35000
		Prepreg	1506*2	11.50000
6	IN 3	Copper foil	1oz(1.35)	1.35000
		Core	3mil	3.09000
7	VCC	Copper foil	1oz(1.35)	1.35000
		Prepreg	1506	5.50000
8	IN 4	Copper foil	1oz(1.35)	1.35000
		Core	4mil	3.89000
9	GND 3	Copper foil	1oz(1.35)	1.30000
		Prepreg	1080	2.75000
10	Bottom	Copper foil	0.5oz(0.68)	0.65000
		Add Plating		1.45000
		SolderMask	min 0.4	0.50000
	Overall Thickness (1.45mm ± 10%)			57.91000

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

need to update Power Status and PM
Table

DSC DP/HDMI Port	Connetion
Port C	Dock DP port 2
Port D	Dock DP port 1
Port E	MB HDMI Conn

USB PORT#	DESTINATION
0	JUSB1 (Right side Top)
1	JUSB2 (Right side Bottom)
2	JESA1 (Right side ESATA)
3	MLK DOCK
4	WLAN
5	WWAN
6	JMINI3(Flash)
7	USH->BIO
8	DOCKING
9	JUSB (Left side)
10	Express card
11	Bluetooth
12	Camera
13	LCD Touch

USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	E3 Module Bay (USB3)
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

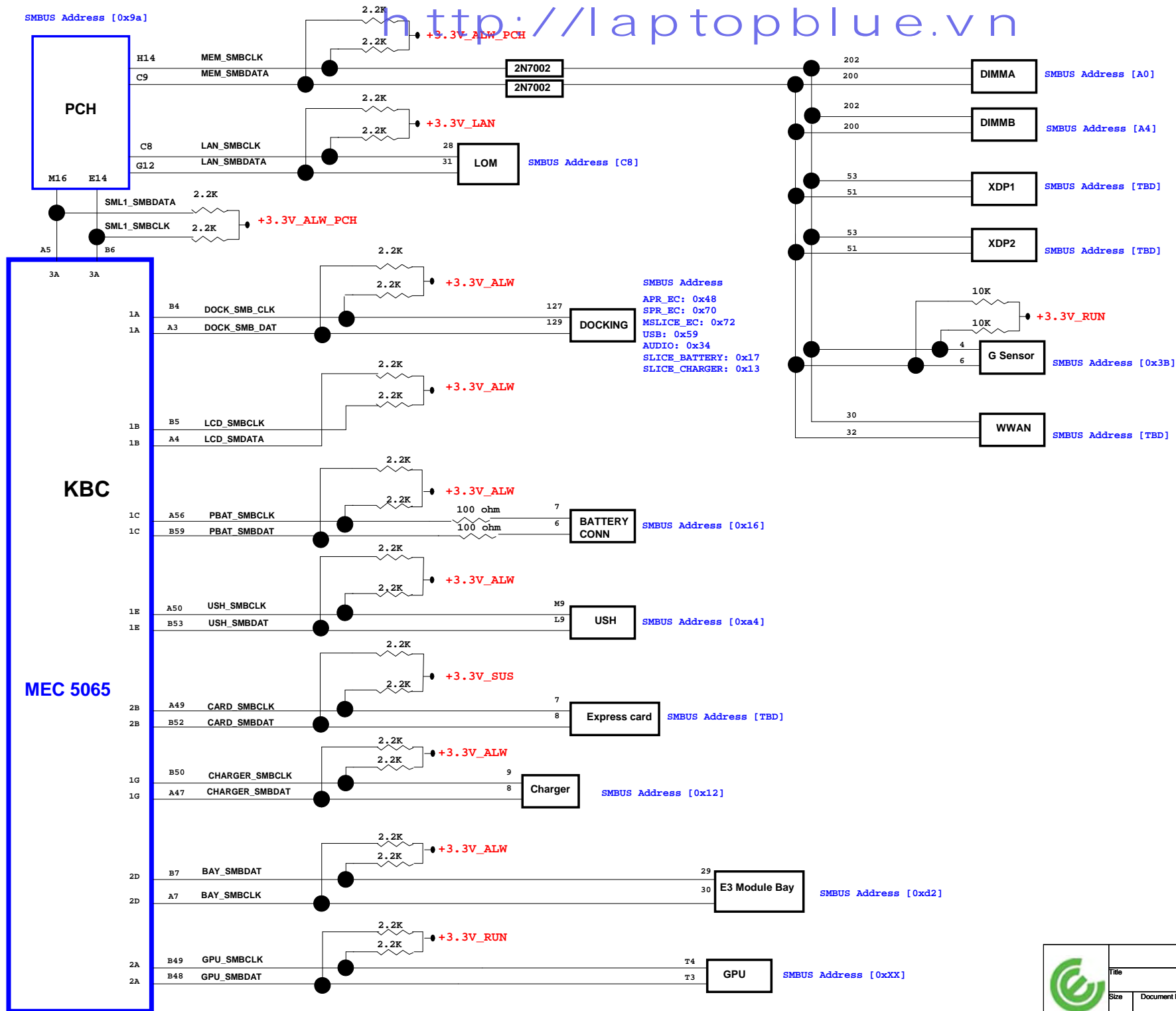
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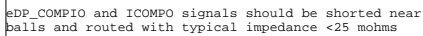
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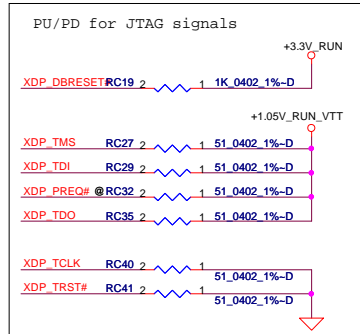
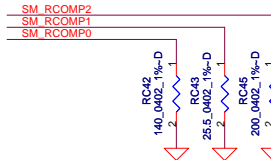
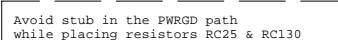
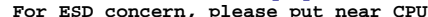
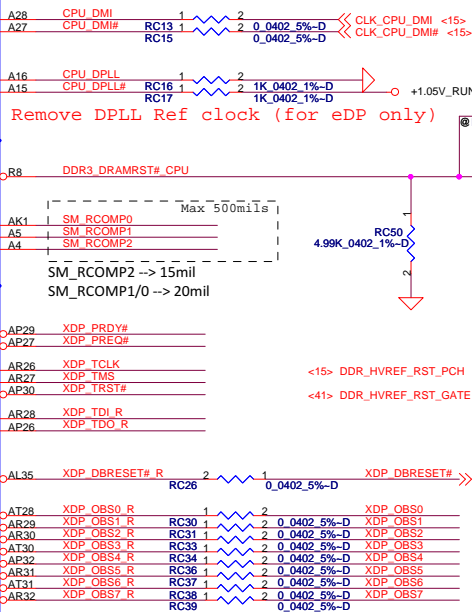
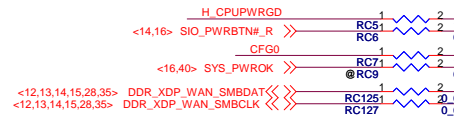
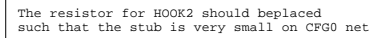
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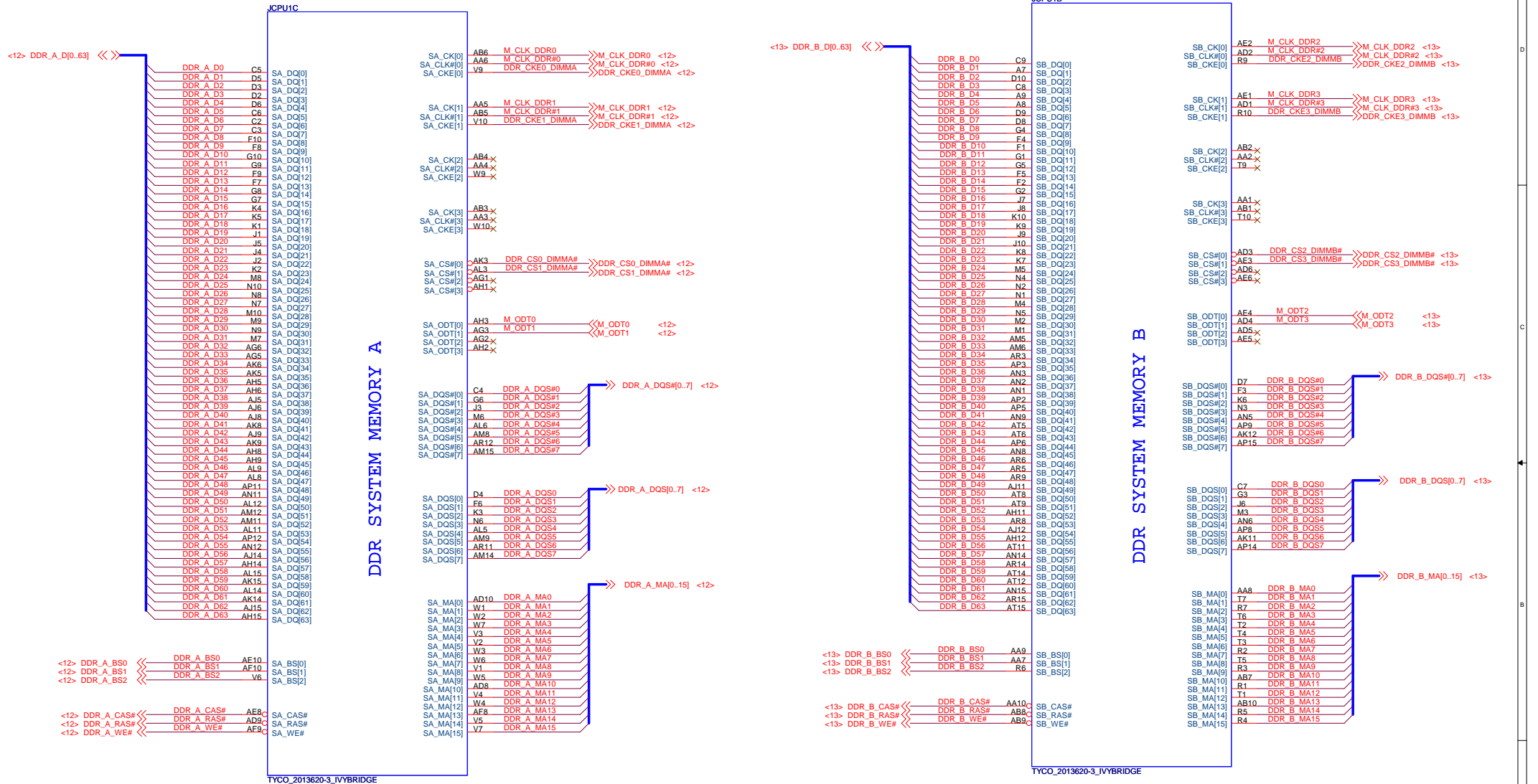
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SMBUS Address [0x9a]









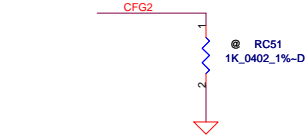
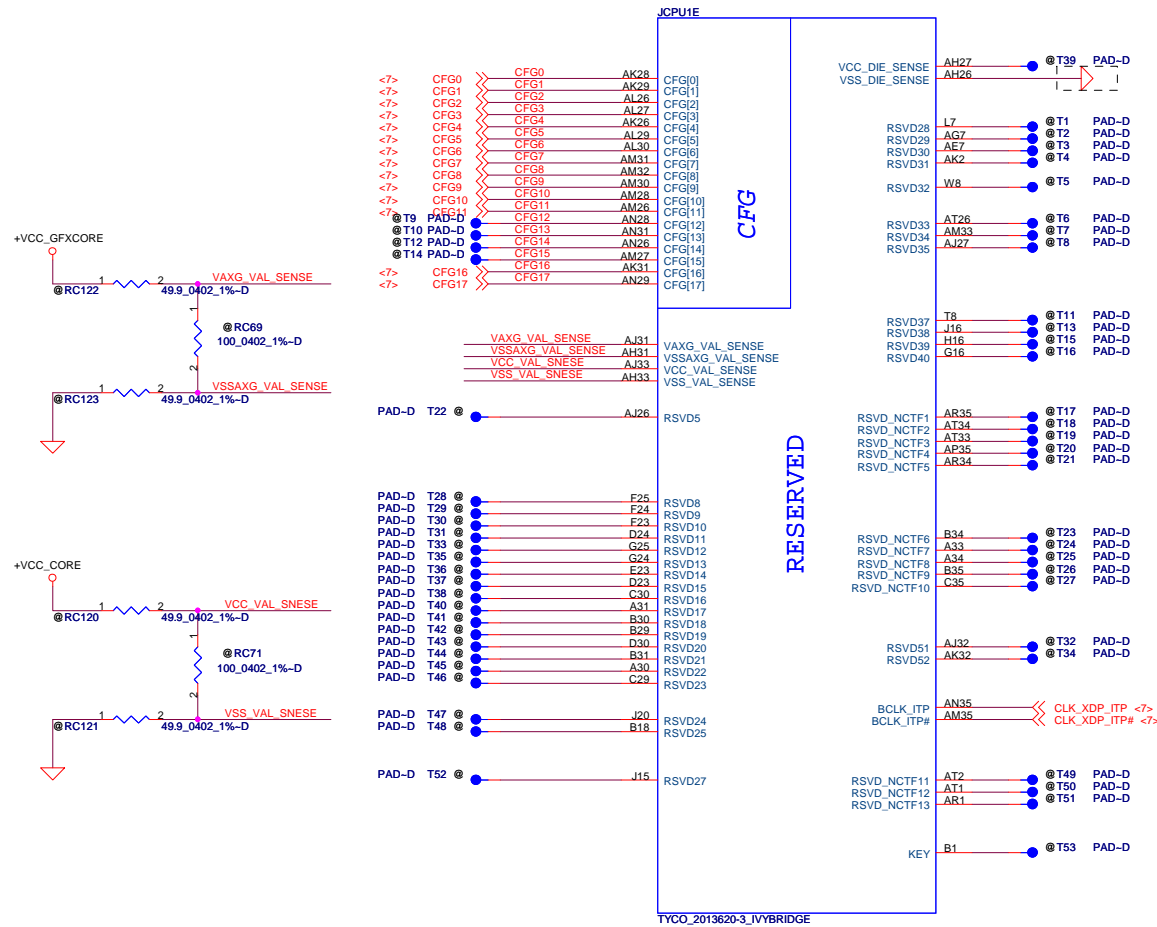
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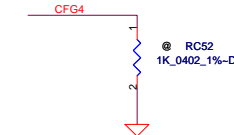
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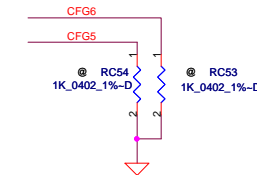
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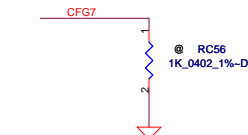
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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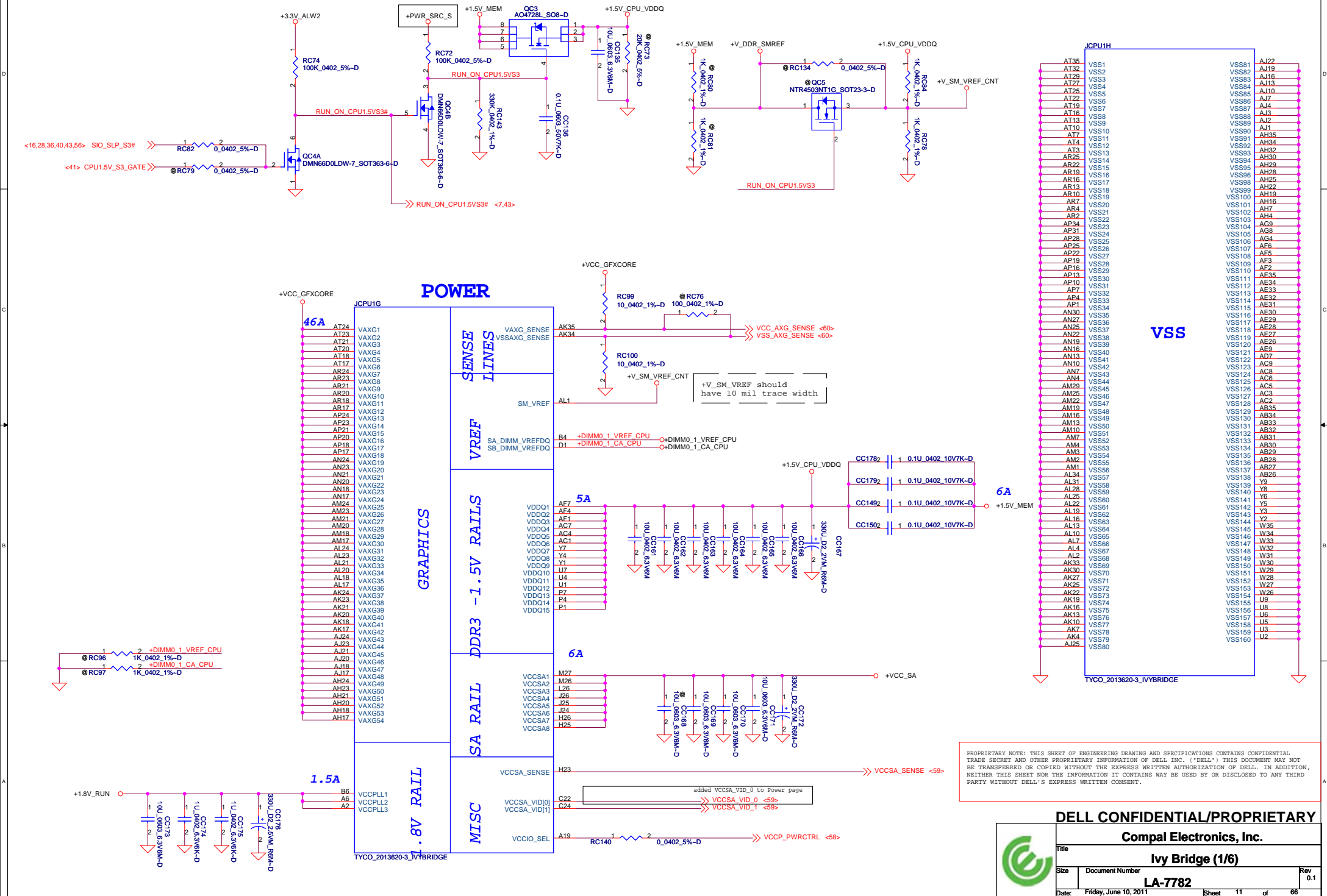
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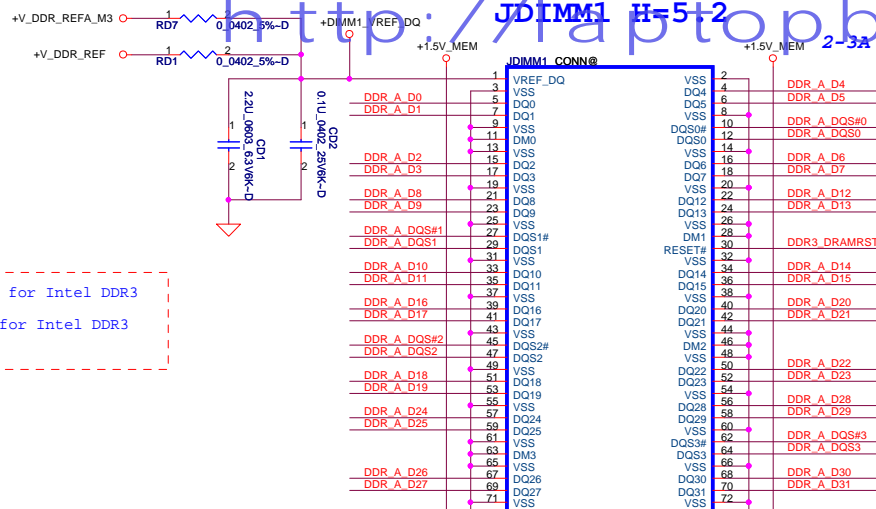
+1.5V_CPU VDDQ Source



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Ivy Bridge (1/6)		
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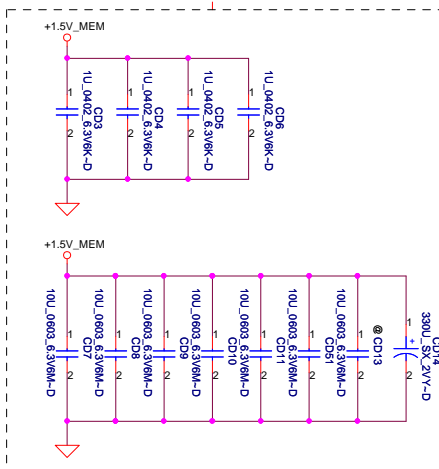


Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

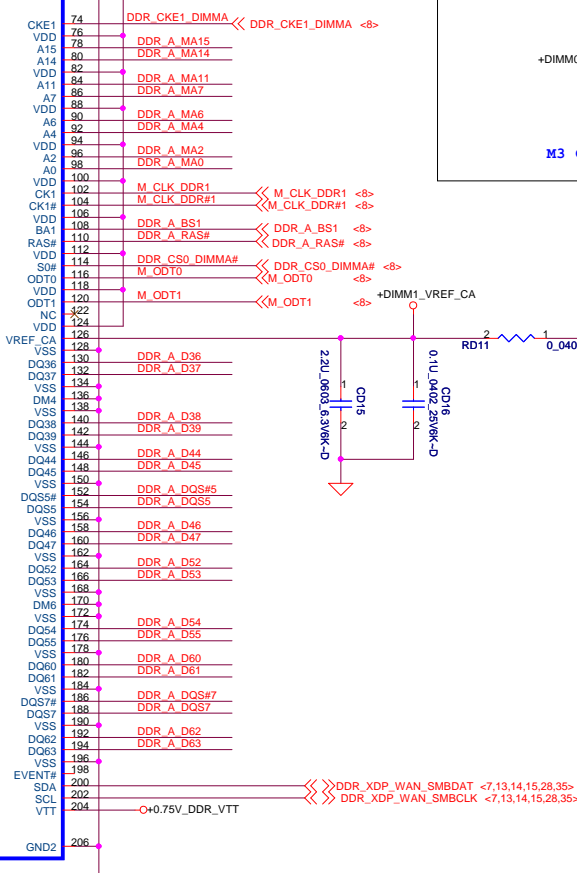
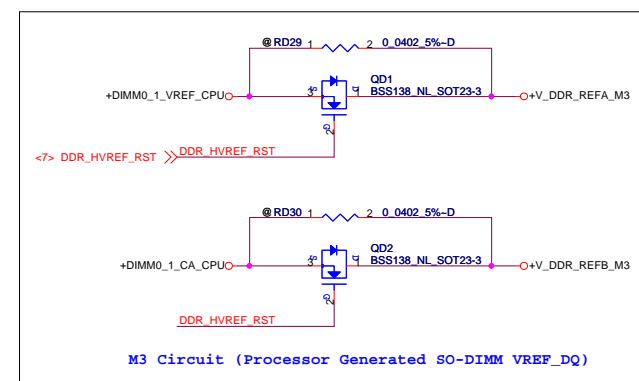
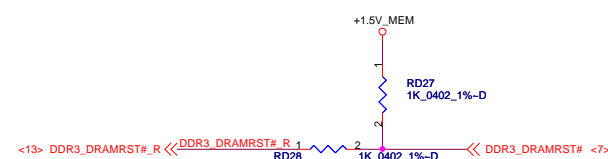
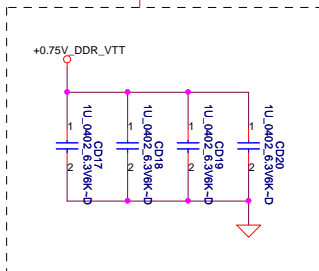
All VREF traces should have 10 mil trace width

<8> DDR_A_DQS#[0..7] <<>>
<8> DDR_A_D#[0..63] <<>>
<8> DDR_A_DQS#[0..7] <<>>
<8> DDR_A_MA#[0..15] <<>>

Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204



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3300 SX 2V2-C

CD28
100,000.0, 6.3V6K-D

CD27
100,000.0, 6.3V6K-D

CD26
100,000.0, 6.3V6K-D

CD25
100,000.0, 6.3V6K-D

CD24
100,000.0, 6.3V6K-D

CD23
100,000.0, 6.3V6K-D

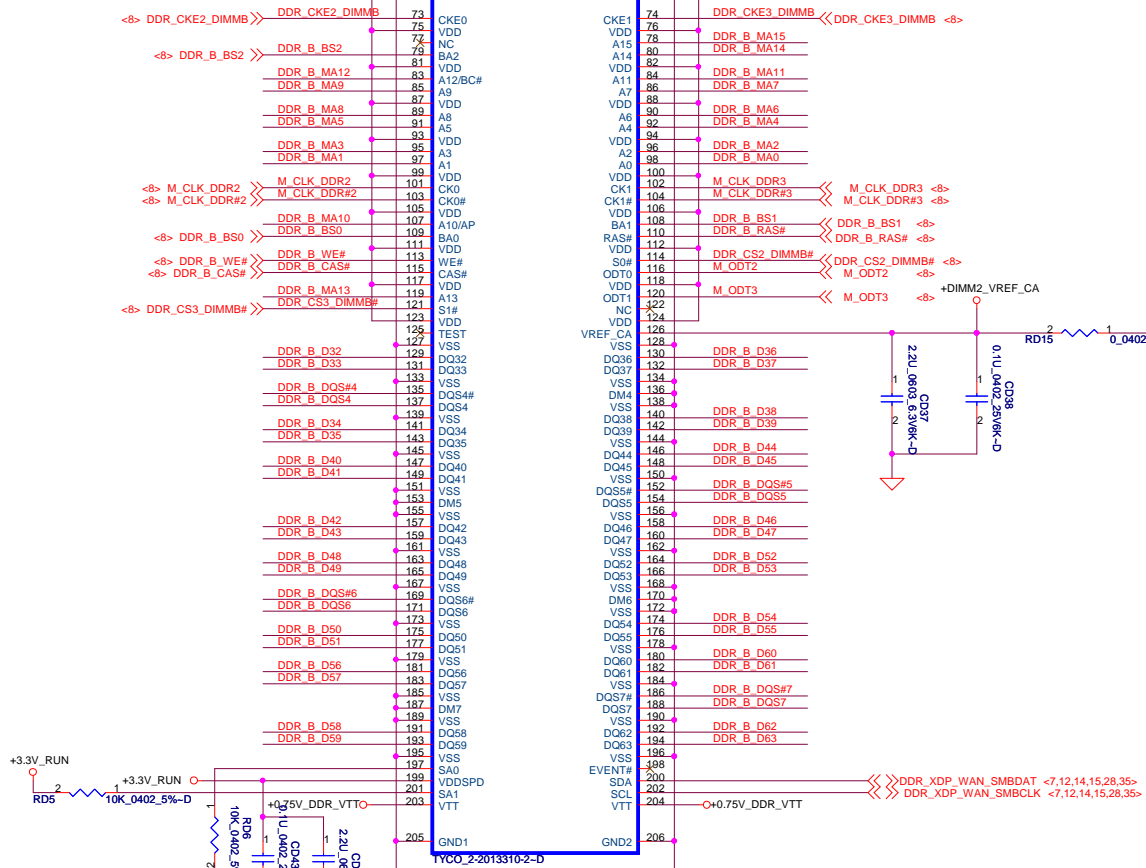
CD32
100,000.0, 6.3V6K-D

CD31
100,000.0, 6.3V6K-D

CD30
100,000.0, 6.3V6K-D

CD29
100,000.0, 6.3V6K-D

1.5V MEM



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ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

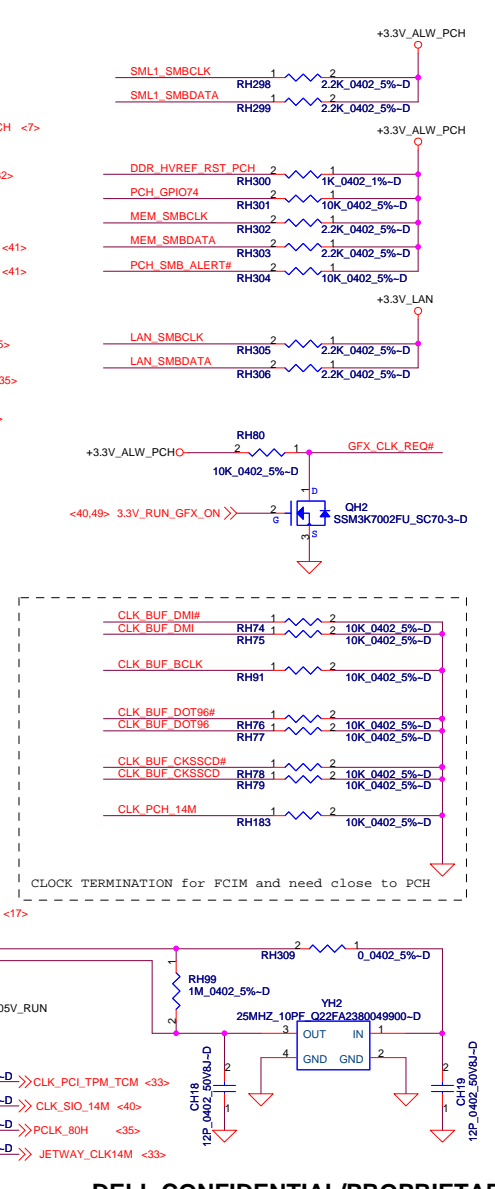
PCH_AZ_SYNC is sampled
at the rising edge of RSMRST# pin.
So signal should be PU to the ALWAYS rail.



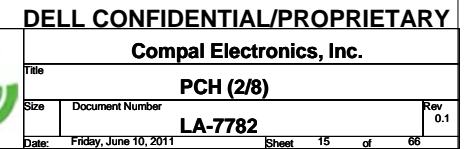
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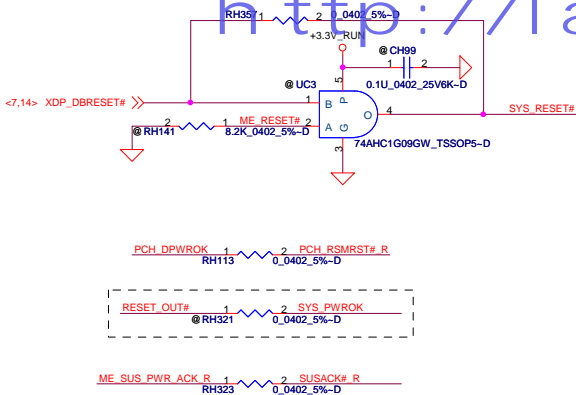
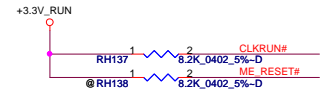
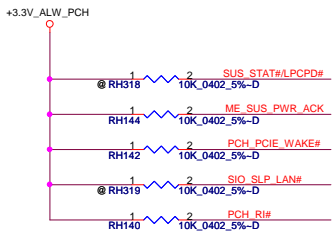


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PCH (1/8)			
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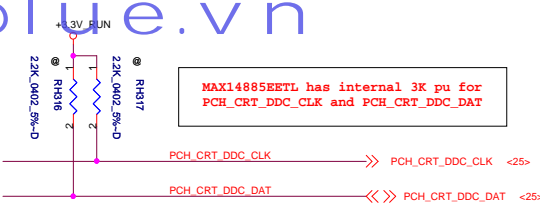


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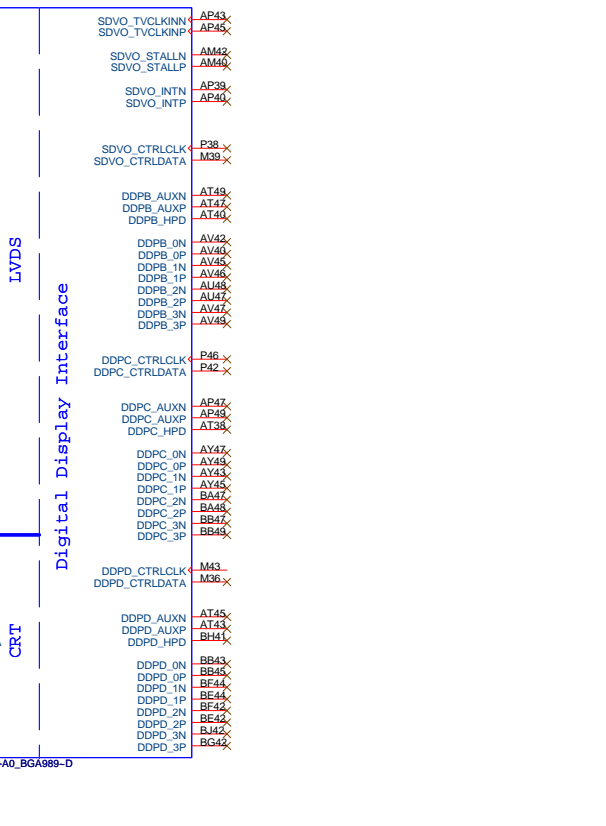
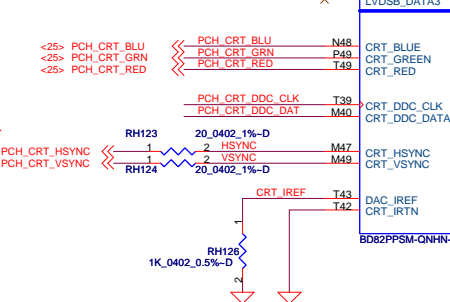
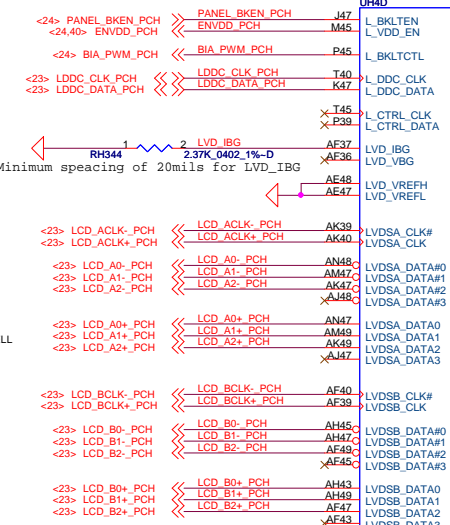
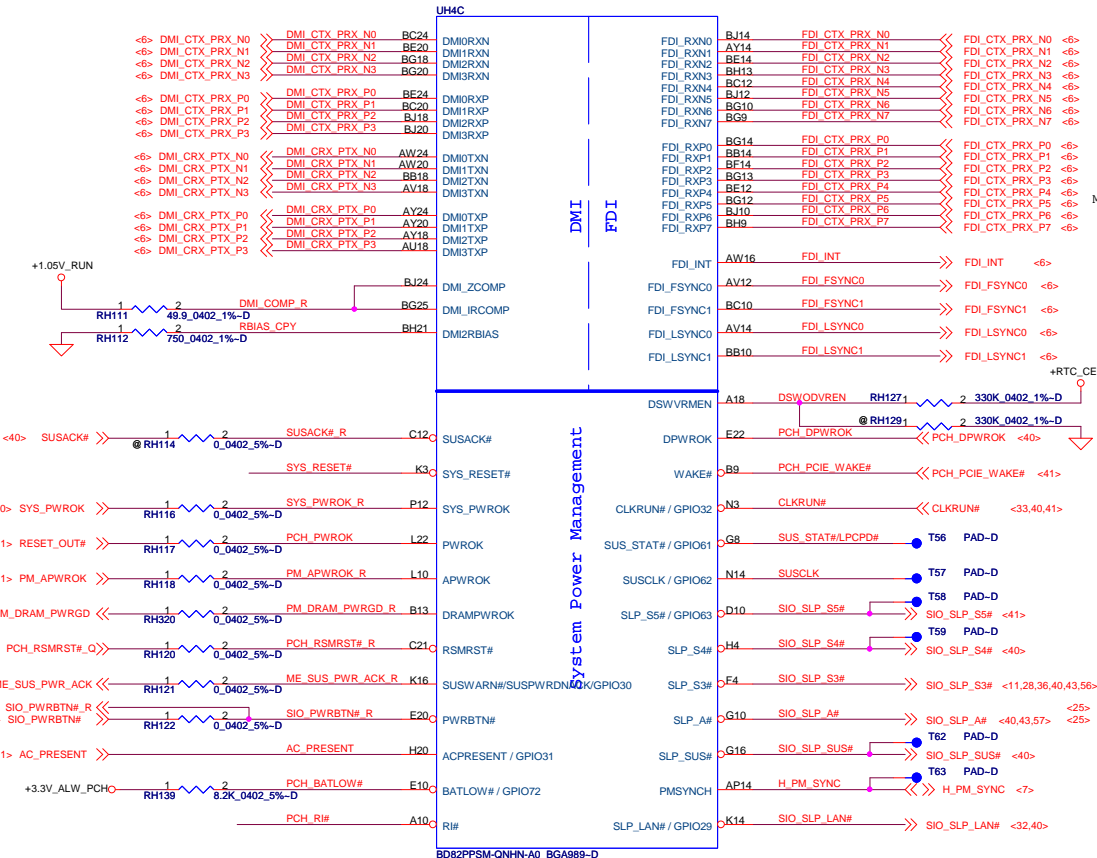




DSWODVREN - On Die DSW VR Enable
Enabled (DEFAULT)
HIGH: RH127 STUFFED,
RH129 UNSTUFFED
Disabled
LOW: RH129 STUFFED,
RH127 UNSTUFFED



MAX1485EETL has internal 3K pu for
PCH_CRT_DDC_CLK and PCH_CRT_DDC_DAT



Intel request DDPB can not support eDP

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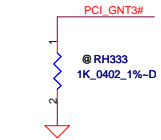
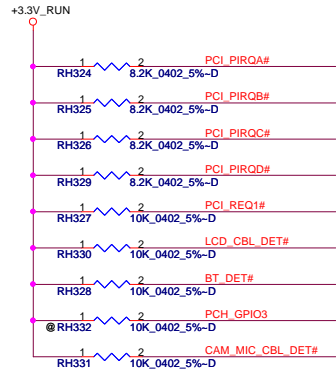
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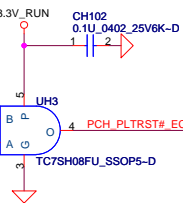
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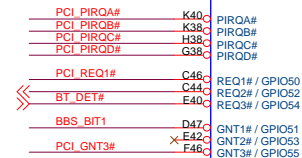


A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

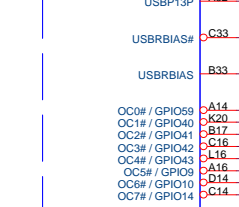
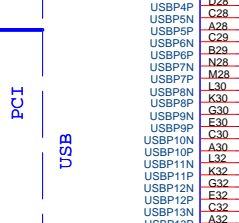
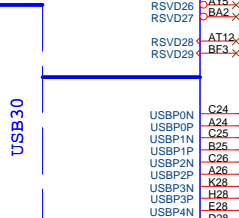
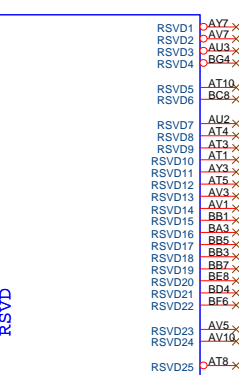
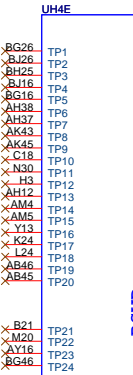
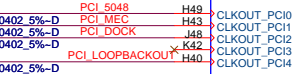
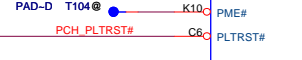


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<42> BT_DET#

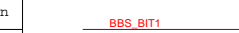
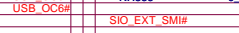
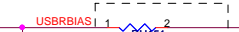
<24> LCD_CBL_DET#
<28> HDD_FALL_INT



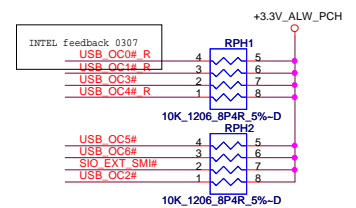
<24> LCD_CBL_DET#
<28> HDD_FALL_INT



BD82PPSM-QNH-A0_BGA989-D

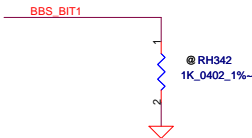


- >Right Side Top
- >Right Side Bottom
- >Right side E-SATA
- >MLK DOCK
- >WLAN/WIMAX
- >WWAN/UWB
- >Flash
- >USH
- >DOCK
- >Left side
- >Express Card
- >Blue Tooth
- >Camera
- >LCD Touch



Route single-end 50-ohms and max 500-mils length.
Minimum spacing to other signals: 15 mils

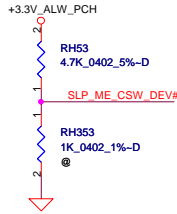
Boot BIOS Strap		
BBS_BIT1	SATA_SLDP (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



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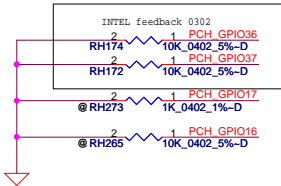
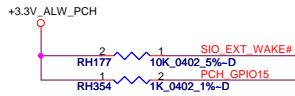
Compal Electronics, Inc.		
PCH (4/8)		
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Date: Friday, June 10, 2011	Sheet 17 of 66	



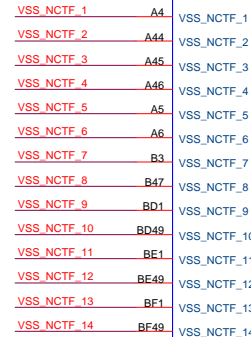
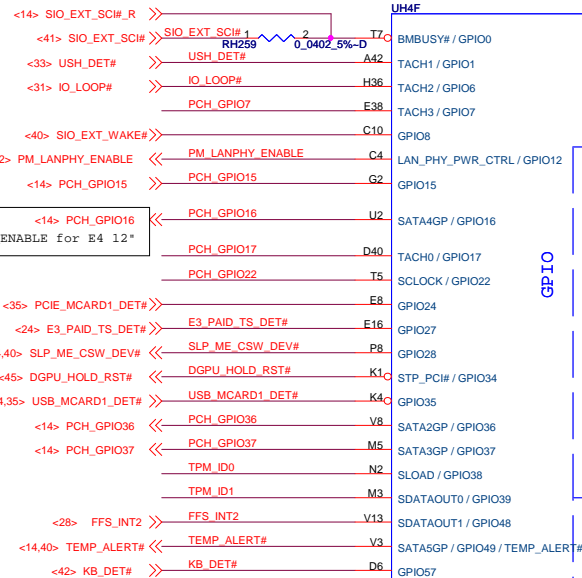
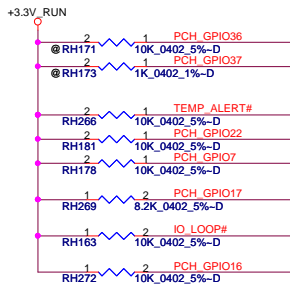
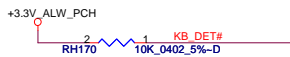
Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET# (GPIO27)

SLP_ME_CSW_DEV# PLL ON DIE VR ENABLE

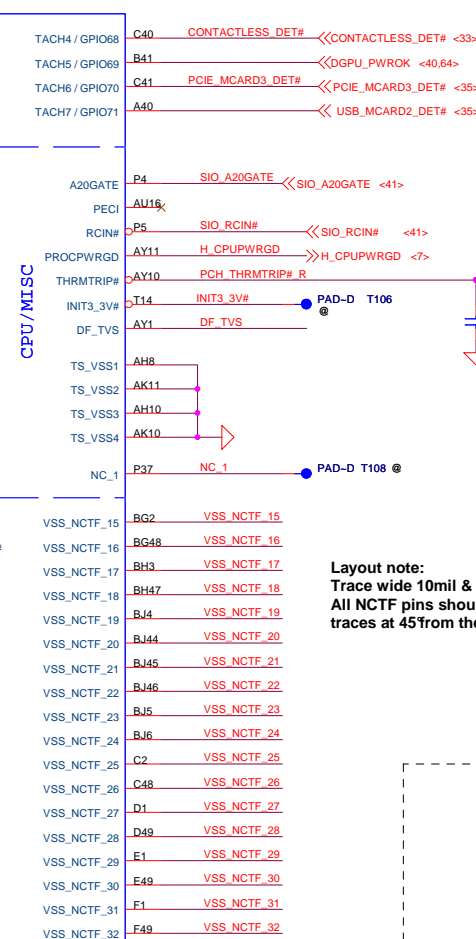
ENABLED - HIGH DEFAULT
DISABLED - LOW



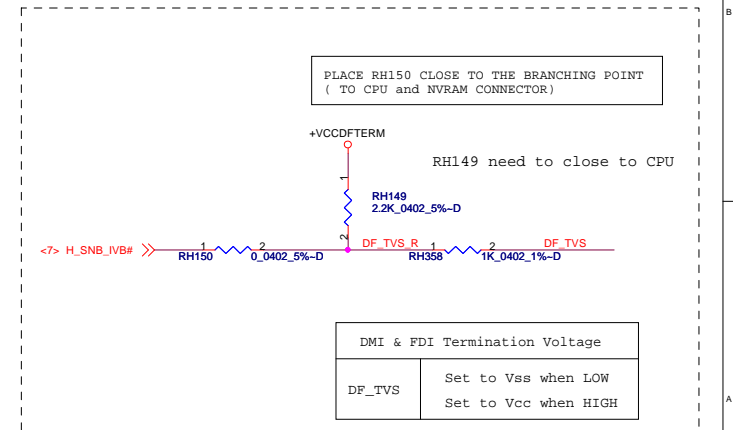
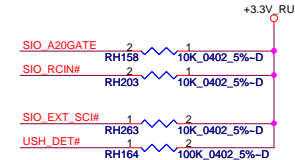
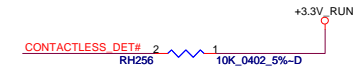
Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45 from the pad.



	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
TBD		
TPM	1	1

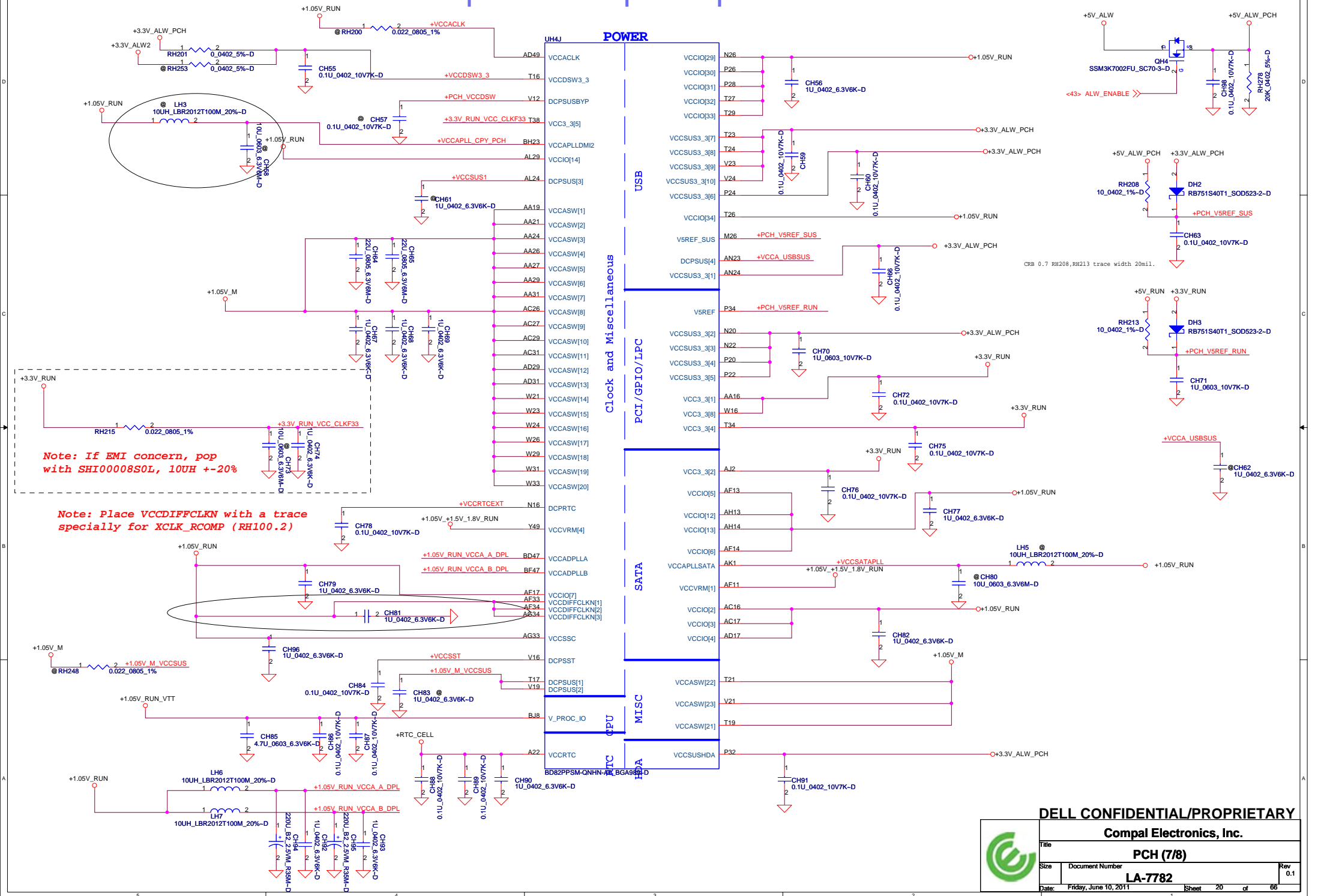


Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45 from the pad.



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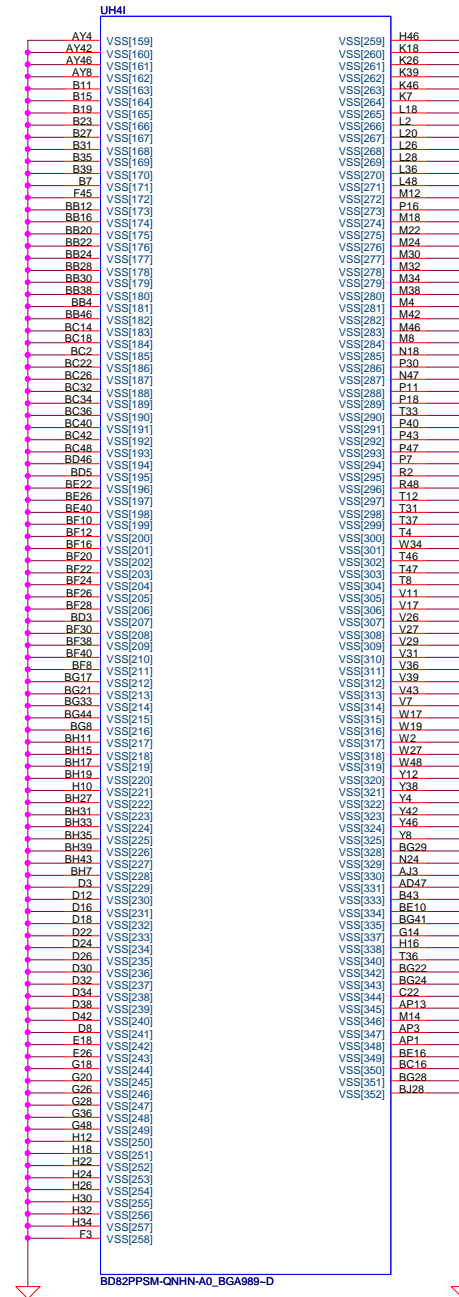
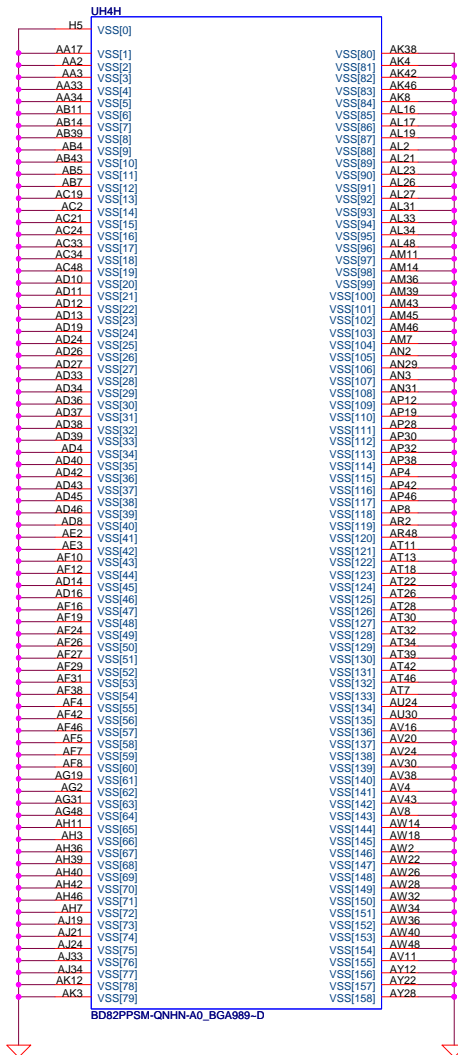
Compal Electronics, Inc.			
PCH (5/8)			
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Compal Electronics, Inc.			
PCH (7/8)			
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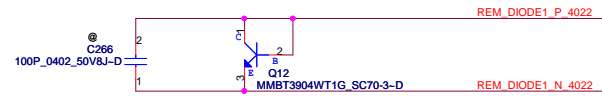
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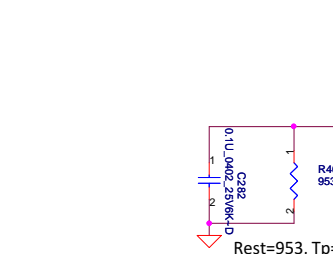
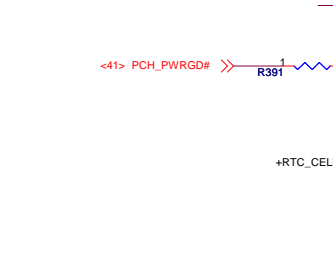
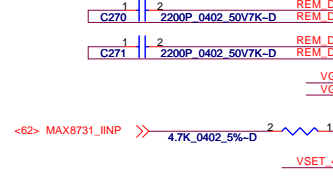
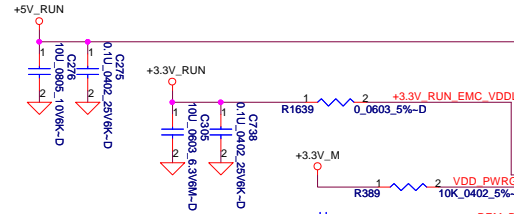
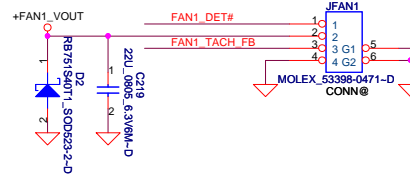
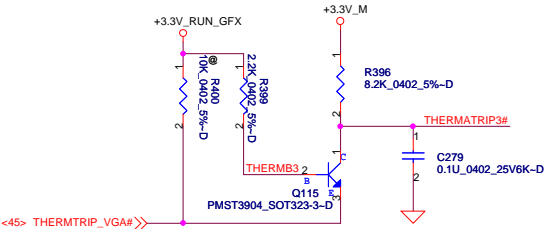
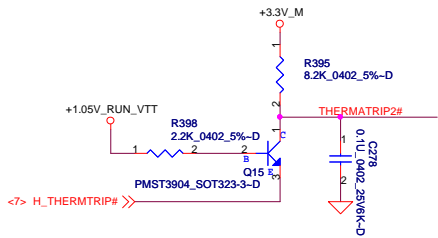
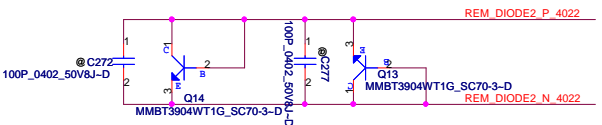
Compal Electronics, Inc.

Title			
PCH (8/8)			
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Place under CPU
Place C266 close to the Q12 as possible

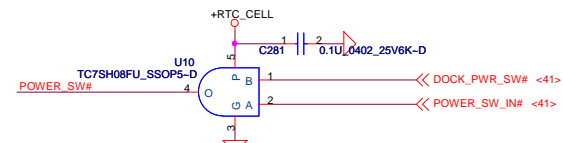
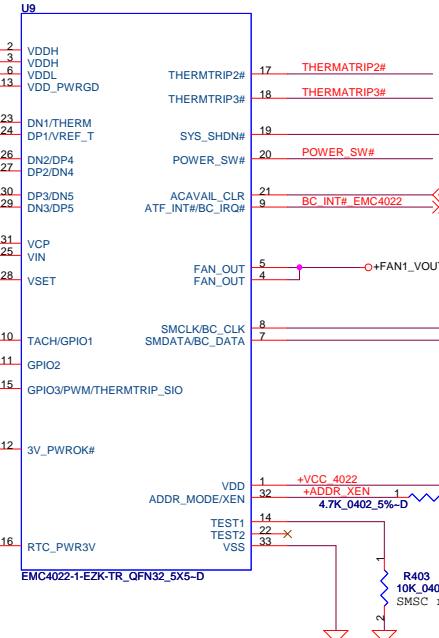
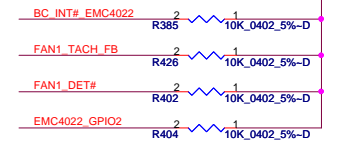
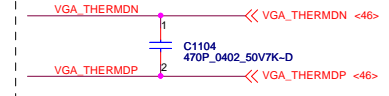


- DP3/DN3 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
- DP5/DN5 for Skin on Q13, place Q13 close to Vcore VR choke.



Rest=953, Tp=88degree

DSC only



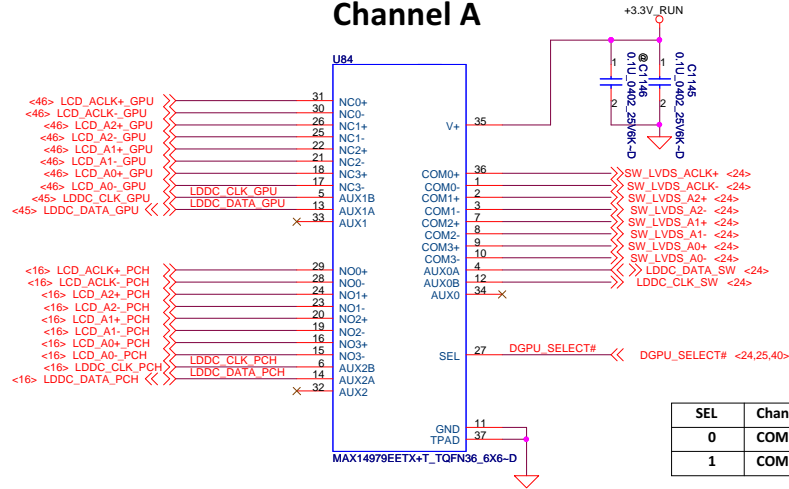
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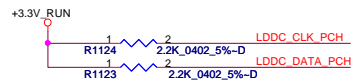
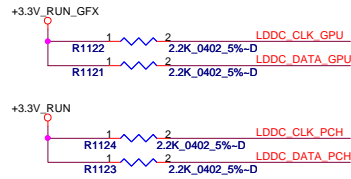
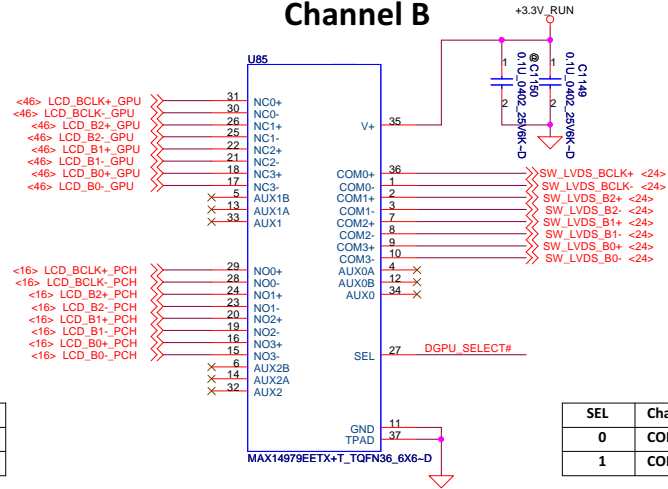
Compal Electronics, Inc.			
Title	FAN & Thermal Sensor		
Size	Document Number	Rev	0.1
LA-7782			
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Channel A



Channel B

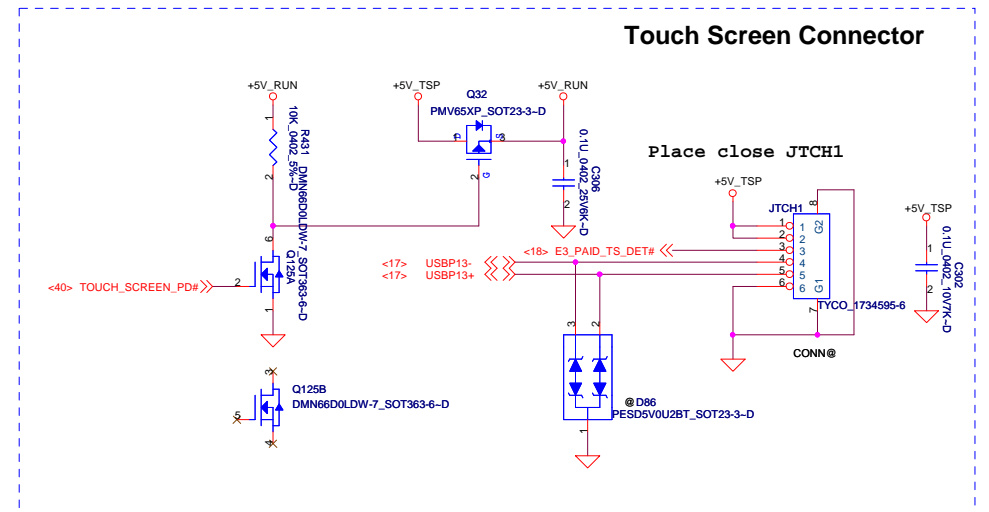
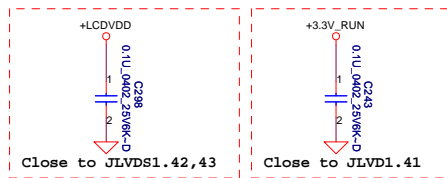
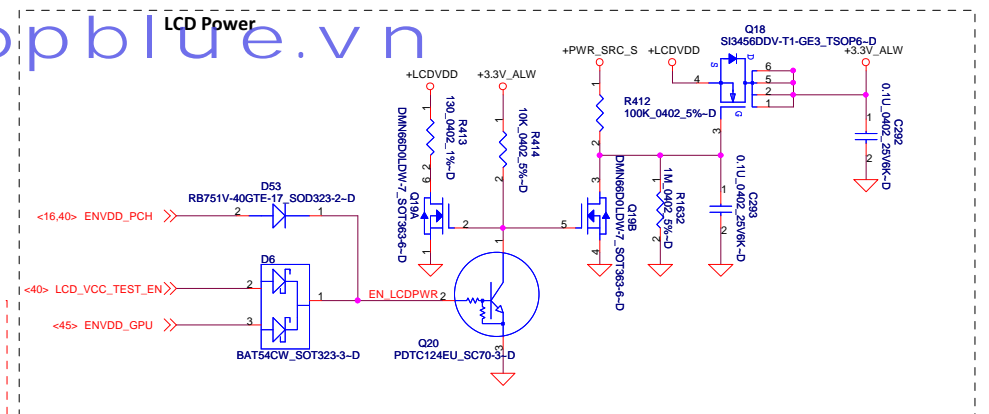


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0.1

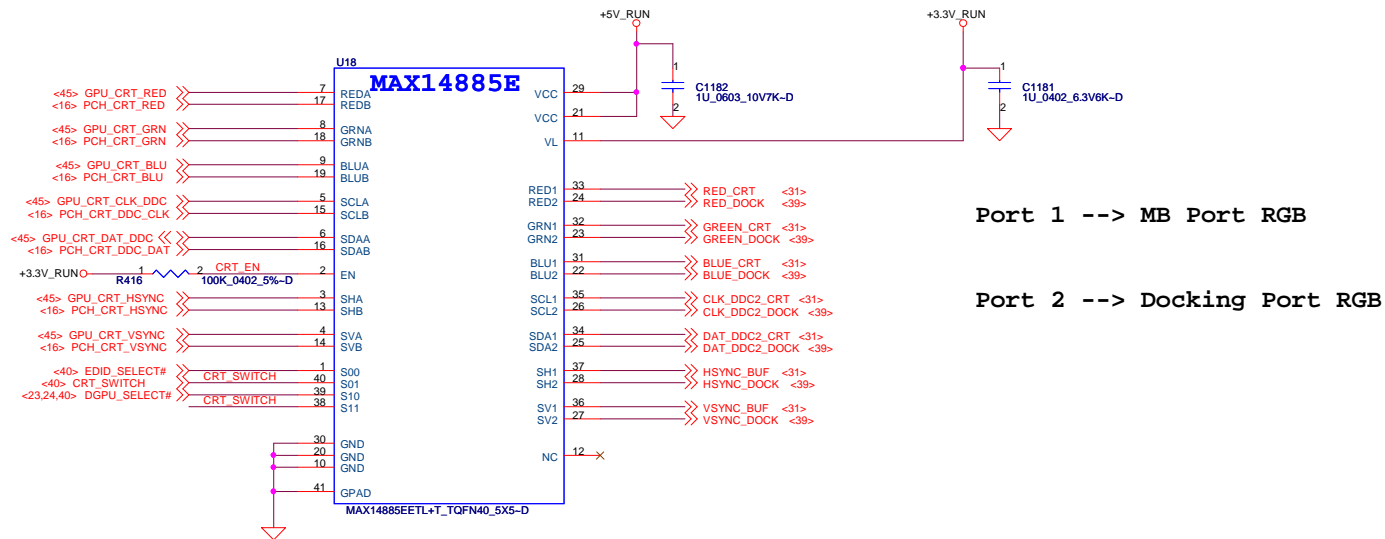
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Channel A --> GPU

Channel B --> PCH

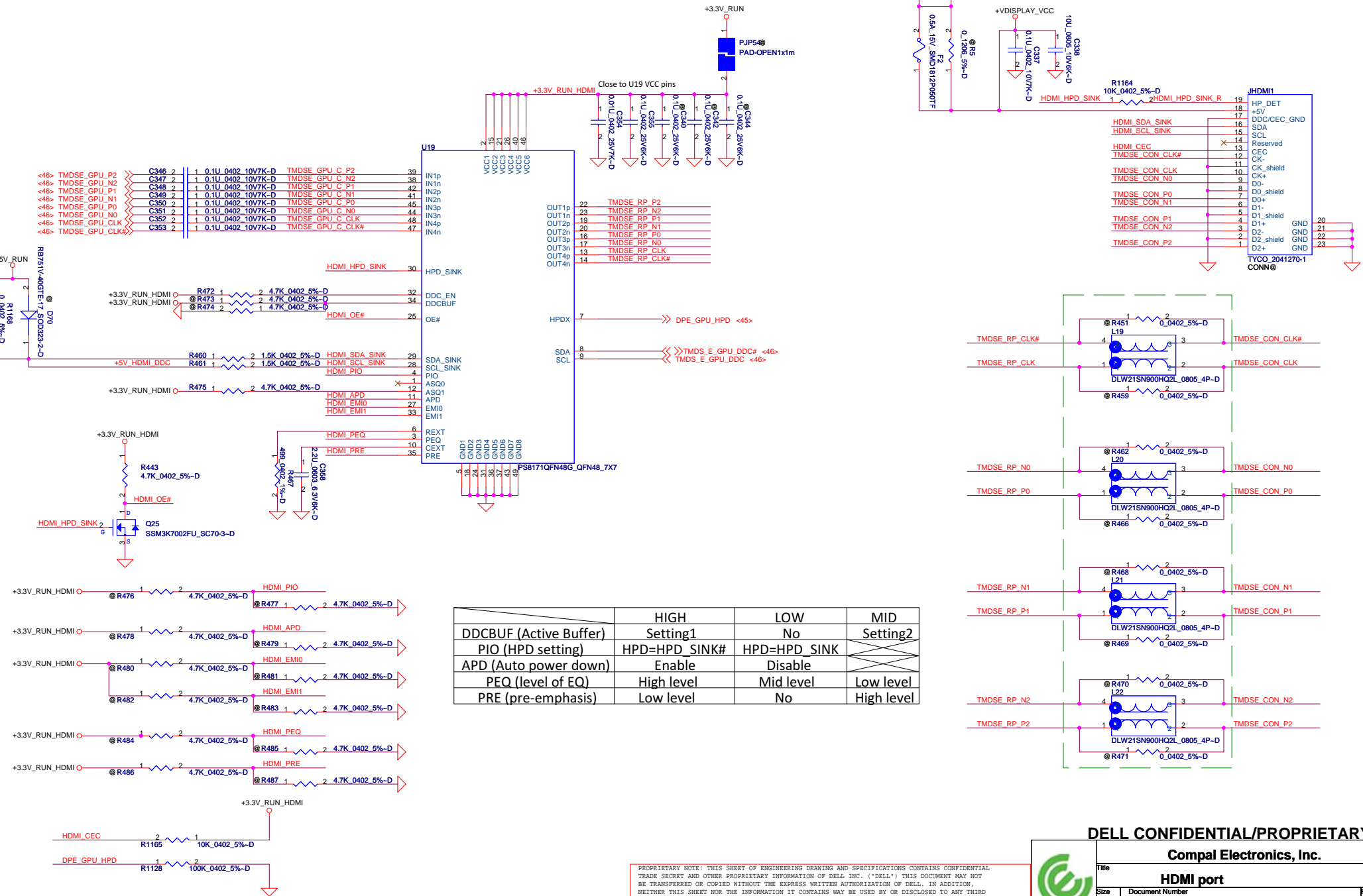


CRT_SWITCH	0	0	1	1
DGPU_SELECT#	0	1	0	1
EDID_SELECT#	0	1	0	1
	A --> Port 1	B --> Port 1	A --> Port 2	B --> Port 2

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Title CRT/Video switch			
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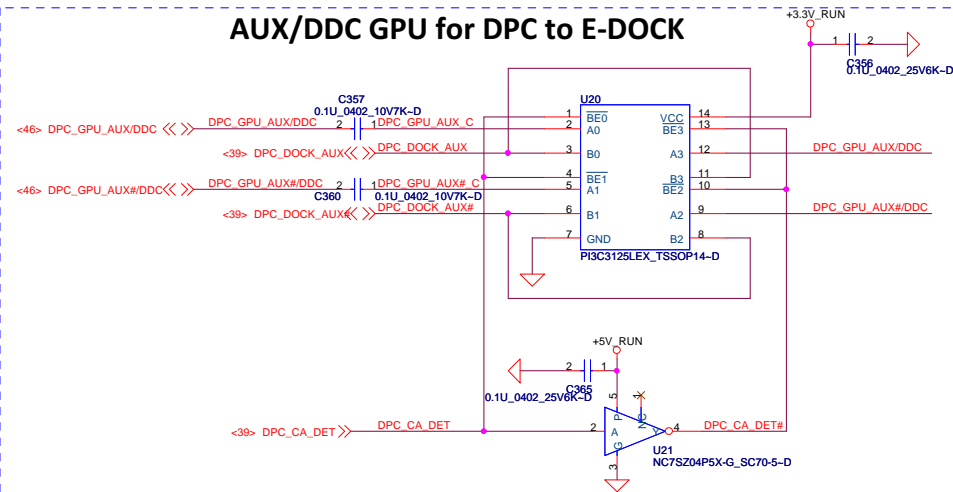


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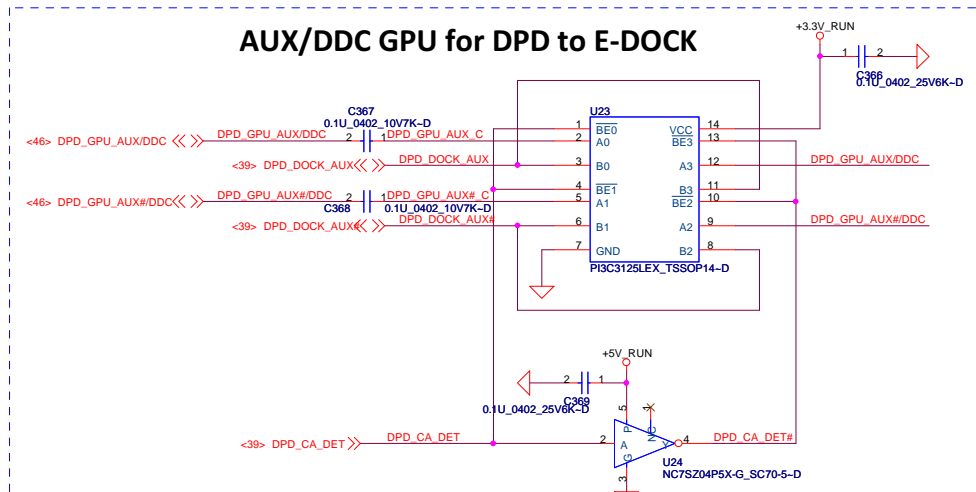
Compal Electronics, Inc.

Title		HDMI port	
Size	Document Number	LA-7782	
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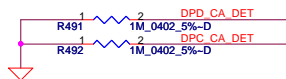
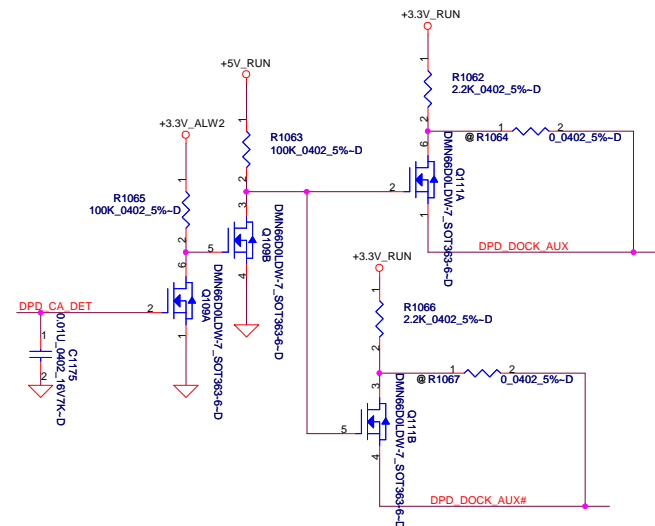
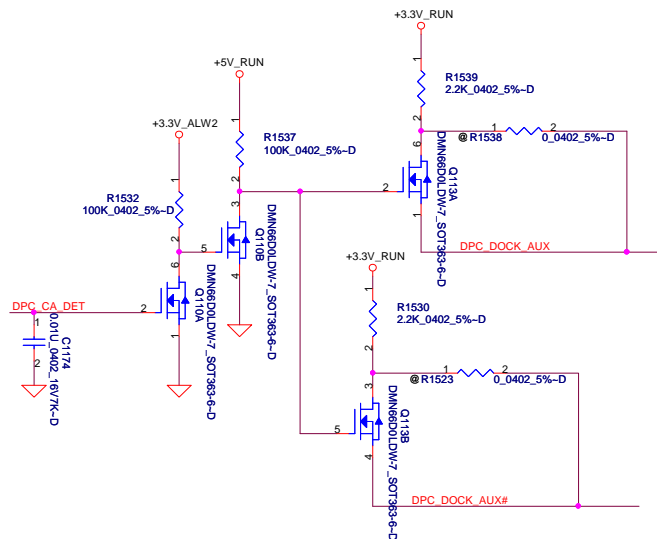
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AUX/DDC GPU for DPD to E-DOCK



There is a new die for PI3C3125. Sample available on May.



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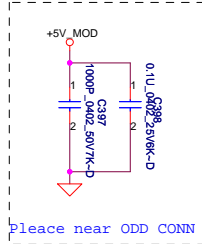
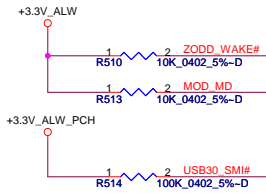
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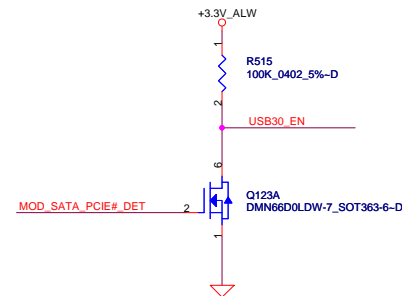
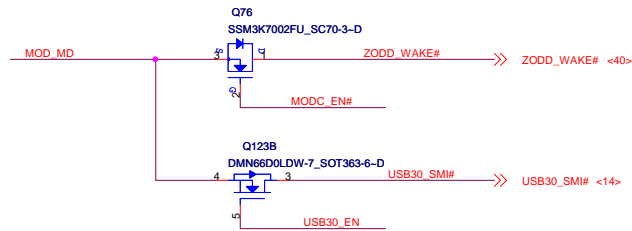
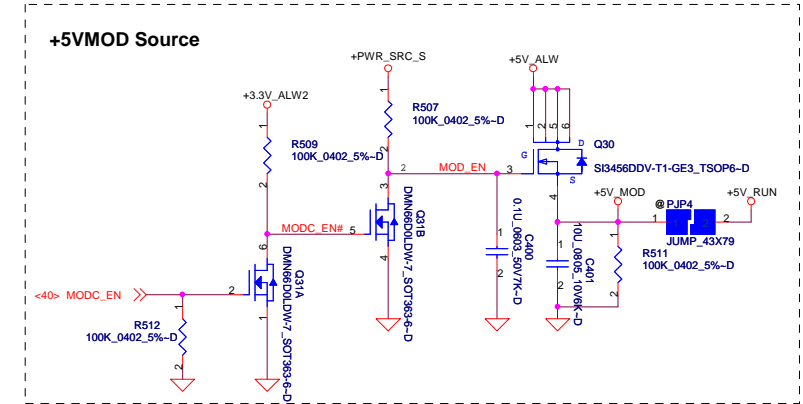
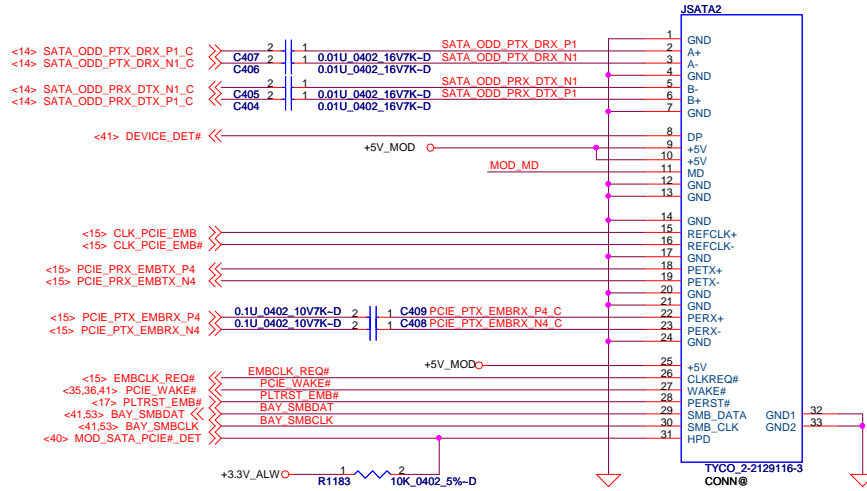
Title			
DP AUX SW			
Size	Document Number		Rev
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For ODD



place near ODD CONN



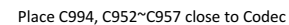
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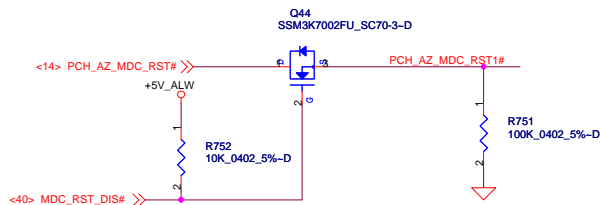
Compal Electronics, Inc.

Title			
ODD CONNECTOR			
Size	Document Number	Rev	
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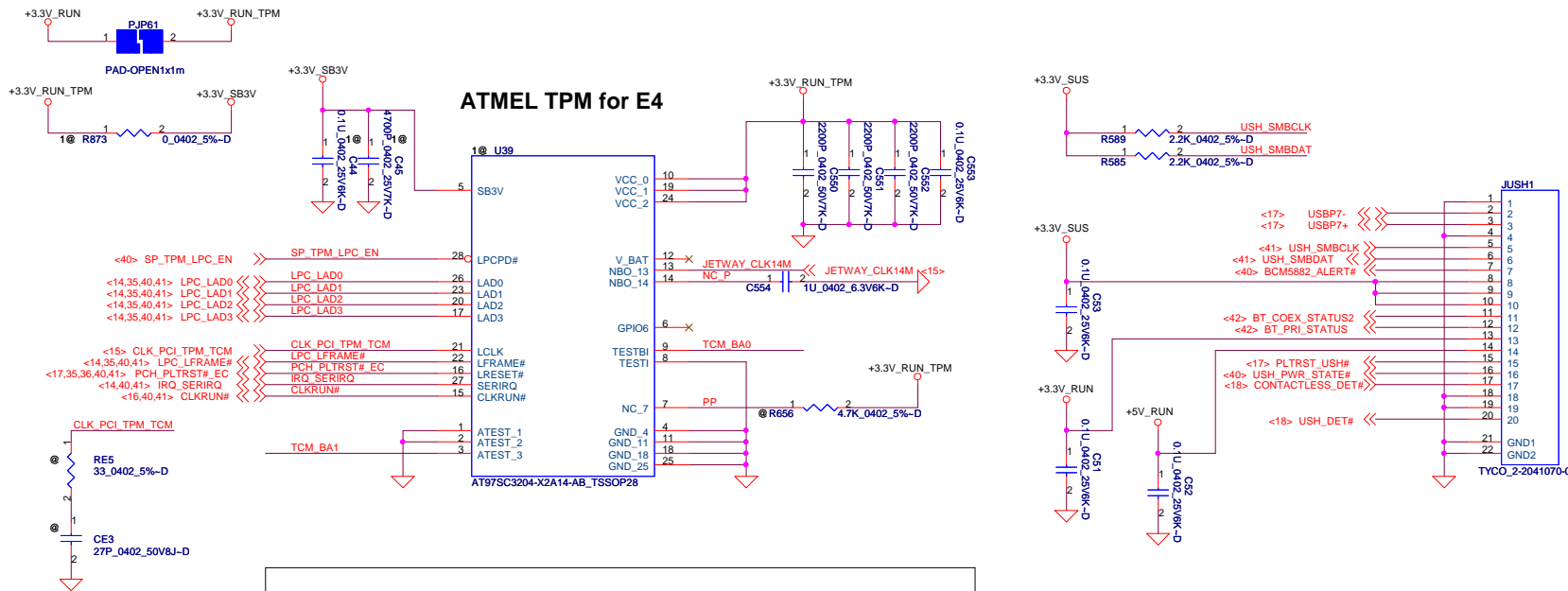
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http://laptopblue



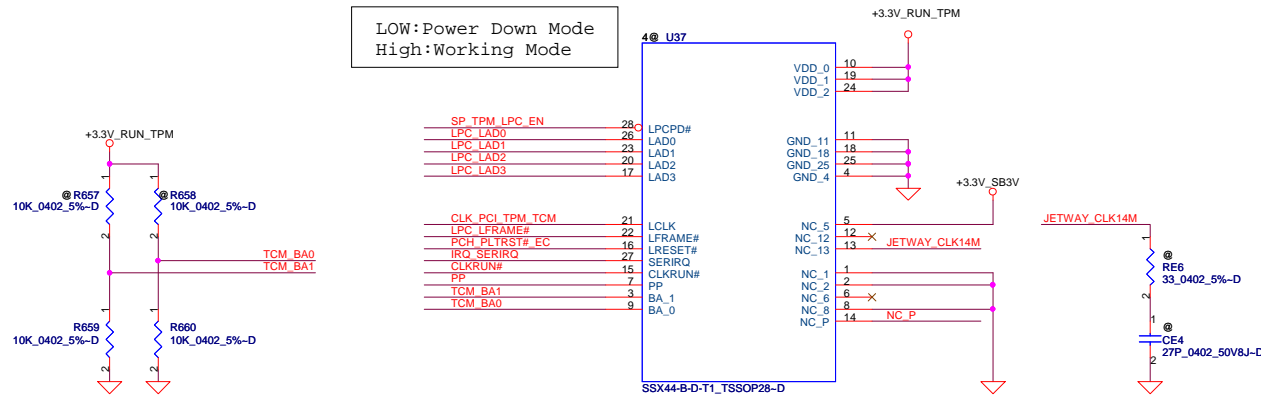


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China TCM: NationZ & Jetway co-layer

LOW:Power Down Mode
High:Working Mode



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Compal Electronics, Inc.

Title			USH conn/TPM
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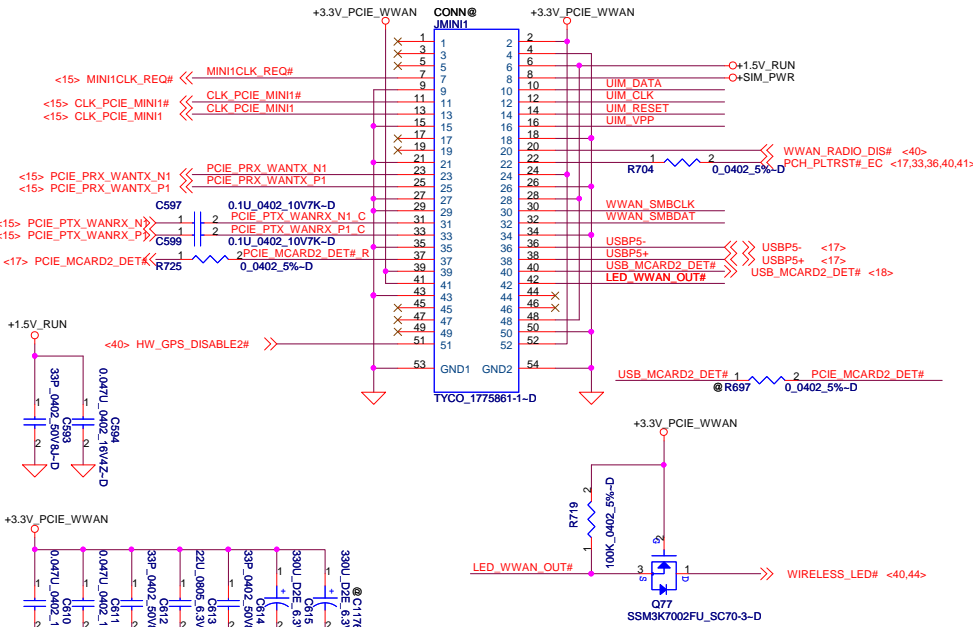
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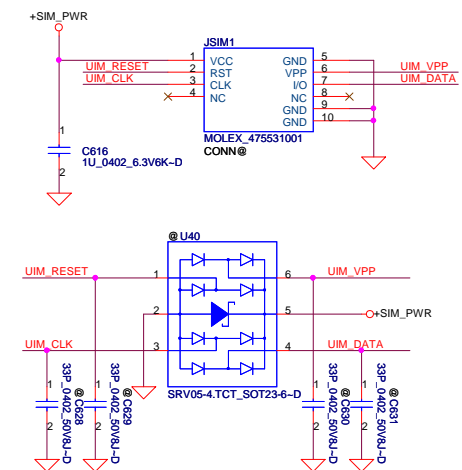
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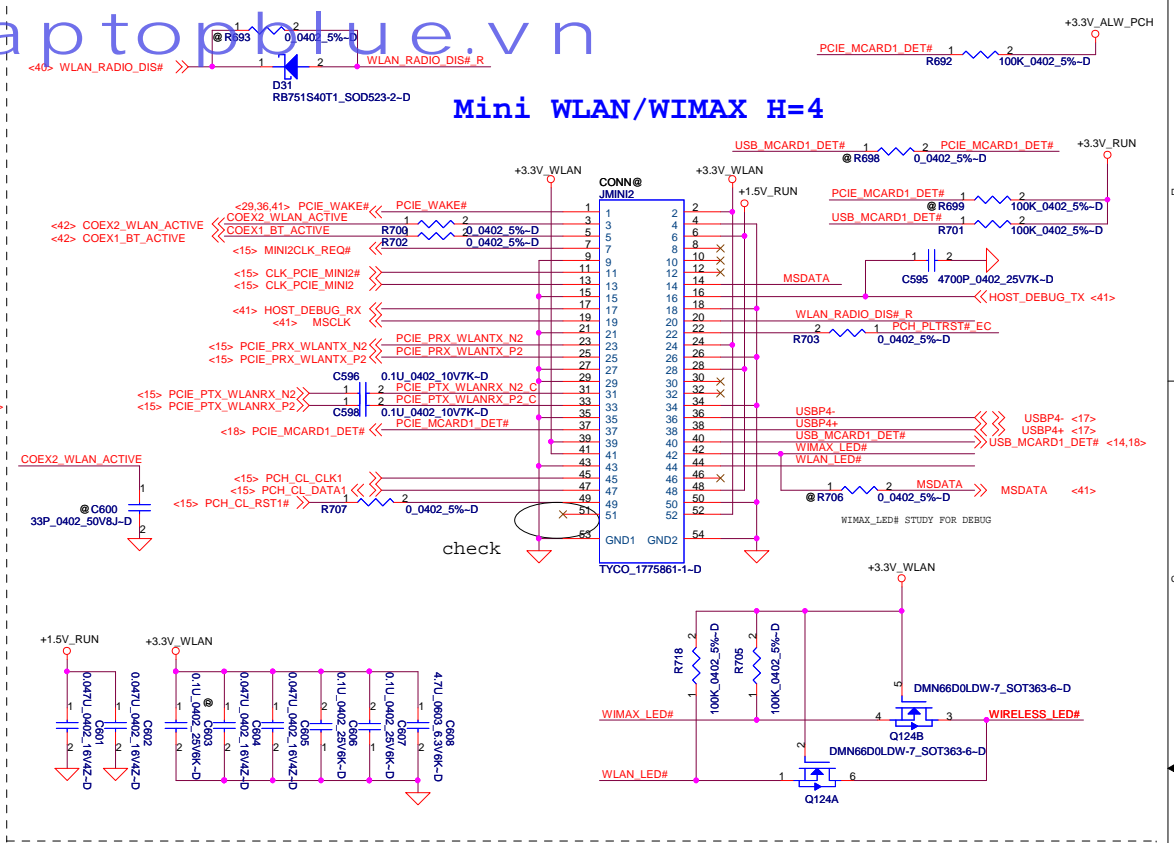
Mini WWAN/GPS/LTE H=5.2



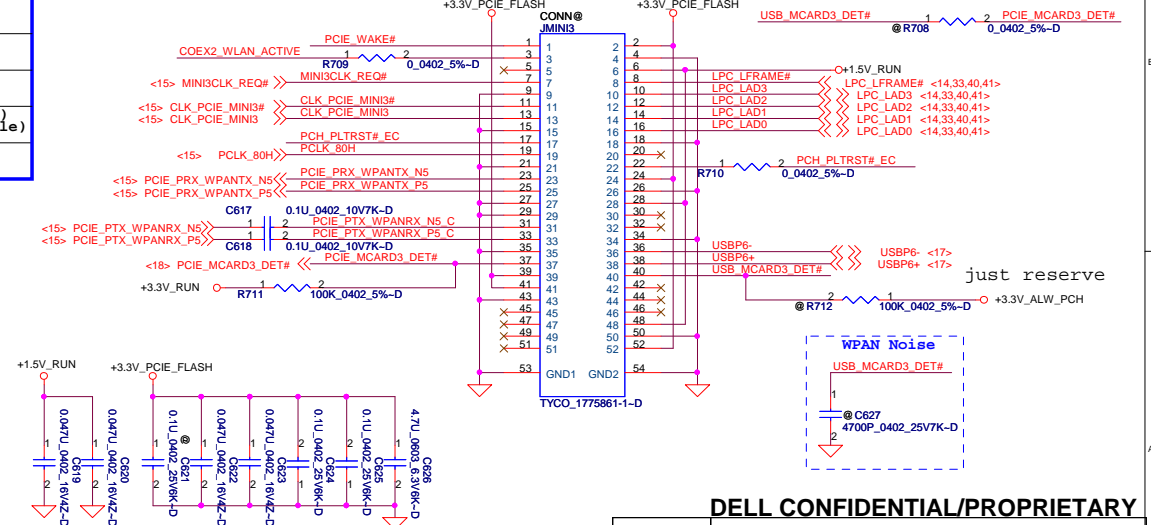
SIM Card Push-Push



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+/-9%	1000	750	
+3.3Vaux	+/-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+/-5%	500	375	NA



1/2 Minicard Pink Pather/60GHZ Card H=4



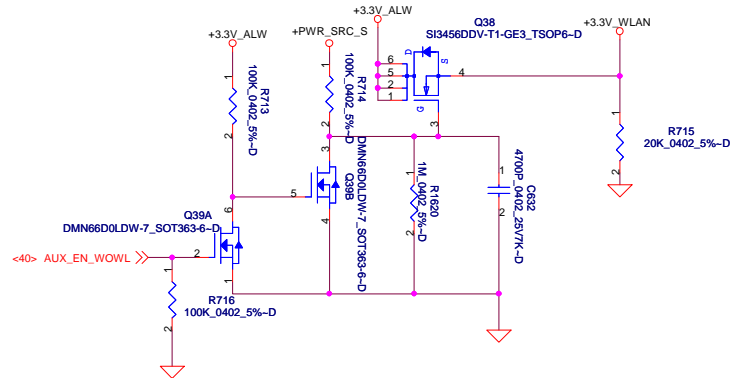
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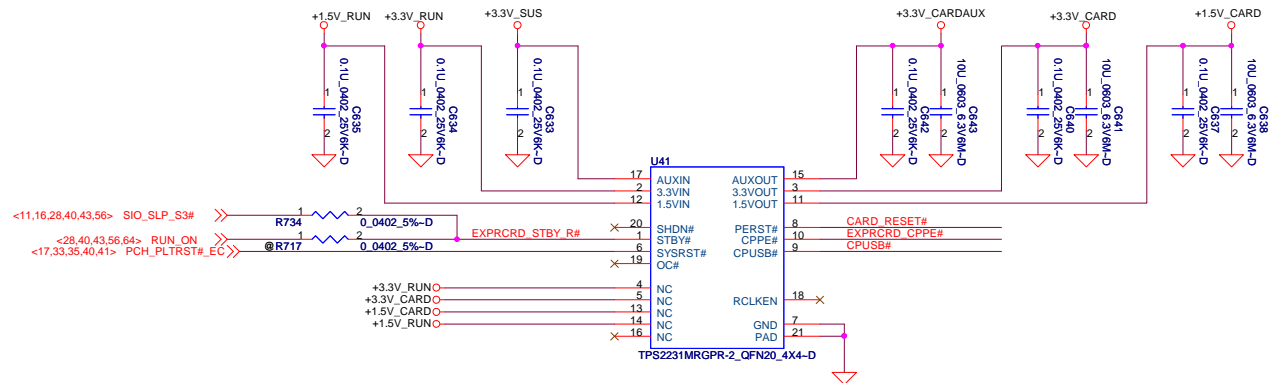
Compal Electronics, Inc.			
Mini Card			
LA-7782	Document Number	Rev	0.1
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Power Control for Mini card2

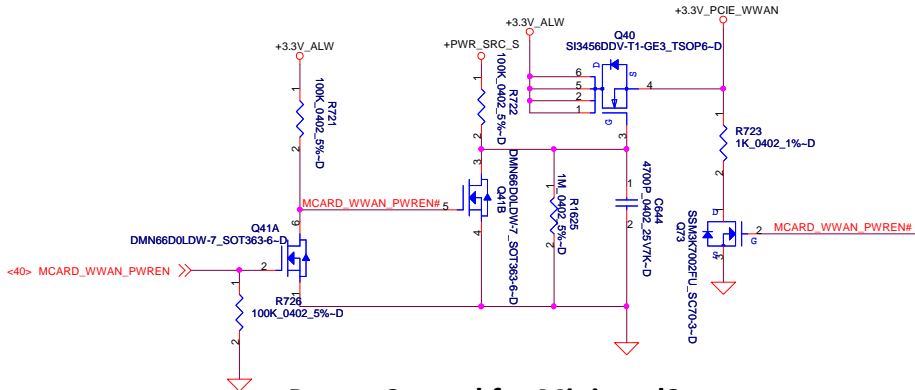


Express Card PWR S/W

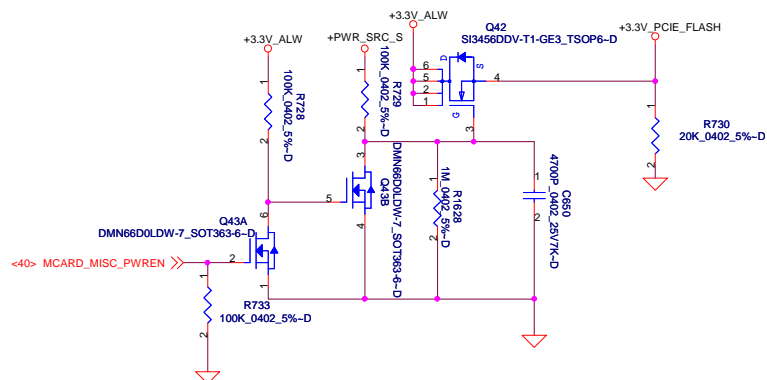


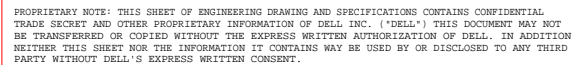
Note: Add connection on pin4, pin5, pin13 and pin14 to support GMT 2nd source part

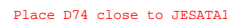
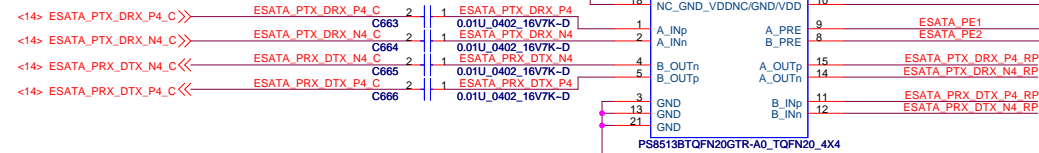
Power Control for Mini card1



Power Control for Mini card3







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Title **USB/ESATA/IO/MDC**

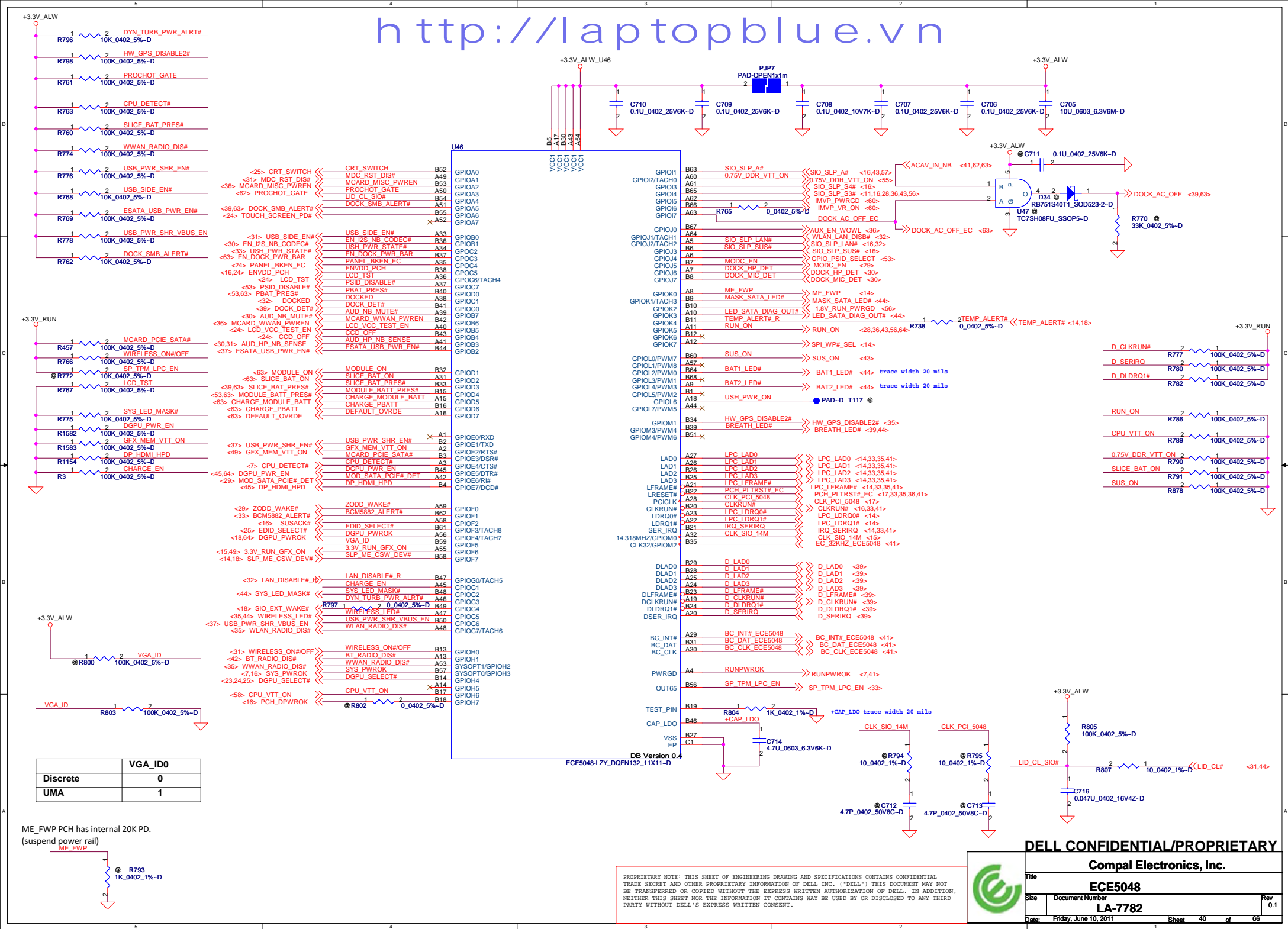
LA-7782

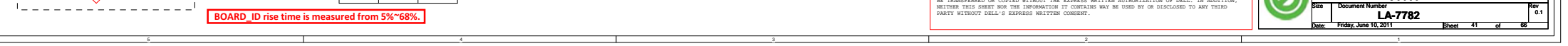
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Rev	0.1
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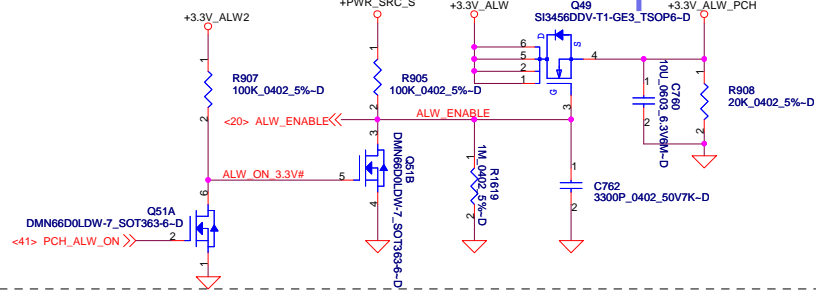
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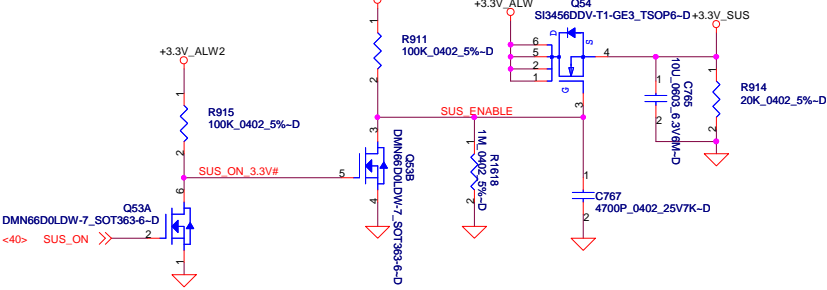




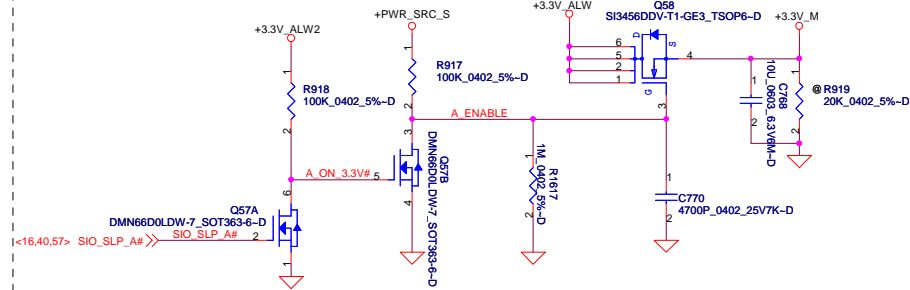
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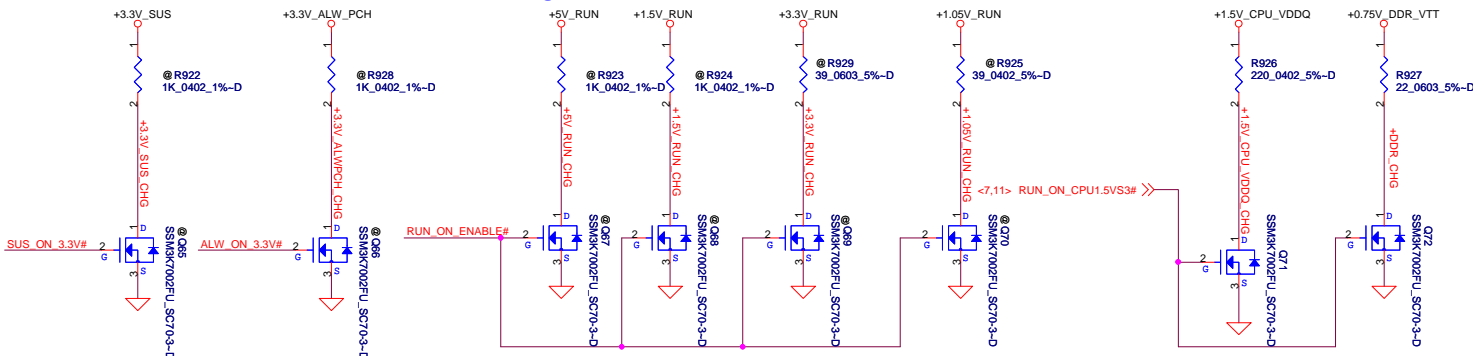
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+3.3V_M Source

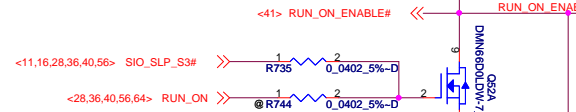


Discharge Circuit

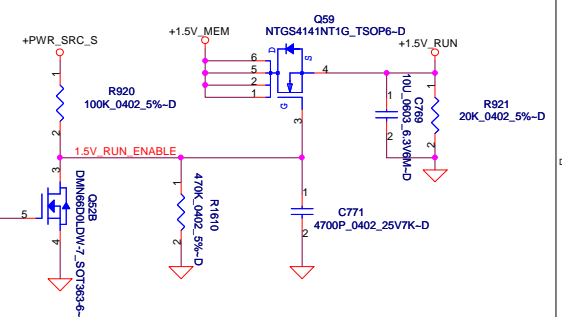


DC/DC Interface

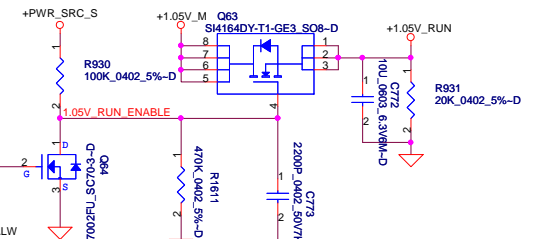
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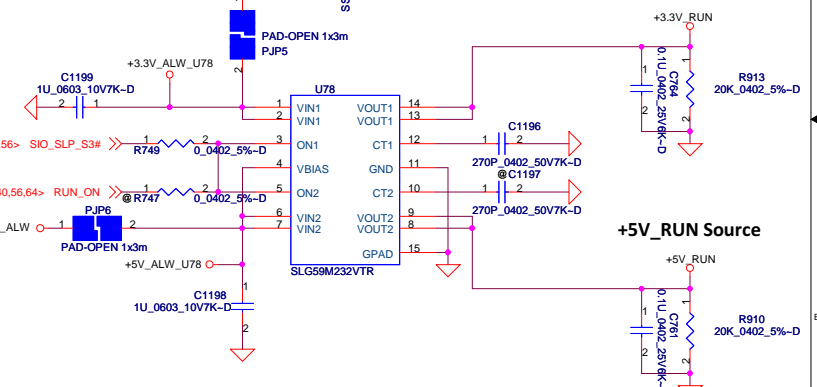
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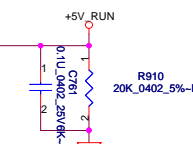
+1.05V_RUN Source



+3.3V_RUN Source



+5V_RUN Source



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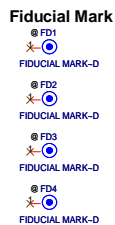
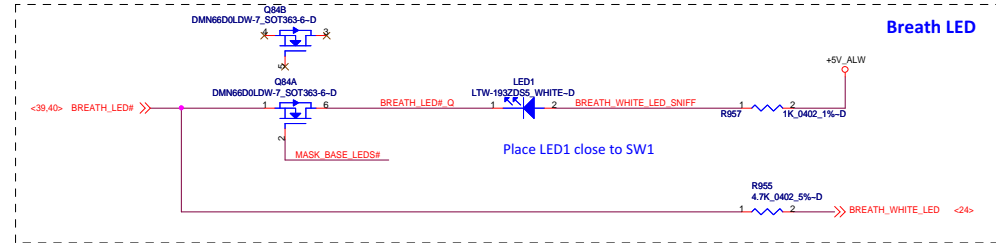
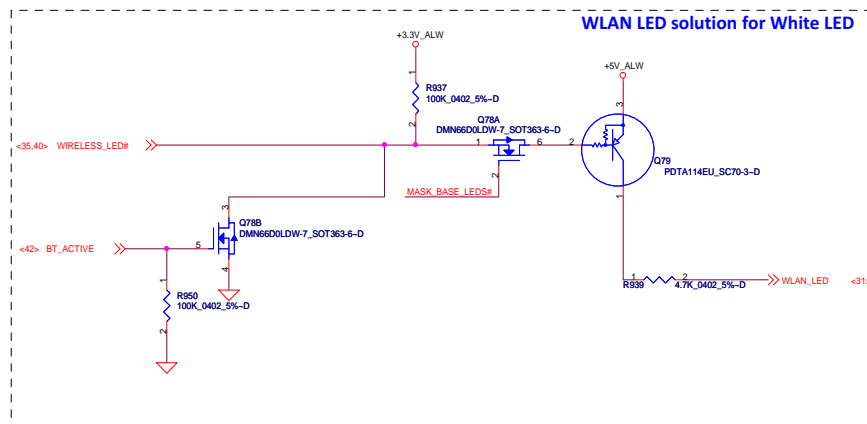
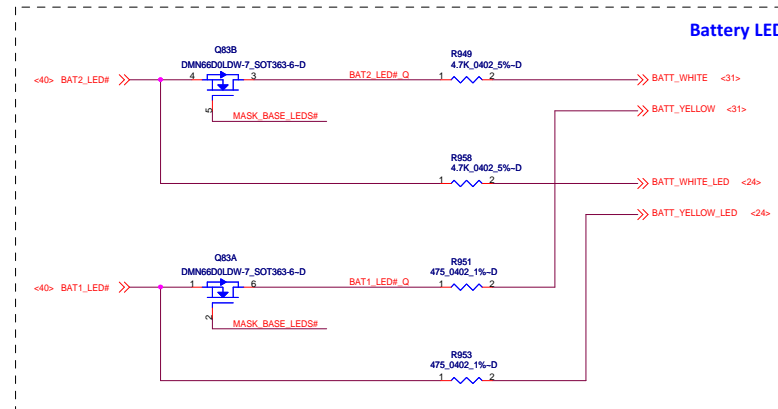
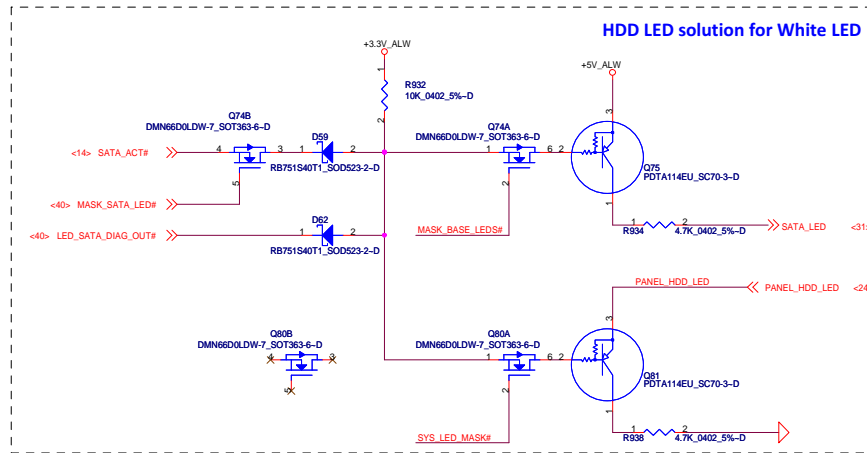
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POWER CONTROL

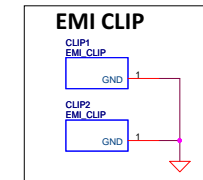
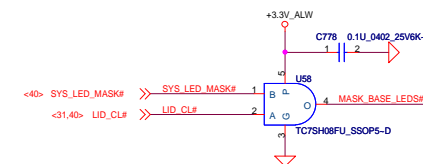
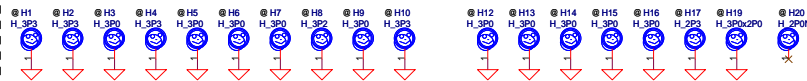
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LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



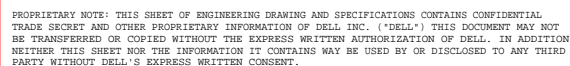
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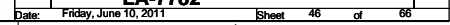
Compal Electronics, Inc.

PAD and Standoff

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Date: Friday, June 10, 2011 Sheet 44 of 66

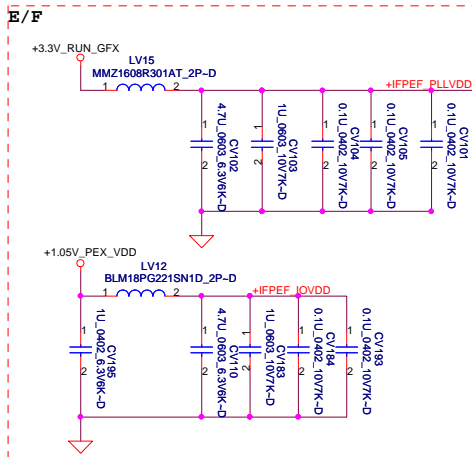
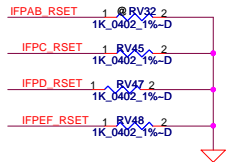
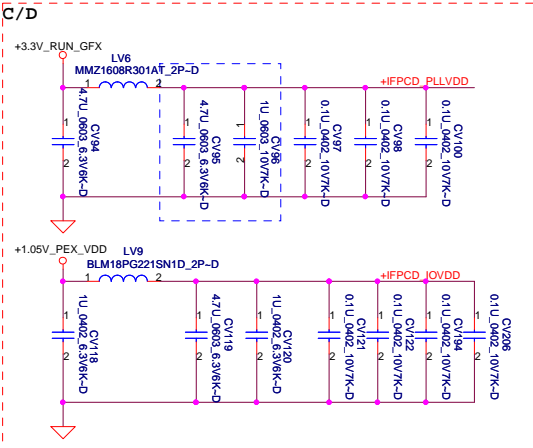
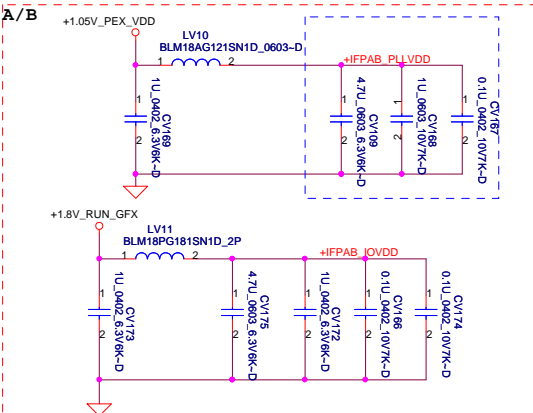
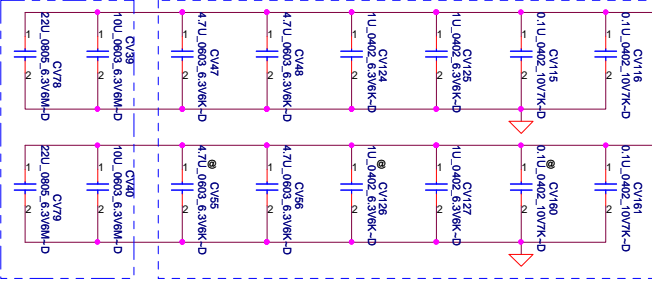
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close to the GPU

Close to Pin



POWER

PEX_IOVDDQ_0
PEX_IOVDDQ_1
PEX_IOVDDQ_2
PEX_IOVDDQ_3
PEX_IOVDDQ_4
PEX_IOVDDQ_5
PEX_IOVDDQ_6
PEX_IOVDDQ_7
PEX_IOVDDQ_8
PEX_IOVDDQ_9
PEX_IOVDDQ_10
PEX_IOVDDQ_11
PEX_IOVDDQ_12
PEX_IOVDDQ_13

PEX_IOVDD_0
PEX_IOVDD_1
PEX_IOVDD_2
PEX_IOVDD_3
PEX_IOVDD_4
PEX_IOVDD_5

PEX_PLLVDD
AG26

VDD33_0
VDD33_1
VDD33_2
VDD33_3

FB_CAL_PD_VDDQ
J27

FB_CAL_PU_GND
H27

FB_CAL_TERM_GND
H25

FB_GND_SENSE
F2

FB_VDDQ_SENSE
E1

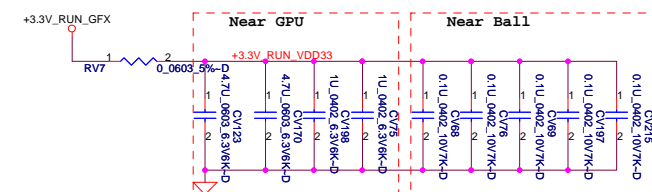
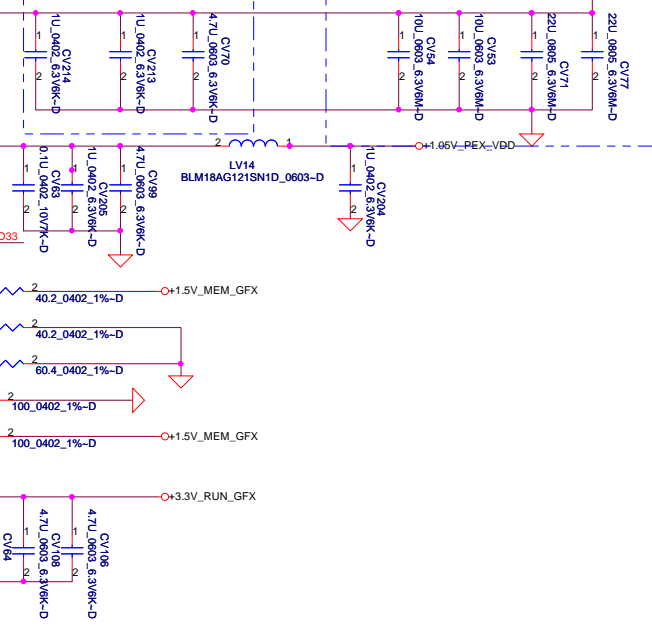
PEX_PLL_HVDD
AH12

PEX_SVDD_3V3
AG12

N13M_F0BGA908-D

PLACE UNDER BGA

PLACE NEAR GPU



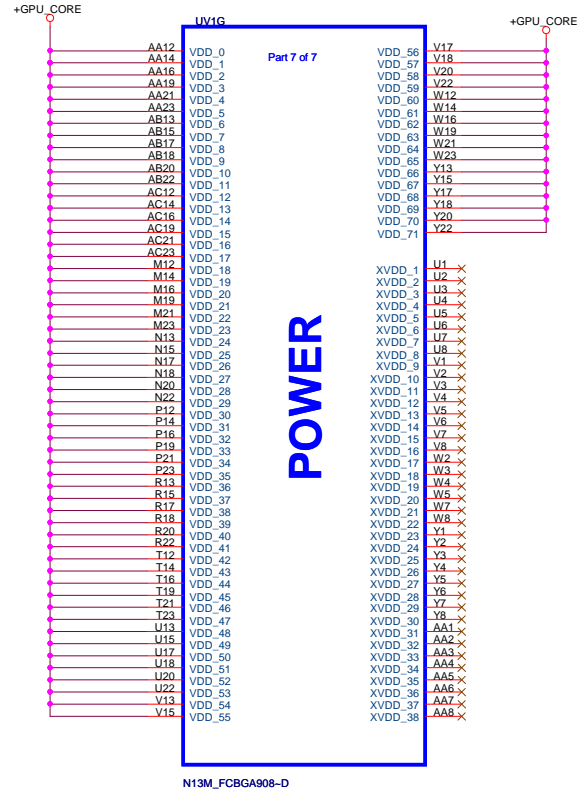
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Title		
N12P Power		
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Caps on Power Side



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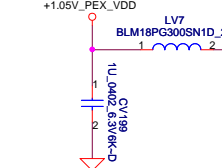
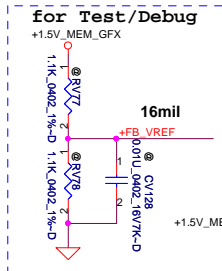
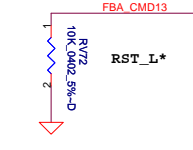
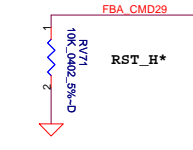
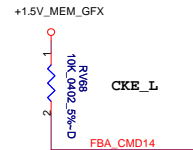
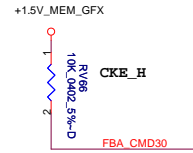


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Title		N12P Power GFX Core		Rev
Size		Document Number		0.1
Date		LA-7782		
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FBA_D[0..63] <<> FBA_D[0..63] <51..52>
FBA_CMD[0..31] <<> FBA_CMD[0..31] <51..52>
FBA_DB[0..7] <<> FBA_DB[0..7] <51..52>
FBA_EDC[0..7] <<> FBA_EDC[0..7] <51..52>



Part 2 of 7

FBA_D0	L28	FBA_D00	U30	FBA_CMD0	U30	FBA_CMD0	U30
FBA_D1	M29	FBA_D01	F31	FBA_CMD1	F31	FBA_CMD1	F31
FBA_D2	L29	FBA_D02	F32	FBA_CMD2	F32	FBA_CMD2	F32
FBA_D3	M28	FBA_D03	F33	FBA_CMD3	F33	FBA_CMD3	F33
FBA_D4	N31	FBA_D04	F34	FBA_CMD4	F34	FBA_CMD4	F34
FBA_D5	P29	FBA_D05	F35	FBA_CMD5	F35	FBA_CMD5	F35
FBA_D6	R29	FBA_D06	F36	FBA_CMD6	F36	FBA_CMD6	F36
FBA_D7	P28	FBA_D07	F37	FBA_CMD7	F37	FBA_CMD7	F37
FBA_D8	J28	FBA_D08	F38	FBA_CMD8	F38	FBA_CMD8	F38
FBA_D9	H29	FBA_D09	F39	FBA_CMD9	F39	FBA_CMD9	F39
FBA_D10	J29	FBA_D10	F40	FBA_CMD10	F40	FBA_CMD10	F40
FBA_D11	H28	FBA_D11	F41	FBA_CMD11	F41	FBA_CMD11	F41
FBA_D12	G29	FBA_D12	F42	FBA_CMD12	F42	FBA_CMD12	F42
FBA_D13	E31	FBA_D13	F43	FBA_CMD13	F43	FBA_CMD13	F43
FBA_D14	E32	FBA_D14	F44	FBA_CMD14	F44	FBA_CMD14	F44
FBA_D15	F30	FBA_D15	F45	FBA_CMD15	F45	FBA_CMD15	F45
FBA_D16	C34	FBA_D16	F46	FBA_CMD16	F46	FBA_CMD16	F46
FBA_D17	D32	FBA_D17	F47	FBA_CMD17	F47	FBA_CMD17	F47
FBA_D18	C33	FBA_D18	F48	FBA_CMD18	F48	FBA_CMD18	F48
FBA_D19	C33	FBA_D19	F49	FBA_CMD19	F49	FBA_CMD19	F49
FBA_D20	F33	FBA_D20	F50	FBA_CMD20	F50	FBA_CMD20	F50
FBA_D21	F32	FBA_D21	F51	FBA_CMD21	F51	FBA_CMD21	F51
FBA_D22	H32	FBA_D22	F52	FBA_CMD22	F52	FBA_CMD22	F52
FBA_D23	H32	FBA_D23	F53	FBA_CMD23	F53	FBA_CMD23	F53
FBA_D24	P34	FBA_D24	F54	FBA_CMD24	F54	FBA_CMD24	F54
FBA_D25	P32	FBA_D25	F55	FBA_CMD25	F55	FBA_CMD25	F55
FBA_D26	P31	FBA_D26	F56	FBA_CMD26	F56	FBA_CMD26	F56
FBA_D27	P33	FBA_D27	F57	FBA_CMD27	F57	FBA_CMD27	F57
FBA_D28	L31	FBA_D28	F58	FBA_CMD28	F58	FBA_CMD28	F58
FBA_D29	L34	FBA_D29	F59	FBA_CMD29	F59	FBA_CMD29	F59
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FBA_D32	AG28	FBA_D32	F62	FBA_CMD32	F62	FBA_CMD32	F62
FBA_D33	AF29	FBA_D33	F63	FBA_CMD33	F63	FBA_CMD33	F63
FBA_D34	AG29	FBA_D34	F64	FBA_CMD34	F64	FBA_CMD34	F64
FBA_D35	AF28	FBA_D35	F65	FBA_CMD35	F65	FBA_CMD35	F65
FBA_D36	AD30	FBA_D36	F66	FBA_CMD36	F66	FBA_CMD36	F66
FBA_D37	AD29	FBA_D37	F67	FBA_CMD37	F67	FBA_CMD37	F67
FBA_D38	AC29	FBA_D38	F68	FBA_CMD38	F68	FBA_CMD38	F68
FBA_D39	AD28	FBA_D39	F69	FBA_CMD39	F69	FBA_CMD39	F69
FBA_D40	AJ29	FBA_D40	F70	FBA_CMD40	F70	FBA_CMD40	F70
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FBA_D44	AM29	FBA_D44	F74	FBA_CMD44	F74	FBA_CMD44	F74
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FBA_D57	AD32	FBA_D57	F87	FBA_CMD57	F87	FBA_CMD57	F87
FBA_D58	AC30	FBA_D58	F88	FBA_CMD58	F88	FBA_CMD58	F88
FBA_D59	AD33	FBA_D59	F89	FBA_CMD59	F89	FBA_CMD59	F89
FBA_D60	AF31	FBA_D60	F90	FBA_CMD60	F90	FBA_CMD60	F90
FBA_D61	AG34	FBA_D61	F91	FBA_CMD61	F91	FBA_CMD61	F91
FBA_D62	AG32	FBA_D62	F92	FBA_CMD62	F92	FBA_CMD62	F92
FBA_D63	AG33	FBA_D63	F93	FBA_CMD63	F93	FBA_CMD63	F93

MEMORY INTERFACE

A

N13M_FCBGA908-D

FBA_CLK0

FBA_CLK0_N

FBA_CLK1

FBA_CLK1_N

FBA_WCK01

FBA_WCK01_N

FBA_WCK02

FBA_WCK02_N

FBA_WCK03

FBA_WCK03_N

FBA_WCK04

FBA_WCK04_N

FBA_WCK05

FBA_WCK05_N

FBA_WCK06

FBA_WCK06_N

FBA_WCK07

FBA_WCK07_N

FBA_WCK08

FBA_WCK08_N

FBA_WCK09

FBA_WCK09_N

FBA_WCK10

FBA_WCK10_N

FBA_WCK11

FBA_WCK11_N

FBA_WCK12

FBA_WCK12_N

FBA_WCK13

FBA_WCK13_N

FBA_WCK14

FBA_WCK14_N

FBA_WCK15

FBA_WCK15_N

FBA_WCK16

FBA_WCK16_N

FBA_WCK17

FBA_WCK17_N

FBA_WCK18

FBA_WCK18_N

FBA_WCK19

FBA_WCK19_N

FBA_WCK20

FBA_WCK20_N

FBA_WCK21

FBA_WCK21_N

FBA_WCK22

FBA_WCK22_N

FBA_WCK23

FBA_WCK23_N

FBA_WCK24

FBA_WCK24_N

FBA_WCK25

FBA_WCK25_N

FBA_WCK26

FBA_WCK26_N

FBA_WCK27

FBA_WCK27_N

FBA_WCK28

FBA_WCK28_N

FBA_WCK29

FBA_WCK29_N

FBA_WCK30

FBA_WCK30_N

FBA_WCK31

FBA_WCK31_N

FBA_WCK32

FBA_WCK32_N

FBA_WCK33

FBA_WCK33_N

FBA_WCK34

FBA_WCK34_N

FBA_WCK35

FBA_WCK35_N

FBA_WCK36

FBA_WCK36_N

FBA_WCK37

FBA_WCK37_N

FBA_WCK38

FBA_WCK38_N

FBA_WCK39

FBA_WCK39_N

FBA_WCK40

FBA_WCK40_N

FBA_WCK41

FBA_WCK41_N

FBA_WCK42

FBA_WCK42_N

FBA_WCK43

FBA_WCK43_N

FBA_WCK44

FBA_WCK44_N

FBA_WCK45

FBA_WCK45_N

FBA_WCK46

FBA_WCK46_N

FBA_WCK47

FBA_WCK47_N

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FBA_WCK48_N

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FBA_WCK50

FBA_WCK50_N

FBA_WCK51

FBA_WCK51_N

FBA_WCK52

FBA_WCK52_N

FBA_WCK53

FBA_WCK53_N

FBA_WCK54

FBA_WCK54_N

FBA_WCK55

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FBA_WCK56

FBA_WCK56_N

FBA_WCK57

FBA_WCK57_N

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FBA_WCK68_N

FBA_WCK69

FBA_WCK69_N

FBA_WCK70

FBA_WCK70_N

FBA_WCK71

FBA_WCK71_N

FBA_WCK72

FBA_WCK72_N

FBA_WCK73

FBA_WCK73_N

FBA_WCK74

FBA_WCK74_N

FBA_WCK75

FBA_WCK75_N

FBA_WCK76

FBA_WCK76_N

FBA_WCK77

FBA_WCK77_N

FBA_WCK78

FBA_WCK78_N

FBA_WCK79

FBA_WCK79_N

FBA_WCK80

FBA_WCK80_N

FBA_WCK81

FBA_WCK81_N

FBA_WCK82

FBA_WCK82_N

FBA_WCK83

FBA_WCK83_N

FBA_WCK84

FBA_WCK84_N

FBA_WCK85

FBA_WCK85_N

FBA_WCK86

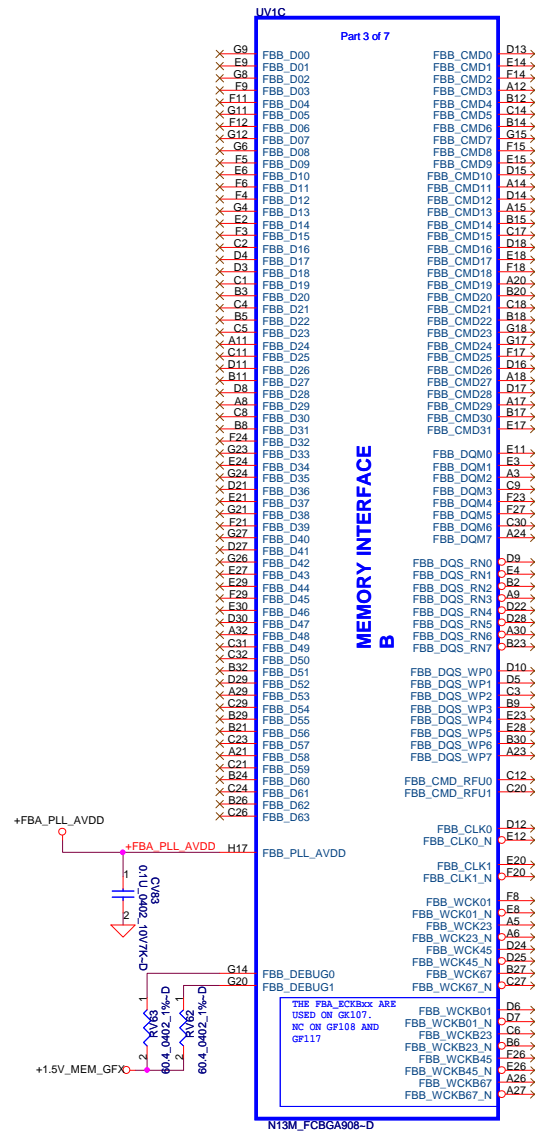
FBA_WCK86_N

FBA_WCK87

FBA_WCK87_N

FBA_WCK88

CHANNEL-B NOT TO USE, NEED TO BE DISABLED



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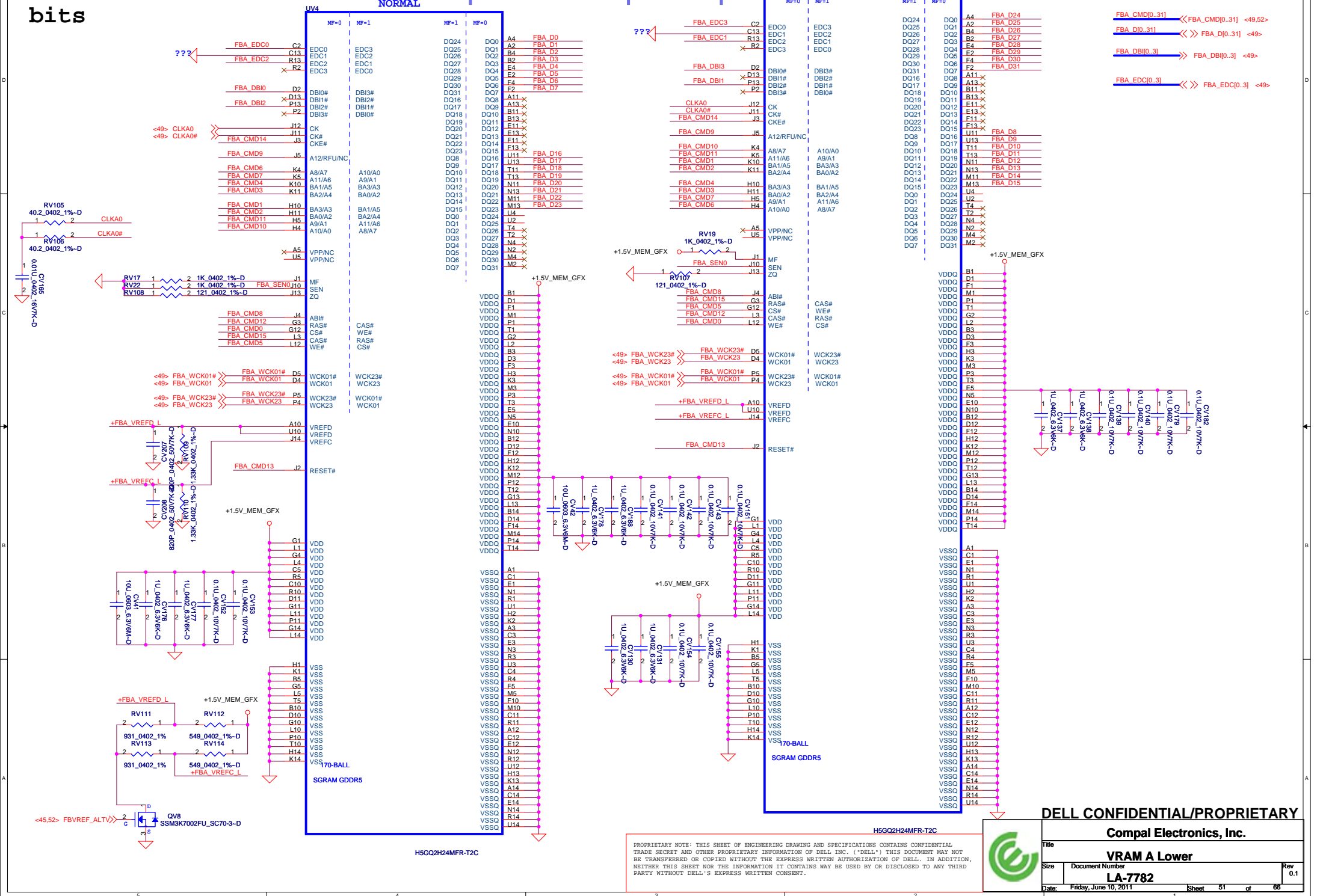
Compal Electronics, Inc.

Title		
N12P Memory (2)		
Size	Document Number	Rev
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Date:	Friday, May 20, 2011	Sheet 50 of 66

Memory Partition A - Lower 32 bits

64X32 GDDR5

MIRRO



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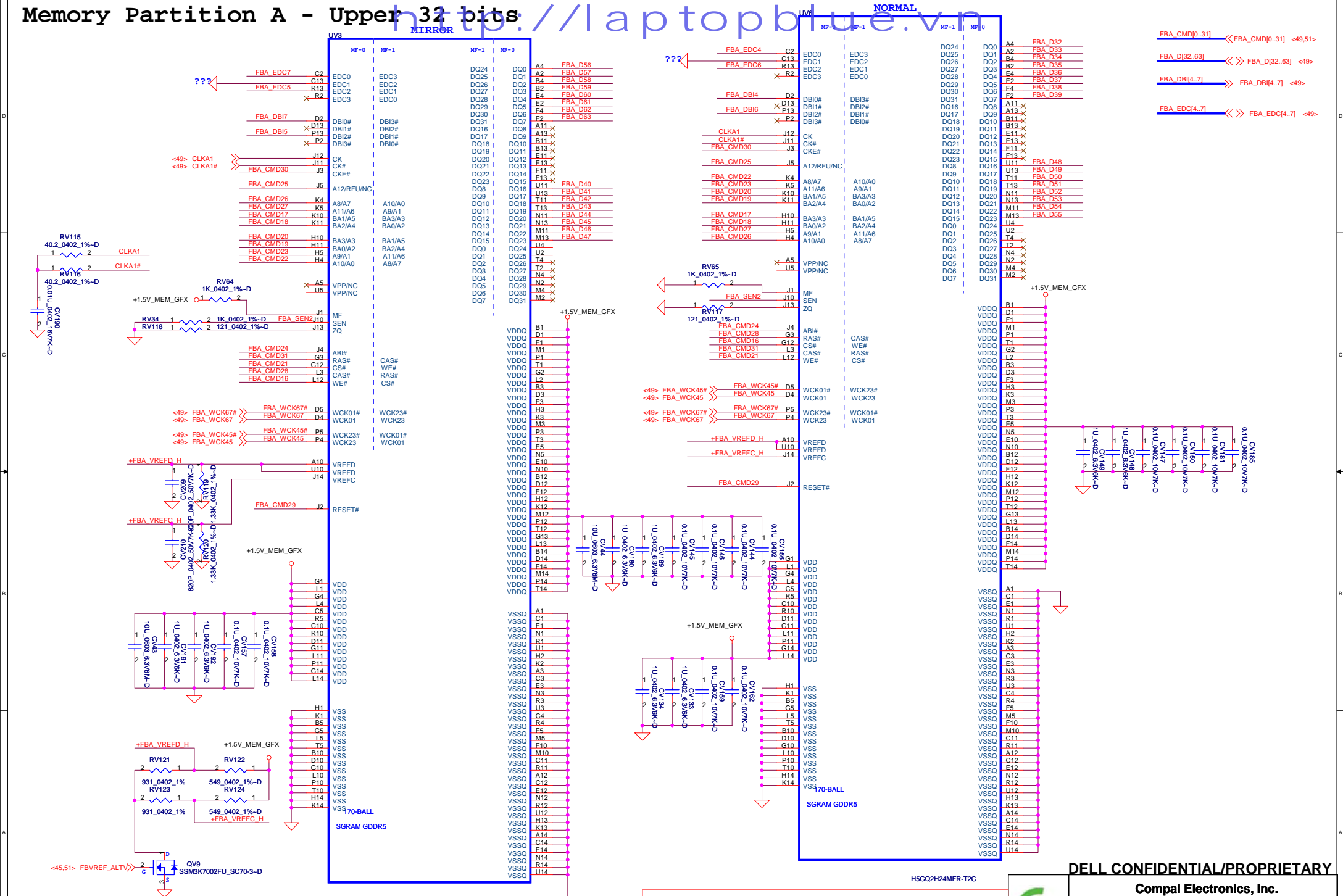
Compal Electronics, Inc.

Title	VRAM A Lower
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Size	Document Number
	LA-7782

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Memory Partition A - Upper 32 bits



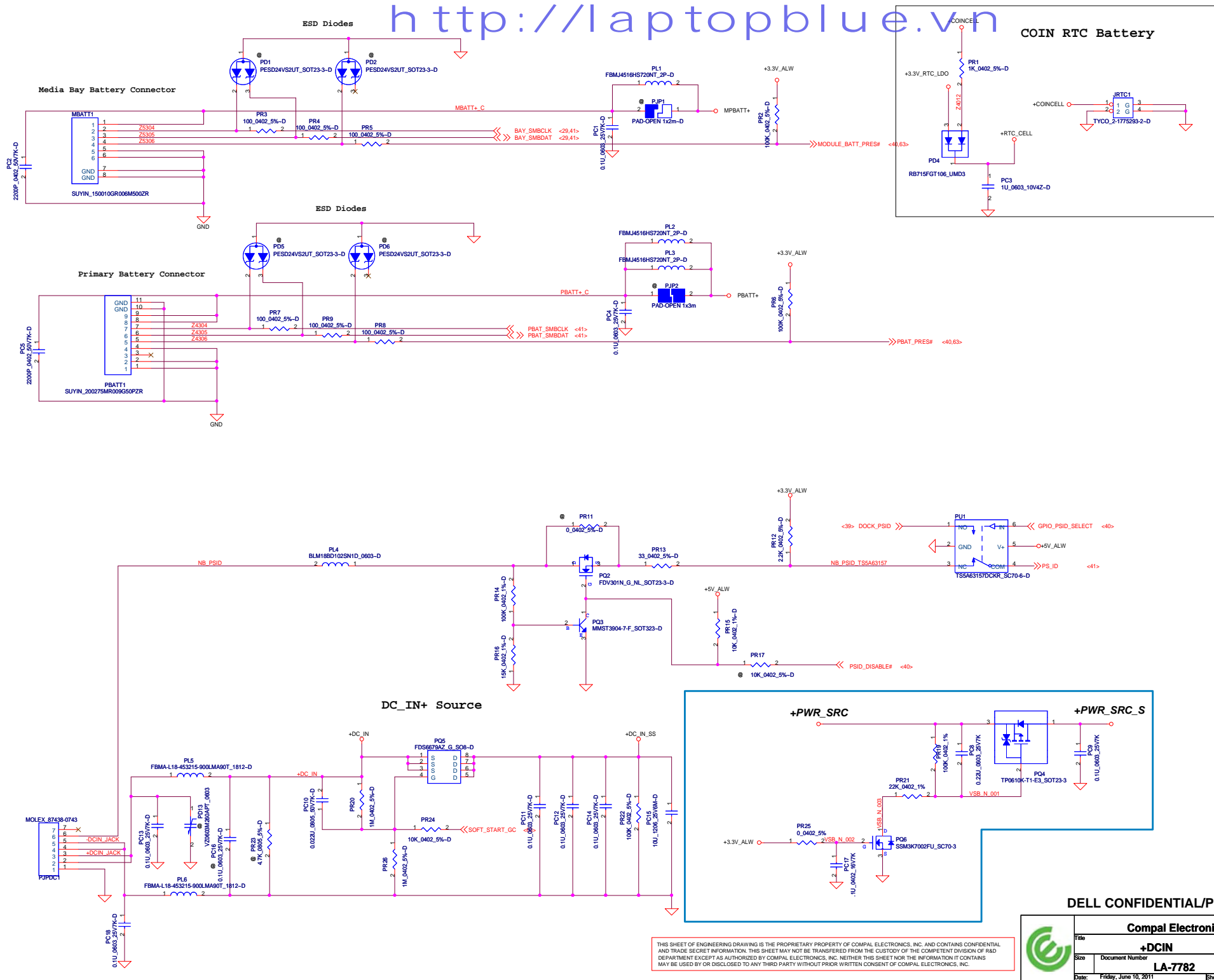
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Compal Electronics, Inc.


Title		
VRAM A Upper		
Size	Document Number	Rev

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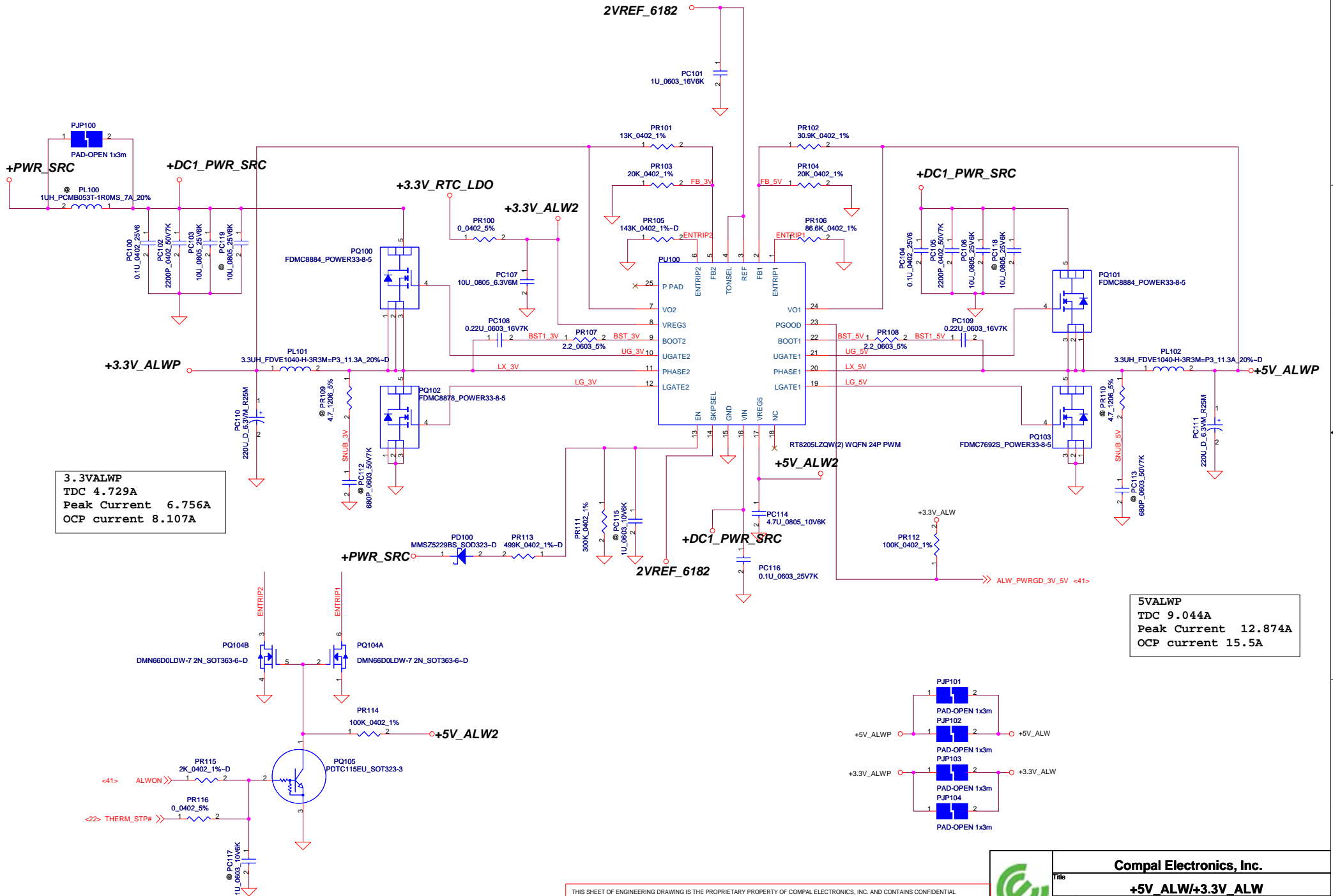
Date: Friday, June 10, 2011 Sheet 32 of 50



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		+DCIN	
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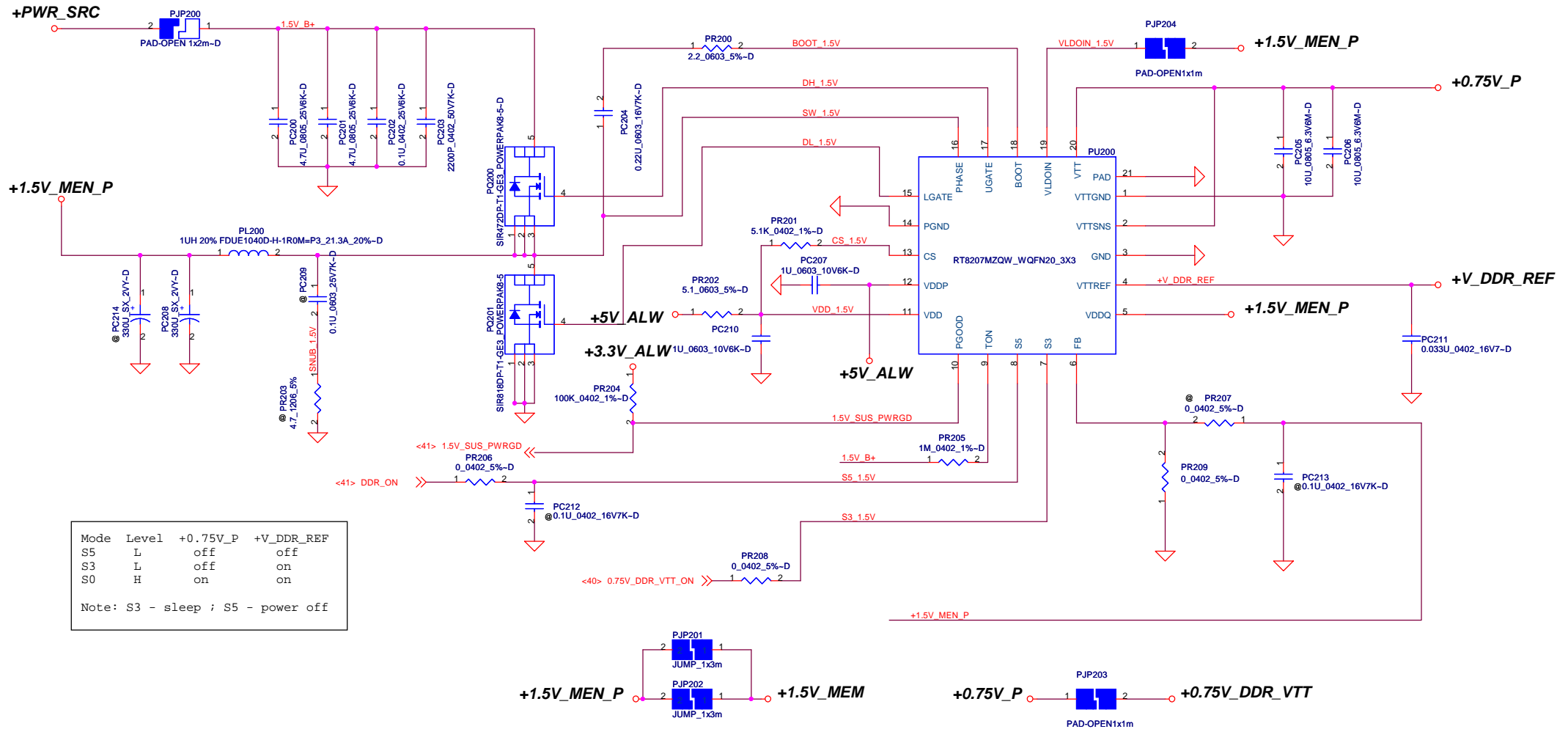
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Compal Electronics, Inc.			
Title	+5V_ALW/+3.3V_ALW		
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1.5Volt +/- 5%
TDC 9.74A
Peak Current 13.915A
OCP current 16.698A

0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A



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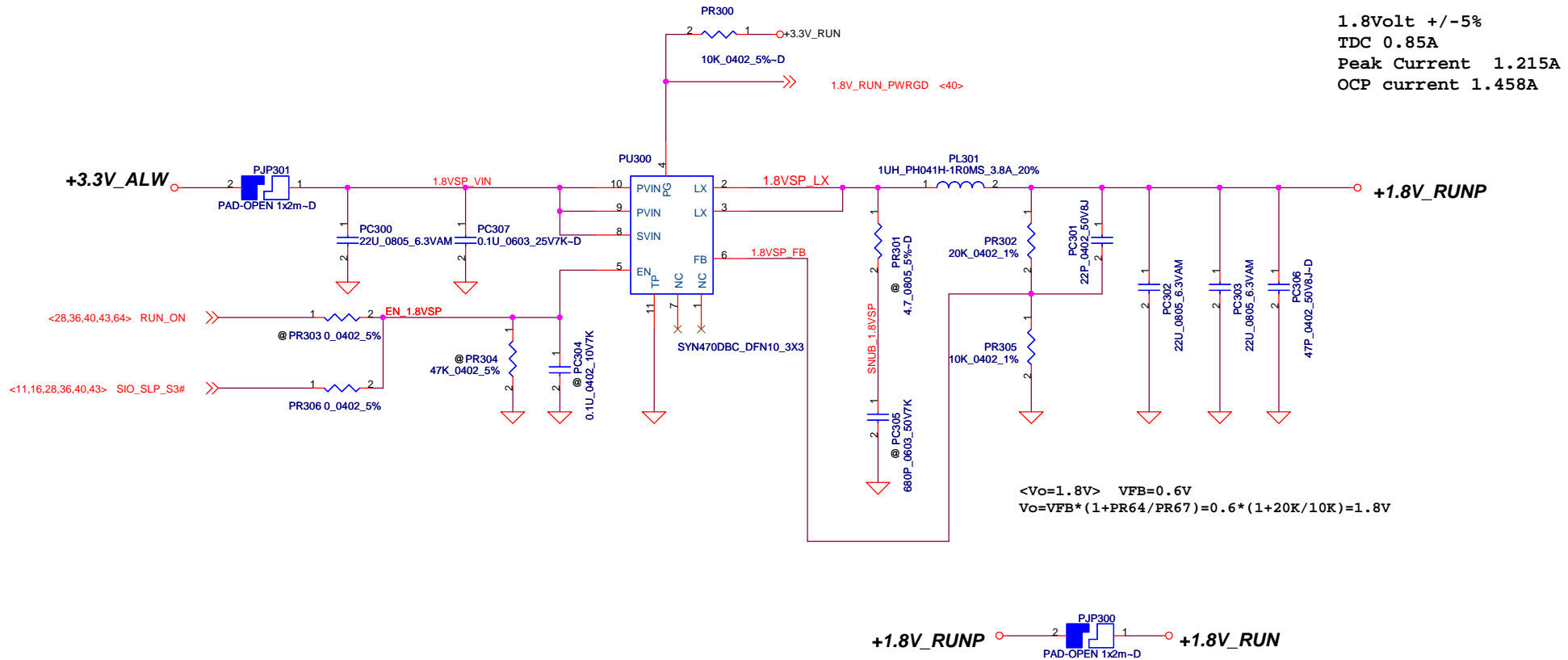
+1.5V_MEN/+0.75V_DDR_VTT

Title
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Rev 0.1

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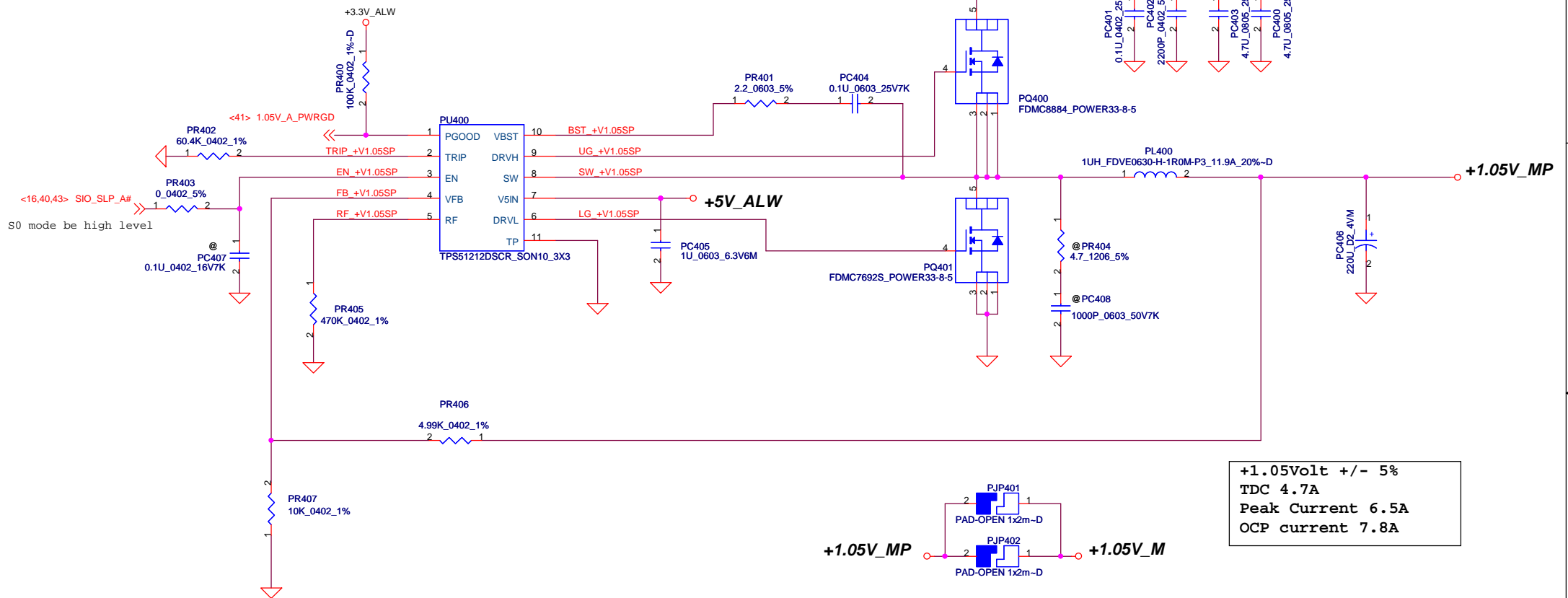
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Compal Electronics, Inc.			
Title	+1.8V_RUN		
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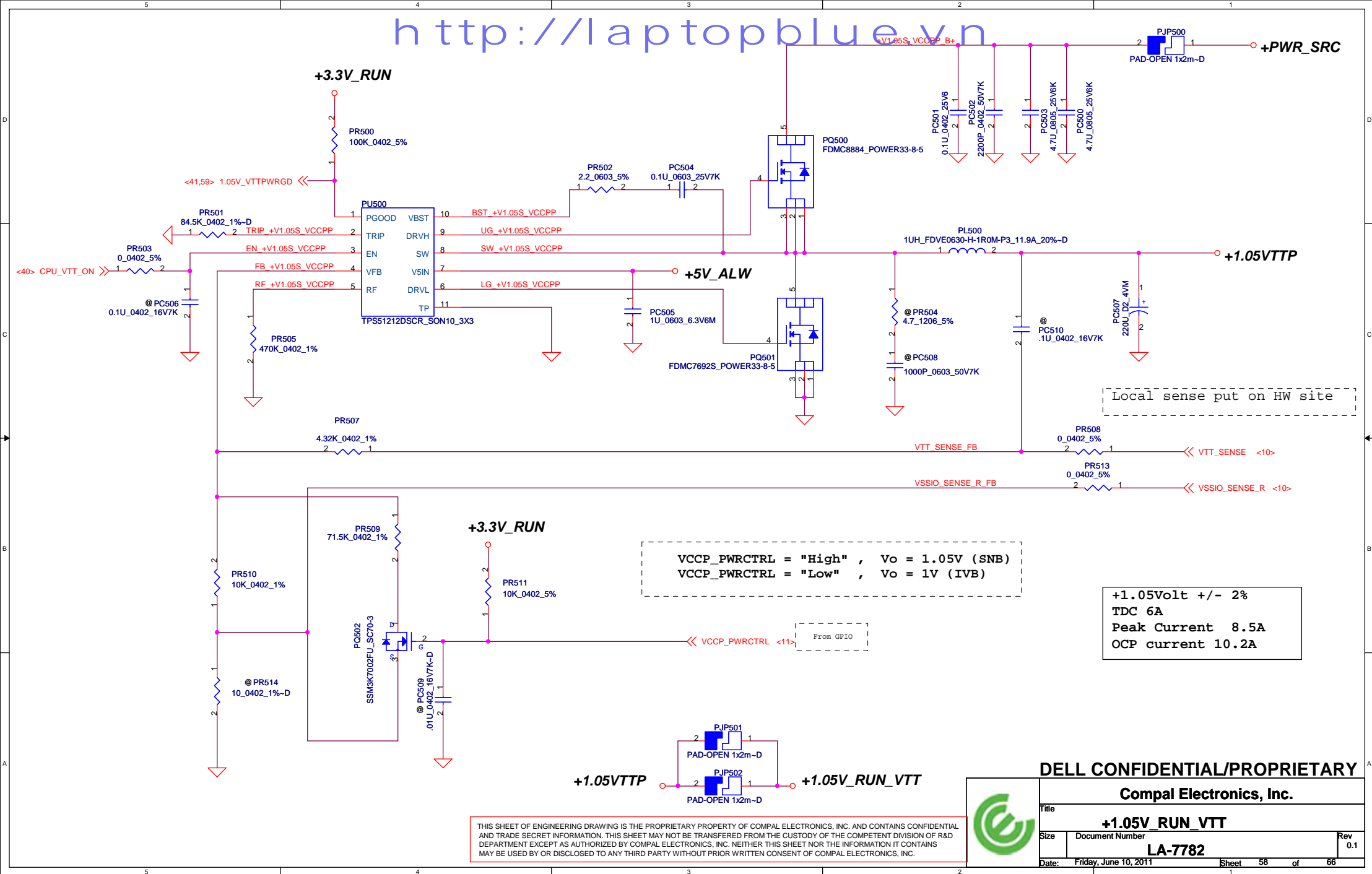
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Compal Electronics, Inc.

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+1.05V_M			
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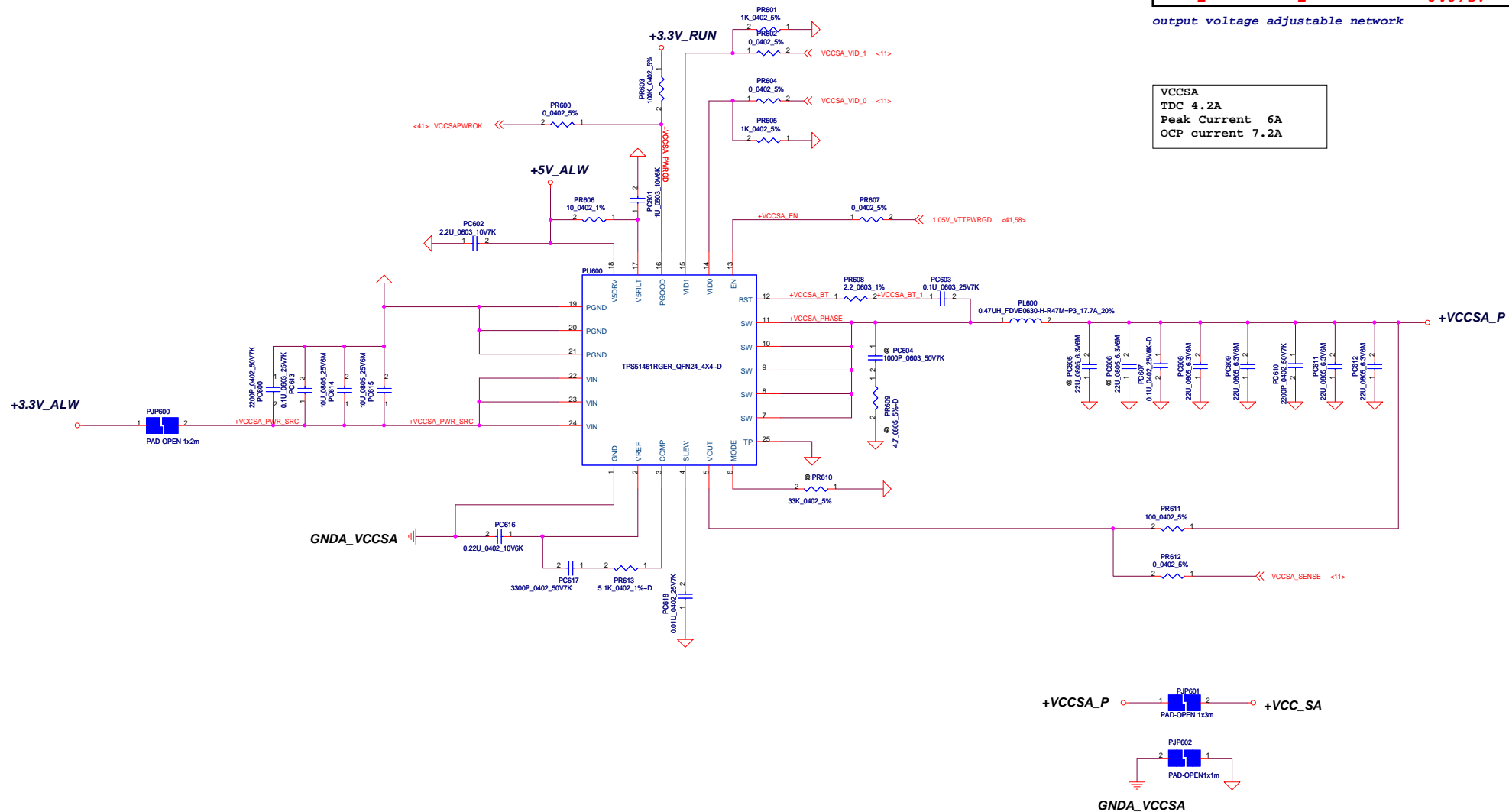


The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

VCCSA
TDC 4.2A
Peak Current 6A
OCP current 7.2A



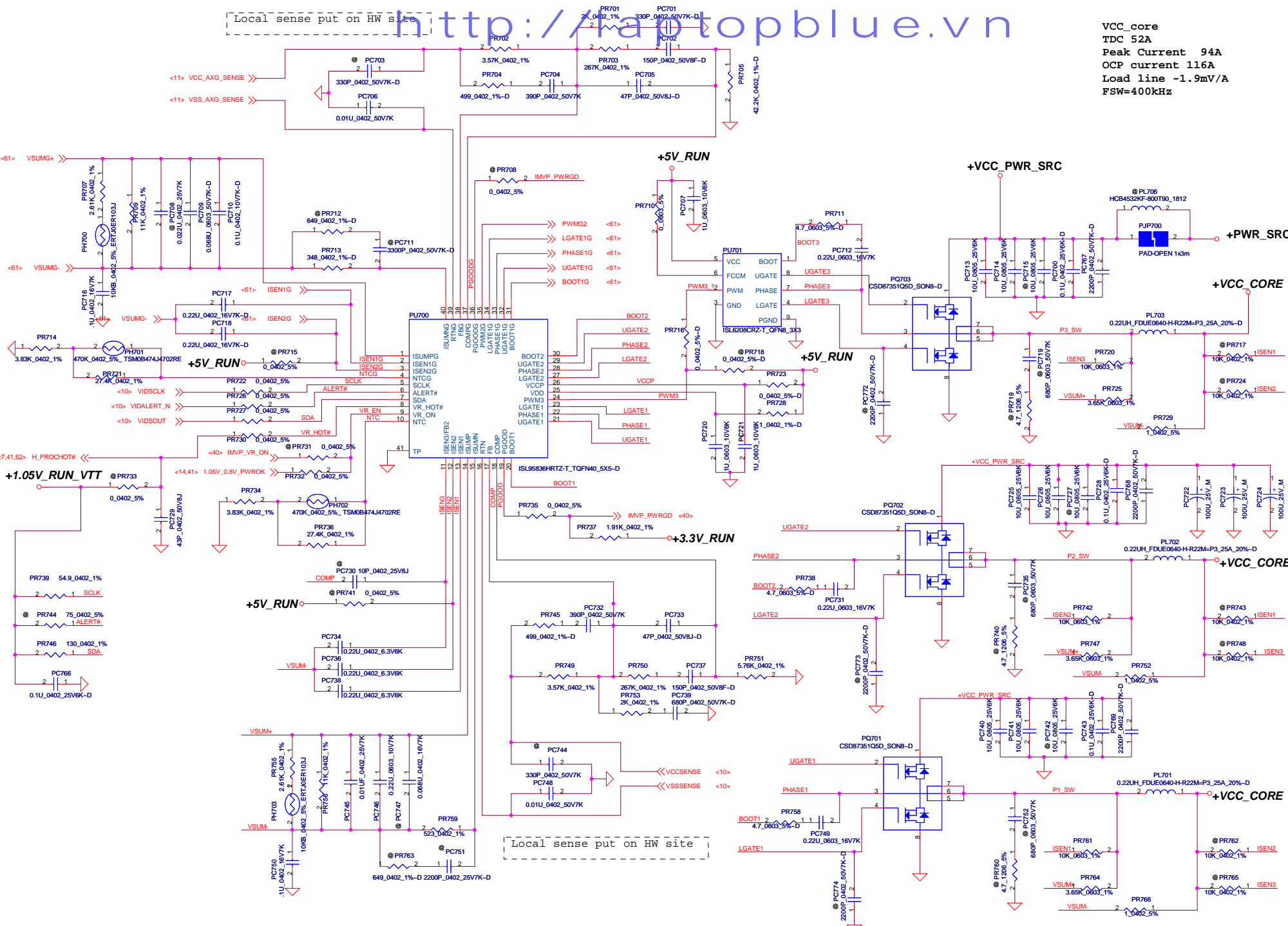
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+VCC SA		Size	
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http://laptopblue.vn

VCC_core
TDC 52A
Peak Current 94A
OCP current 116A
Load line -1.9mV/A
FSW=400kHz



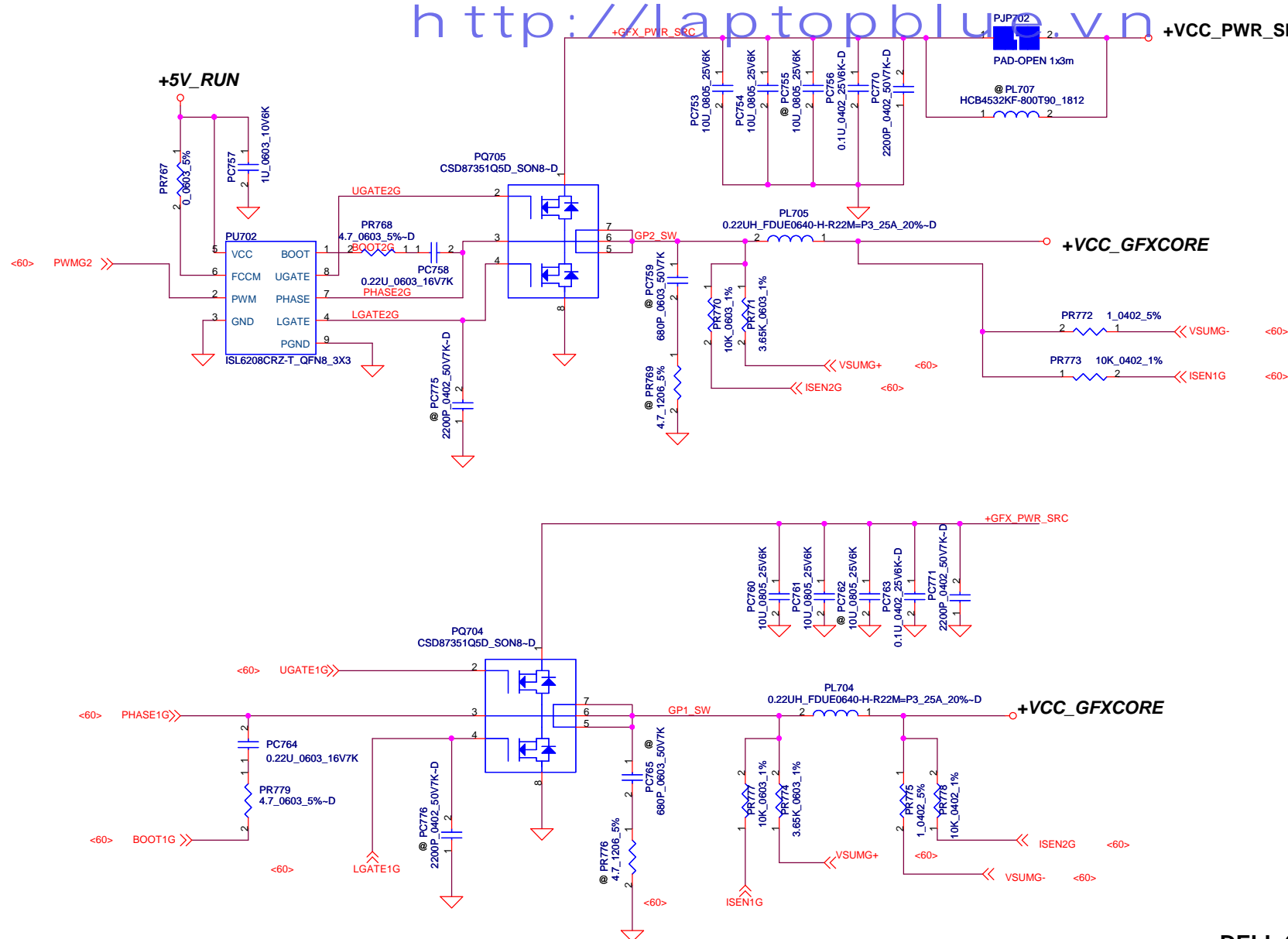
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Compal Electronics, Inc.			
+VCC_CORE			
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VCC_GFXCORE
TDC 38A
Peak Current 46A
OCP current 57.18A
Load line -3.9mV/A
FSW=400kHz



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Title			
+VCC_GFXCORE			
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E2 AC_OK=17.7 Volt

PR1313
TI bq24745 = 316K
Intersil ISL88731 = 226K
Maxim = 383K

Vref
TI bq24747 = 3.3V
Intersil ISL88731C = 3.2V
VDDP
TI bq24747 = 6V
Intersil ISL88731C = 5.1V

Maximum charging current is 7.2A

	DYN_TUR_CURRENT_SET#
90W	High
130W	Low

Adapter Protection Circuit for Turbo Mode

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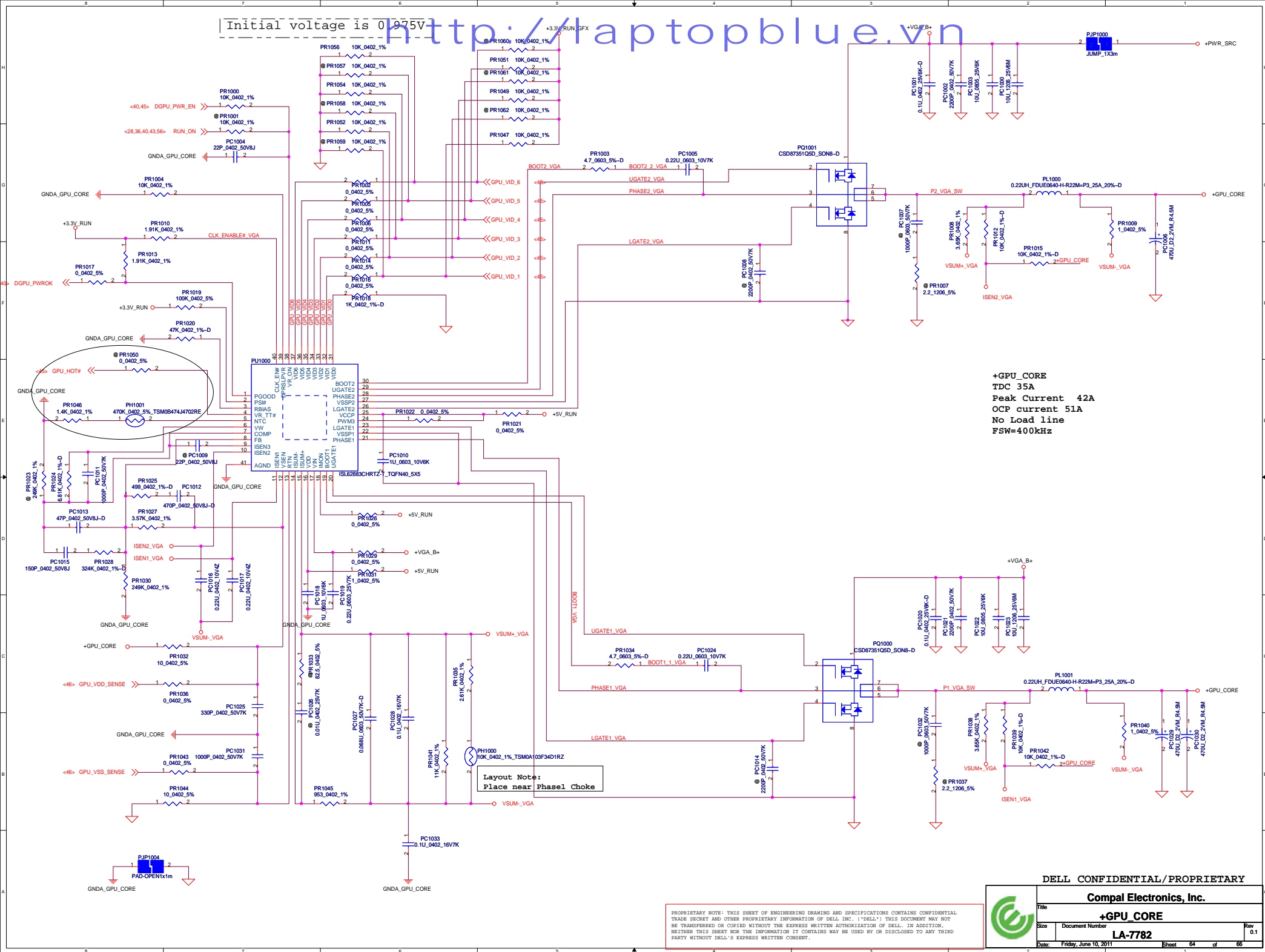
Title		Charger
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Initial voltage is 0.975V

http://laptopblue.vn



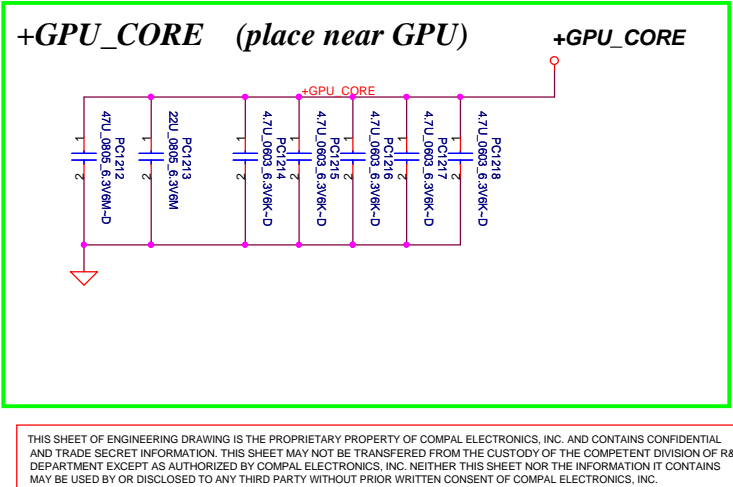
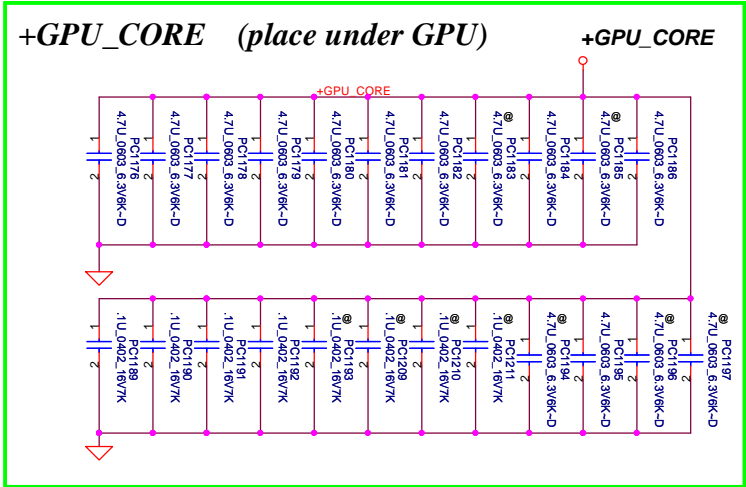
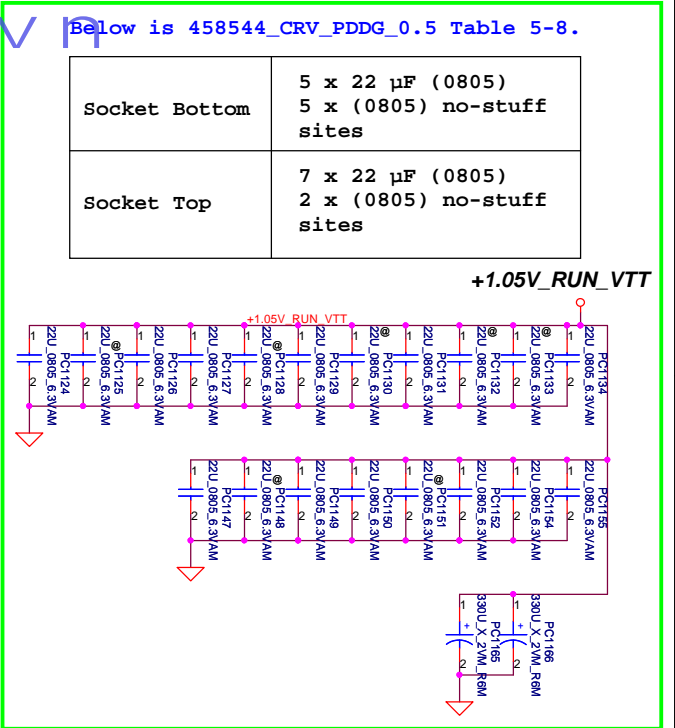
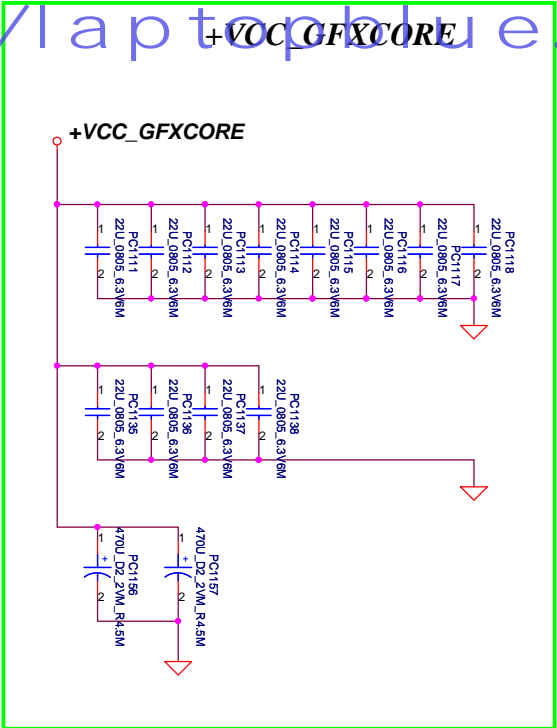
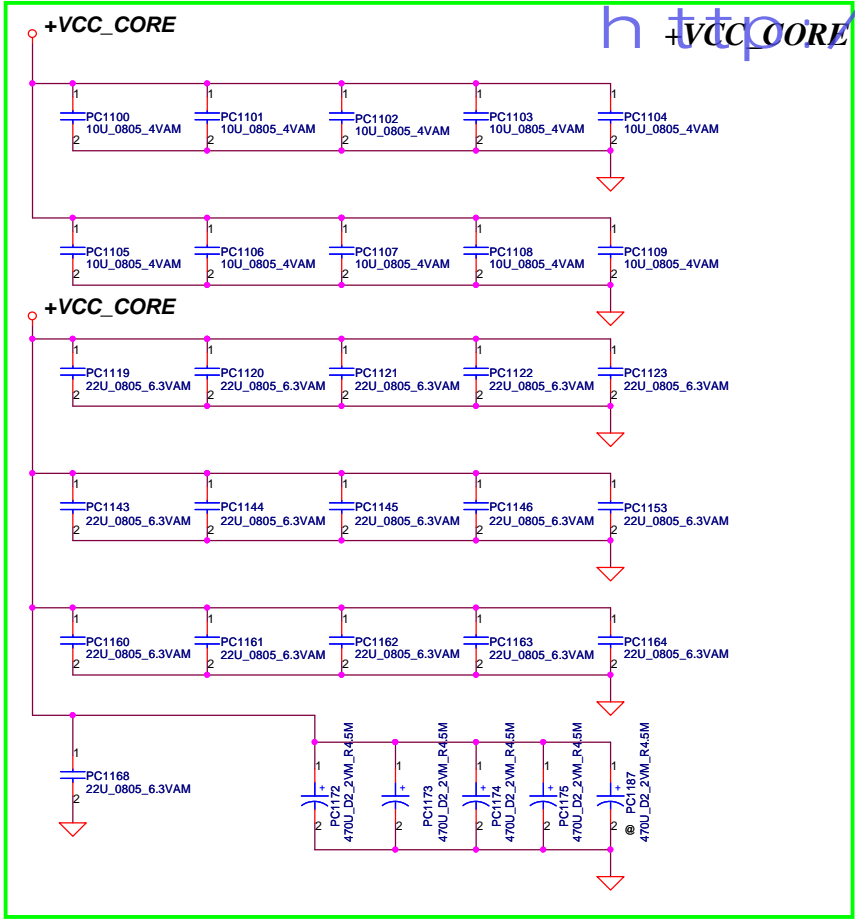
+GPU_CORE
TDC 35A
Peak Current 42A
OCP current 51A
No Load line
FSW=400kHz

Layout Note:
Place near Phase1 Choke

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