

COMPAL CONFIDENTIAL

MODEL NAME : *NAL60*  
PCB NO : *LA-5691P ( DAA00001K00 )*  
BOM P/N : *43178731L01/43178731L02*

M10 Lafite  
BGA Arrandale (34 x 28 mm) +  
SFF IBEXPEAK-M

2009-07-07  
REV : 0.1(X00)

@ : Nopop Component

MB Type	BOM P/N	CPU	With BLT	Non BLT	TCM		TPM		BOM CONFIG
			1@	2@	W(3@)	W/O(4@)	W(5@)	W/O(6@)	
BLT EN,TPM EN	43178731L01	SV 2.4G	*			*	*		1@,4@,5@
BLT EN,TPM EN	43178731L02	SV 2.0G	*		*			*	1@,3@,6@
BLT DIS,TCM EN	43178731L03	LV 1.8G		*		*	*		2@,4@,5@

MB PCB	
Part Number	Description
DAA00001K00	PCB QAW LA-5691P REV0 M/B

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Title

Cover Sheet

Size

Document Number

LA-5691P

Rev

0.1

Date

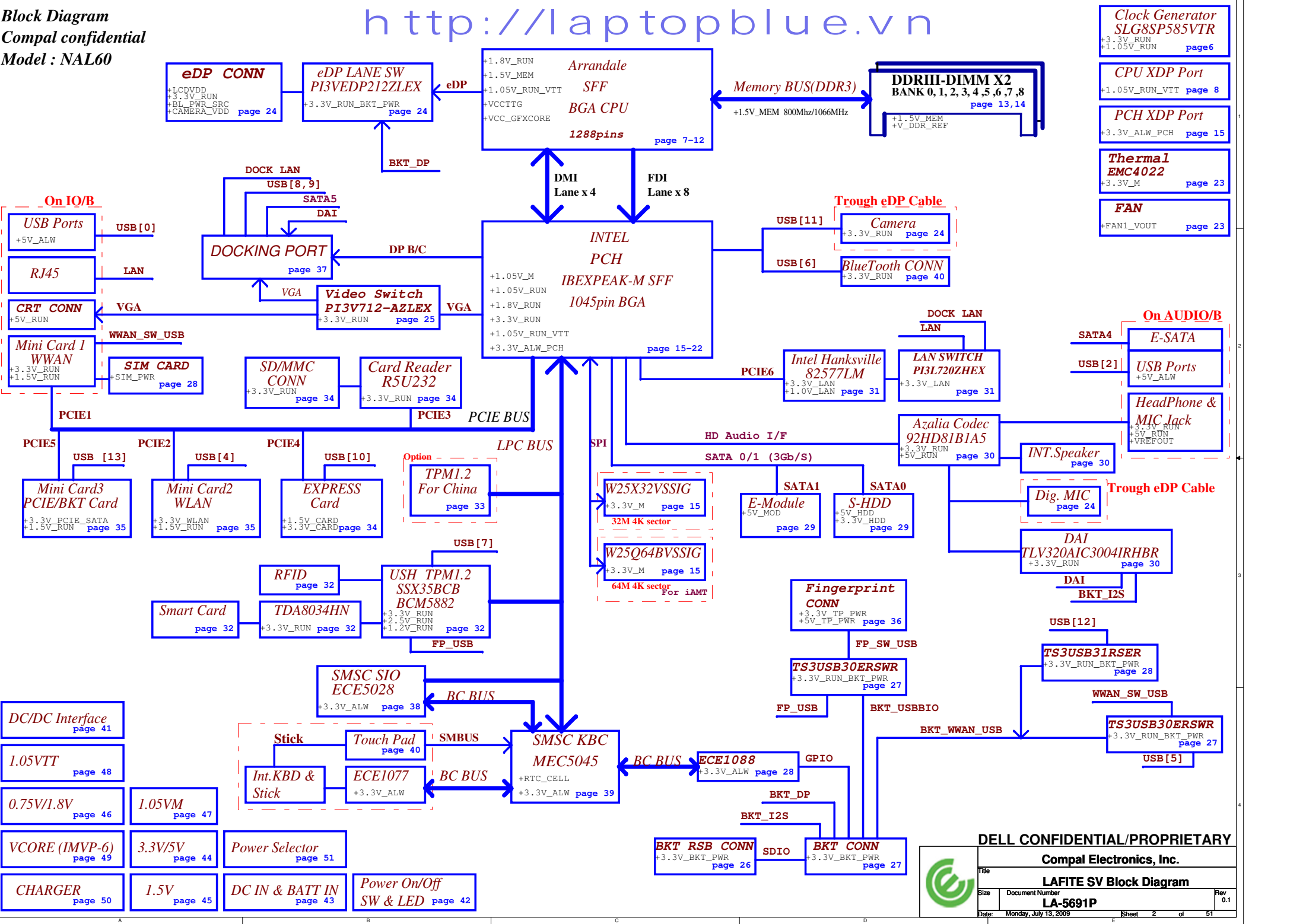
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LAFITE SV Block Diagram			
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# POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	ON
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

# PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCH	USB PORT#	DESTINATION
	0	USB Port (Ext Right Side)
	1	NA
	2	USB Port (Ext Left Side )
	3	NA
	4	WLAN
	5	WWAN
	6	Bloetooth
	7	USB->BIO
	8	DOCKING
	9	DOCKING
	10	Express Card
	11	Camera
	12	BKT
	13	WPAN/NVMHCI

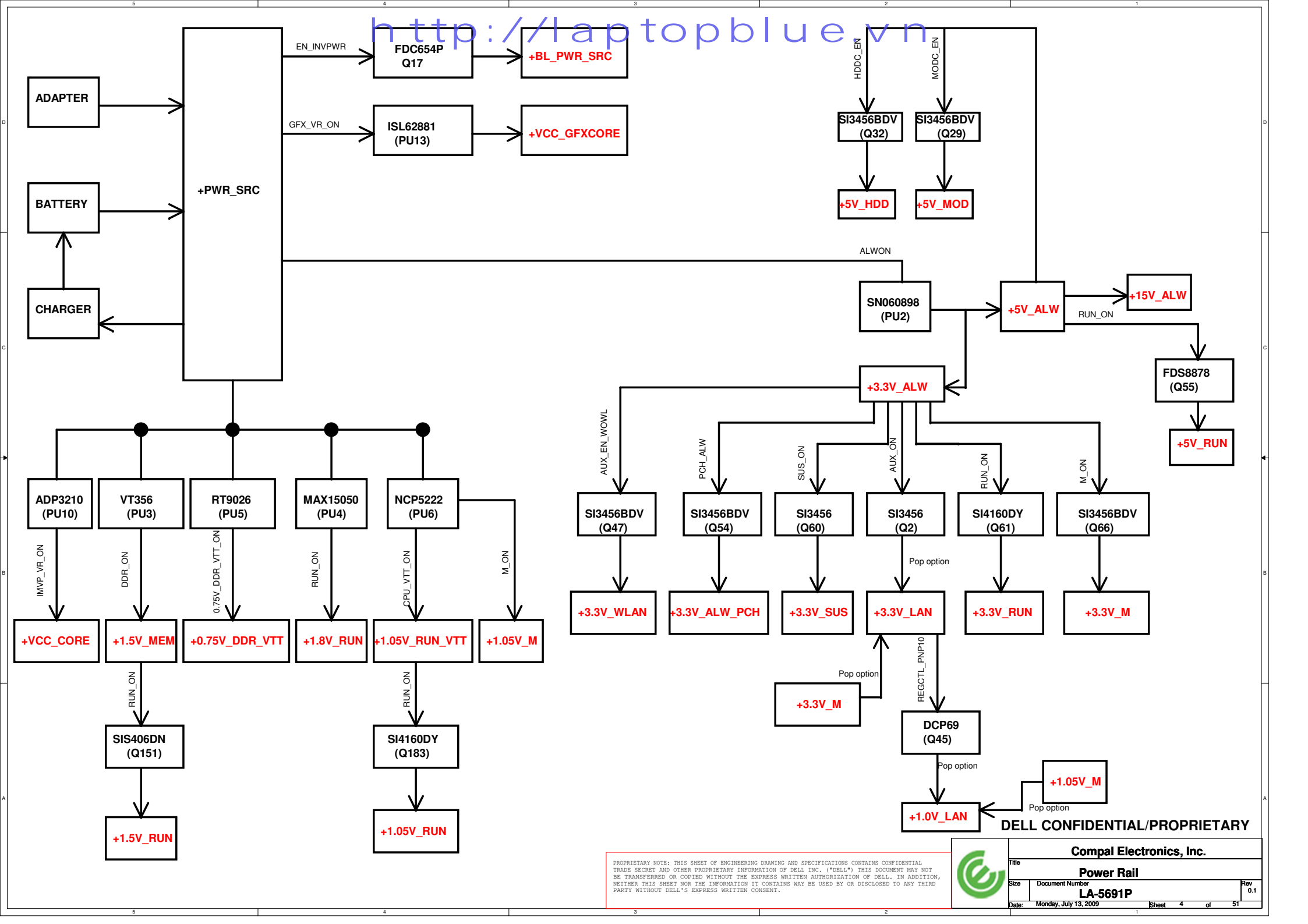
PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Card Reader
Lane 4	EXPRESS CARD
Lane 5	MINI CARD-3 WPAN/NVMHCI
Lane 6	10/100/1G LAN
Lane 7	None
Lane 8	None

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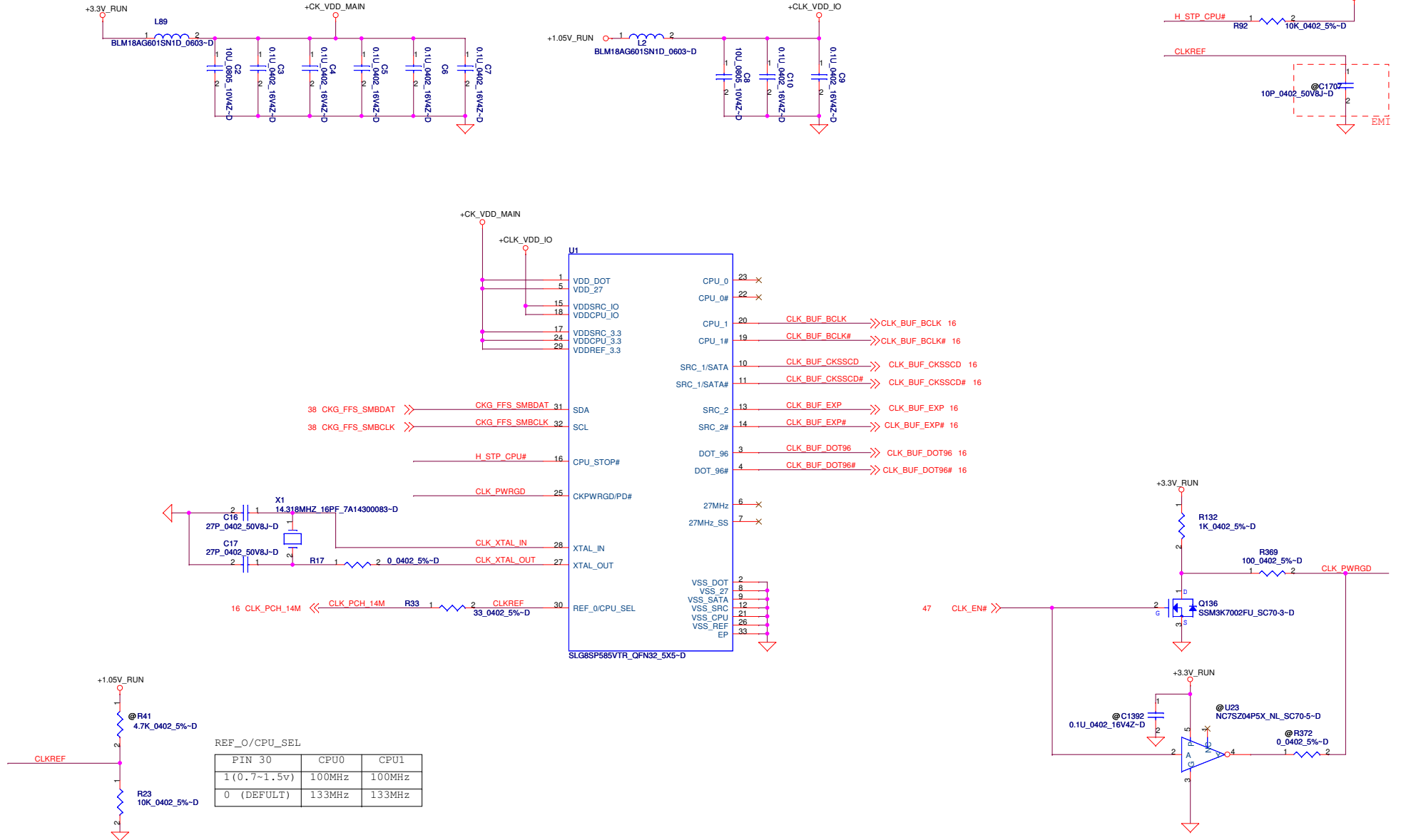
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+CLK\_VDD\_IO CAN BE RANGE FROM 1.05V TO 3V

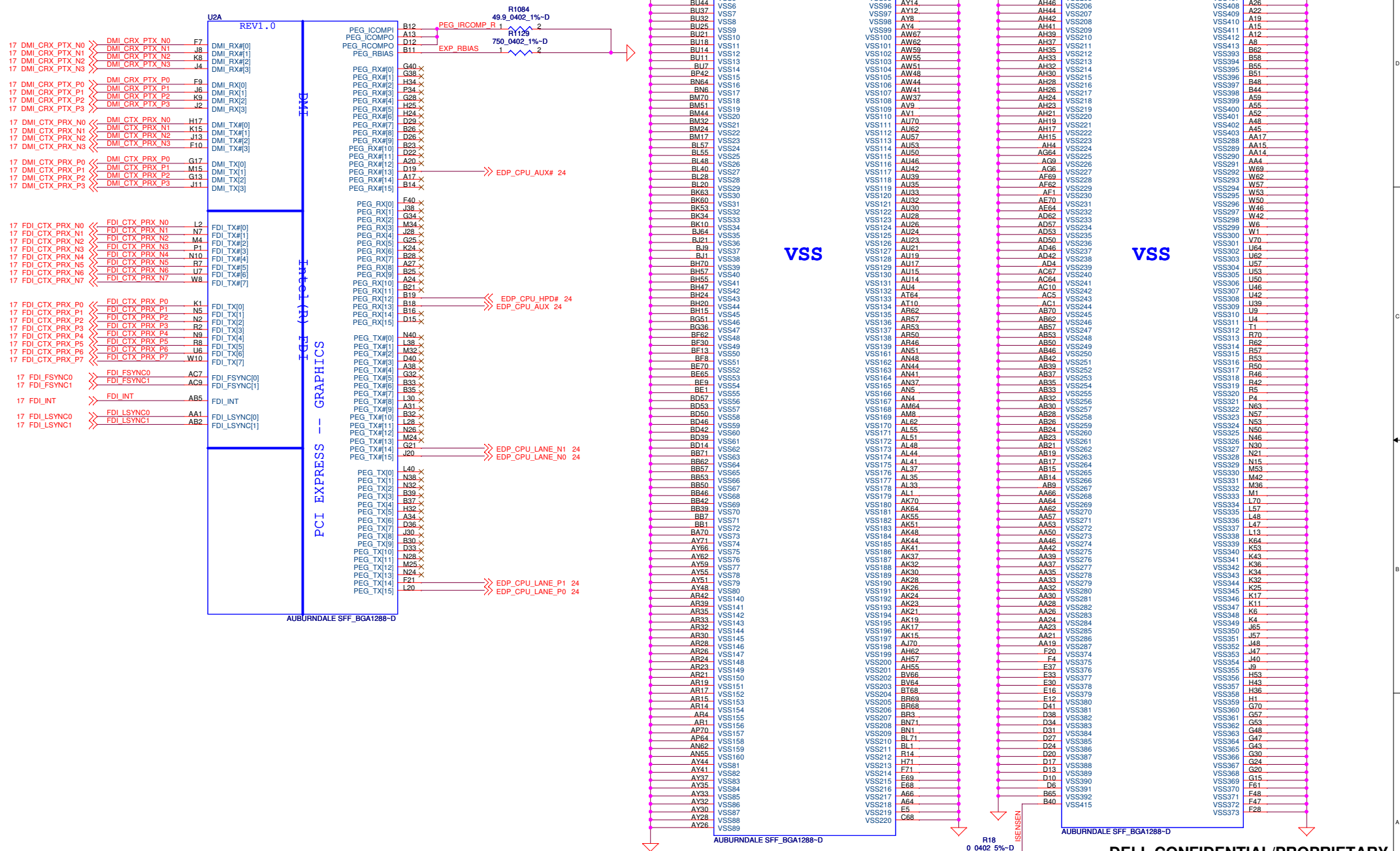


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Clock Generator			
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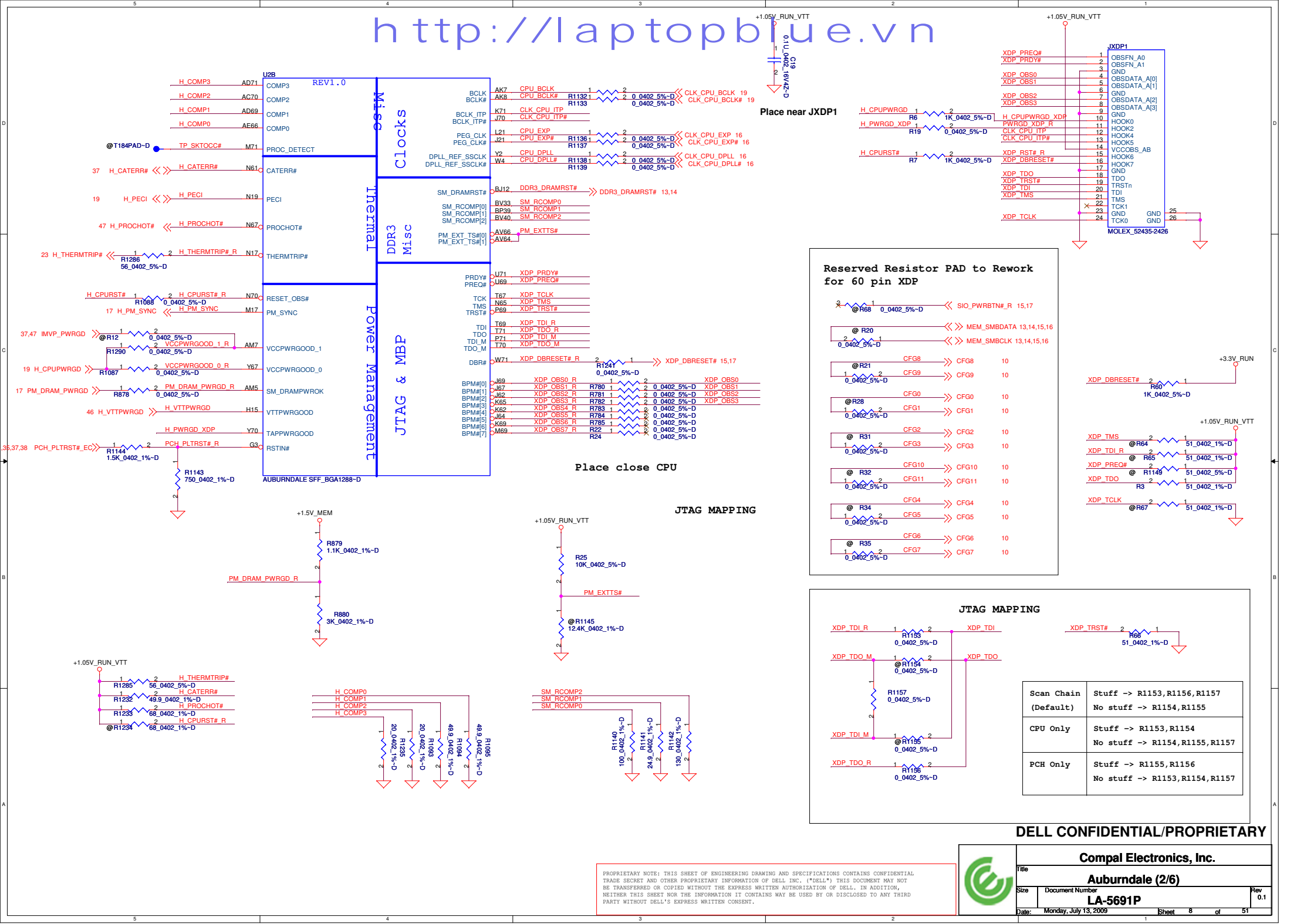
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**Auburndale (1/6)**

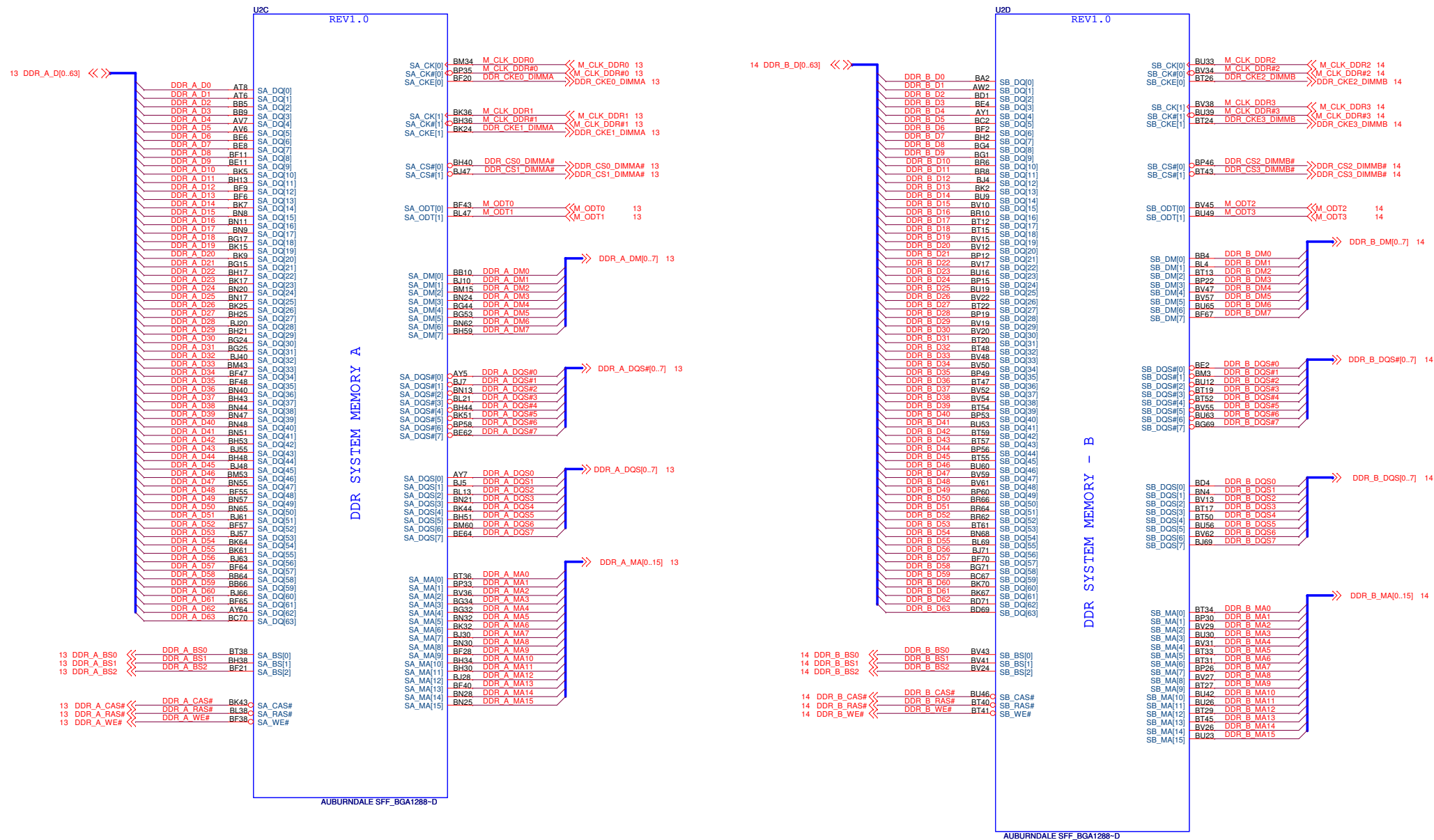
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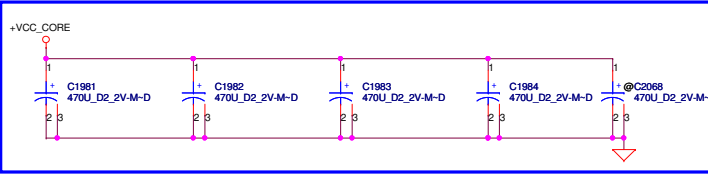
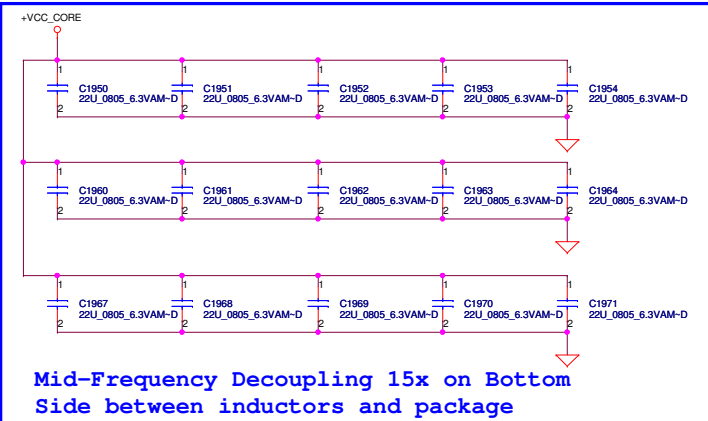
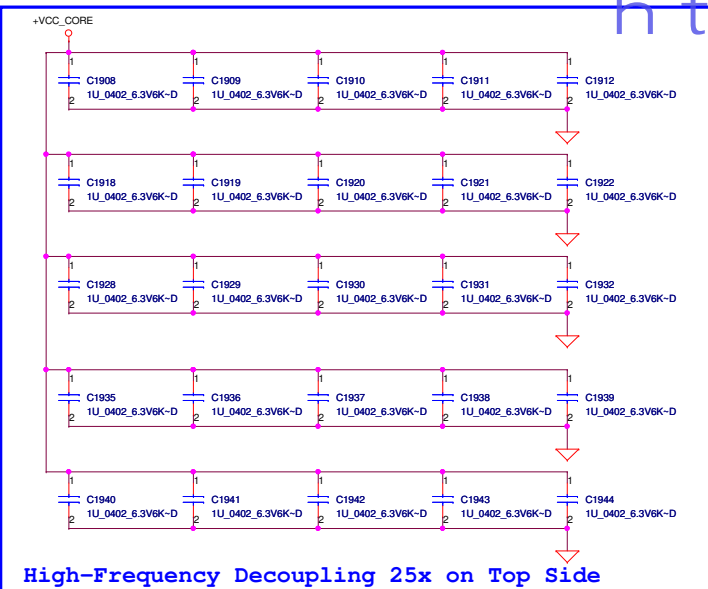
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**LA-5691P**

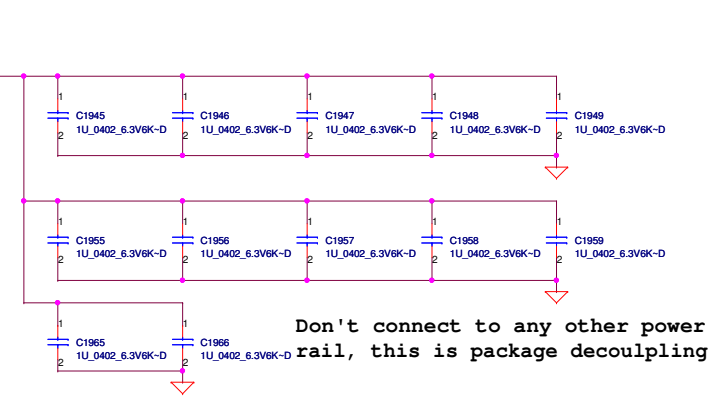
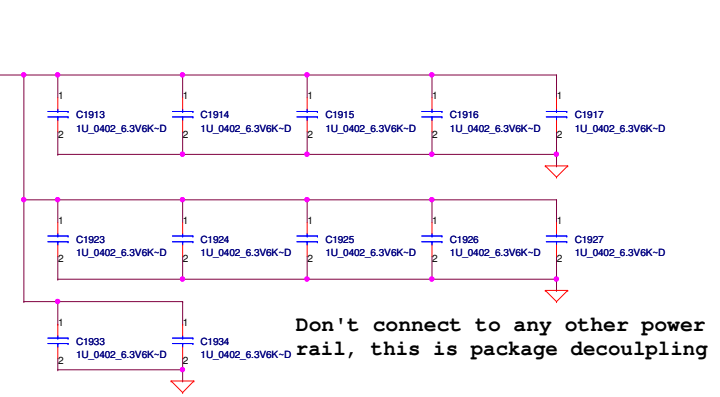
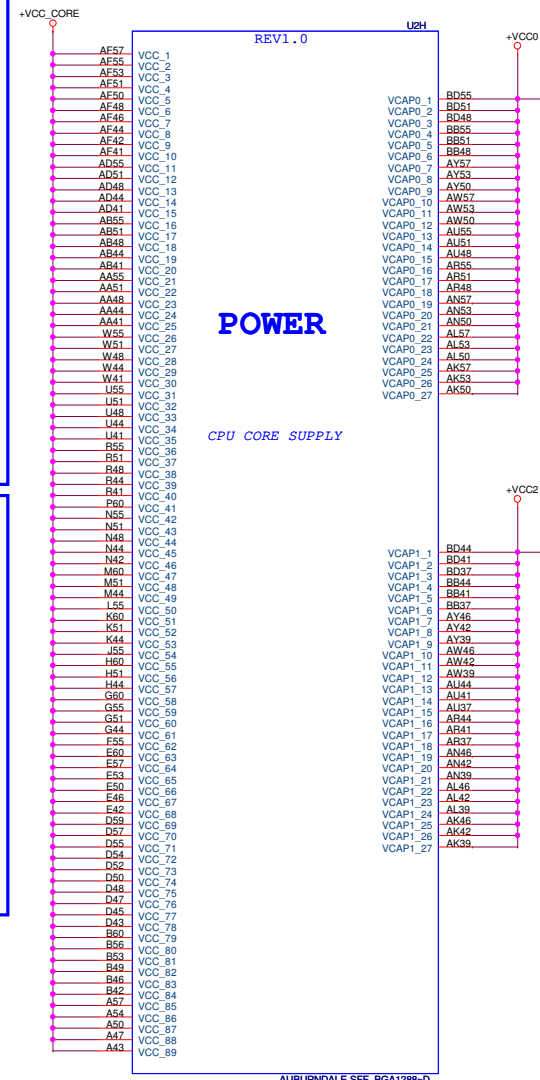
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Current =48A



PROCESSOR Power Rail Table (EDS V1.0)		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VXMG	1.5	22
VccPLL	1.8	1.35
VCORE	0.75	48
VDDR	1.5	3
VTT	1.05	18

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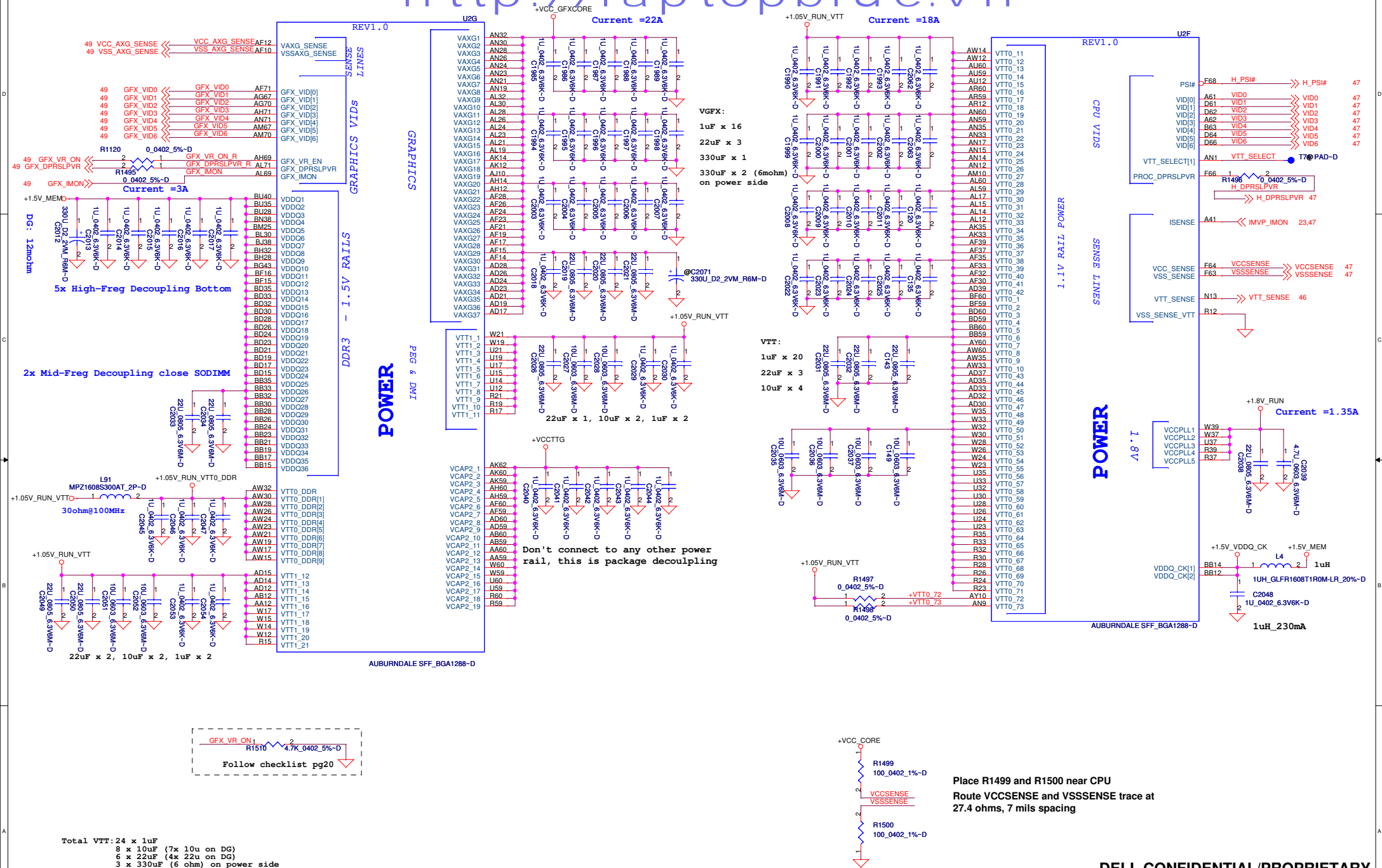
Auburndale (5/6)

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**Auburndale (6/6)**

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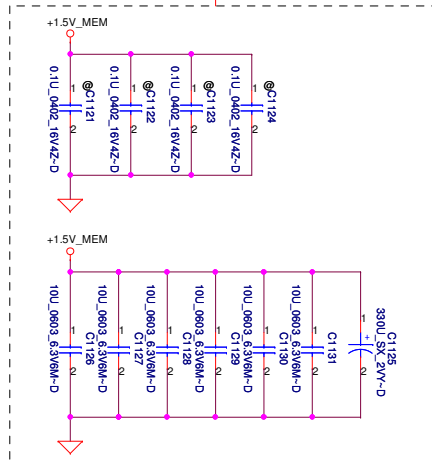
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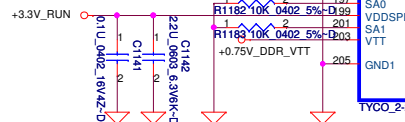
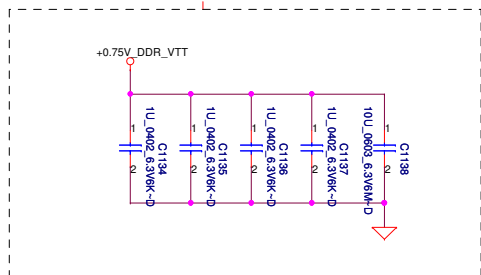
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9 DDR\_A\_D[0..63] <<>>  
9 DDR\_A\_DM[0..7] <<>>  
9 DDR\_A\_DQS[0..7] <<>>  
9 DDR\_A\_MA[0..15] <<>>

Populate R87 for Intel DDR3  
VREFDQ multiple methods M1

Layout Note:  
Place near JDIMMA



Layout Note:  
Place near JDIMMA.203,204



9 DDR\_CKE0\_DIMMA >>> DDR\_CKE0\_DIMMA

9 DDR\_A\_BS2 >>> DDR\_A\_BS2

9 M\_CLK\_DDR0 >>> M\_CLK\_DDR0

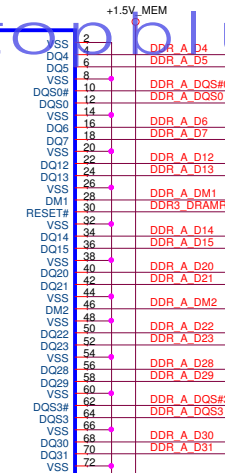
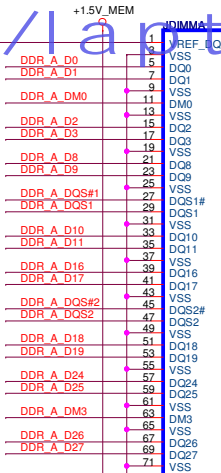
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9 DDR\_A\_BS0 >>> DDR\_A\_BS0

9 DDR\_A\_WE# >>> DDR\_A\_WE#

9 DDR\_A\_CAS# >>> DDR\_A\_CAS#

9 DDR\_CS1\_DIMMA# >>> DDR\_CS1\_DIMMA#



9 DDR\_CKE1\_DIMMA >>> DDR\_CKE1\_DIMMA

9 DDR\_A\_MA12 >>> DDR\_A\_MA12

9 M\_CLK\_DDR1 >>> M\_CLK\_DDR1

9 M\_CLK\_DDR#1 >>> M\_CLK\_DDR#1

9 DDR\_A\_BS1 >>> DDR\_A\_BS1

9 DDR\_A\_WE# >>> DDR\_A\_WE#

9 DDR\_A\_CAS# >>> DDR\_A\_CAS#

9 DDR\_CS1\_DIMMA# >>> DDR\_CS1\_DIMMA#

9 M\_CLK\_DDR1 >>> M\_CLK\_DDR1

9 M\_CLK\_DDR#1 >>> M\_CLK\_DDR#1

9 DDR\_A\_BS1 >>> DDR\_A\_BS1

9 DDR\_A\_WE# >>> DDR\_A\_WE#

9 DDR\_A\_CAS# >>> DDR\_A\_CAS#

9 DDR\_CS1\_DIMMA# >>> DDR\_CS1\_DIMMA#

9 M\_CLK\_DDR1 >>> M\_CLK\_DDR1

9 M\_CLK\_DDR#1 >>> M\_CLK\_DDR#1

9 DDR\_A\_BS1 >>> DDR\_A\_BS1

9 DDR\_A\_WE# >>> DDR\_A\_WE#

9 DDR\_A\_CAS# >>> DDR\_A\_CAS#

9 DDR\_CS1\_DIMMA# >>> DDR\_CS1\_DIMMA#

9 M\_CLK\_DDR1 >>> M\_CLK\_DDR1

9 M\_CLK\_DDR#1 >>> M\_CLK\_DDR#1

9 DDR\_A\_BS1 >>> DDR\_A\_BS1

9 DDR\_A\_WE# >>> DDR\_A\_WE#

9 DDR\_A\_CAS# >>> DDR\_A\_CAS#

9 DDR\_CS1\_DIMMA# >>> DDR\_CS1\_DIMMA#

9 M\_CLK\_DDR1 >>> M\_CLK\_DDR1

9 M\_CLK\_DDR#1 >>> M\_CLK\_DDR#1

9 DDR\_A\_BS1 >>> DDR\_A\_BS1

9 DDR\_A\_WE# >>> DDR\_A\_WE#

9 DDR\_A\_CAS# >>> DDR\_A\_CAS#

9 DDR\_CS1\_DIMMA# >>> DDR\_CS1\_DIMMA#

9 M\_CLK\_DDR1 >>> M\_CLK\_DDR1

9 M\_CLK\_DDR#1 >>> M\_CLK\_DDR#1

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9 DDR\_A\_WE# >>> DDR\_A\_WE#

9 DDR\_A\_CAS# >>> DDR\_A\_CAS#

9 DDR\_CS1\_DIMMA# >>> DDR\_CS1\_DIMMA#

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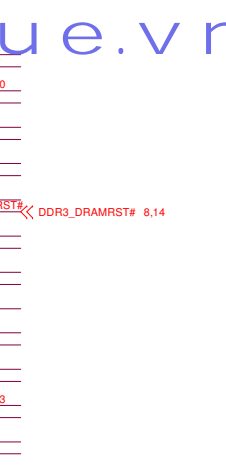
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9 DDR\_CKE1\_DIMMA >>> DDR\_CKE1\_DIMMA

9 DDR\_A\_MA15 >>> DDR\_A\_MA15

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9 M\_CLK\_DDR#1 >>> M\_CLK\_DDR#1

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9 DDR\_A\_WE# >>> DDR\_A\_WE#

9 DDR\_A\_CAS# >>> DDR\_A\_CAS#

9 DDR\_CS1\_DIMMA# >>> DDR\_CS1\_DIMMA#

9 M\_CLK\_DDR1 >>> M\_CLK\_DDR1

9 M\_CLK\_DDR#1 >>> M\_CLK\_DDR#1

9 DDR\_A\_BS1 >>> DDR\_A\_BS1

9 DDR\_A\_WE# >>> DDR\_A\_WE#

9 DDR\_A\_CAS# >>> DDR\_A\_CAS#

9 DDR\_CS1\_DIMMA# >>> DDR\_CS1\_DIMMA#

9 M\_CLK\_DDR1 >>> M\_CLK\_DDR1

9 M\_CLK\_DDR#1 >>> M\_CLK\_DDR#1

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9 DDR\_A\_WE# >>> DDR\_A\_WE#

9 DDR\_A\_CAS# >>> DDR\_A\_CAS#

9 DDR\_CS1\_DIMMA# >>> DDR\_CS1\_DIMMA#

9 M\_CLK\_DDR1 >>> M\_CLK\_DDR1

9 M\_CLK\_DDR#1 >>> M\_CLK\_DDR#1

9 DDR\_A\_BS1 >>> DDR\_A\_BS1

9 DDR\_A\_WE# >>> DDR\_A\_WE#

9 DDR\_A\_CAS# >>> DDR\_A\_CAS#

9 DDR\_CS1\_DIMMA# >>> DDR\_CS1\_DIMMA#

9 M\_CLK\_DDR1 >>> M\_CLK\_DDR1

9 M\_CLK\_DDR#1 >>> M\_CLK\_DDR#1

9 DDR\_A\_BS1 >>> DDR\_A\_BS1

9 DDR\_A\_WE# >>> DDR\_A\_WE#

9 DDR\_A\_CAS# >>> DDR\_A\_CAS#

9 DDR\_CS1\_DIMMA# >>> DDR\_CS1\_DIMMA#

9 M\_CLK\_DDR1 >>> M\_CLK\_DDR1

9 M\_CLK\_DDR#1 >>> M\_CLK\_DDR#1

9 DDR\_A\_BS1 >>> DDR\_A\_BS1

9 DDR\_A\_WE# >>> DDR\_A\_WE#

9 DDR\_A\_CAS# >>> DDR\_A\_CAS#

9 DDR\_CS1\_DIMMA# >>> DDR\_CS1\_DIMMA#

9 M\_CLK\_DDR1 >>> M\_CLK\_DDR1

9 M\_CLK\_DDR#1 >>> M\_CLK\_DDR#1

9 DDR\_A\_BS1 >>> DDR\_A\_BS1

9 DDR\_A\_WE# >>> DDR\_A\_WE#

9 DDR\_A\_CAS# >>> DDR\_A\_CAS#

9 DDR\_CS1\_DIMMA# >>> DDR\_CS1\_DIMMA#



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DDR3-SODIMM SLOT1

LA-5691P

Rev 0.1

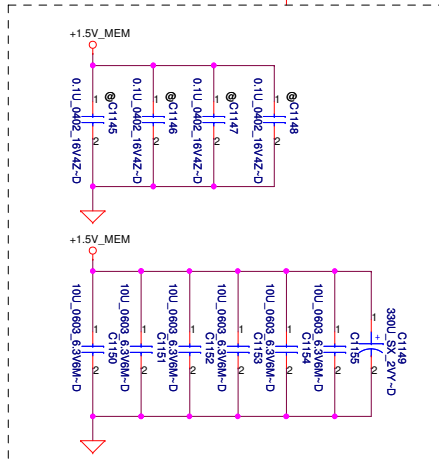
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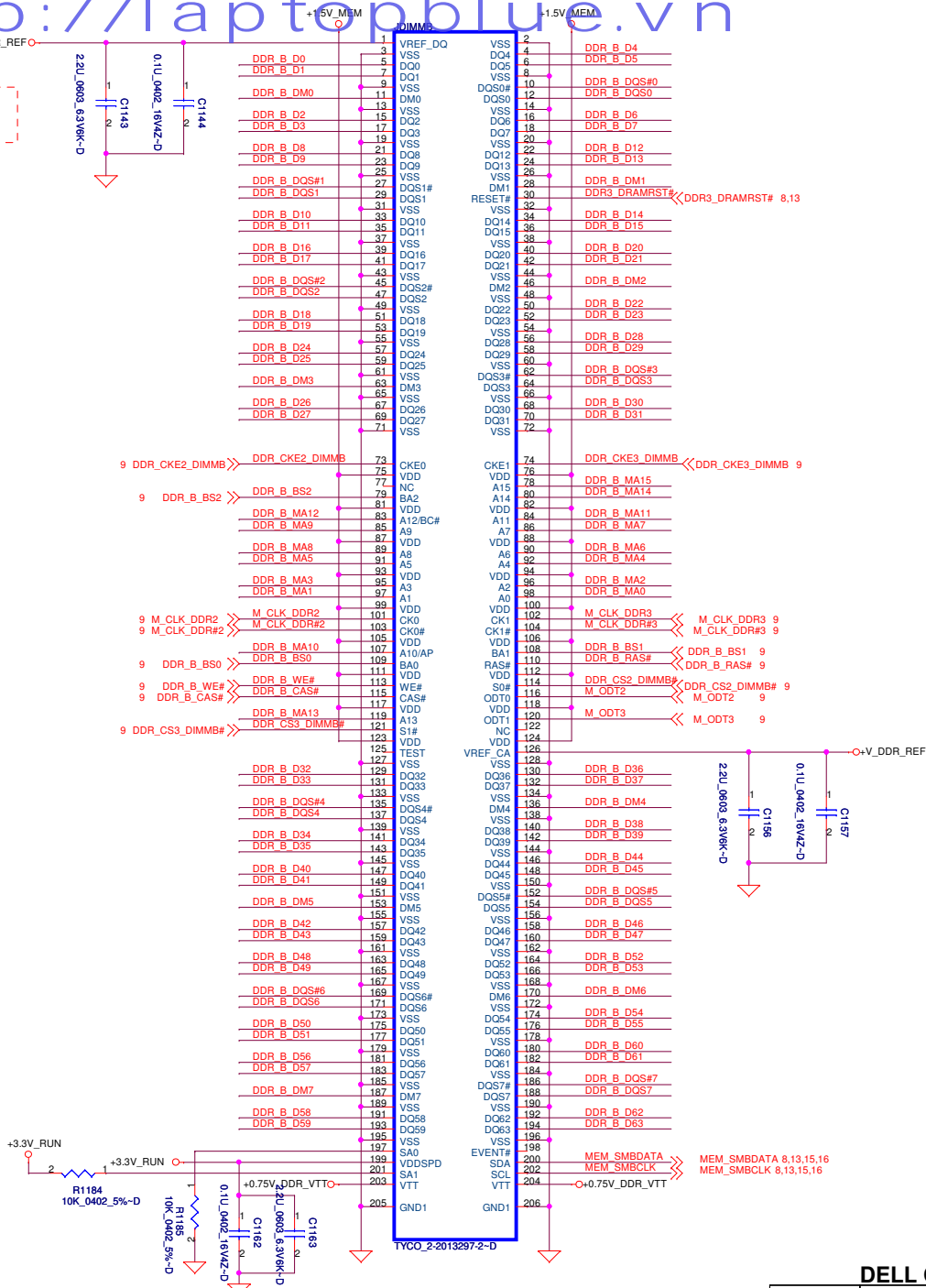
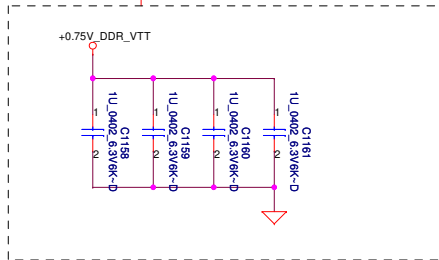
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 9 DDR\_B\_DQS#[0..7] <<>>  
 9 DDR\_B\_MA[0..15] <<>>

Populate R88 for Intel DDR3  
 VREFDQ multiple methods M1

Layout Note:  
 Place near JDIMMB



Layout Note:  
 Place near JDIMMB.203,204



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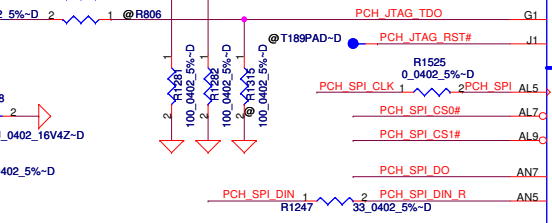
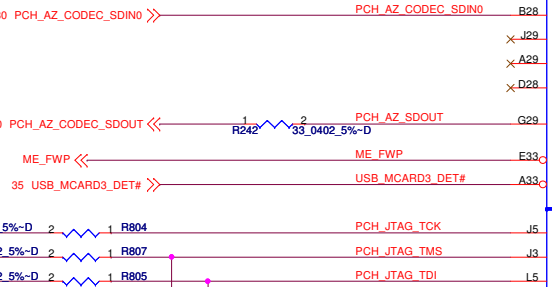
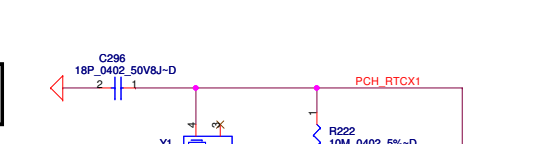
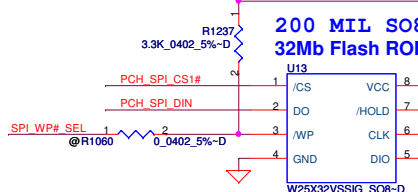
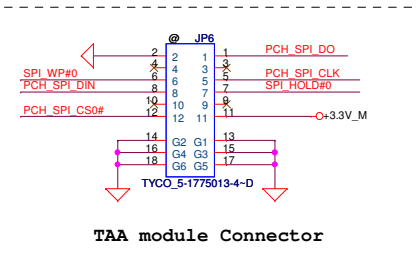
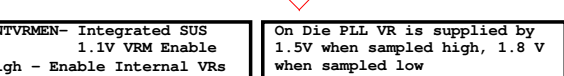
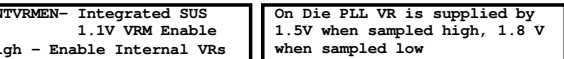


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DDR3-SODIMM SLOT2			
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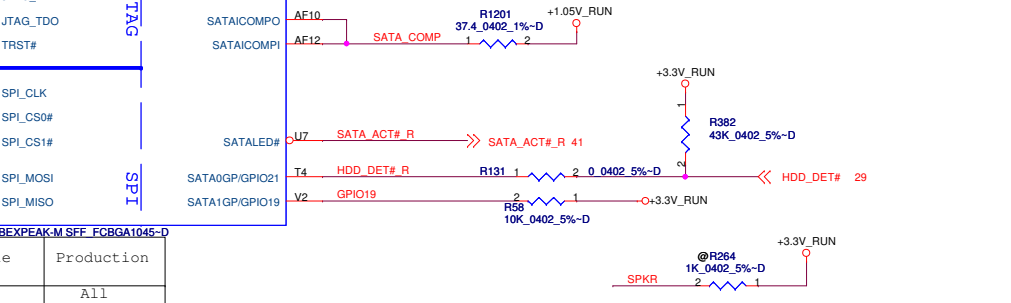
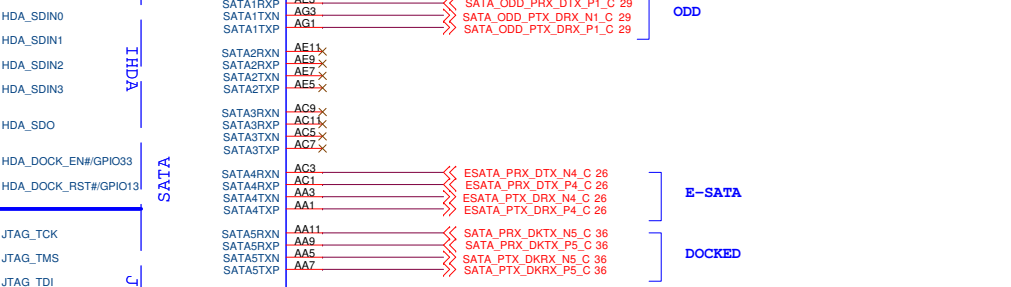
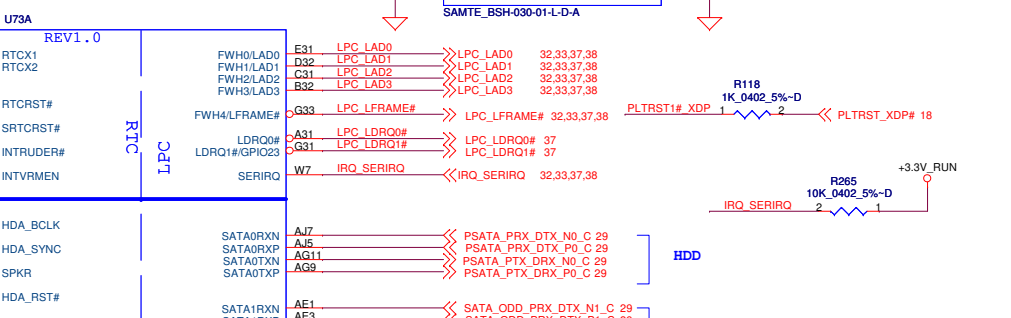
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ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



		PCH JTAG Enable		PCH JTAG Disable		Production
PCH Pin	Ref.	ES1	ES2	ES1	ES2	All
TDO	R806	No Stuff	200 ohm	No Stuff	No Stuff	51 ohm
	R1315	No Stuff	100 ohm	No Stuff	No Stuff	No Stuff
TMS	R807	200 ohm	200 ohm	No Stuff	No Stuff	51 ohm
	R1281	100 ohm	100 ohm	No Stuff	No Stuff	No Stuff
TDI	R805	200 ohm	200 ohm	20K ohm	No Stuff	51 ohm
	R1282	100 ohm	100 ohm	10K ohm	No Stuff	No Stuff
TCK	R804	51 ohm	51 ohm	51 ohm	51 ohm	51 ohm
TRST#	R808	20K ohm	20K ohm	No Stuff	No Stuff	
	R1316	10K ohm	10K ohm	No Stuff	No Stuff	



No Reboot Strap	
SPKR	Low = Default
	High = No Reboot

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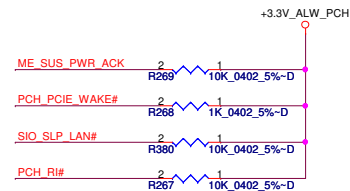
**PCH (1/8)**

Title				<b>PCH (1/8)</b>			
Size	Document Number						Rev
	<b>LA-5691P</b>						<b>0.1</b>
Date:	Monday, July 13, 2009				Sheet	15	of 51

	1
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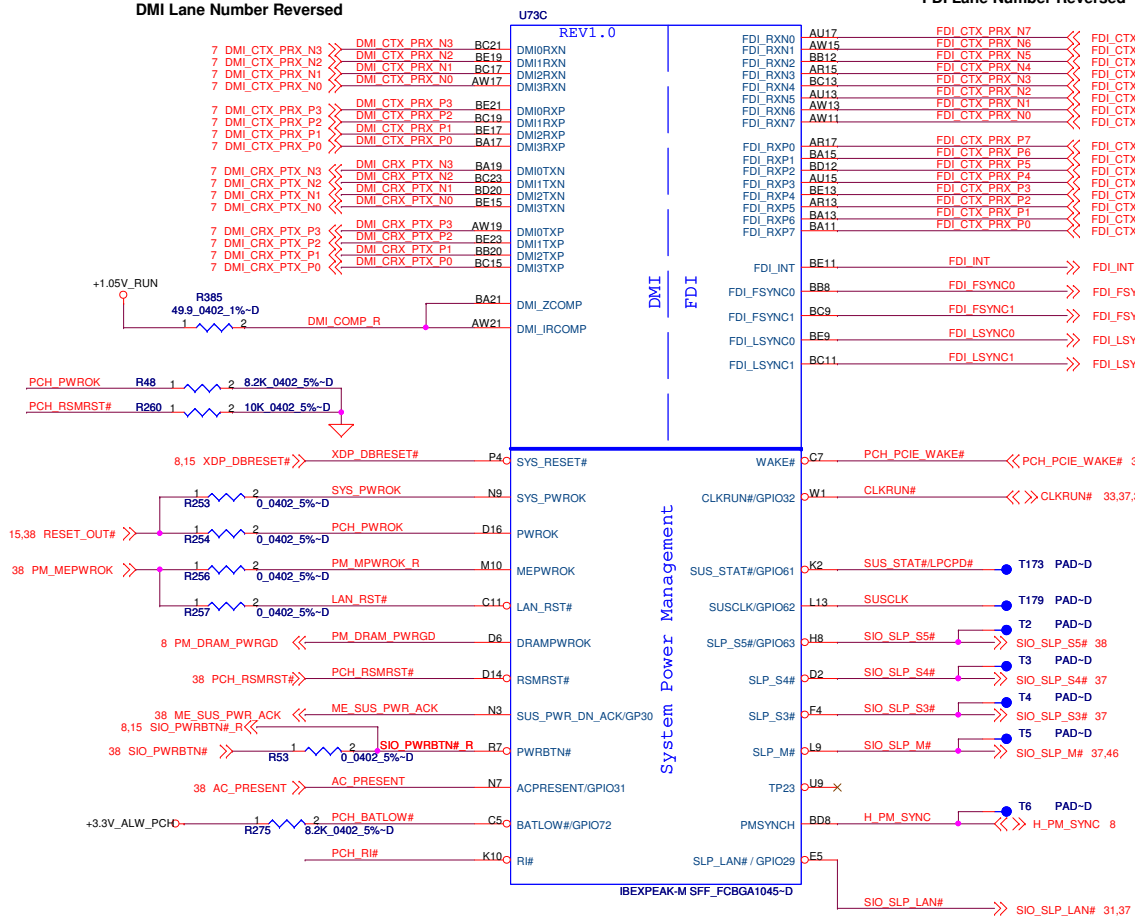




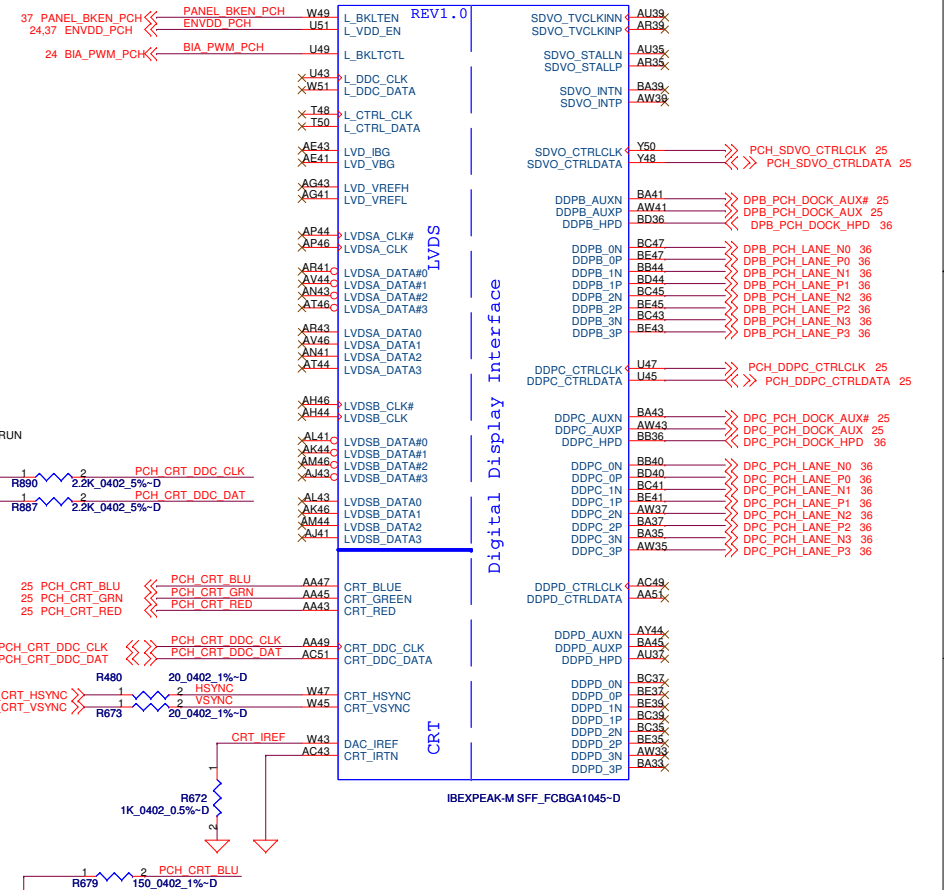


DMI Lane Number Reversed

FDI Lane Number Reversed



U73D

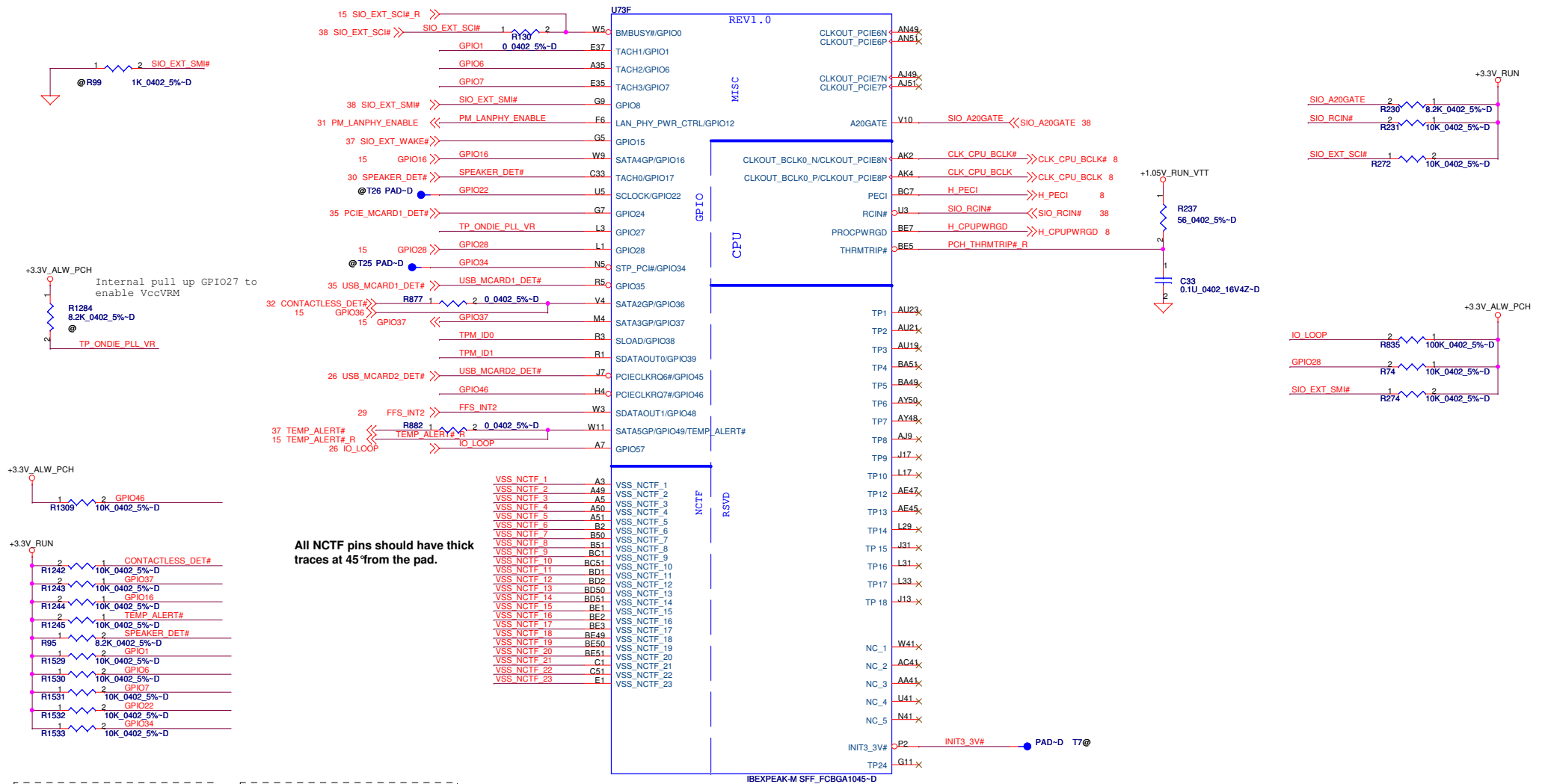


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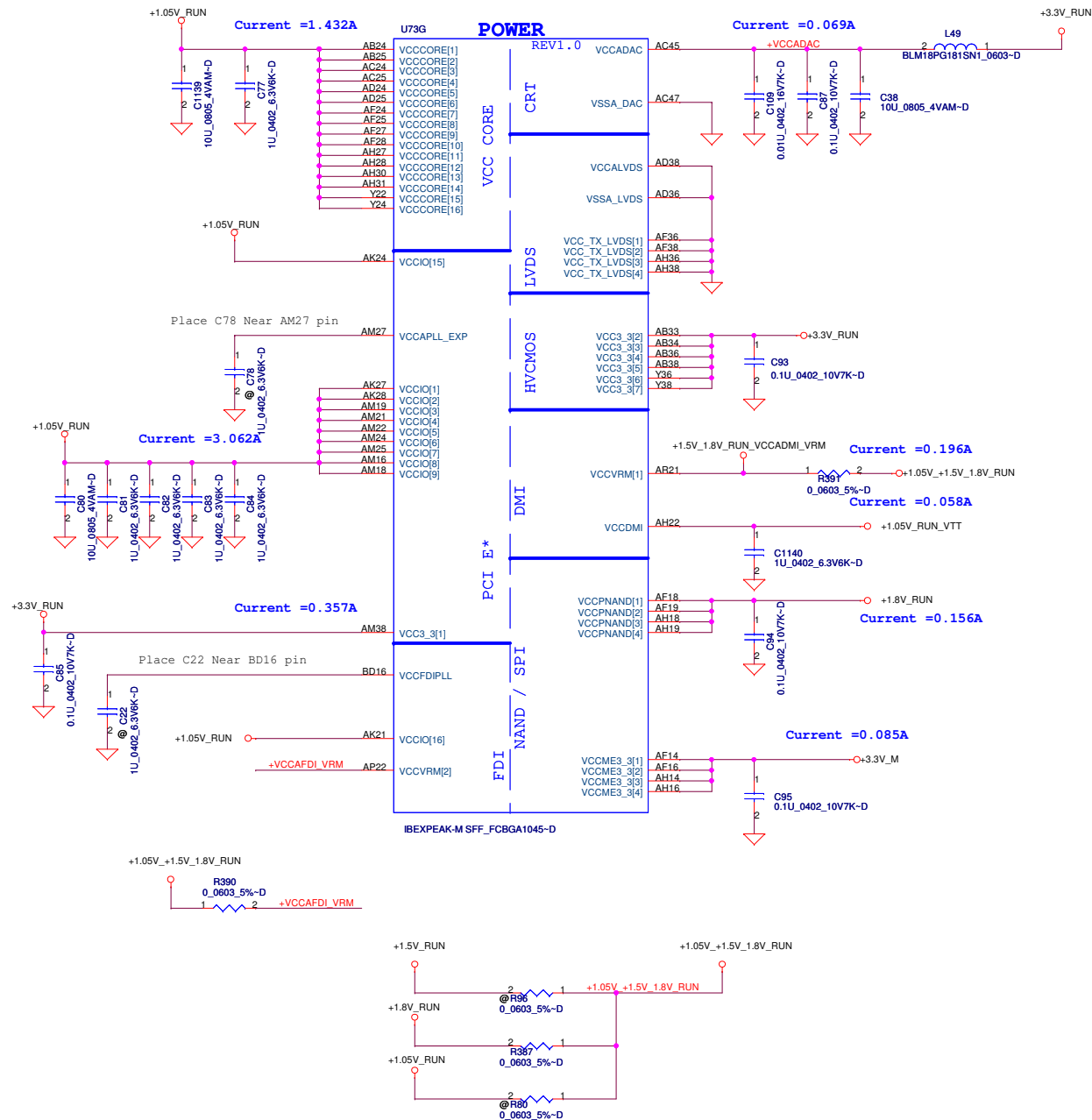
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Title			
Size	Document Number	Rev	
	LA-5691P	0.1	
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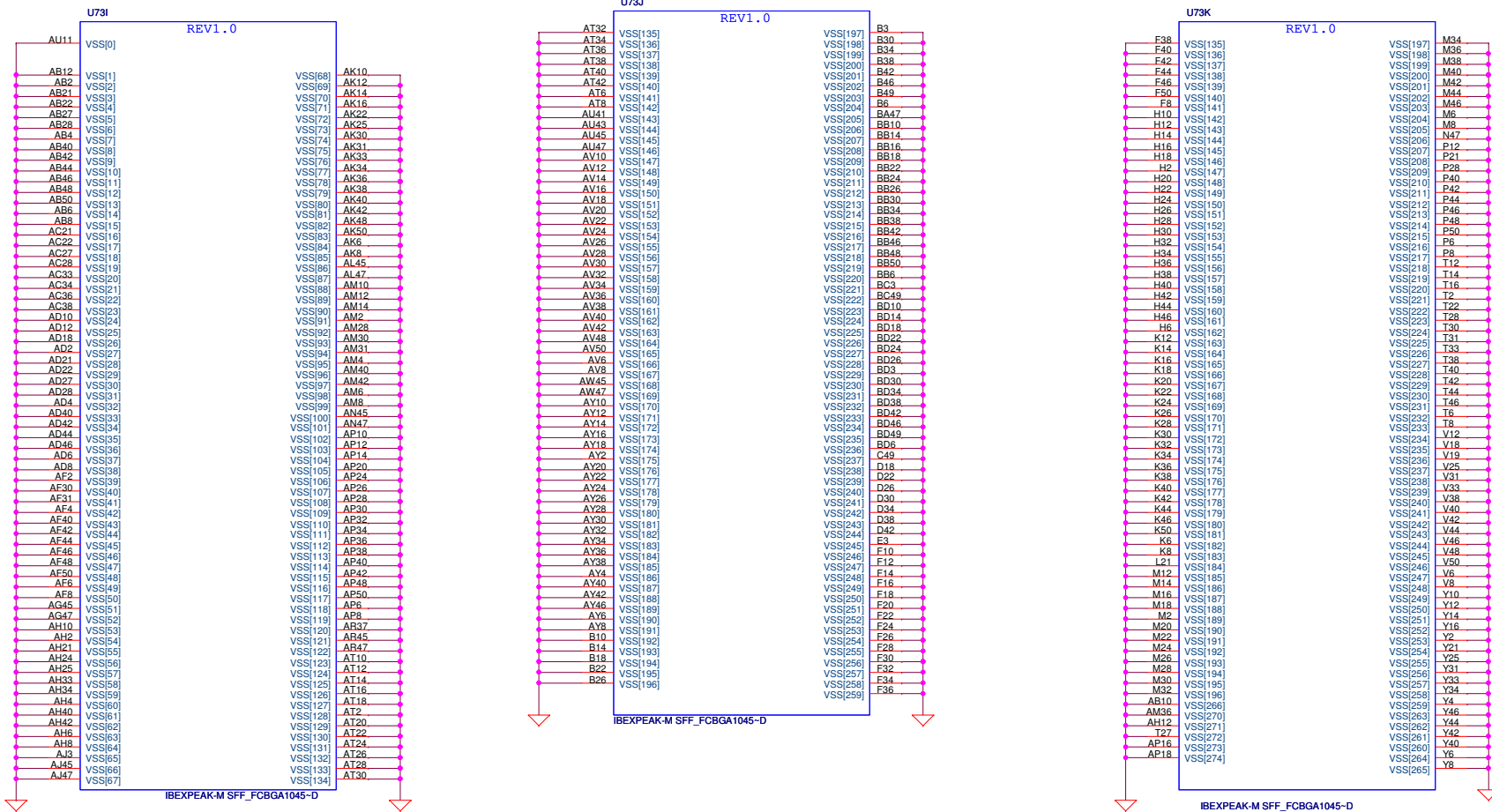


	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
USH1.0 (For SSI)	1	0
USH2.0	1	1

-----> will use MEMO control pop R339  
& de-pop R787 when USH1.0 enable  
for SSI build only







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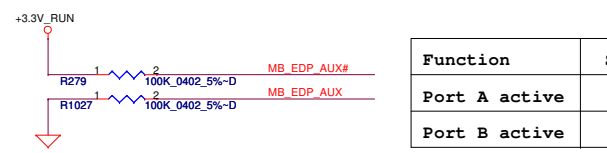
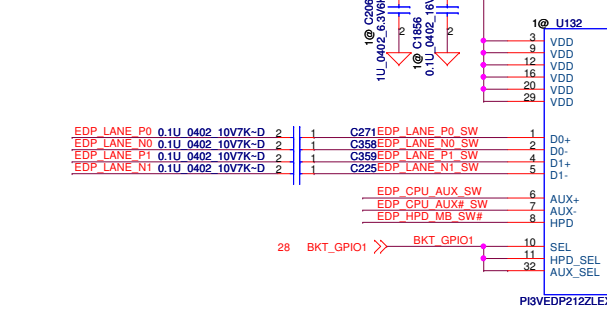
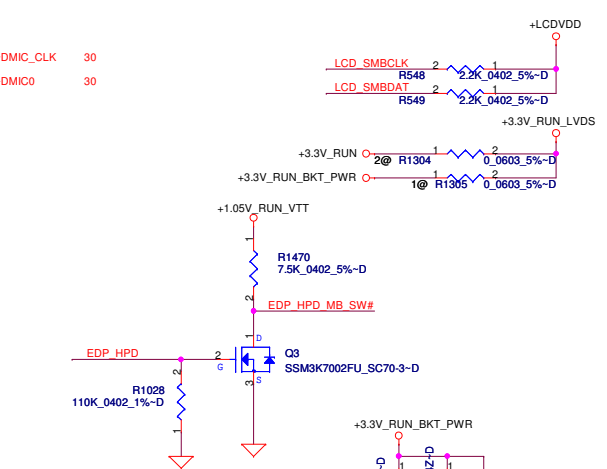
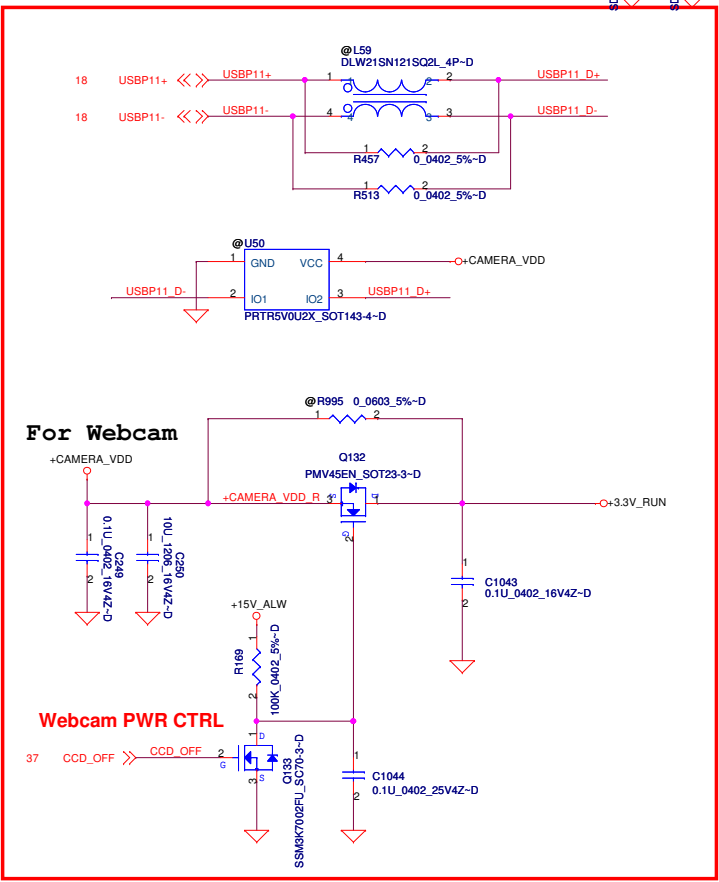
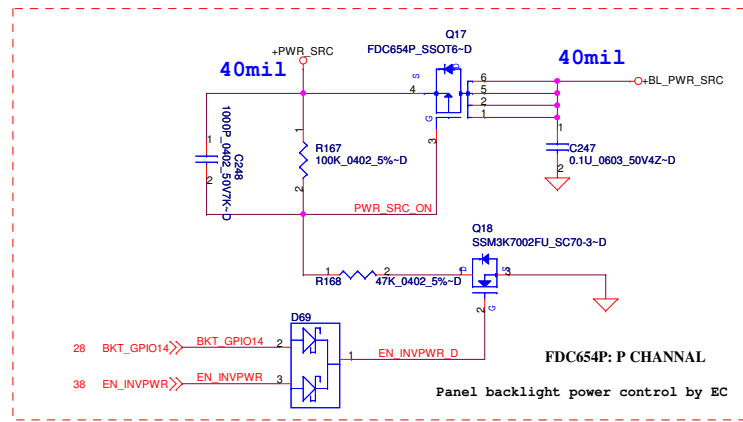
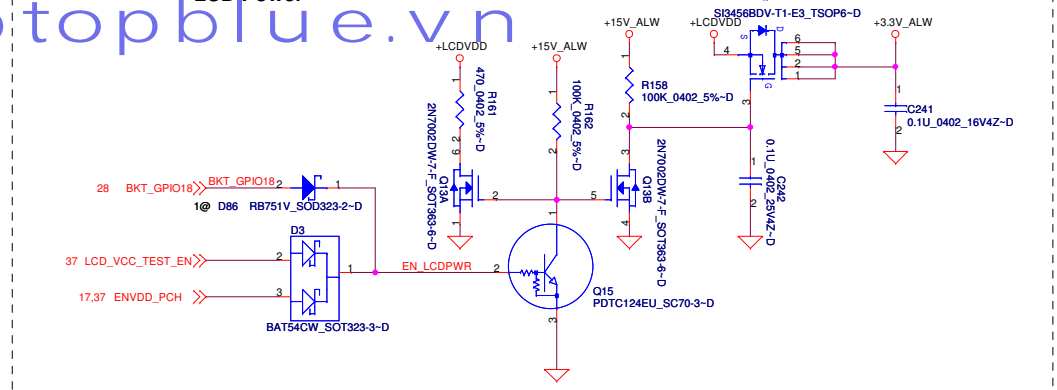
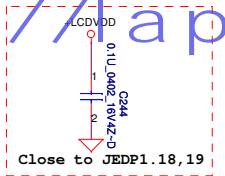
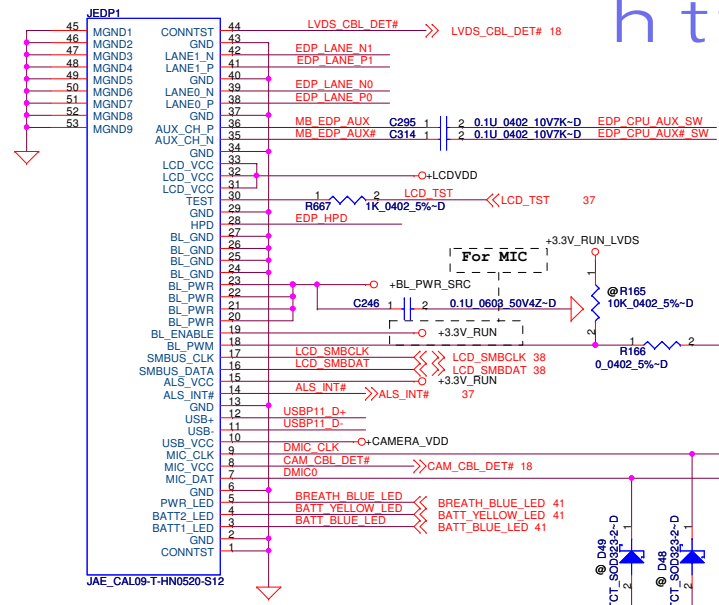
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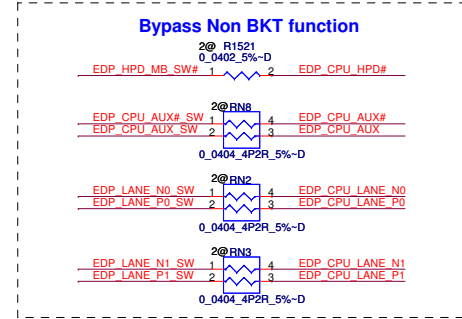




LCD Power



Function	SEL/HPD_SEL/AUX_SSEL
Port A active	L
Port B active	H



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eDP & CAM Conn

LA-5691P

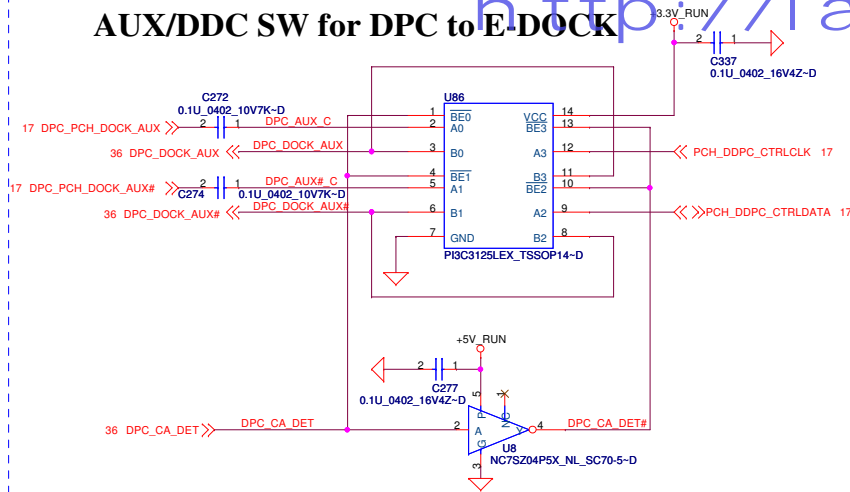
Monday, July 13, 2009

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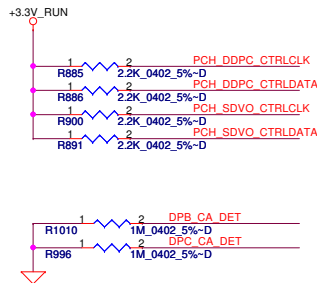
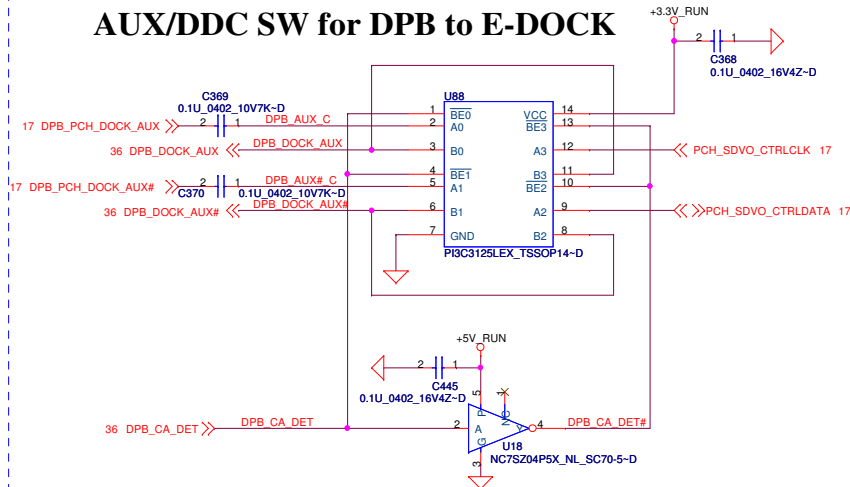
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## AUX/DDC SW for DPC to E-DOCK



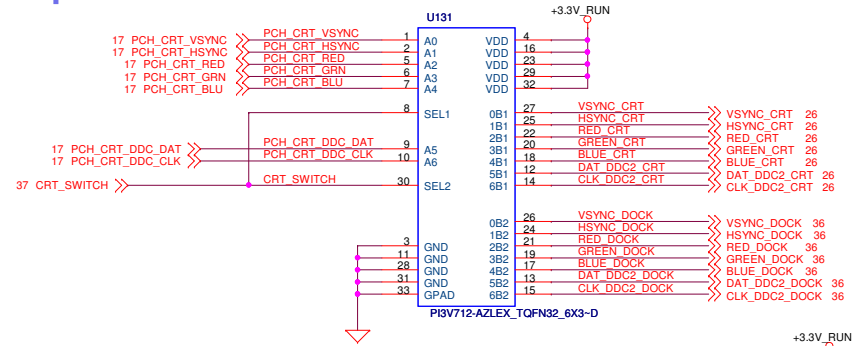
## AUX/DDC SW for DPB to E-DOCK



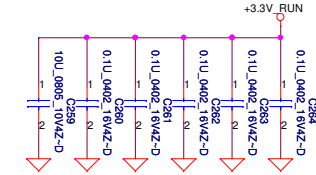
Intel WW18 Strapping option

Intel WW18 Strapping option

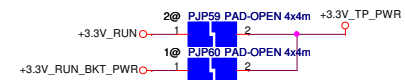
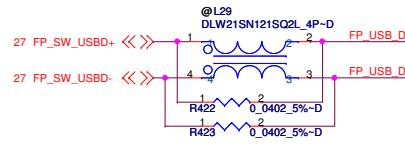
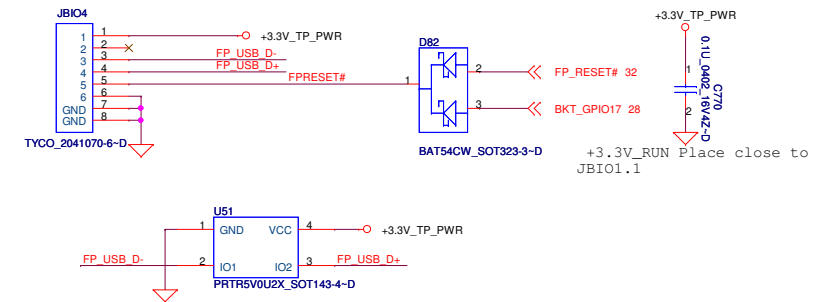
## VGA SW for MB/DOCK



SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR



## Fingerprint CONN.



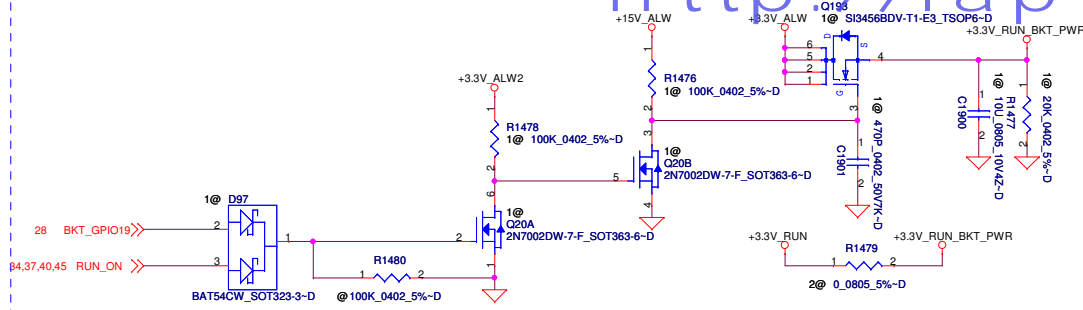
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Compal Electronics, Inc.			
Title			
DPC DPD SW for DOCK			
Size	Document Number	Rev	
	LA-5691P	0.1	
Date	Monday, July 13, 2009	Sheet	25 of 51

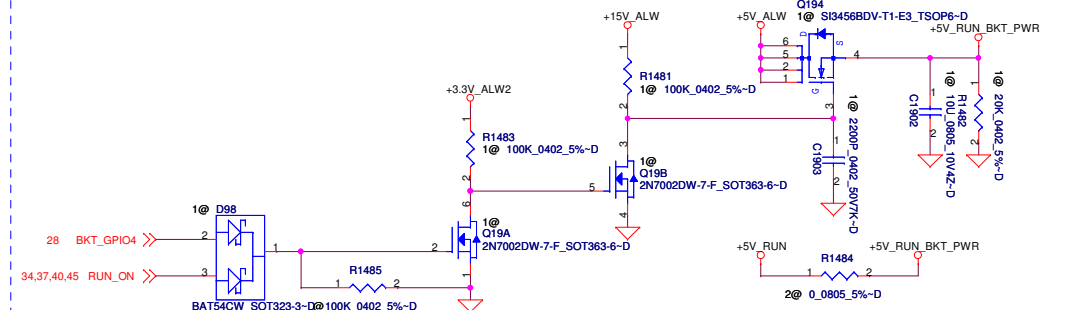
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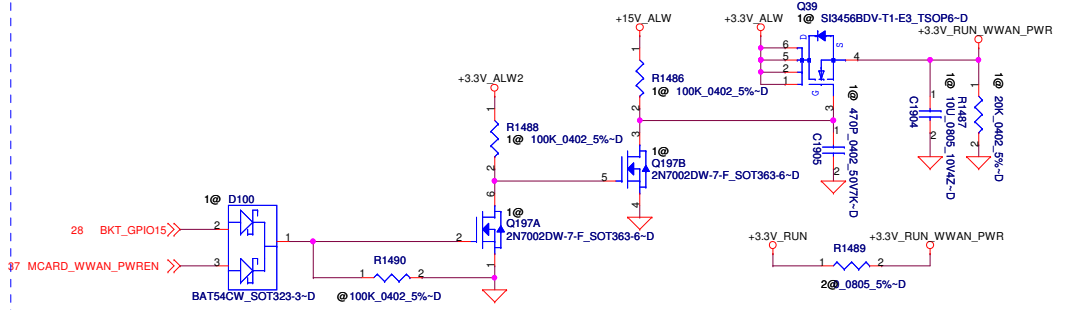
### +3.3V\_RUN\_BKT\_PWR Source



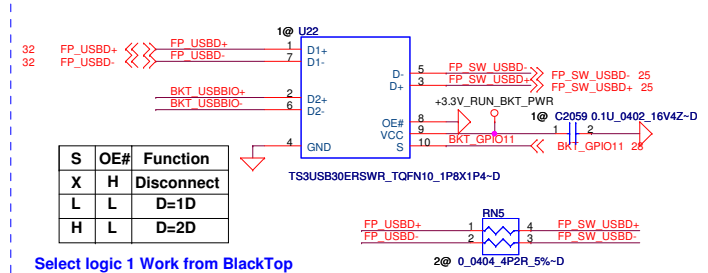
### +5V\_RUN\_BKT\_PWR Source, for Touch Pad and Audio Amplifier



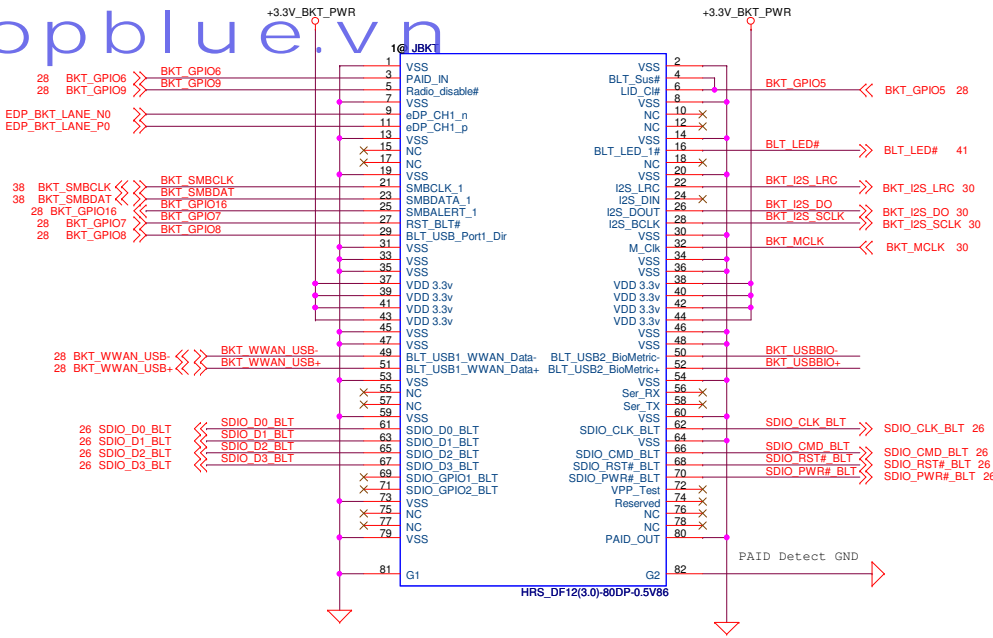
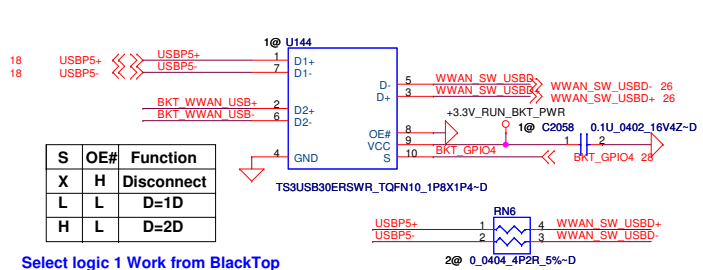
### +3.3V\_RUN\_WWAN\_PWR Source, for WWAN



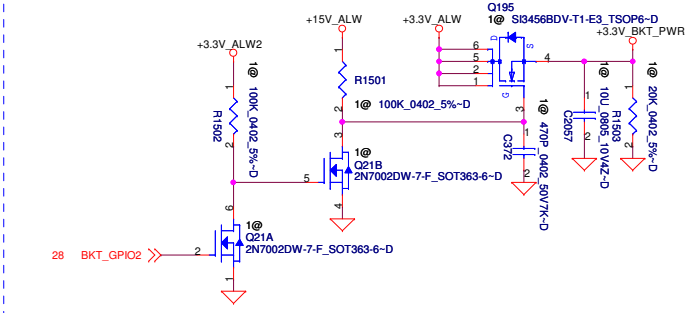
### For Biometric USB signals isolation



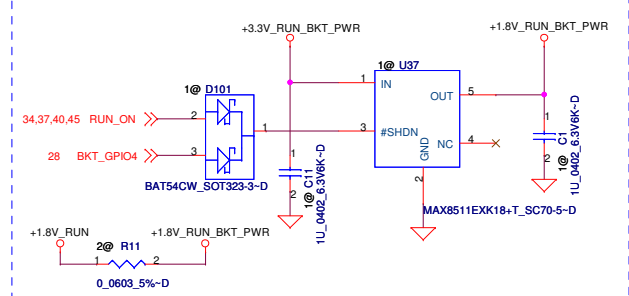
### For WWAN USB signals isolation



### Enable BlackTop POWER



### For Audio I2S



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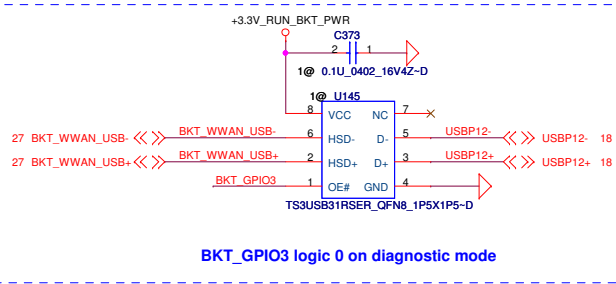


Compal Electronics, Inc.			
BlackTop POWER and CONN			
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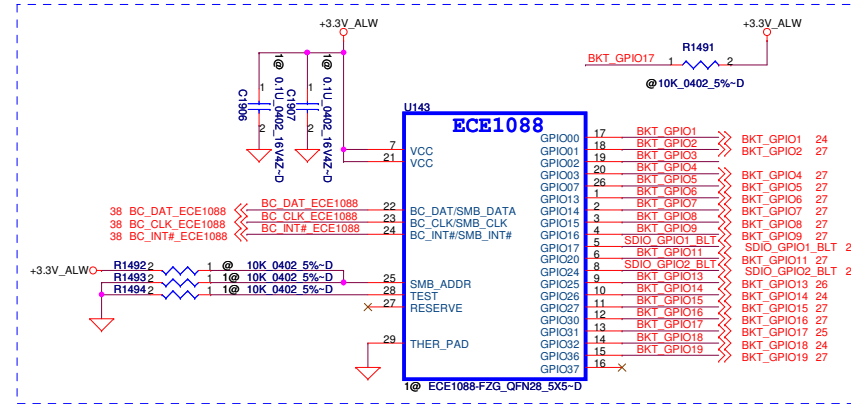
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## GPIO Expander for BlackTop

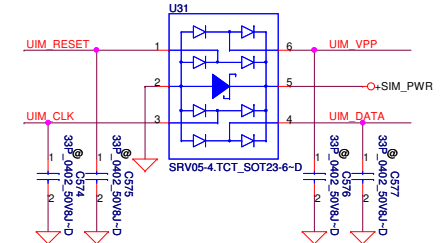
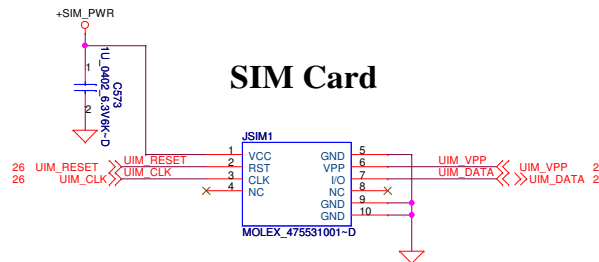
Add BlackTop to PCH interface by USB signal when diagnostic mode



- BKT\_GPIO1 → For eDP signals switch
- BKT\_GPIO2 → For BKT power switch
- BKT\_GPIO3 → For TP power switch&USB signal switch
- BKT\_GPIO4 → For AMP/TP power source&USB signal switch
- BKT\_GPIO5 → For LID\_Closed
- BKT\_GPIO6 → For PAD\_Out
- BKT\_GPIO7 → For BKT Reset
- BKT\_GPIO8 → For USB\_SEL\_BLK
- BKT\_GPIO9 → For Radio\_OFF
- BKT\_GPIO11 → Biometric mux switch
- BKT\_GPIO12 → For WLAN antenna mux control
- BKT\_GPIO13 → RSB\_DET#
- BKT\_GPIO14 → For Inverter Power
- BKT\_GPIO15 → For WWAN Power
- BKT\_GPIO16 → For SMBALERT
- BKT\_GPIO17 → For Biometric reset signal
- BKT\_GPIO18 → For LVDS Power switch
- BKT\_GPIO19 → For TP Power



## SIM Card



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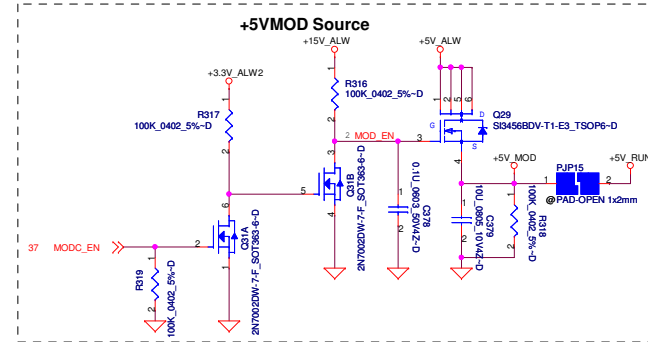
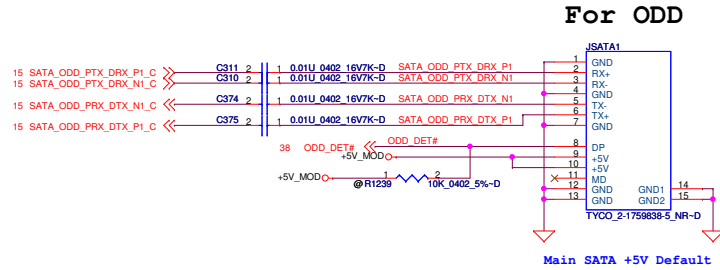
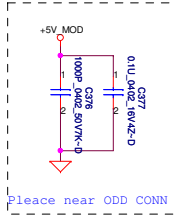
Compal Electronics, Inc.

Title  
**Braidwood/ SATA repeater & PCIE SATA SW**

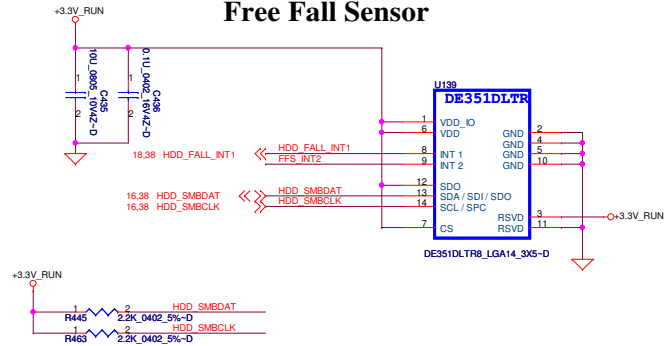
Size Document Number  
**LA-5691P**

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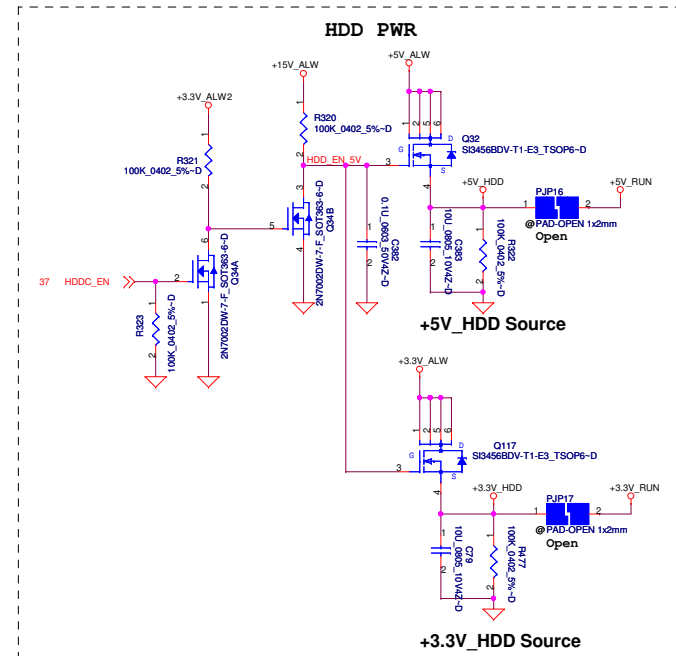
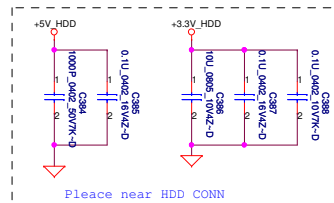
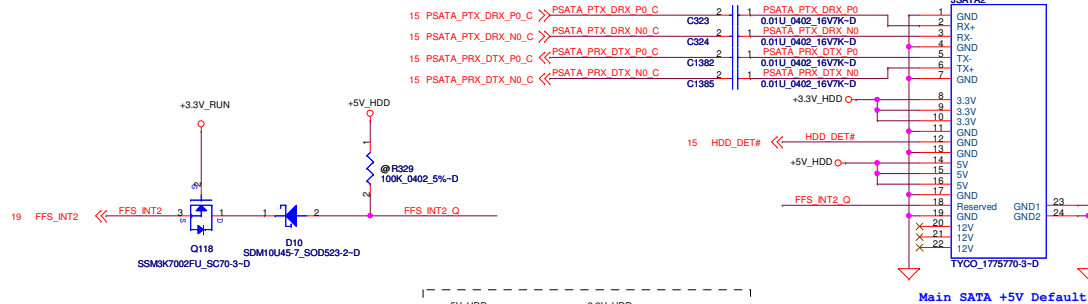
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## Free Fall Sensor



## For HDD



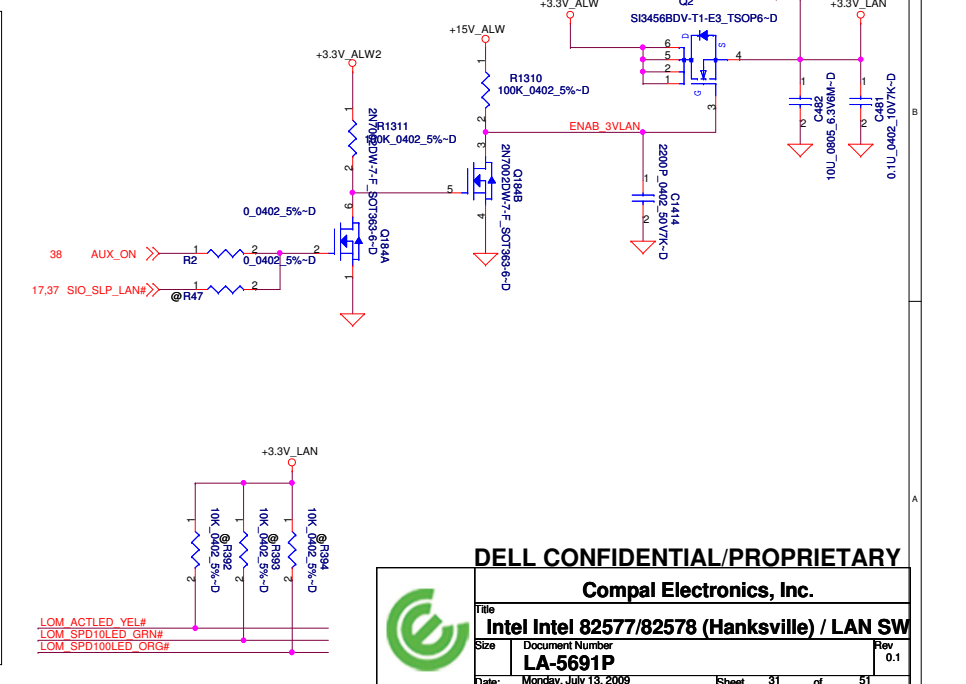
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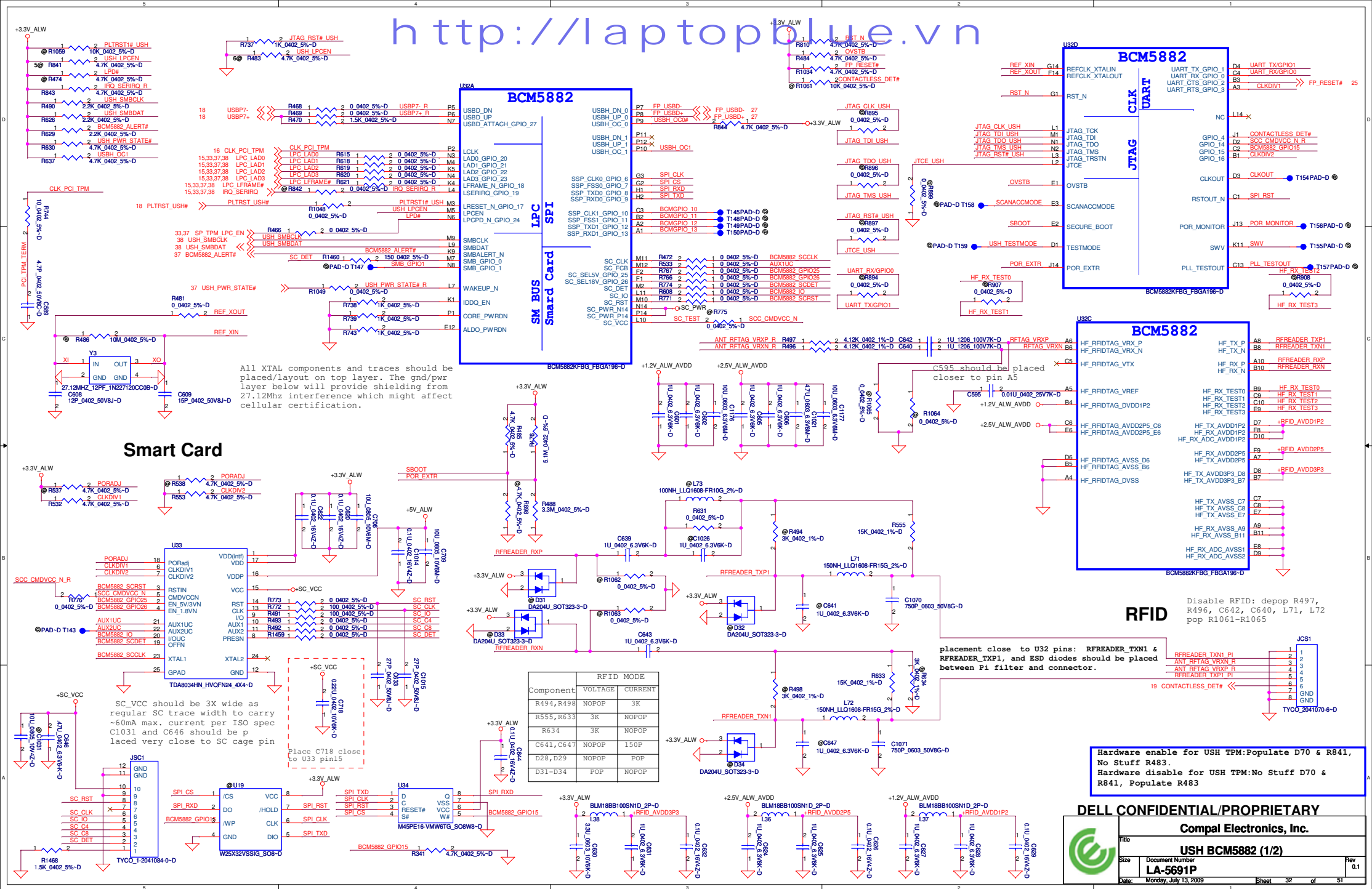
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Size	Document Number	LA-5691P	
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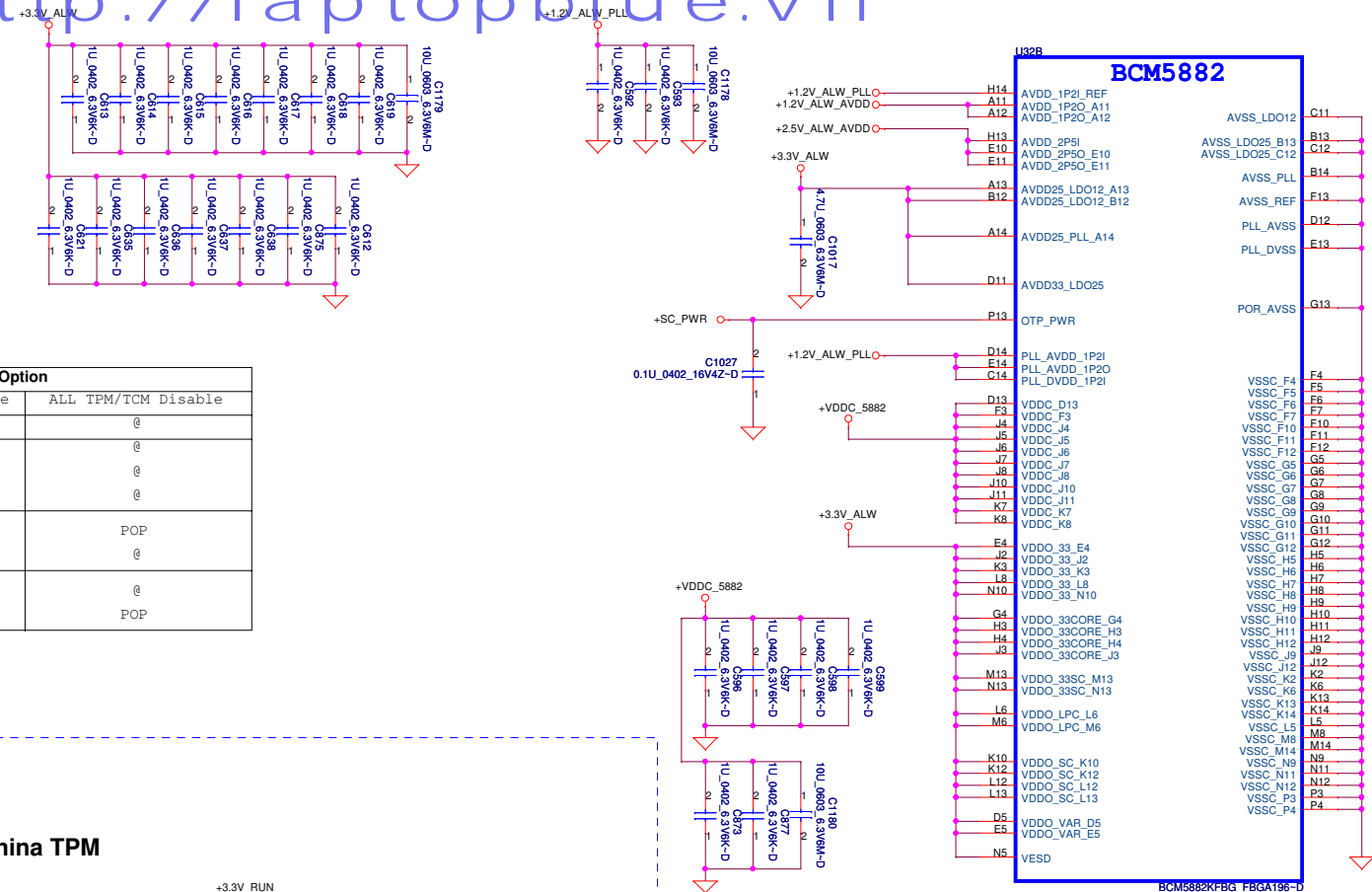




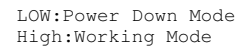




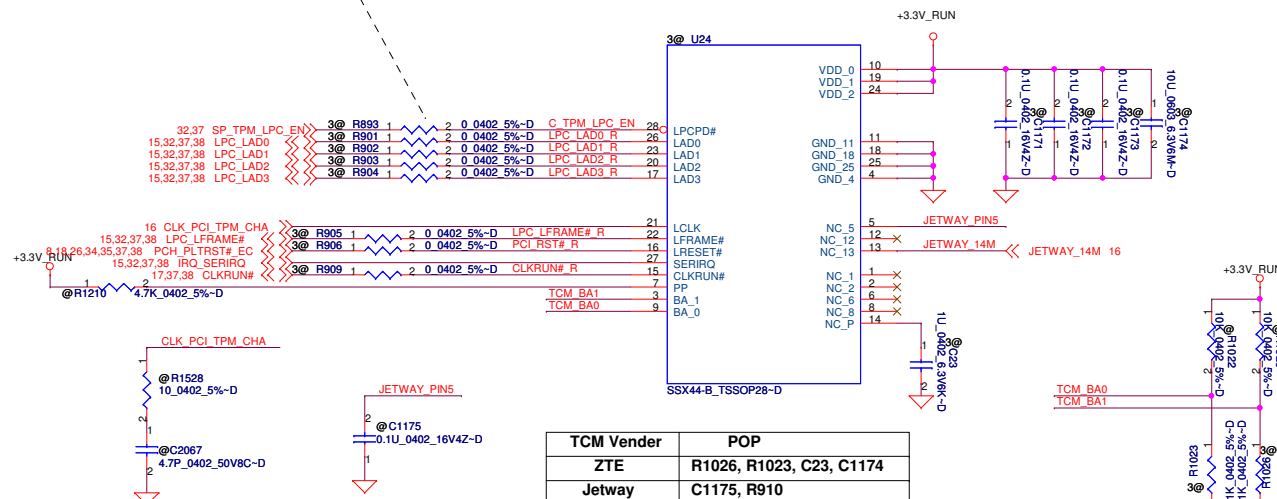




USH BCM5882 and China TPM Z8H172T Option				
PART/PIN	Ref Des	TCM Enable	TPM Enable	ALL TPM/TCM Disable
TCM circuit	All 3@	POP	@	@
SIO 5028 ->SP_TPM_LPC_EN	PU R841	@	POP	@
	PD R483	POP	@	@
	PU R788	@	@	@
PCH GPIO39 ->TPM_ID1	PU R787	@	@	POP
	PD R339	POP	POP	@
PCH GPIO38 ->TPM_ID0	PU R273	POP	POP	@
	PD R922	@	@	POP



## China TPM



TCM Vender	POP
ZTE	R1026, R1023, C23, C1174
Jetway	C1175, R910

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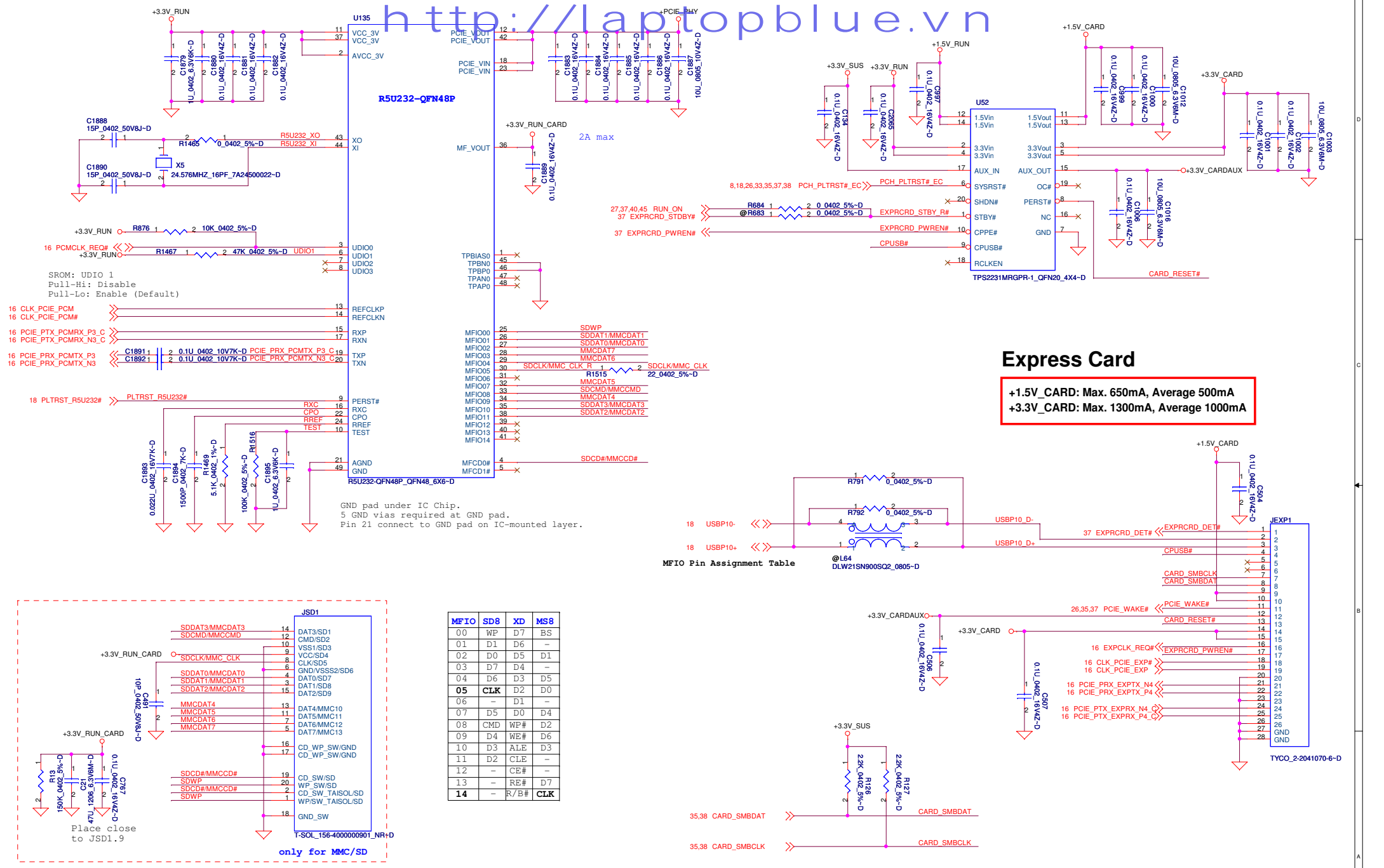
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**USH BCM5882 (2/2)**

**LA-5691P**

Rev	
0.1	



### Express Card

**+1.5V\_CARD: Max. 650mA, Average 500mA**  
**+3.3V\_CARD: Max. 1300mA, Average 1000mA**

MFIO Pin Assignment Table

MFIO	SD8	XD	MS8
00	WP	D7	BS
01	D1	D6	-
02	D0	D5	D1
03	D7	D4	-
04	D6	D3	D5
05	CLK	D2	D0
06	-	D1	-
07	D5	D0	D4
08	CMD	WP#	D2
09	D4	WE#	D6
10	D3	ALE	D3
11	D2	CLE	-
12	-	CE#	-
13	-	RE#	D7
14	-	R/B#	CLK

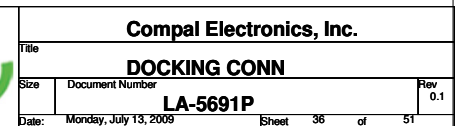
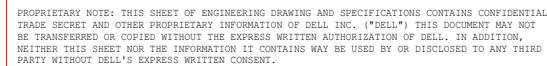
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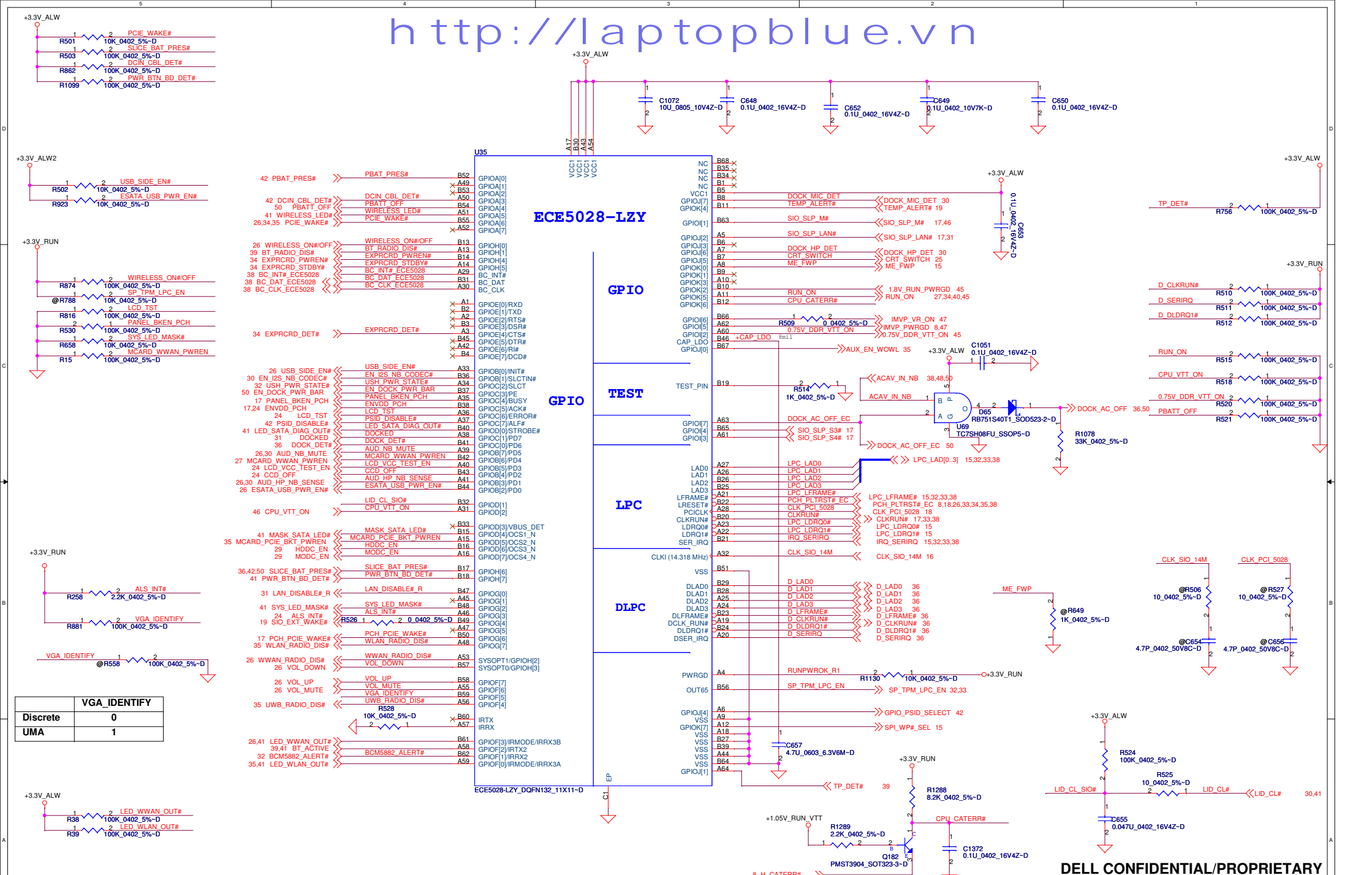
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R5U232			
Size	Document Number		Rev
Custom	LA-5691P		0.1
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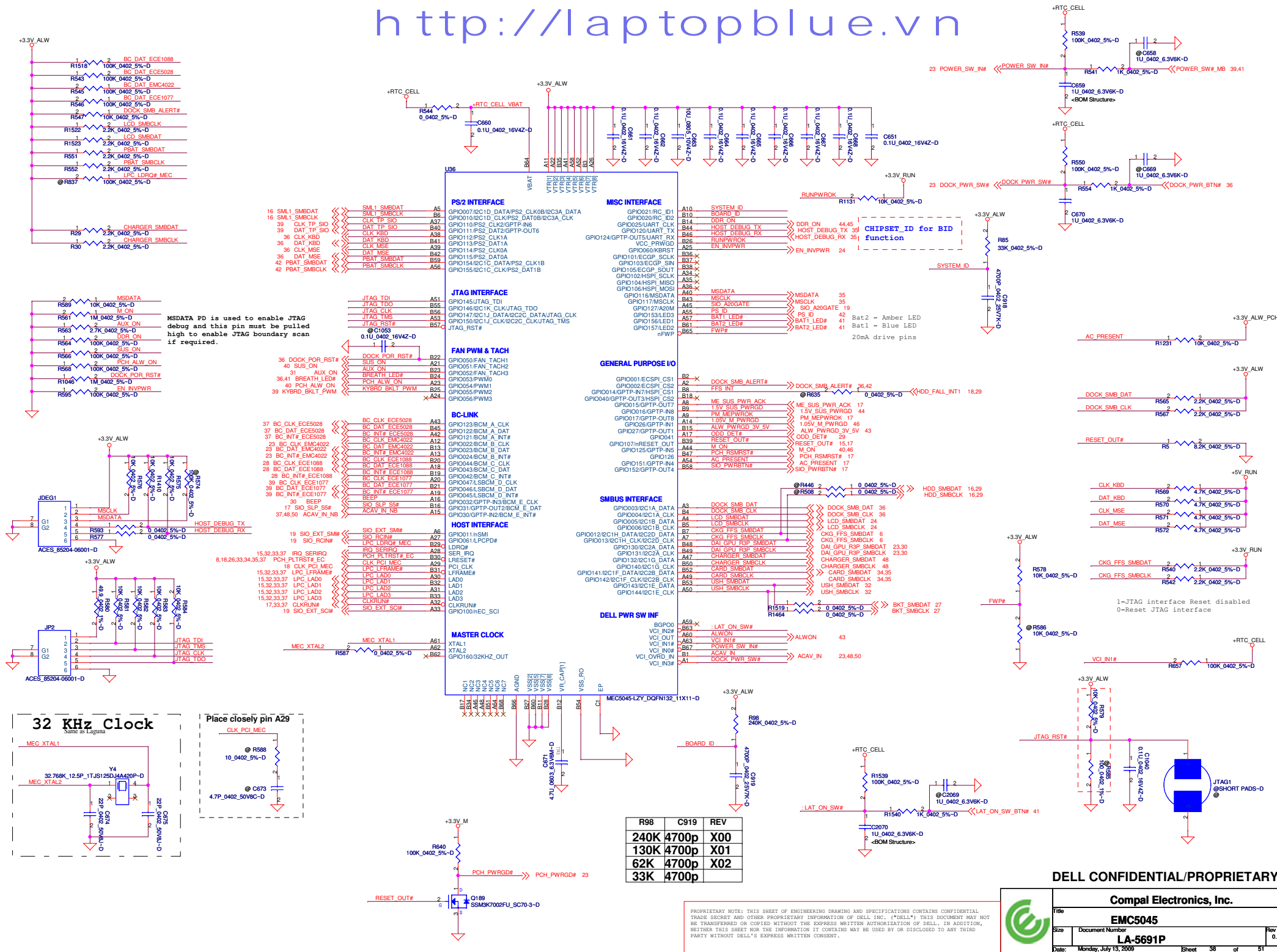
**ECE5028**

**LA-5691P**

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	<b>LA-5691P</b>	0.1
Date:	Monday, July 13, 2009	Sheet 37 of 51

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R98	C919	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	

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		Title	
		EMC5045	
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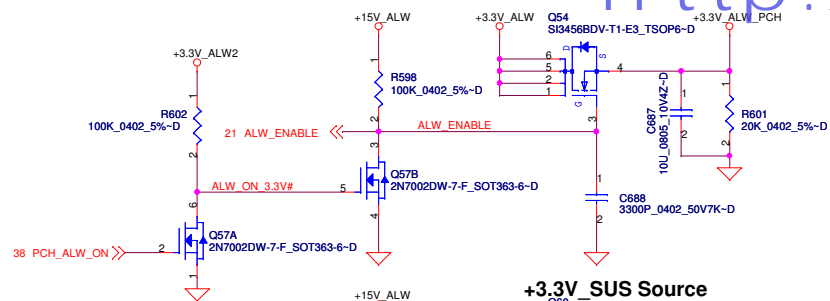
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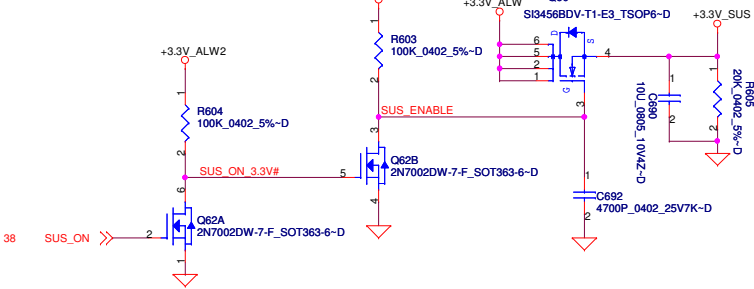


## DC/DC Interface

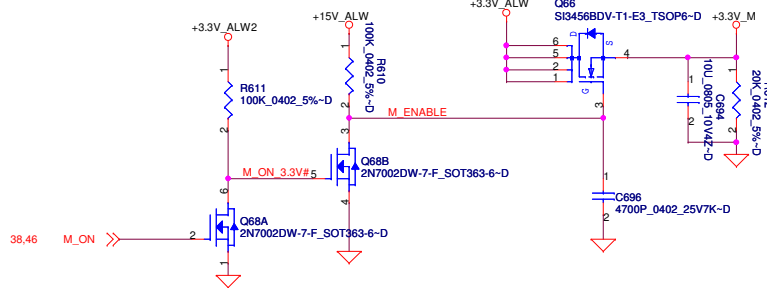
### +3.3V\_ALW\_PCH Source



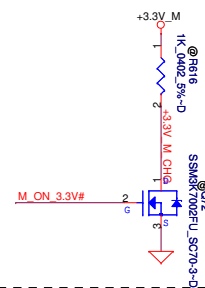
### +3.3V\_SUS Source



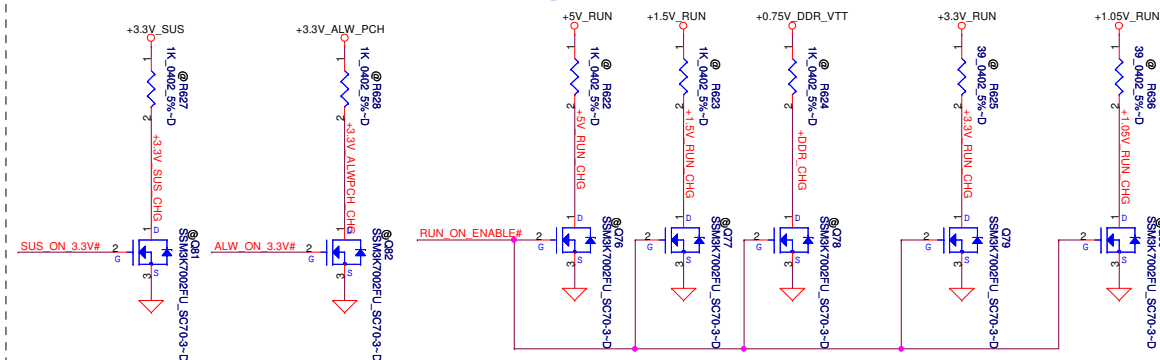
### +3.3VM Source



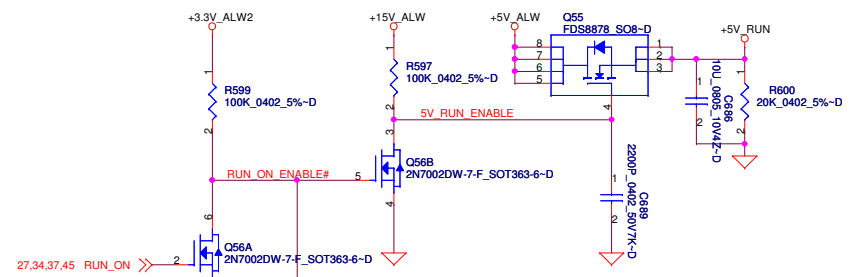
### Discharg Circuit



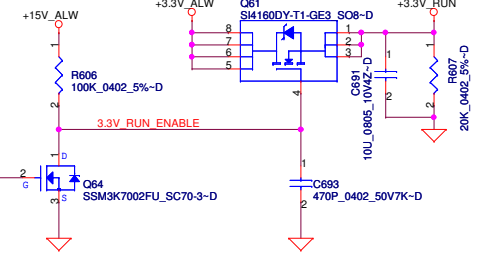
### Discharg Circuit



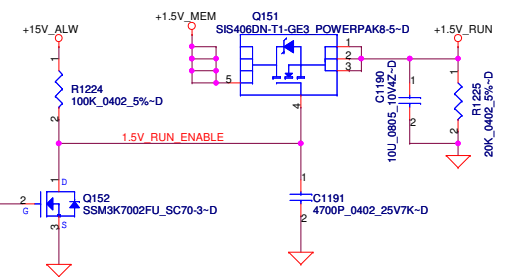
### +5VRUN Source



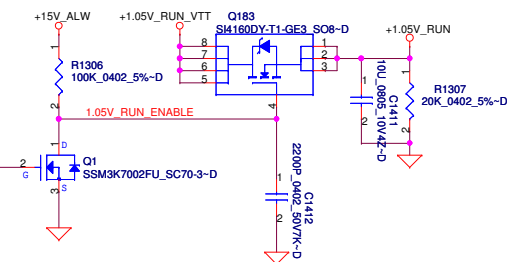
### +3.3V\_RUN Source



### +1.5V\_RUN Source



### +1.05V\_RUN Source



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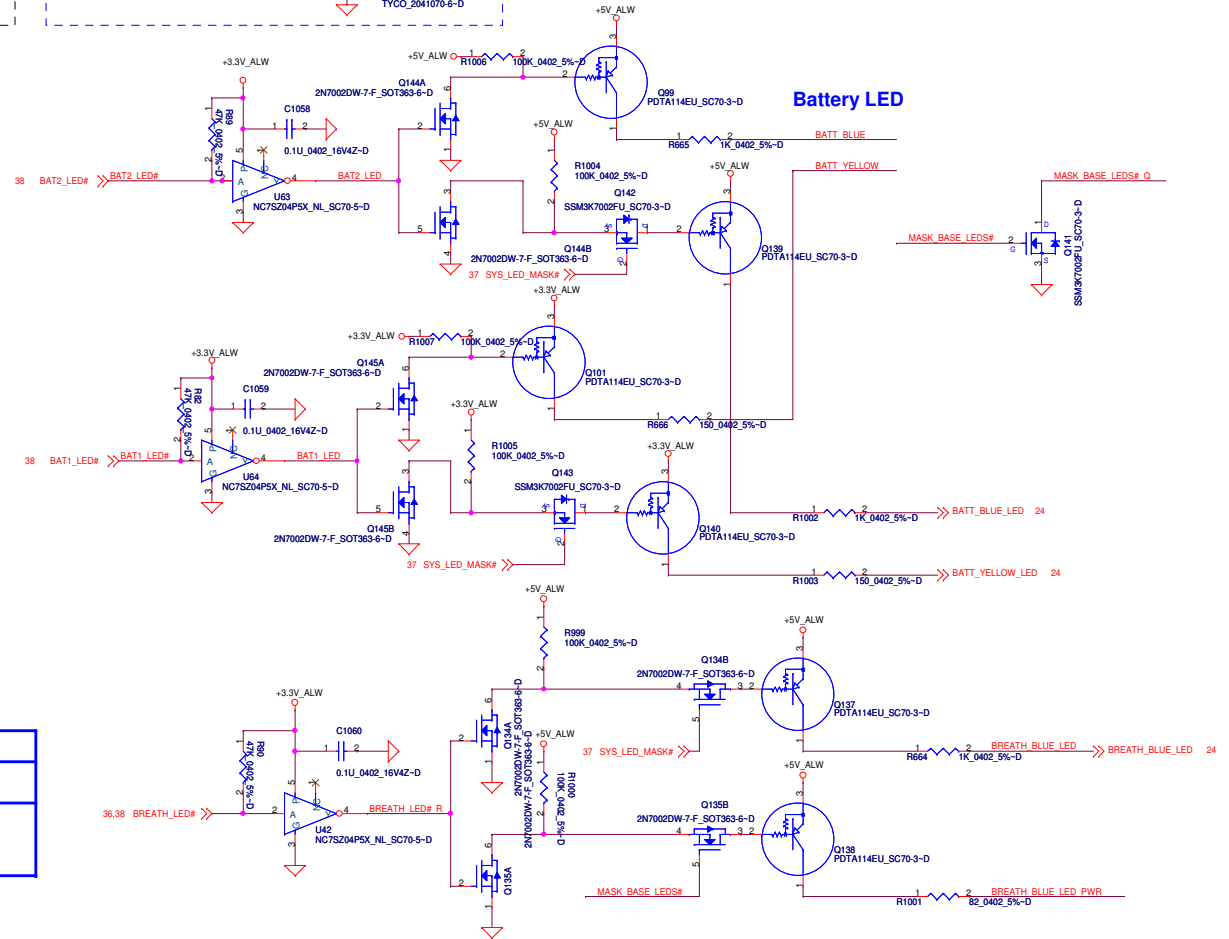
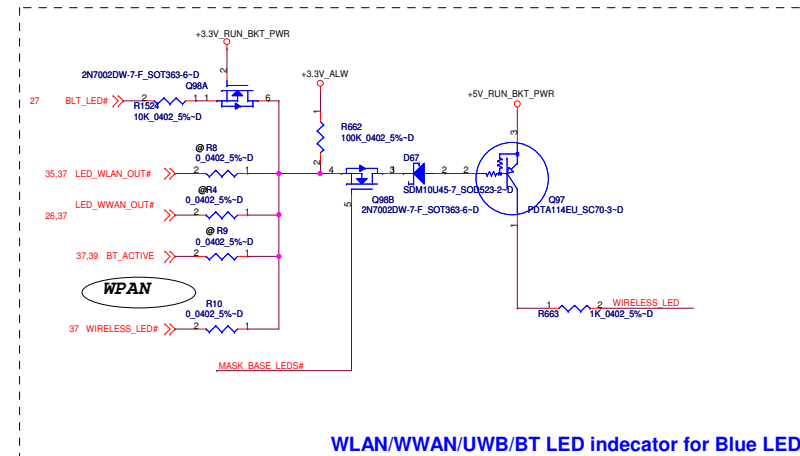
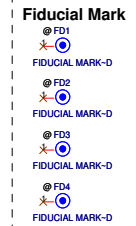
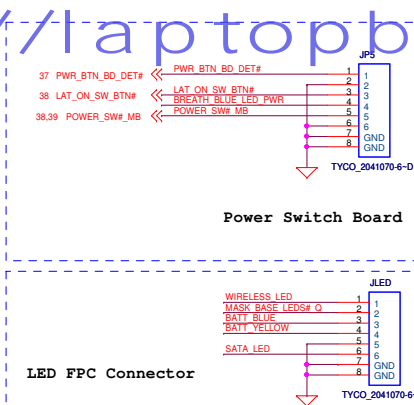
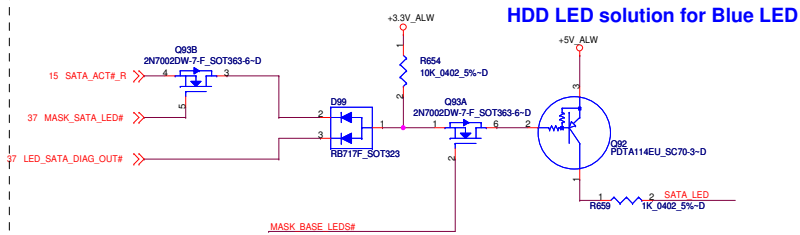
POWER CONTROL

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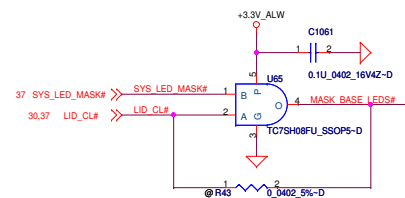
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LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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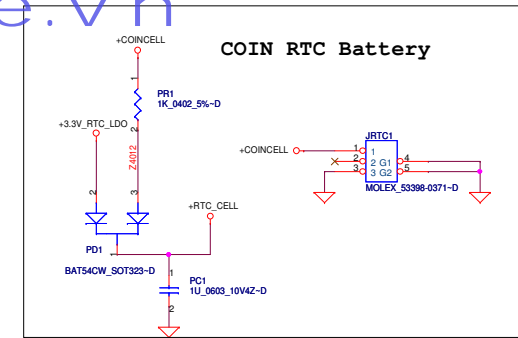
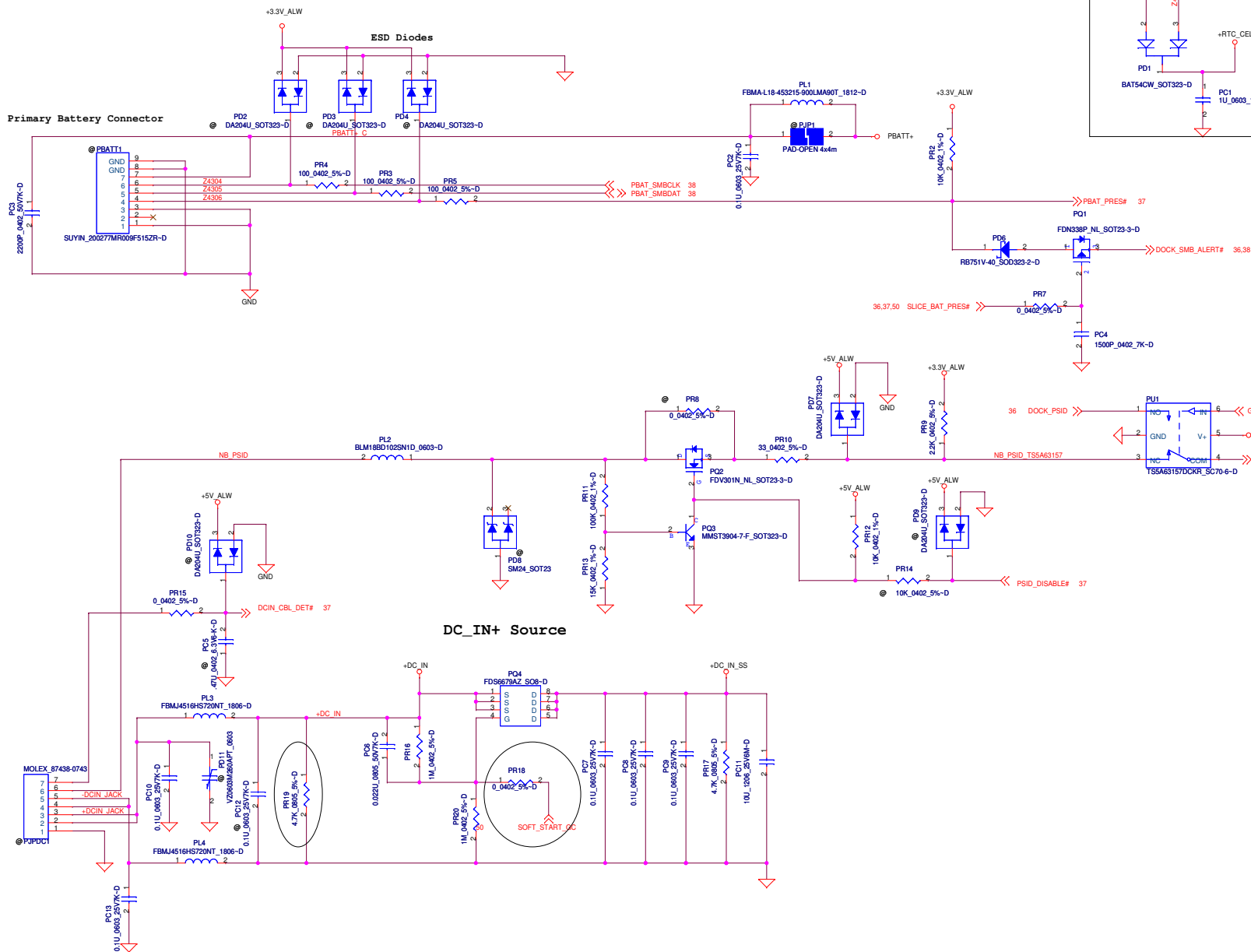
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PAD and Standoff

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+DCIN

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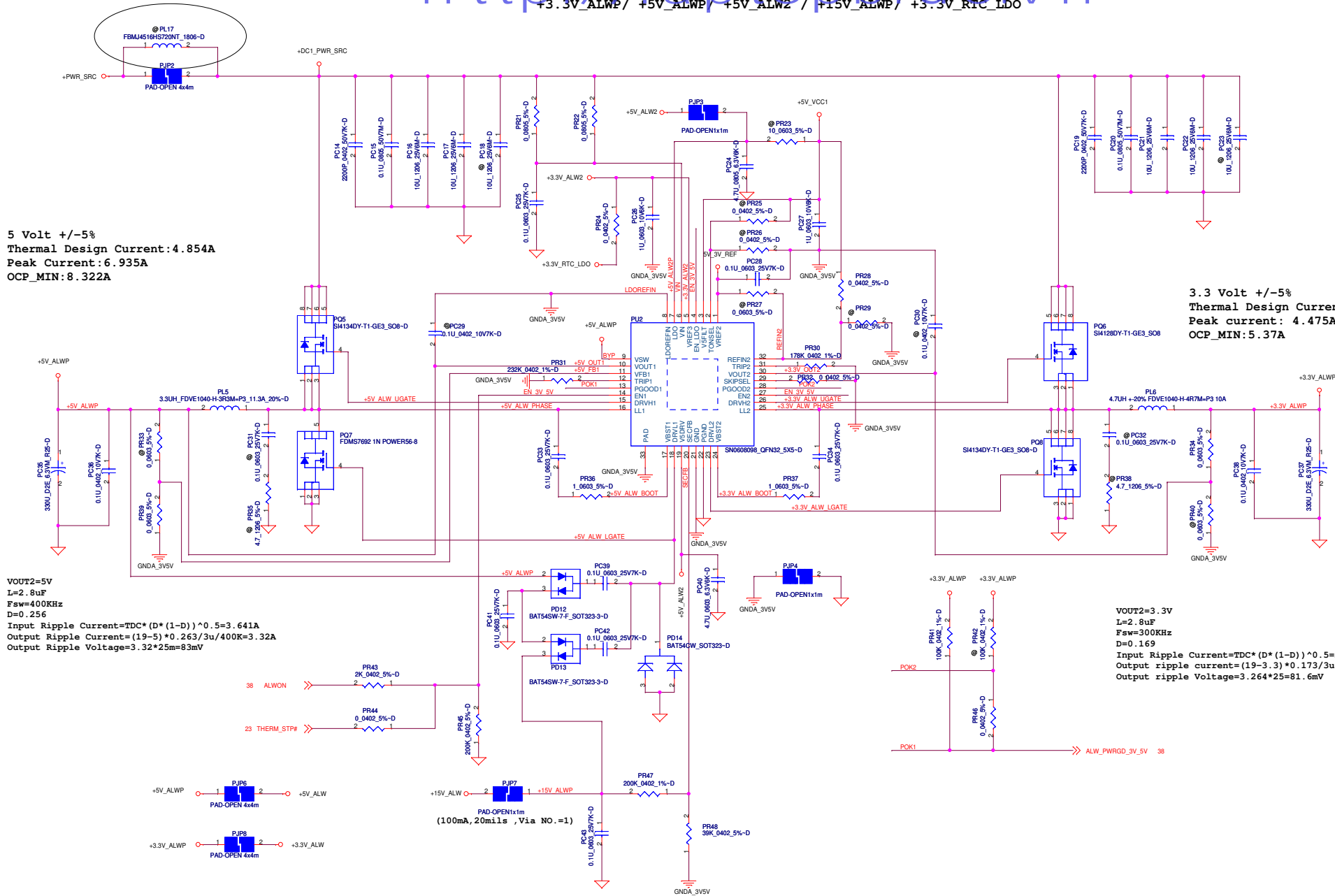
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5 Volt +/-5%  
Thermal Design Current:4.854A  
Peak Current:6.935A  
OCP\_MIN:8.322A


3.3 Volt +/-5%  
Thermal Design Current: 3.133A  
Peak current: 4.475A  
OCP\_MIN:5.37A

VOUT2=5V  
L=2.8uF  
Fsw=400KHz  
D=0.256  
Input Ripple Current= $TDC * (D * (1-D))^{0.5} = 3.641A$   
Output Ripple Current= $(19-5) * 0.263/3u/400K = 3.32A$   
Output Ripple Voltage= $3.32 * 25m = 83mV$

VOUT2=3.3V  
L=2.8uF  
Fsw=300KHz  
D=0.169  
Input Ripple Current= $TDC * (D * (1-D))^{0.5} = 2.051A$   
Output ripple current= $(19-3.3) * 0.173/3u/300K = 3.264A$   
Output ripple Voltage= $3.264 * 25 = 81.6mV$



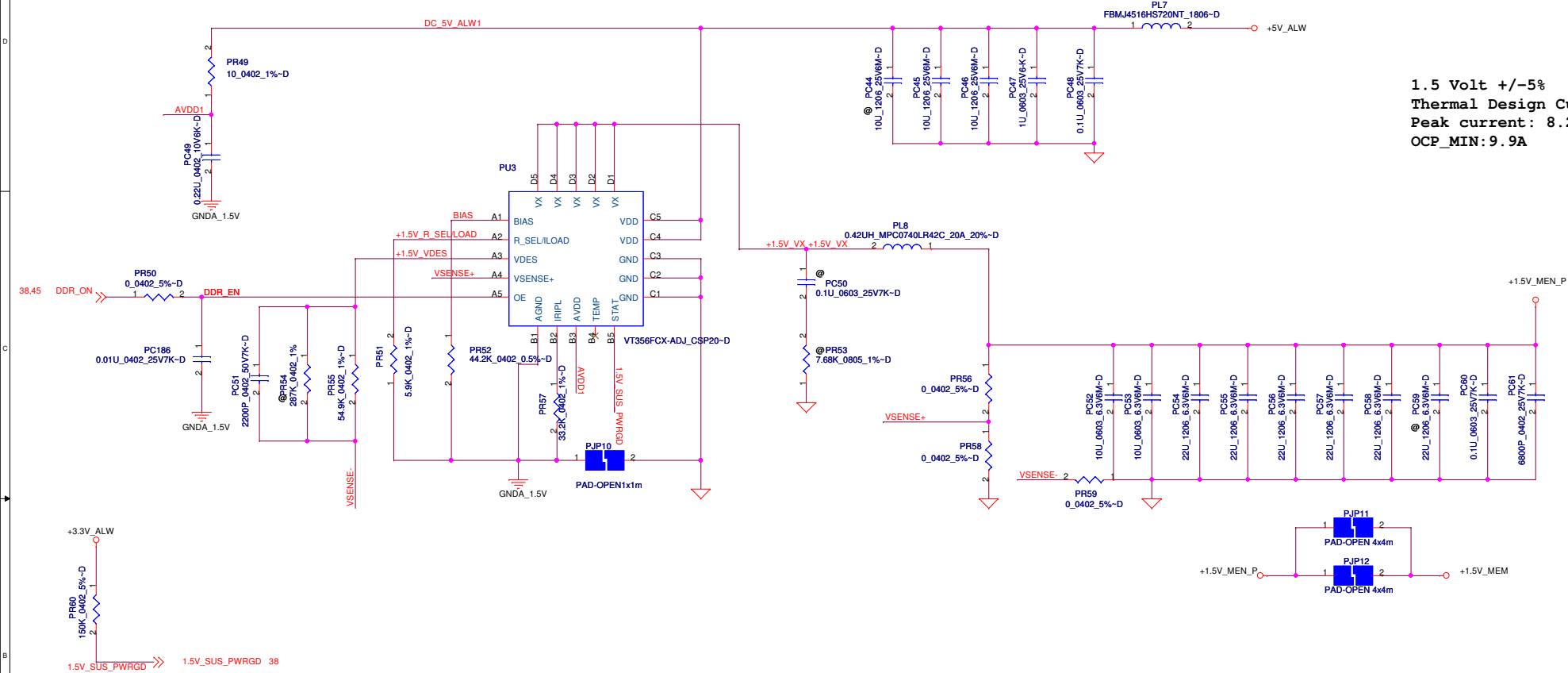
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		DC/DC +3V/ +5V	
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+1.5V\_MEN\_P (VT356)

1.5 Volt +/-5%  
Thermal Design Current: 5.775A  
Peak current: 8.25A  
OCP\_MIN: 9.9A



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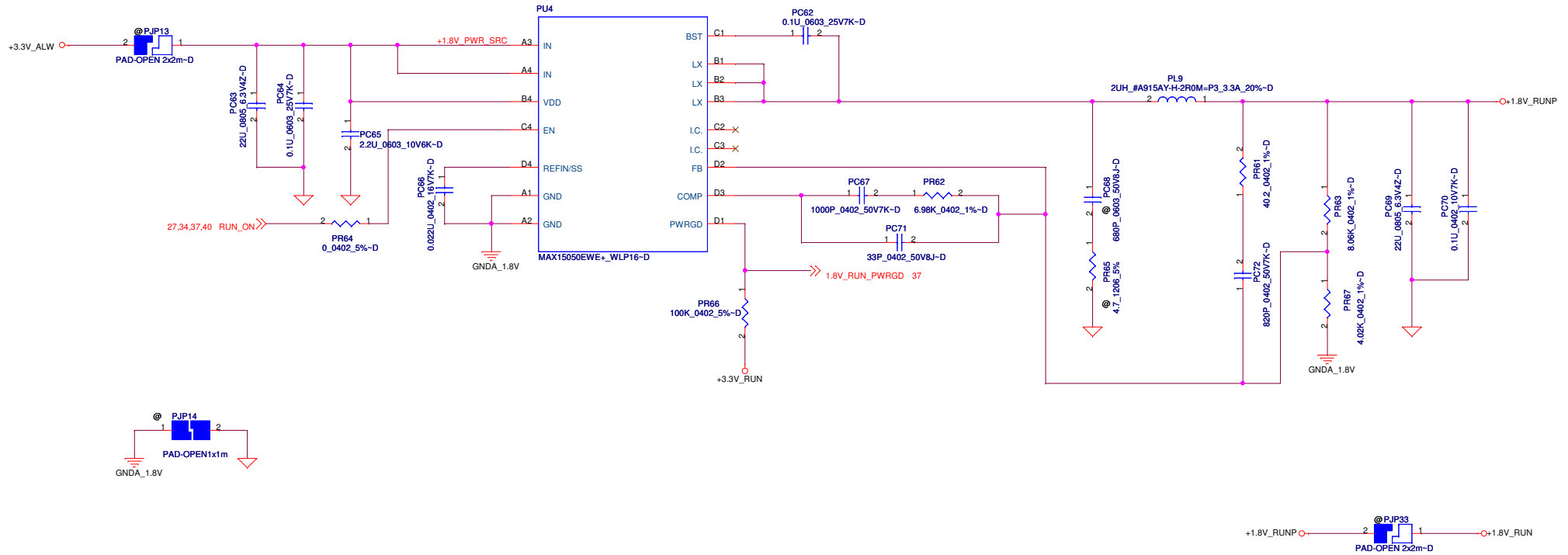
+1.5V\_MEM

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## +1.8V\_RUN

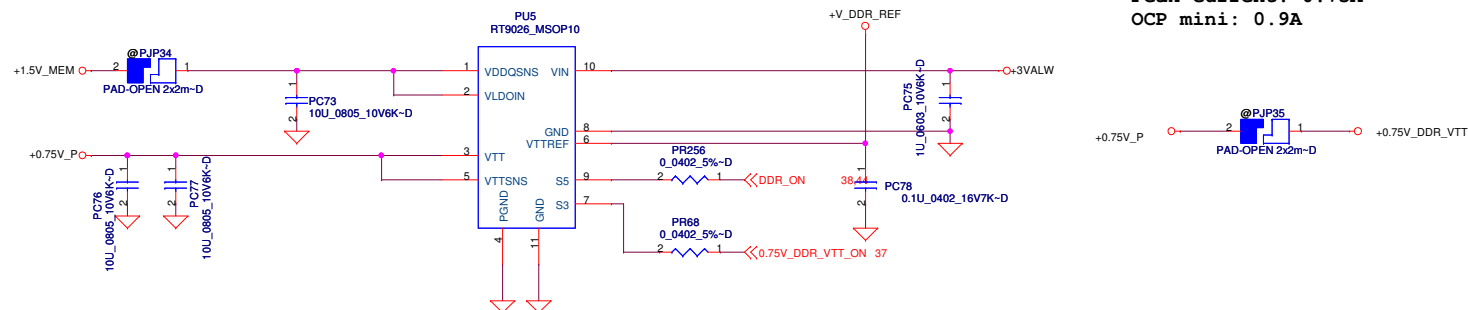
1.8 Volt +/-5%  
Thermal Design Current: 0.894A  
Peak current: 1.277A  
OCP\_min:1.532A



## +0.75V\_DDR\_VTT

DDR3 Termination

0.75Volt +/-5%  
Thermal Design Current: 0.525A  
Peak current: 0.75A  
OCP mini: 0.9A



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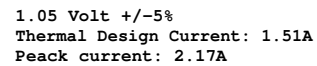
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Title			
+1.8V_RUN/+0.75V_DDR_VT			
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# http://laptopblue.v

1.05 Volt +/-5%  
Thermal Design Current: 1.51A  
Peack current: 2.17A





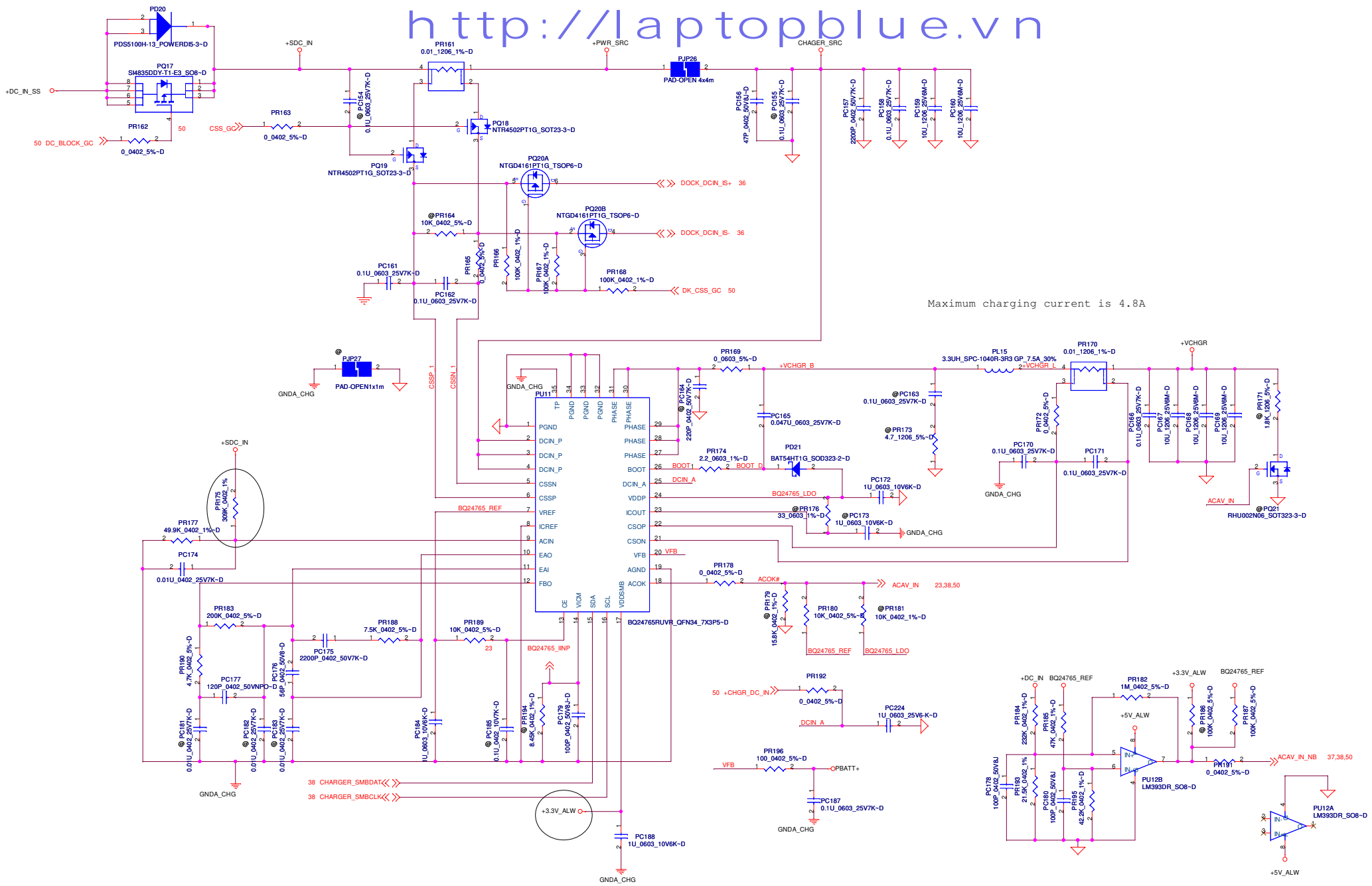
+VCC CORE

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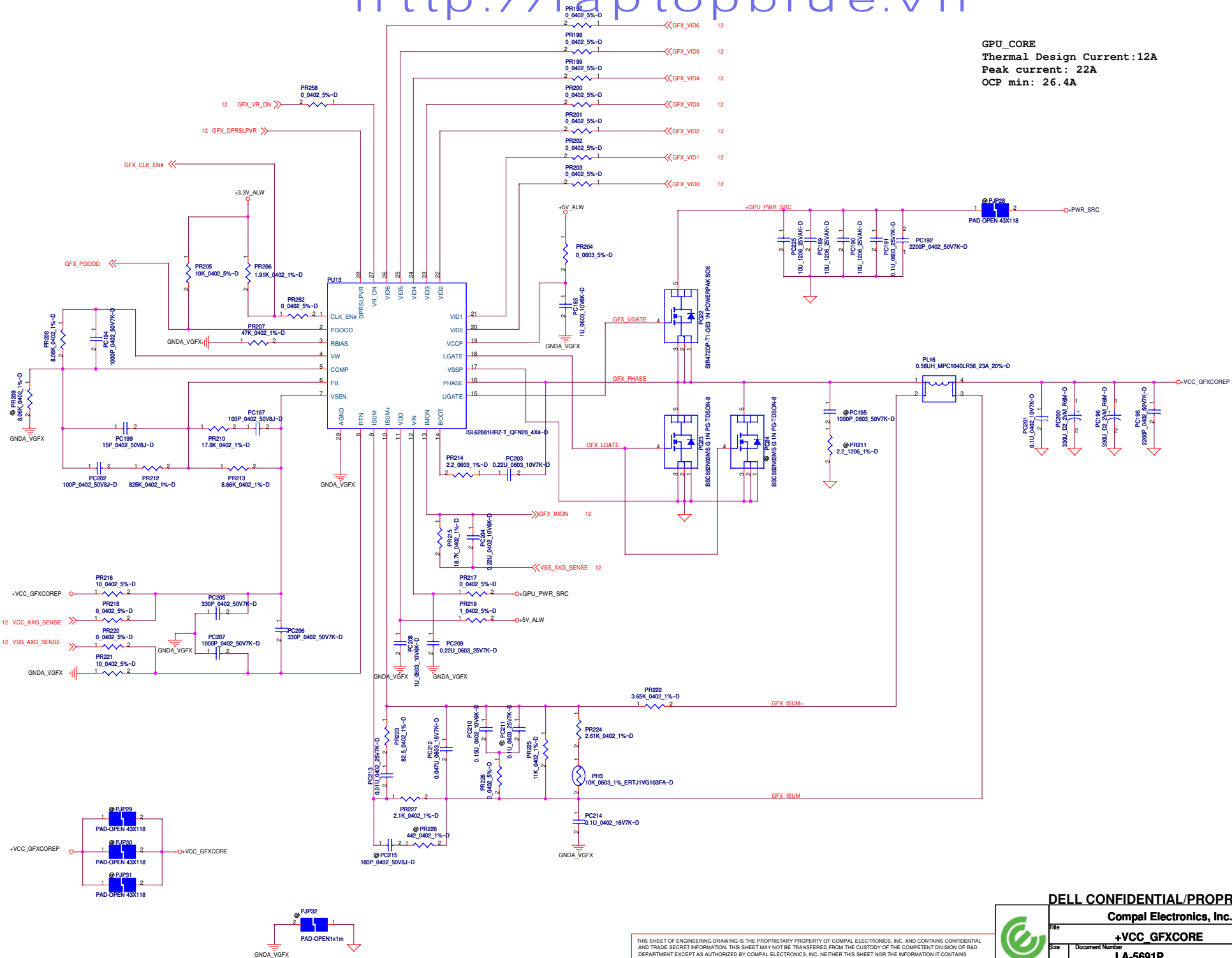




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		Charger	
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```
GPU_CORE
Thermal Design Current:12A
Peak current: 22A
OCP min: 26.4A
```

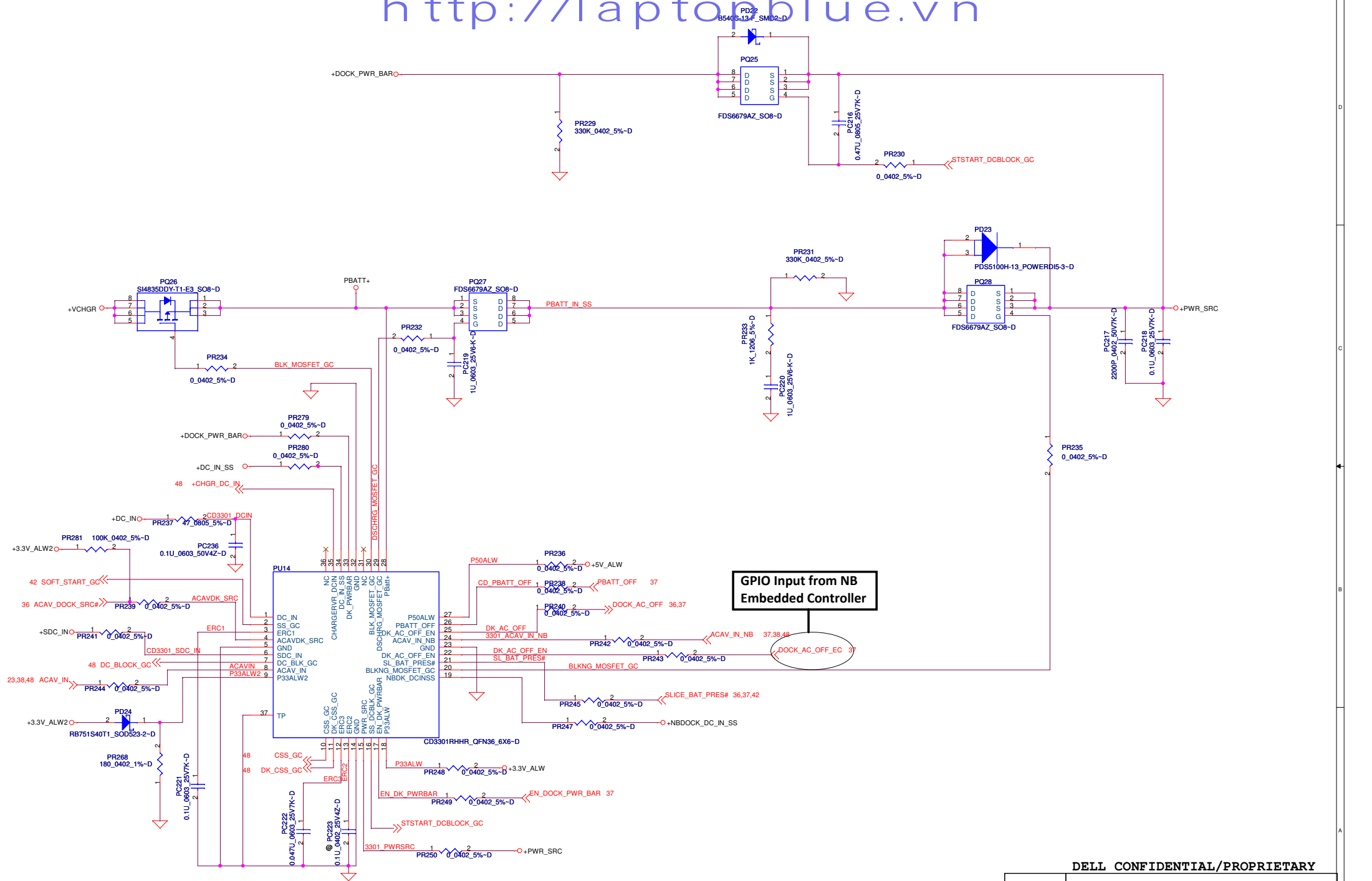
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+VCC\_GFXCORE


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