

**COMPAL CONFIDENTIAL**

<http://laptopblue.vn>

**MODEL NAME : JAZ00**

**PCB NO : LA-4291P**

**BOM P/N : 46155331L01**



# MINICOOPER

**uFCBGA Mobile Penryn SFF ULV  
Intel Cantiga GS(High Performance) + ICH9M SFF**

**12-07-2007**

**REV : 0.1(X00)**

**@ : Nopop Component**

**1@ : TAA board Used only**

**2@ : Without TAA board Used only**

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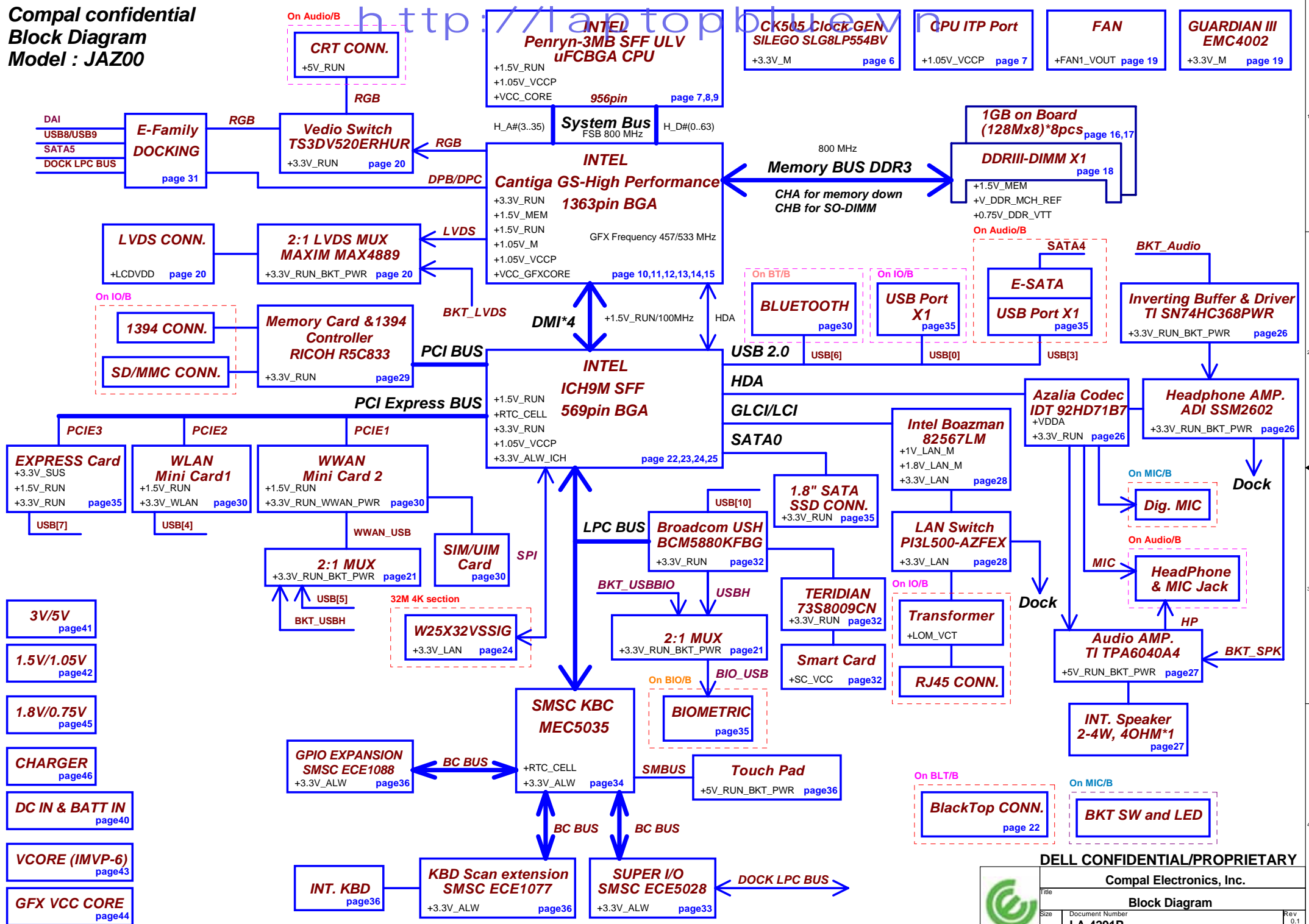
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**Cover sheet**

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**Block Diagram**  
**Model : JAZ00**



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Block Diagram		
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# POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

USB PORT#	DESTINATION
0	JUSB (Ext Right Side)
1	NONE
2	NONE
3	JESATA (Ext Left Side)
4	WLAN
5	WWAN
6	BT
7	Express card
8	DOCKING
9	DOCKING
10	USH->BIO
11	NONE

# PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW +3.3V_ALW_ICH +3.3V_RTC_LDO +1.5V_ALW_HDA	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_GFXCORE +VCC_CORE +1.05V_VCCP	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)	+3.3V_RUN_BKT_PWR +5V_RUN_BKT_PWR +3.3V_RUN_WWAN_PWR +INV_PWR_SRC +LCDVDD	+3.3V_BKT_PWR
S0	ON	ON	ON	ON	ON	ON	OFF
S3	ON	ON	OFF	ON	OFF	OFF	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF	OFF	OFF
BLT mode	ON	OFF	OFF	OFF	OFF	ON	ON

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-2 WWAN
Lane 2	MINI CARD-1 WLAN
Lane 3	None
Lane 4	EXPRESS CARD
Lane 5	None
Lane 6	Giga LAN

# PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	AD17	REQ#1 / GNT#1	PIRQ[C..D]

SATA	DESTINATION
SATA0	SSD
SATA1	None
SATA4	ESATA
SATA5	DOCKING

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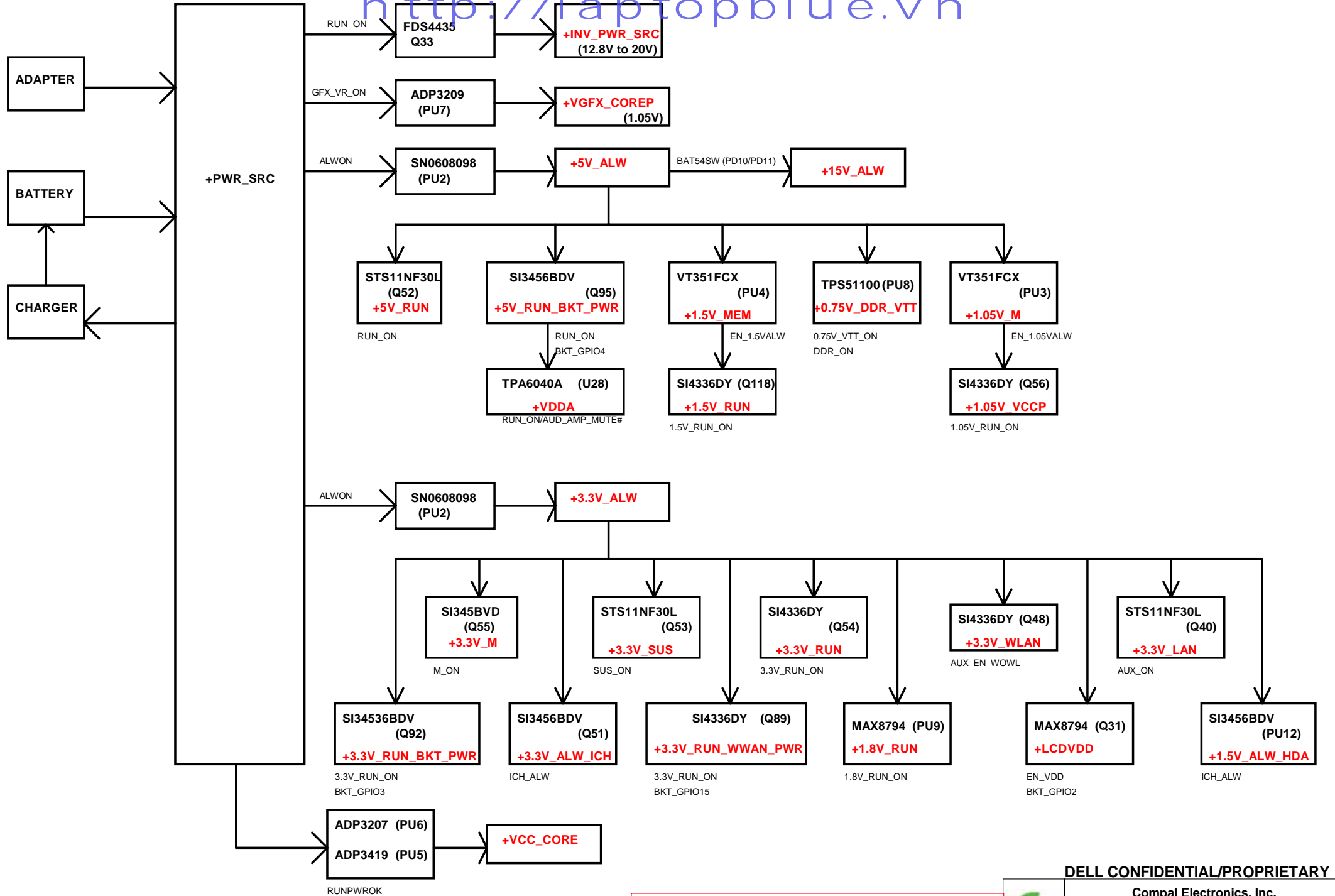
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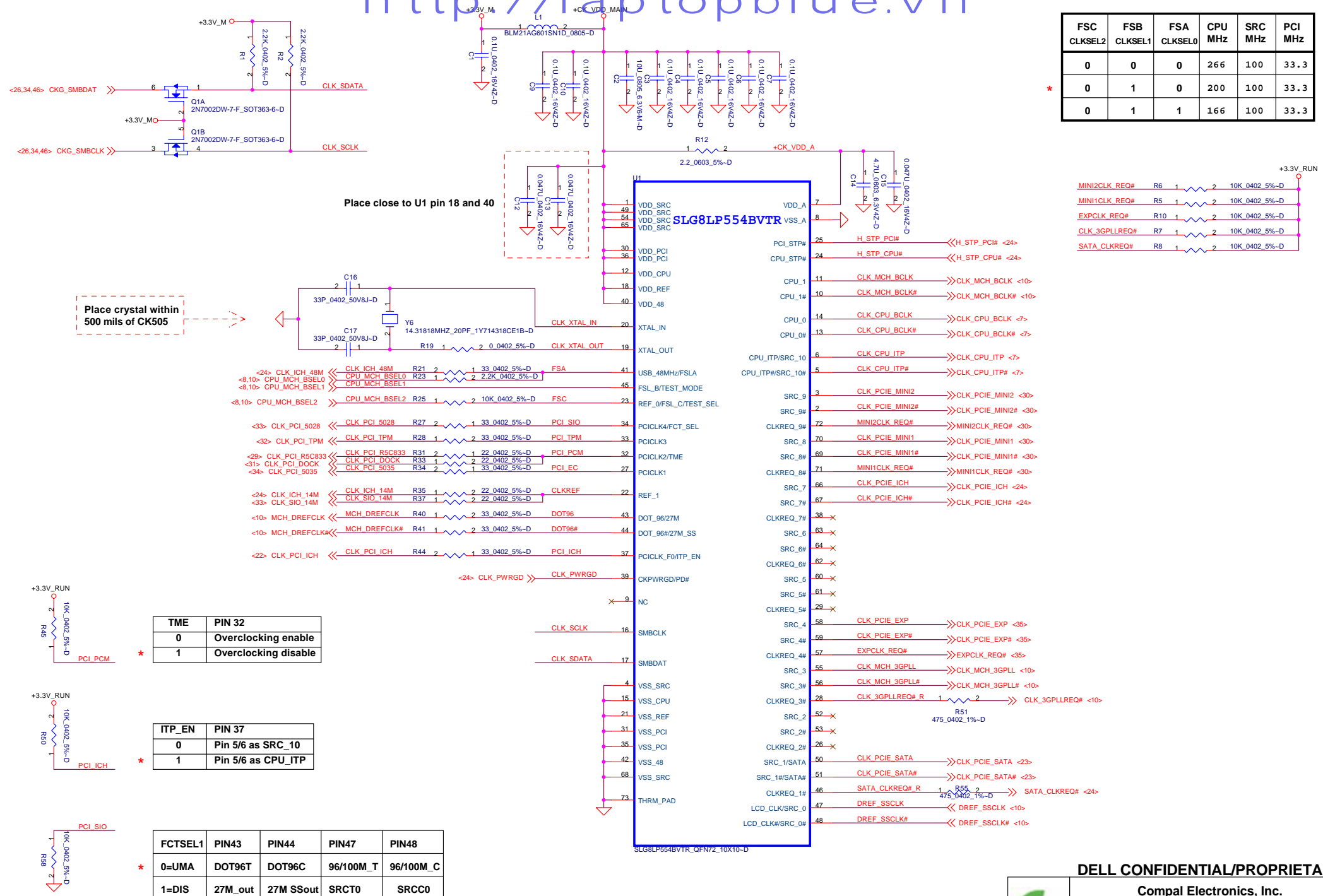
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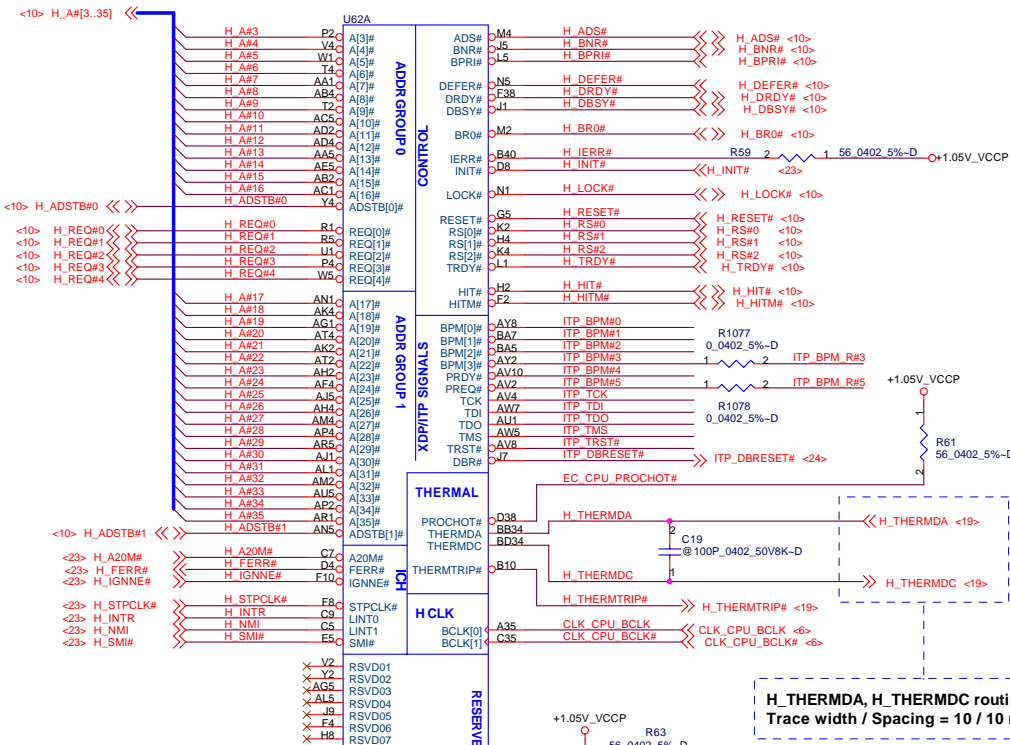
Title Power Rails

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Place close to J1TP within 100 mil

Place close to J1TP within 100 mil

Place close to J1TP within 1ns = 5000 mil

Place close to J1TP within 200ps = 1000 mil

Place close to CPU within 200 mil

Place close to CPU within 200ps = 1000 mil

Layout Note: for ITP700Flex debug port with a XDP based Run Control Tools

ITP\_BPM#[0..5], TCK, and TMS routings must be a maximum of 1.5ns = 7500 mil

ITP\_BPM#[0..5], and TCK to FBO routings must be length matched to within 50ps = 250 mil

Place R70 close to J1TP pin 5  
TCK to FBO routing should refer to debug port design guide  
H\_RESET# should be routed from GMCH with split to ITP conn. Refer to DG page #56

Depop J1TP, C18, R68, R70, R64, R67, R69 when JIP connector is depopulated

H\_THERMDA, H\_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

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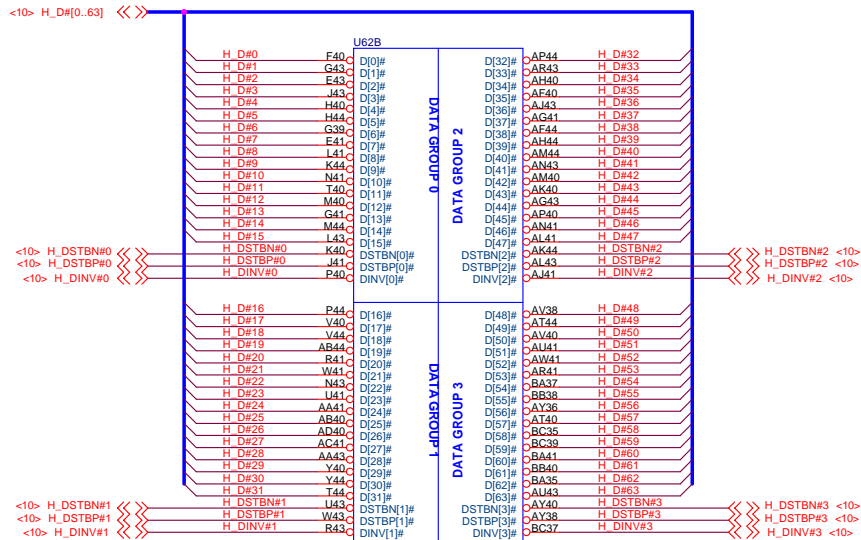
Penryn SFF ULV Processor(1/3)

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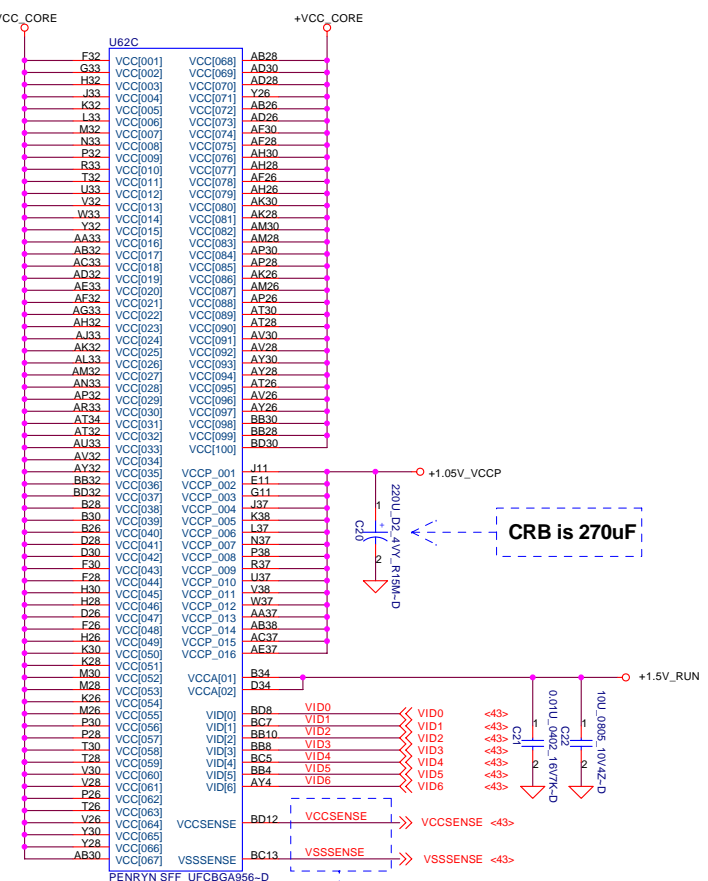
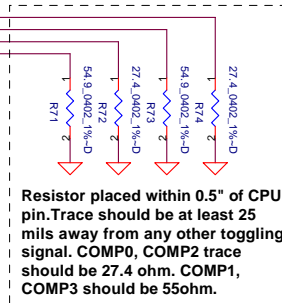
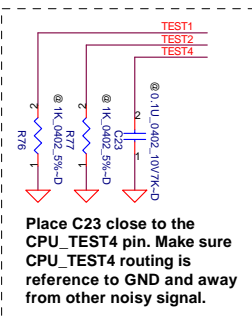
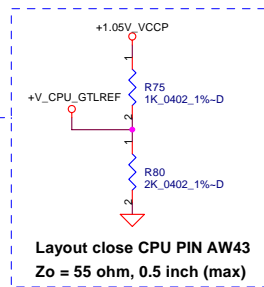
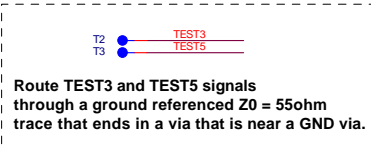
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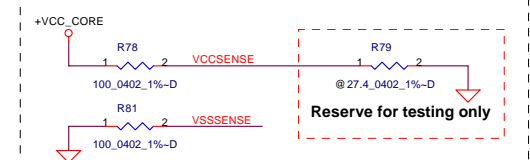


FSB	BCLK	BSEL2	BSEL1	BSEL0
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0



Length match within 25 mils, Z0=27.4 ohm

Place R78 and R81 close to CPU within 1000 mil



Route VCCSENSE and VSSSENSE trace at 27.4 ohms with 7 mil spacing

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U62F			U62E		
+VCC_CORE	BD28	VCC_101	VCCP_021	AL37	+1.05V_VCCP
BB26	VCC_102	VCCP_022	AN37		
BD26	VCC_103	VCCP_023	AP38		
B22	VCC_104	VCCP_024	C33		
B24	VCC_105	VCCP_025	D32		
D22	VCC_106	VCCP_026	D32		
D24	VCC_107	VCCP_027	E35		
L24	VCC_108	VCCP_028	F34		
F22	VCC_109	VCCP_029	G35		
H24	VCC_110	VCCP_030	H36		
H22	VCC_111	VCCP_031	I36		
K24	VCC_112	VCCP_032	J35		
K22	VCC_113	VCCP_033	K36		
M24	VCC_114	VCCP_034	L35		
M22	VCC_115	VCCP_035	N35		
M24	VCC_116	VCCP_036	O36		
P22	VCC_117	VCCP_037	P35		
T24	VCC_118	VCCP_038	U35		
T22	VCC_119	VCCP_039	W36		
V24	VCC_120	VCCP_040	X35		
V22	VCC_121	VCCP_041	Y36		
Y24	VCC_122	VCCP_042	AA35		
Y22	VCC_123	VCCP_043	AB36		
AB24	VCC_124	VCCP_044	AC35		
AB22	VCC_125	VCCP_045	AD36		
AD24	VCC_126	VCCP_046	AE35		
AD22	VCC_127	VCCP_047	AF36		
AF24	VCC_128	VCCP_048	AG35		
AF22	VCC_129	VCCP_049	AH36		
AH24	VCC_130	VCCP_050	AI35		
AH22	VCC_131	VCCP_051	AJ36		
AK24	VCC_132	VCCP_052	AK35		
AK22	VCC_133	VCCP_053	AL36		
AM24	VCC_134	VCCP_054	AM35		
AM22	VCC_135	VCCP_055	AN36		
AP24	VCC_136	VCCP_056	AO35		
AP22	VCC_137	VCCP_057	AP36		
AT24	VCC_138	VCCP_058	AQ35		
AT22	VCC_139	VCCP_059	AR36		
AV24	VCC_140	VCCP_060	AS35		
AV22	VCC_141	VCCP_061	AT36		
AY24	VCC_142	VCCP_062	AU35		
AY22	VCC_143	VCCP_063	AV36		
BB24	VCC_144	VCCP_064	AW35		
BB22	VCC_145	VCCP_065	AX36		
BD24	VCC_146	VCCP_066	AY35		
BD22	VCC_147	VCCP_067	AZ36		
B18	VCC_148	VCCP_068	BA35		
B20	VCC_149	VCCP_069	BB36		
D16	VCC_150	VCCP_070	BC35		
D18	VCC_151	VCCP_071	BD36		
F18	VCC_152	VCCP_072	BE35		
F16	VCC_153	VCCP_073	BF36		
H16	VCC_154	VCCP_074	BG35		
H18	VCC_155	VCCP_075	BH36		
D20	VCC_156	VCCP_076	BI35		
F20	VCC_157	VCCP_077	BJ36		
H20	VCC_158	VCCP_078	BK35		
K18	VCC_159	VCCP_079	BL36		
K16	VCC_160	VCCP_080	BM35		
M18	VCC_161	VCCP_081	BN36		
M16	VCC_162	VCCP_082	BO35		
M20	VCC_163	VCCP_083	BP36		
P18	VCC_164	VCCP_084	BQ35		
P16	VCC_165	VCCP_085	BR36		
P18	VCC_166	VCCP_086	BS35		
T18	VCC_167	VCCP_087	BT36		
T16	VCC_168	VCCP_088	BU35		
V18	VCC_169	VCCP_089	BV36		
V16	VCC_170	VCCP_090	BW35		
P20	VCC_171	VCCP_091	BX36		
T20	VCC_172	VCCP_092	BY35		
V20	VCC_173	VCCP_093	BZ36		
Y18	VCC_174	VCCP_094	CA35		
Y16	VCC_175	VCCP_095	CB36		
AB18	VCC_176	VCCP_096	CC35		
AB16	VCC_177	VCCP_097	CD36		
AD18	VCC_178	VCCP_098	CE35		
AD16	VCC_179	VCCP_099	CF36		
Y20	VCC_180	VCCP_100	CG35		
AB20	VCC_181	VCCP_101	CH36		
AD20	VCC_182	VCCP_102	CI35		
AF16	VCC_183	VCCP_103	CK36		
AF18	VCC_184	VCCP_104	CL35		
AH16	VCC_185	VCCP_105	CM36		
AH18	VCC_186	VCCP_106	CN35		
AF20	VCC_187	VCCP_107	CO36		
AH20	VCC_188	VCCP_108	CP35		
AK18	VCC_189	VCCP_109	CQ36		
AK16	VCC_190	VCCP_110	CR35		
AM18	VCC_191	VCCP_111	CS36		
AM16	VCC_192	VCCP_112	CT35		
AP18	VCC_193	VCCP_113	CU36		
AP16	VCC_194	VCCP_114	CV35		
AK20	VCC_195	VCCP_115	AW36		
AM20	VCC_196	VCCP_116	AX35		
AP20	VCC_197	VCCP_117	AY36		
AT18	VCC_198	VCCP_118	AZ35		
AT16	VCC_199	VCCP_119	BA36		
AV18	VCC_200	VCCP_120	BB35		
AV16	VCC_201	VCCP_121	BC36		
AY18	VCC_202	VCCP_122	BD35		
AY16	VCC_203	VCCP_123	BE36		
AT20	VCC_204	VCCP_124	BF35		
AV20	VCC_205	VCCP_125	BG36		
AY20	VCC_206	VCCP_126	BH35		
BB18	VCC_207	VCCP_127	BI36		
BB16	VCC_208	VCCP_128	BJ35		
BD18	VCC_209	VCCP_129	BK36		
BD16	VCC_210	VCCP_130	BL35		
BD20	VCC_211	VCCP_131	BM36		
AM14	VCC_212	VCCP_132	BN35		
AP14	VCC_213	VCCP_133	BO36		
AT14	VCC_214	VCCP_134	BP35		
AV14	VCC_215	VCCP_135	BQ36		
AY14	VCC_216	VCCP_136	BR35		
BB14	VCC_217	VCCP_137	BS36		
BD14	VCC_218	VCCP_138	BT35		
	VCC_219	VCCP_139	BU36		
	VCC_220	VCCP_140	BV35		
		VCCP_141	BW36		
		VCCP_142	BX35		
		VCCP_143	BY36		
		VCCP_144	BZ35		
		VCCP_145	CA36		

+1.05V\_VCCP

AF38

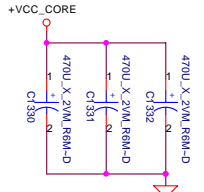
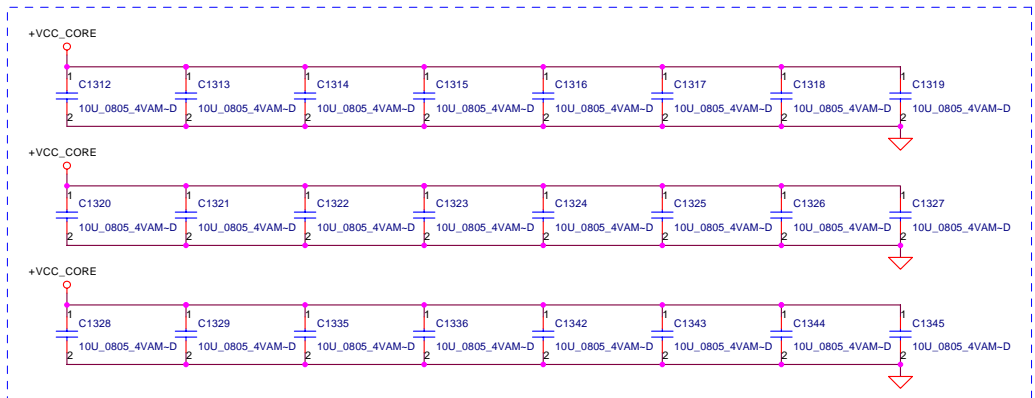
AG37

AK38

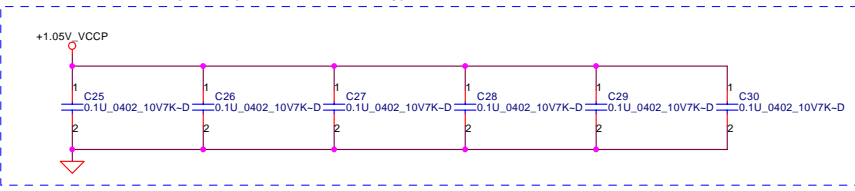
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U62E		
G35	VSS_162	VSS_280
G36	VSS_163	VSS_281
G37	VSS_164	VSS_282
G38	VSS_165	VSS_283
G39	VSS_166	VSS_284
H35	VSS_167	VSS_285
H36	VSS_168	VSS_286
H37	VSS_169	VSS_287
H38	VSS_170	VSS_288
H39	VSS_171	VSS_289
I35	VSS_172	VSS_290
I36	VSS_173	VSS_291
I37	VSS_174	VSS_292
I38	VSS_175	VSS_293
I39	VSS_176	VSS_294
J35	VSS_177	VSS_295
J36	VSS_178	VSS_296
J37	VSS_179	VSS_297
J38	VSS_180	VSS_298
J39	VSS_181	VSS_299
K35	VSS_182	VSS_300
K36	VSS_183	VSS_301
K37	VSS_184	VSS_302
K38	VSS_185	VSS_303
K39	VSS_186	VSS_304
L35	VSS_187	VSS_305
L36	VSS_188	VSS_306
L37	VSS_189	VSS_307
L38	VSS_190	VSS_308
L39	VSS_191	VSS_309
M35	VSS_192	VSS_310
M36	VSS_193	VSS_311
M37	VSS_194	VSS_312
M38	VSS_195	VSS_313
M39	VSS_196	VSS_314
N35	VSS_197	VSS_315
N36	VSS_198	VSS_316
N37	VSS_199	VSS_317
N38	VSS_200	VSS_318
N39	VSS_201	VSS_319
O35	VSS_202	VSS_320
O36	VSS_203	VSS_321
O37	VSS_204	VSS_322
O38	VSS_205	VSS_323
O39	VSS_206	VSS_324
P35	VSS_207	VSS_325
P36	VSS_208	VSS_326
P37	VSS_209	VSS_327
P38	VSS_210	VSS_328
P39	VSS_211	VSS_329
Q35	VSS_212	VSS_330
Q36	VSS_213	VSS_331
Q37	VSS_214	VSS_332
Q38	VSS_215	VSS_333
Q39	VSS_216	VSS_334
R35	VSS_217	VSS_335
R36	VSS_218	VSS_336
R37	VSS_219	VSS_337
R38	VSS_220	VSS_338
R39	VSS_221	VSS_339
S35	VSS_222	VSS_340
S36	VSS_223	VSS_341
S37	VSS_224	VSS_342
S38	VSS_225	VSS_343
S39	VSS_226	VSS_344
T35	VSS_227	VSS_345
T36	VSS_228	VSS_346
T37	VSS_229	VSS_347
T38	VSS_230	VSS_348
T39	VSS_231	VSS_349
U35	VSS_232	VSS_350
U36	VSS_233	VSS_351
U37	VSS_234	VSS_352
U38	VSS_235	VSS_353
U39	VSS_236	VSS_354
V35	VSS_237	VSS_355
V36	VSS_238	VSS_356
V37	VSS_239	VSS_357
V38	VSS_240	VSS_358
V39	VSS_241	VSS_359
W35	VSS_242	VSS_360
W36	VSS_243	VSS_361
W37	VSS_244	VSS_362
W38	VSS_245	VSS_363
W39	VSS_246	VSS_364
X35	VSS_247	VSS_365
X36	VSS_248	VSS_366
X37	VSS_249	VSS_367
X38	VSS_250	VSS_368
X39	VSS_251	VSS_369
Y35	VSS_252	VSS_370
Y36	VSS_253	VSS_371
Y37	VSS_254	VSS_372
Y38	VSS_255	VSS_373
Y39	VSS_256	VSS_374
Z35	VSS_257	VSS_375
Z36	VSS_258	VSS_376
Z37	VSS_259	VSS_377
Z38	VSS_260	VSS_378
Z39	VSS_261	VSS_379
AA35	VSS_262	VSS_380
AA36	VSS_263	VSS_381
AA37	VSS_264	VSS_382
AA38	VSS_265	VSS_383
AA39	VSS_266	VSS_384
AB35	VSS_267	VSS_385
AB36	VSS_268	VSS_386
AB37	VSS_269	VSS_387
AB38	VSS_270	VSS_388
AB39	VSS_271	VSS_389
AC35	VSS_272	VSS_390
AC36	VSS_273	VSS_391
AC37	VSS_274	VSS_392
AC38	VSS_275	VSS_393
AC39	VSS_276	VSS_394
AD35	VSS_277	VSS_395
AD36	VSS_278	VSS_396
AD37	VSS_279	VSS_397

PENRYN SFF\_UFCBGA956-D



Place these inside cavity on L8(North side Secondary)



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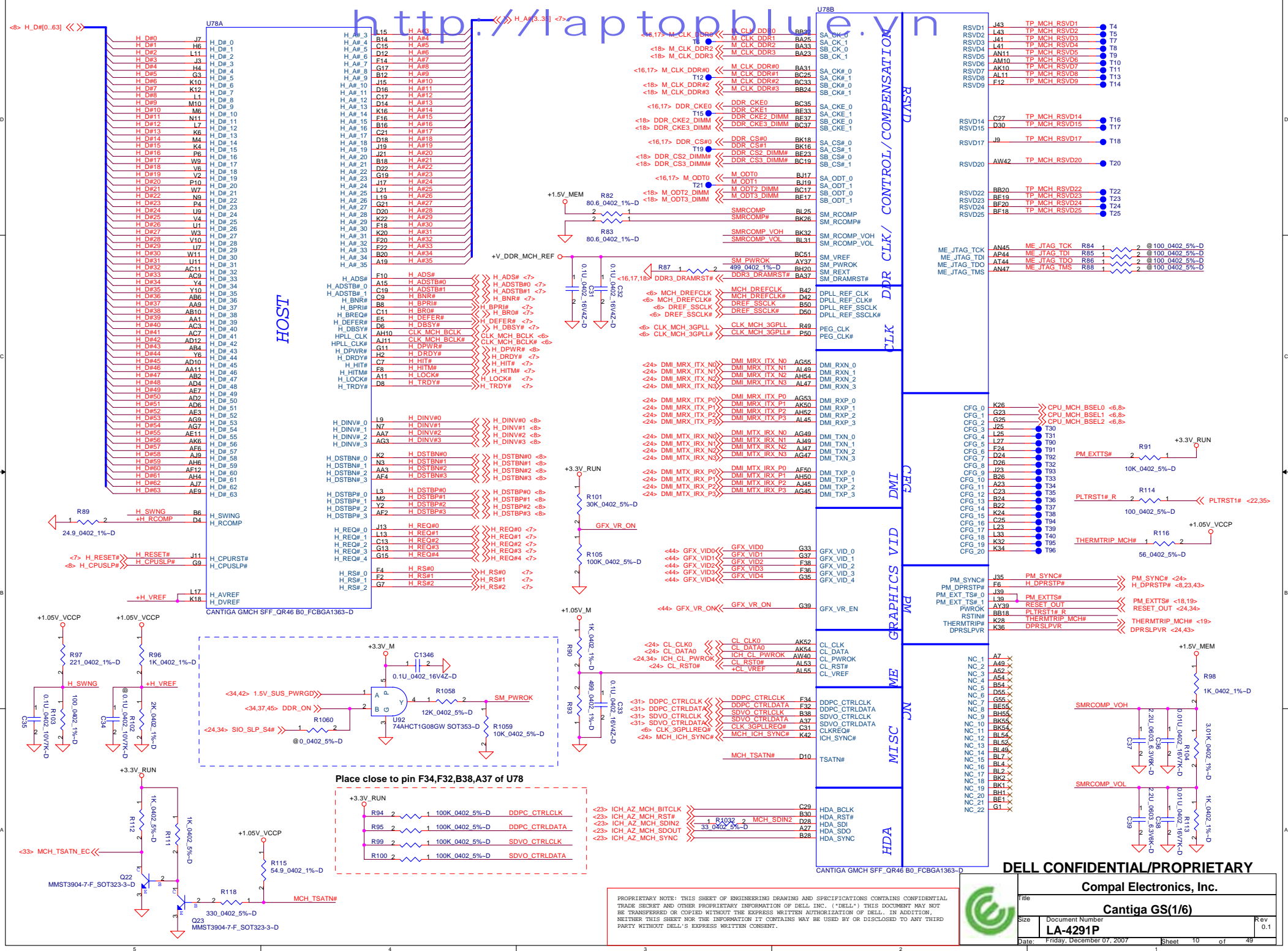
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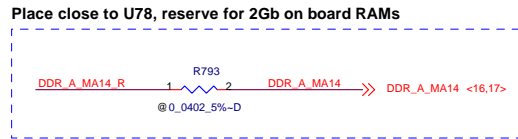
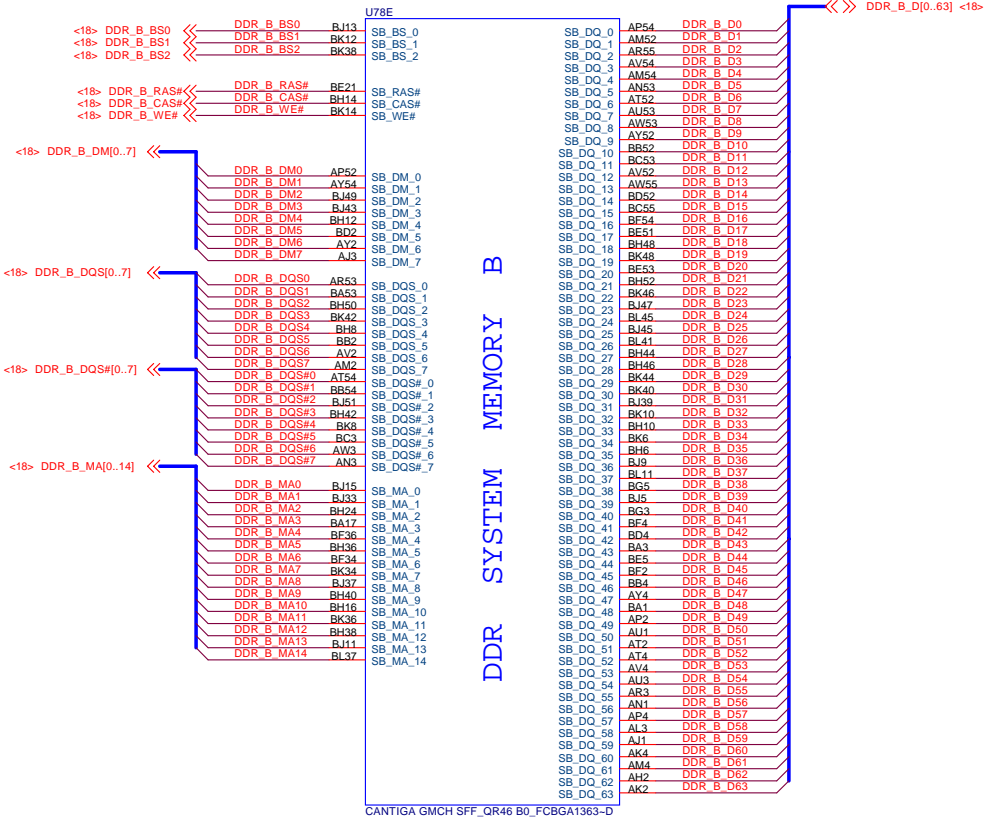
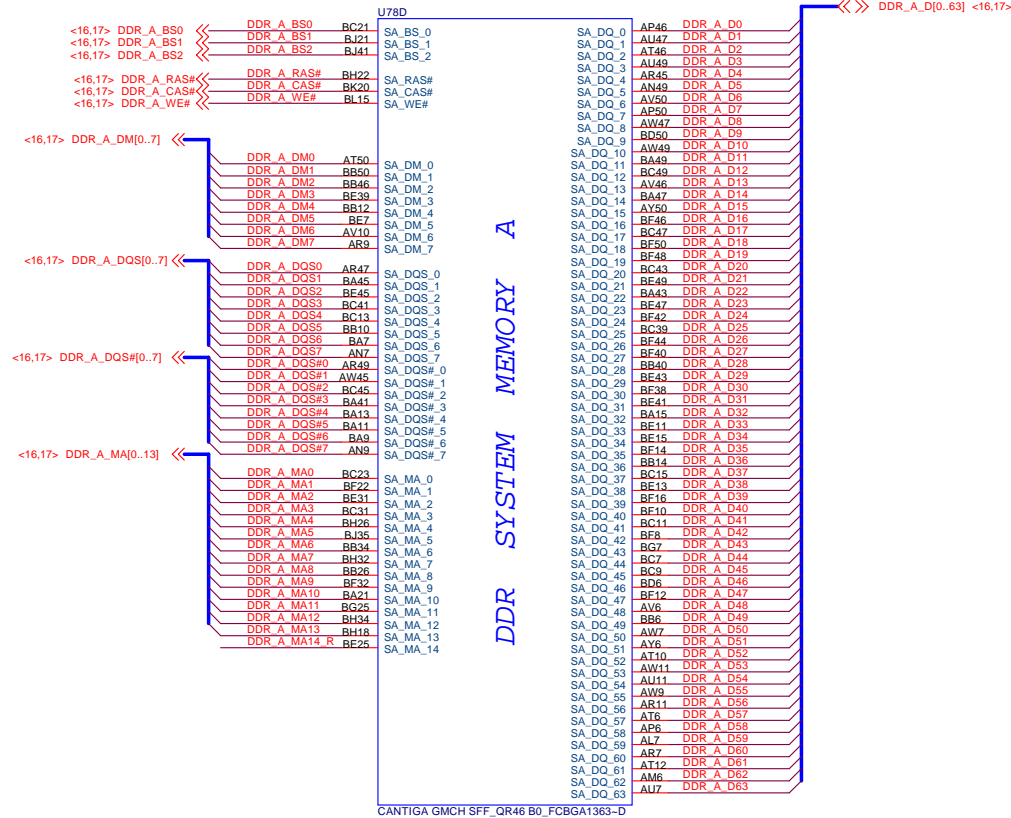
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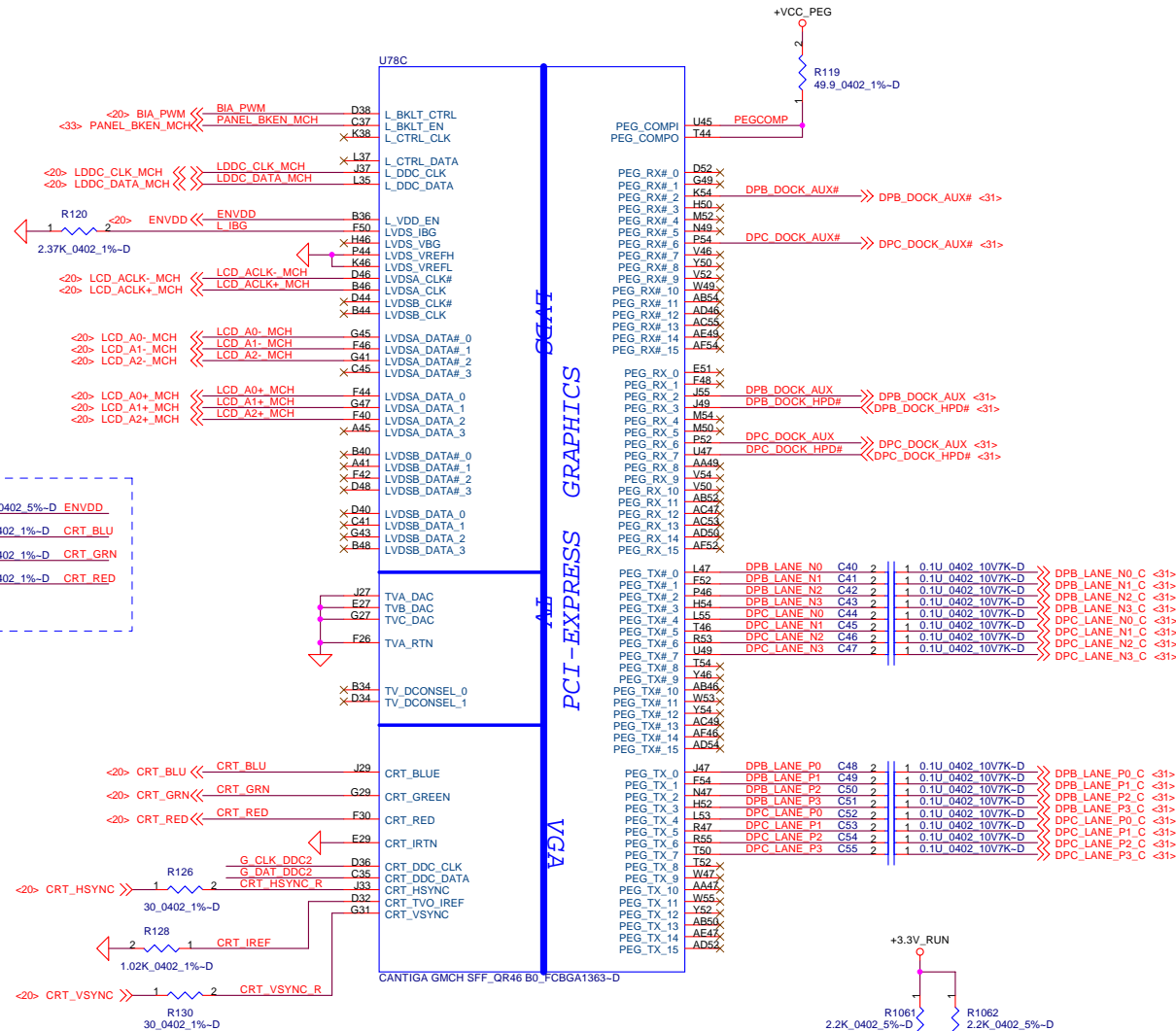


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Cantiga GS(2/6)

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Strap Pin Table		
CFG5	DMI X2 Select	Low = DMI x 2 High = DMI x 4 (Default)
CFG6	iTPM Host Interface	Low = iTPM enable High = iTPM disable(Default)
CFG7	Management Engine Crypto Strap	Low = TLS cipher suite with no confidentiality High = TLS cipher suite with confidentiality(Default)
CFG9	PCI Express Graphic Lane	Low = Reverse Lane High = Normal Operation(Default)
CFG10	PCI Express Lookpack enable	Low = Enable High = Disable(default)
CFG12	ALLZ	Low = ALLZ mode enable High = Disable(default)
CFG13	XOR	Low = XOR mode enable High = Disable(default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIe1 is operational (default) High=SDVO and PCIe1 are operating simultaneously via PEG port
SDVO_CTRL_DATA		Low=No SDVO Device Present (default) High=SDVO Device Present
DDPC_CTRLDATA		Low=DisplayPort disabled (default) High=DisplayPort device present

CFG[5:16] have internal pullup

CFG[19:20] have internal pulldown

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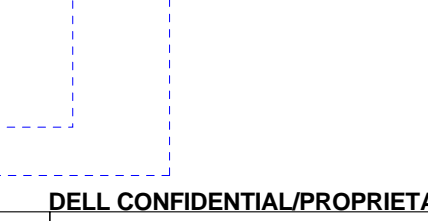
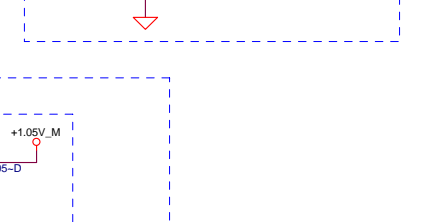
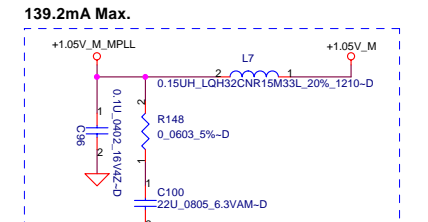
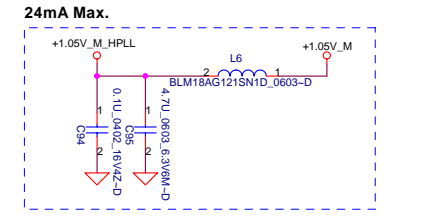
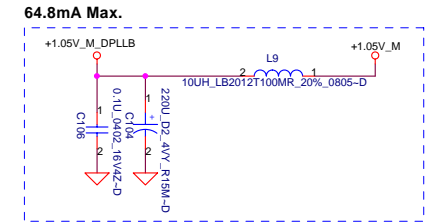
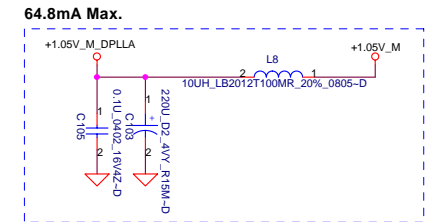
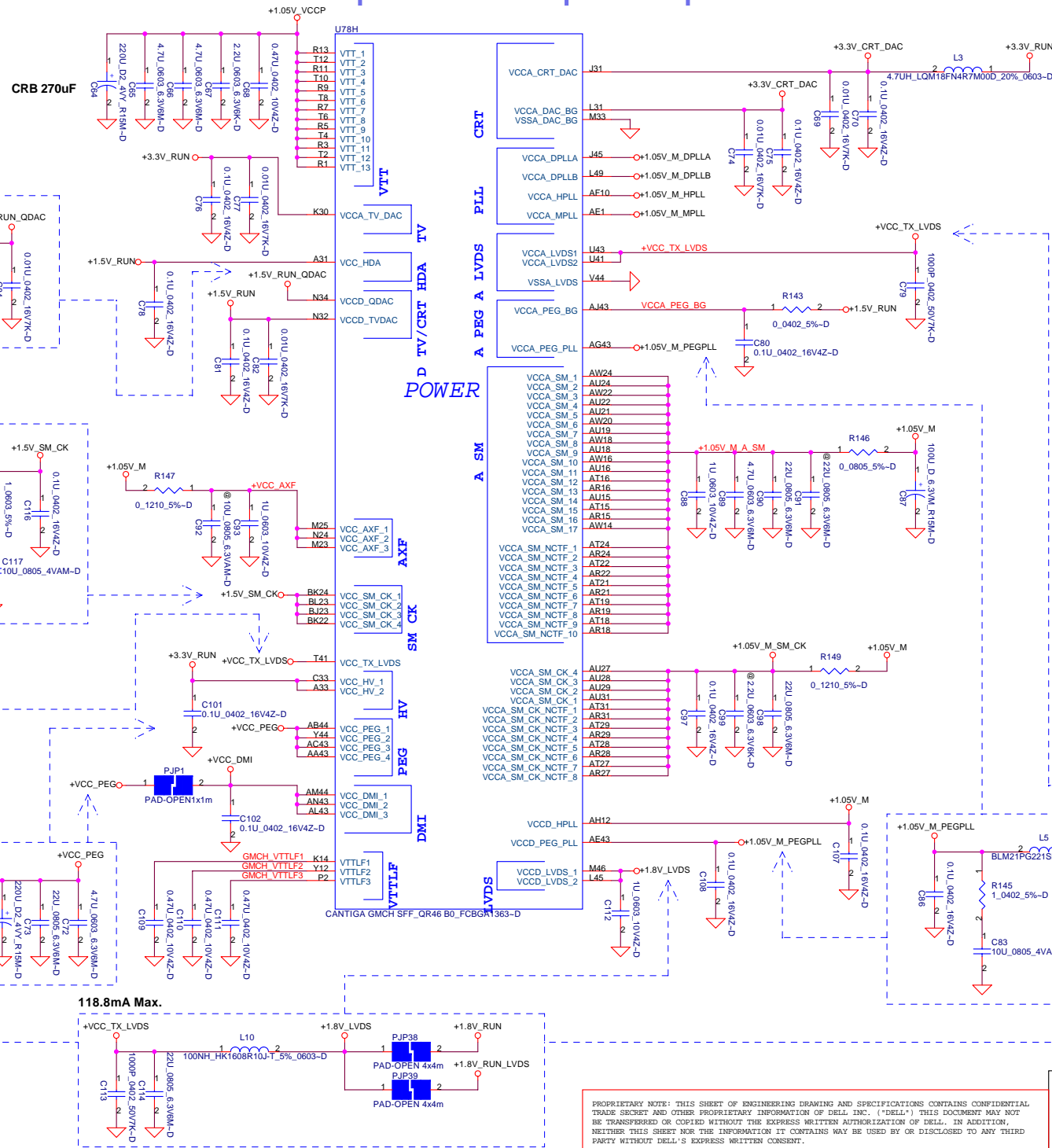
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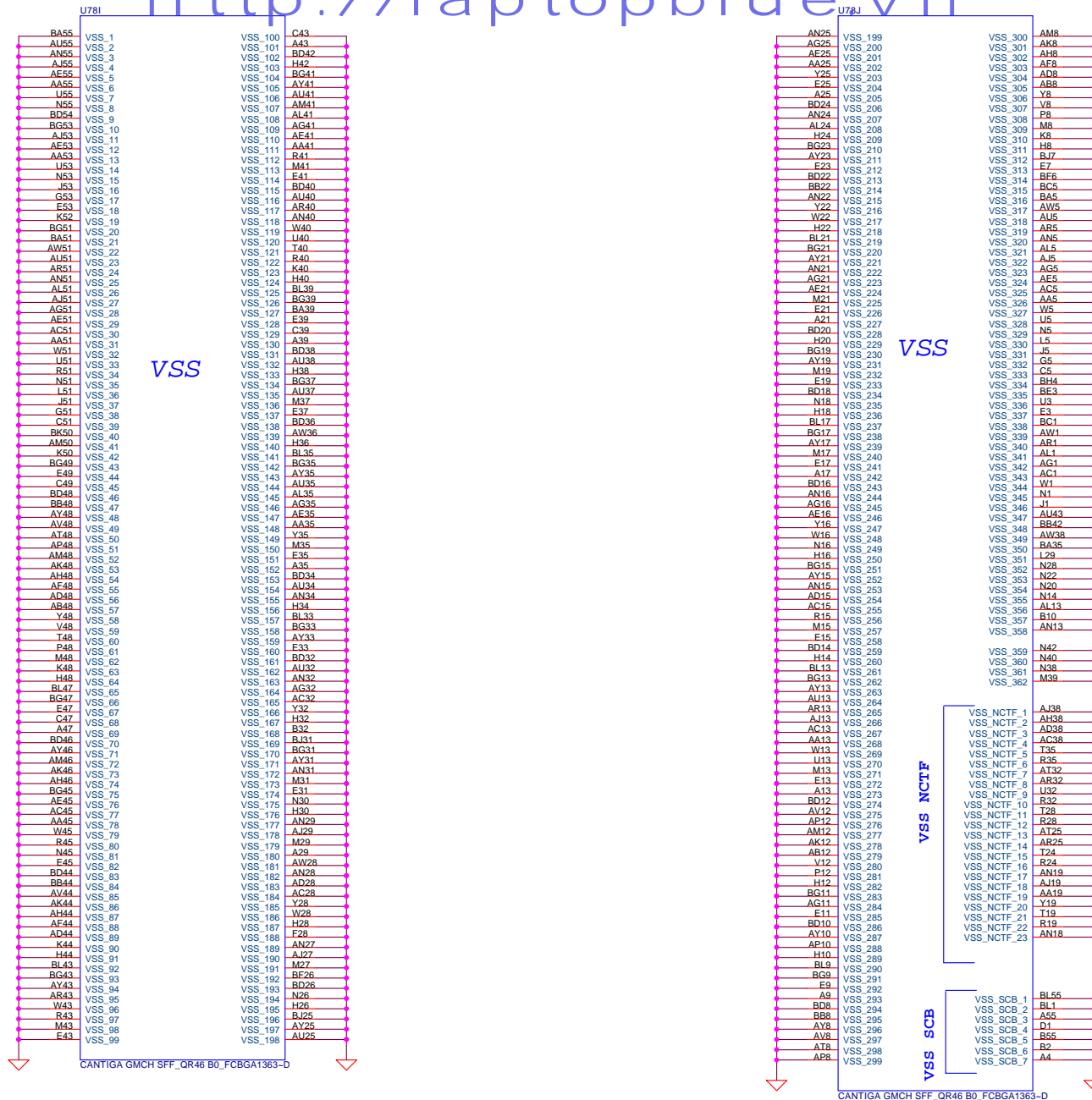
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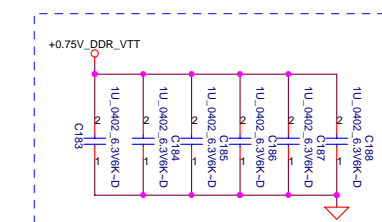
Cantiga GS(6/6)

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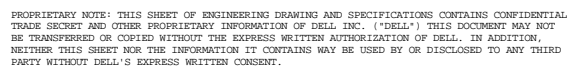




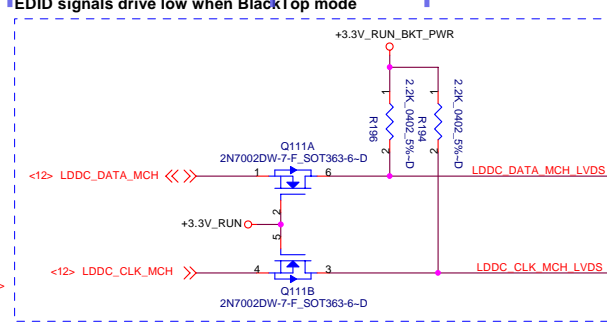
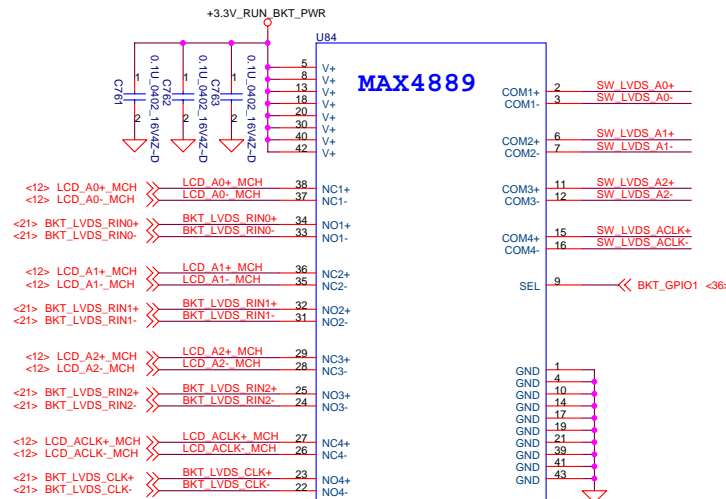
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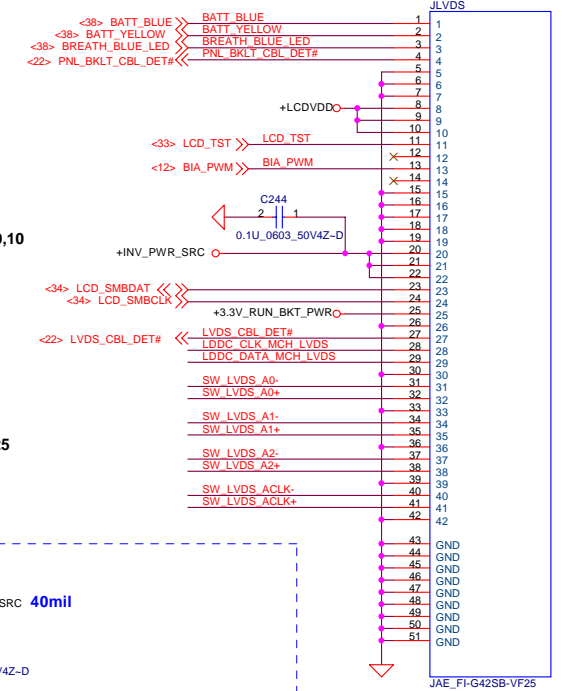


EDID signals drive low when BlackTop mode



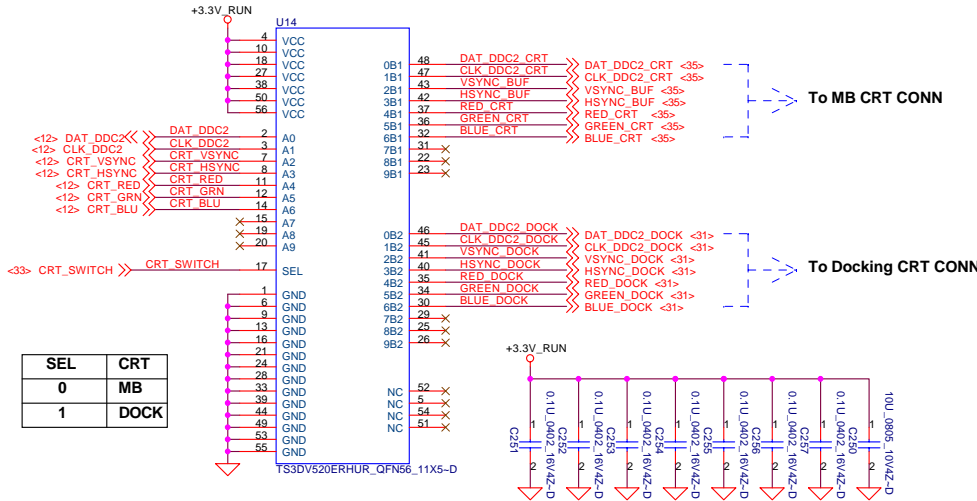
Place close to JLVDS.8,9,10

Place close to JLVDS.25

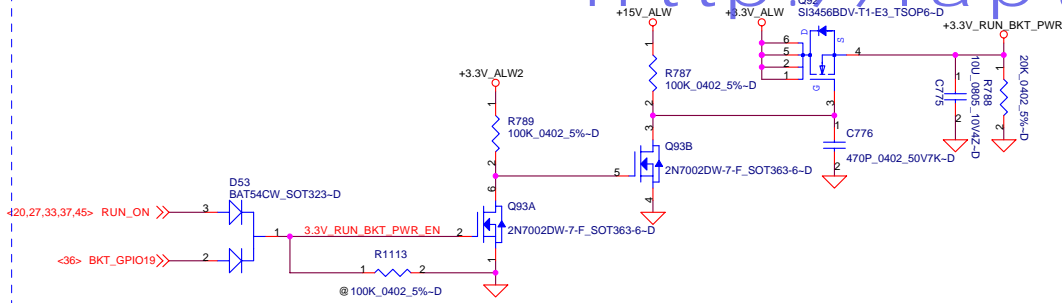


**SEL Logic 1 Work from BKT**

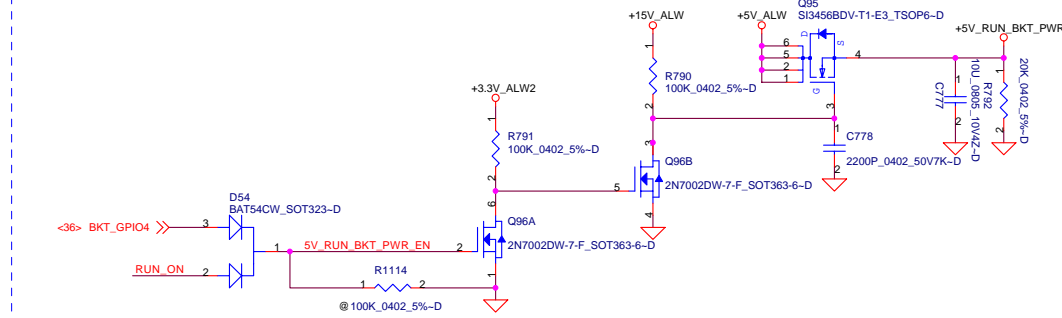
SEL	NC to COM	NO to COM
0	ON	OFF
1	OFF	ON



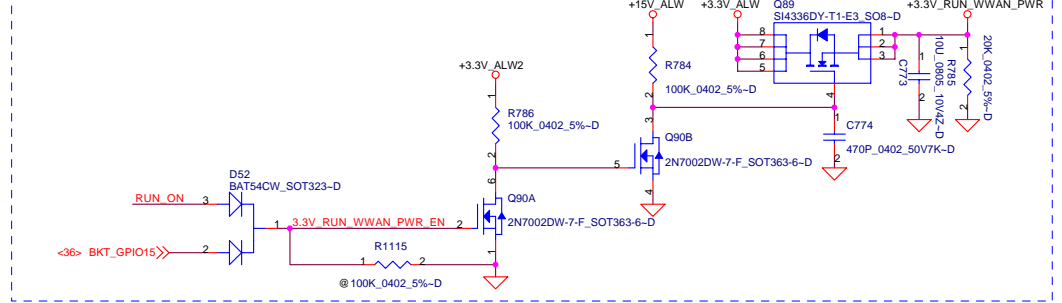
### +3.3V\_RUN\_BKT\_PWR Source



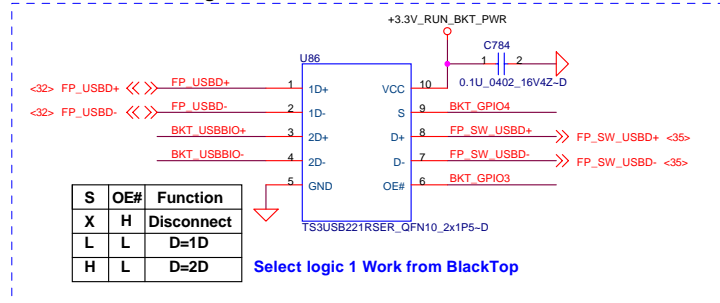
### +5V\_RUN\_BKT\_PWR Source, for Touch Pad and Audio Amplifier



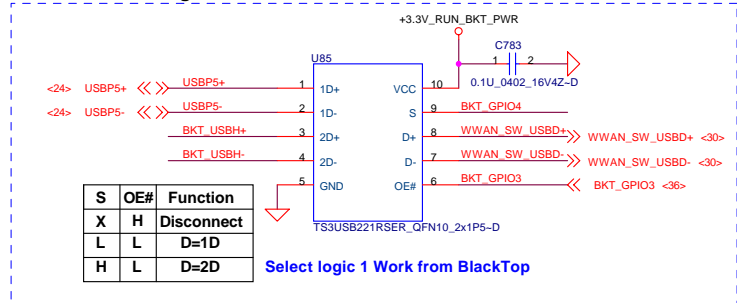
### +3.3V\_RUN\_WWAN\_PWR Source, for WWAN



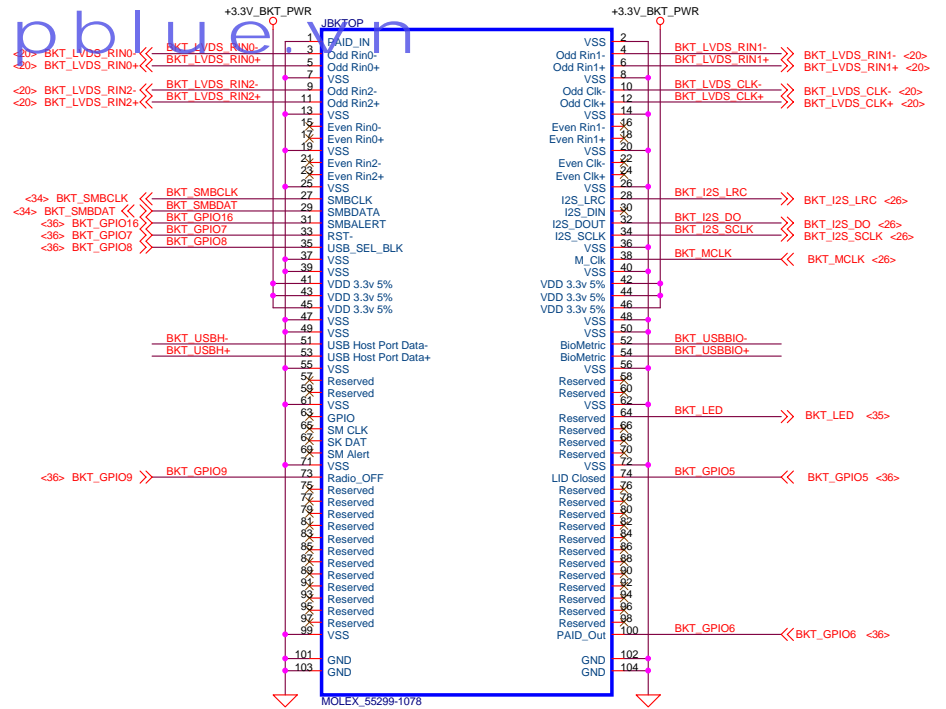
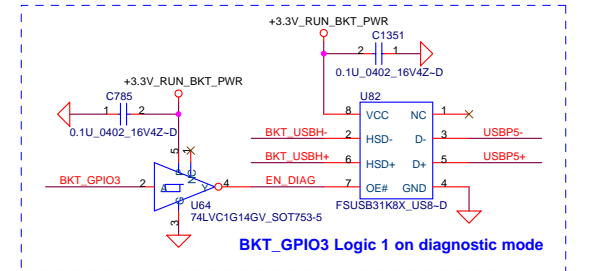
### For Biometric USB signals isolation



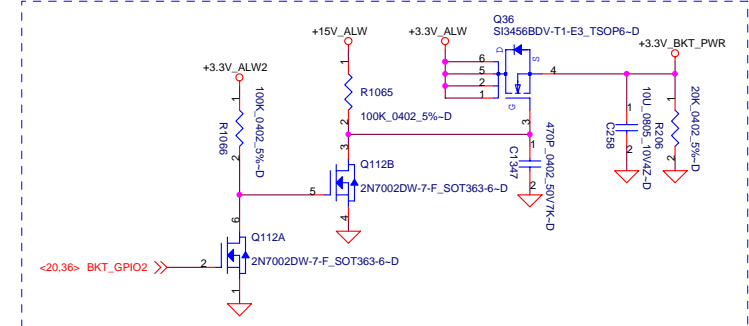
### For WWAN USB signals isolation



### Add BlackTop to ICH9M interface by USB signals when diagnostic mode



### Enable BlackTop POWER



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BlackTop POWER and CONN

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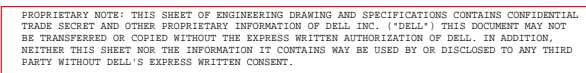
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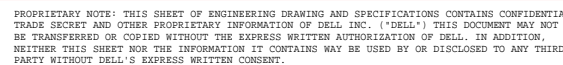
ICH9M SFF(3/4)

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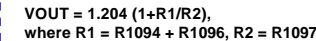
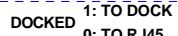
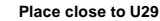








+3.3V\_LAN SOURCE



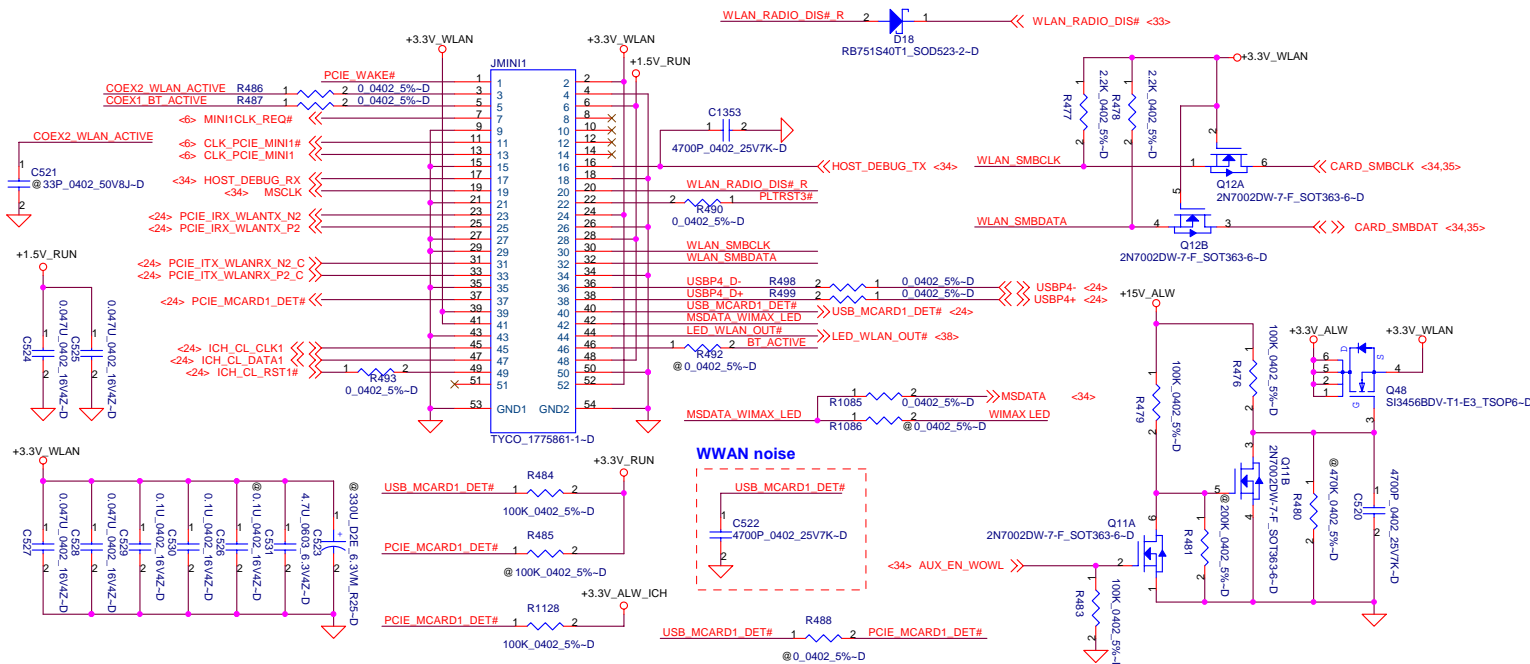
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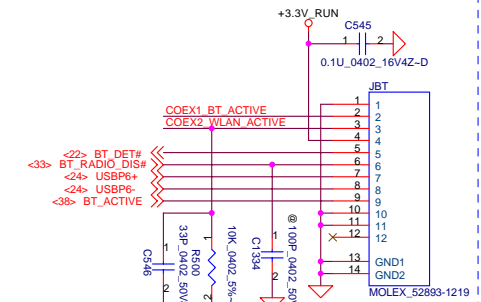




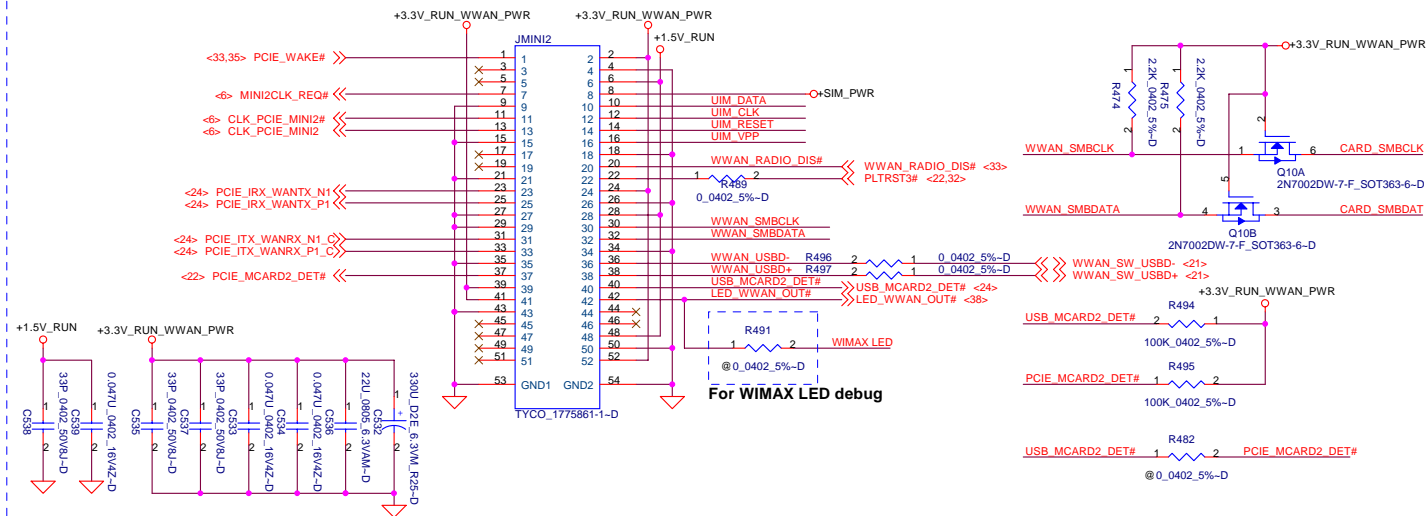




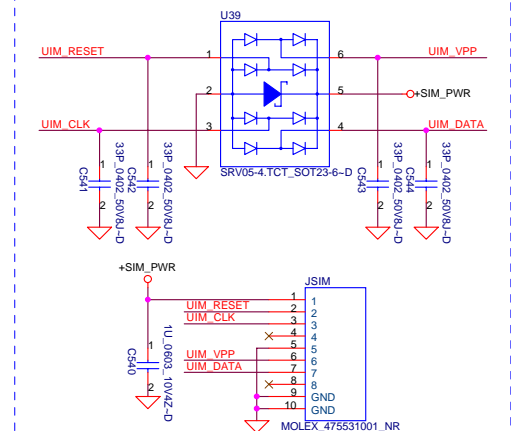
## Bluetooth



## Mini Card 2---WWAN



## SIM Card



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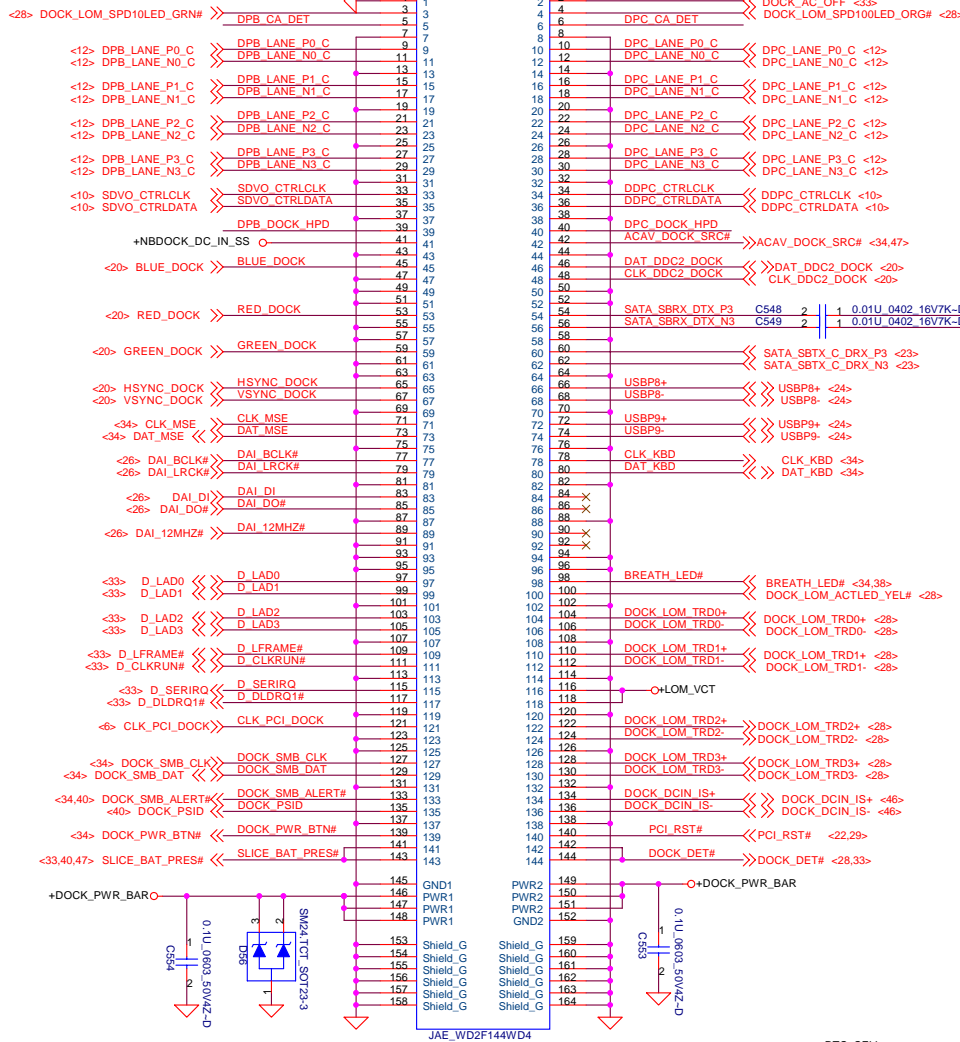
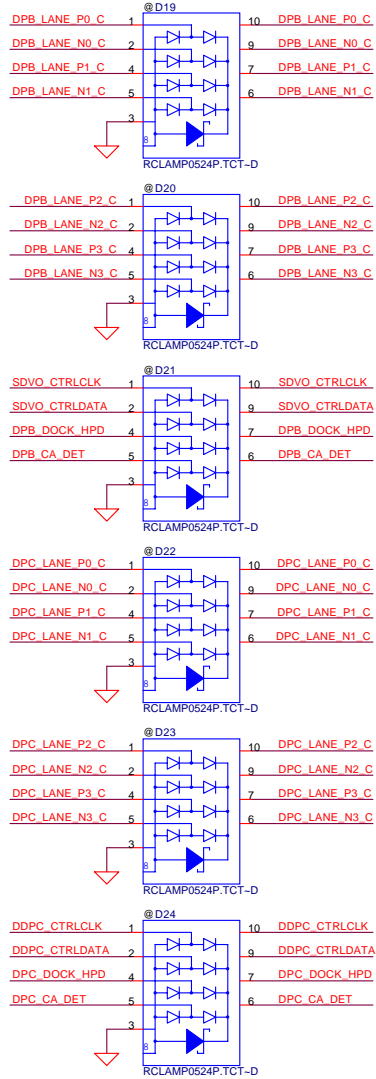
Title	Mini W/L AN/PA/WAN, SIM card and BT
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Mini WLAN/WWAN, SIM card and BT		
Size	Document Number	Rev

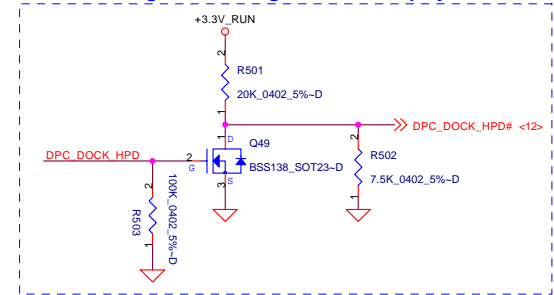
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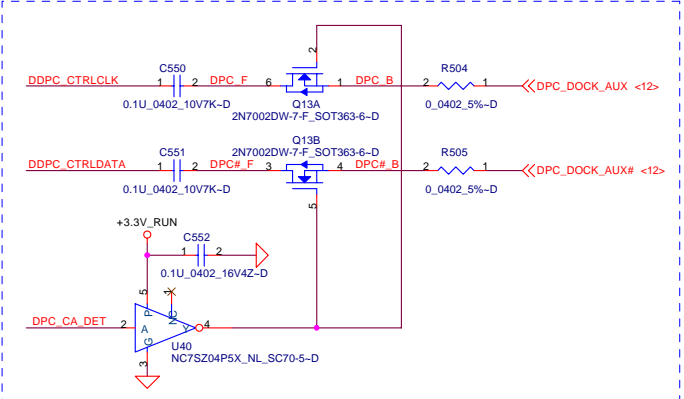
## Place close to JDock connector



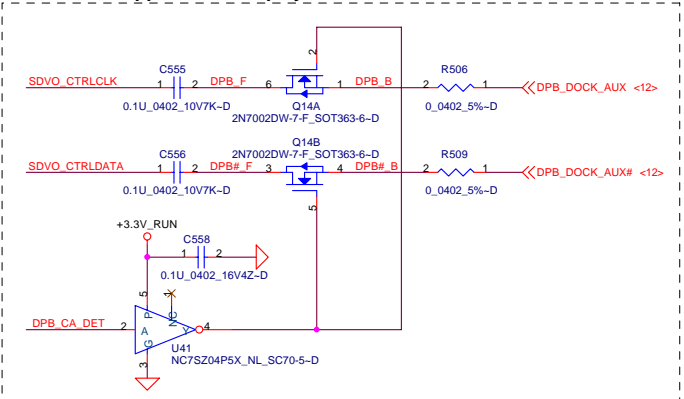
## HPD# Inverting level shifting circuit for DisplayPort C



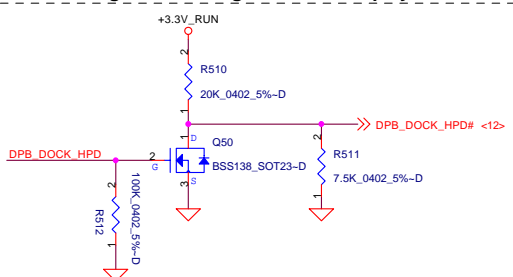
## Switch that support both DisplayPort C and DVI/HDMI



## Switch that support both DisplayPort B and DVI/HDMI



## HPD# Inverting level shifting circuit for DisplayPort B



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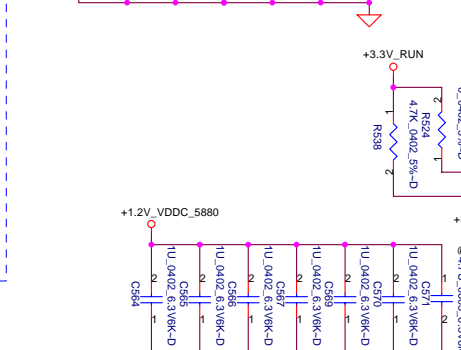
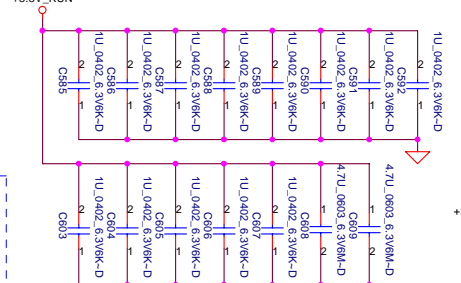
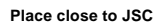
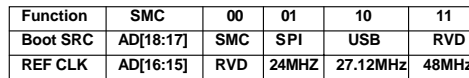
Compal Electronics, Inc.



DOCKING CONNECTOR

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**Compal Electronics, Inc.**

**USH BCM5880**

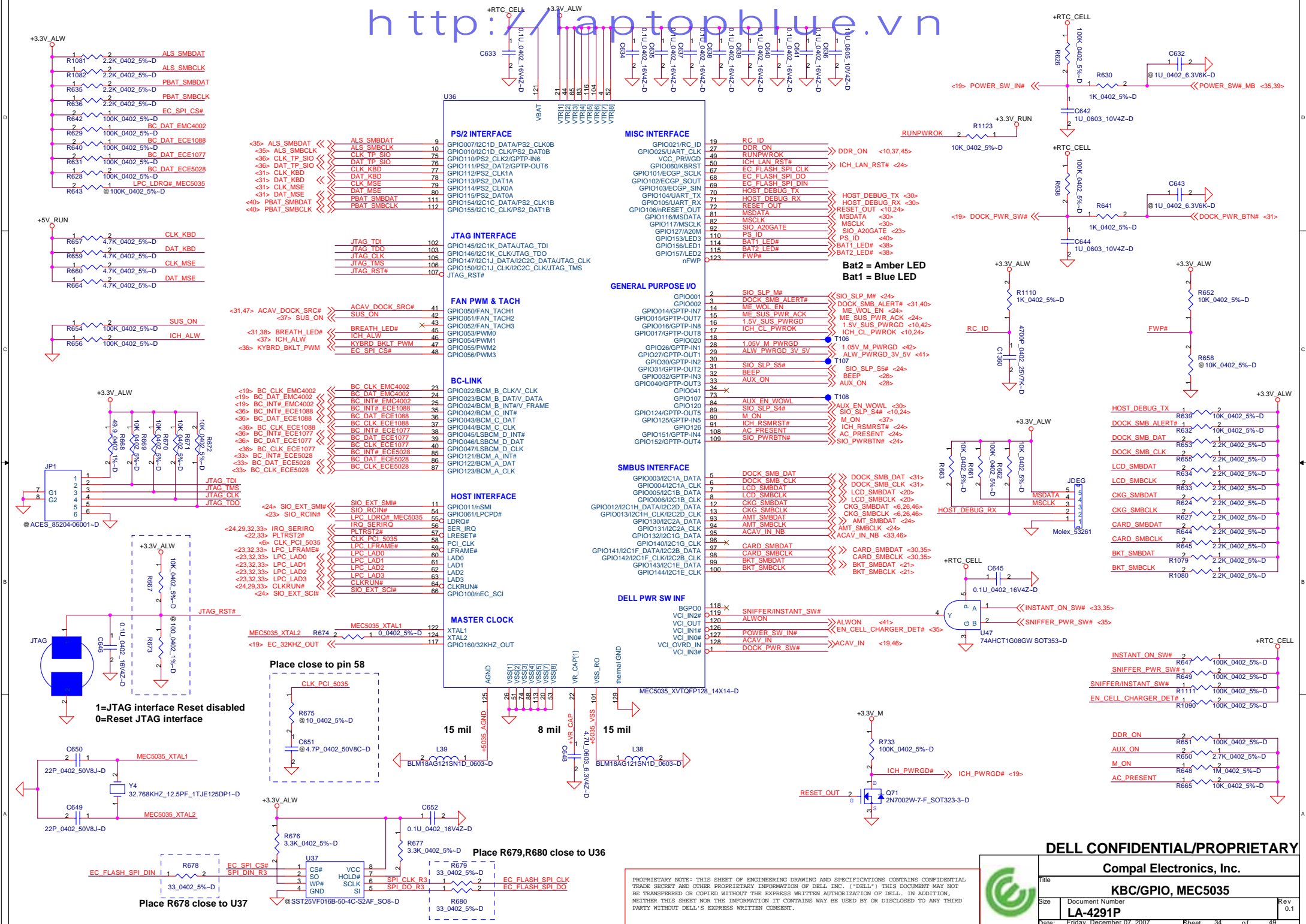
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http://laptopblue.vn

GPIO	Signal	Signal	Signal
52			
51	IO_BD_DET#	IO_BD_DET#	<24>
50	POWER_SW_MB	POWER_SW_MB	<34,39>
49	BREATH_BLUE_LED_PWR	BREATH_BLUE_LED_PWR	<38>
48	LAN_ACTLED_YEL_R#	LAN_ACTLED_YEL_R#	<28>
47	LED_100_GRN_R#	LED_100_GRN_R#	<28>
46	LED_100_ORG_R#	LED_100_ORG_R#	<28>
45			
44			
43	SW_LAN_TX0+	SW_LAN_TX0+	<28>
42	SW_LAN_TX1+	SW_LAN_TX0+	<28>
41	SW_LAN_TX1+	SW_LAN_TX1+	<28>
40	SW_LAN_TX1+	SW_LAN_TX1+	<28>
39	SW_LAN_TX2+	SW_LAN_TX2+	<28>
38	SW_LAN_TX2+	SW_LAN_TX2+	<28>
37	SW_LAN_TX3+	SW_LAN_TX3+	<28>
36	SW_LAN_TX3+	SW_LAN_TX3+	<28>
35			
34		3.3V_LAN	
33		HL0M_VCT	
32	CELL_CHARGER_DET_R#	USB_POWERSHARE_PWR_EN#	<33>
31			
30	SW_USB0P+	SW_USB0P+	<24>
29	SW_USB0P+	SW_USB0P+	<24>
28			
27			
26	5V_ALW		
25			
24			
23	TPA0+	TPA0+	<29>
22	TPA0+	TPA0+	<29>
21	TPB0+	TPB0+	<29>
20	TPB0+	TPB0+	<29>
19	TPB0+	TPB0+	<29>
18	1394_DET#	1394_DET#	<24>
17	USB_OC0#	USB_OC0#	<24>
16			
15		3.3V_RUN	
14	CARD_EN	CARD_EN	<29>
13	SDWP#	SDWP#	<29>
12	SDCMD# MMCMD#	SDCMD# MMCMD#	<29>
11	SDCDAT1 MMCMDAT1	SDCDAT1 MMCMDAT1	<29>
10	SDCDAT0 MMCMDAT0	SDCDAT0 MMCMDAT0	<29>
9	SDCCLK MMCCLK	SDCCLK MMCCLK	<29>
8	MMCMDAT7	MMCMDAT7	<29>
7	DETECT_GND		
6	SDCCMD MMCMD#	SDCCMD MMCMD#	<29>
5		SDCDAT3 MMCMDAT3	<29>
4	MMCMDAT3 MMCMDAT3	MMCMDAT3 MMCMDAT3	<29>
3	MMCMDAT4	MMCMDAT4	<29>
2	SDCDAT2 MMCMDAT2	SDCDAT2 MMCMDAT2	<29>
1			

**Pin-to-pin connection diagram for FOX Q515056-1010-7F:**

Pin	Signal	Pin	Signal
<24>	AUDIO BD DET#	1	DMIC_CLK
<21>	BKT_LED	2	DMIC0
<33,34>	INSTANT_ON_SW#	3	BLUE_CRT
		4	GREEN_CRT
<20>	CLK_DDC2_CRT	5	RED_CRT
<20>	DAT_DDC2_CRT	6	HSYNC_BUF
		7	VSYNC_BUF
+3.3V_RUN		8	USBP3+
+3.3V_RUN_C		9	USBP3-
+5V_RUN		10	5V_ALW
		11	ESATA_USB_PWR_EN#
		12	ESATA_USB_OC#
<23>	ESATA_IRX_DTX_P4_C	13	AUD_EXT_MIC_L
<23>	ESATA_IRX_DTX_N4_C	14	AUD_EXT_MIC_R
<23>	ESATA_ITX_DRX_N4	15	DETECT_GND
<23>	ESATA_ITX_DRX_P4	16	
		17	
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The diagram illustrates the SATA controller interface, showing the connection between the SATA controller chip and the SATA connector. The SATA controller chip is shown with its pins and internal components, including a 0.1uF capacitor (C341) and a 0.1uF capacitor (C710). The SATA connector is shown with its pins and internal components, including a 0.1uF capacitor (C341) and a 0.1uF capacitor (C710). The diagram is labeled with component values and pin numbers.

**SATA Controller Chip (PJP2) Connections:**

- Pin 1:** +3.3V\_RUN0
- Pin 2:** +3.3V\_HDD
- Pin 3:** PAD-OPEN 4x4m
- Pin 4:** <24> HDD\_DET#
- Pin 5:** <23> PSATA\_IRX\_DTX\_P0\_C
- Pin 6:** <23> PSATA\_IRX\_DTX\_N0\_C
- Pin 7:** 0.01U\_0402 16V7K-D
- Pin 8:** 0.01U\_0402 16V7K-D
- Pin 9:** <23> PSATA\_ITX\_DRX\_N0
- Pin 10:** <23> PSATA\_ITX\_DRX\_P0

**SATA Connector (MOLEX\_52893-1219) Connections:**

- Pin 1:** JHDD
- Pin 2:** GND1
- Pin 3:** GND2
- Pin 4:** 1
- Pin 5:** 2
- Pin 6:** 3
- Pin 7:** 4
- Pin 8:** 5
- Pin 9:** 6
- Pin 10:** 7
- Pin 11:** 8
- Pin 12:** 9
- Pin 13:** 10
- Pin 14:** 11
- Pin 15:** 12
- Pin 16:** 13
- Pin 17:** 14

**Internal Components:**

- C341:** 0.1uF capacitor
- C710:** 0.1uF capacitor
- 0.1uF 0402 16V7K-D:** 0.1uF capacitor
- 0.1uF 0805 10V4Z-D:** 0.1uF capacitor

**Place close to JHDD**

The schematic shows the internal circuitry of the module connected to a 16-pin Molex connector. It includes two NPN transistors (Q86 and Q88) for signal amplification or switching, resistors R757 and R758, and various power supply connections (+3.3V\_ALW, +5V\_ALW). Signal labels include SNIFFER\_YELLOW#, SNIFFER\_BLUE#, SNIFFER\_DET#, SNIFFER\_PWR\_SW#, WIRELESS\_ON#/OFF#, LID\_CL#, FP\_SW\_USBD-, FP\_SW\_USBD+, BIO\_DET#, FP\_RESET#, and DETECT\_GND.

The schematic diagram illustrates the internal components and external connections for the SW\_DET pin. On the left, the internal circuit includes transistors Q119A and Q119B, resistors R1083, R1084, and R1085, and capacitors CAPSW\_ALS\_SMBDAT and CAPSW\_ALS\_SMBCLK. The circuit is powered by +3.3V\_RUN\_BKT\_PWR. The right side shows the connection to the MOLEX\_52746-1070 connector, with pins labeled G1, G2, G3, DETECT\_GND, CAP\_SW\_SMB\_INT#, CAPSW\_ALS\_SMBDAT, CAPSW\_ALS\_SMBCLK, SW\_BD\_DET#, and +5V\_RUN\_BKT\_PWR.

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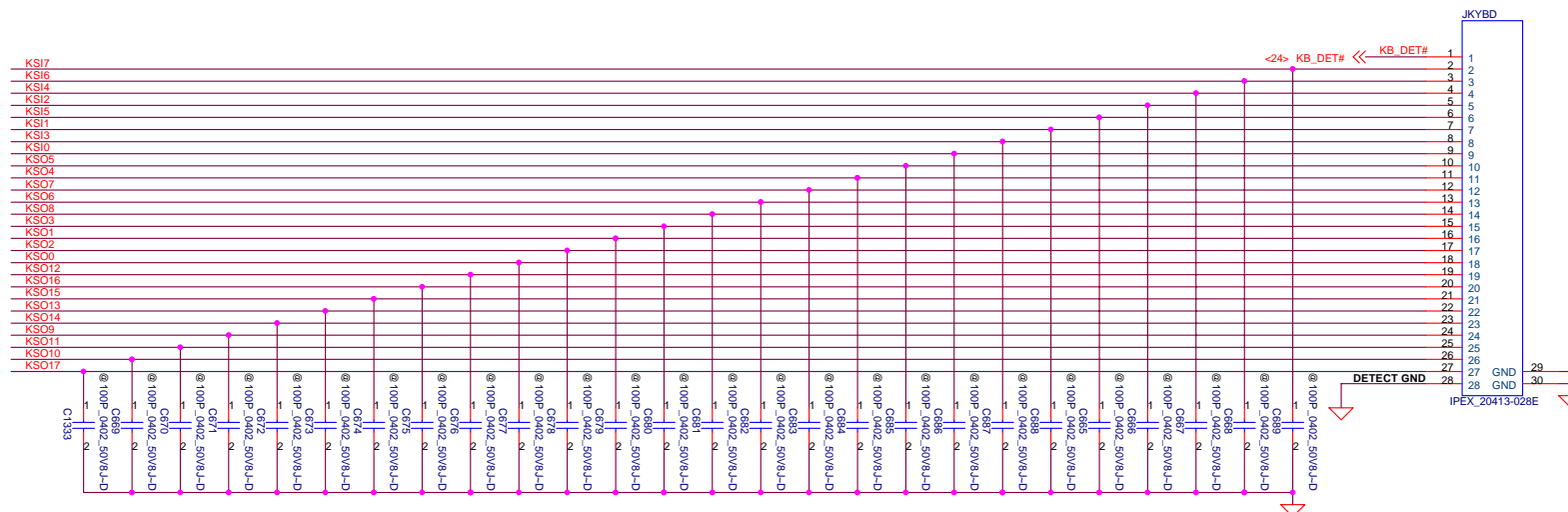
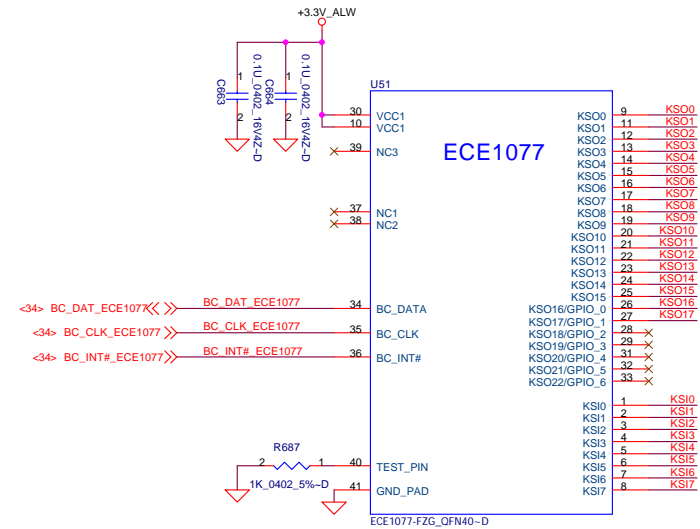


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Pin connection diagram for the KYBRD module:

- Pin 1: +5V\_RUN\_BKT\_PWR
- Pin 2: KYBRD\_BKLT\_PWM
- Pin 3: KYBRD\_BKLT\_DET#
- Pin 4: KYBRD\_BKT\_DET#
- Pin 5: GND
- Pin 6: GND

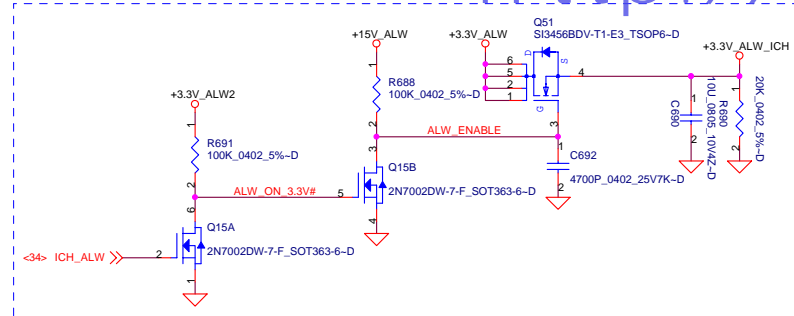
Additional labels and connections:

- I\_KBBKT (connected to Pin 1)
- <34> KYBRD\_BKLT\_PWM (connected to Pin 2)
- <24> KYBRD\_BKT\_DET# (connected to Pin 3)
- GND (connected to Pin 5)
- GND (connected to Pin 6)

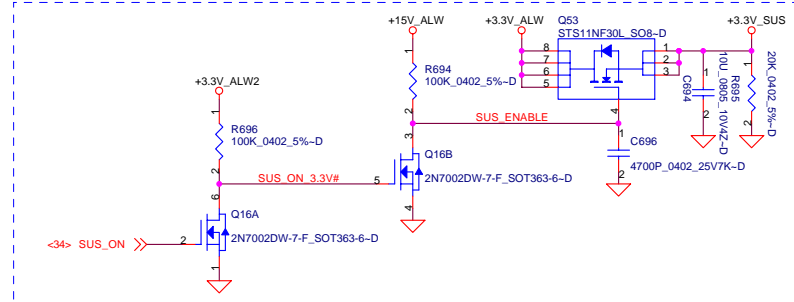
MOLEX\_52745-0459



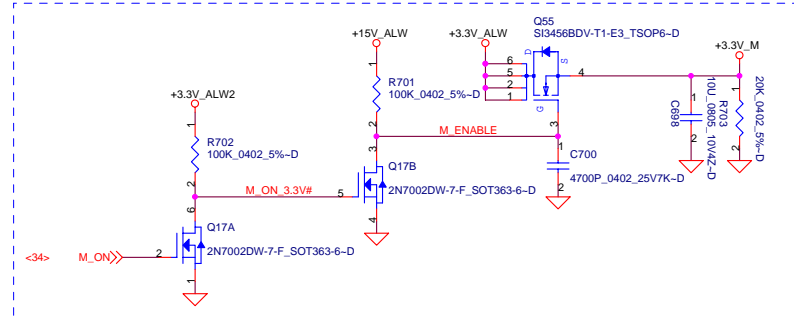
### +3.3V\_ALW\_ICH Source



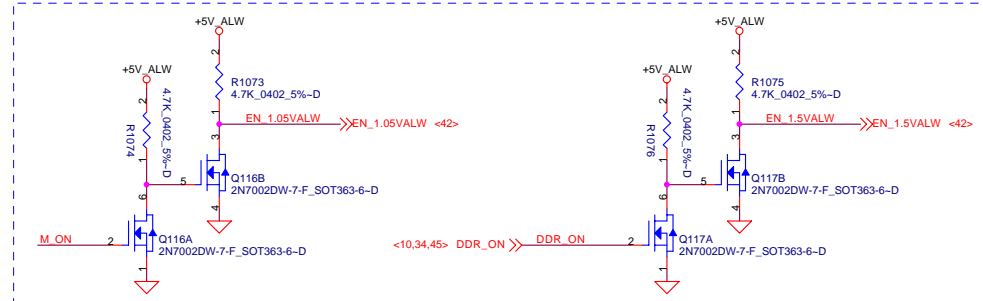
### +3.3V\_SUS Source



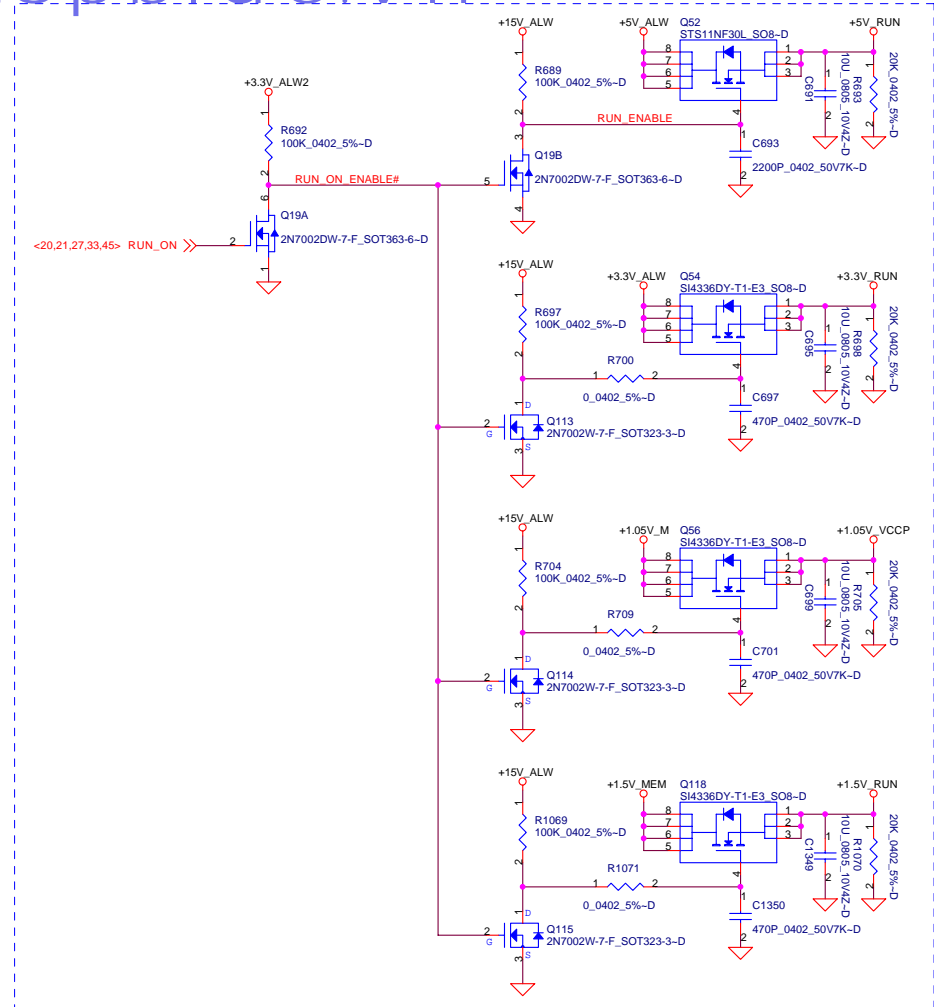
### +3.3V\_M Source



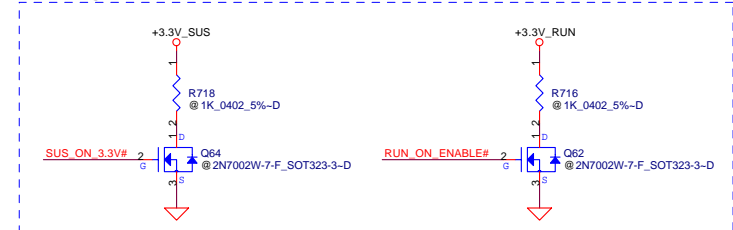
### Level shifter for +1.05V\_M and +1.5V\_MEM PWM IC



### +5V\_RUN/+3.3V\_RUN/+1.05V\_VCCP/+1.5V\_RUN Source



### Discharg Circuit



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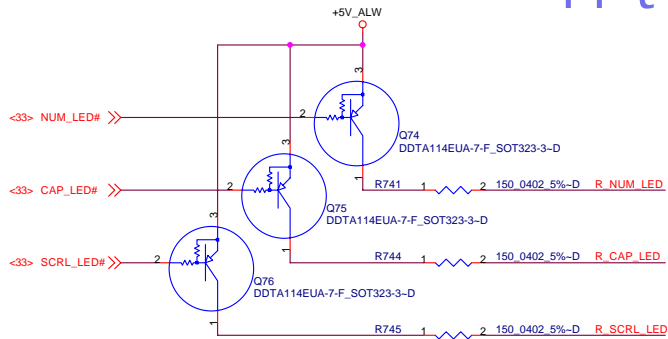
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POWER CONTROL

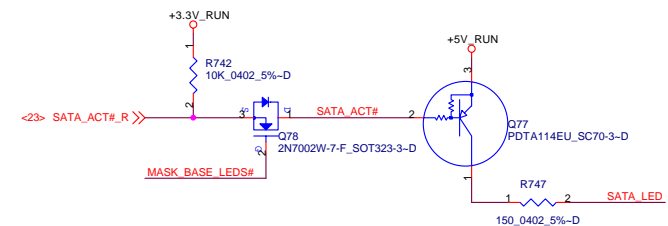
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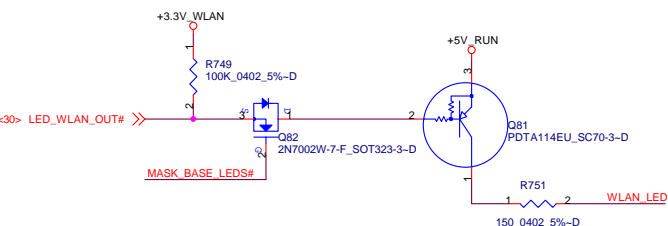
## Keyboard Status, Num Lock/Caps Lock/Scroll Lock LEDs



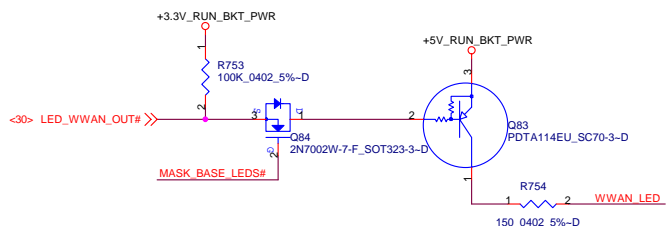
## HDD LED



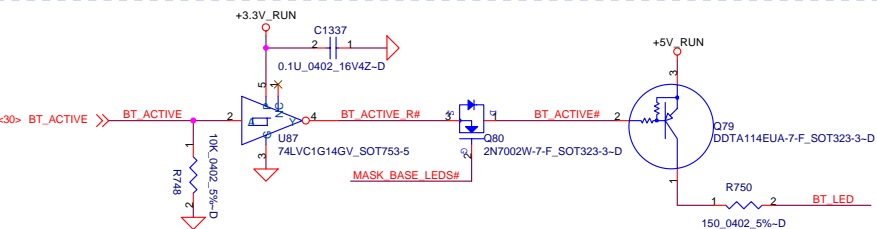
## WLAN LED



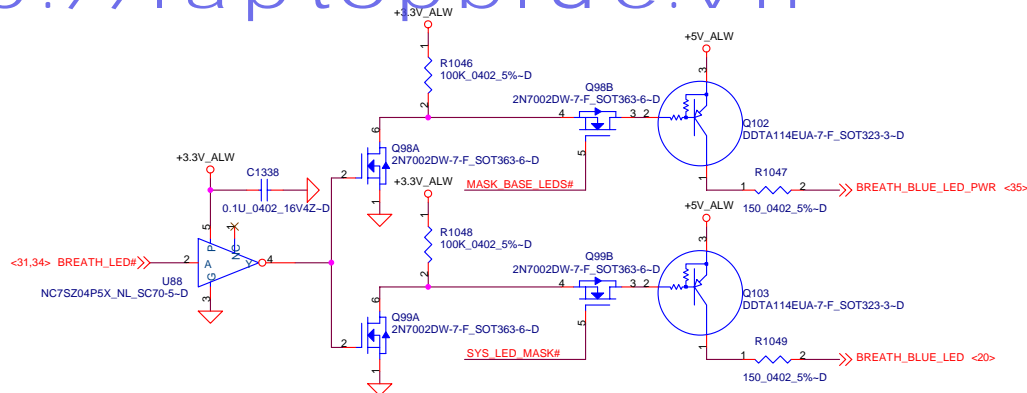
## WWAN LED



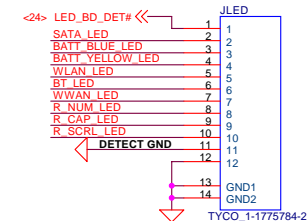
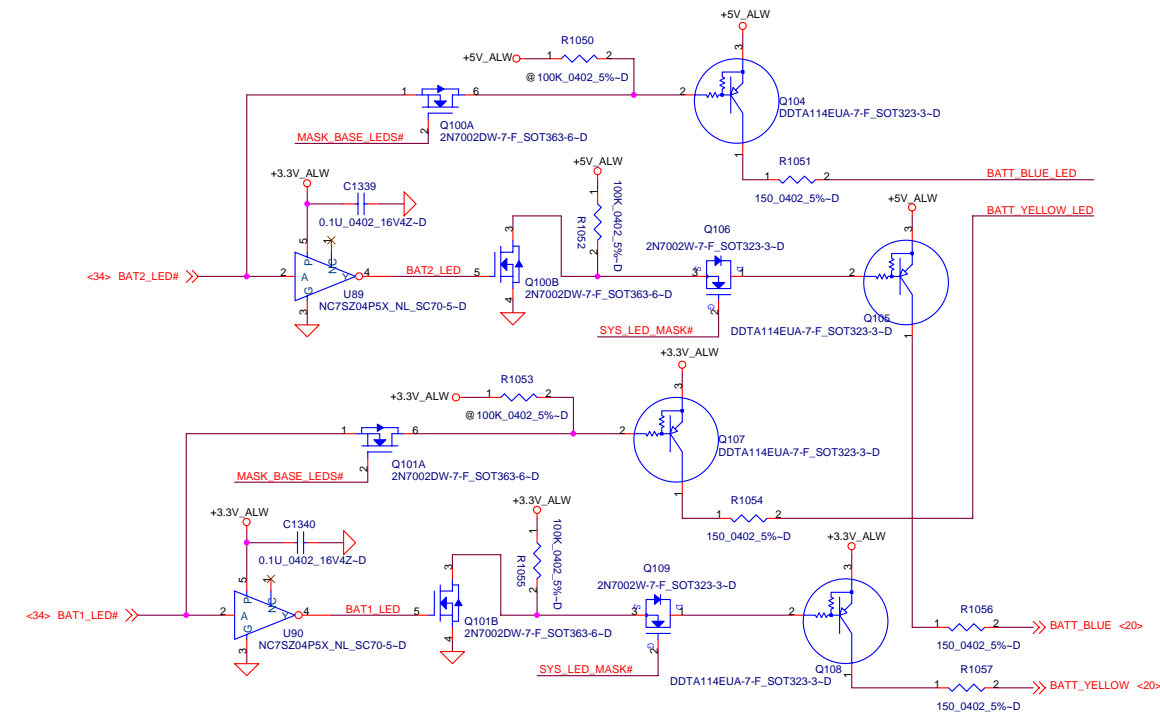
## BLUETOOTH LED



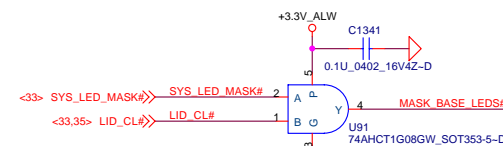
## POWER/SUSPEND breathing LED



## BATTERY LED



LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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System LEDs Control

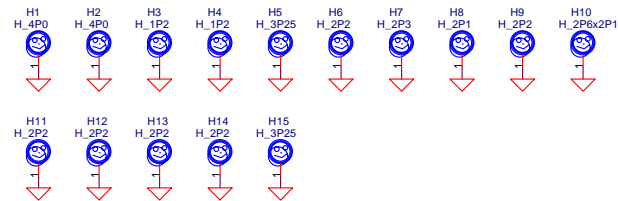
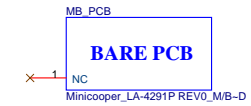
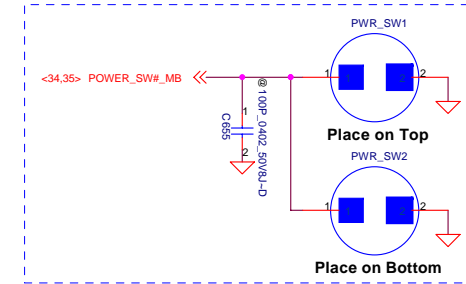
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### Fiducial Mark



### Power button switch for debug



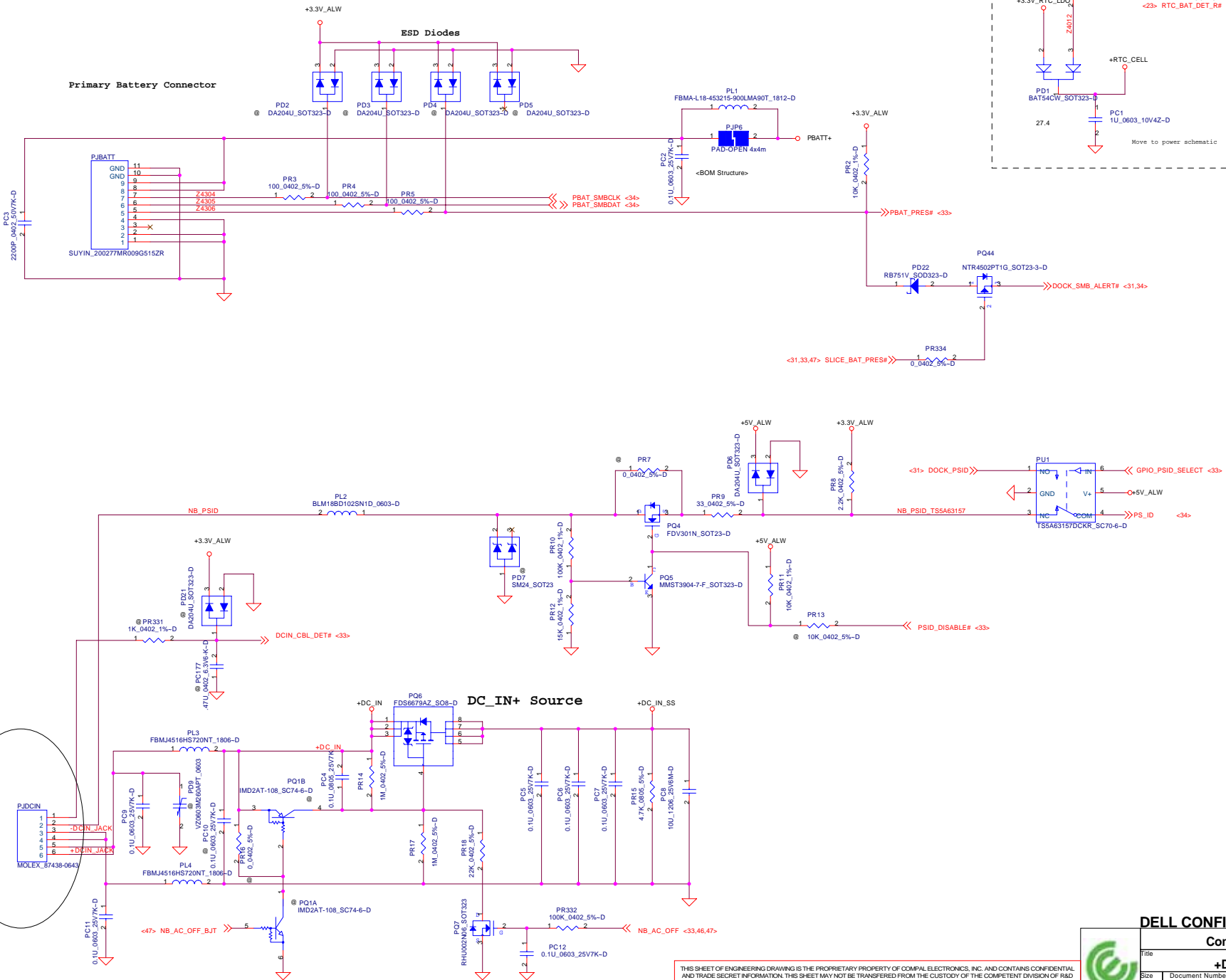
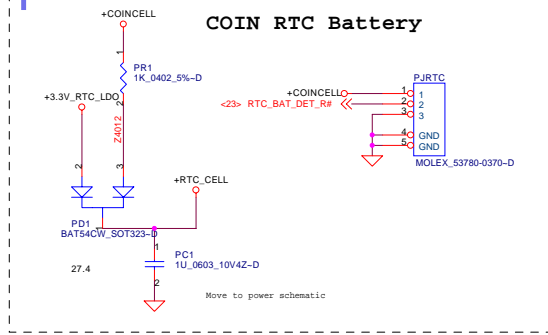
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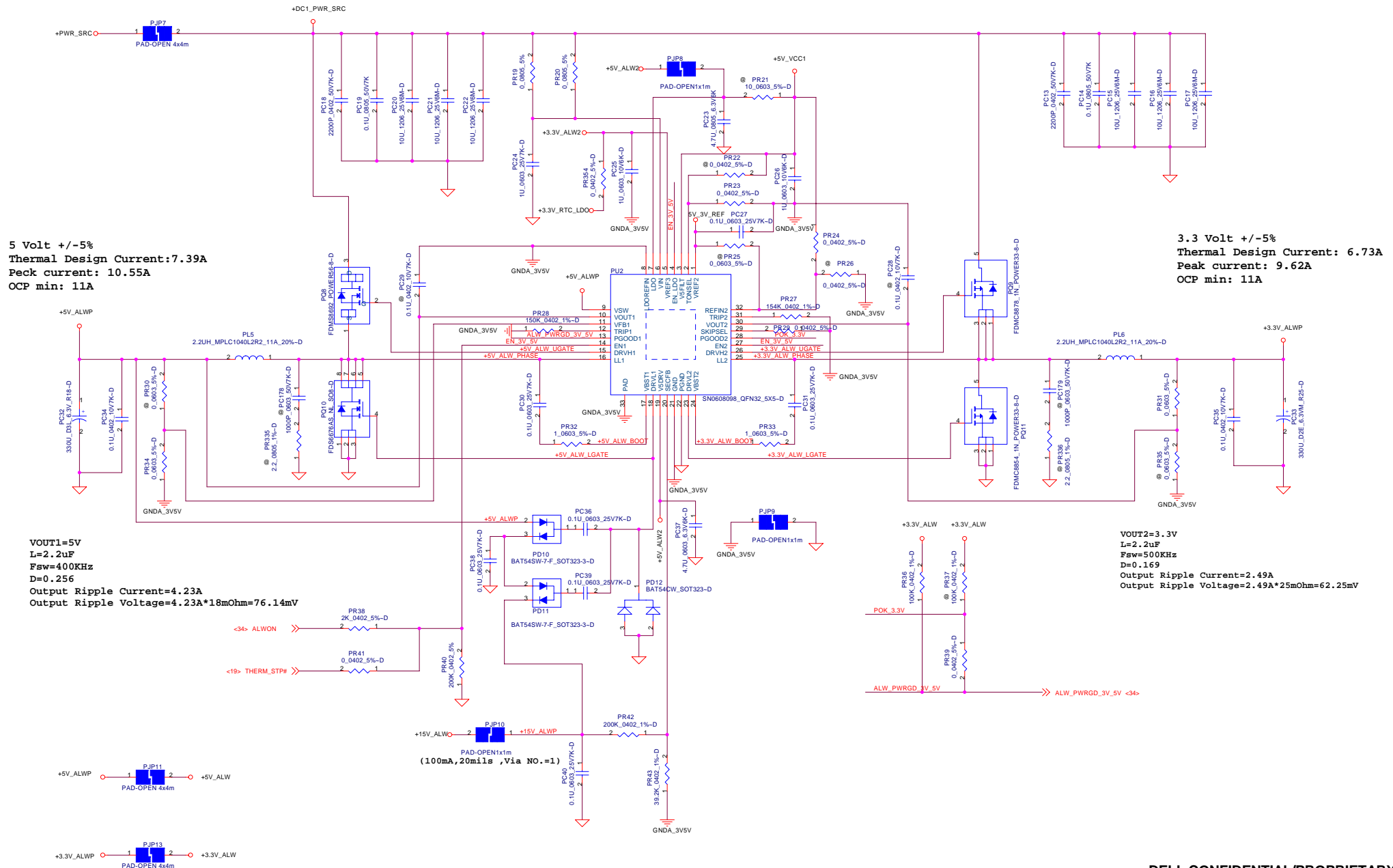
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**+DCIN**

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+3.3V\_ALWP/ +5V\_ALWP/ +5V\_ALW2 / +15V\_ALWP



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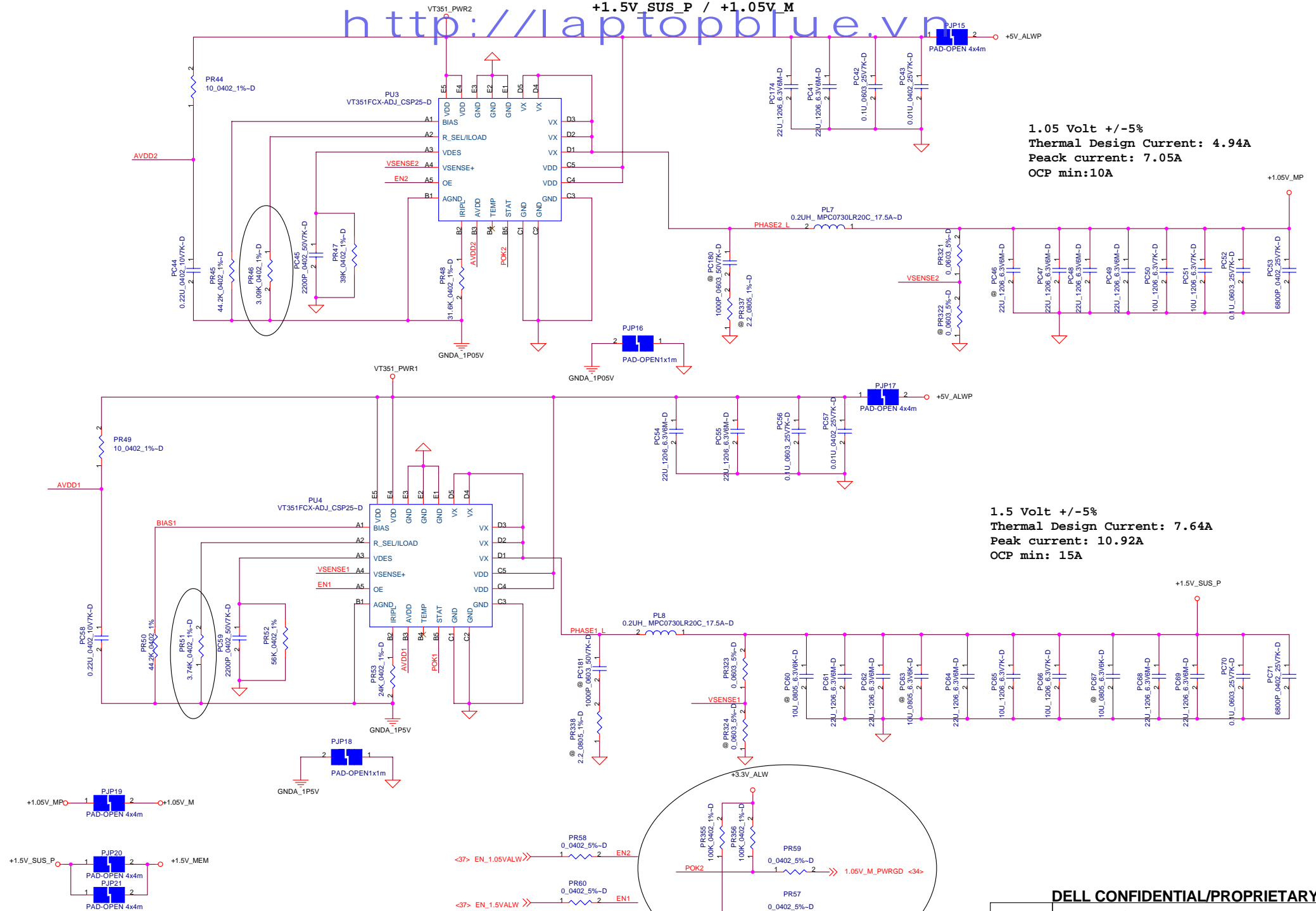
DC/DC +3V/ +5V

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+1.5V SUS P / +1.05V MP

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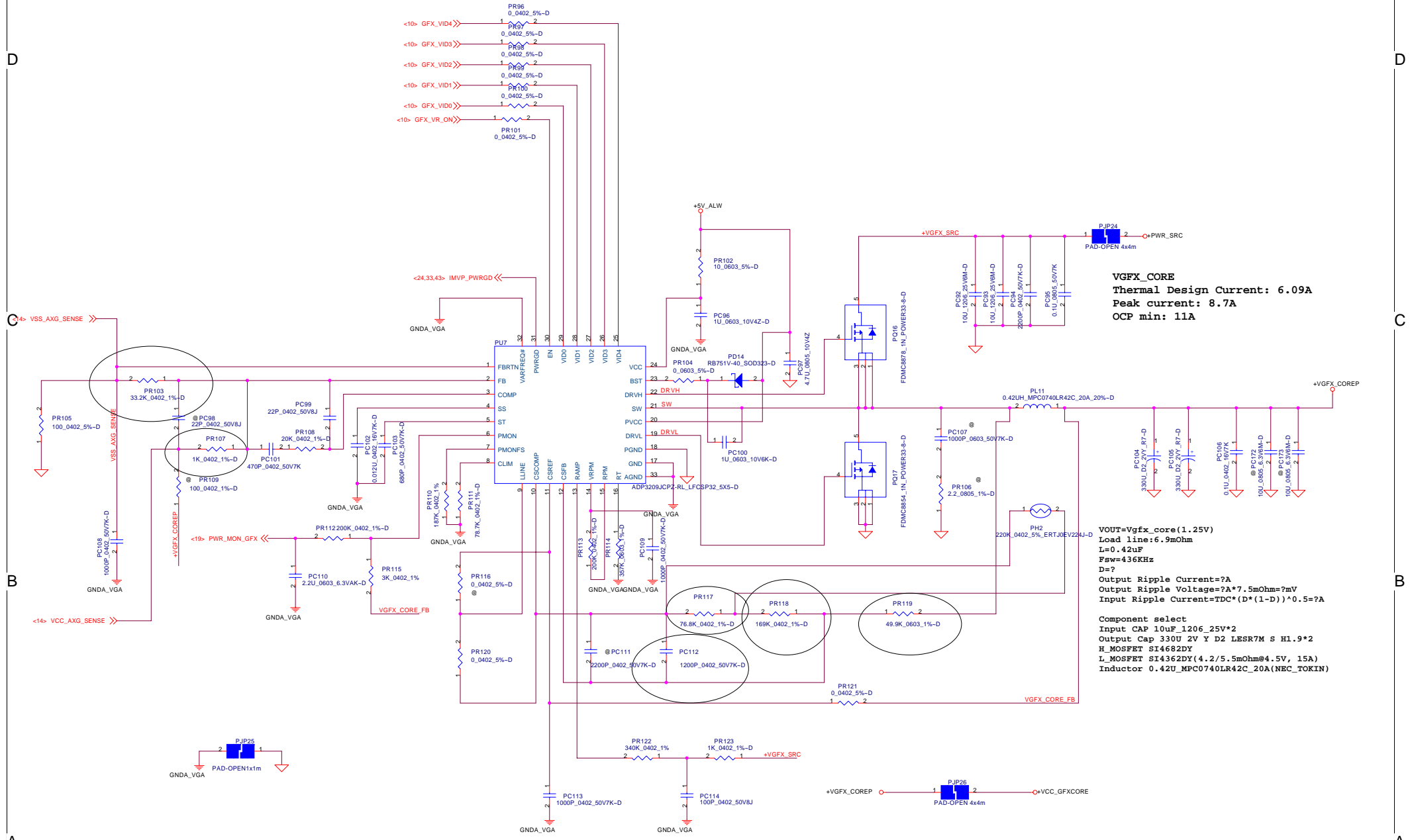


The diagram shows a closed circuit with two parallel wires. The left wire contains a battery and a switch. The right wire contains a resistor. The circuit is closed, and current flows clockwise.

PR 1K 2

PC8 1008  
002\_1  
V  
0013V\_0002\_10V  
DA\_C  
002\_5%  
9  
002\_5  
93  
040:  
94  
040:  
NOT  
De-

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**V GFX\_CORE**  
Thermal Design Current: 6.09A  
Peak current: 8.7A  
OCP min: 11A

VOUT=Vgfx\_core(1.25V)  
Load line: 6.9mOhm  
L=0.42uF  
Fsw=436KHz  
D=?  
Output Ripple Current=?A  
Output Ripple Voltage=?A\*7.5mOhm=mV  
Input Ripple Current=TDC\*(D\*(1-D))^0.5=?A

Component select  
Input CAP 10uF\_1206\_25V\*2  
Output Cap 330U 2V Y D2 LESR7M S H1.9\*2  
H\_MOSFET SI4362DY(4.2/5.5mOhm@4.5V, 15A)  
Inductor 0.42U\_MPC0740LR42C\_20A(NEC\_TOKIN)



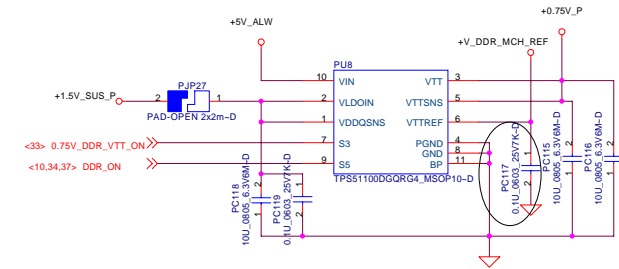
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ADP3209_NB_core			
Size	Document Number	Rev	
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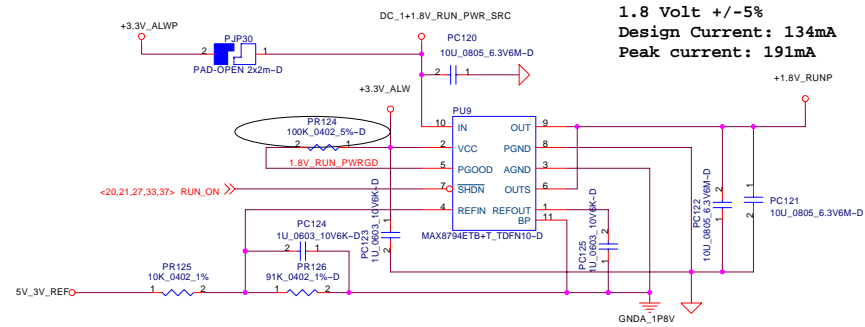
# http://laptopblu.e.vn

## +1.8V RUN/ +0.75V DDR\_VTT

### DDR3 Termination



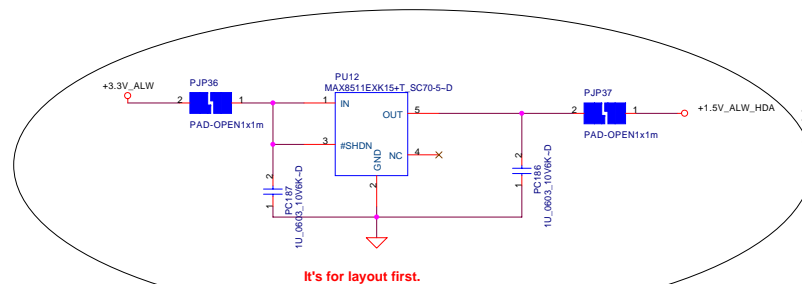
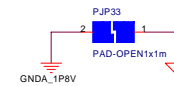
0.75Volt +/-5%  
Thermal Design Current: 0.7A  
Peak current: 1A



1.8 Volt +/-5%  
Design Current: 134mA  
Peak current: 191mA



PGND and GND should be tied together at one point near the GND Pin



1.5 Volt +/-5%  
Design Current: ?mA  
Peak current: ?mA

It's for layout first.

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+1.8VRUN/ +0.75V\_DDR\_VT

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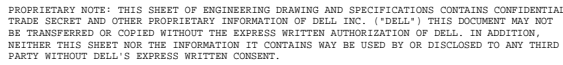


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## Charger

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<b>Charger</b>			
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*Version Change List ( P. I. R. List )*

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*P. I. R. List*) <http://laptopblue.vn>

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