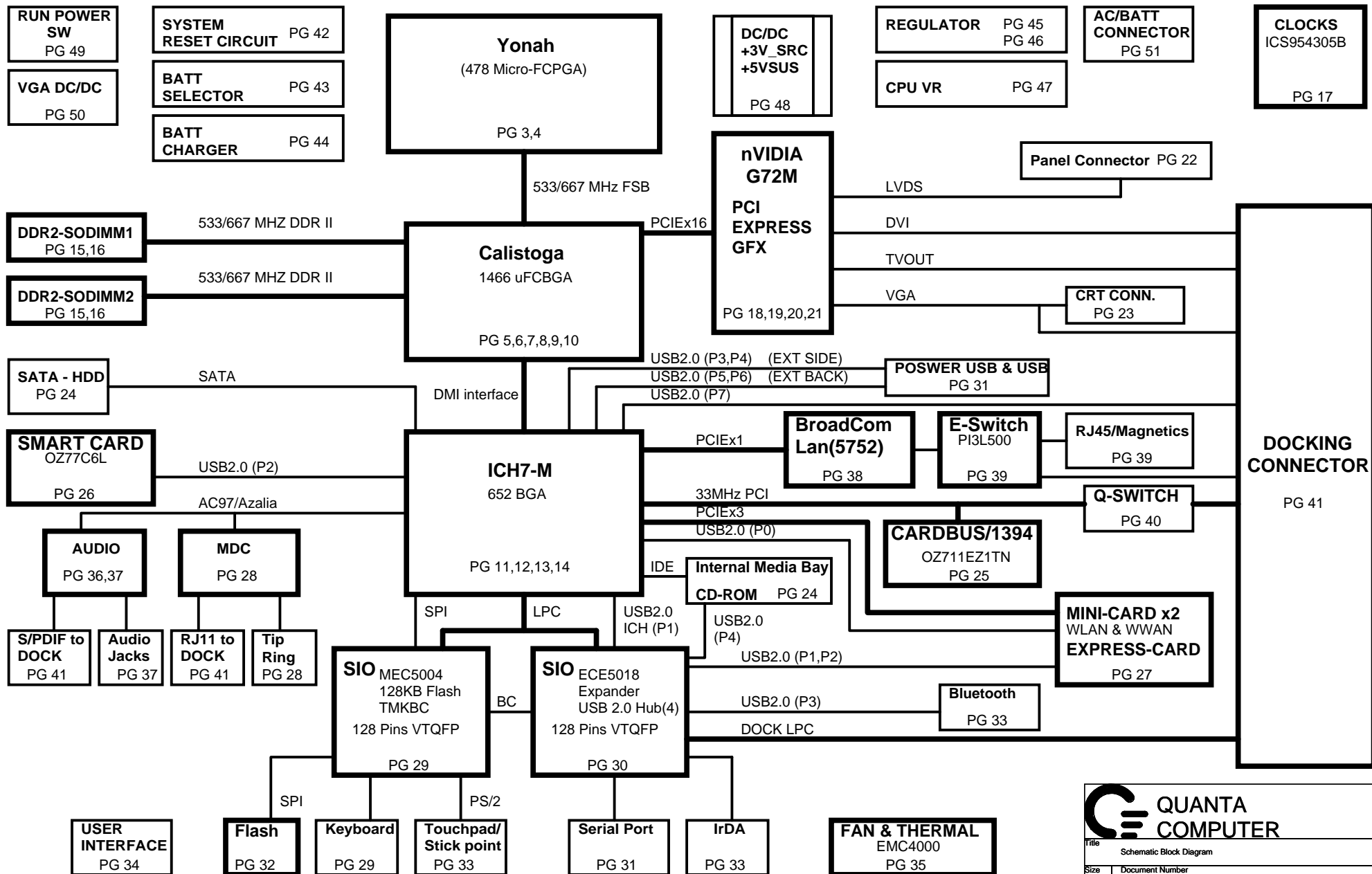


**PWA XD617, PWB FF094,
SCHEM YD536. (256MB)
VER : 2A**




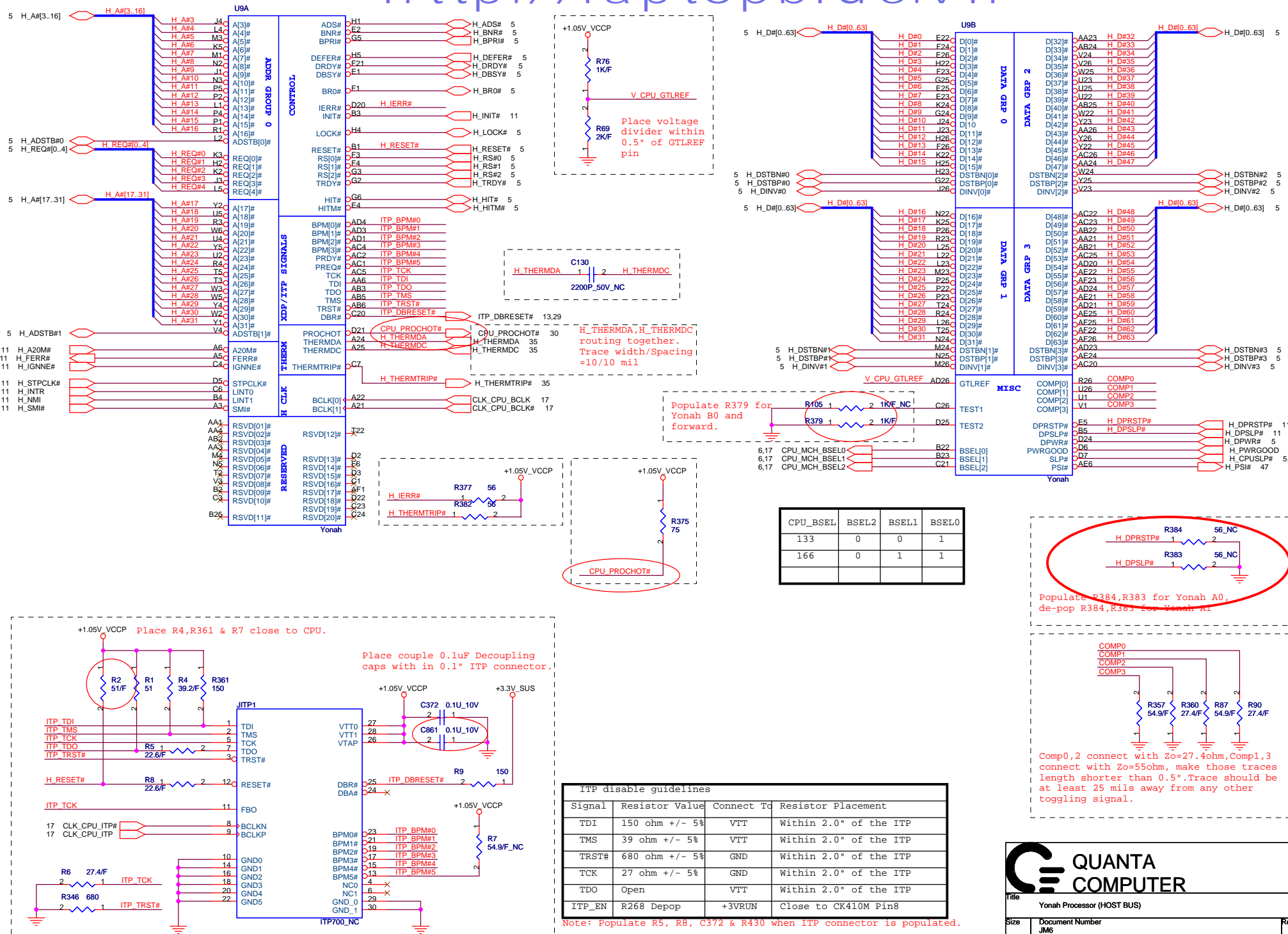
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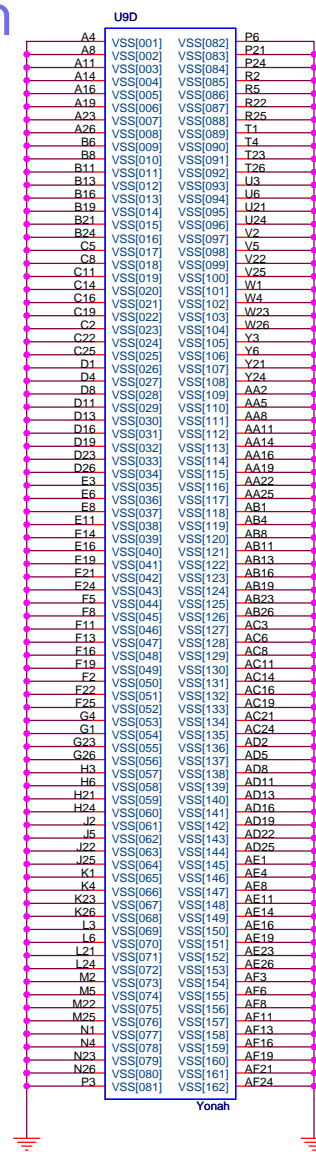
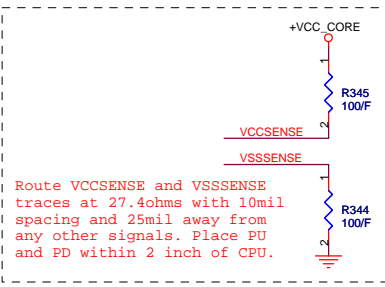
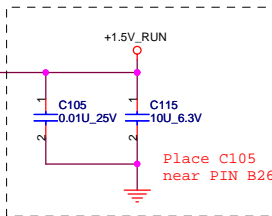
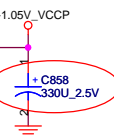
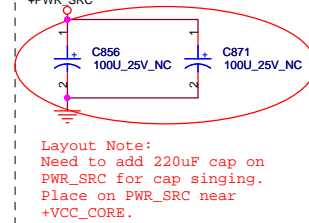
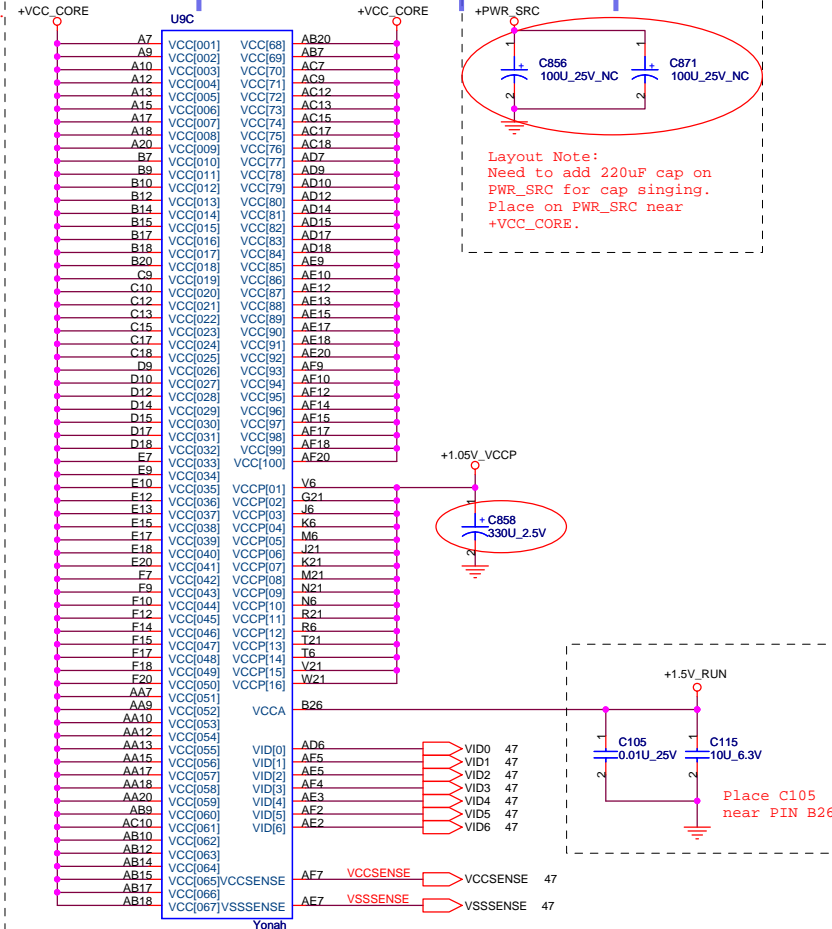
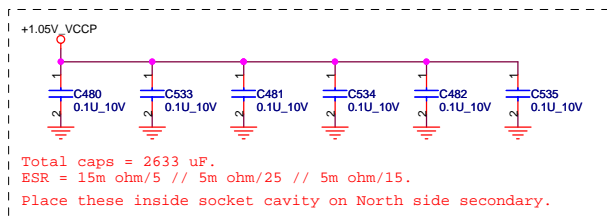
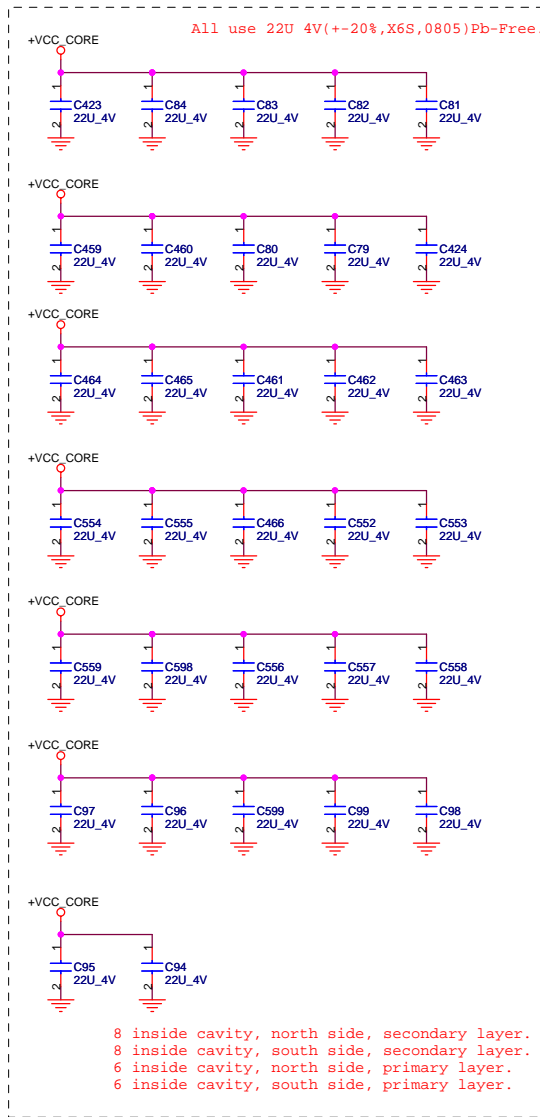
| Pg# | Description | DNI LIST |
|-------|----------------------------------|----------|
| 1 | Schematic Block Diagram | |
| 2 | Front Page | |
| 3-4 | Yonah | |
| 5-10 | Calistoga | |
| 11-14 | ICH7 | |
| 15-16 | DDR2 SO-DIMM(200P) | |
| 17 | Clock Generator | |
| 18-21 | VGA | |
| 22 | LCD Conn. & SSP | |
| 23 | CRT Conn | |
| 24 | SATA & IDE Conn | |
| 25 | PCCARD/Conn & 1394 | |
| 26 | Express Card & Smart Card | |
| 27 | Mini Card | |
| 28 | MDC Conn. | |
| 29 | SIO (MEC5004) | |
| 30 | SIO (MEC5018) | |
| 31 | SERIAL PORT & USB | |
| 32 | Flash ROM & RTC Circuit | |
| 33 | TP,BT & FIR | |
| 34 | Switch,Keyboard & LED | |
| 35 | FAN & Thermal | |
| 36-37 | Audio CODEC(STAC9200)/Phone Jack | |
| 38-39 | LOM (BCM5752)/Switch | |
| 40-41 | Docking Conn/Q-Switch | |
| 42 | System Reset Circuit | |
| 43-44 | Battery Selector & Charger | |
| 45 | DDR2_1.8VSUS, 0.9V | |
| 46 | 1.5VSUS,1.05V(VTT) | |
| 47 | CPU Power | |
| 48 | D/D Power | |
| 49 | RUN Power Switch | |
| 50 | VGA DC/DC | |
| 51 | DCIN/Batt Conn. | |
| 52 | PAD& SCREW | |
| 53 | SMBUS BLOCK | |

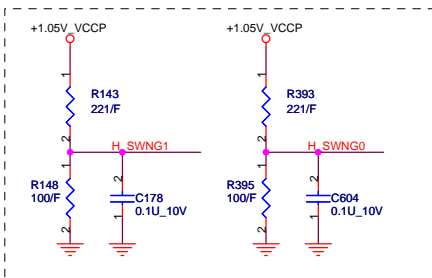
Power & Ground

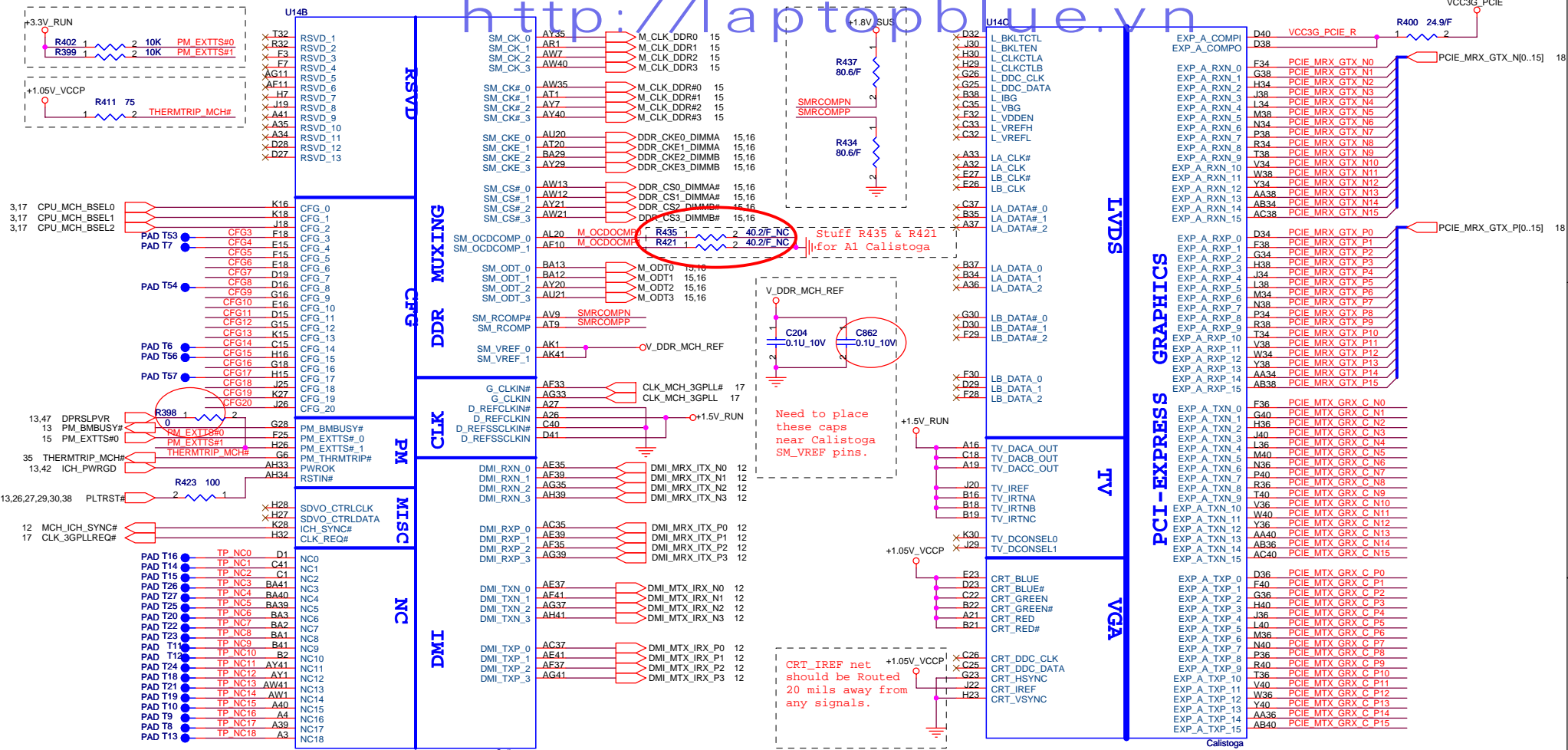
| Label | Pg# | Description | Control Signal |
|---|-----------|-----------------------------|----------------|
| DC_IN+ | | AC ADAPTER (20V) | |
| PBATT+ | | MAIN BATTERY + (10~17V) | |
| PWR_SRC | | MAIN POWER (10~20V) | |
| RTC_PWR3_3V | | RTC & PCL POWER (3_3V) | |
| +12V | | +12V | DRUNPWROK |
| VHCORE | | CPU CORE POWER (1.25/1.15V) | RUNPWROK |
| V1_2RUN | | AGTL+ POWER (1.2V) | RUNPWROK |
| | | | |
| +3VRUN | | SLP_S3# CTRLD POWER | RUN_ON |
| +3VSUS | | SLP_S5# CTRLD POWER | SUS_ON |
| +5VALW | | 8051 POWER (5V) | |
| +5VRUN | | SLP_S3# CTRLD POWER | RUN_ON |
| +5VSUS | | SLP_S5# CTRLD POWER | SUS_ON |
| +5VHDD | | HDD POWER (5V) | HDDC_EN# |
| +5VMOD | | MODULE POWER (5V) | MODC_EN# |
| STRB#5V | | EXTERNAL FDD POWER (5V) | FDD/LPT# |
| +5VFAN1, +5VFAN2 | | FAN POWER (5V) | FAN_OFF/ON# |
| VDDA | | AUDIO ANALOG POWER (5V) | RUN_ON |
| 1_8VSUS | | RESUME WELL IN ICH | |
| 1_8VRUN | | SLP_S3# CTRLD POWER | |
| +3VALW | | 8051 POWER (3V) | |
| V1_5RUN | | AGP I/O POWER | |
| | | | |
|  GND | ALL PAGES | DIGITAL GROUND | |
| | | | |
|  GNDP | | CPU POWER GND | |
|  CGNDP | | CHARGER GND | |
|  DGNDP | | DC/DC POWER GND | |
| LANGND | | COMBO CONN GND | |

| | | |
|--|---------------------|--------|
|  QUANTA COMPUTER | | |
| Title Index, DNI, Power & Ground | | |
| Size | Document Number JM6 | Rev 2A |
| Date: Thursday, September 08, 2005 | Sheet 2 | of 54 |

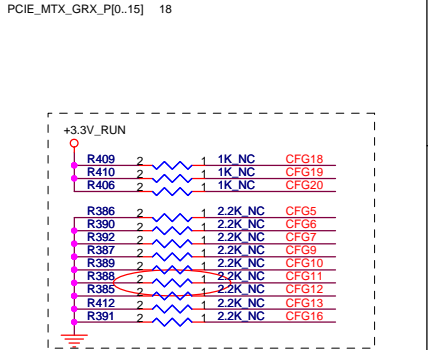
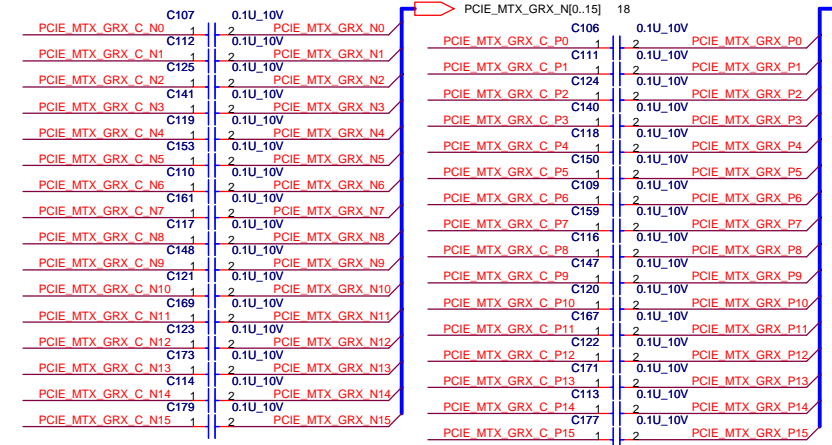









| | |
|---|--|
| CFG5 | Low=DMiX2 High=DMiX4 |
| CFG6 | Low=Moby Disk High=Calistoga. |
| CFG7 CPU_Strap | Low=RSVD High=Mobile CPU |
| CFG9 PCIe Graphics Lane | Low= Reverse Lane High=Normal operation |
| CFG10 Host PLL VCC Select | Low=Reserved High=Mobility |
| CFG11 PSB 4X CLK Enable | Low=Calistoga High=Reserved |
| CFG[13:12] | 00=Reserved. 01=XOR Mode Enable. 11=Normal operation. |
| CFG16 FSB Dynamic ODT | Low=Dynamic ODT Disable High=Dynamic ODT Enable |
| CFG18 VCC Select | Low=1.05V High=1.5V |
| CFG19 DMI Lane Reversal | Low=Normal High=Lane Reversed |
| CFG20 PCIe Backward Interpoerability mode | Low=Only SDVO or PCIeI1 is operational (defaults) High=SDVO and PCIeI1 are operating simultaneously via PEG port |
| SDVO_CTRLDATA | Low=No SDVO device present. High=SDVO device present. |





QUANTA

COMPUTER

Title

Calistoga (VGA,DMI)

Size

Document Number

JM6

Date:

Thursday, September 08, 2005

Sheet

6

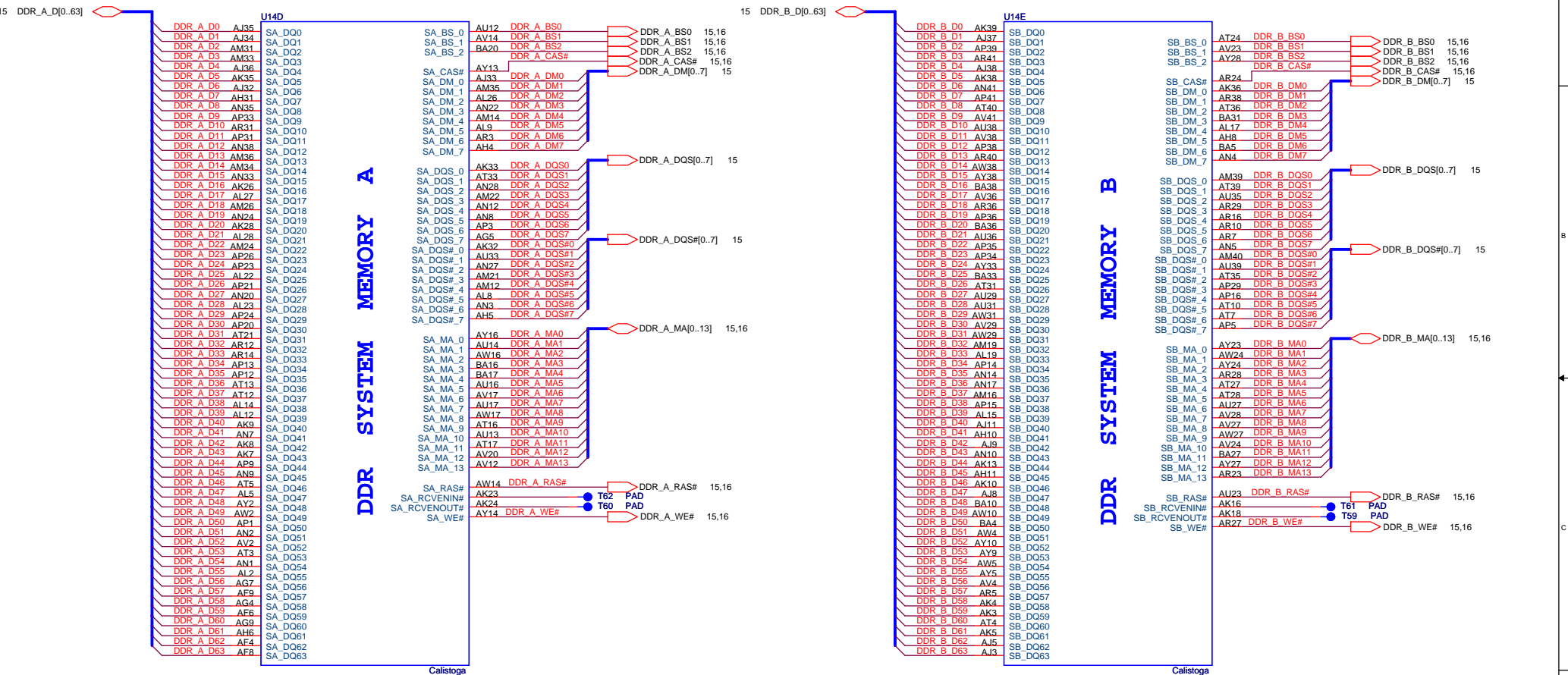
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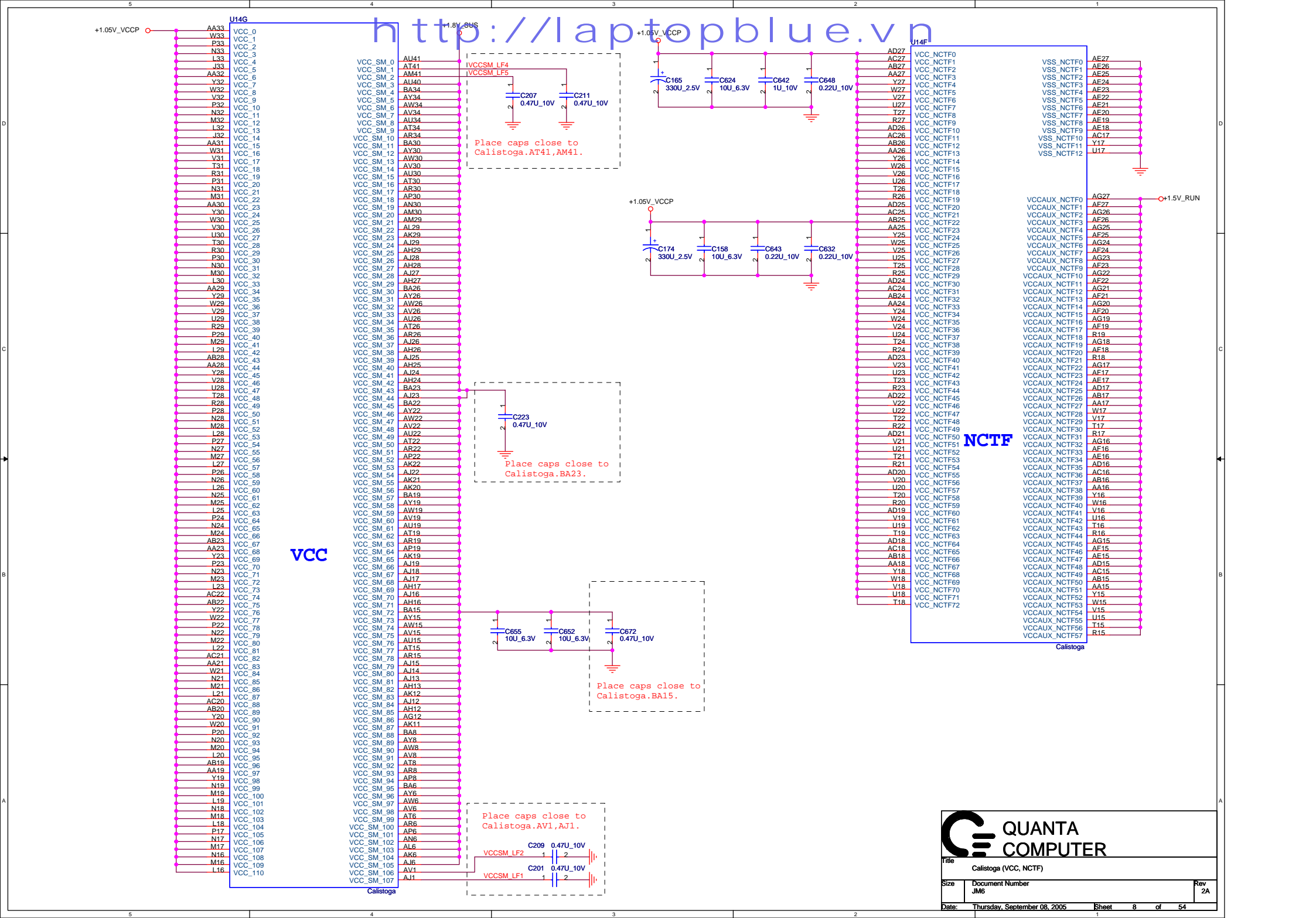
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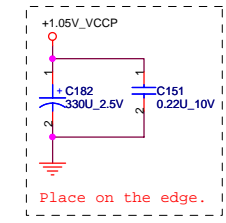
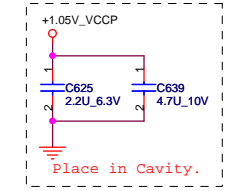
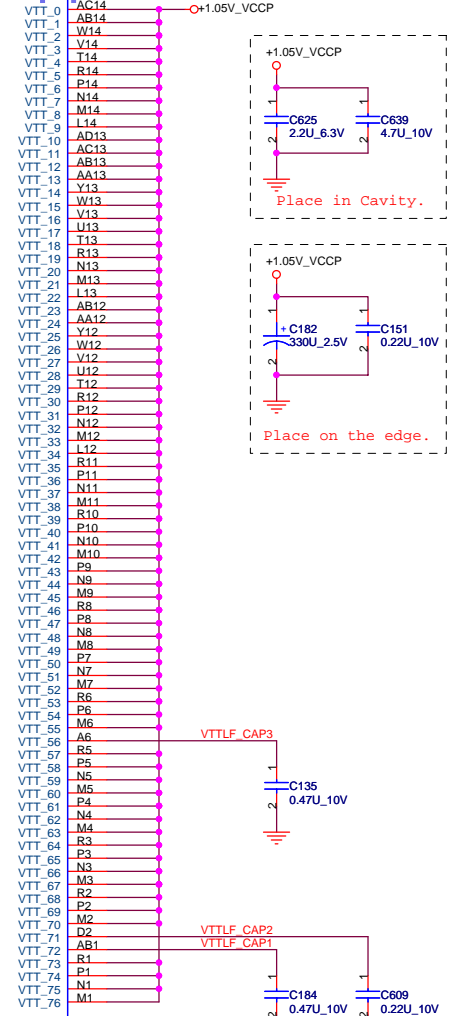
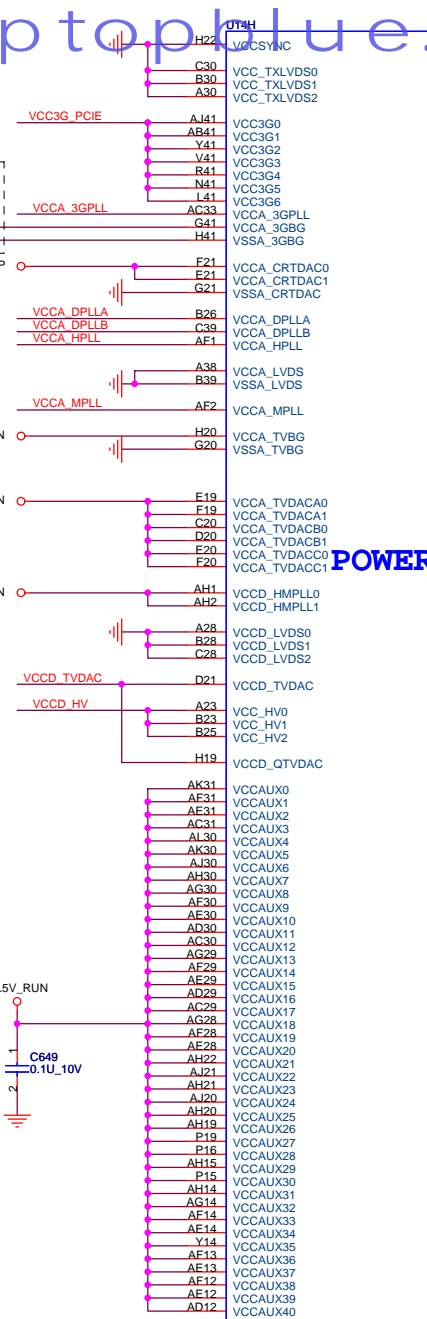
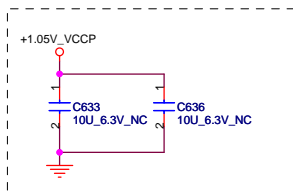
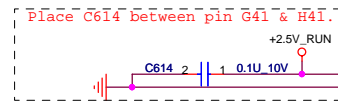
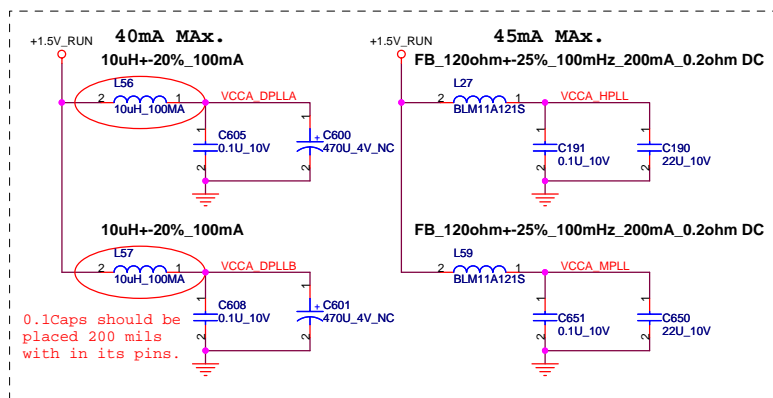
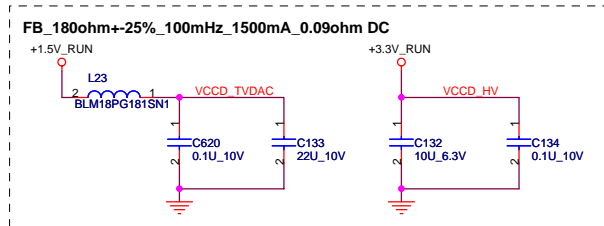
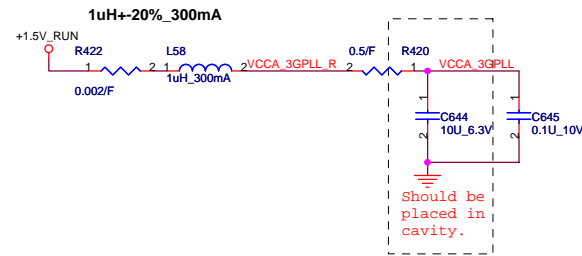
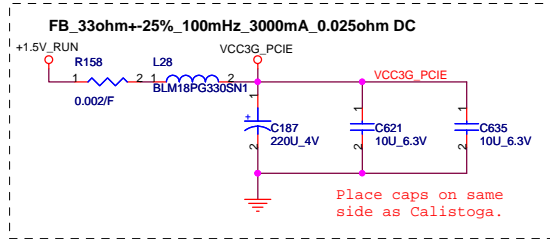
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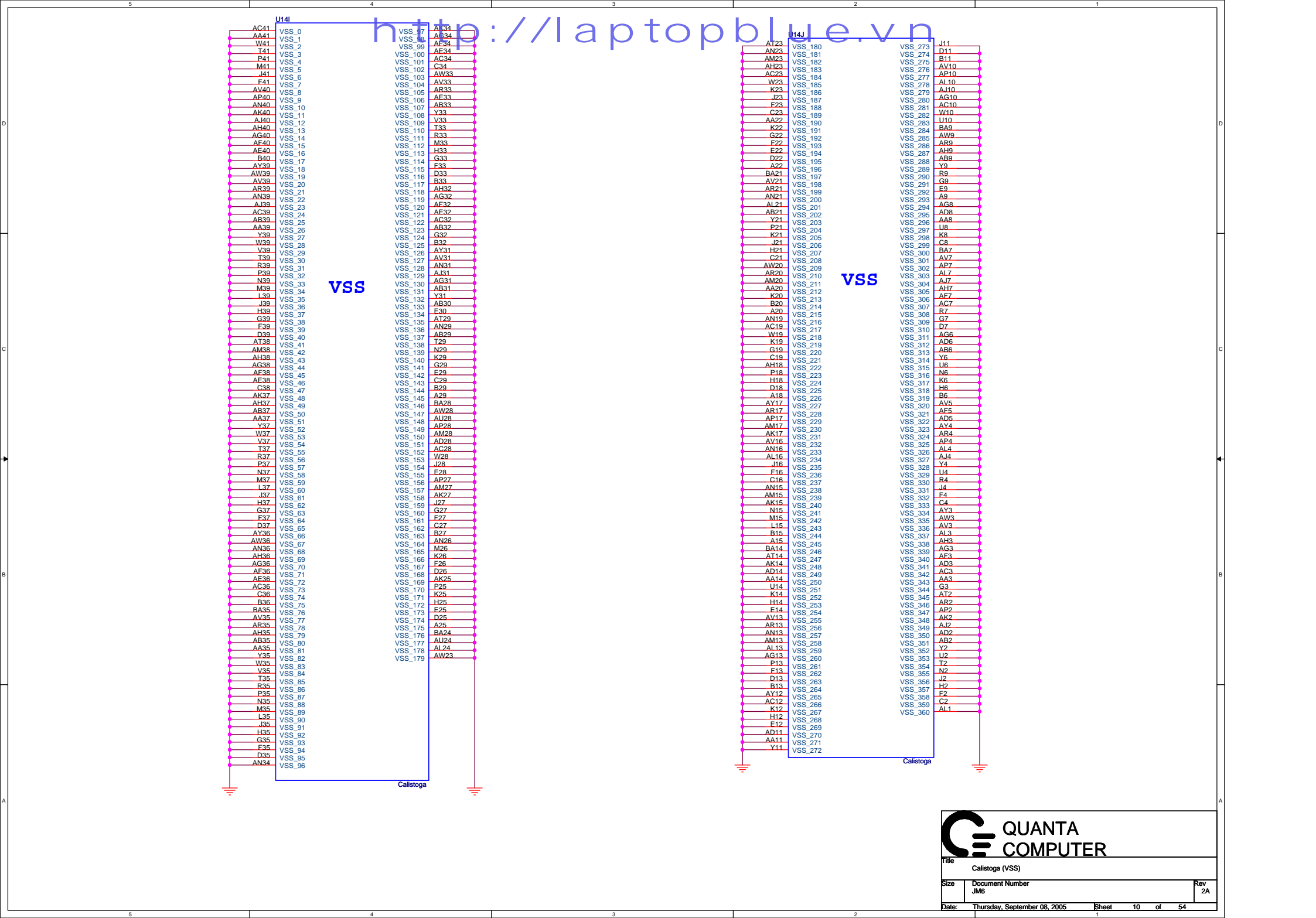
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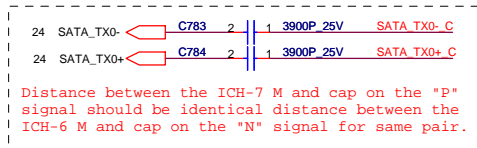
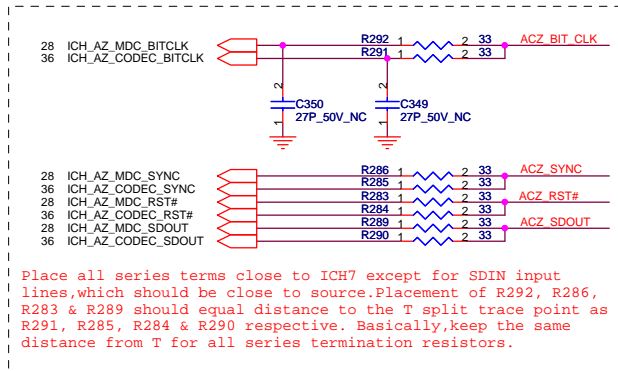
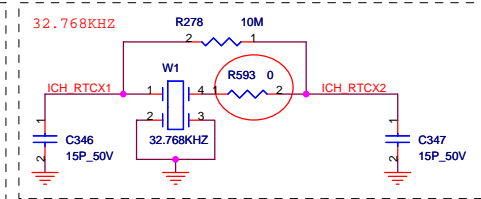
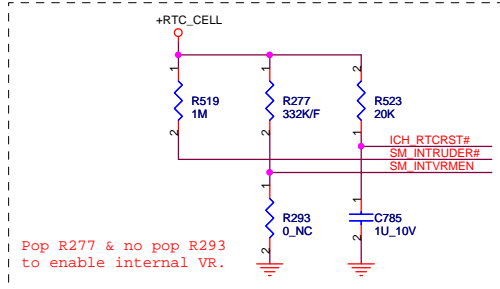
DC Blocked Cap.



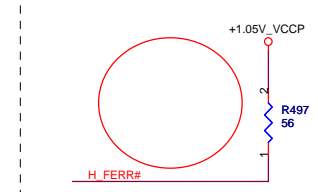
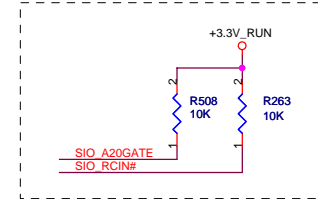
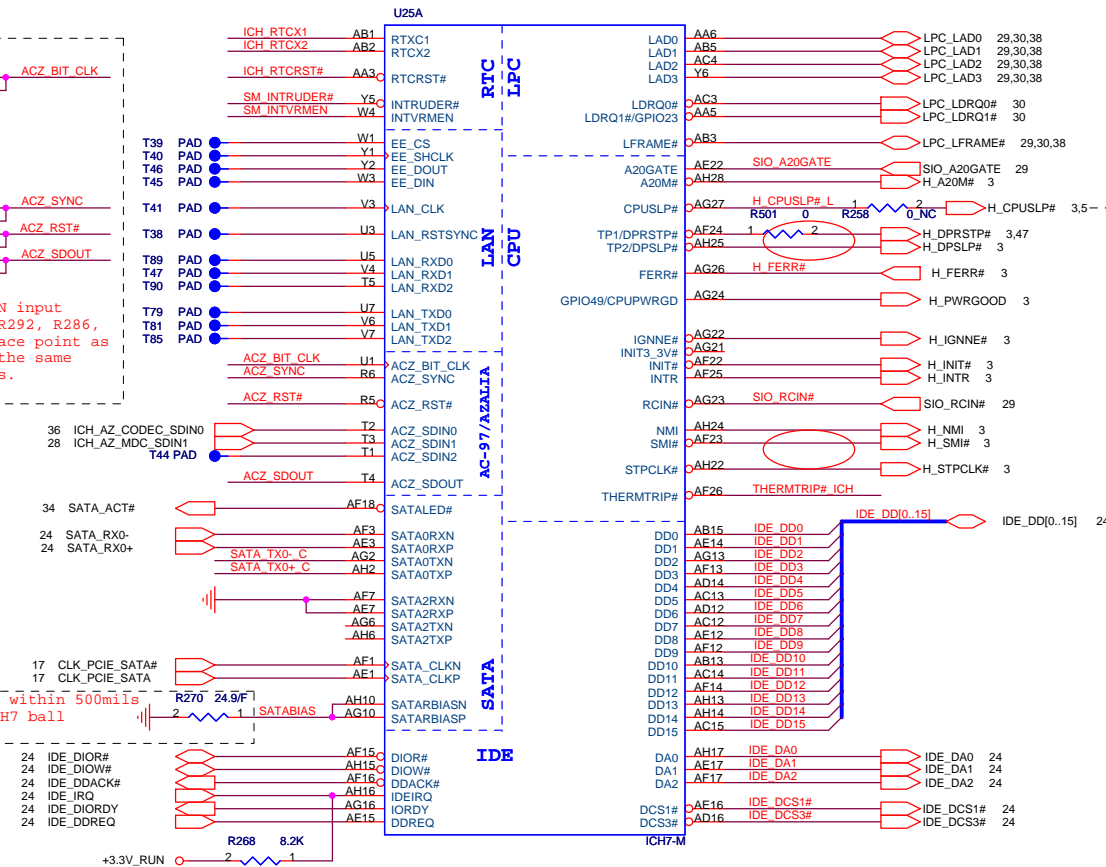




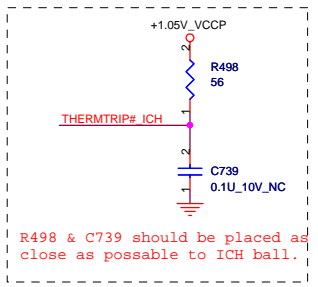


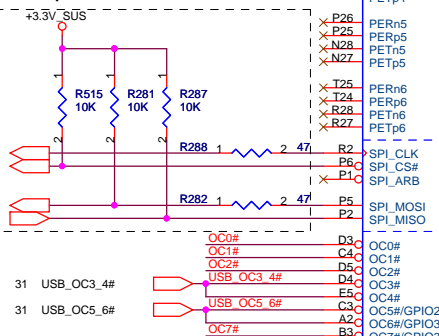
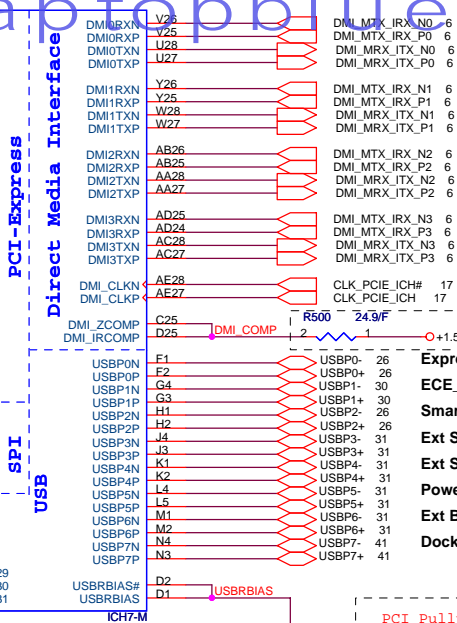
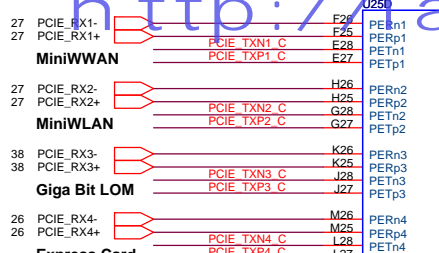


Place within 500mils of ICH7 ball



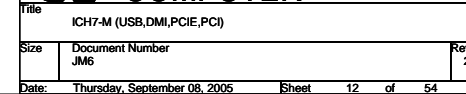
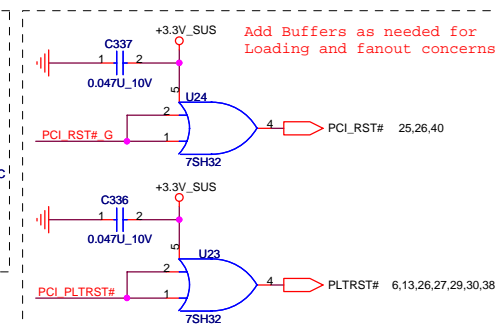
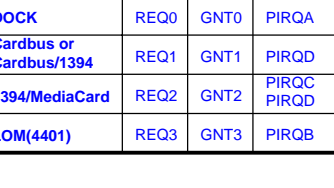
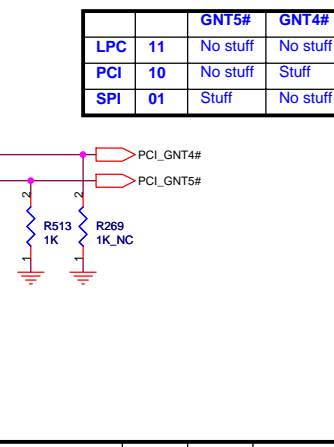
Depop R258 if the MCH is driving CPUSLP# to the CPU. Place the resistors from ICH & MCH close together minimize stubs for either pop option.

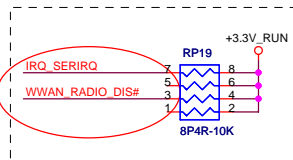
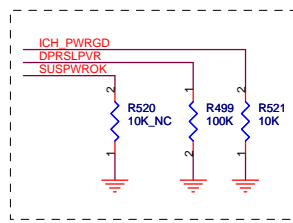
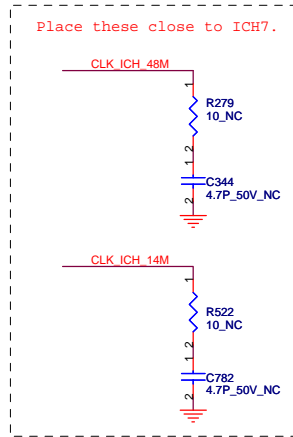
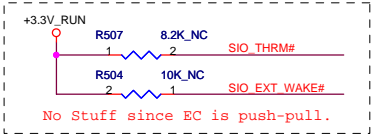
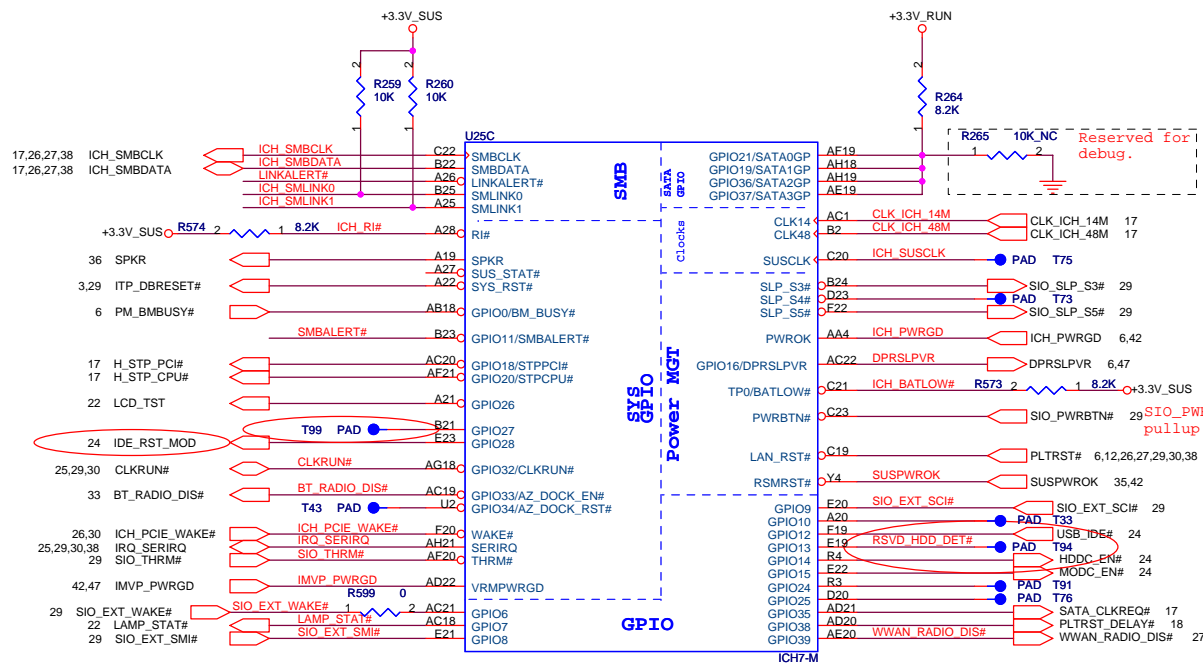
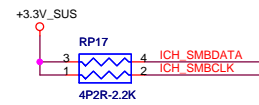
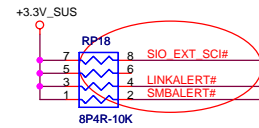
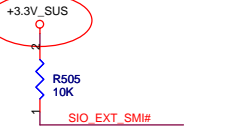
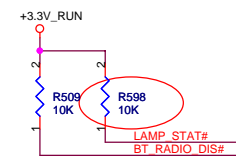
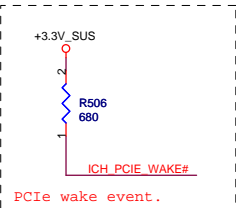
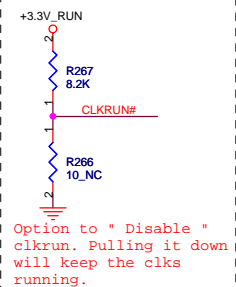


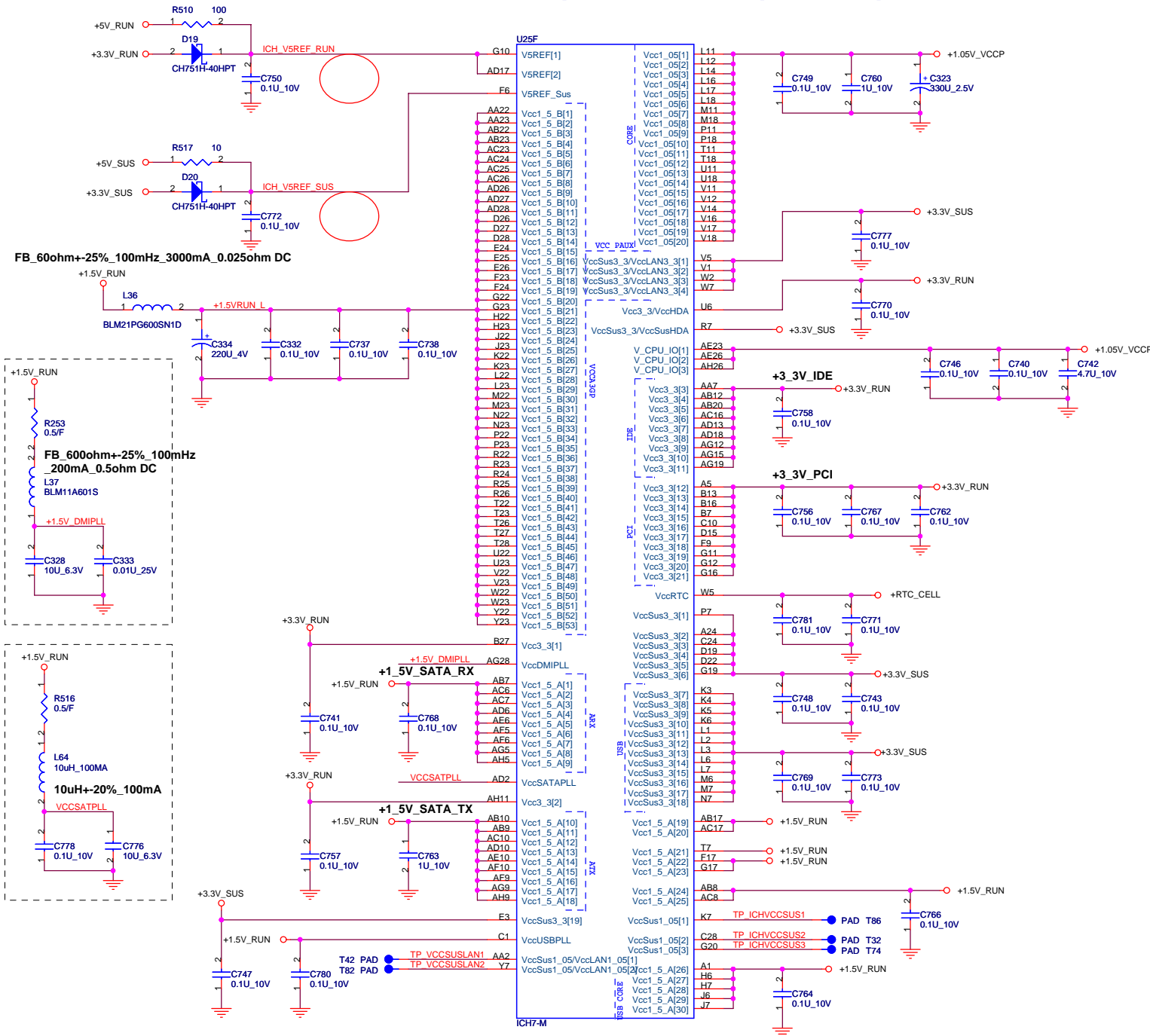


Place within 500mils of ICH7

| | | GNT5# | GNT4# |
|-----|----|----------|----------|
| LPC | 11 | No stuff | No stuff |
| PCI | 10 | No stuff | Stuff |
| SPI | 01 | Stuff | No stuff |

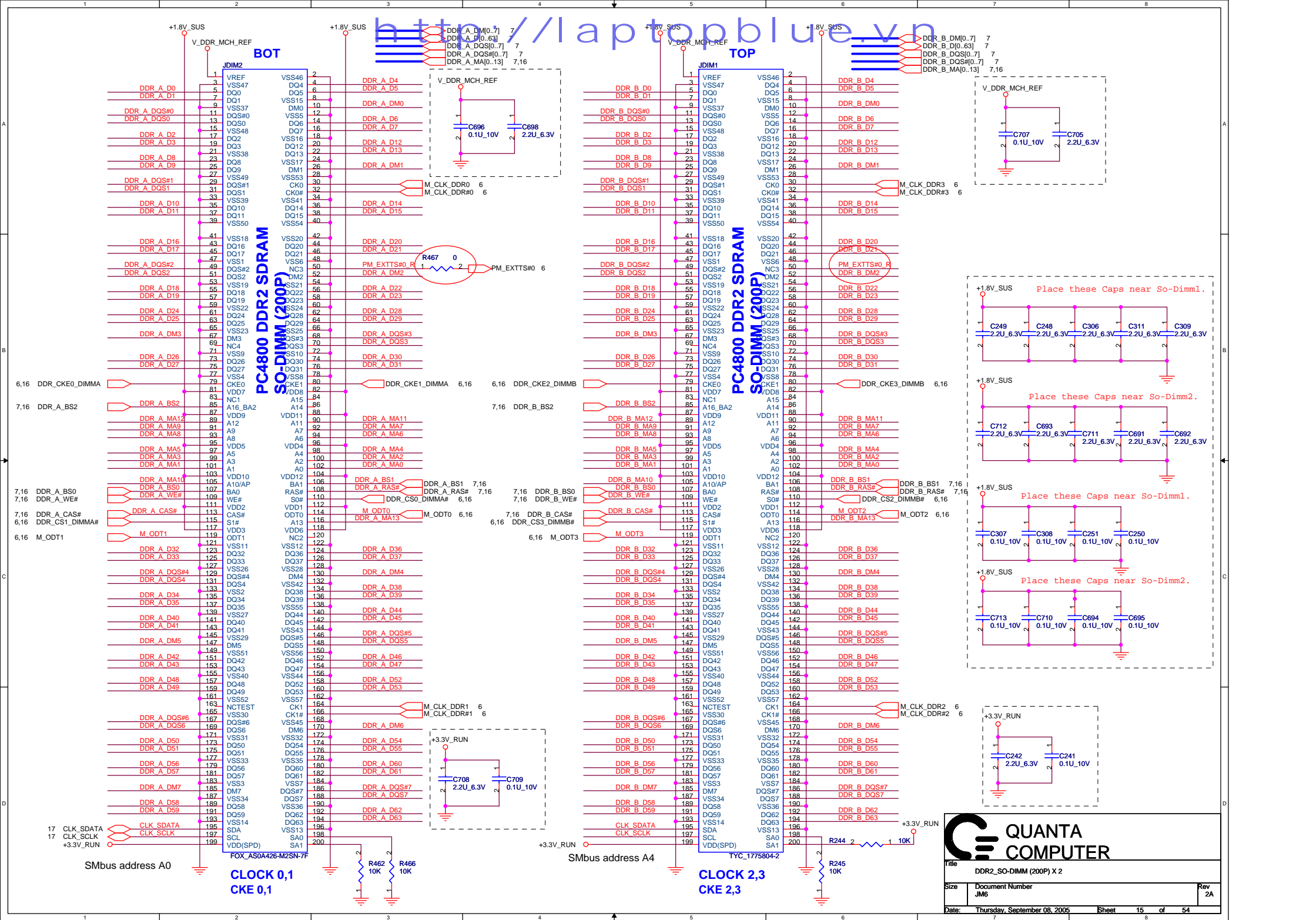


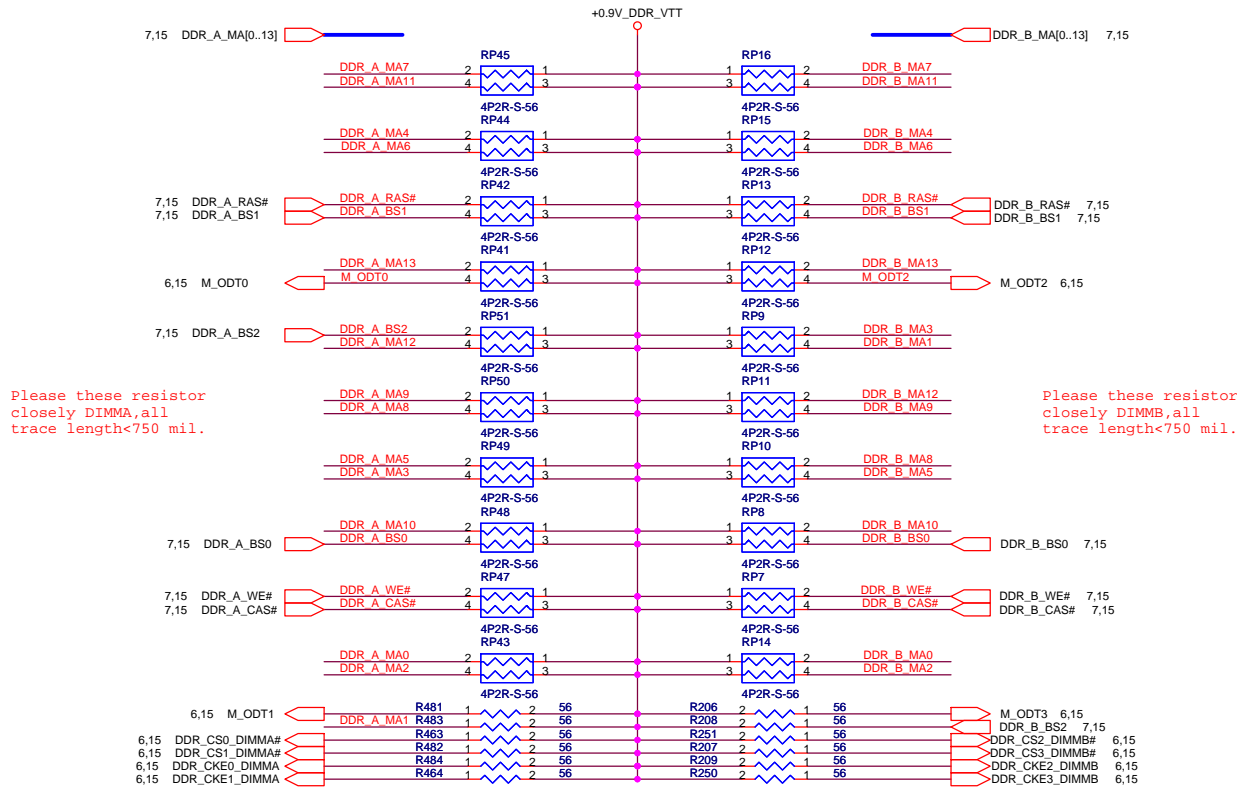
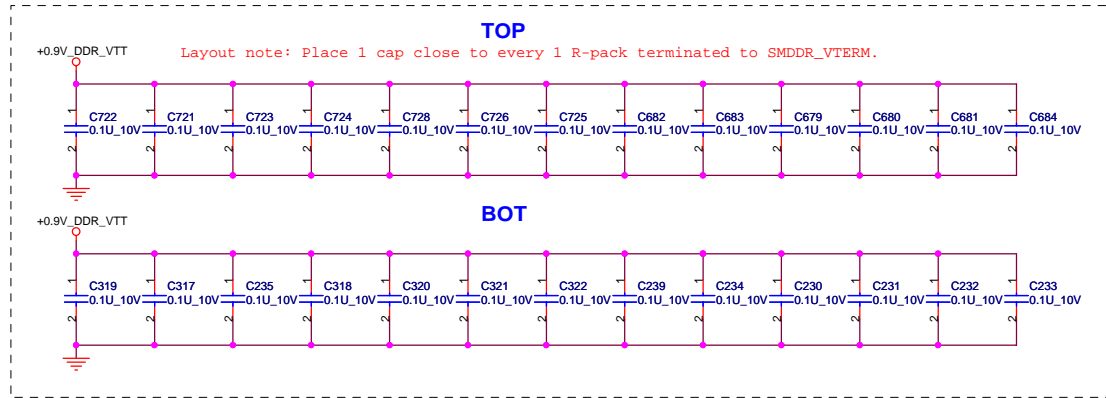


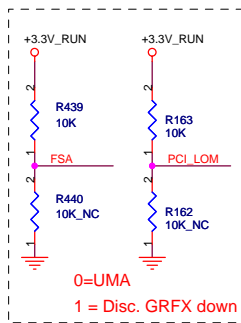


| U25E | | |
|------|---------|-----|
| A4 | VSS[1] | P28 |
| A23 | VSS[2] | R1 |
| B1 | VSS[3] | R11 |
| B8 | VSS[4] | R12 |
| B11 | VSS[5] | R13 |
| B14 | VSS[6] | R14 |
| B17 | VSS[7] | R15 |
| B20 | VSS[8] | R16 |
| B26 | VSS[9] | R17 |
| B28 | VSS[10] | R18 |
| C6 | VSS[11] | T6 |
| C27 | VSS[12] | T12 |
| D10 | VSS[13] | T13 |
| D13 | VSS[14] | T14 |
| D21 | VSS[15] | T15 |
| D24 | VSS[16] | T16 |
| E1 | VSS[17] | T17 |
| E2 | VSS[18] | U4 |
| E4 | VSS[19] | U12 |
| E5 | VSS[20] | U13 |
| F3 | VSS[21] | U14 |
| F4 | VSS[22] | U15 |
| F5 | VSS[23] | U16 |
| F7 | VSS[24] | U17 |
| F8 | VSS[25] | U18 |
| F9 | VSS[26] | U19 |
| F10 | VSS[27] | U20 |
| F11 | VSS[28] | U21 |
| F12 | VSS[29] | U22 |
| F13 | VSS[30] | U23 |
| F14 | VSS[31] | U24 |
| F15 | VSS[32] | U25 |
| F16 | VSS[33] | U26 |
| F17 | VSS[34] | U27 |
| F18 | VSS[35] | U28 |
| F19 | VSS[36] | U29 |
| F20 | VSS[37] | U30 |
| F21 | VSS[38] | U31 |
| F22 | VSS[39] | U32 |
| F23 | VSS[40] | U33 |
| F24 | VSS[41] | U34 |
| F25 | VSS[42] | U35 |
| F26 | VSS[43] | U36 |
| F27 | VSS[44] | U37 |
| F28 | VSS[45] | U38 |
| F29 | VSS[46] | U39 |
| F30 | VSS[47] | U40 |
| F31 | VSS[48] | U41 |
| F32 | VSS[49] | U42 |
| F33 | VSS[50] | U43 |
| F34 | VSS[51] | U44 |
| F35 | VSS[52] | U45 |
| F36 | VSS[53] | U46 |
| F37 | VSS[54] | U47 |
| F38 | VSS[55] | U48 |
| F39 | VSS[56] | U49 |
| F40 | VSS[57] | U50 |
| F41 | VSS[58] | U51 |
| F42 | VSS[59] | U52 |
| F43 | VSS[60] | U53 |
| F44 | VSS[61] | U54 |
| F45 | VSS[62] | U55 |
| F46 | VSS[63] | U56 |
| F47 | VSS[64] | U57 |
| F48 | VSS[65] | U58 |
| F49 | VSS[66] | U59 |
| F50 | VSS[67] | U60 |
| F51 | VSS[68] | U61 |
| F52 | VSS[69] | U62 |
| F53 | VSS[70] | U63 |
| F54 | VSS[71] | U64 |
| F55 | VSS[72] | U65 |
| F56 | VSS[73] | U66 |
| F57 | VSS[74] | U67 |
| F58 | VSS[75] | U68 |
| F59 | VSS[76] | U69 |
| F60 | VSS[77] | U70 |
| F61 | VSS[78] | U71 |
| F62 | VSS[79] | U72 |
| F63 | VSS[80] | U73 |
| F64 | VSS[81] | U74 |
| F65 | VSS[82] | U75 |
| F66 | VSS[83] | U76 |
| F67 | VSS[84] | U77 |
| F68 | VSS[85] | U78 |
| F69 | VSS[86] | U79 |
| F70 | VSS[87] | U80 |
| F71 | VSS[88] | U81 |
| F72 | VSS[89] | U82 |
| F73 | VSS[90] | U83 |
| F74 | VSS[91] | U84 |
| F75 | VSS[92] | U85 |
| F76 | VSS[93] | U86 |
| F77 | VSS[94] | U87 |
| F78 | VSS[95] | U88 |
| F79 | VSS[96] | U89 |
| F80 | VSS[97] | U90 |

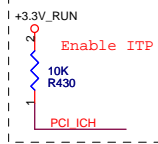
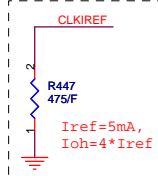
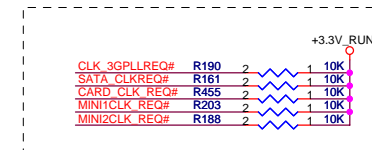
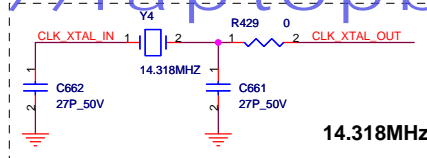
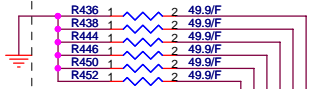






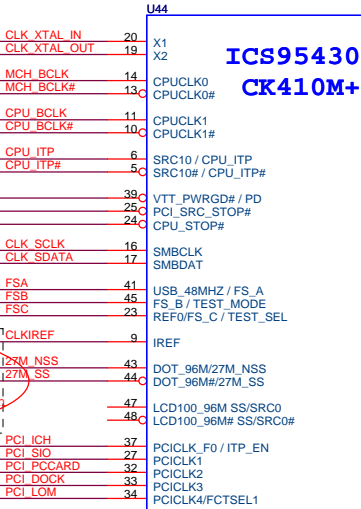
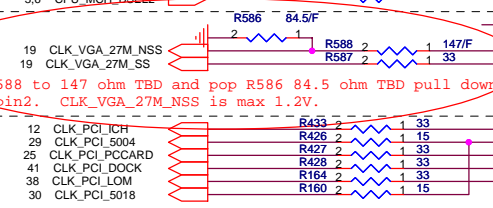


Place these termination to close CK410M.



Discrete

Change R588 to 147 ohm TBD and pop R586 84.5 ohm TBD pull down on R588 pin2. CLK_VGA_27M_NSS is max 1.2V.



ICS954305
CK410M+

POWER PLANE

250mA (MAX.)

ICS_954305DKLFT

THEM PAD

GND48

GNDPCL_0

GNDPCL_1

GNDREF

GND

GNDCPU

GNDPCL_0

GNDPCL_1

GNDREF

GND

GNDCPU

GNDPCL_0

GNDPCL_1

GNDREF

GND

GNDCPU

GNDPCL_0

GNDPCL_1

GNDREF

GND

GNDCPU

GNDPCL_0

GNDPCL_1

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GNDCPU

GNDPCL_0

GNDPCL_1

GNDREF

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GNDCPU

GNDPCL_0

GNDPCL_1

GNDREF

GND

GNDCPU

GNDPCL_0

GNDPCL_1

GNDREF

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GNDCPU

GNDPCL_0

GNDPCL_1

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GNDPCL_0

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GNDREF

GND

GNDCPU

GNDPCL_0

GNDPCL_1

GNDREF

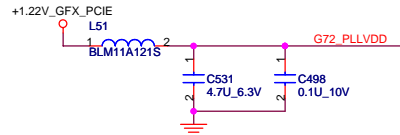
GND

GNDCPU

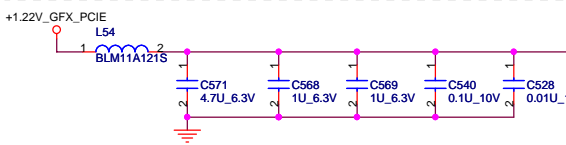
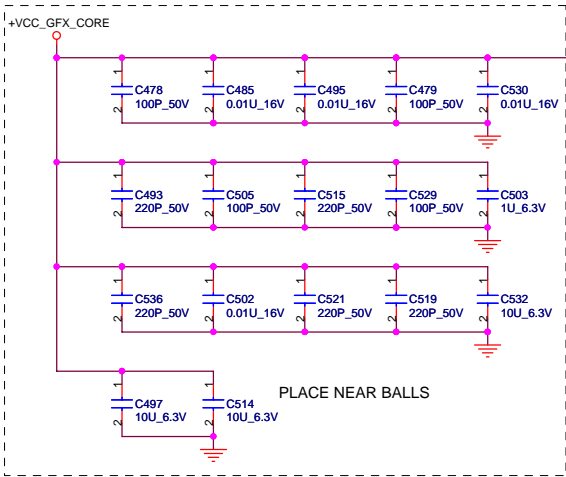
GNDPCL_0

6 PCIE_MTX_GRX_P[0..15]
6 PCIE_MTX_GRX_N[0..15]

6 PCIE_MRX_GTX_P[0..15]



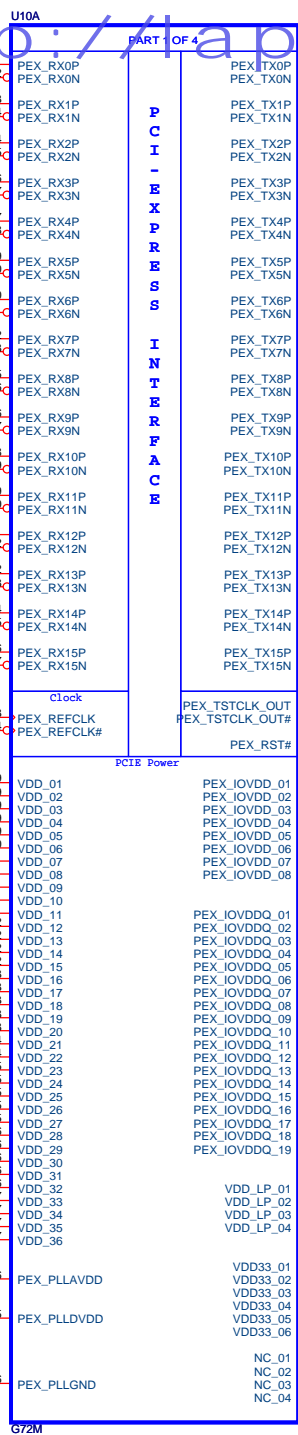
17 CLK_PCIE_VGA
17 CLK_PCIE_VGA#



PCIE_MTX_GRX_P0 AF1
PCIE_MTX_GRX_N0 AG2
PCIE_MTX_GRX_P1 AG3
PCIE_MTX_GRX_N1 AG4
PCIE_MTX_GRX_P2 AF4
PCIE_MTX_GRX_N2 AE5
PCIE_MTX_GRX_P3 AG6
PCIE_MTX_GRX_N3 AG7
PCIE_MTX_GRX_P4 AE7
PCIE_MTX_GRX_N4 AE8
PCIE_MTX_GRX_P5 AG9
PCIE_MTX_GRX_N5 AG10
PCIE_MTX_GRX_P6 AF10
PCIE_MTX_GRX_N6 AE11
PCIE_MTX_GRX_P7 AG12
PCIE_MTX_GRX_N7 AG13
PCIE_MTX_GRX_P8 AG15
PCIE_MTX_GRX_N8 AG16
PCIE_MTX_GRX_P9 AF16
PCIE_MTX_GRX_N9 AE17
PCIE_MTX_GRX_P10 AG18
PCIE_MTX_GRX_N10 AG19
PCIE_MTX_GRX_P11 AF19
PCIE_MTX_GRX_N11 AE20
PCIE_MTX_GRX_P12 AG21
PCIE_MTX_GRX_N12 AG22
PCIE_MTX_GRX_P13 AF22
PCIE_MTX_GRX_N13 AE23
PCIE_MTX_GRX_P14 AG24
PCIE_MTX_GRX_N14 AG25
PCIE_MTX_GRX_P15 AG26
PCIE_MTX_GRX_N15 AE27

VDD_01
VDD_02
VDD_03
VDD_04
VDD_05
VDD_06
VDD_07
VDD_08
VDD_09
VDD_10
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VDD_29
VDD_30
VDD_31
VDD_32
VDD_33
VDD_34
VDD_35
VDD_36

PCIE_PLL_AVDD_Y6
PCIE_PLL_DVDD_AA5
PCIE_PLL_GND_AA6



PCIE_MRX_GTX_C_P0 AD5
PCIE_MRX_GTX_C_N0 AD6
PCIE_MRX_GTX_C_P1 AE6
PCIE_MRX_GTX_C_N1 AE7
PCIE_MRX_GTX_C_P2 AD7
PCIE_MRX_GTX_C_N2 AC7
PCIE_MRX_GTX_C_P3 AE9
PCIE_MRX_GTX_C_N3 AE10
PCIE_MRX_GTX_C_P4 AD10
PCIE_MRX_GTX_C_N4 AC10
PCIE_MRX_GTX_C_P5 AE12
PCIE_MRX_GTX_C_N5 AE13
PCIE_MRX_GTX_C_P6 AD13
PCIE_MRX_GTX_C_N6 AC13
PCIE_MRX_GTX_C_P7 AC15
PCIE_MRX_GTX_C_N7 AD15
PCIE_MRX_GTX_C_P8 AE15
PCIE_MRX_GTX_C_N8 AE16
PCIE_MRX_GTX_C_P9 AC18
PCIE_MRX_GTX_C_N9 AD18
PCIE_MRX_GTX_C_P10 AE18
PCIE_MRX_GTX_C_N10 AE19
PCIE_MRX_GTX_C_P11 AC21
PCIE_MRX_GTX_C_N11 AD21
PCIE_MRX_GTX_C_P12 AE21
PCIE_MRX_GTX_C_N12 AE22
PCIE_MRX_GTX_C_P13 AD22
PCIE_MRX_GTX_C_N13 AD23
PCIE_MRX_GTX_C_P14 AE25
PCIE_MRX_GTX_C_N14 AE25
PCIE_MRX_GTX_C_P15 AE24
PCIE_MRX_GTX_C_N15 AD24

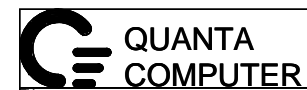
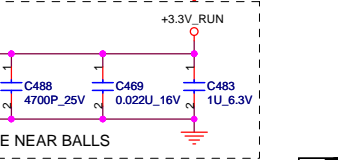
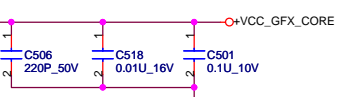
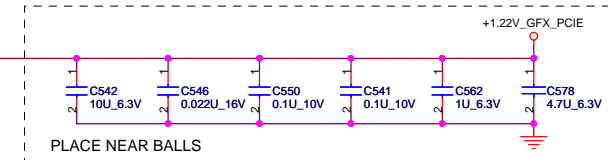
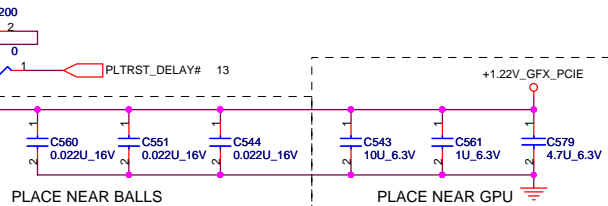
AB10
AB11
AB14
AB15
W17
AB20
AB21

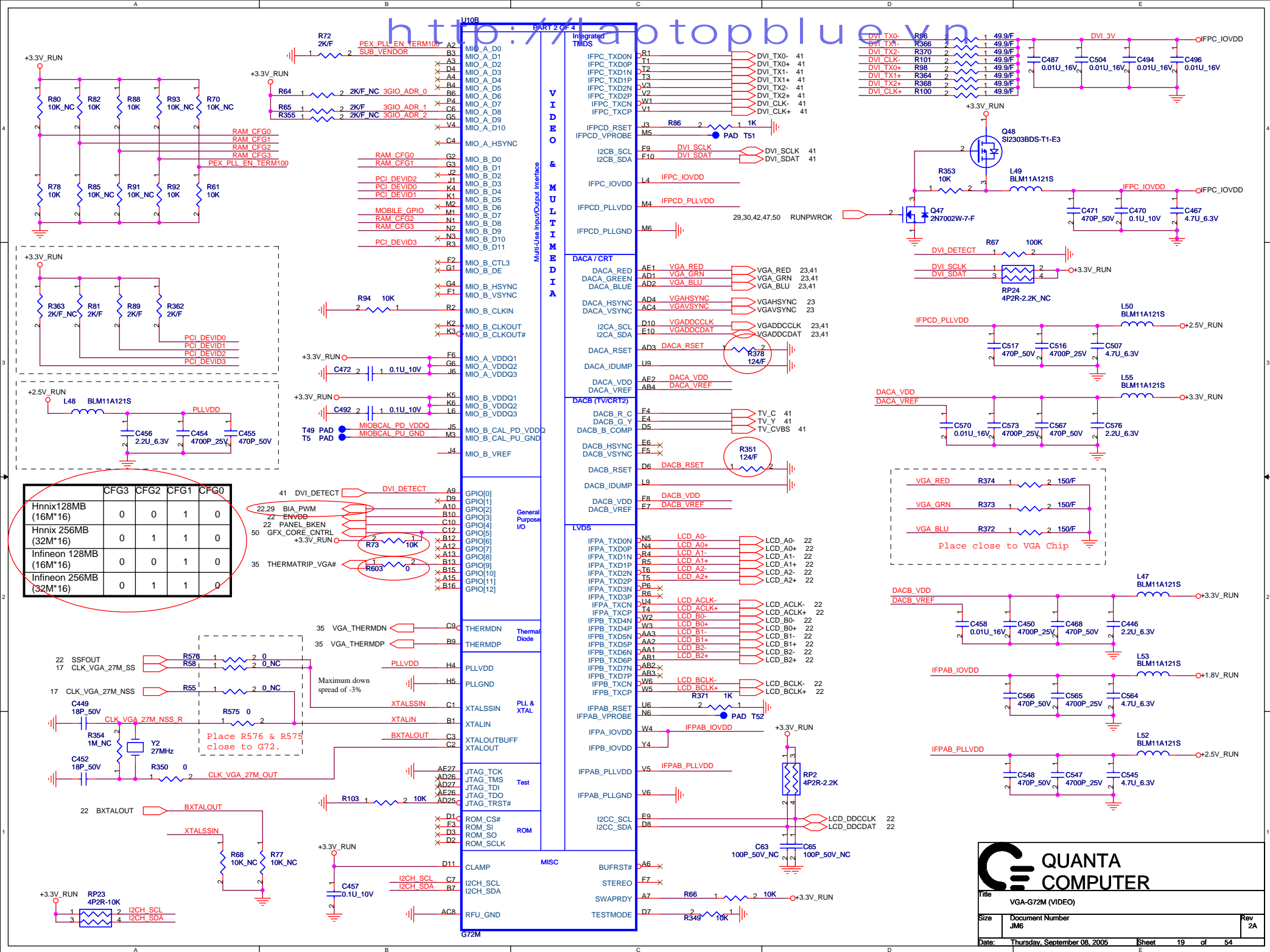
AA4
AB5
AB6
AB7
AB8
AB9
AC9
AC11
AC12
AB13
AB16
AB16
AB17
AC17
AB18
AB19
AC19
AC20

W9
W10
W11
W12

J12
F13
J13
F14
J15
F15
J16
F16
D12
E12
F12
C13

6 PCIE_MRX_GTX_N[0..15]

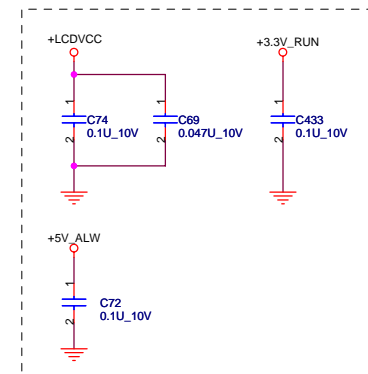
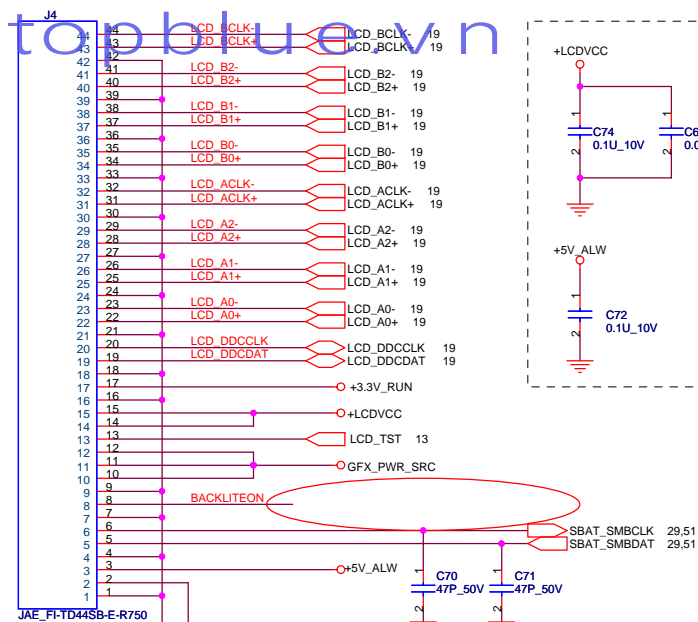
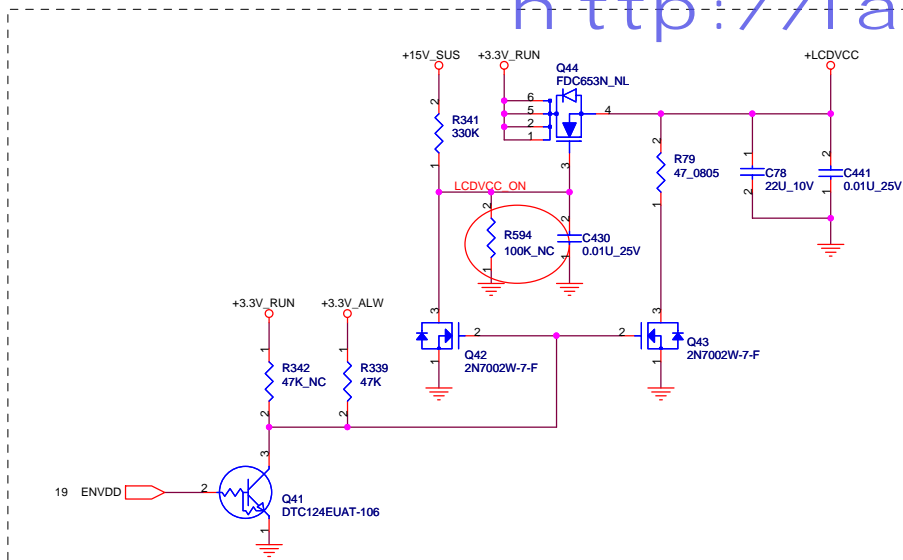




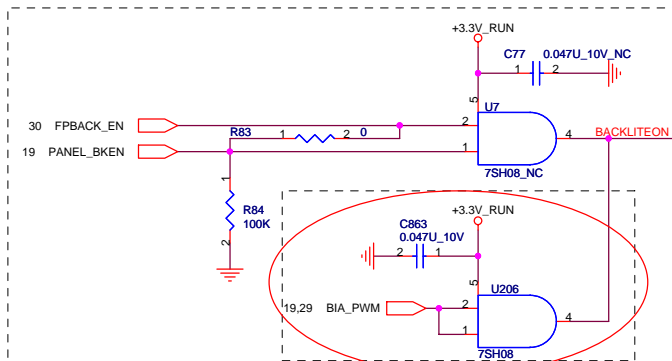


Rev

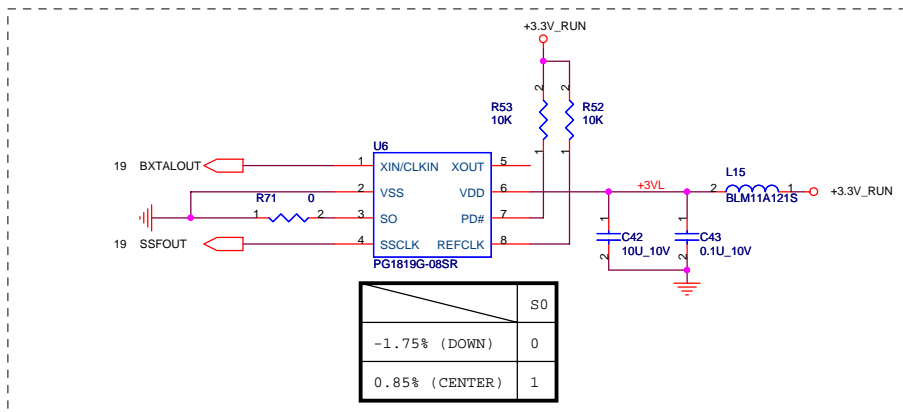
54



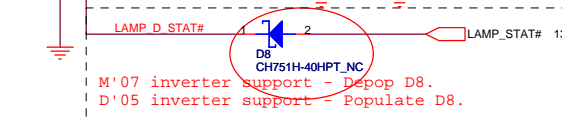
Address : A9H --Contrast
AAH --Backlight



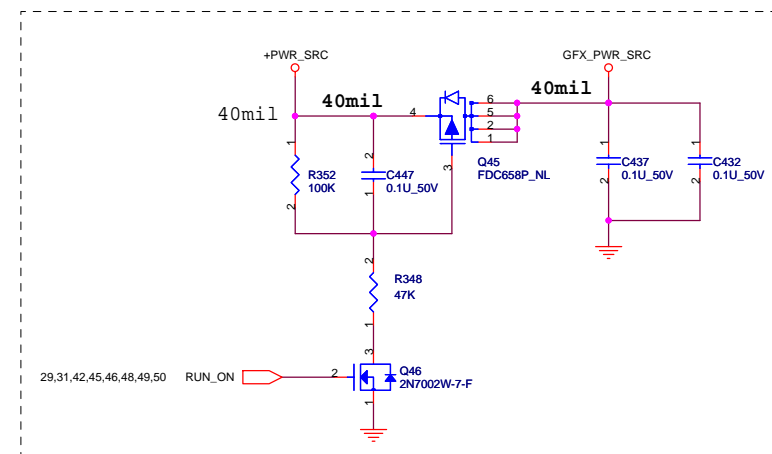
M'07 inverter support - Populate R83,U206,C863 Depop U7,C77.
D'05 inverter support - Populate U7,C77; Depop R83,U206,C863.

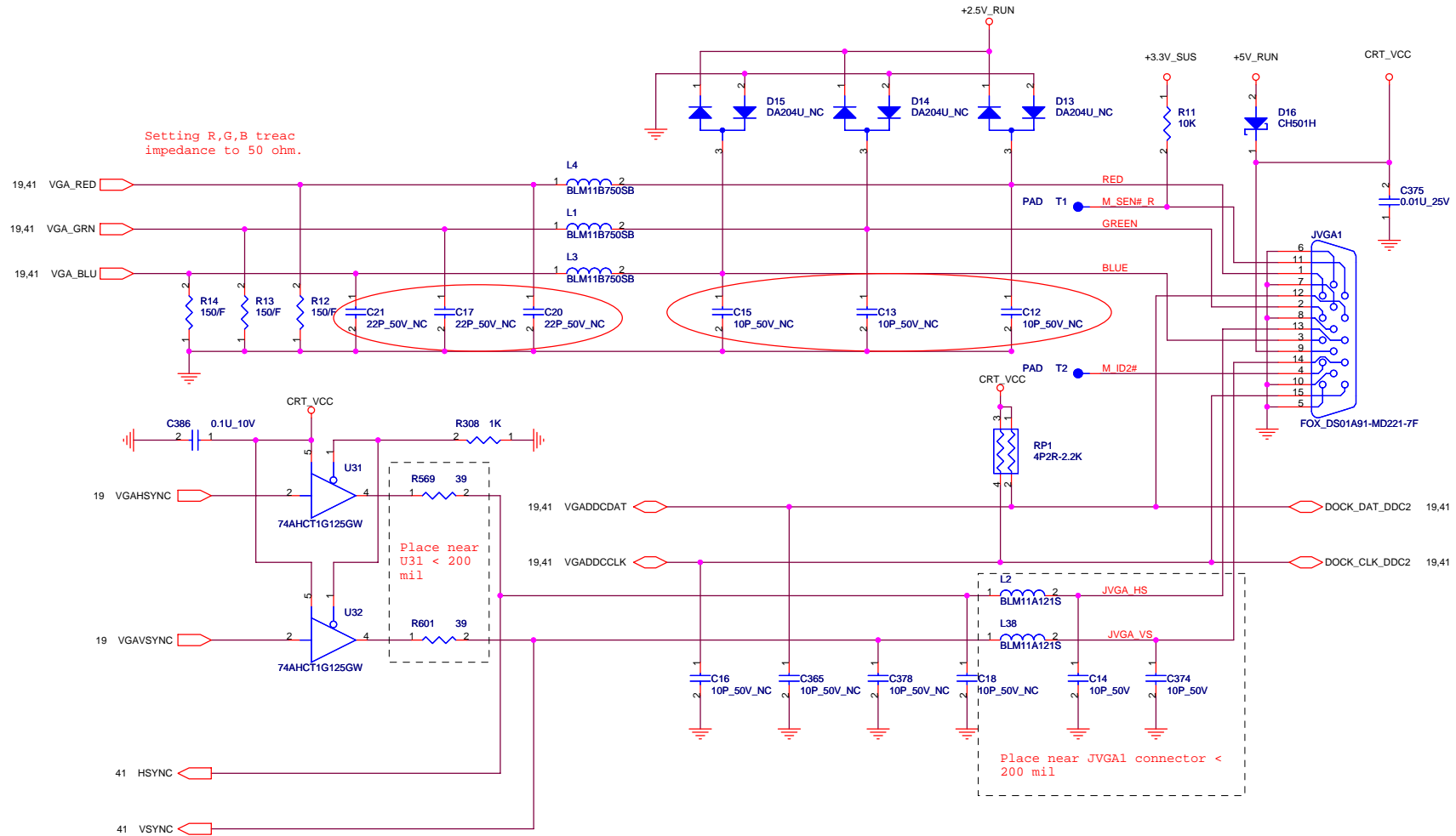


| | S0 |
|----------------|----|
| -1.75% (DOWN) | 0 |
| 0.85% (CENTER) | 1 |



M'07 inverter support - Depop D8.
D'05 inverter support - Populate D8.



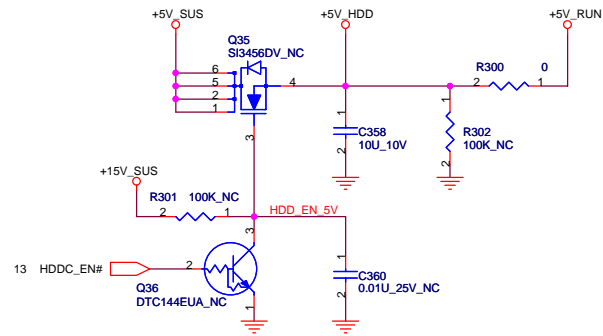


The diagram shows the pin connections for the MLX_67492-1821 connector. The connector is labeled CON6 and has 22 pins. The connections are as follows:

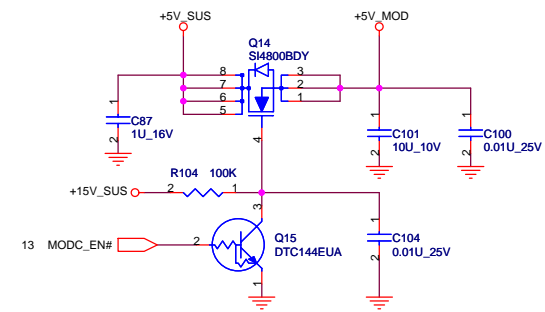
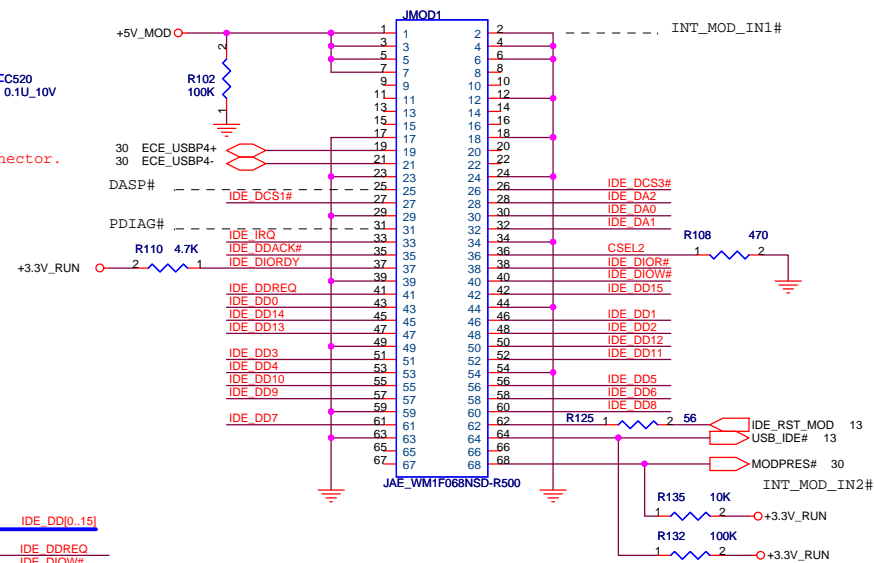
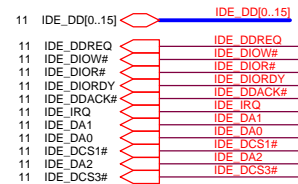
- Pin 1: GND1
- Pin 2: RXN
- Pin 3: TXN
- Pin 4: TXP
- Pin 5: GND3
- Pin 6: 3.3V_0
- Pin 7: 3.3V_1
- Pin 8: 3.3V_2
- Pin 9: GND4
- Pin 10: GND5
- Pin 11: GND6
- Pin 12: 5V_0
- Pin 13: 5V_1
- Pin 14: 5V_2
- Pin 15: GND7
- Pin 16: RSVD
- Pin 17: GND8
- Pin 18: 12V_0
- Pin 19: 12V_1
- Pin 20: 12V_2

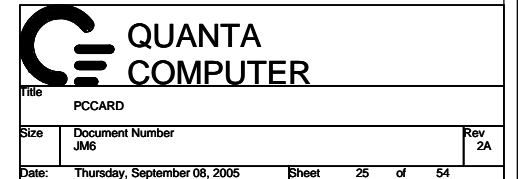
The following table summarizes the connections:

| Pin | Signal | Notes |
|-----|--------|-------------|
| 1 | GND1 | |
| 2 | RXN | SATA_RXN0_C |
| 3 | TXN | SATA_RXP0_C |
| 4 | TXP | |
| 5 | GND3 | |
| 6 | 3.3V_0 | 3.3V_RUN |
| 7 | 3.3V_1 | |
| 8 | 3.3V_2 | |
| 9 | GND4 | |
| 10 | GND5 | |
| 11 | GND6 | |
| 12 | 5V_0 | 5V_HDD |
| 13 | 5V_1 | |
| 14 | 5V_2 | |
| 15 | GND7 | |
| 16 | RSVD | |
| 17 | GND8 | |
| 18 | 12V_0 | |
| 19 | 12V_1 | |
| 20 | 12V_2 | |

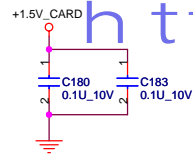
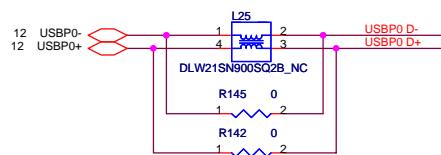


Place caps close to connector.

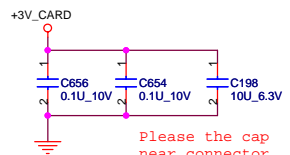




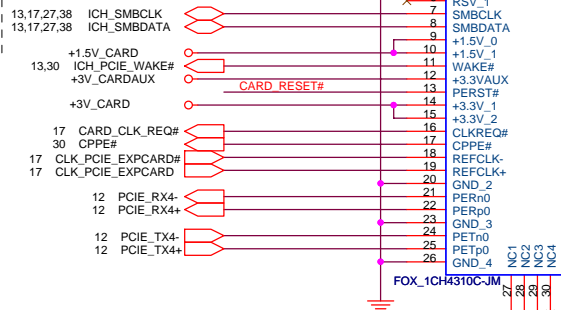
<http://laptopblue.vn>



Please the cap
near connector.

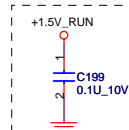
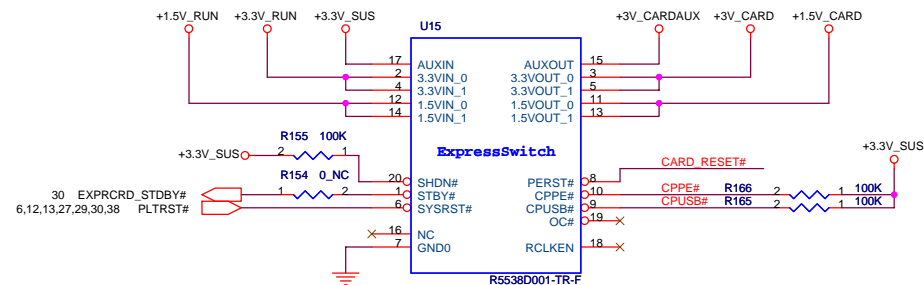


Please the cap
near connector.

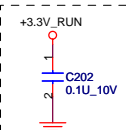


JAE PX10FS16PH-26P

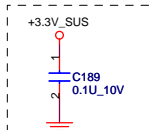
PCI-Express TX and RX direct to connector.



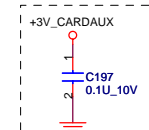
Please the cap
near pin 12 &
14(1.5VIN).



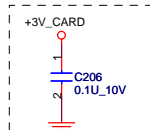
Please the cap near pin 2 & 4 (3.3VIN).



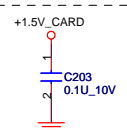
Please the cap
near pin 17
(AUXIN).



```
| Please the cap  
| near pin 15  
| (AUXOUT).
```



Please the cap
near pin 3 & 5
(3.3VOUT).

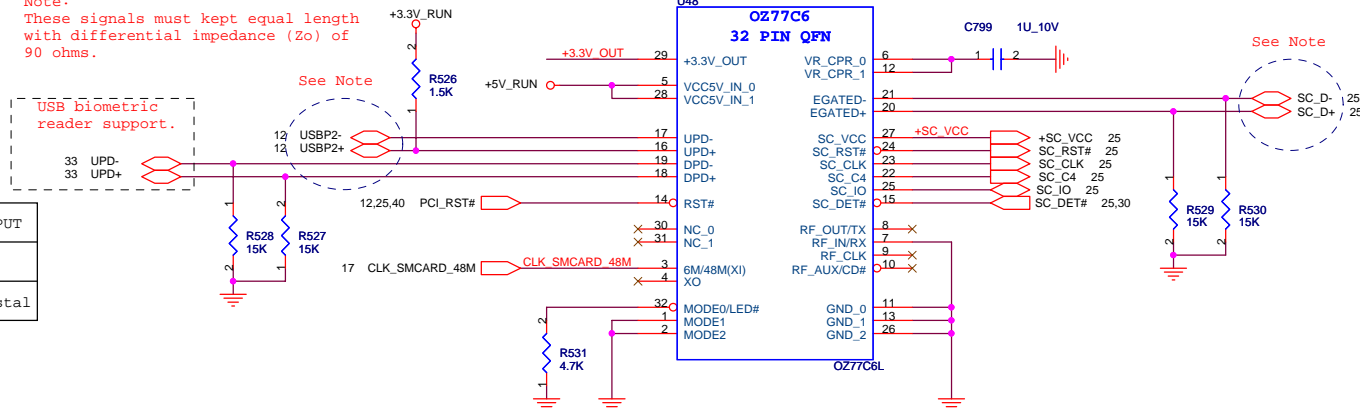


Please the cap
near pin 11 &
13(1.5VOUT).

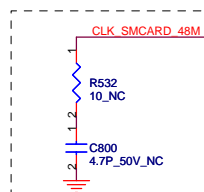
Smart Card

Note:
These signals must kept equal length
with differential impedance (Z_0) of
90 ohms.

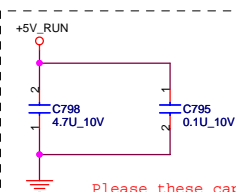
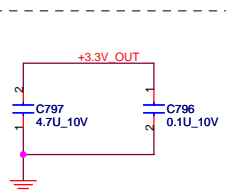
USB biometric
reader support.



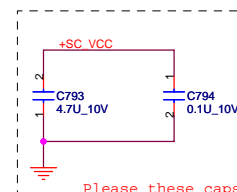
| | |
|-------|--------------|
| MODEL | CLOCK INPUT |
| LOW | 48MHz |
| HIGH | 6MHz Crystal |



Reserved for EMI.
Place the parts
near pin 45.



Please these
near 0Z77C6L.



Please these
near OZ77C6L.



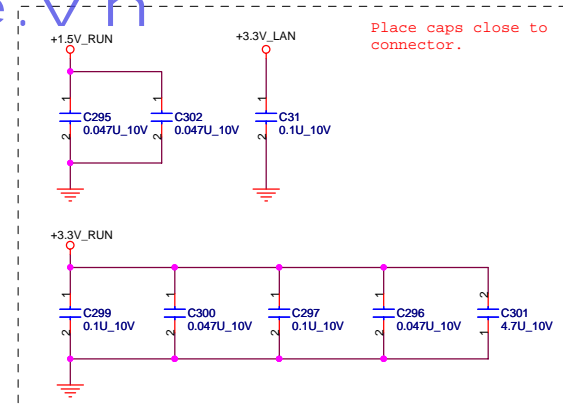
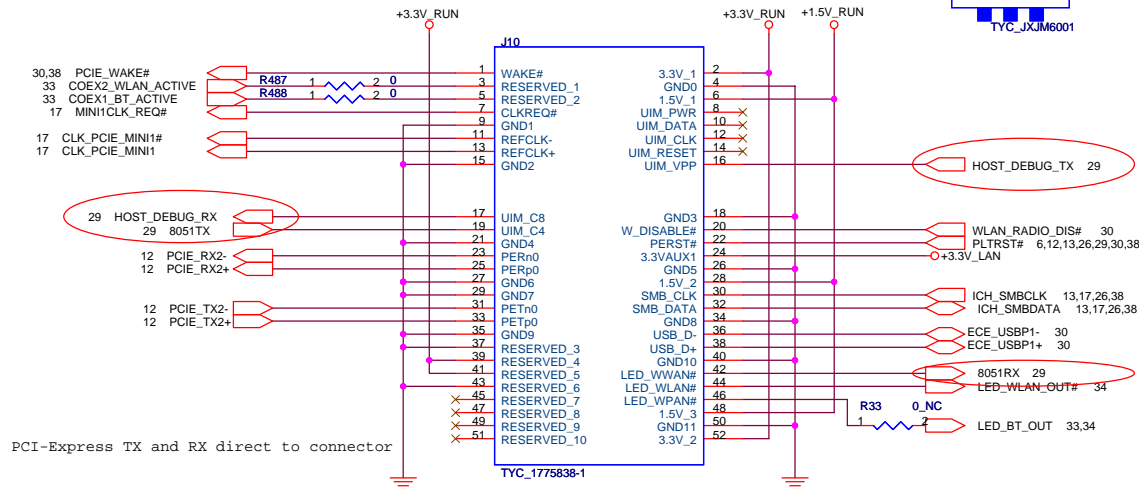
| | |
|-------|-----------------------|
| Title | ExpressCard/SmartCard |
|-------|-----------------------|

| | |
|------|------------------------|
| Size | Document Number JM6 |
|------|------------------------|

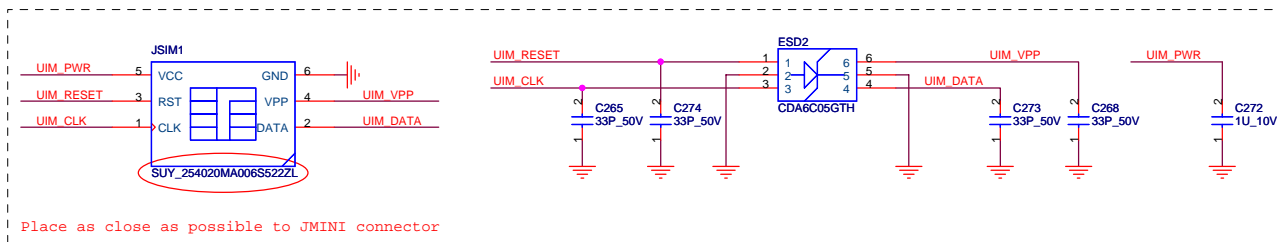
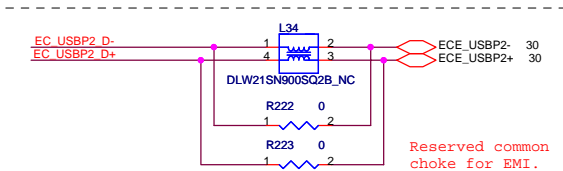
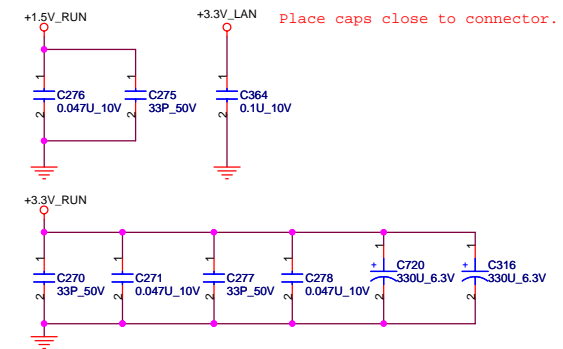
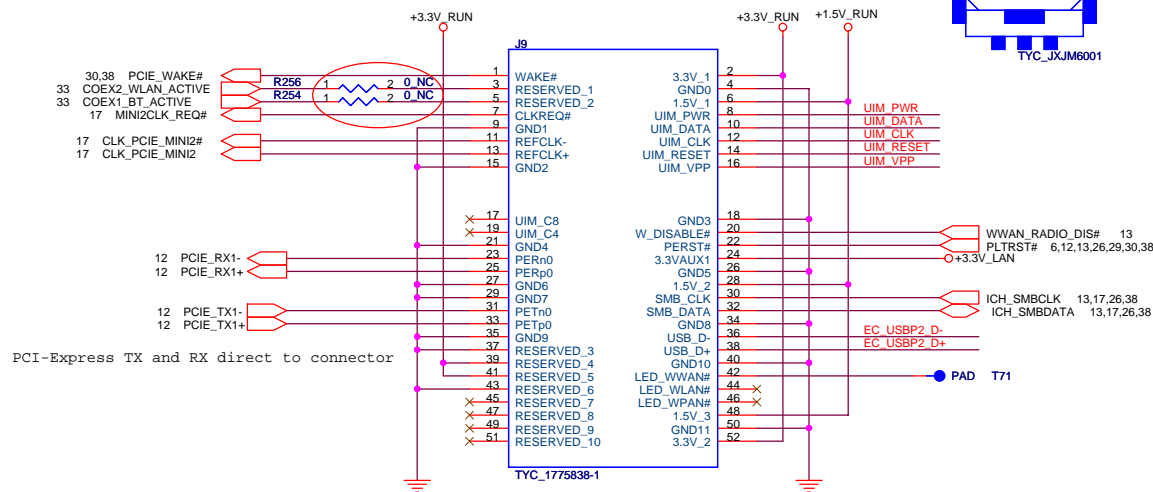
Rev
2A

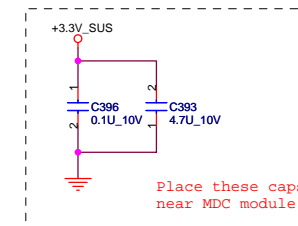
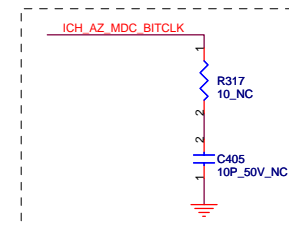
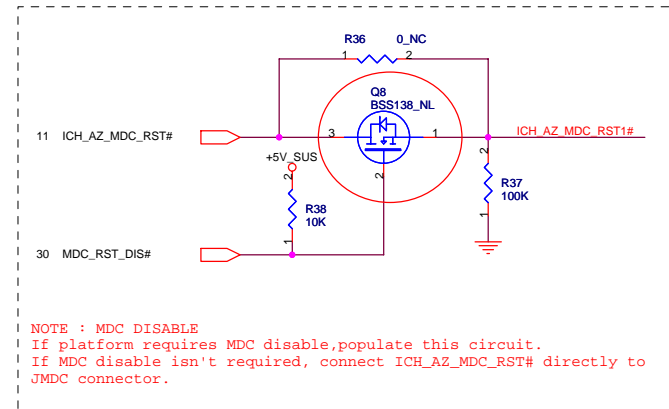
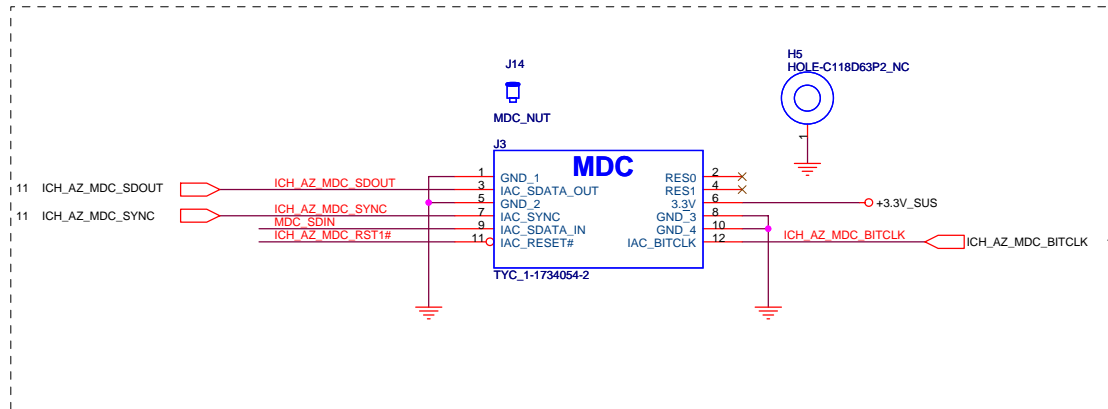
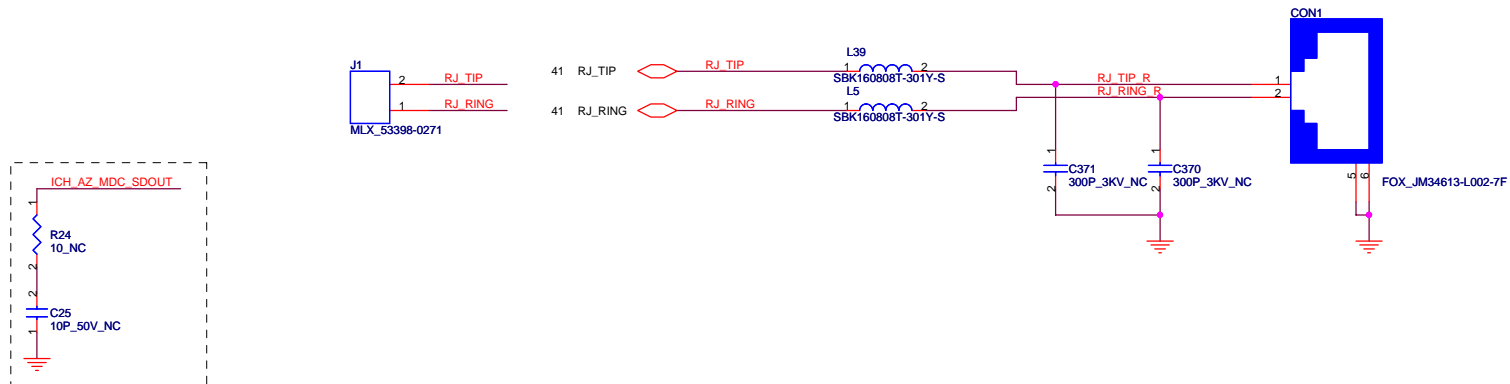
Date: Thursday, September 08, 2005

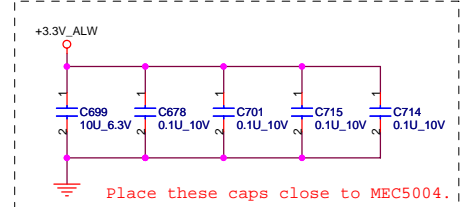
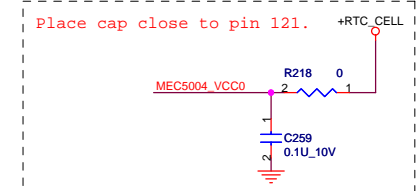
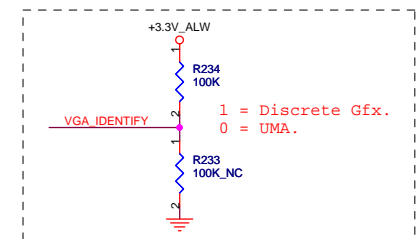
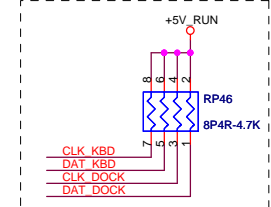
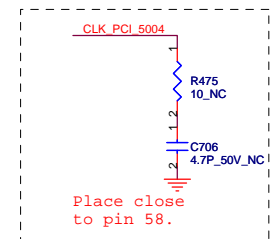
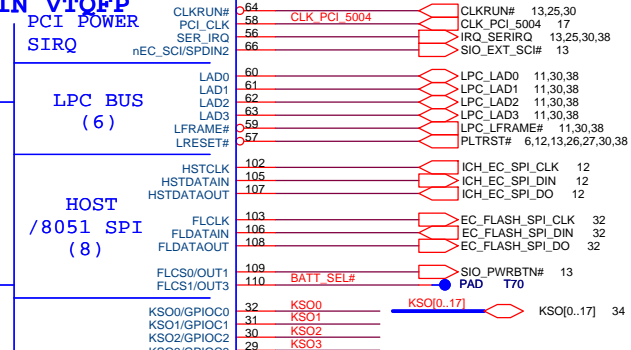
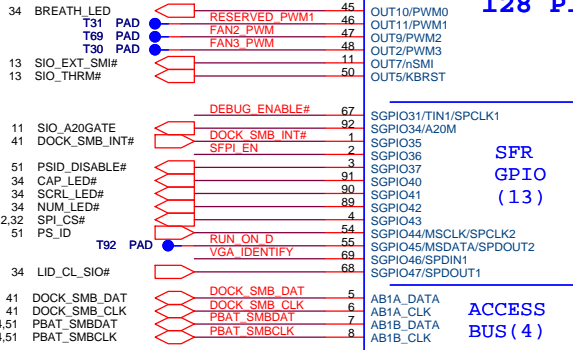
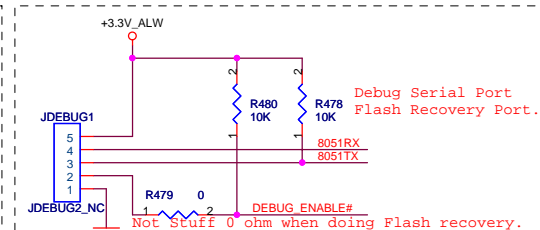
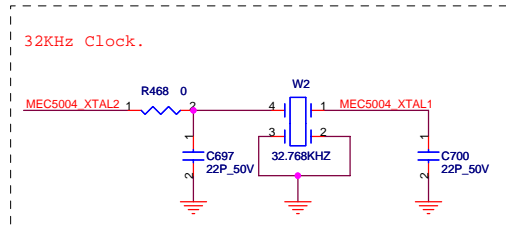
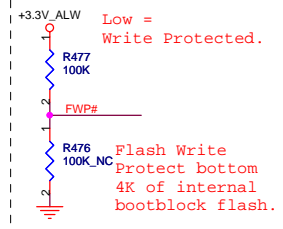
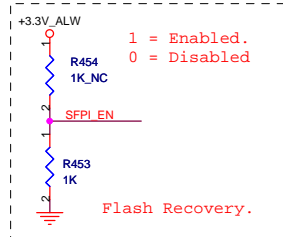
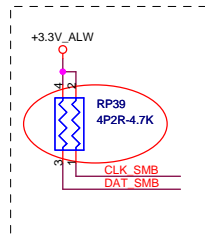
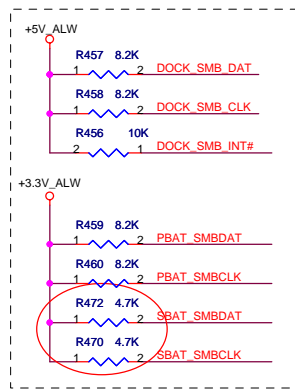
Sheet 26 of 54

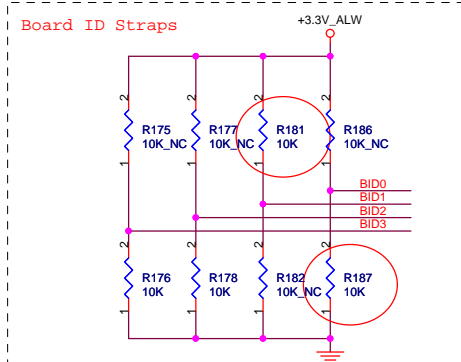
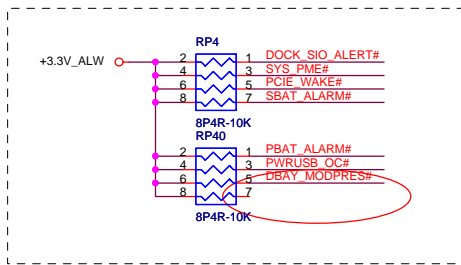


MiniCard WWAN connector

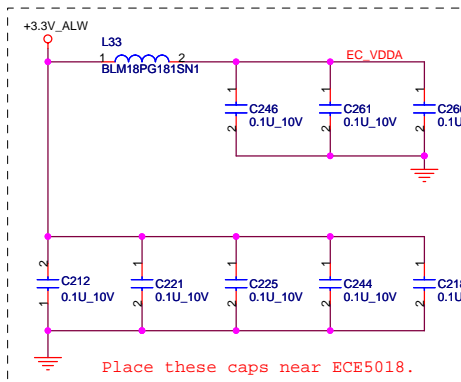
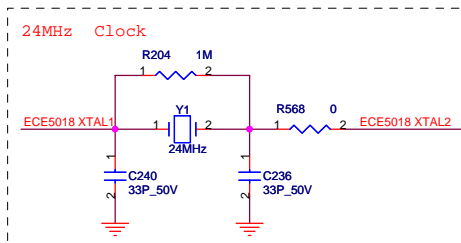








| BID3 | BID2 | BID1 | BID0 | Board Revision |
|------|------|------|------|----------------|
| 0 | 0 | 0 | 0 | ENG1 (M00) |
| 0 | 0 | 0 | 1 | ENG2 (X00) |
| 0 | 0 | 1 | 0 | ENG3 (X01) |
| 0 | 0 | 1 | 1 | ENG4 (X02) |
| 0 | 1 | 0 | 0 | QT (X03) |
| 0 | 1 | 0 | 1 | RAMP (A00) |



27.38 PCIE_WAKE#
25.40 SYS_PME#
41 DOKK_SIO_ALERT#
51 PBAT_ALARM#
43.51 SBAT_ALARM#
43 CHG_PBAT#
43 CHG_SBATT#
43 SBAT_LOW

13.26 ICH_PCIE_WAKE#
12 ICH_PME#
35 THERMTRIP_SIO
26 CPPE#
22 FBACK_EN
3 CPU_PROCHOT#
41 DOKK_PWR_EN
34 SNIFFER_WIRELESS_ON/OFF#
24 MODPRES#
25.26 SC_DET#
27 WLAN_RADIO_DIS#

12 USBP1+
12 USBP1-
27 ECE_USBP1+
27 ECE_USBP1-
27 ECE_USBP2+
27 ECE_USBP2-
33 ECE_USBP3+
33 ECE_USBP3-
24 ECE_USBP4+
24 ECE_USBP4-

38 LOM_TPM_EN#
38 LOM_LOW_PWR
36 AUDIO_AVDD_ON
36 BEEP

PAD T93

EC_VDDA

C262 4.7U_6.3V

C864 4.7U_6.3V

VDDA33PLL

VDDA33_0

VDDA33_1

VDDA33_2

VSS_0

VSS_1

VSS_2

VSS_3

VSS_4

VSS_5

VSS_6

VSS_7

VSS_8

VSS_9

VCC1_0

VCC1_1

VCC1_2

VCC1_3

VCC1_4

VDD18

CAP_LDO

VDDA18PLL

C226 4.7U_6.3V

C229 0.1U_10V

C213 4.7U_6.3V

C243 4.7U_6.3V

C226 4.7U_6.3V

C229 0.1U_10V

C213 4.7U_6.3V

C243 4.7U_6.3V

C226 4.7U_6.3V

C229 0.1U_10V

C213 4.7U_6.3V

C243 4.7U_6.3V

PCIE_WAKE#
SYS_PME#
DOKK_SIO_ALERT#
BID0
BID1
BID2
BID3

CBUS_GRST#
CB_HWPSPND#

OUT65

R220 2 12K/F
R219 2 10K

ECE5018 XTAL2
ECE5018 XTAL1

USBP0
USBP1
USBP2
USBP3
USBP4

LOM_TPM_EN#
LOM_LOW_PWR
AUDIO_AVDD_ON
BEEP

PAD T93

EC_VDDA

C262 4.7U_6.3V

C864 4.7U_6.3V

VDDA33PLL

VDDA33_0

VDDA33_1

VDDA33_2

VSS_0

VSS_1

VSS_2

VSS_3

VSS_4

VSS_5

VSS_6

VSS_7

VSS_8

VSS_9

VCC1_0

VCC1_1

VCC1_2

VCC1_3

VCC1_4

VDD18

CAP_LDO

VDDA18PLL

C226 4.7U_6.3V

C229 0.1U_10V

C213 4.7U_6.3V

C243 4.7U_6.3V

C226 4.7U_6.3V

C229 0.1U_10V

C213 4.7U_6.3V

C243 4.7U_6.3V

C226 4.7U_6.3V

C229 0.1U_10V

C213 4.7U_6.3V

C243 4.7U_6.3V

USIO1

ECE5018 Midway 128 PIN VTQFP

PCI POWER

SIRQ (3)

LPC BUS

(8)

DOCKING LPC

(8)

BC

PARALLEL

PORT (17)

UART

(8)

IRCC

(8)

SIO

RESET

(4)

MISCELLANEOUS

(4)

GPIOA[0]
GPIOA[1]
GPIOA[2]
GPIOA[3]
GPIOA[4]
GPIOA[5]
GPIOA[6]
GPIOA[7]
GPIOF[4]
GPIOF[5]
GPIOF[6]
GPIOF[7]
GPIOG[0]
GPIOG[1]
GPIOG[2]
GPIOG[3]
GPIOG[4]
GPIOG[5]
GPIOG[6]
GPIOG[7]
GPIOH[4]
GPIOH[5]
GPIOH[6]
GPIOH[7]
OUT65
RBIAS
ATEST
XTAL2
XTAL1/CLKIN
USBP0
USBP1
USBP2
USBP3
USBP4
GPIOI[0]
GPIOI[1]
GPIOI[2]
GPIOI[3]
GPIOI[4]
GPIOI[5]
GPIOI[6]
GPIOI[7]
GPIOJ[0]
GPIOJ[1]
GPIOJ[2]
GPIOJ[3]
GPIOJ[4]
GPIOJ[5]
GPIOJ[6]
GPIOJ[7]
GPIOK[0]
GPIOK[1]
GPIOK[2]
GPIOK[3]
GPIOK[4]
GPIOK[5]
GPIOK[6]
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GPIOX[7]
GPIOY[0]
GPIOY[1]
GPIOY[2]
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GPIOY[5]
GPIOY[6]
GPIOY[7]
GPIOZ[0]
GPIOZ[1]
GPIOZ[2]
GPIOZ[3]
GPIOZ[4]
GPIOZ[5]
GPIOZ[6]
GPIOZ[7]

USB (19)

POWER PLANES (21)

CLKRUN# 13.25,29
CLK_PCI_5018 17
IRQ_SERIRQ 13.25,29,38

LPC_LAD0 11.29,38
LPC_LAD1 11.29,38
LPC_LAD2 11.29,38
LPC_LAD3 11.29,38
LPC_LFRAME# 11.29,38
PLTRST# 6.12,13,26,27,29,38
LPC_LDRQ0# 11
LPC_LDRQ1# 11

D_LAD0 41
D_LAD1 41
D_LAD2 41
D_LAD3 41
D_LFRAME# 41
D_CLKRUN# 41
D_DLRQ1# 41
D_SERIRQ 41

BC_CLK 29
BC_DAT 29
BC_INT# 29

PWRUSB_OC# 31
PWRUSB_EN 31
HP_NB_SENSE 36,37
DOCK_HP_MUTE# 36
5V_CAL_SIO2# 35

5V_CAL_SIO# 35
IMVP6_PROCHOT# 47

SPDIF_SHDN 36
LOM_CABLE_DETECT 38
MDC_RST_DIS# 28
ADAPT_OC 44
EXPRCRD_STDBY# 26

AC OFF

RX0# 31
TX0# 31
RTS0# 31
DSR0# 31
CTS0# 31
DTR0# 31
RI0# 31
DCD0# 31

IRTX 33
IRRX 33
SBAT_ALARM# 51
PBAT_ALARM# 51
DBAY_MODPRES# 31
USB_BACK_EN# 31
USB_SIDE_EN# 31
IRMODE 33

DOCKED 39,41
QBUEEN# 40
T28 PAD
T98 PAD

CLK_SIO_14M 17

TEST_PIN PWRGD

CLK_PCI_5018

CLKRUN# 13.25,29
CLK_PCI_5018 17
IRQ_SERIRQ 13.25,29,38

LPC_LAD0 11.29,38
LPC_LAD1 11.29,38
LPC_LAD2 11.29,38
LPC_LAD3 11.29,38
LPC_LFRAME# 11.29,38
PLTRST# 6.12,13,26,27,29,38
LPC_LDRQ0# 11
LPC_LDRQ1# 11

D_LAD0 41
D_LAD1 41
D_LAD2 41
D_LAD3 41
D_LFRAME# 41
D_CLKRUN# 41
D_DLRQ1# 41
D_SERIRQ 41

BC_CLK 29
BC_DAT 29
BC_INT# 29

PWRUSB_OC# 31
PWRUSB_EN 31
HP_NB_SENSE 36,37
DOCK_HP_MUTE# 36
5V_CAL_SIO2# 35

5V_CAL_SIO# 35
IMVP6_PROCHOT# 47

SPDIF_SHDN 36
LOM_CABLE_DETECT 38
MDC_RST_DIS# 28
ADAPT_OC 44
EXPRCRD_STDBY# 26

AC OFF

RX0# 31
TX0# 31
RTS0# 31
DSR0# 31
CTS0# 31
DTR0# 31
RI0# 31
DCD0# 31

IRTX 33
IRRX 33
SBAT_ALARM# 51
PBAT_ALARM# 51
DBAY_MODPRES# 31
USB_BACK_EN# 31
USB_SIDE_EN# 31
IRMODE 33

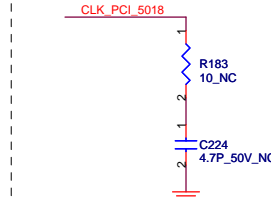
DOCKED 39,41
QBUEEN# 40
T28 PAD
T98 PAD

CLK_SIO_14M 17

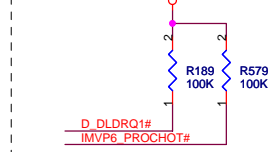
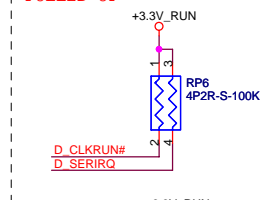
TEST_PIN PWRGD

CLK_PCI_5018

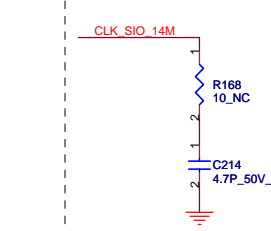
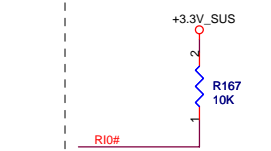
Place closely pin USIO2.

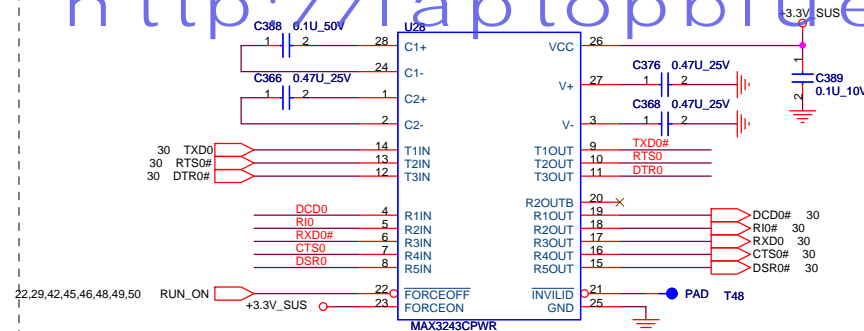
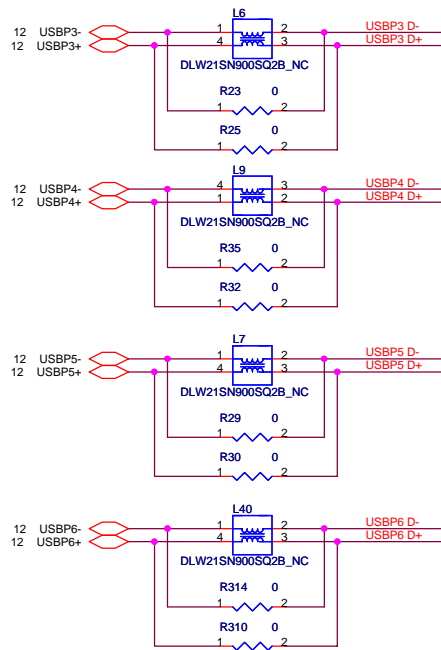


DOCKING PULLED UP

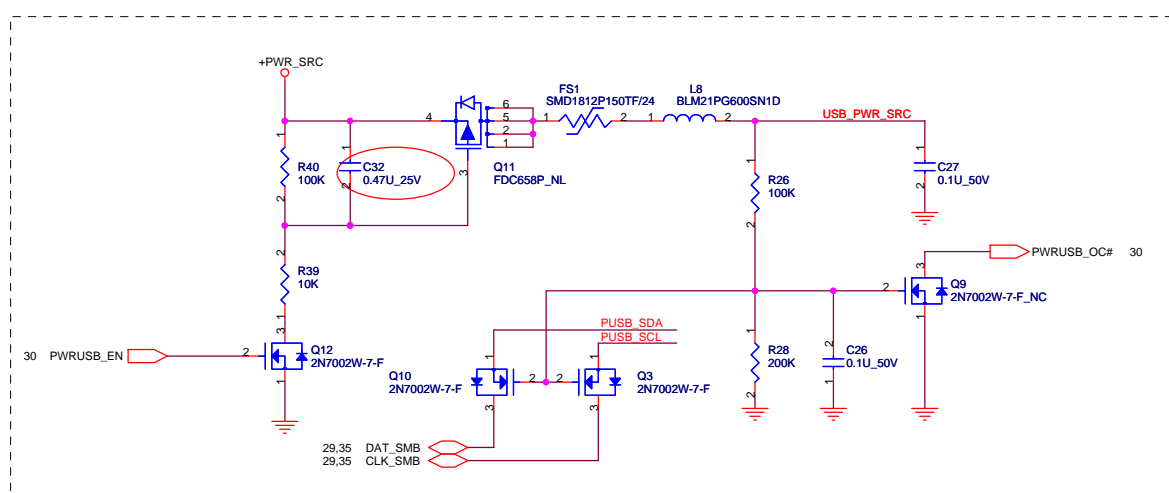
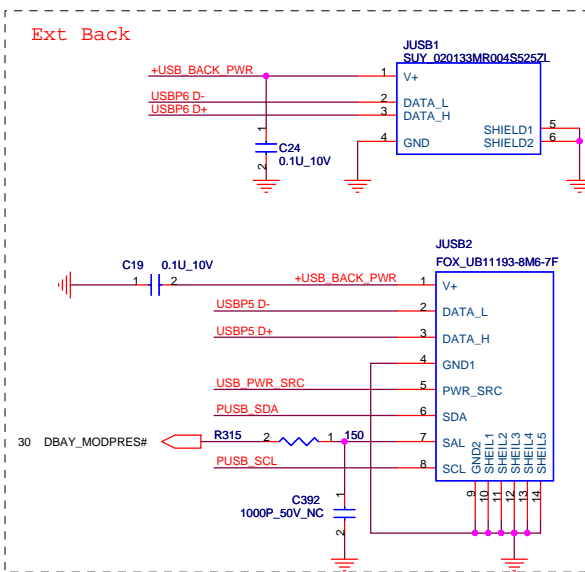
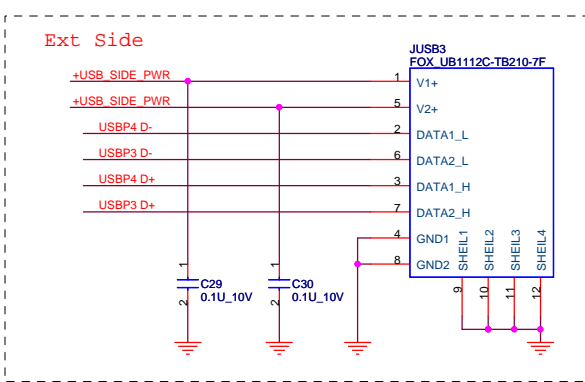
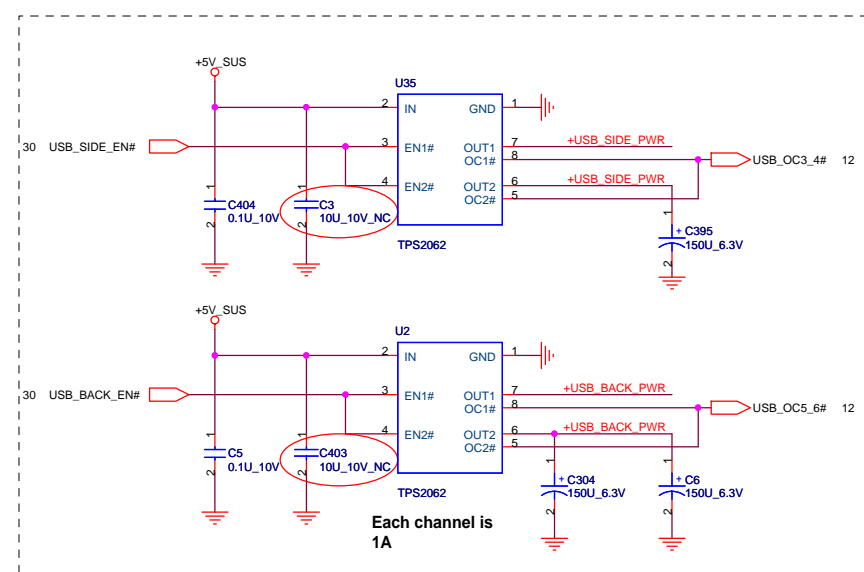


To MDC disable ckt.
Reserved.
To Express Card Pwr Switch.

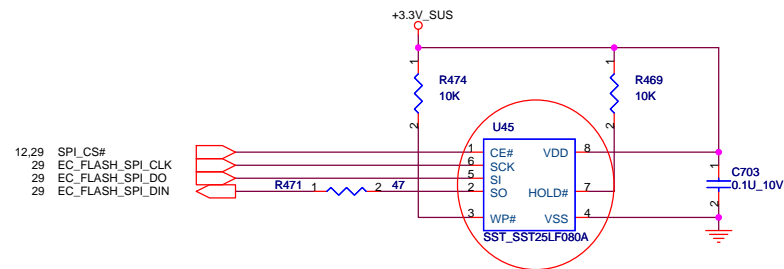




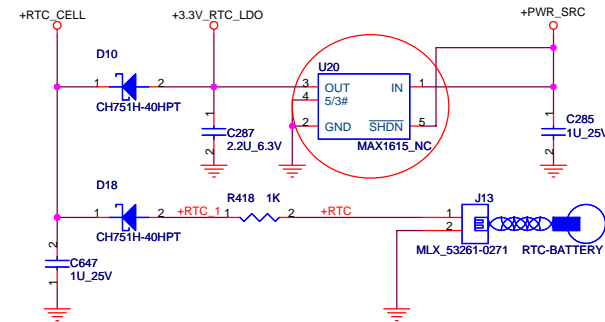
Place these beads close to JCOM1 as soon as possible
If MAX3243 pin 22 tied to RUN_ON, then it can not support Ring Out



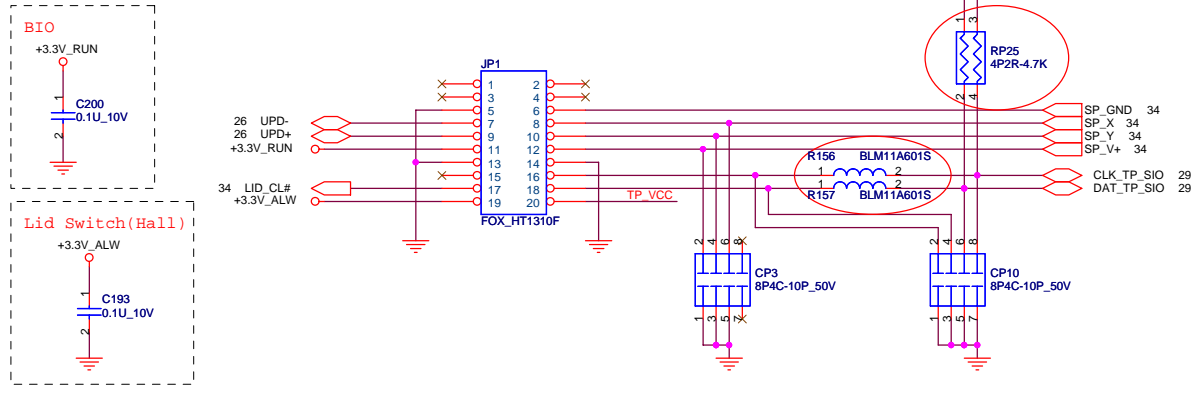
8Mbit (1M Byte), SPI



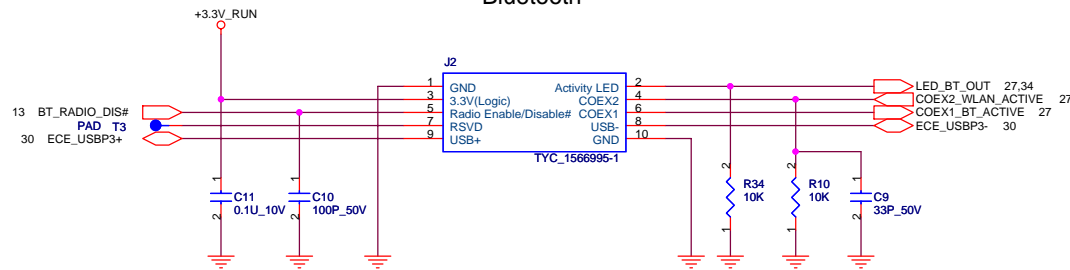
RTC BATTERY



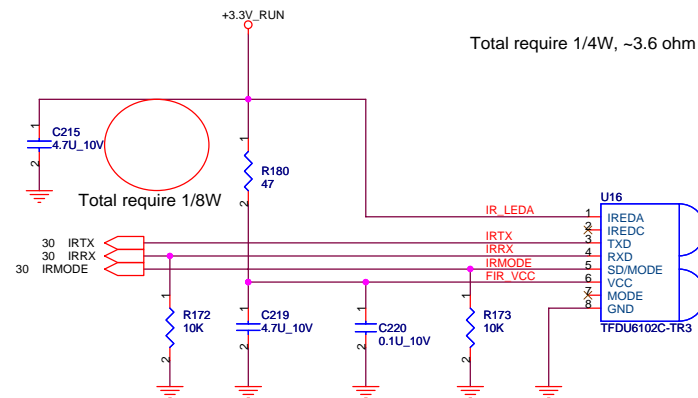
Touch Pad



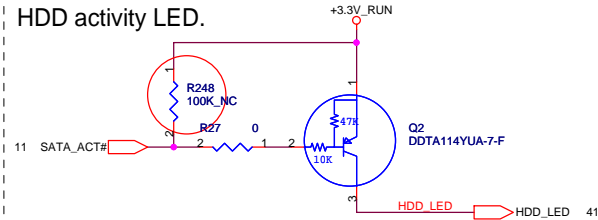
Bluetooth



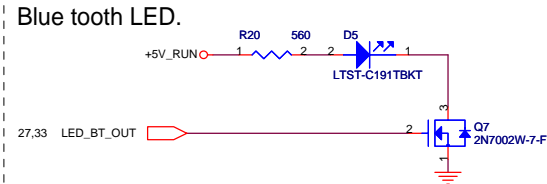
FIR



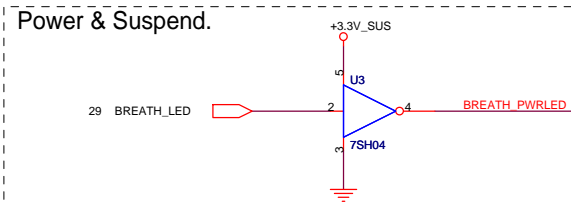
HDD activity LED.



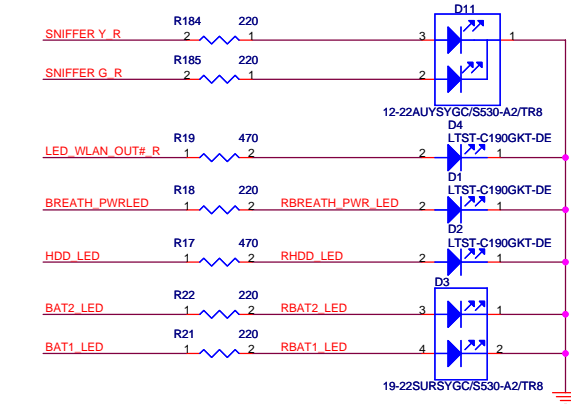
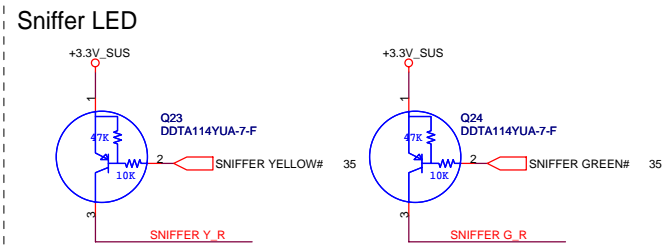
Blue tooth LED.



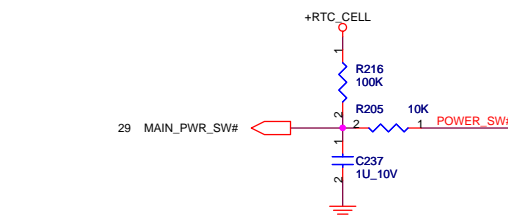
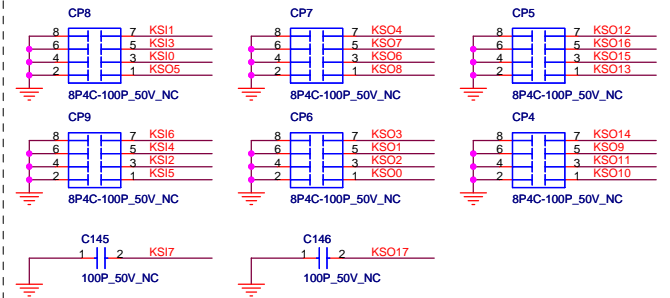
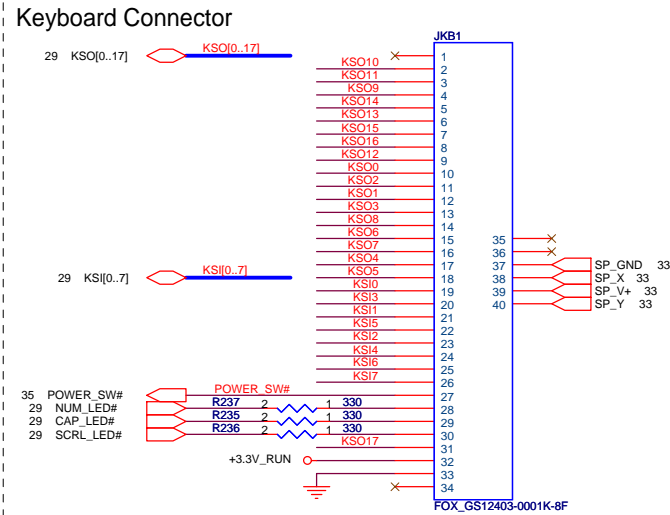
Power & Suspend.



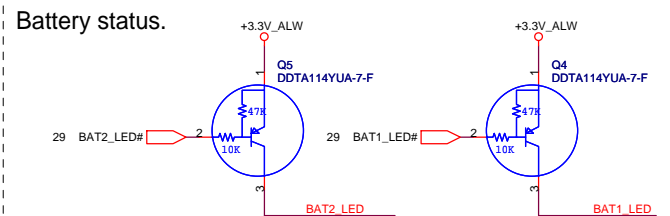
Sniffer LED



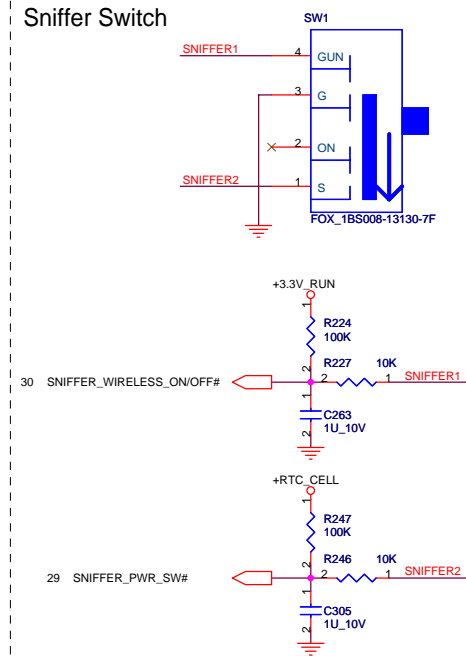
Keyboard Connector



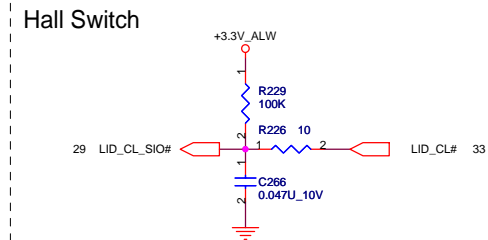
Battery status.



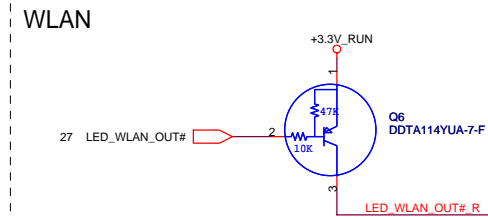
Sniffer Switch

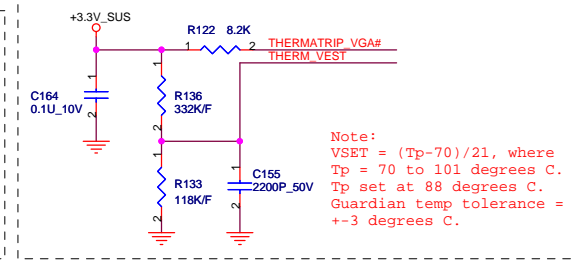
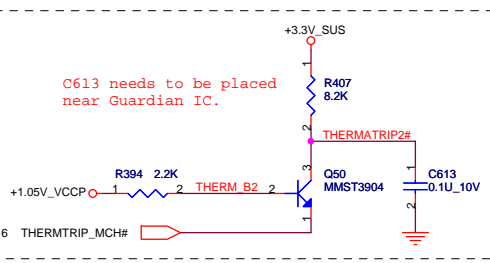
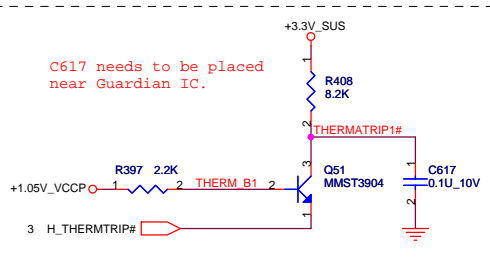
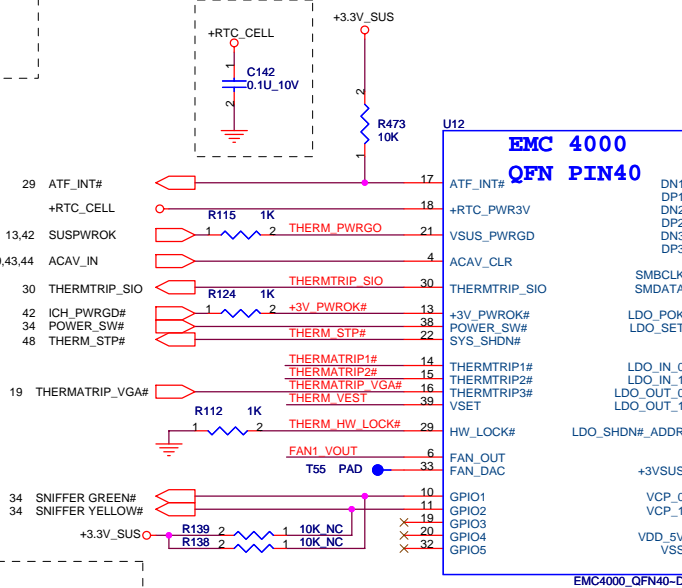
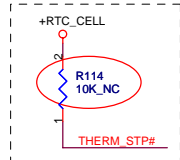
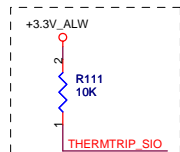
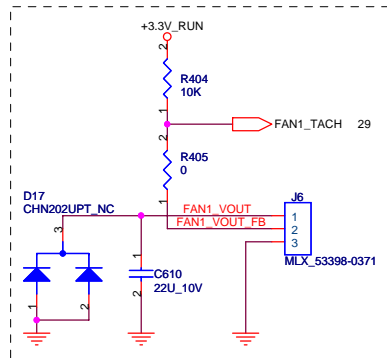


Hall Switch

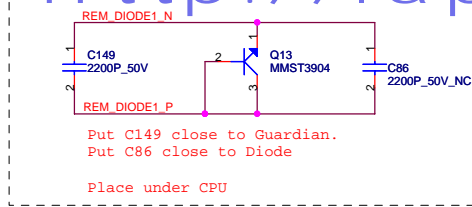


WLAN

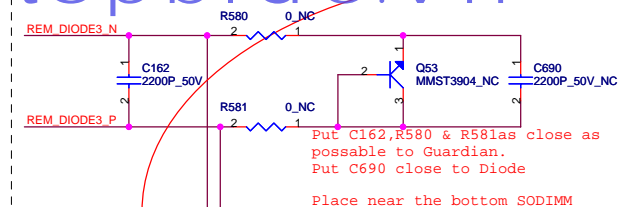




Note:
VSET = (Tp-70)/21, where
Tp = 70 to 101 degrees C.
Tp set at 88 degrees C.
Guardian temp tolerance =
+/-3 degrees C.



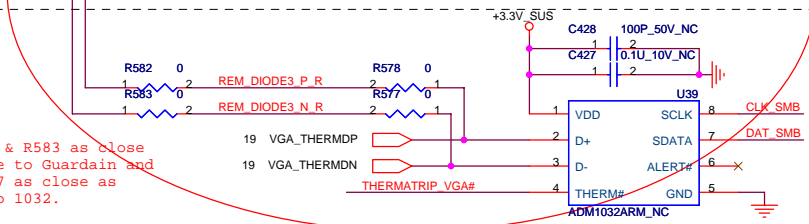
Put C149 close to Guardian.
Put C86 close to Diode
Place under CPU



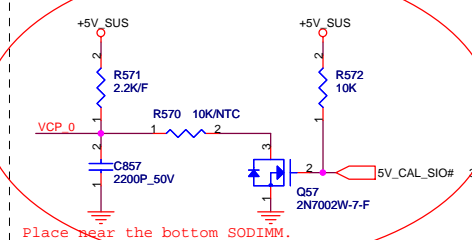
Put C162, R580 & R581as close as possible to Guardian.
Put C690 close to Diode
Place near the bottom SODIMM

Discrete

Place R582 & R583 as close as possible to Guardian and R578 & R577 as close as possible to 1032.

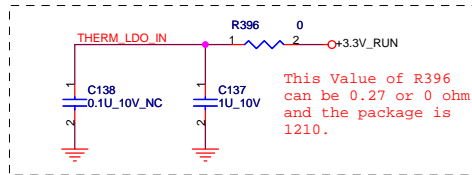
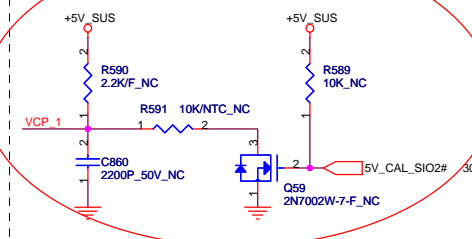


Can place and stuff this thermistor circuit for additional sensor in Discrete Down Designs.



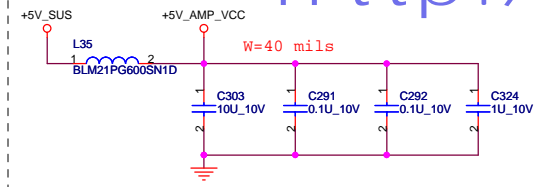
Place near the bottom SODIMM.

May need to place and stuff this thermistor circuit for additional sensor in Discrete Down Designs.

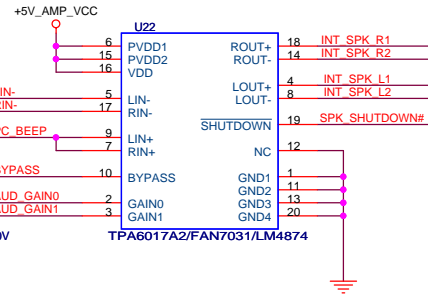


0603 package.
Voltage margining circuit for LDO output. For Vmargin stuff R31 and R27=30K. R27=1K for production.

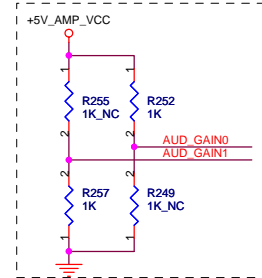
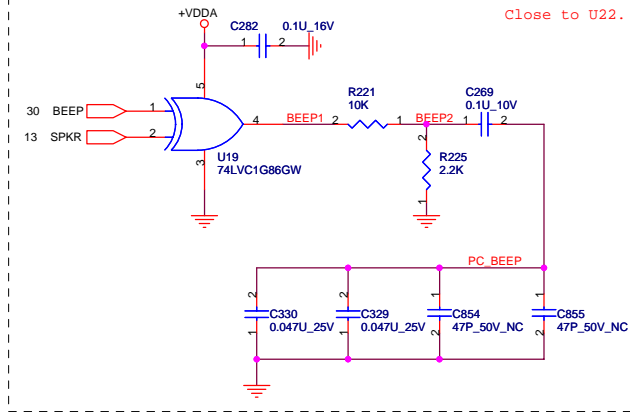
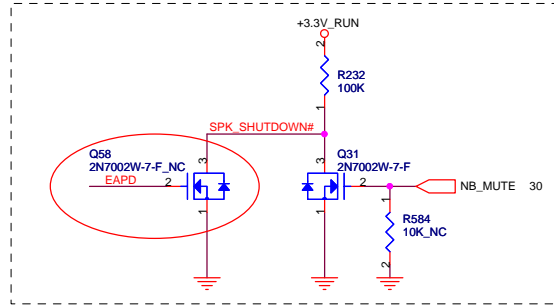
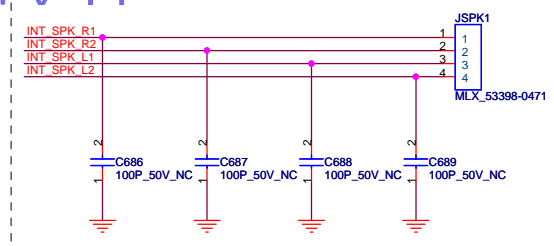
INTERNAL SPEAKER AMP



NOTE: Speaker trace width should be minimum 10 Mils.

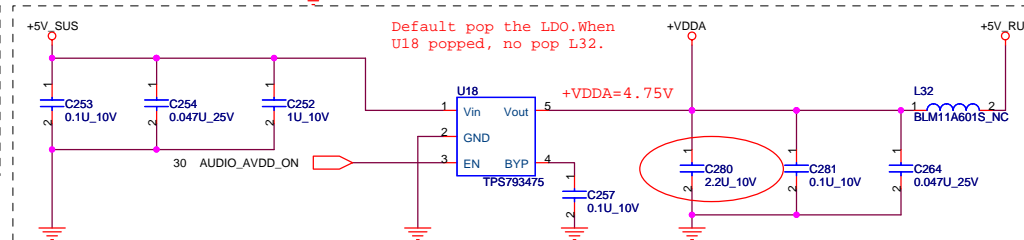
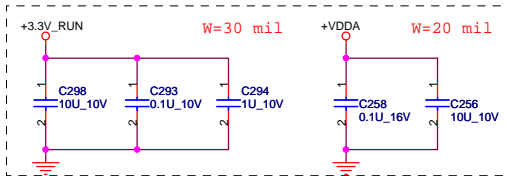
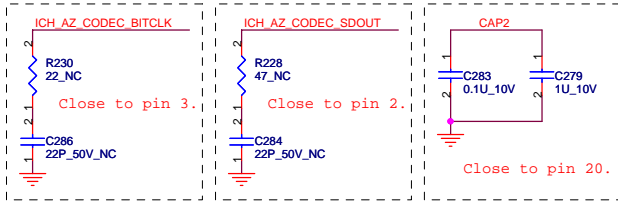
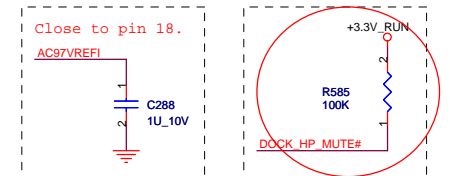
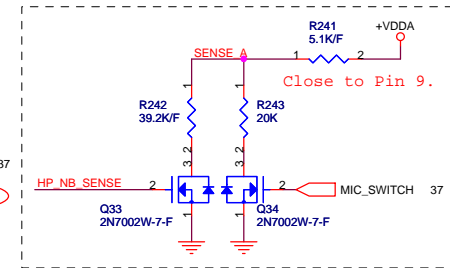
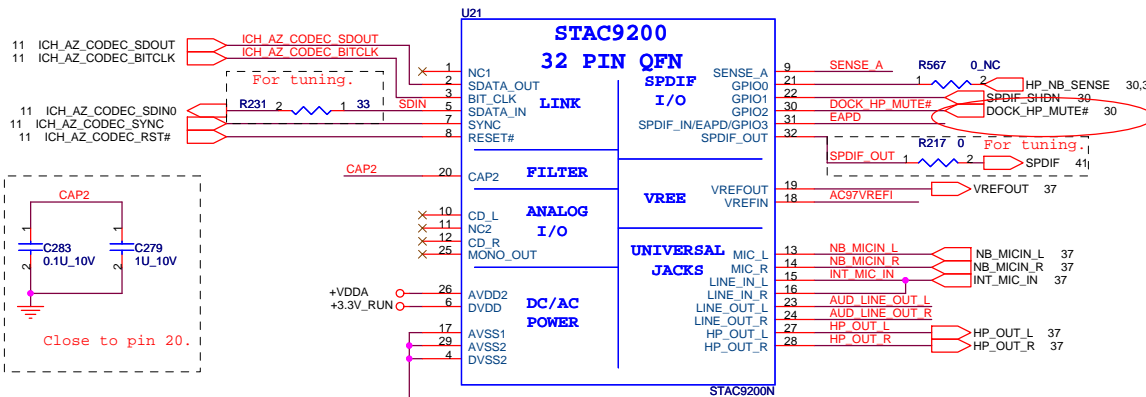


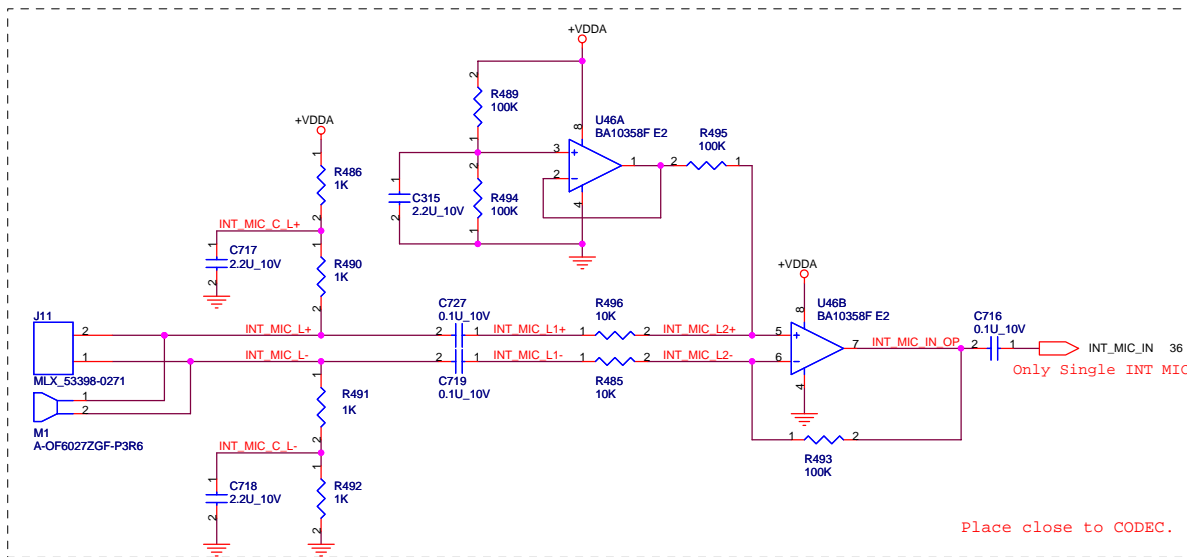
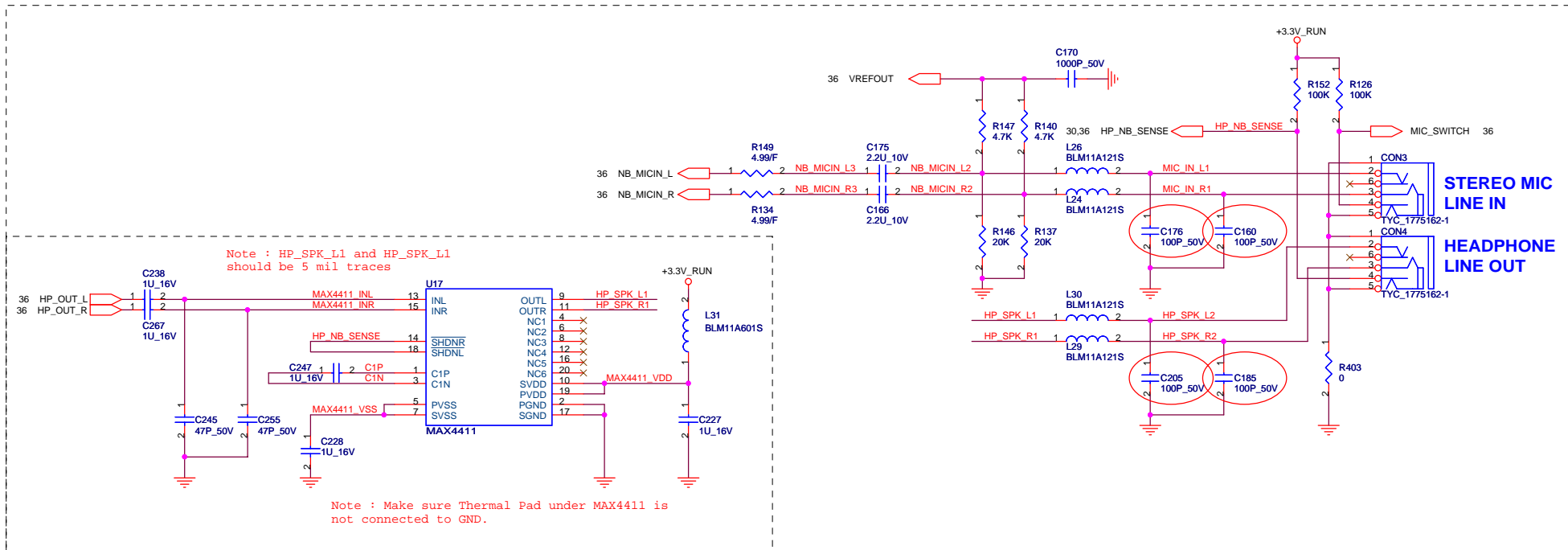
| GAIN0 | GAIN1 | AV | RIN |
|-------|-------|--------|-----|
| 0 | 0 | 6dB | 90K |
| 0 | 1 | 10dB | 70K |
| 1 | 0 | 15.6dB | 45K |
| 1 | 1 | 21.6dB | 25K |



AZALIA (HD) CODEC

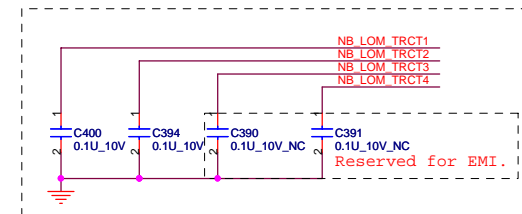
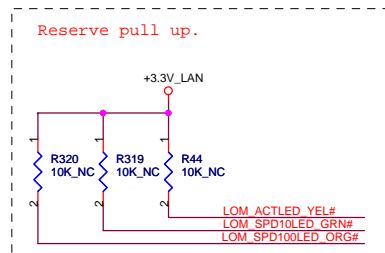
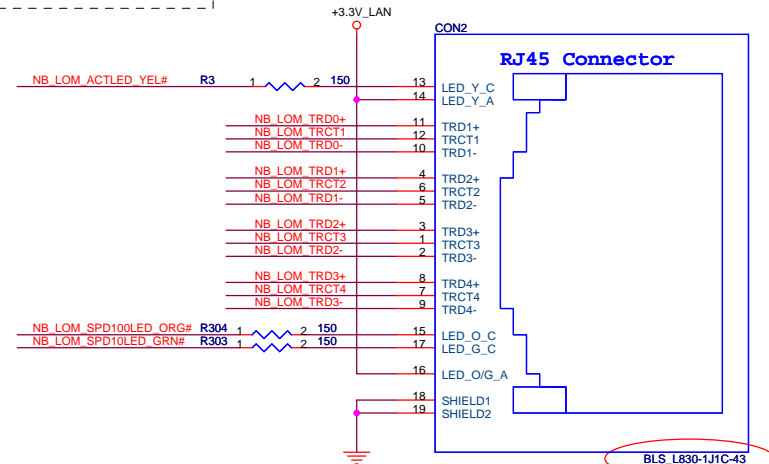
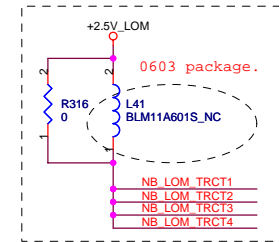
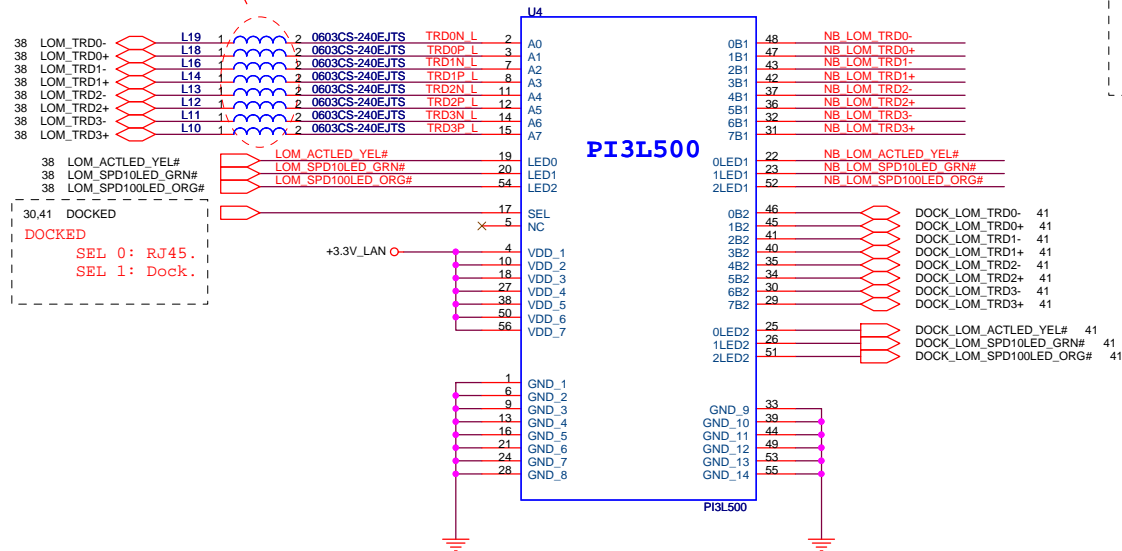
All CODEC analog audio inputs and outputs should be 5 Mil traces.

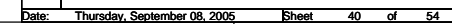


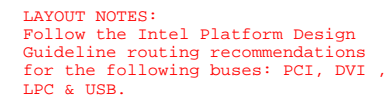


TRANSFORM+RJ45

24nH is a suggested value.
Actual value will be systgem dependent.
Must use 0603 package for lower DC resistance.

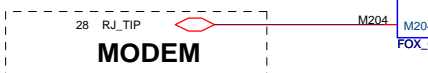
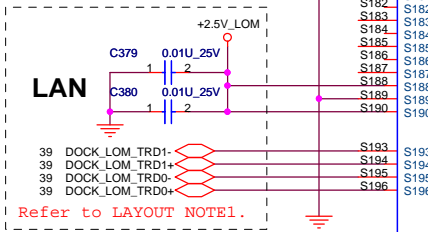
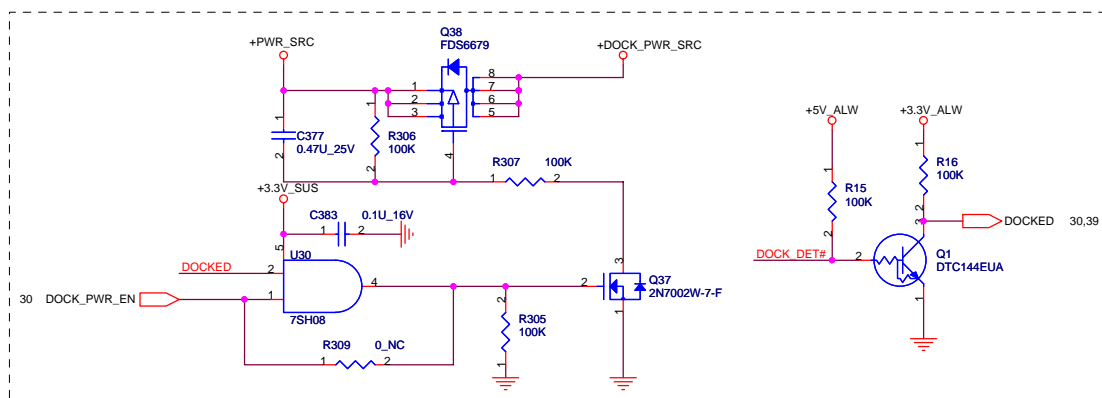
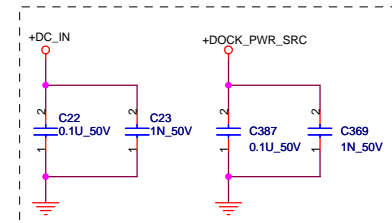
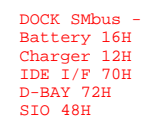






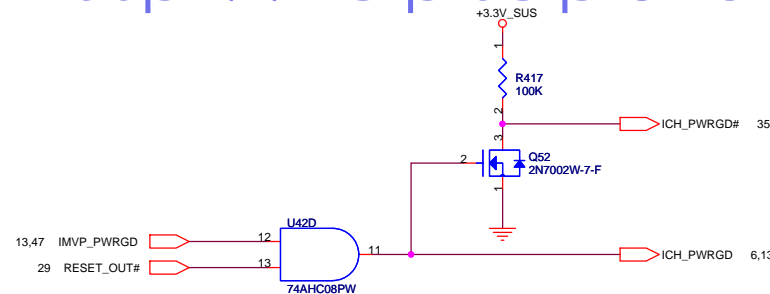
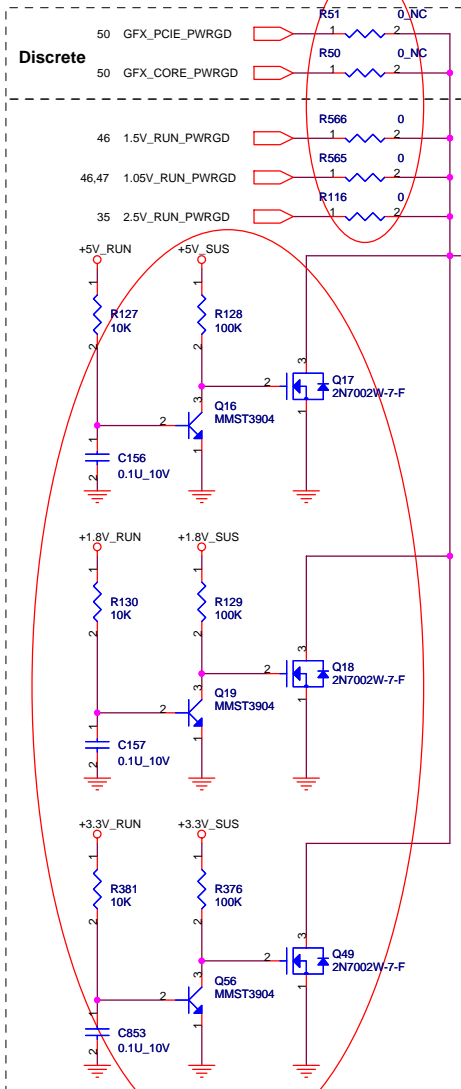
LAYOUT NOTES:

- Terminators should be as close as possible to dock connector pins.
- Keep traces as short as possible.

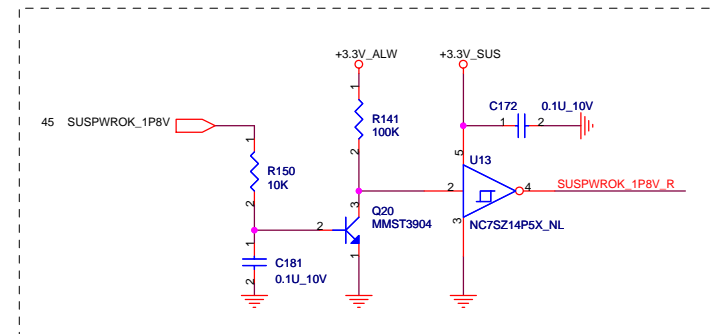
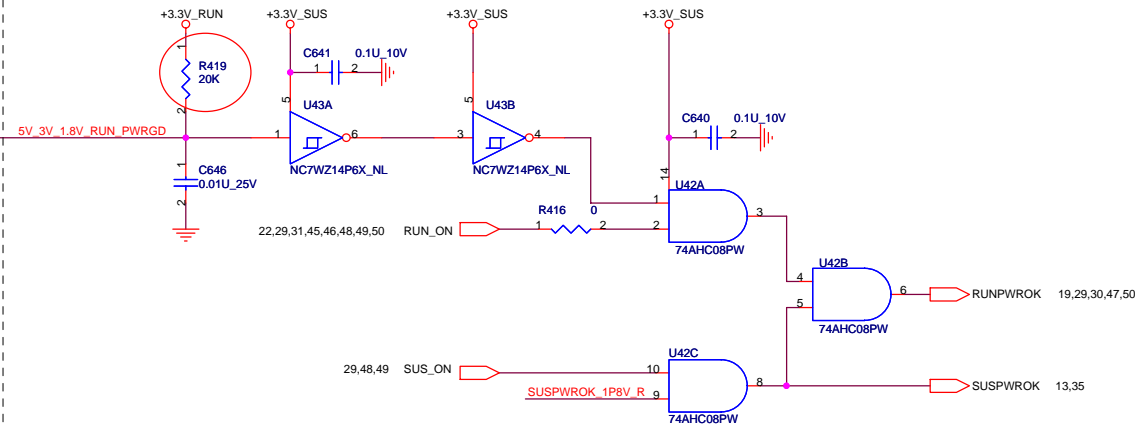


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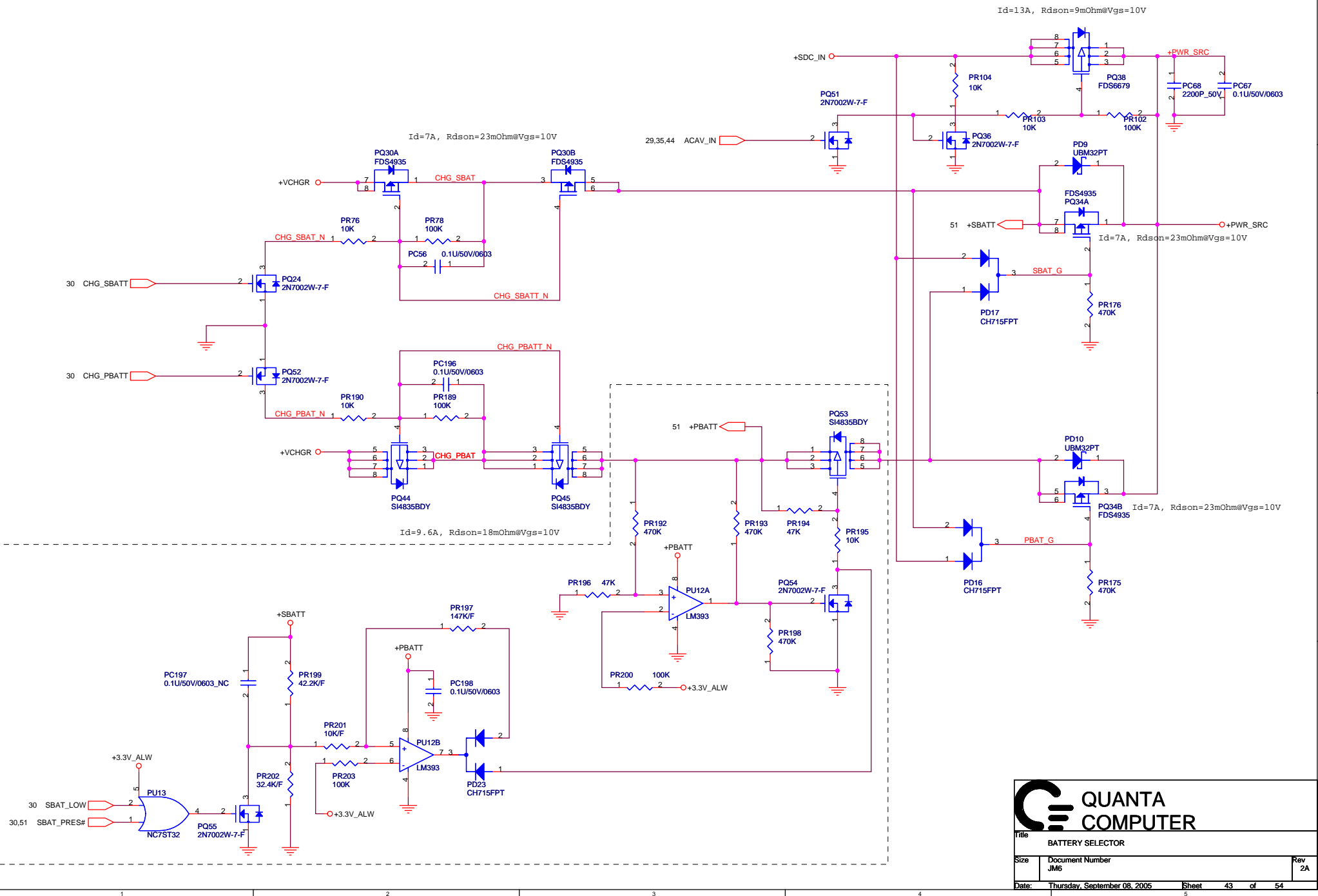
Discrete




Keep Away from high speed buses



| | | |
|------------------------------------|-----------------|--------|
| QUANTA COMPUTER | | |
| Title POWER GOOD | | |
| Size JM6 | Document Number | Rev 2A |
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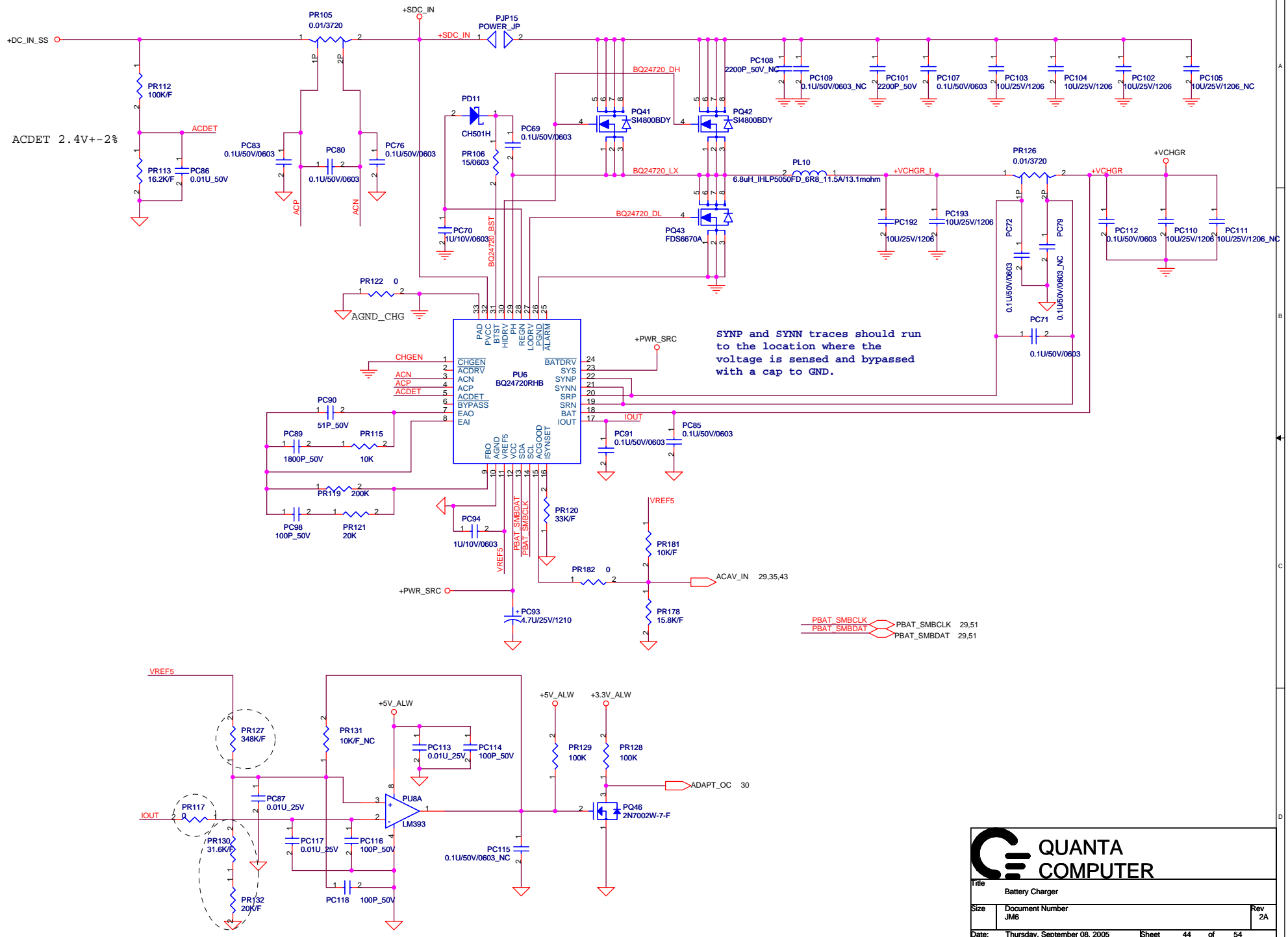


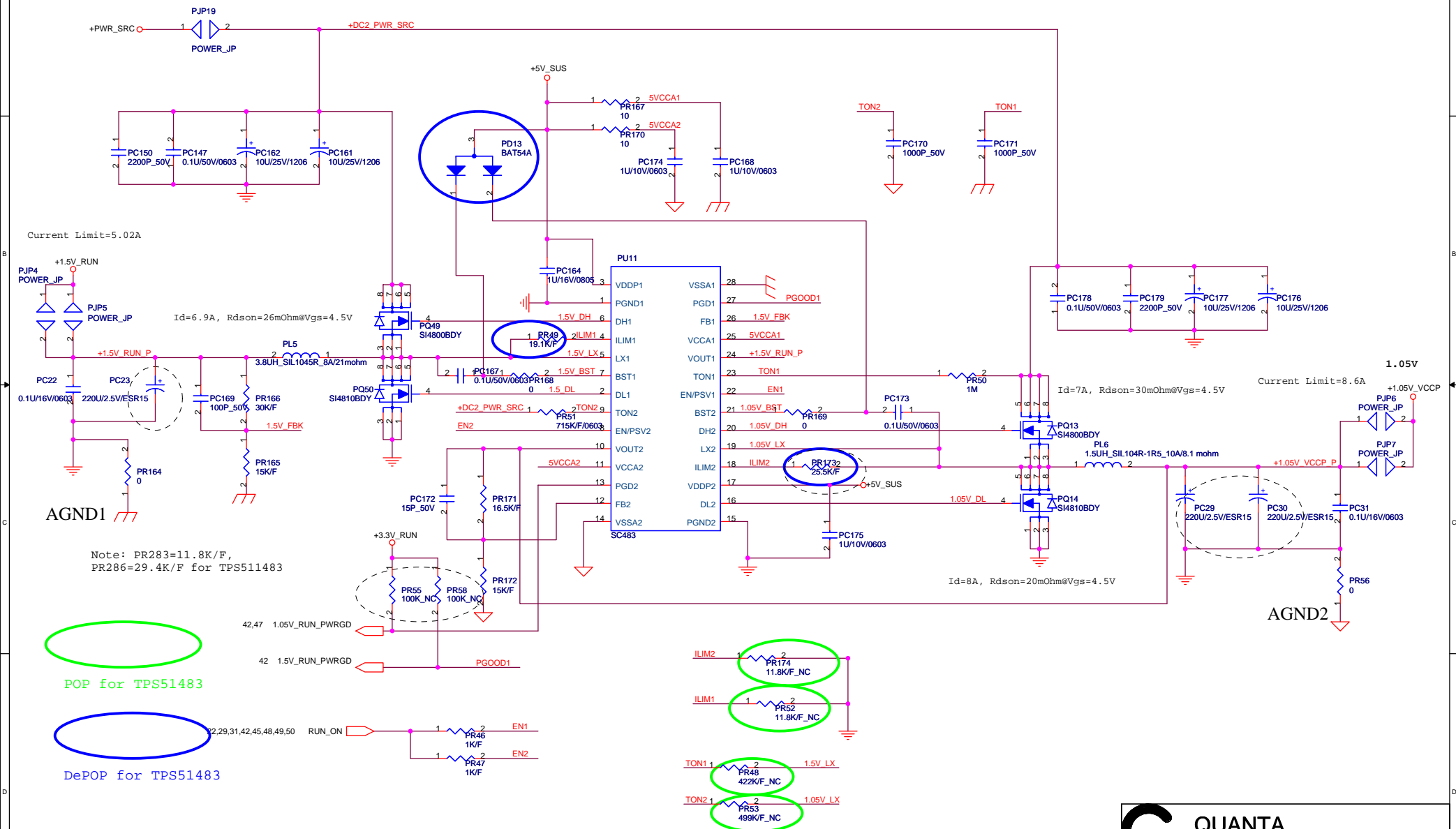


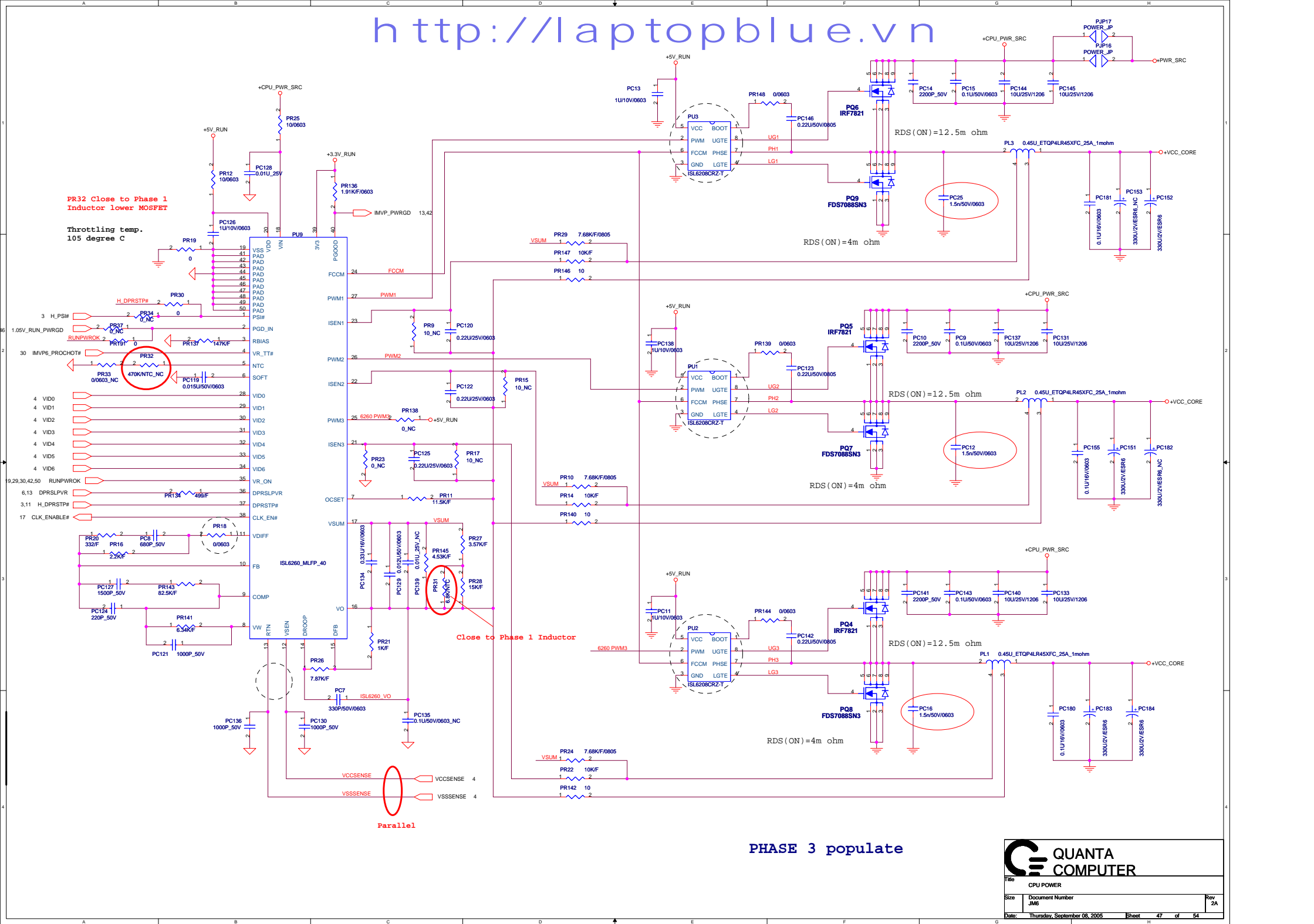
QUANTA

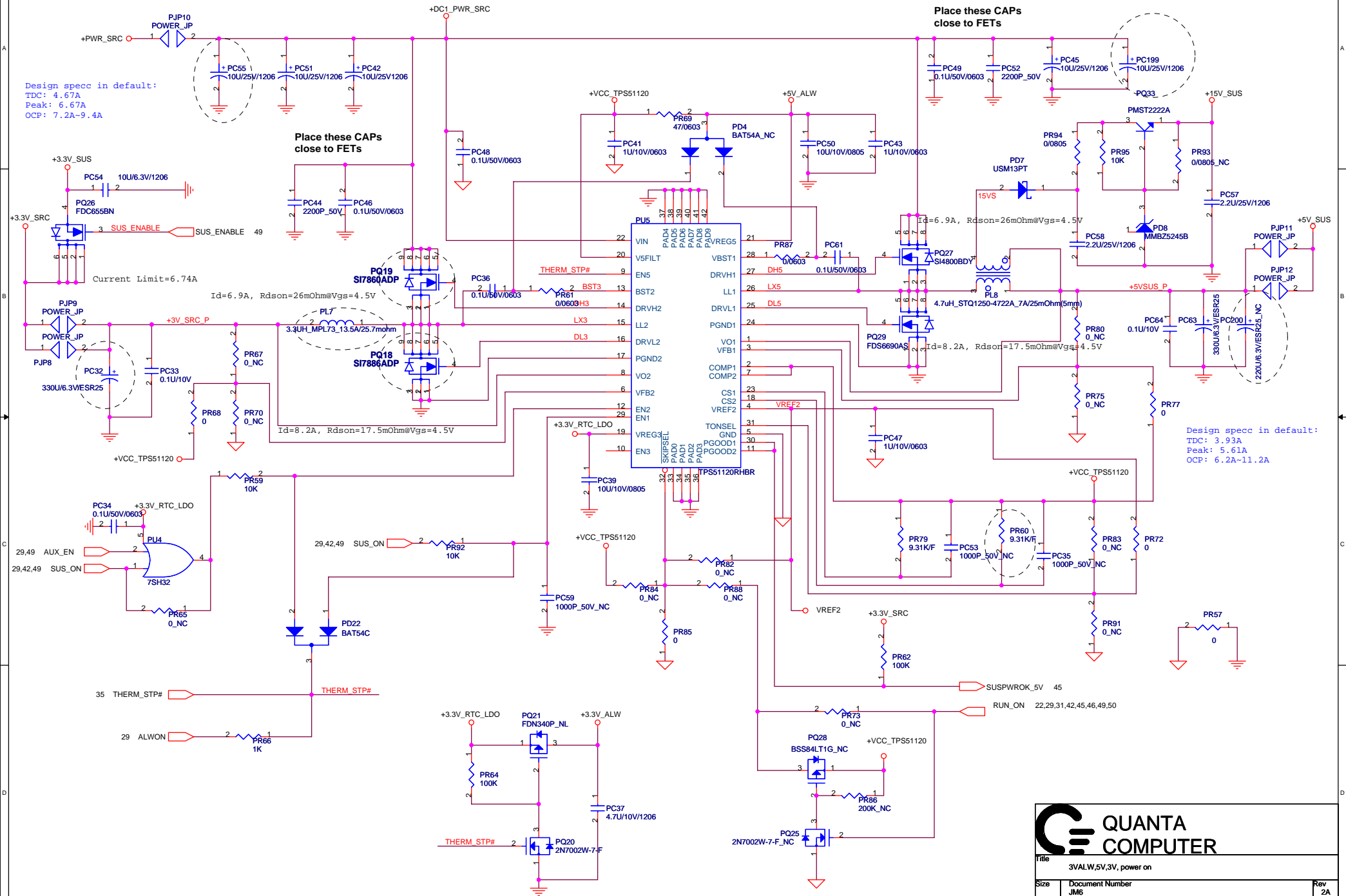
COMPUTER

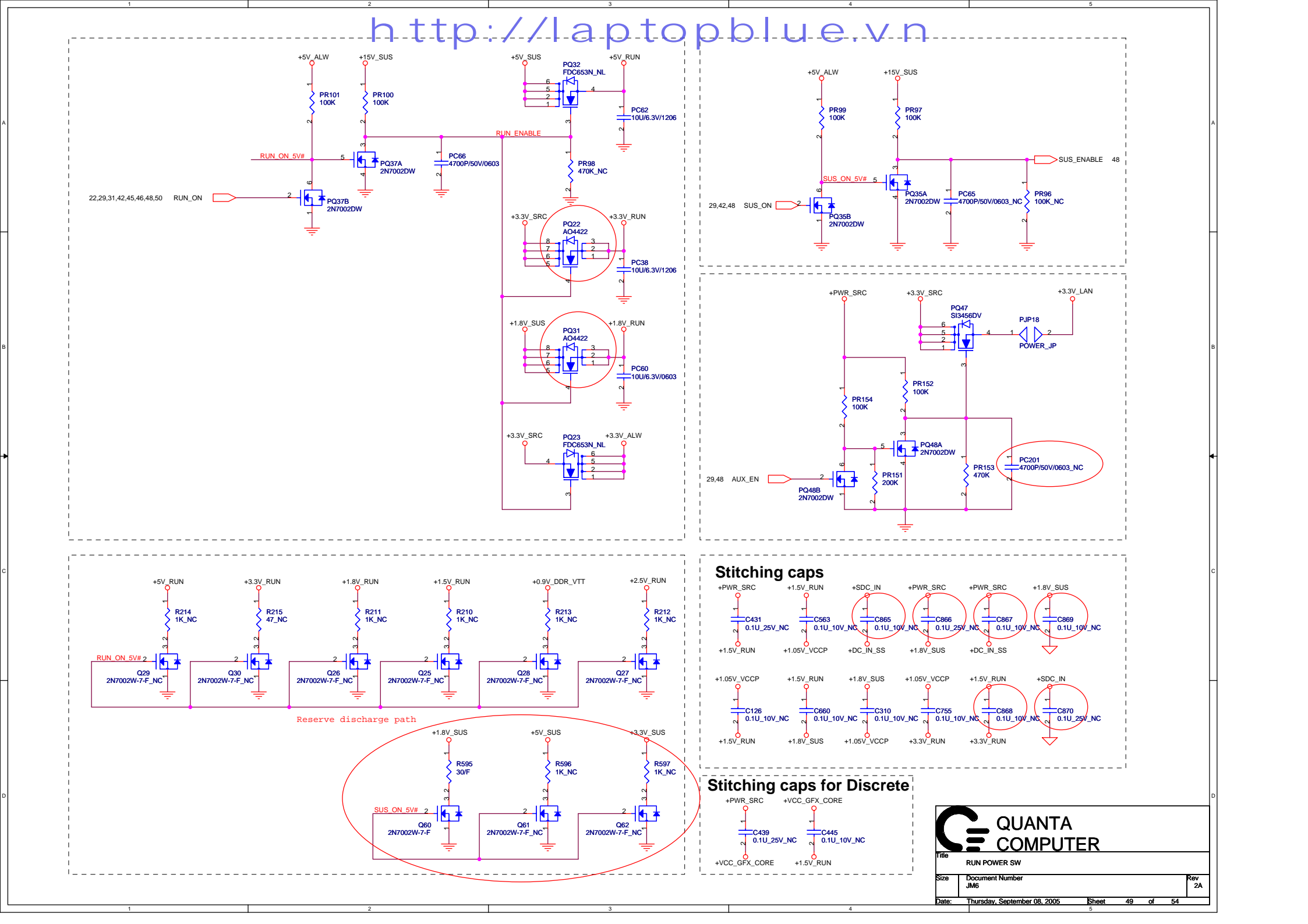
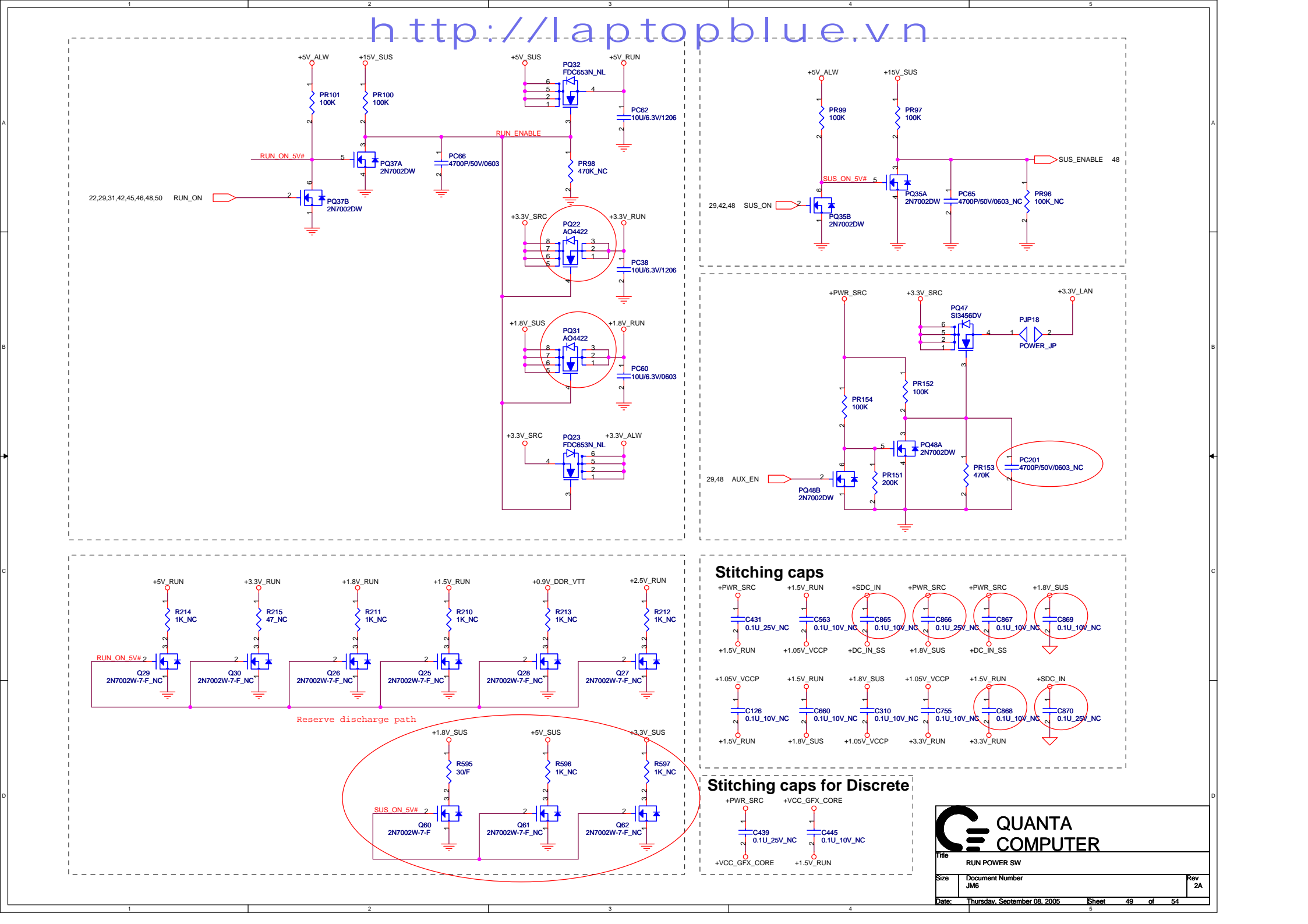
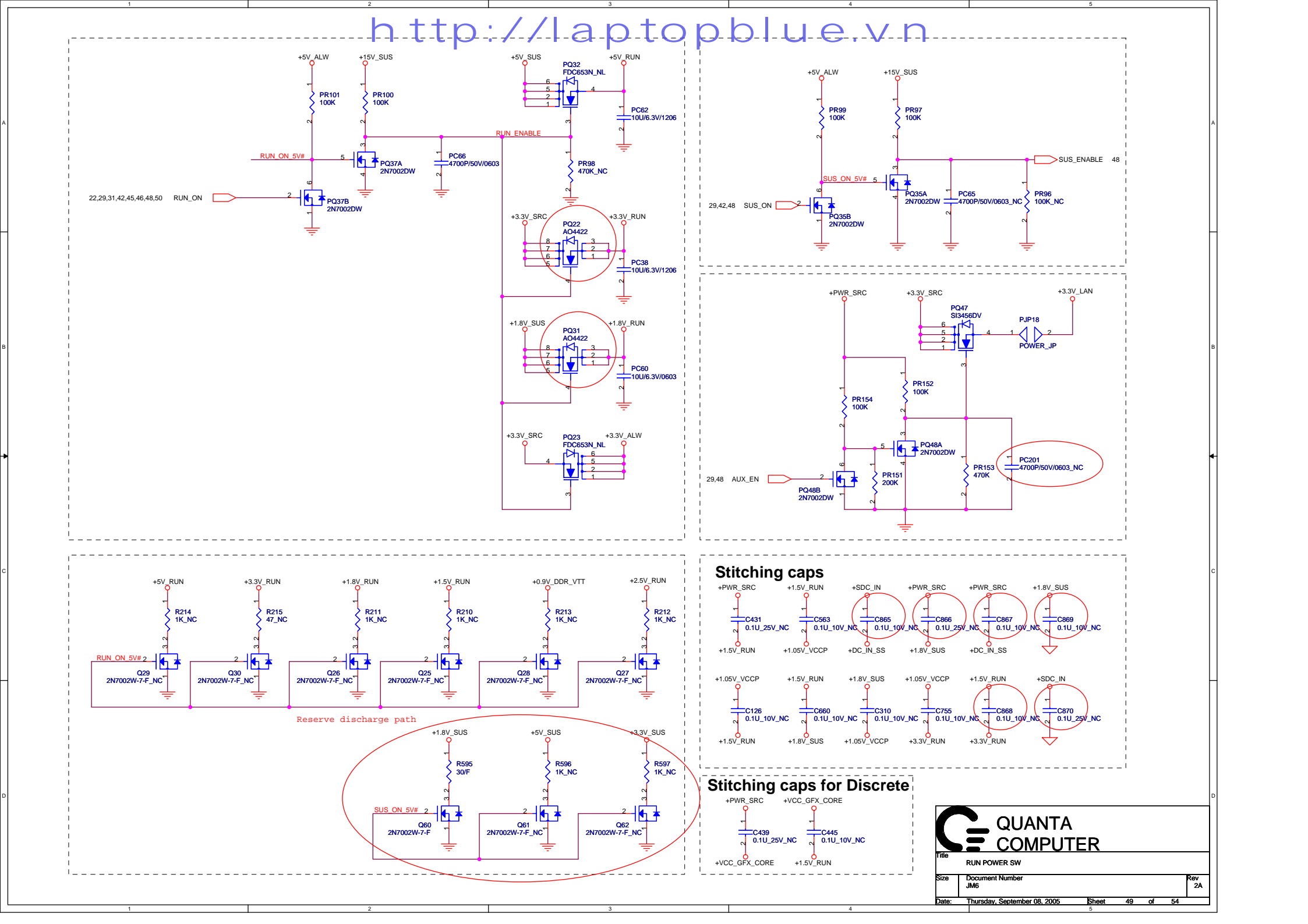
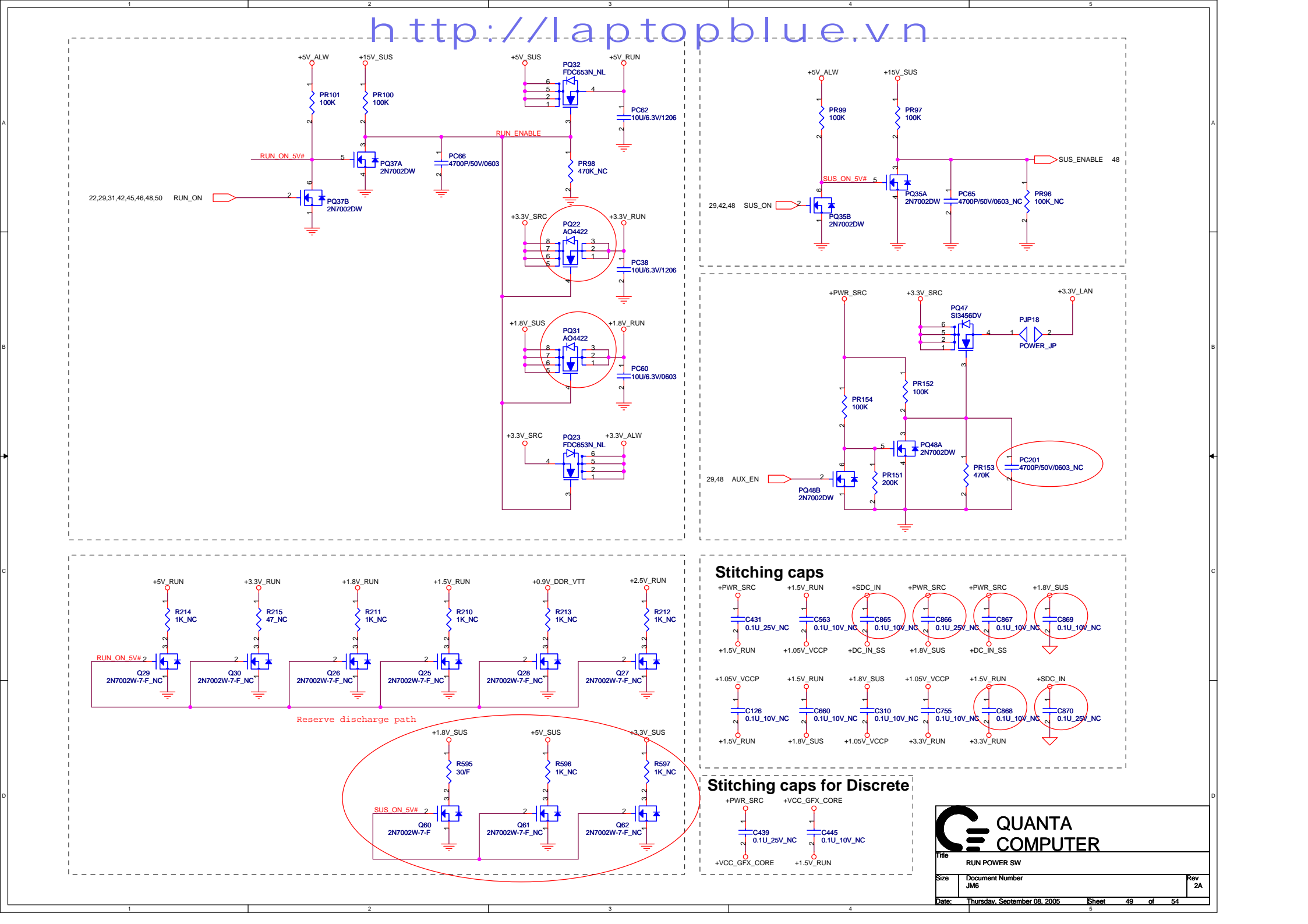
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|---------------------------------------|-----------------|-----------|
| Title BATTERY SELECTOR | | |
| Size Jm6 | Document Number | Rev 2A |
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Section 1: RUN ON 5V# and SUS_ON 5V# Control

Section 2: Power Source Selection and Switching

Section 3: Reserve discharge path

Section 4: Stitching caps

Section 5: Stitching caps for Discrete

QUANTA COMPUTER

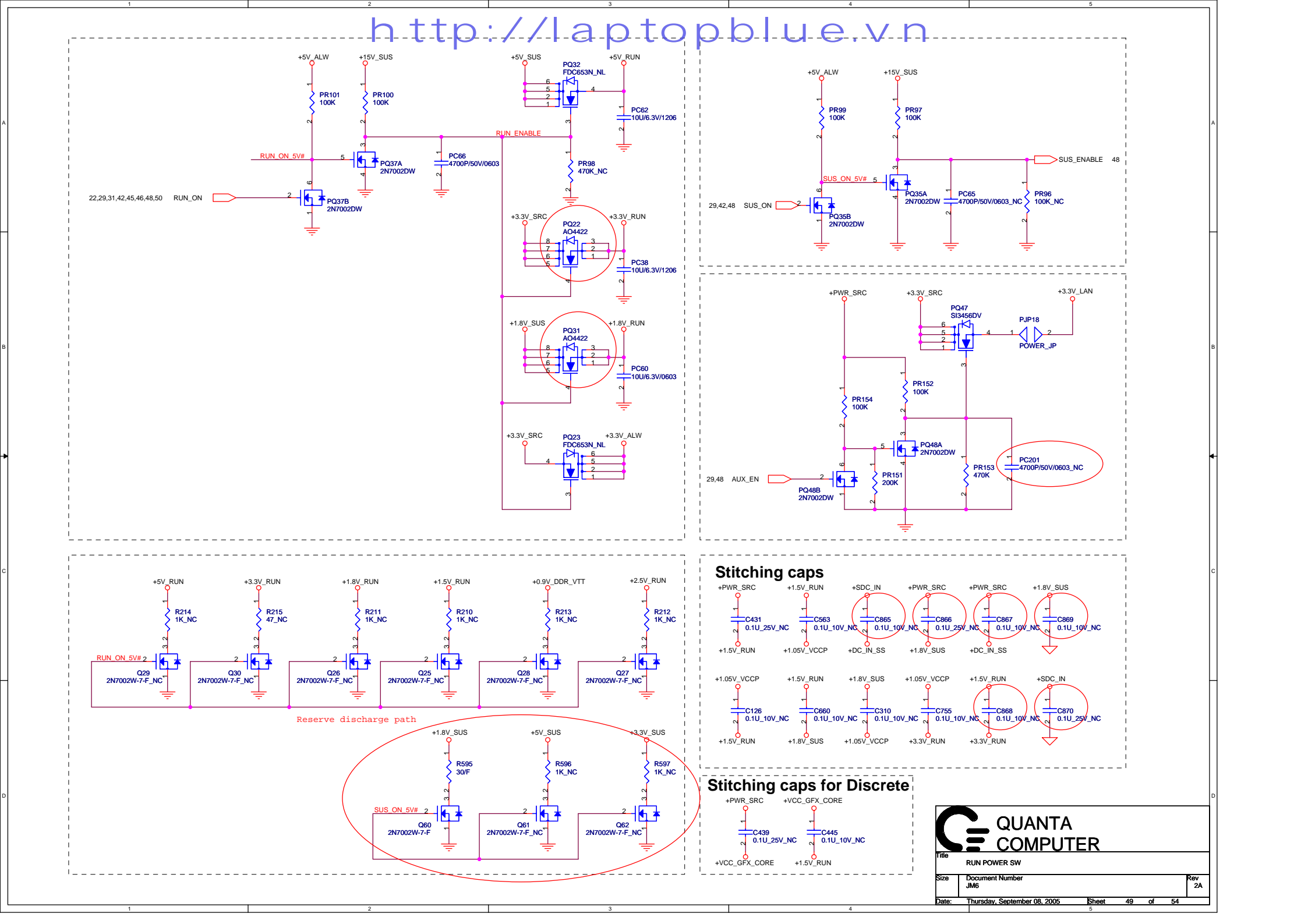
File: RUN POWER SW

Size: Document Number JM6

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Section 1: RUN ON 5V# and SUS_ON 5V# Control

Section 2: Power Source Selection and Switching

Section 3: Reserve discharge path

Section 4: Stitching caps

Section 5: Stitching caps for Discrete

QUANTA COMPUTER

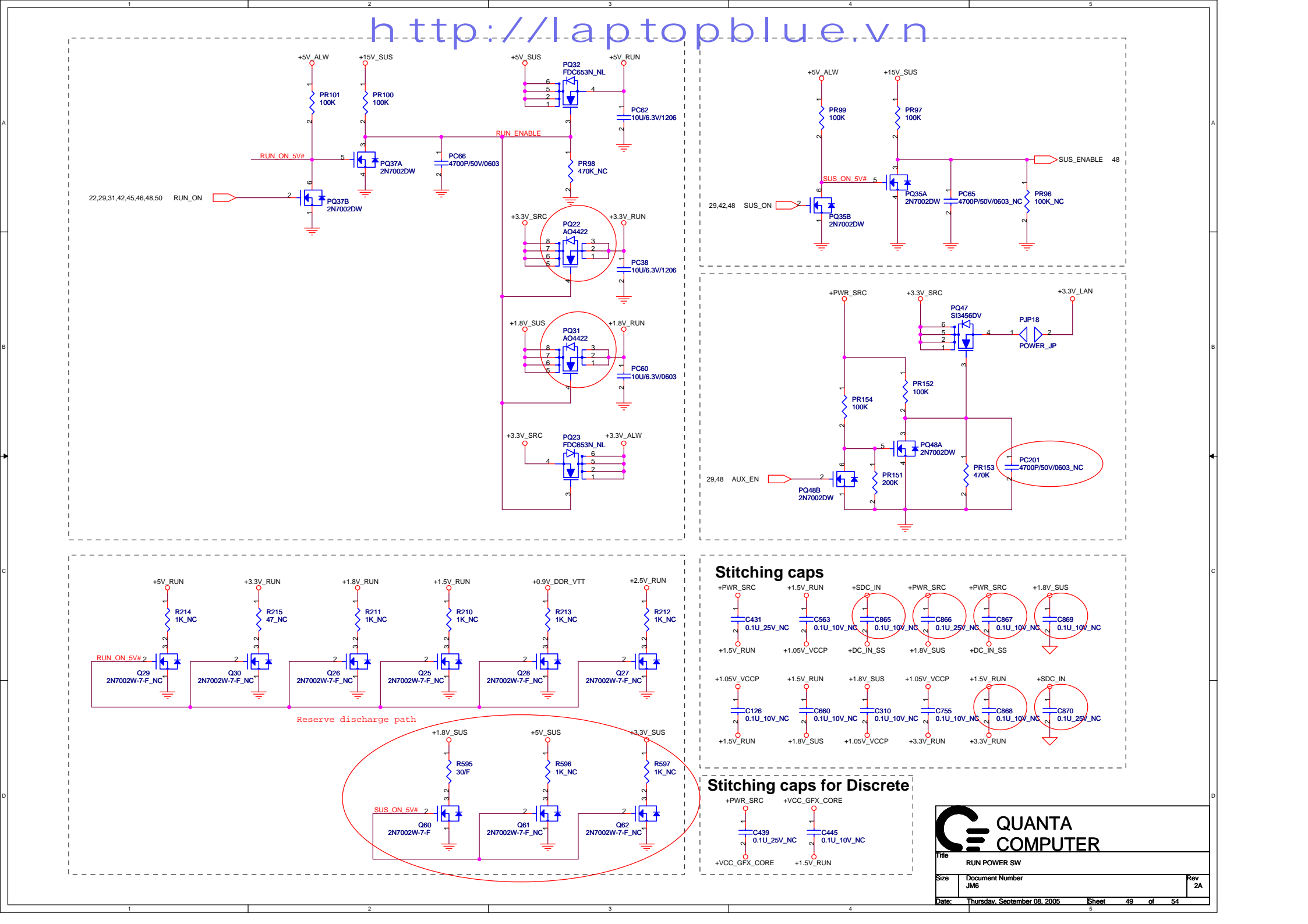
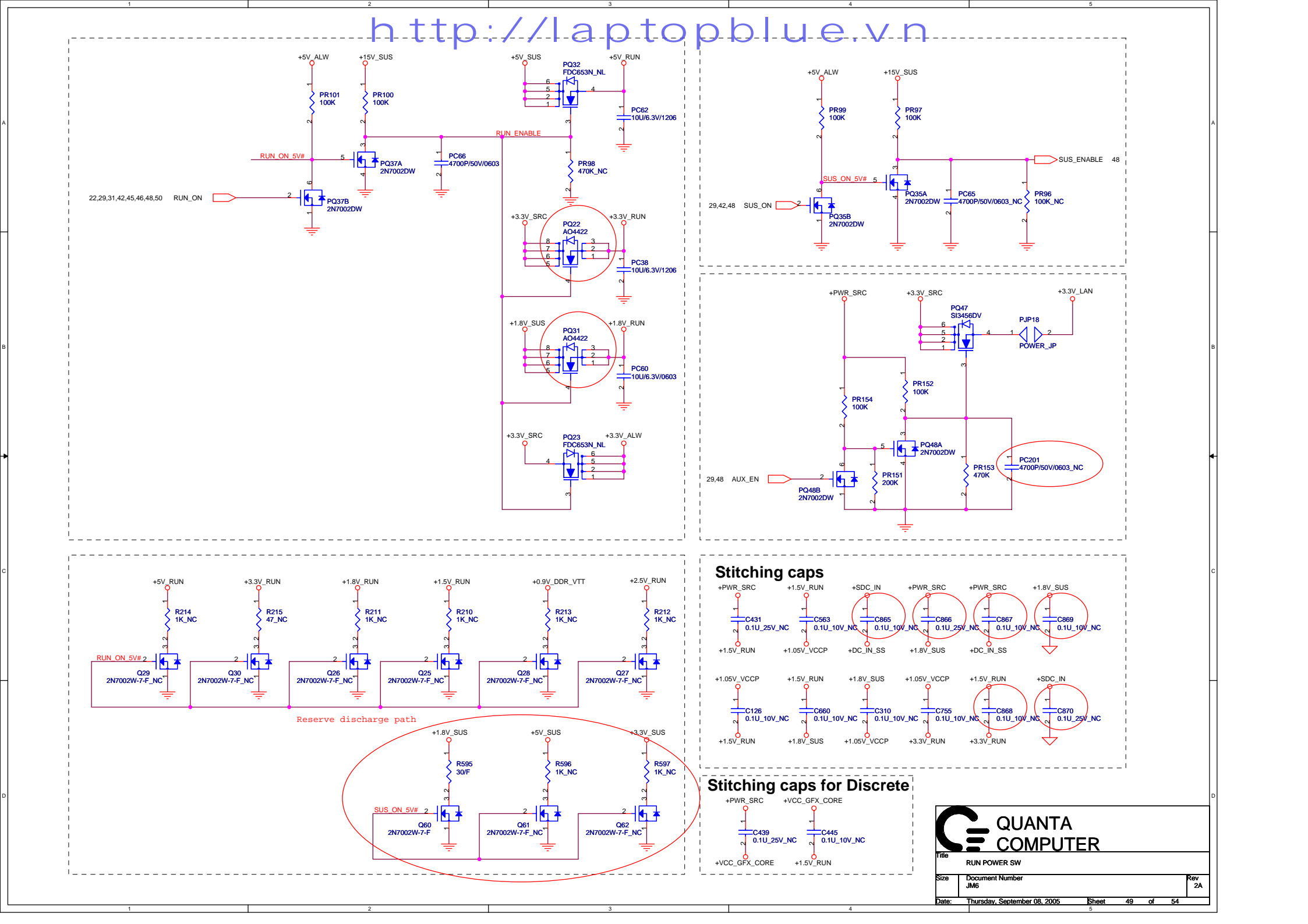
File: RUN POWER SW

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Section 1: RUN ON 5V# and SUS_ON 5V# Control

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QUANTA COMPUTER

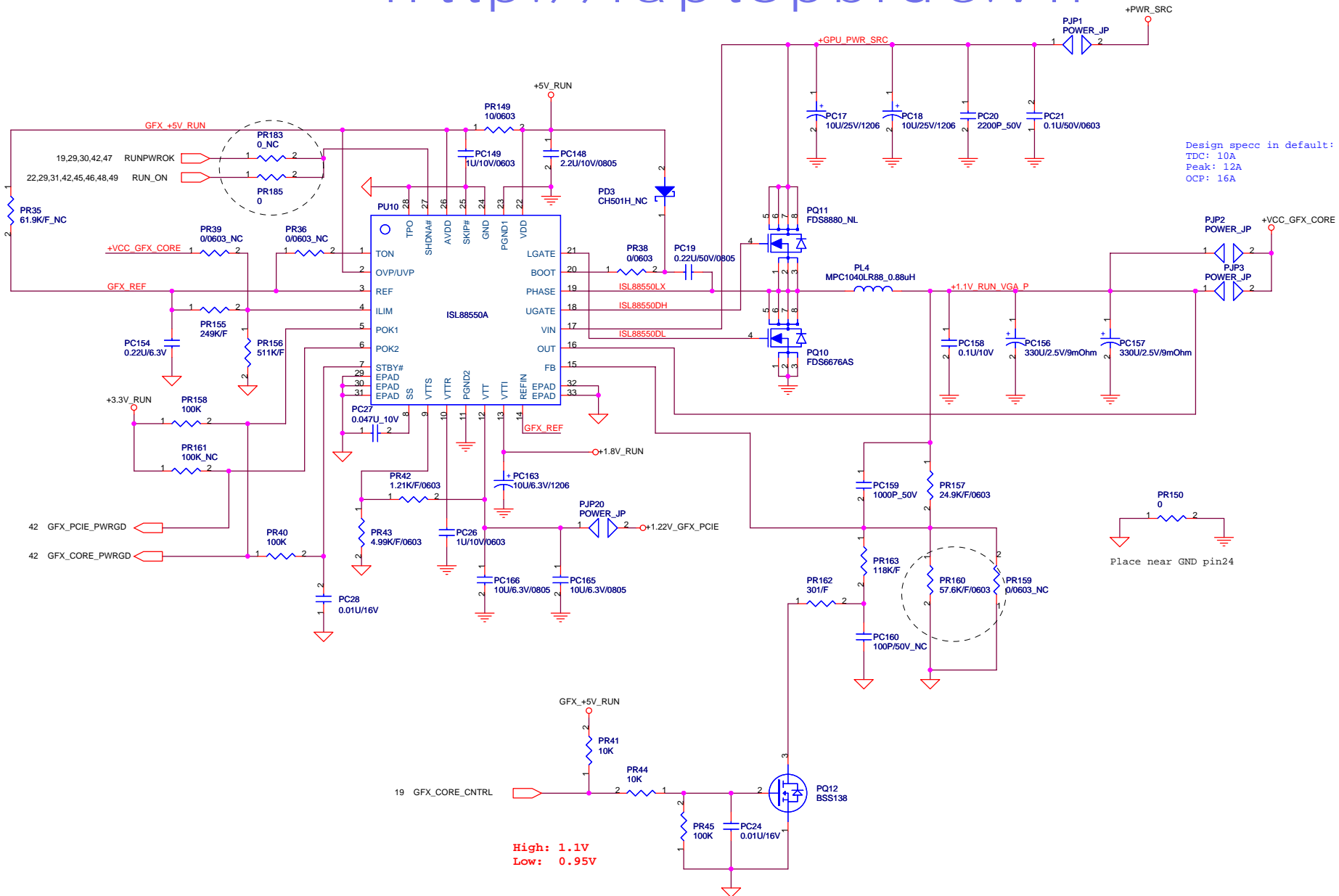
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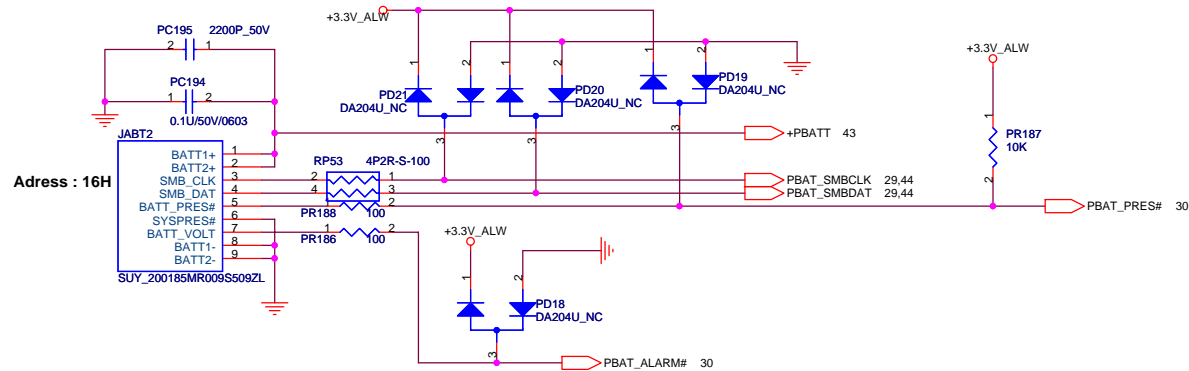
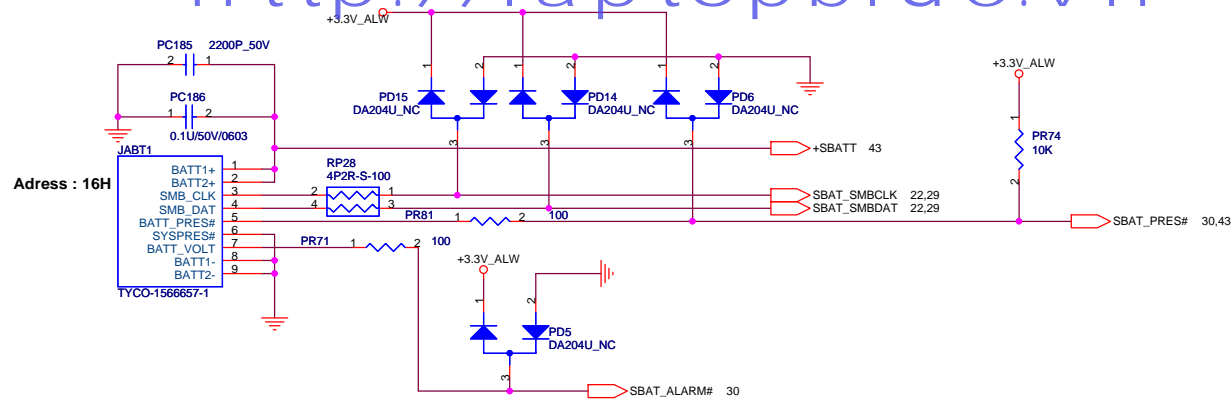
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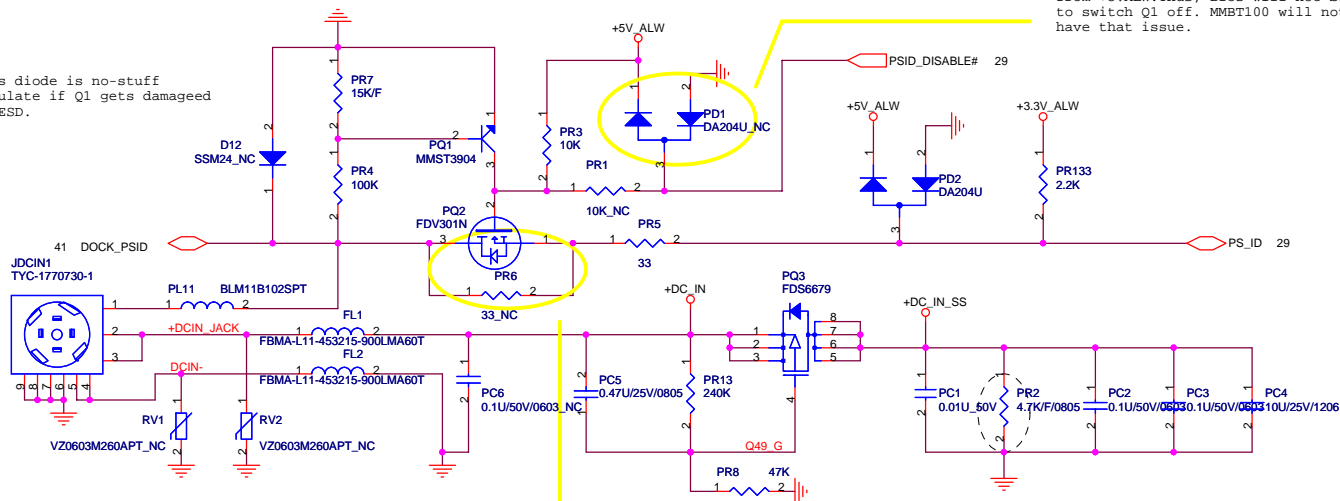
Rev: 2A



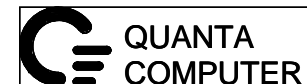


This resistor must be depopulated if FDV301N/FDV303 are used to avoid a 1.36mA constant current drain from +3VALW. Thus, Bios will not be to switch Q1 off. MMBT100 will not have that issue.

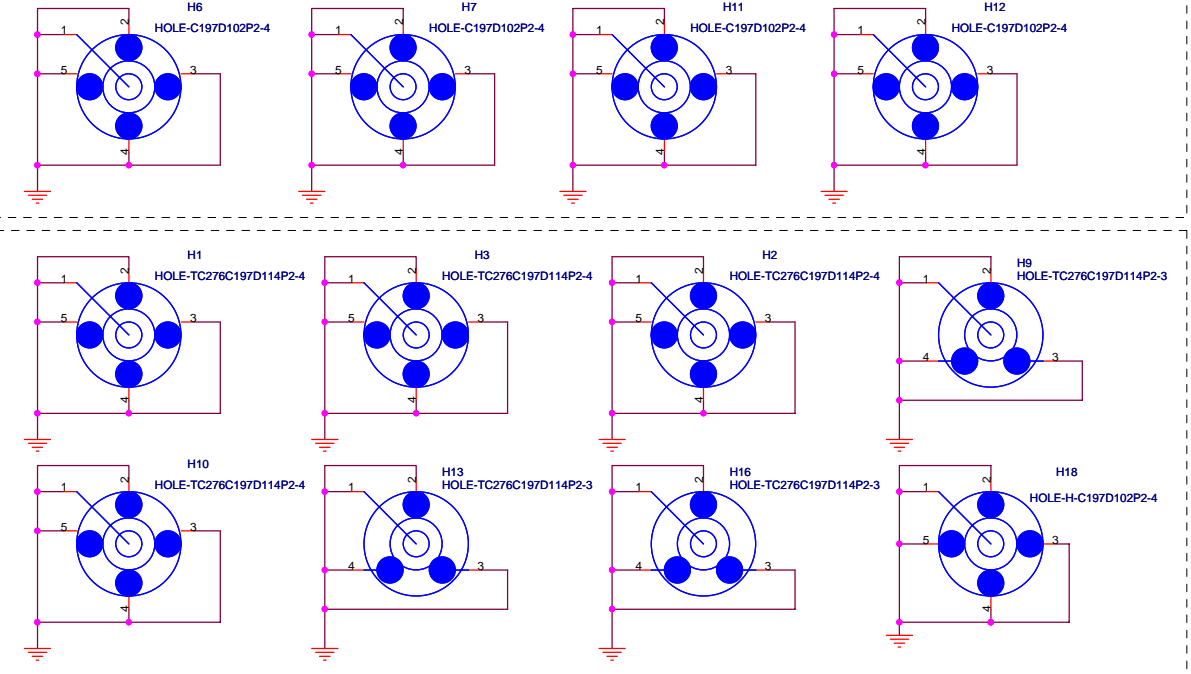
This diode is no-stuff populate if Q1 gets damaged by ESD.



Three transistor can be used for Q1 (pin compatible): FDV301N/FDV303N has low Vgs_on w/ built-in ESD protection. MMBT100 BJT works in reverse conduction mode.



CPU

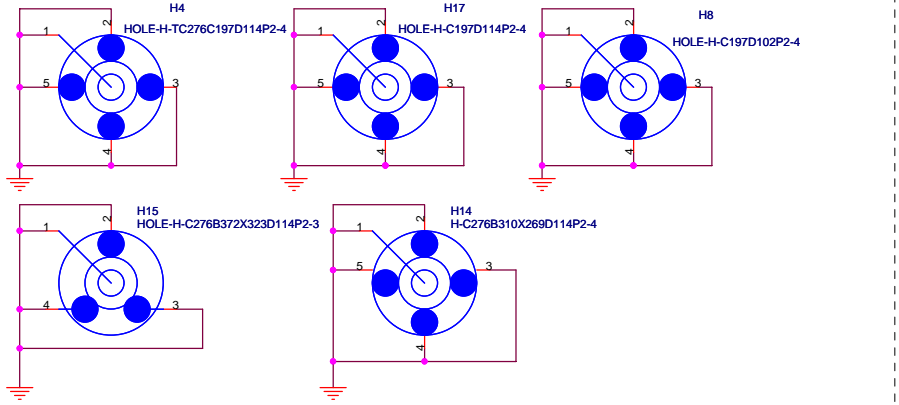


Reserved for EMI.

Reserved for EMI.

Reserved for EMI.

HDD



Reserved for EMI.

| | | |
|---|-----------------|--------|
| | | |
| Title SCREW PAD | | |
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