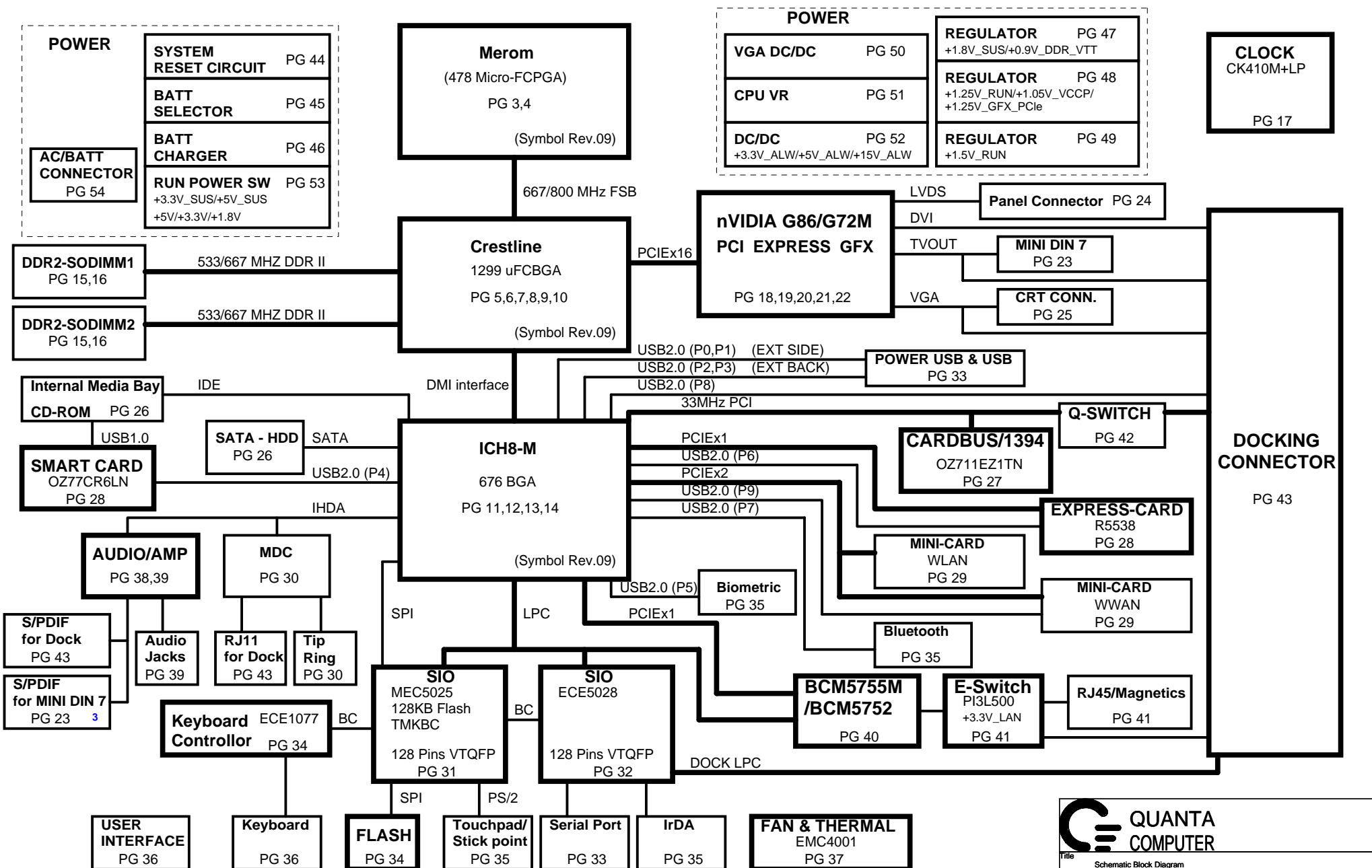


http://laptopblue.vn JM7B-DISCRETE

PWA FP382, PWB UW445,
SCHEM PM333. (128MB)
VER : 2B



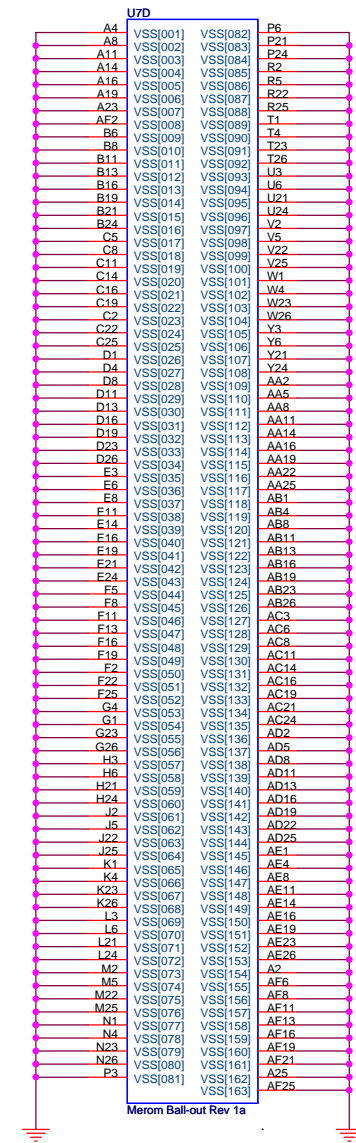
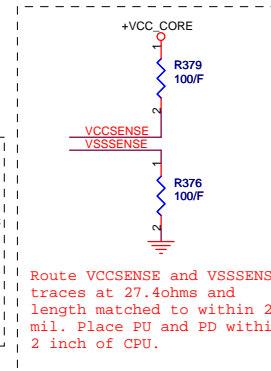
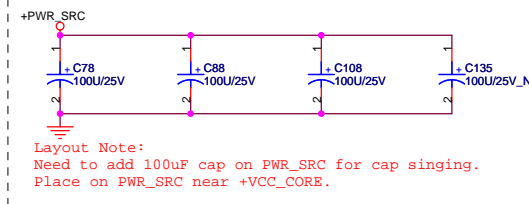
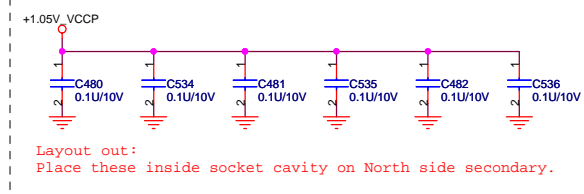
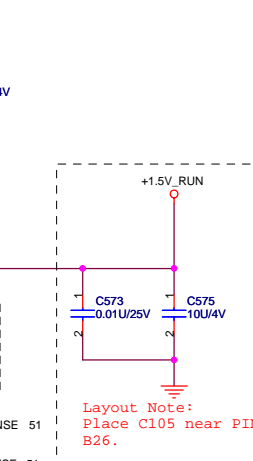
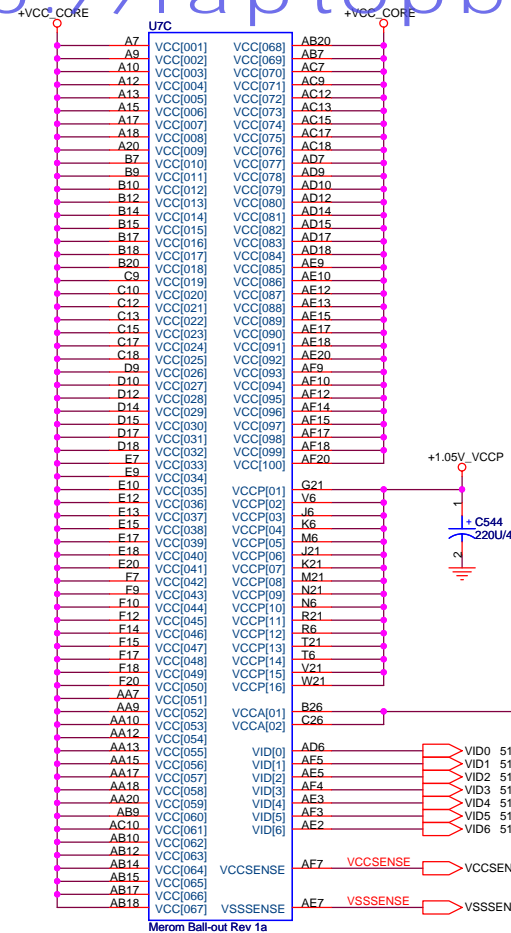
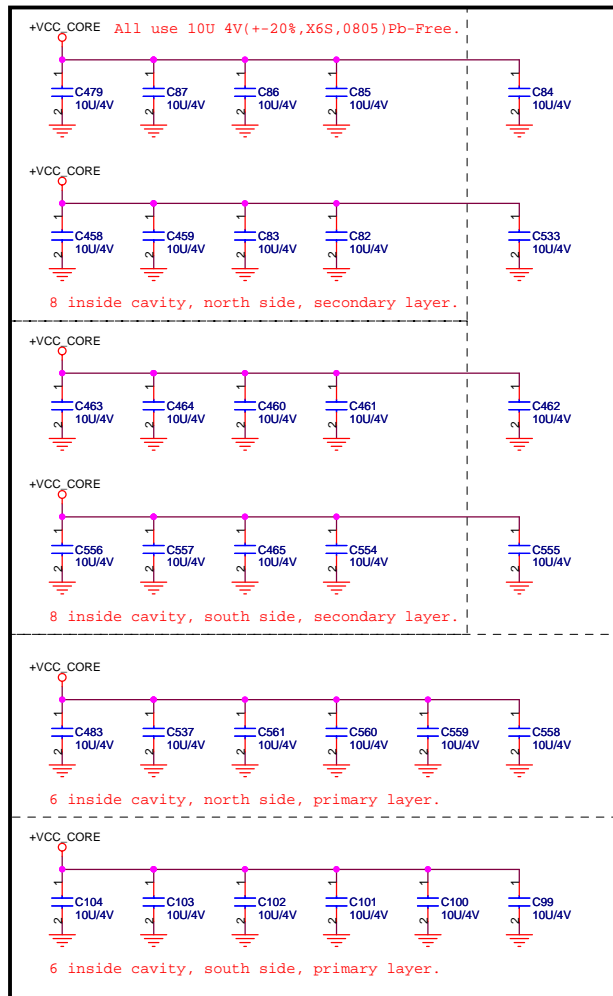
Title Schematic Block Diagram		
Size	Document Number JM7B	Rev 2B
Date: Wednesday, November 01, 2006	Sheet 1	of 57

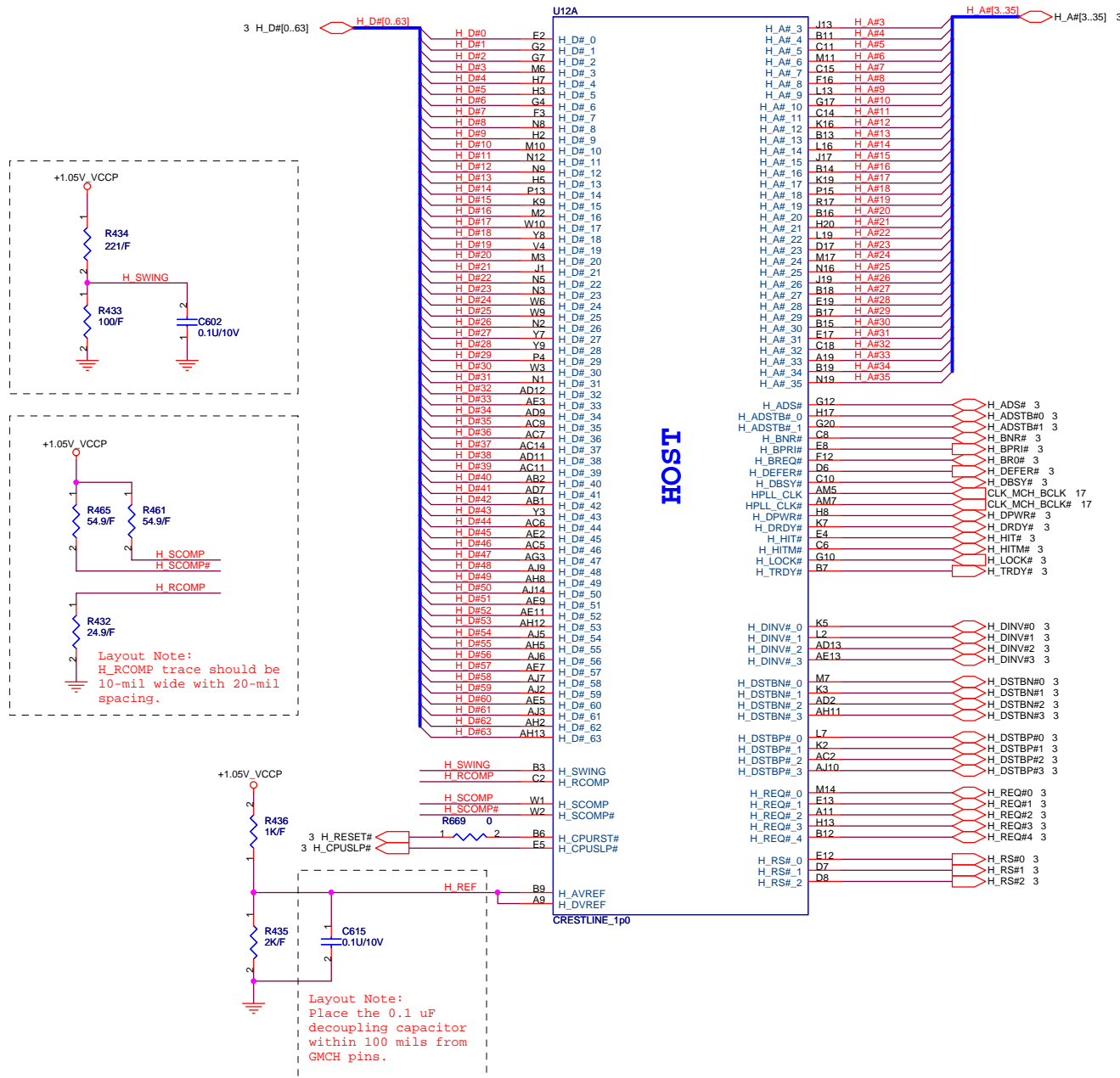
INDEX

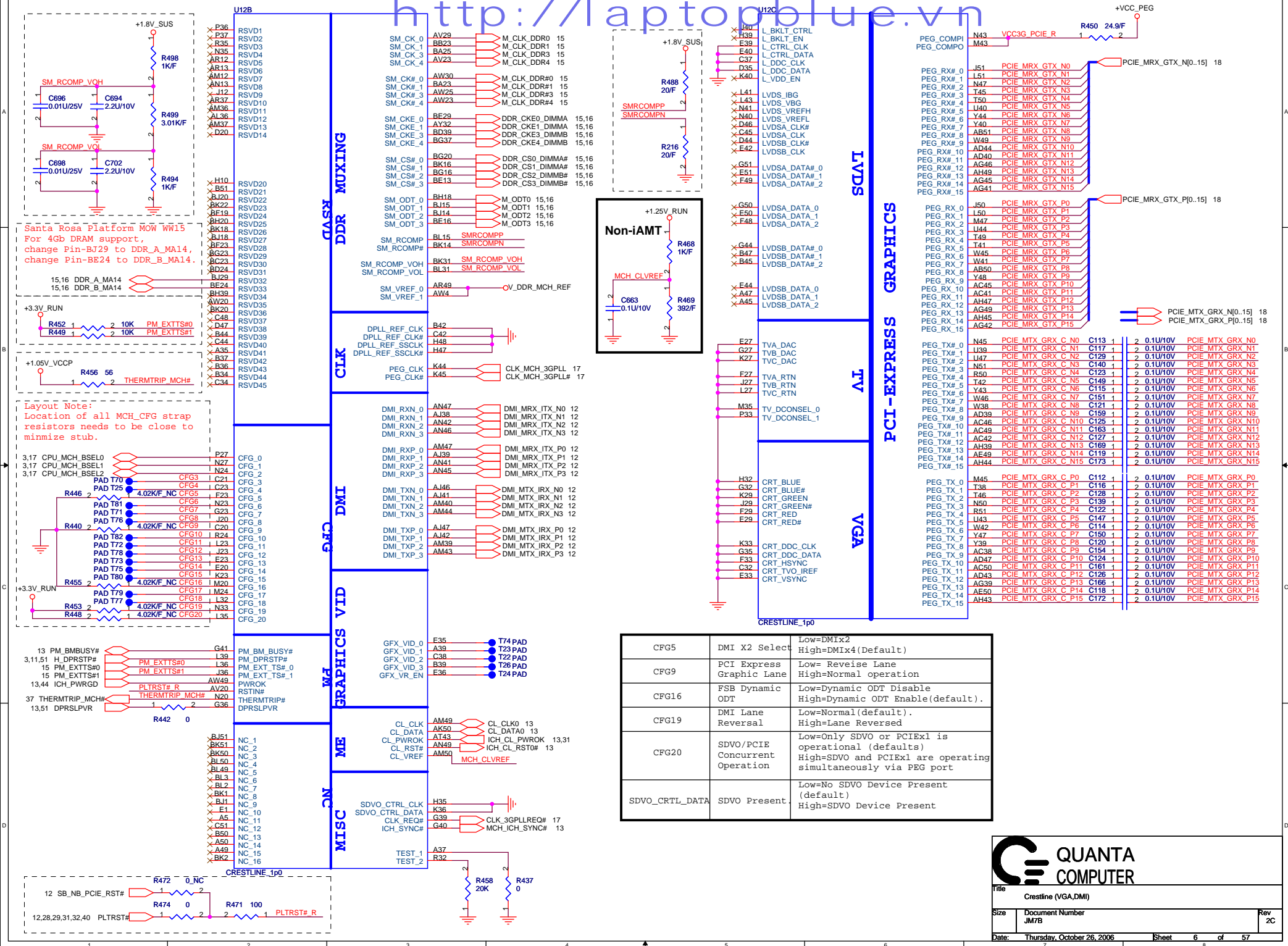
Pg#	Description
1	Schematic Block Diagram
2	Front Page
3-4	Merom
5-10	Crestline
11-14	ICH8M
15-16	DDRII SO-DIMM(200P)
17	Clock Generator
18-23	VGA
24	LCD Conn. & SSP
25	CRT Conn
26	SATA & IDE Conn
27	PCCARD/Conn & 1394
28	Express Card & Smart Card
29	Mini Card
30	MDC Conn.
31	SIO (MEC5025)
32	SIO (MEC5018)
33	SERIAL PORT & USB
34	Flash ROM, RTC & ECE1077
35	TP,BT & FIR
36	Switch,Keyboard & LED
37	FAN & Thermal
38-39	Audio CODEC(STAC9205)/Phone Jack
40-41	LOM (Nineveh)/Switch
42-43	Docking Conn/Q-Switch
44	System Reset Circuit
45-46	Battery Selector & Charger
47	DDR2_1.8VSUS, 0.9V
48	1.5VSUS,1.05V(VTT)
49	VGA DC/DC,1.25V,1.05V
50	CPU_MAX8786(3phase)
51	D/D Power
52	RUN Power Switch
53	DCIN,Batt
54	PAD& SCREW
55	EMI CAP
56	SMBUS BLOCK

Power States

Power Rail	Control Signal	S0/M0	S3/M1	S3/M1	S4/M1	S3/M-off	S4/M-off	S5/M-off
+3.3V_ALW								
+5V_ALW								
+3.3V_LAN								
+1.25V_SRC_M								
+1.05V_M								
+1.8V_SUS								
+0.9V_DDR_VTT								
+5V_SUS								
+3.3V_SUS								
+5V_RUN								
+3.3V_RUN								
+1.8V_RUN								
+1.25V_RUN								
+1.5V_RUN								
+1.05V_VCCP								
VCC_VCRE								
+LCDVCC								
+5V_MOD								
+VCC_GFX_CORE								
+1.25V_GFX_PCle								
+2.5V_RUN								







Title Crestline (VGA,DM

Size

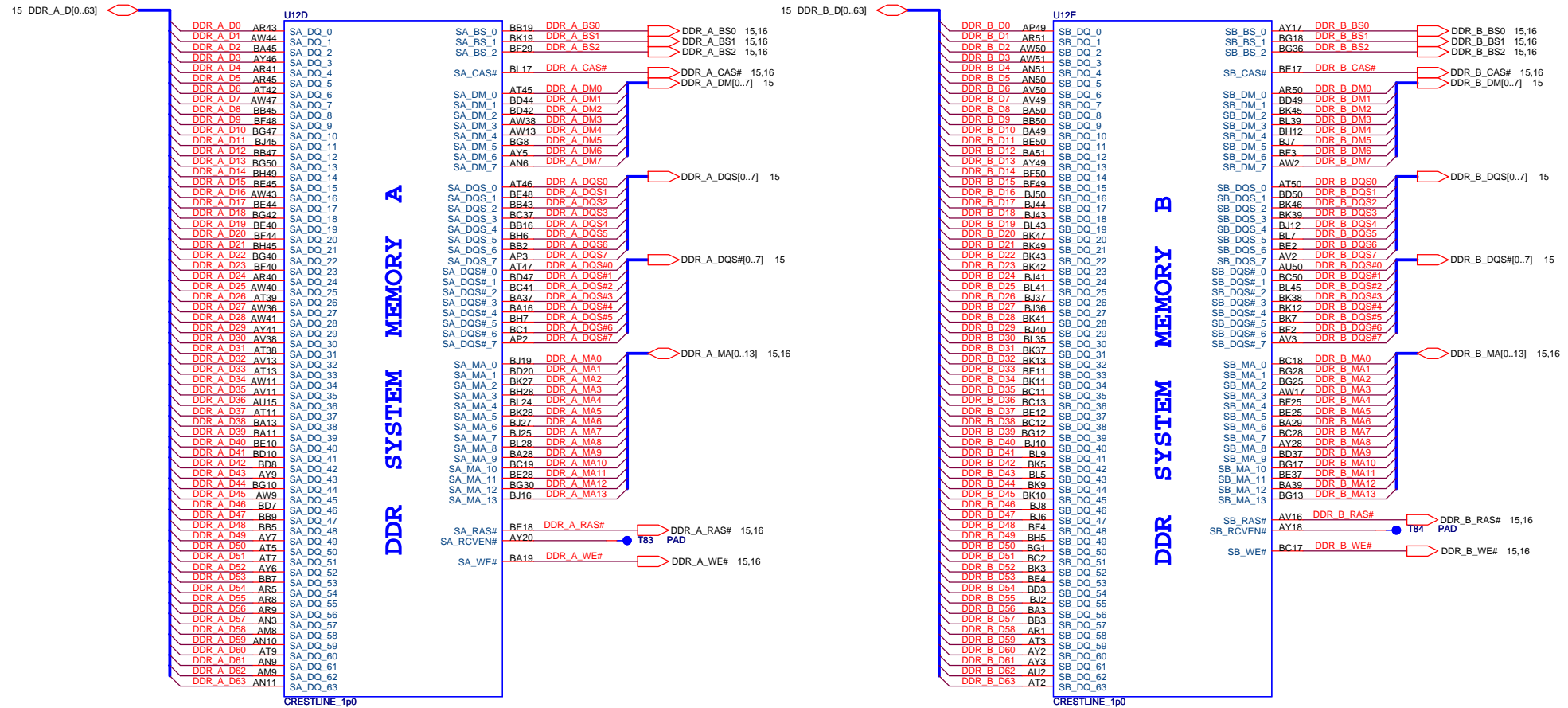
Document Number

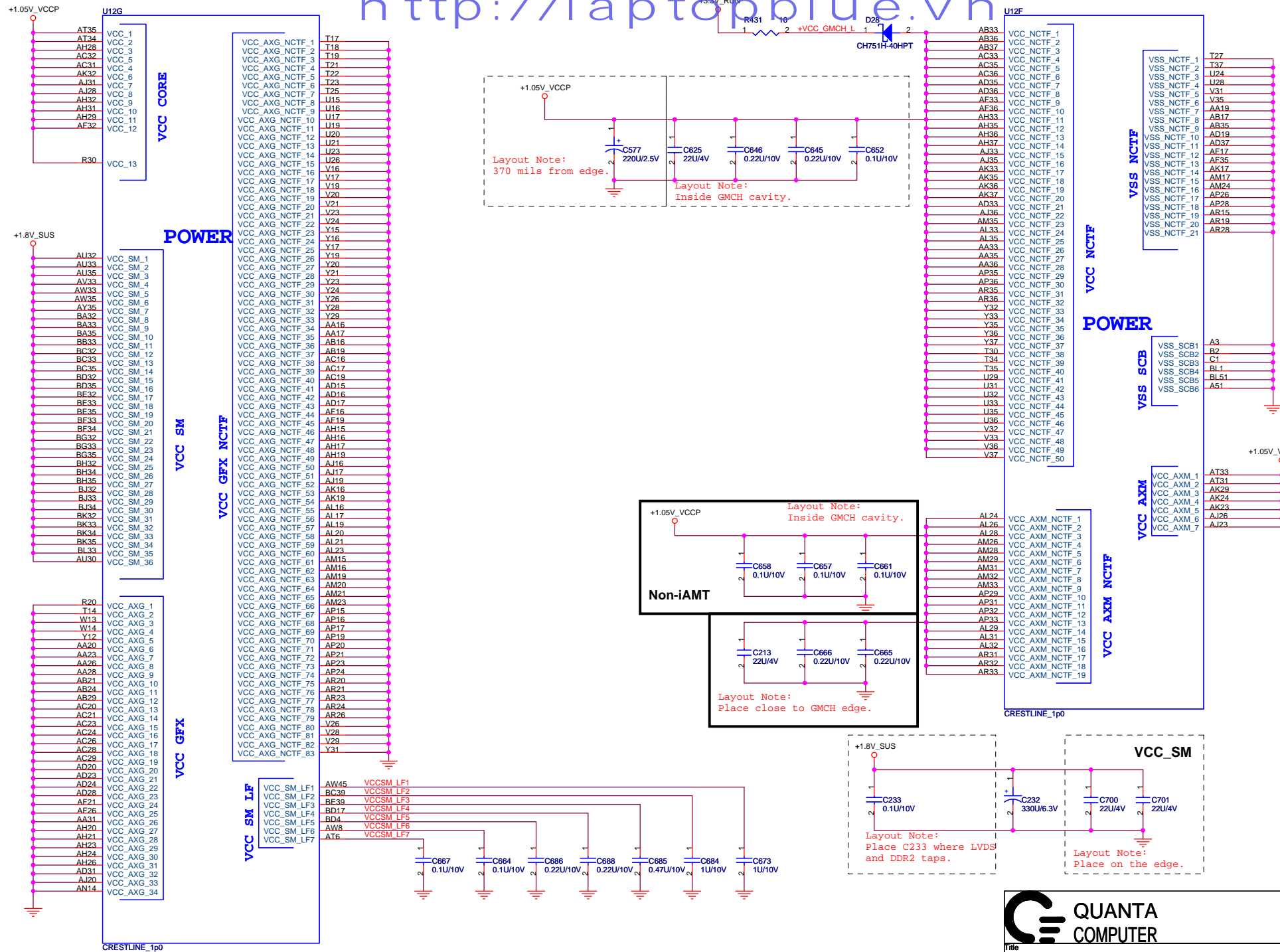
11

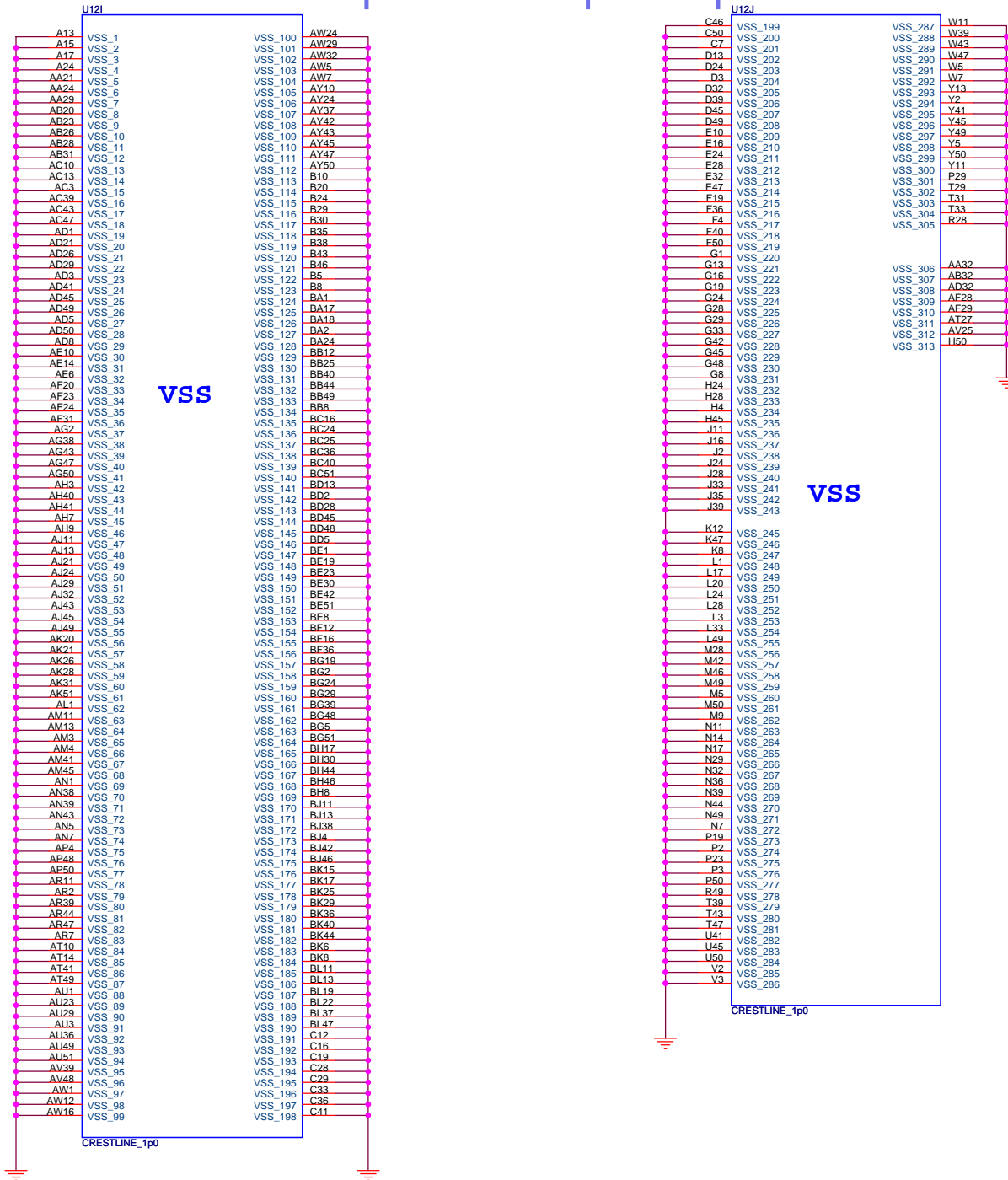
JM7B

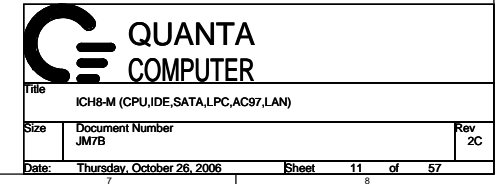
Rev

2C

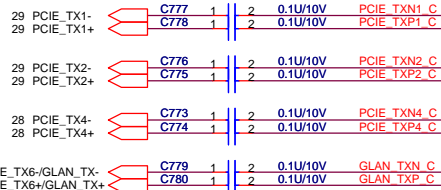




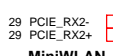




Place TX DC blocking caps close ICH8.



MiniWWAN



MiniWLAN



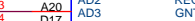
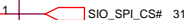
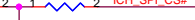
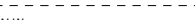
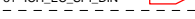
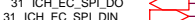
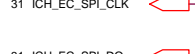
Express Card



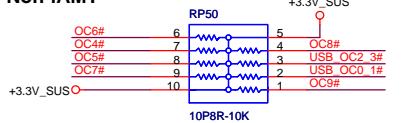
Giga Bit LOM



Layout Note:
Place R581, R582 within
500 mils from ICH.



Non-iAMT



Short F2 and F3 at the package
and keep length to less than
500mils. Trace Impedance
should be 60ohms +/- 15%.

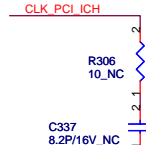
Boot BIOS Strap

	GNT0#	SPI_CS1#
LPC	11	No stuff
PCI	10	No stuff
SPI	01	Stuff

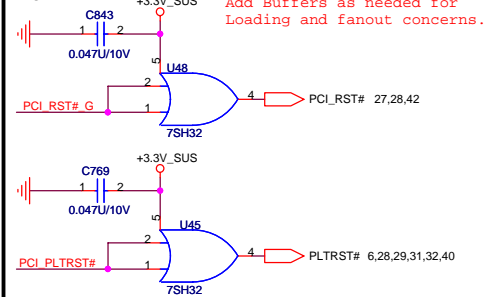
A16 away override strap.

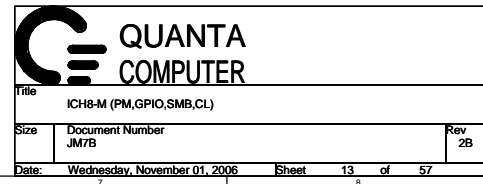
SB_NB_PCIE_RST#	Low = A16 swap override enabled. High = Default.
-----------------	---

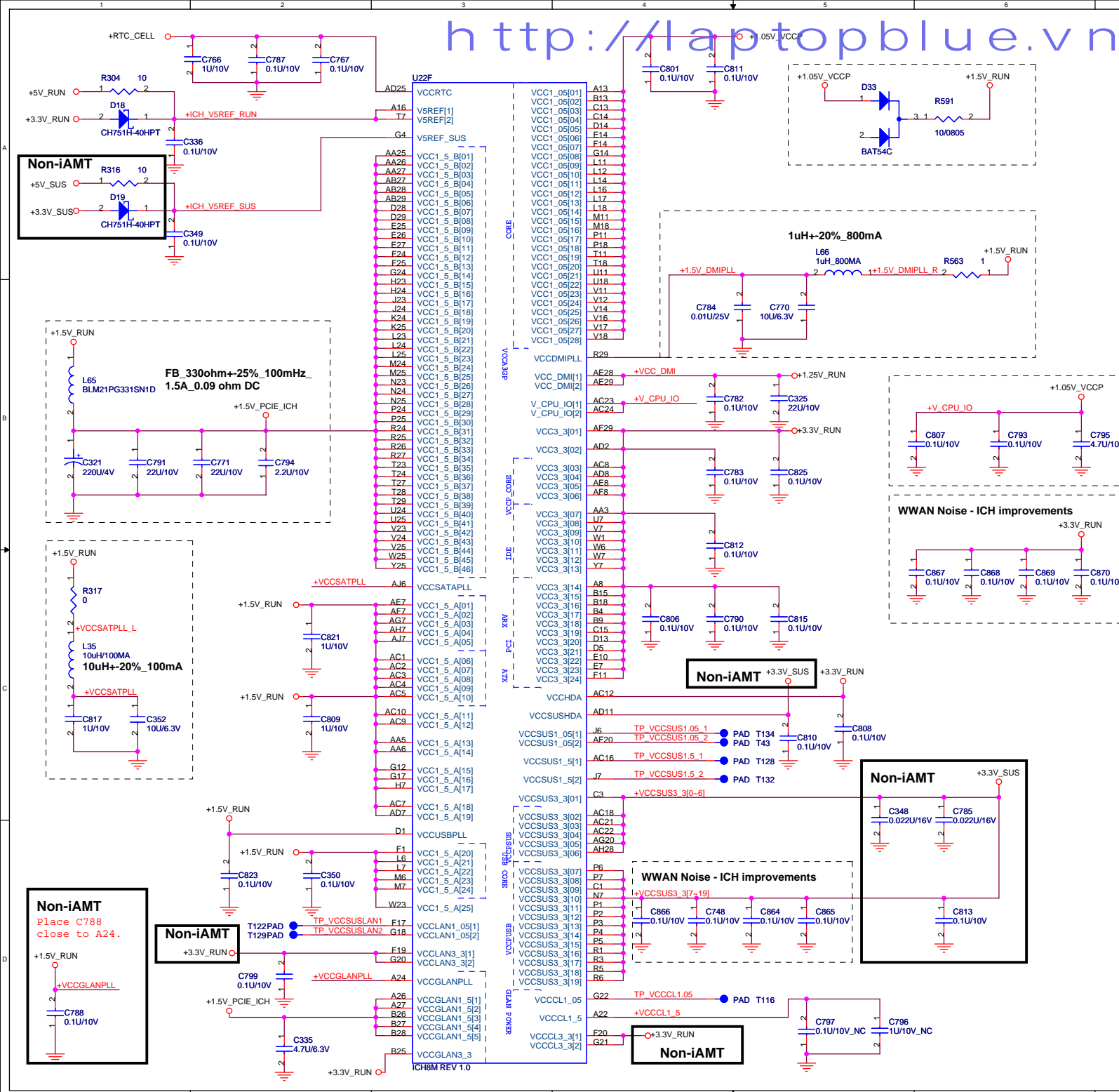
DOCK	REQ0	GNT0	PIRQA
Cardbus or	REQ1	GNT1	PIRQD
1394/MediaCard	REQ2	GNT2	PIRQC
			PIRQD



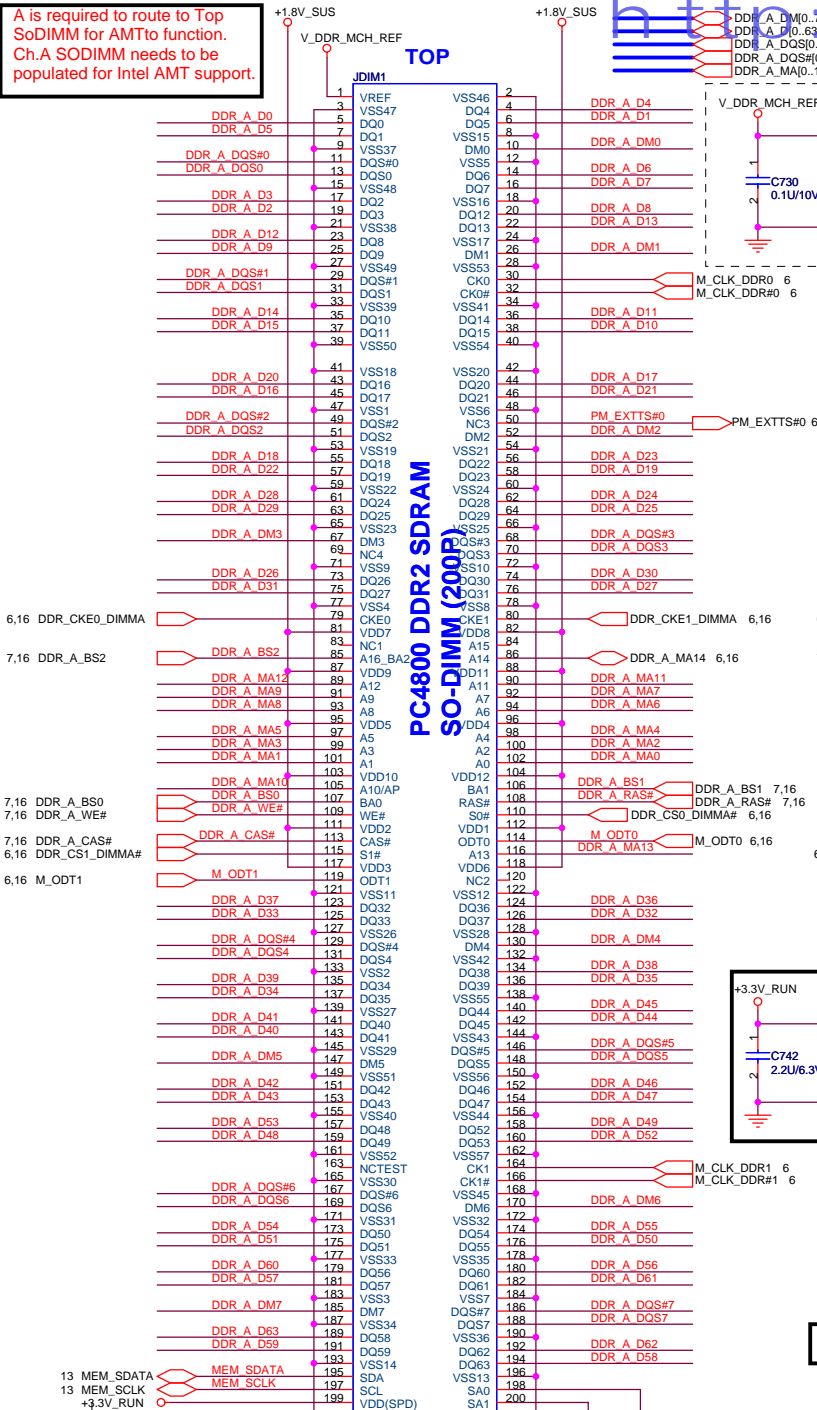
Non-iAMT







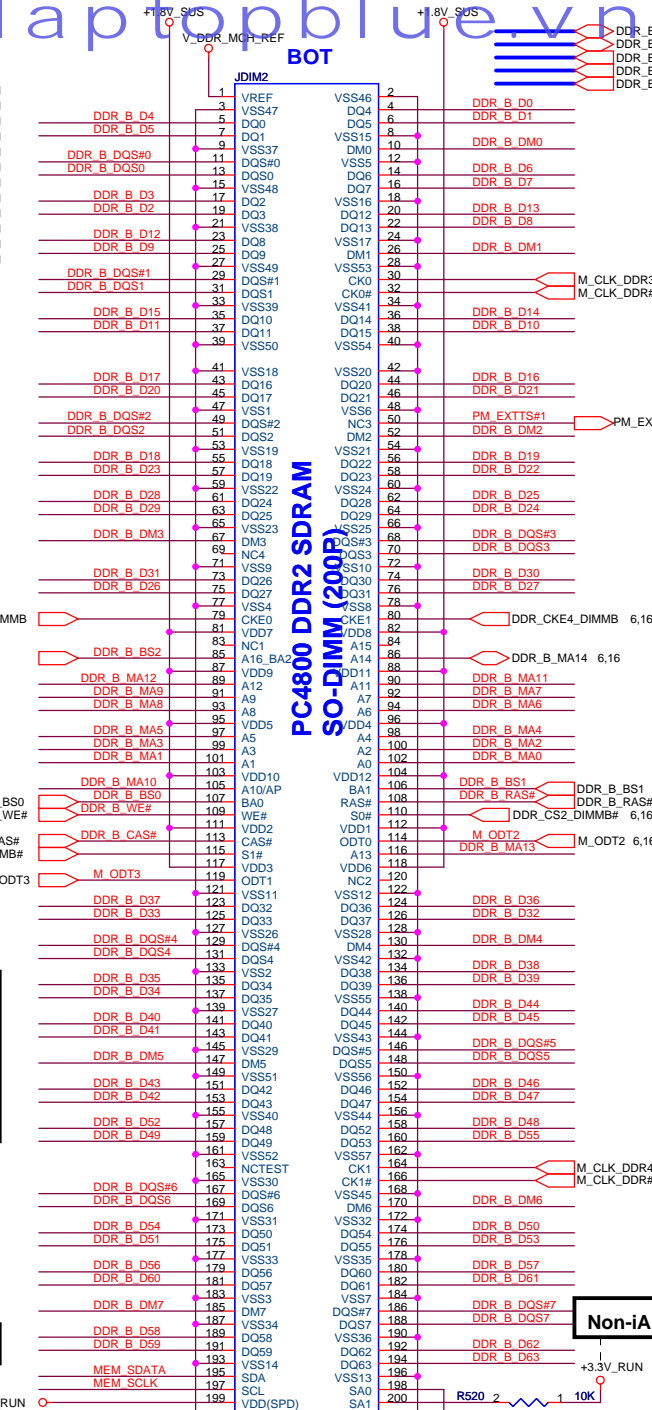
A is required to route to Top SoDIMM for AMTto function. Ch.A SODIMM needs to be populated for Intel AMT support.



Non-iAMT
hexainf@hotmail.com
GRATIS - FOR FREE

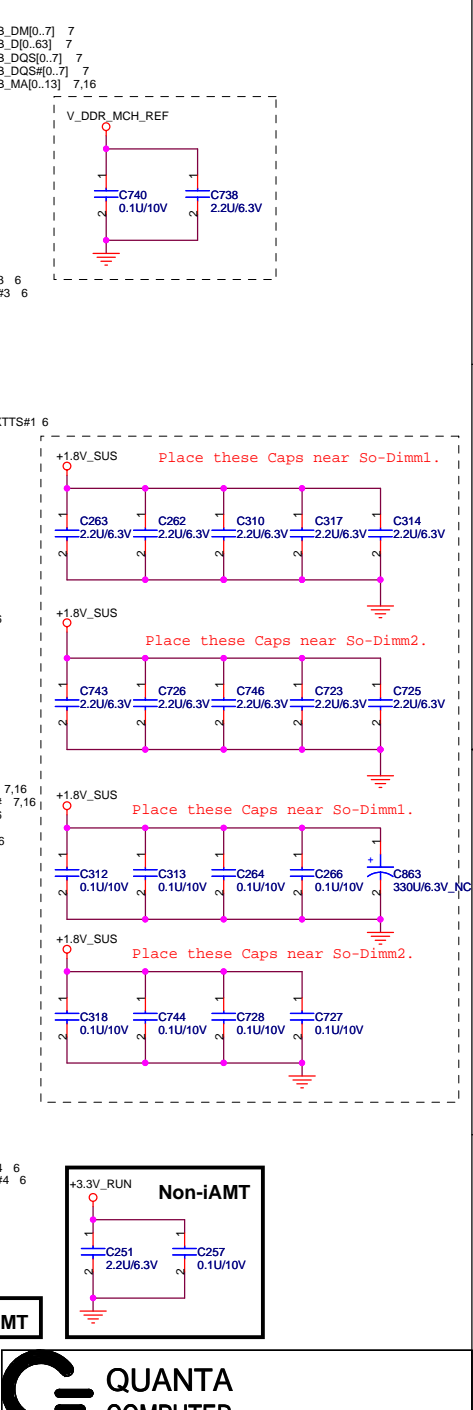
CLOCK 0,1
CKE 0,1

Non-iAMT

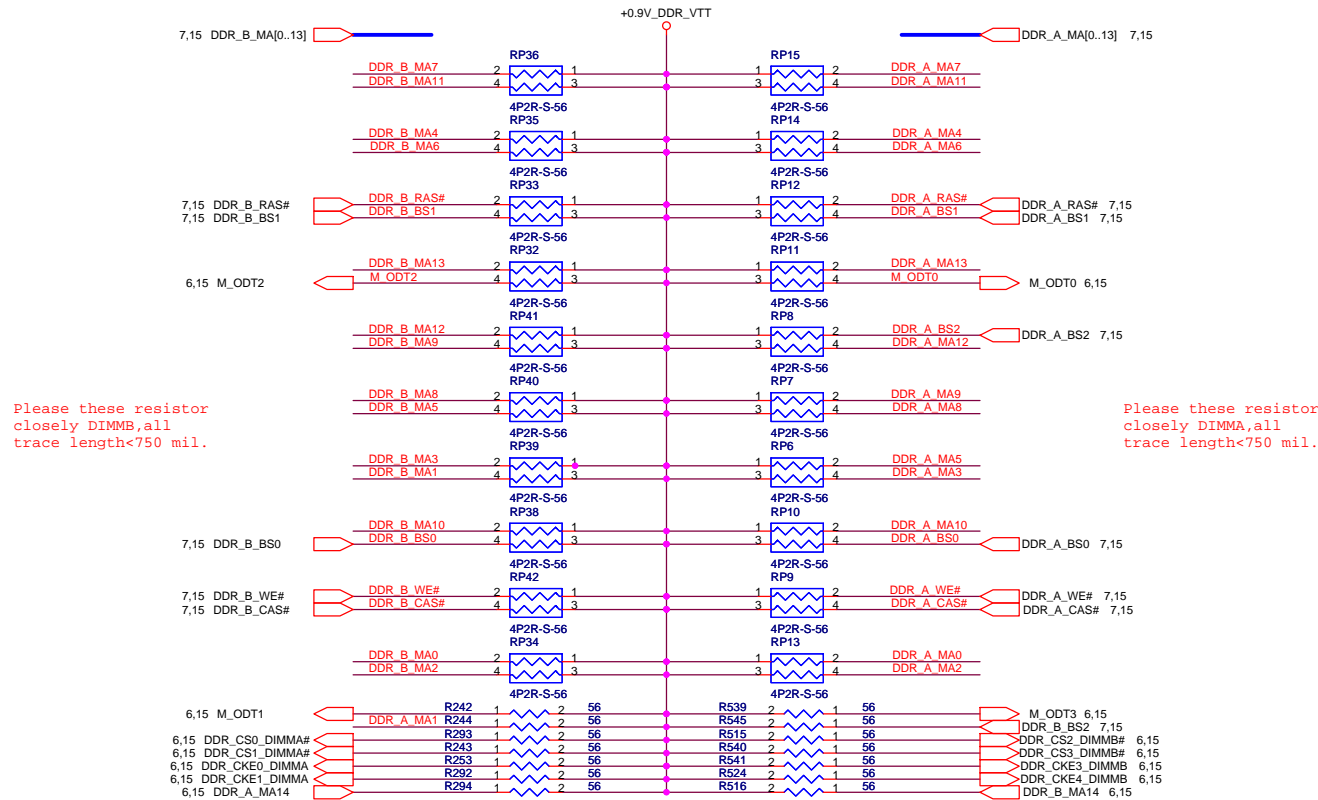
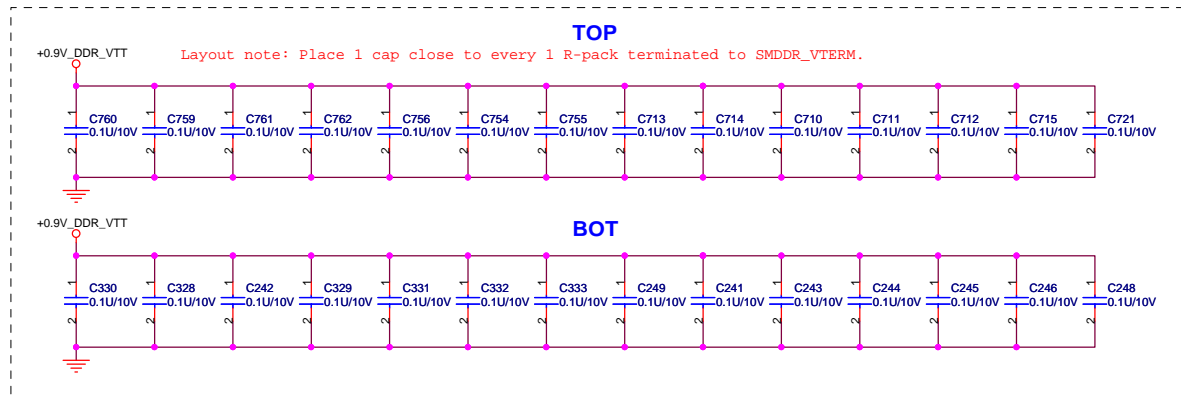


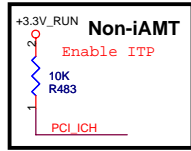
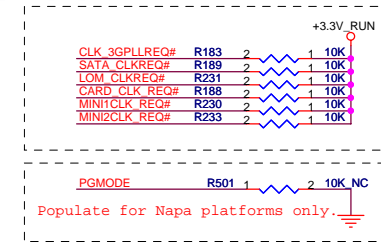
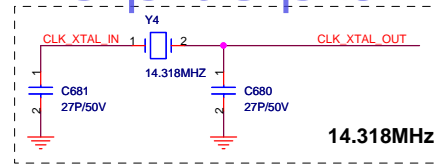
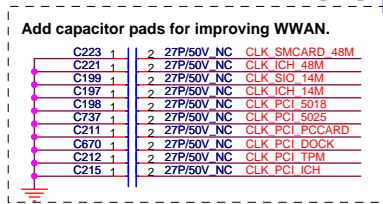
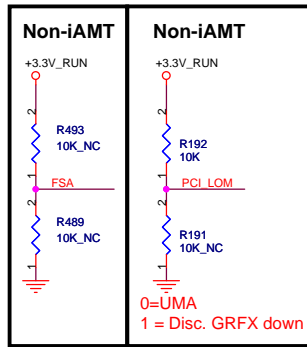
Non-iAMT
SMbus address A4
CLOCK 2,3
CKE 2,3

Non-iAMT

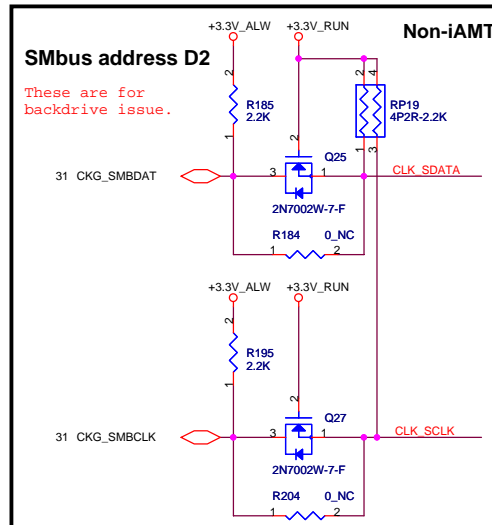
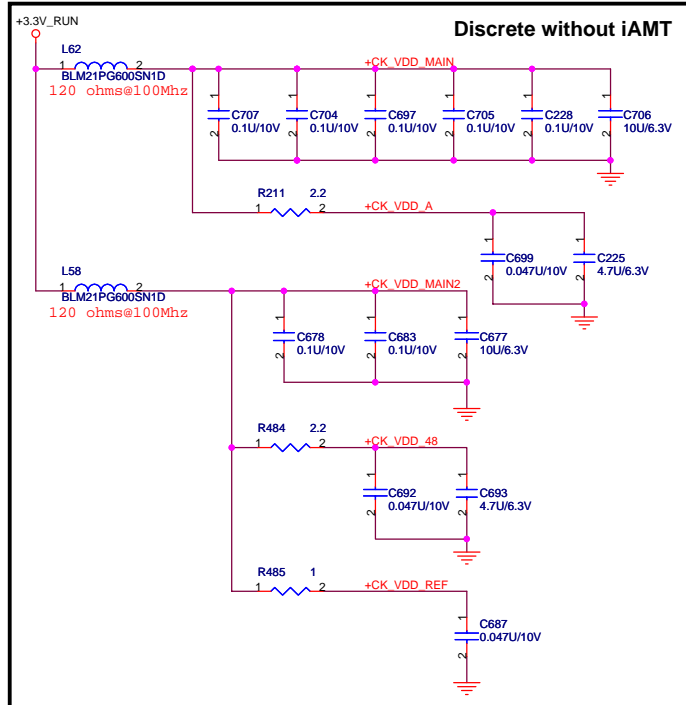
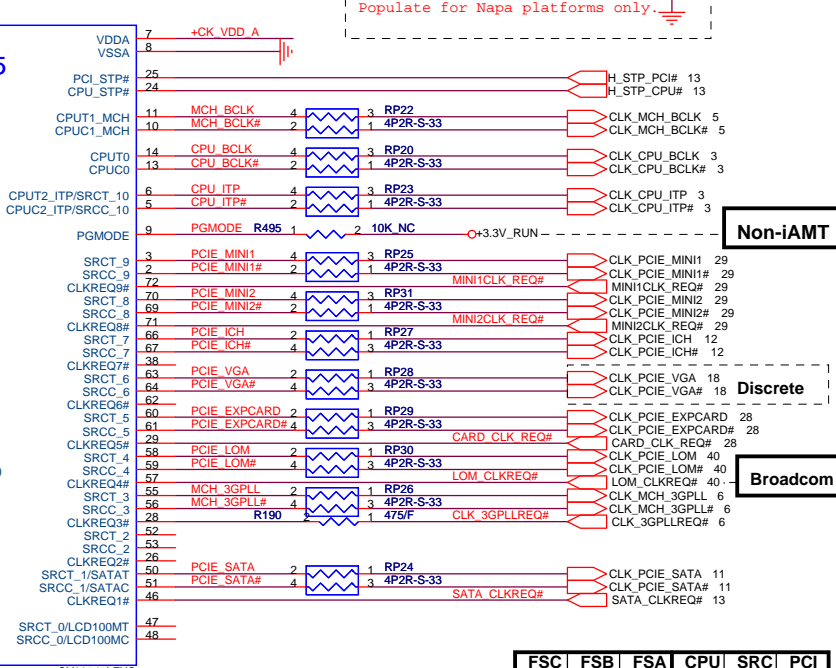
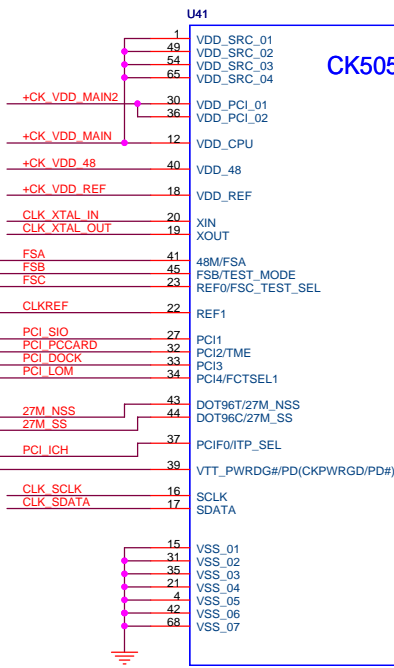
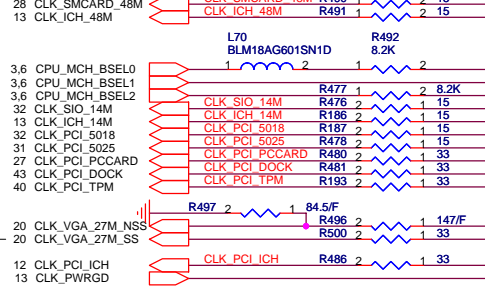


QUANTA COMPUTER
Title: DDR2 SO-DIMM (200P) X 2
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Change R496 to I47
ohm TBD and pop R497
84.5 ohm TBD pull
down on R496 pin2.
CLK_VGA_27M_NSS is
max 1.2V.



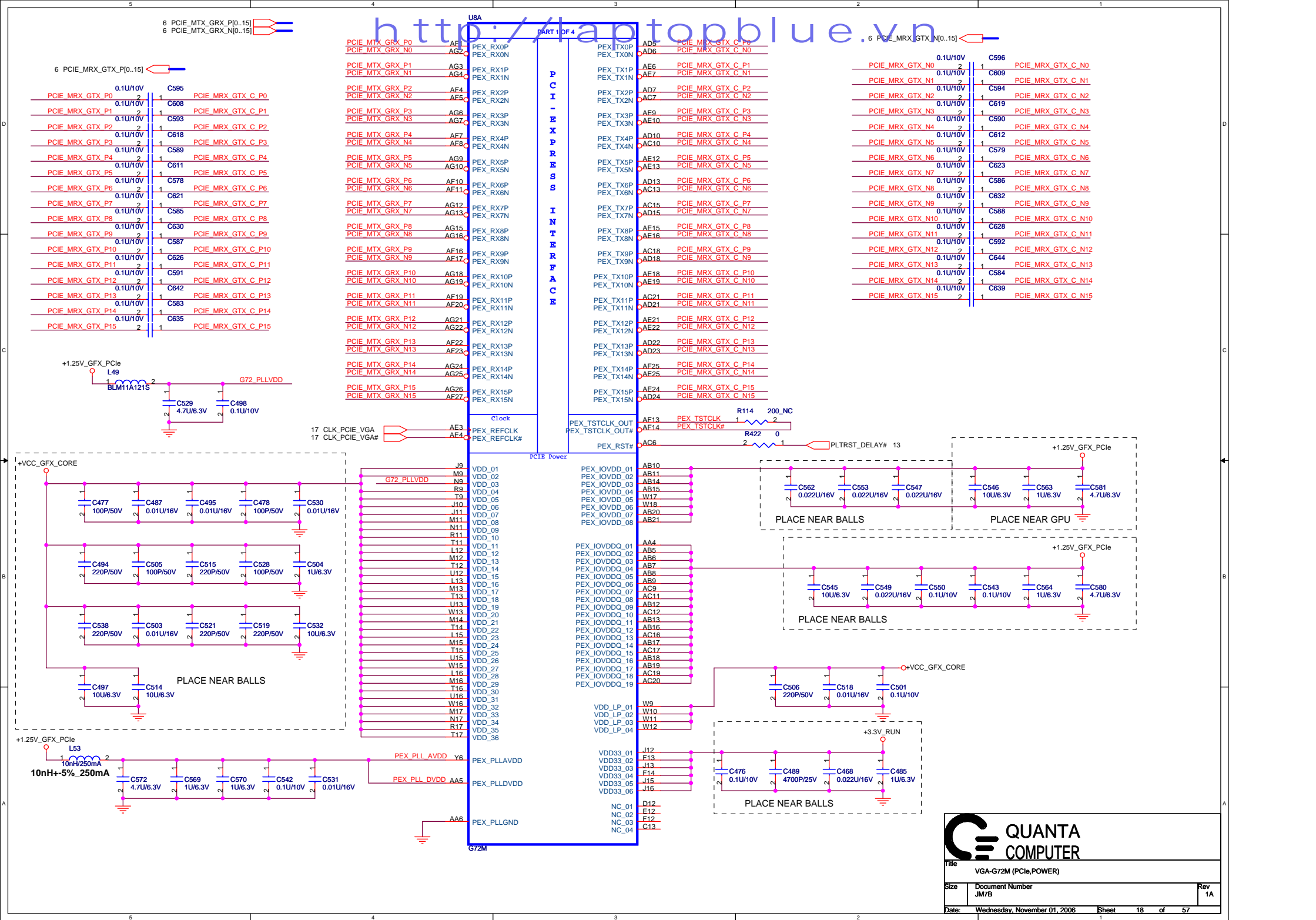
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

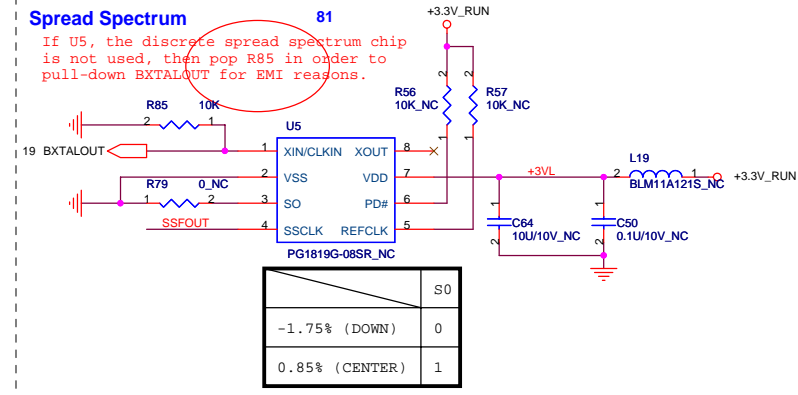
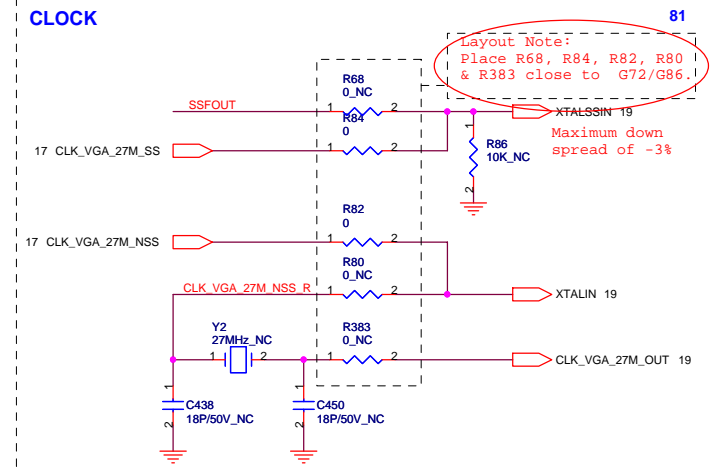
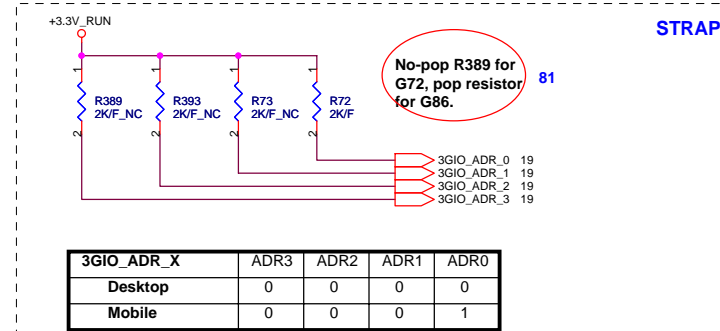
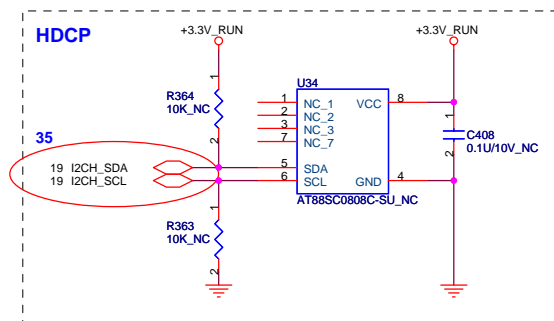
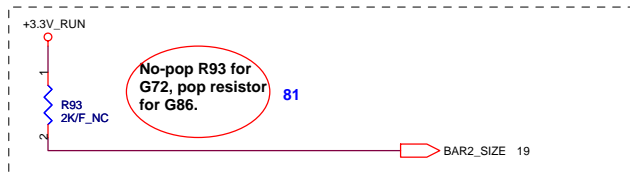
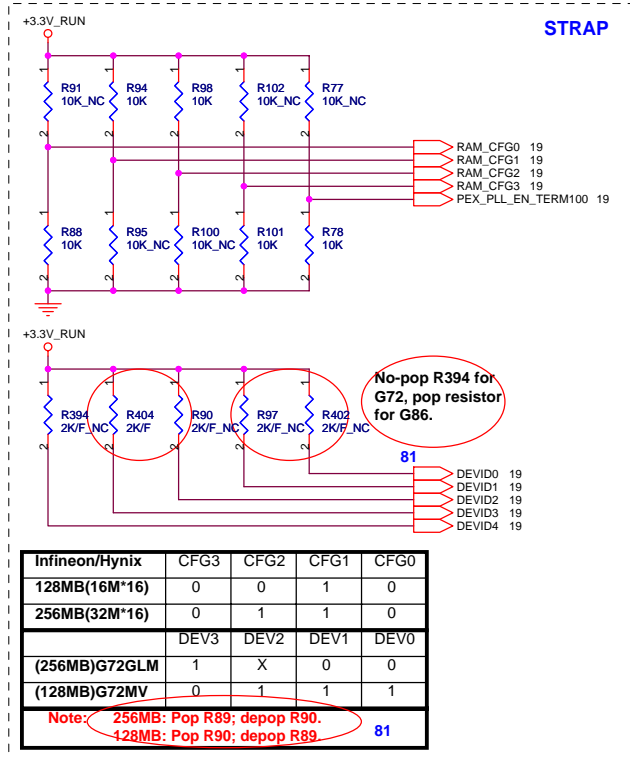
PCI_LOM = FCTSEL1

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRCT0	SRCC0

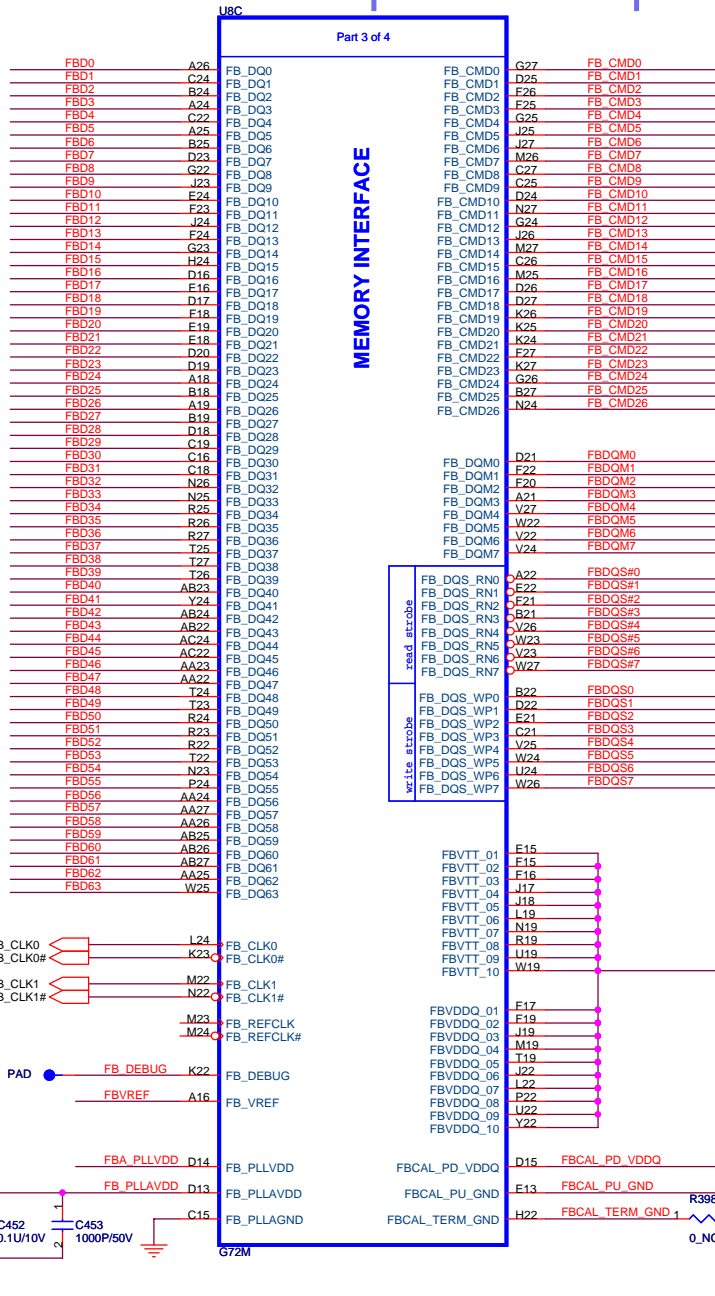


Title			
CLOCK GENERATOR			
Size	Document Number	Rev	
	JM7B	2C	
Date:	Wednesday, November 01, 2006	Sheet	17 of 57

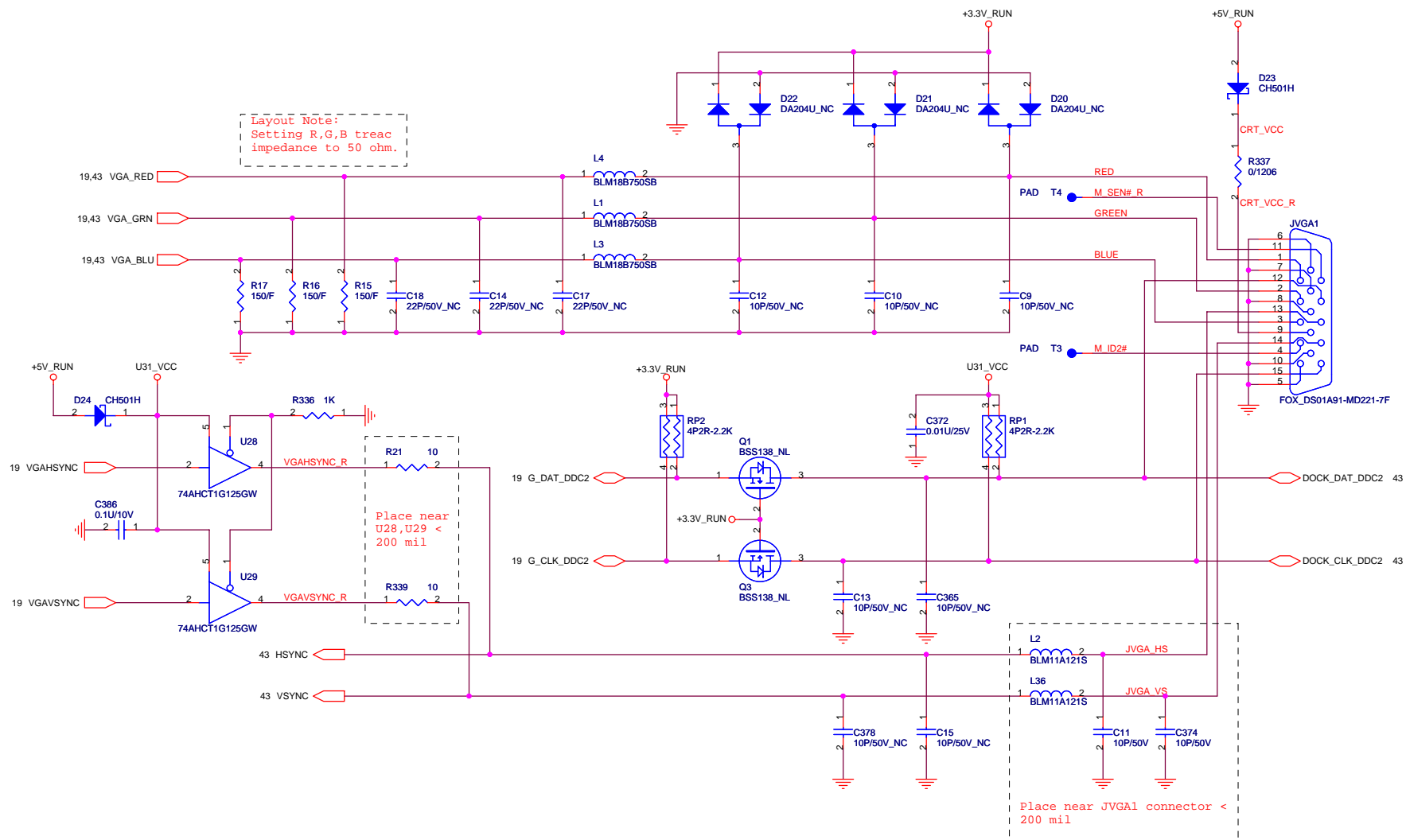




FB_CMD[0..26] 22
FBD[0..63] 22
FBDQM[0..7] 22
FBDQS[0..7] 22
FBDQS#0..7 22

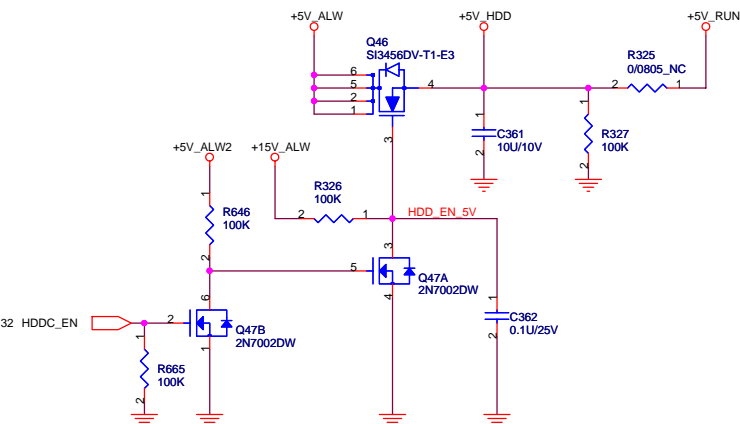
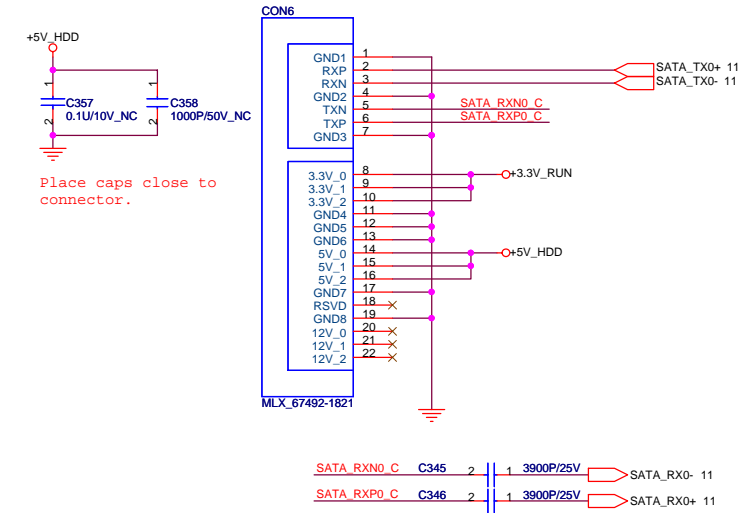




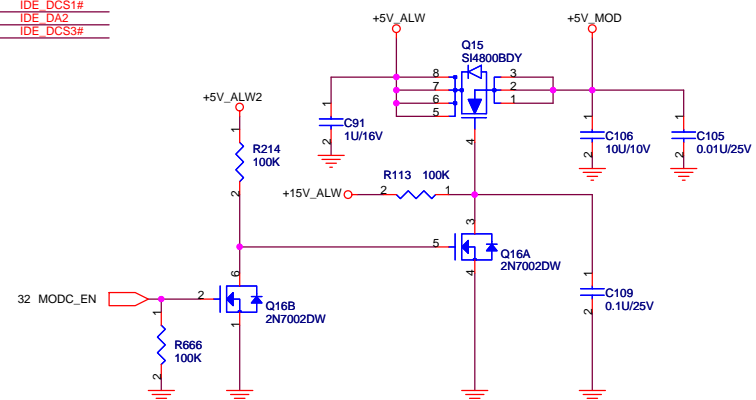
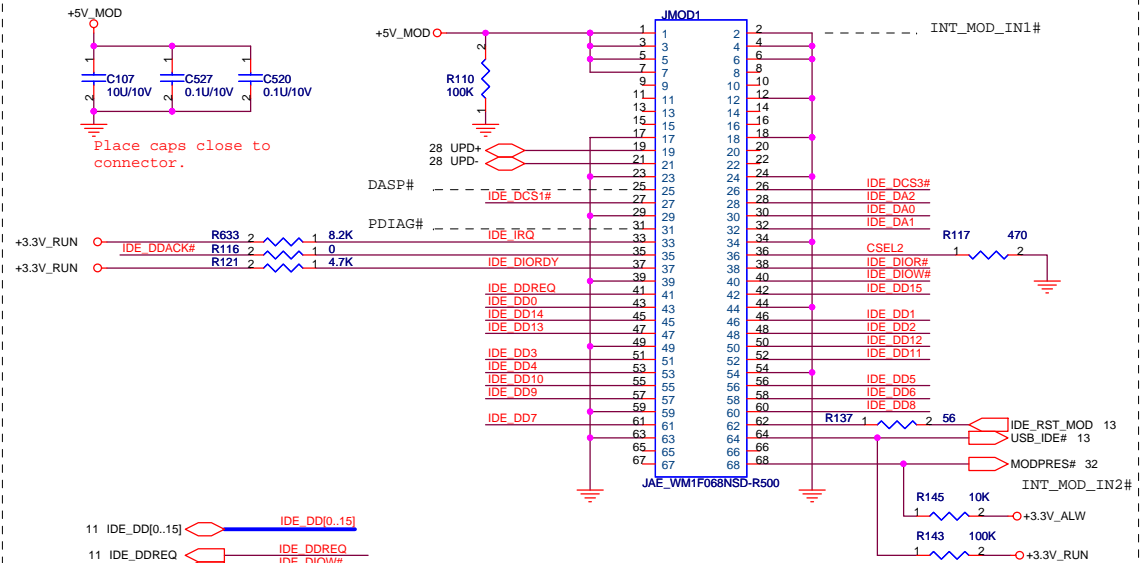


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SATA Connector.



ODD Connector.



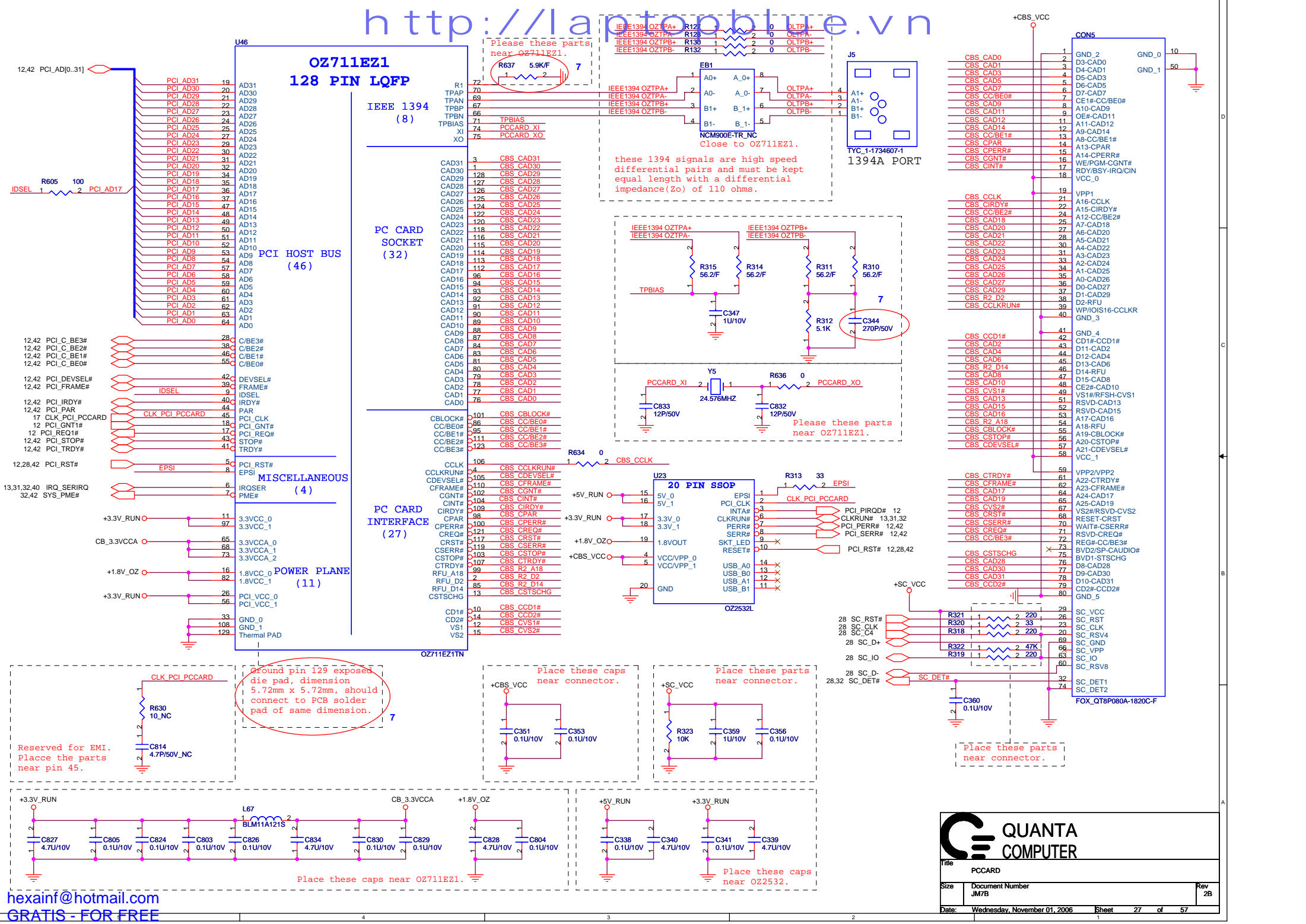
Title	SATA (HDD&CD_ROM)
-------	-------------------

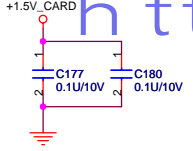
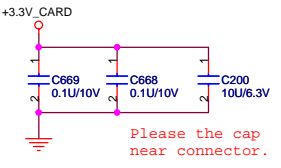
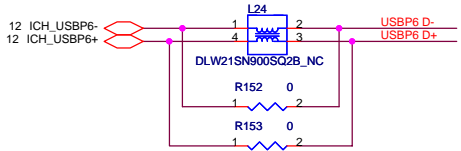
Size	Document Number JM7B
------	-------------------------

Rev
2C

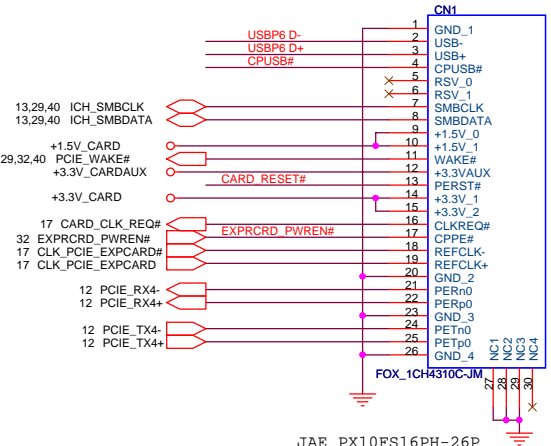
Date: Thursday, October 26, 2006

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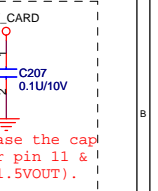
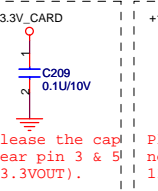
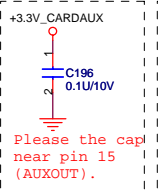
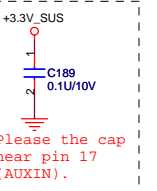
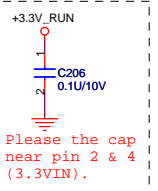
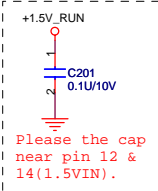
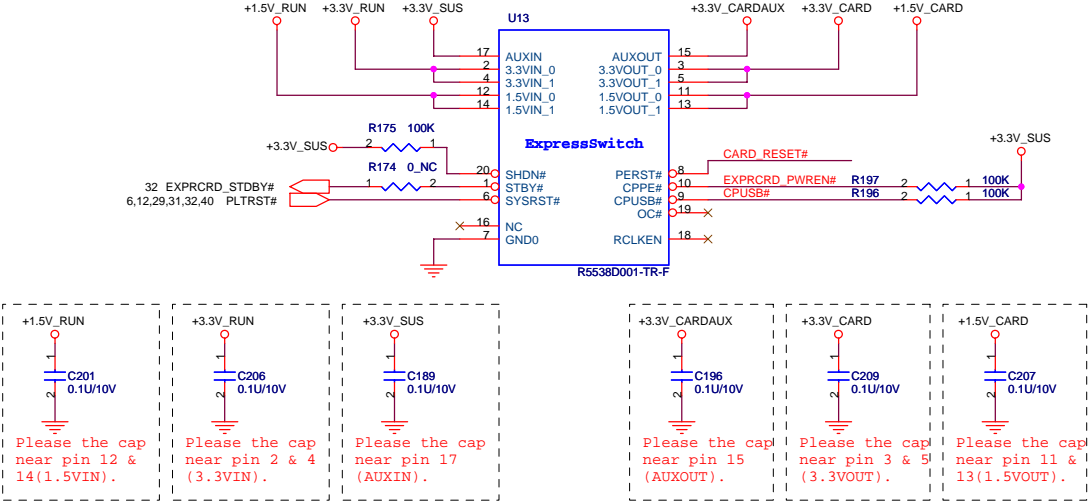




Please the cap near connector.

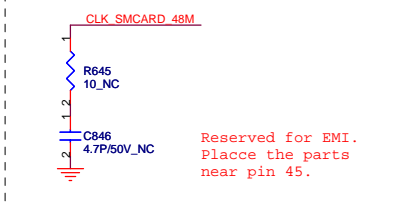
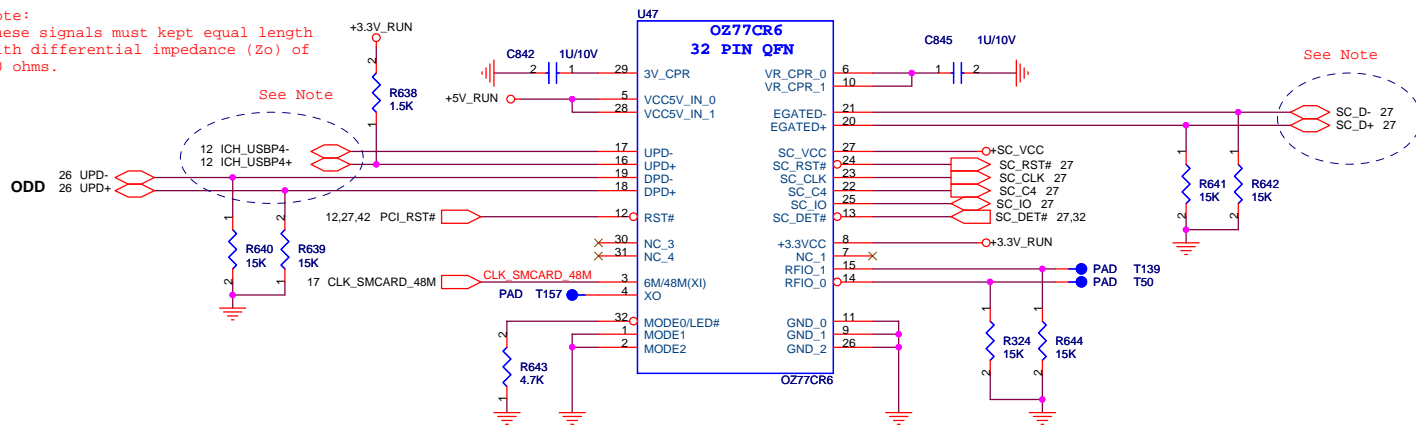


PCI-Express TX and RX direct to connector.

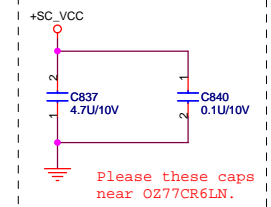
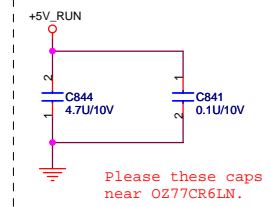
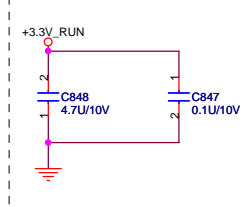



Smart Card

Note:
These signals must kept equal length with differential impedance (Z_0) of 90 ohms.



Reserved for EMI.
Place the parts near pin 45.

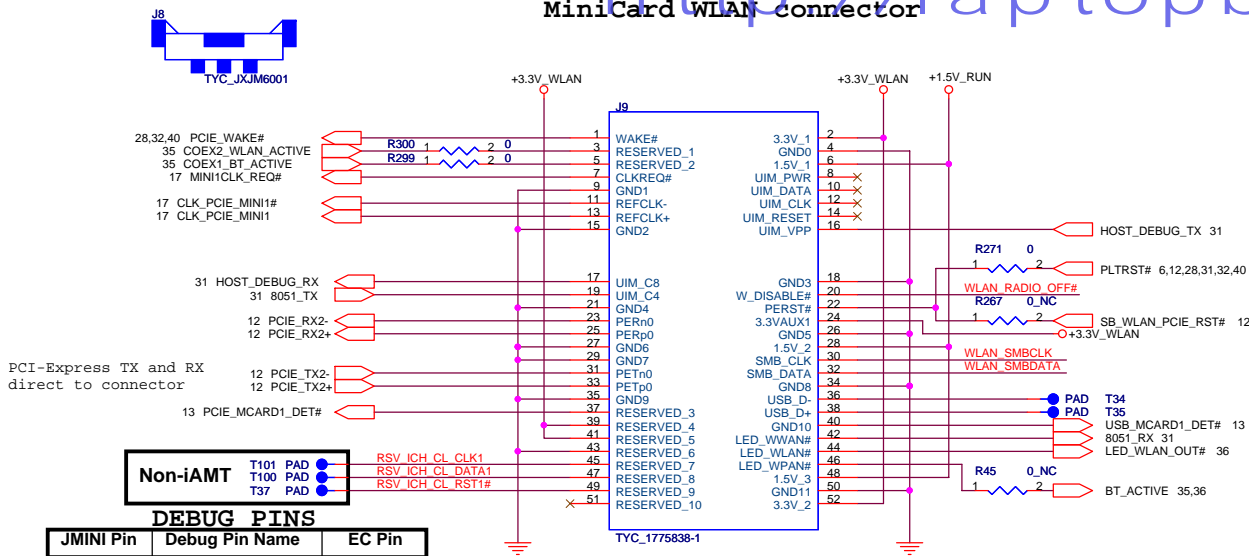




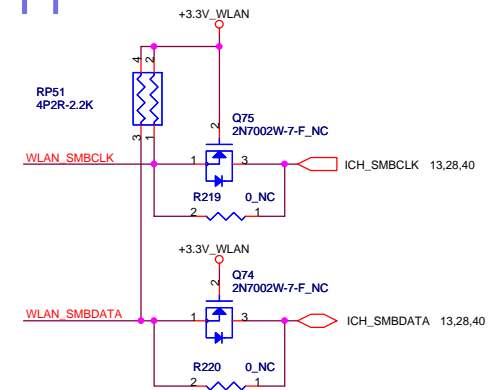
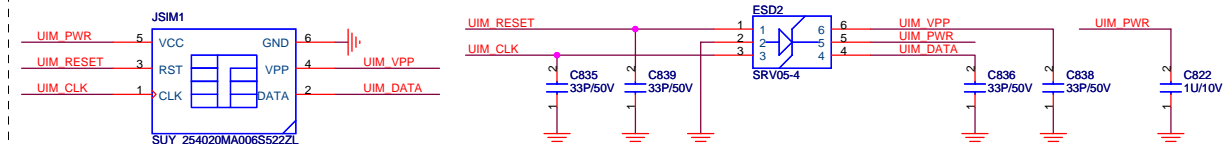
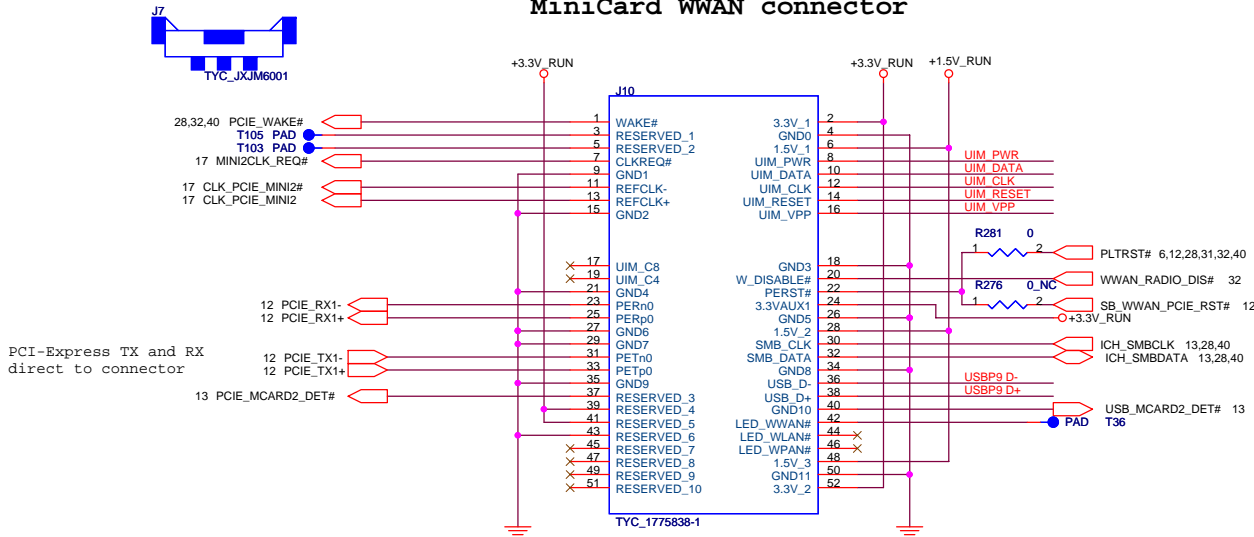
**QUANTA
COMPUTER**

Title ExpressCard/SmartCard		
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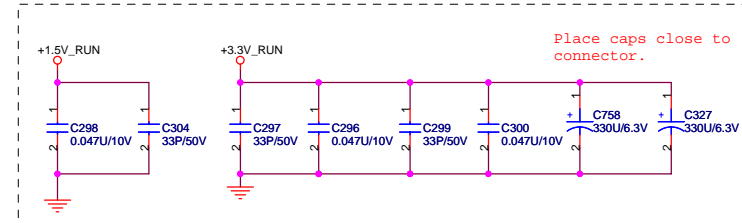
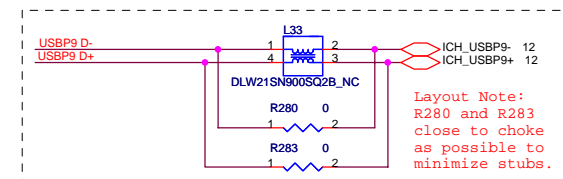
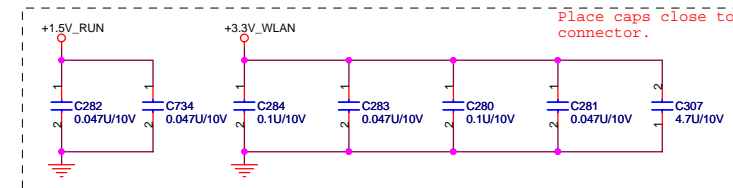
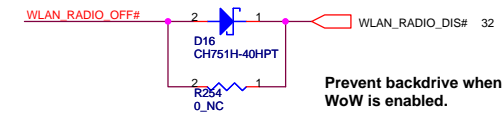
MiniCard WLAN connector



MiniCard WWAN connector



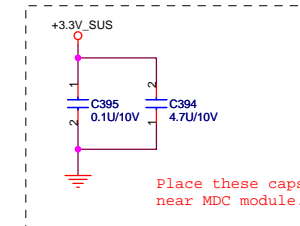
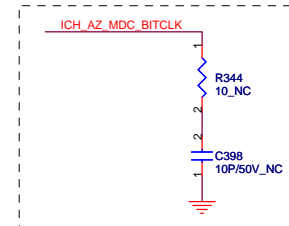
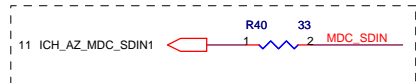
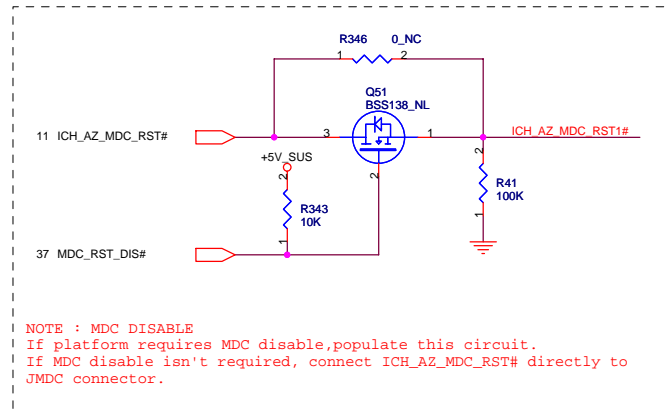
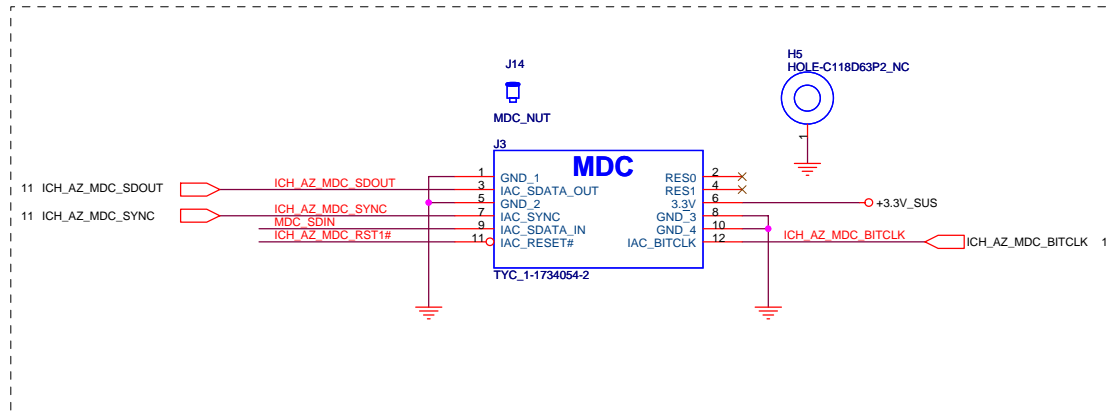
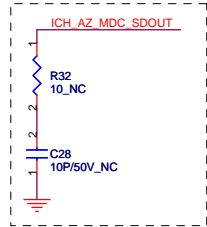
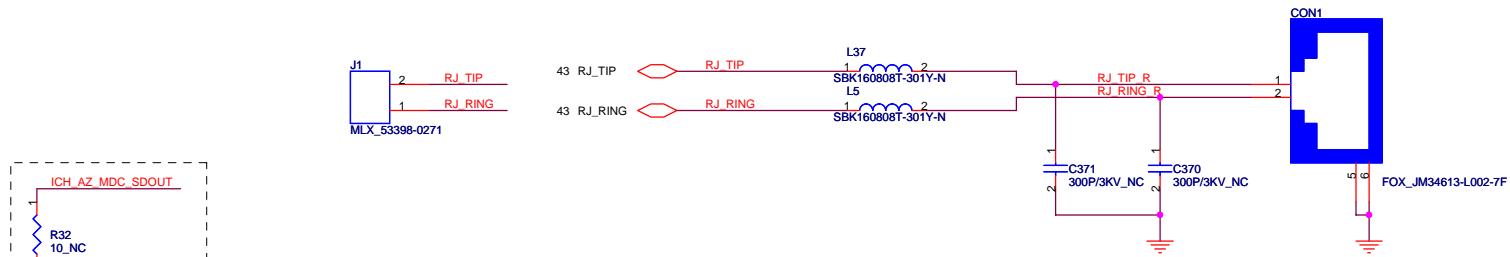
Support for WoW

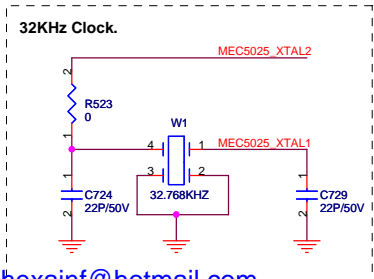
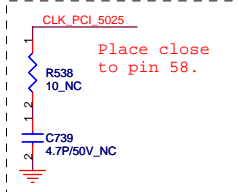
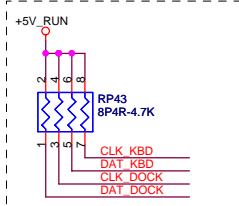
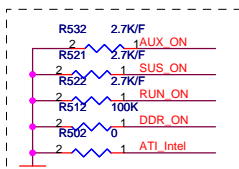


QUANTA COMPUTER	
Title: MINI-PCI	
Size: JM7B	Document Number: Rev 2C
Date: Thursday, October 26, 2006	Sheet: 29 of 57

Place as close as possible to JMINI connector

hexainf@hotmail.com
GRATIS - FOR FREE





Non-iAMT

Non-iAMT

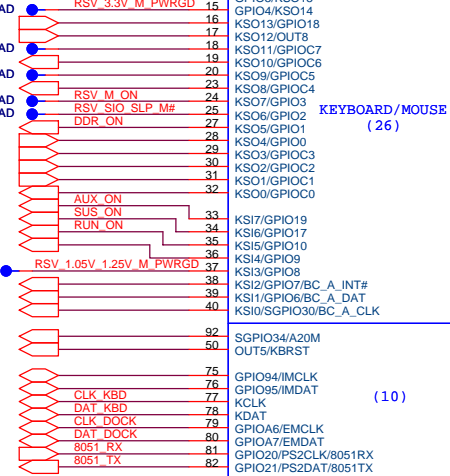
6,12,28,29,32,40 PLTRST#
17 CLK_PCI_5025
11,32,40 LPC_LFRAME#
11,32,40 LPC_LAD0
11,32,40 LPC_LAD1
11,32,40 LPC_LAD2
11,32,40 LPC_LAD3
13,27,32 CLKRUN#
13,27,32,40 IRQ_SERIRQ

12 ICH_EC_SPI_CLK
12 ICH_EC_SPI_DIN
12 ICH_EC_SPI_DO
34 EC_FLASH_SPI_CLK
34 EC_FLASH_SPI_DIN
34 EC_FLASH_SPI_DO
13 SIO_PWRBTN#
36 SNIFFER_YELLOW#
32 BC_CLK
32 BC_DAT
32 BC_INT#

+3.3V_ALW R662 1 2 100K
R527 10K
C235 4.7U/10V
L63 BLM11A121S
L64 BLM11A121S
C736 0.1U/10V
L34 BLM11A121S

32KHz Clock.
MEC5025_XTAL2
W1
MEC5025_XTAL1
C724 22P/50V
C729 22P/50V

MEC5025 EC-08 128 PIN VTQFP



PCI POWER/LPC BUS (9)
LRESET#
PCICLK
LFRAME#
LAD0
LAD1
LAD2
LAD3
CLKRUN#
SER_IRQ

HOST/8051 SPI (8)
HSTCLK
HSTDATAIN
HSTDATAOUT
FLCLK
FLDATAIN
FLDATAOUT
BC_CLK
BC_DAT
BC_INT#

CLOCK (3)
XTAL1
XTAL2
XSEL
VR_CAP
AGND
VCC_PLL
VSS_PLL

POWER PLANES (9)
VSS
VSS
VSS
VSS
VSS

POWER PLANES (6)

POWER_SW_IN2#/GPIO23
POWER_SW_IN1#/GPIO22
POWER_SW_IN0#
ACAV_IN

POWER SWITCH (6)

AB1B_CLK/GPIOA4
AB1B_DATA/GPIOA2
AB1A_CLK
AB1A_DATA

ACCESS BUS (4)

GPIO11/AB2_DATA
GPIO12/AB2_CLK
GPIO13/AB1G_DATA
GPIO14/AB1G_CLK
GPIO8/AB1C_CLK
GPIO85/AB1D_DATA
GPIO84/AB1D_CLK
GPIO93/AB1F_DATA
GPIO92/AB1F_CLK
GPIO91/AB1E_DATA
GPIO90/AB1E_CLK

GPIO (36)

OUT2/PWM3
OUT9/PWM2
OUT11/PWM1
OUT10/PWM0
nEC_SCI/SPDIN2
SGPIO45/MSDATA/SPDOUT2
SGPIO44/MSCLK/SPCLK2
SGPIO46/SPDIN1
SGPIO47/SPDOUT1
SGPIO31/TIN1/SPCLK1

MISCELLANEOUS (8)

SYSOPT0/SGPIO32/LPC_TX
SYSOPT1/SGPIO33/LPC_RX
SGPIO40
SGPIO41
SGPIO42
SGPIO43
SGPIO35
SGPIO36 (SFPI_EN)
SGPIO37
GPIO86/TOUT1
OUT7/nSMI

POWER PLANES (9)

VSS
VSS
VSS
VSS
VSS

MEC5025
LQFP128-16X16-4-FX2
Rev 0.01 (11/09/05)

POWER PLANES (6)

POWER_SW_IN2#/GPIO23
POWER_SW_IN1#/GPIO22
POWER_SW_IN0#
ACAV_IN

POWER SWITCH (6)

AB1B_CLK/GPIOA4
AB1B_DATA/GPIOA2
AB1A_CLK
AB1A_DATA

ACCESS BUS (4)

GPIO11/AB2_DATA
GPIO12/AB2_CLK
GPIO13/AB1G_DATA
GPIO14/AB1G_CLK
GPIO8/AB1C_CLK
GPIO85/AB1D_DATA
GPIO84/AB1D_CLK
GPIO93/AB1F_DATA
GPIO92/AB1F_CLK
GPIO91/AB1E_DATA
GPIO90/AB1E_CLK

GPIO (36)

OUT2/PWM3
OUT9/PWM2
OUT11/PWM1
OUT10/PWM0
nEC_SCI/SPDIN2
SGPIO45/MSDATA/SPDOUT2
SGPIO44/MSCLK/SPCLK2
SGPIO46/SPDIN1
SGPIO47/SPDOUT1
SGPIO31/TIN1/SPCLK1

MISCELLANEOUS (8)

SYSOPT0/SGPIO32/LPC_TX
SYSOPT1/SGPIO33/LPC_RX
SGPIO40
SGPIO41
SGPIO42
SGPIO43
SGPIO35
SGPIO36 (SFPI_EN)
SGPIO37
GPIO86/TOUT1
OUT7/nSMI

POWER PLANES (9)

VSS
VSS
VSS
VSS
VSS

MEC5025
LQFP128-16X16-4-FX2
Rev 0.01 (11/09/05)

POWER PLANES (6)

POWER_SW_IN2#/GPIO23
POWER_SW_IN1#/GPIO22
POWER_SW_IN0#
ACAV_IN

POWER SWITCH (6)

AB1B_CLK/GPIOA4
AB1B_DATA/GPIOA2
AB1A_CLK
AB1A_DATA

ACCESS BUS (4)

GPIO11/AB2_DATA
GPIO12/AB2_CLK
GPIO13/AB1G_DATA
GPIO14/AB1G_CLK
GPIO8/AB1C_CLK
GPIO85/AB1D_DATA
GPIO84/AB1D_CLK
GPIO93/AB1F_DATA
GPIO92/AB1F_CLK
GPIO91/AB1E_DATA
GPIO90/AB1E_CLK

GPIO (36)

OUT2/PWM3
OUT9/PWM2
OUT11/PWM1
OUT10/PWM0
nEC_SCI/SPDIN2
SGPIO45/MSDATA/SPDOUT2
SGPIO44/MSCLK/SPCLK2
SGPIO46/SPDIN1
SGPIO47/SPDOUT1
SGPIO31/TIN1/SPCLK1

MISCELLANEOUS (8)

SYSOPT0/SGPIO32/LPC_TX
SYSOPT1/SGPIO33/LPC_RX
SGPIO40
SGPIO41
SGPIO42
SGPIO43
SGPIO35
SGPIO36 (SFPI_EN)
SGPIO37
GPIO86/TOUT1
OUT7/nSMI

POWER PLANES (9)

VSS
VSS
VSS
VSS
VSS

MEC5025
LQFP128-16X16-4-FX2
Rev 0.01 (11/09/05)

POWER PLANES (6)

POWER_SW_IN2#/GPIO23
POWER_SW_IN1#/GPIO22
POWER_SW_IN0#
ACAV_IN

POWER SWITCH (6)

AB1B_CLK/GPIOA4
AB1B_DATA/GPIOA2
AB1A_CLK
AB1A_DATA

ACCESS BUS (4)

GPIO11/AB2_DATA
GPIO12/AB2_CLK
GPIO13/AB1G_DATA
GPIO14/AB1G_CLK
GPIO8/AB1C_CLK
GPIO85/AB1D_DATA
GPIO84/AB1D_CLK
GPIO93/AB1F_DATA
GPIO92/AB1F_CLK
GPIO91/AB1E_DATA
GPIO90/AB1E_CLK

GPIO (36)

OUT2/PWM3
OUT9/PWM2
OUT11/PWM1
OUT10/PWM0
nEC_SCI/SPDIN2
SGPIO45/MSDATA/SPDOUT2
SGPIO44/MSCLK/SPCLK2
SGPIO46/SPDIN1
SGPIO47/SPDOUT1
SGPIO31/TIN1/SPCLK1

MISCELLANEOUS (8)

SYSOPT0/SGPIO32/LPC_TX
SYSOPT1/SGPIO33/LPC_RX
SGPIO40
SGPIO41
SGPIO42
SGPIO43
SGPIO35
SGPIO36 (SFPI_EN)
SGPIO37
GPIO86/TOUT1
OUT7/nSMI

POWER PLANES (9)

VSS
VSS
VSS
VSS
VSS

MEC5025
LQFP128-16X16-4-FX2
Rev 0.01 (11/09/05)

Place cap close to pin 121.

Place these caps close to MEC5025.

1 = Enabled.
0 = Disabled.

Flash Recovery.

Low = Write Protected.

Flash Write Protect bottom 4K of internal bootblock flash.

Populate for flash corruption issue.

DEBUG Serial Port
Flash Recovery Port.

Flash Write Protect bottom 4K of internal bootblock flash.

Flash Write Protect bottom 4K of internal bootblock flash.

Flash Write Protect bottom 4K of internal bootblock flash.

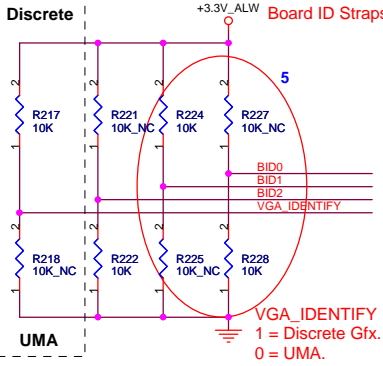
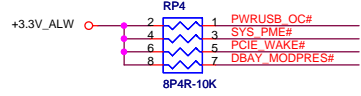
Flash Write Protect bottom 4K of internal bootblock flash.

Flash Write Protect bottom 4K of internal bootblock flash.

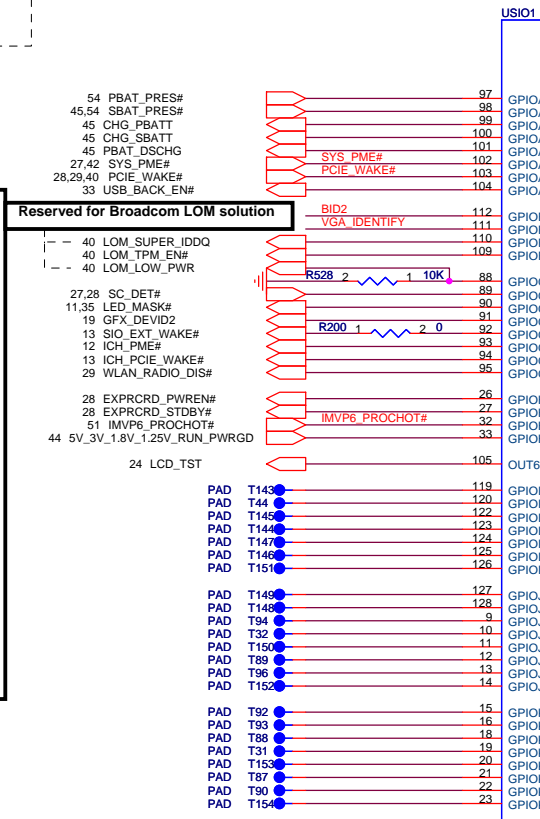
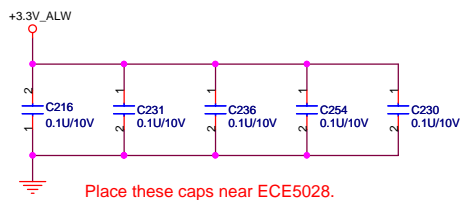
Flash Write Protect bottom 4K of internal bootblock flash.

Flash Write Protect bottom 4K of internal bootblock flash.

Flash Write Protect bottom 4K of internal bootblock flash.



BID2	BID1	BID0	JM7	JM7B
0	0	0	ENG1 (X00)	ENG1 (X00)
0	0	1	ENG2 (X01)	ENG2 (X01)
0	1	0	PT1.5W (X01W)	PT1.5W (X01W)
0	1	1	ENG2.5 (X02)	ENG2.5 (X02)
1	0	0	ST (X03)	ST (X03)
1	0	1	QT (X04)	QT (X04)
1	1	0	RAMP (A00)	RAMP (A00)



ECE5028 Midway 128 PIN VTQFP

PCI POWER
SIRQ (3)

LPC BUS
(8)

LPC DOCKING
(8)

BC
(3)

PARALLEL
PORT (17)

UART
(8)

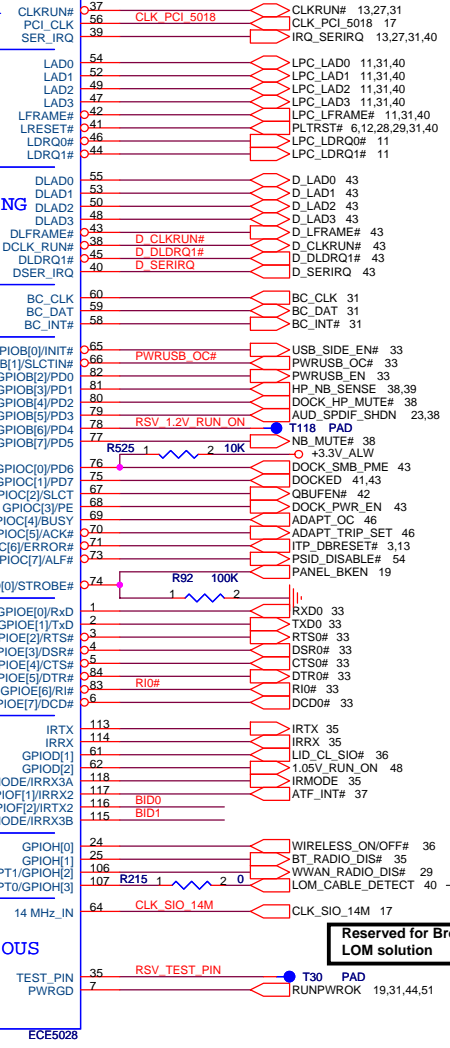
IRCC
(8)

SIO
RESET
(4)

MISCELLANEOUS
(3)

GPIO
(53)

POWER PLANES
(13)



Place closely pin USIO1.

DOCKING
PULLED UP

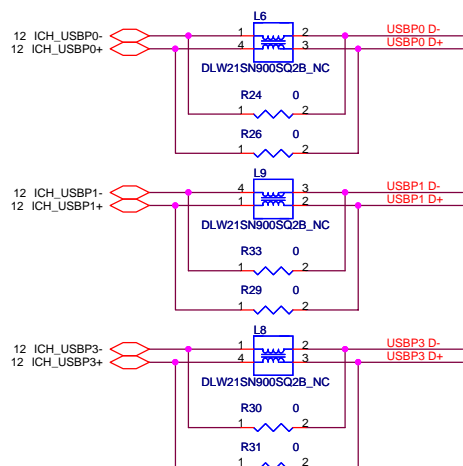
+3.3V_SUS

CLK_SIO_14M



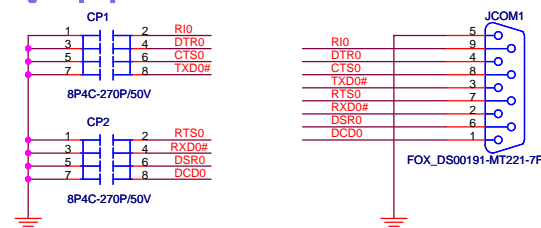
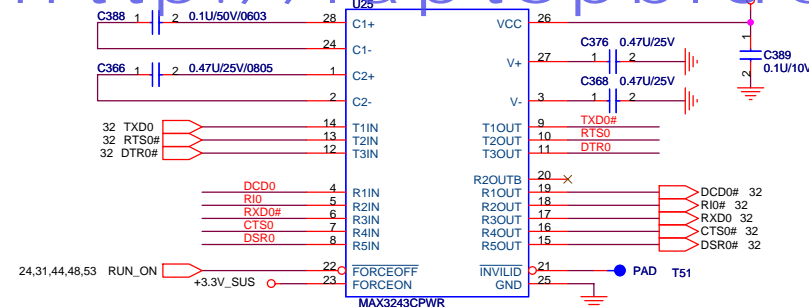
Title Ultra I/O Controller ECE5028		
Size	Document Number JM7B	Rev 2B
Date:	Wednesday, November 01, 2006	Sheet 32 of 57

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

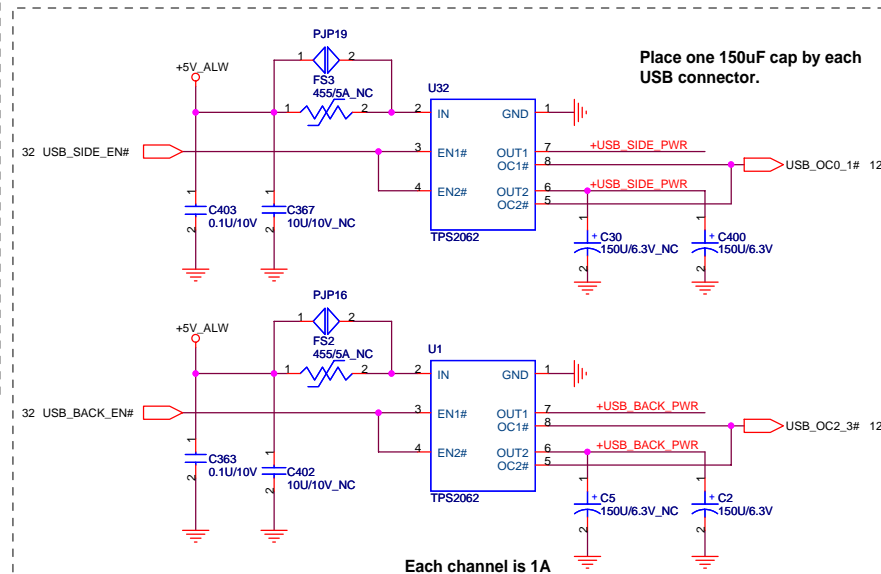


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

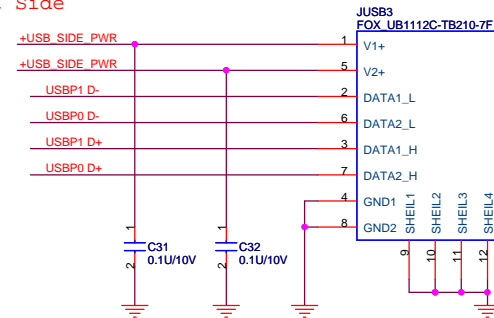
<http://laptopblue.vn>



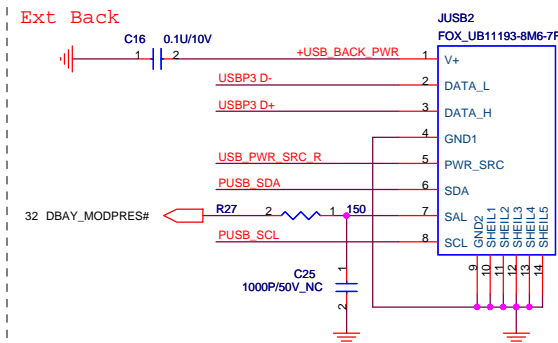
Place these beads close to JCOM1 as soon as possible
If MAX3243 pin 22 tied to RUN_ON, then it can not support Ring Out



Ext Side



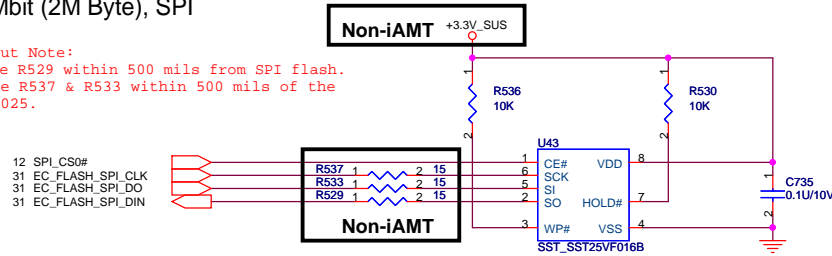
Ext Back



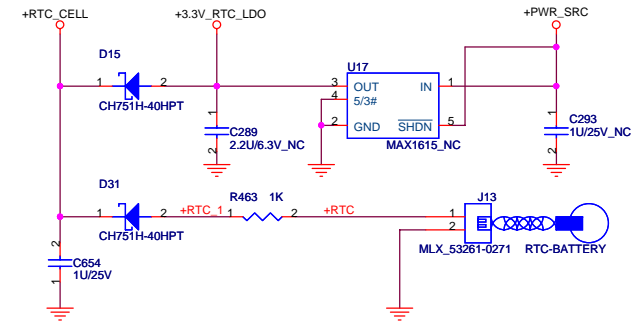
Title			SERIAL PORT & USB
Size	Document Number	Rev	
	JM7B	2C	
Date:	Thursday, October 26, 2006	Sheet	33 of 57

16Mbit (2M Byte), SPI

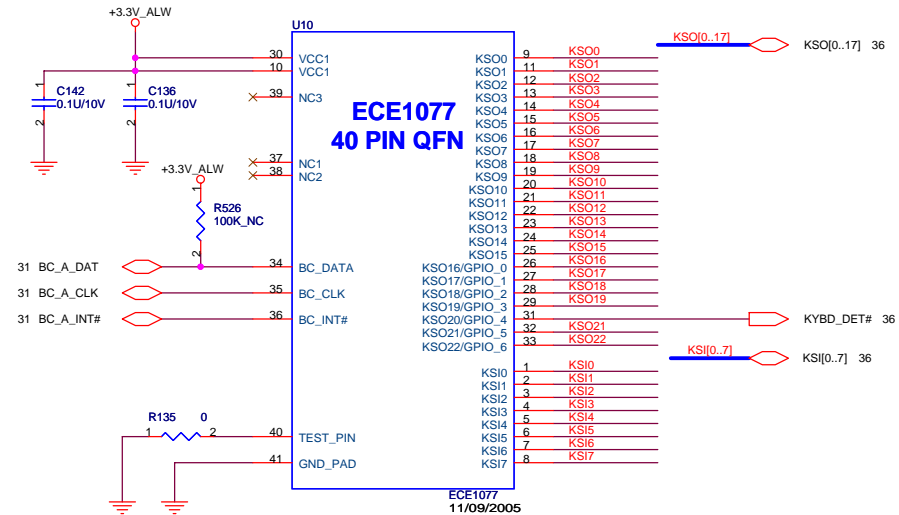
Layout Note:
Place R529 within 500 mils from SPI flash.
Place R537 & R533 within 500 mils of the
MEC5025.

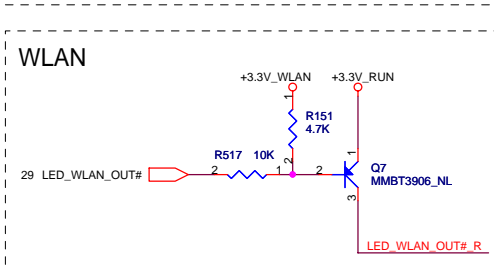
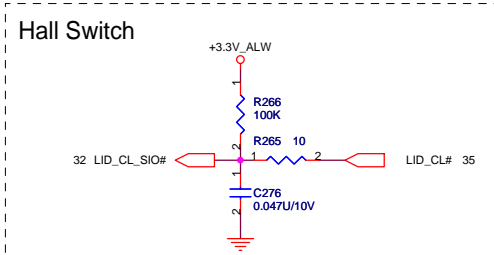
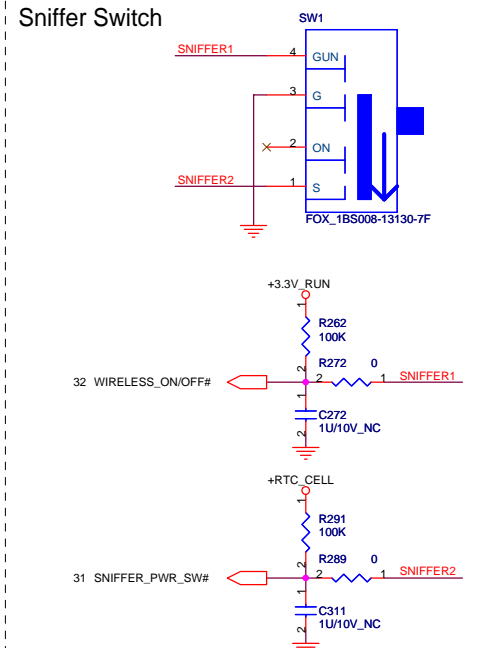
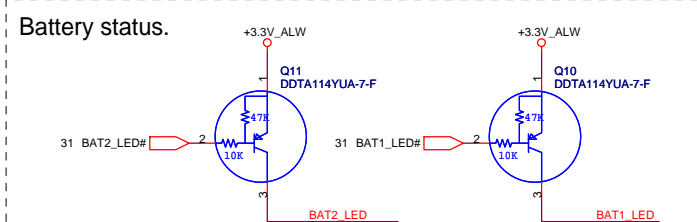
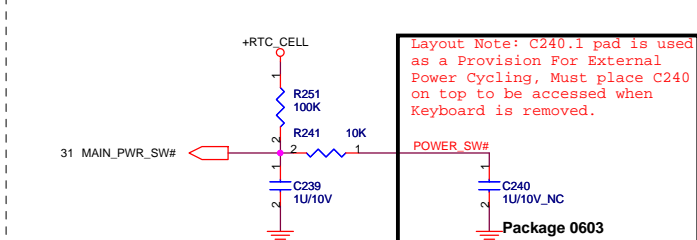
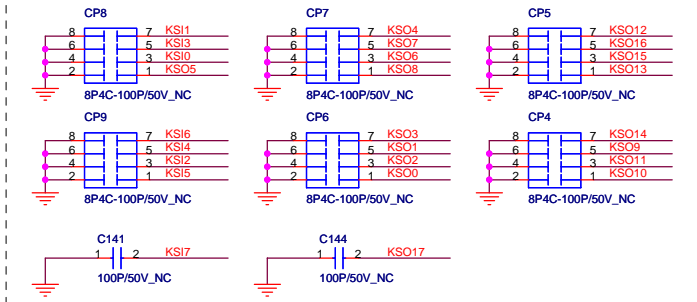
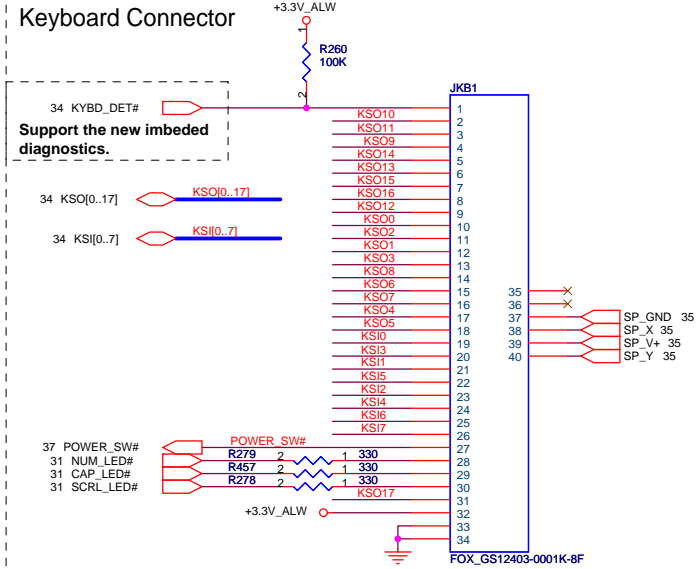
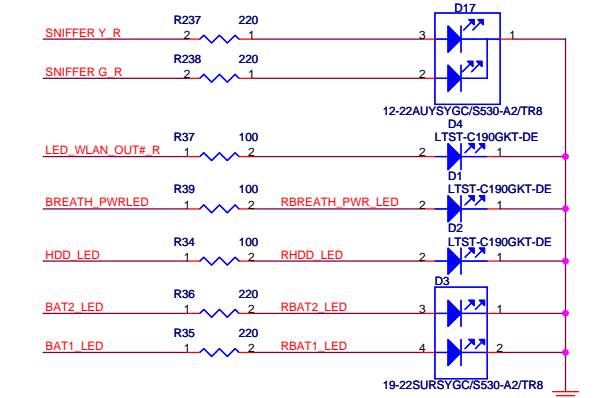
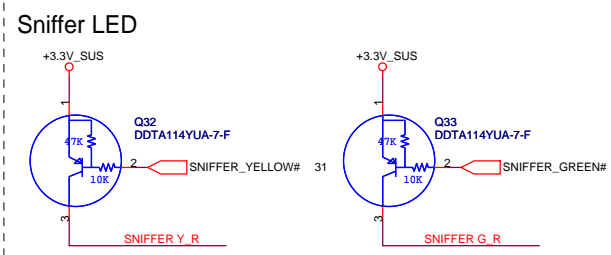
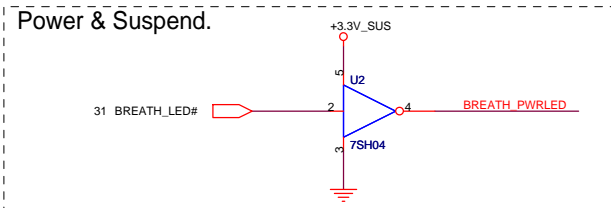
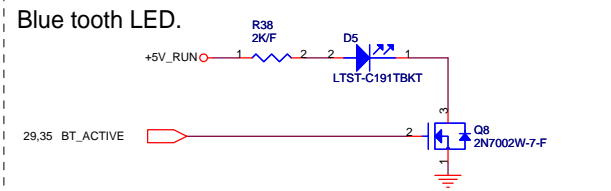
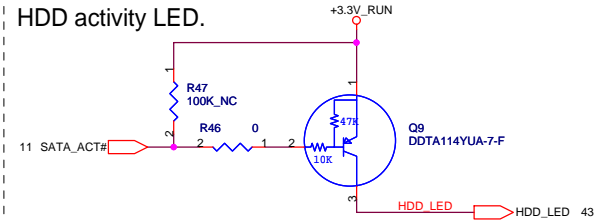


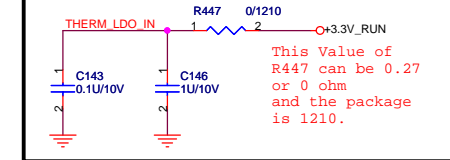
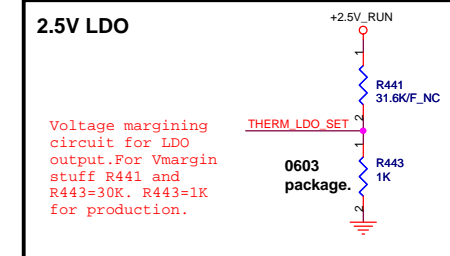
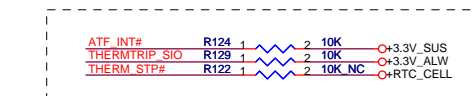
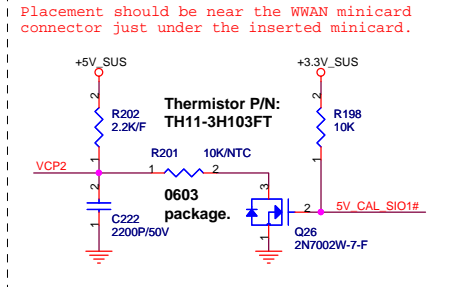
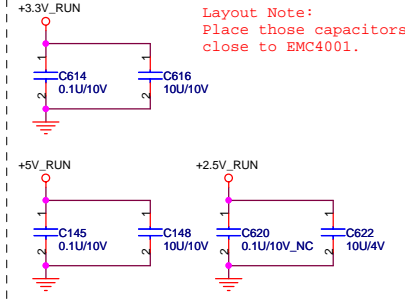
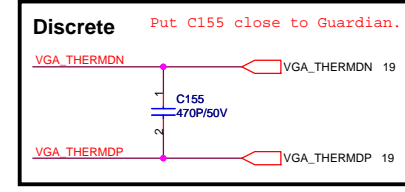
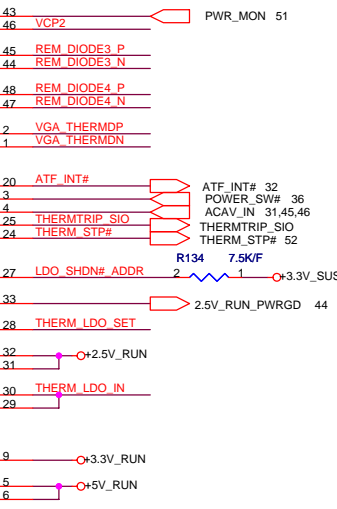
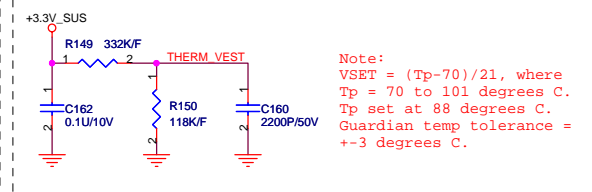
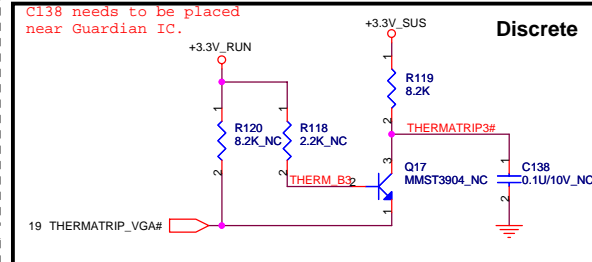
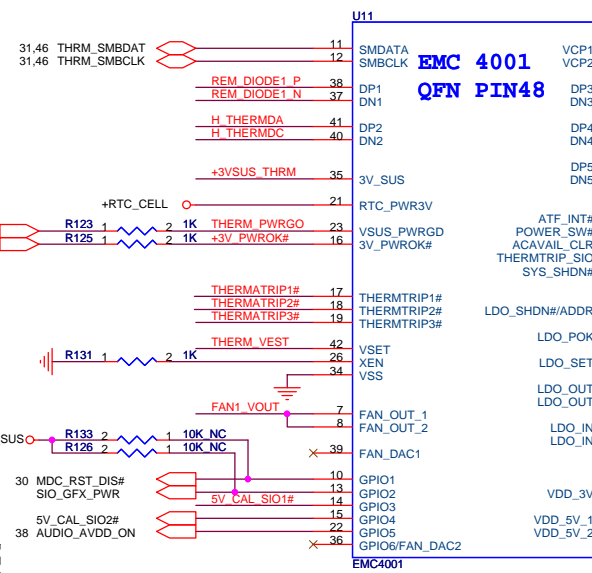
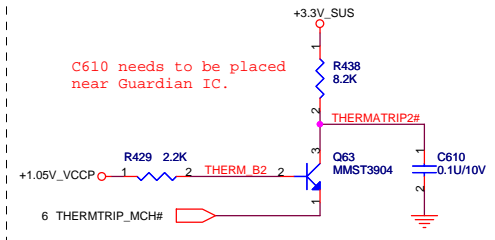
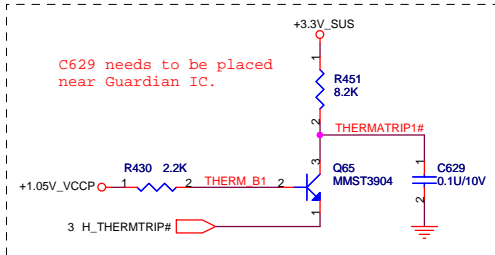
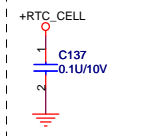
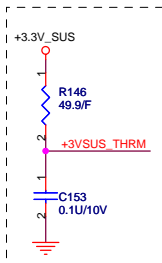
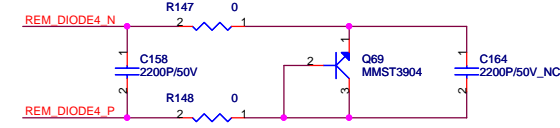
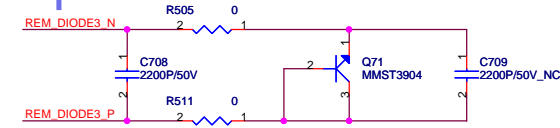
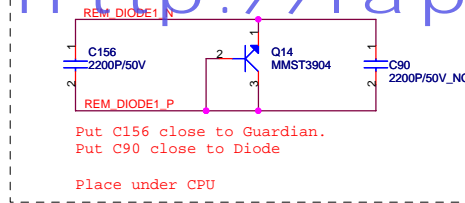
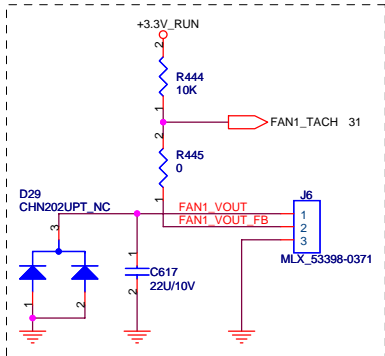
RTC BATTERY



Keyboard Scan Extension







Package 1206 For THD+N performance and Vista Logo requirements.

X7R

AUD LINE OUT L C334 1 2 0.033U/200V
AUD LINE OUT R C291 1 2 0.033U/200V
AUD HP OUT L C768 2 1 2.2U/25V
AUD HP OUT R C751 2 1 2.2U/25V

C753 47P/50V_NC
C764 47P/50V_NC
C288 47P/50V_NC
C323 47P/50V_NC

C308 1U/10V

T106 PAD

+5V_SPK_AMP

For TPA6040A, pop R551, depop R552.

AUDIO AVDD_ON 1 2
R551 0_NC
AUD AMP MUTE#

+5V_SPK_AMP

AUD_SPK_ENABLE#
AUD_EAPD
Q41 2N7002W-7-F
Q34 2N7002W-7-F

+5V_SPK_AMP

AUD AMP GAIN1
AUD AMP GAIN2

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

INTERNAL SPEAKER AMP

U20
MAX9789A
TQFN 32PIN

OUTL+ 6 AUD_SPK_L1
OUTL- 7 AUD_SPK_L2
OUTR+ 20 AUD_SPK_R1
OUTR- 19 AUD_SPK_R2
HPL 16 AUD_HP_JACK_L
HPR 15 AUD_HP_JACK_R
REGEN 4 REGEN
SET 1 SET
VOUT 29
VDD 30
PVDD_8 8
PVDD_18 18
GND_28 28
PGND_5 5
PGND_21 21

MAX9789A

AUDIO AVDD_ON
R557 0
REGEN
C763 0.033U/16V_NC

For TPA6040A, pop C763, depop R557.

C268 0.1U/10V
+3.3V_RUN
U16
AUD_HP_NB_SENSE 4
NB_MUTE# 32

AUD_SPK_R1
AUD_SPK_R2
AUD_SPK_L1
AUD_SPK_L2
C717 100P/50V
C718 100P/50V
C719 100P/50V
C720 100P/50V
JSPK1
MLX_53398-047

L35
FB_600ohm+-25%_100MHz
200mA_0.6ohm DC

VDD
C319 1U/10V
C292 1U/10V
C294 0.1U/10V
Layout Note: Place close U20.

Layout Note: Place close U20.

+5V_SPK_AMP
+5V_RUN
+5V_SPK_AMP

L31
BLM21PG600SN1D
C320 1U/10V_NC
C326 10U/10V_NC

Layout Note: Place close to pin 8.

FB_60ohm+-25%_100MHz
3A_0.05ohm DC

Layout Note: Place close to pin 18.

For TPA6040A, pop C332, depop R298.

SET
C322 0.033U/16V_NC
R298 0

AZALIA (HD) CODEC

U19
STAC9205
QFN 48PIN

11 ICH_AZ_CODEC_BITCLK
11 ICH_AZ_CODEC_SDI#
11 ICH_AZ_CODEC_SDO#
11 ICH_AZ_CODEC_SYNC
11 ICH_AZ_CODEC_RST#

For tuning.

R257 0
AUD_EAPD
SPDIF_OUT

+3.3V_RUN

C305 10U/10V_NC
C301 0.1U/10V
C302 1U/10V

+3.3V_RUN

C260 0.1U/10V

+VDDA

C258 0.1U/16V
C295 1U/10V
C261 10U/10V_NC

SENSE_A
SENSE_B
HDA_BITCLK
HDA_SDI_CODEC
HDA_SDO
HDA_SYNC
HDA_RST#

PORT_A_L
PORT_A_R
VREFOUT_A
PORT_B_L
PORT_B_R
VREFOUT_B
PORT_C_L
PORT_C_R
VREFOUT_C
PORT_D_L
PORT_D_R
PORT_E_L
PORT_E_R
PORT_F_L
PORT_F_R
VREFOUT_F
PORT_G_L
PORT_G_R
VREFOUT_G
PORT_H_L
PORT_H_R
VREFOUT_H
PORT_I_L
PORT_I_R
VREFOUT_I
PORT_J_L
PORT_J_R
VREFOUT_J
PORT_K_L
PORT_K_R
VREFOUT_K
PORT_L_L
PORT_L_R
VREFOUT_L
PORT_M_L
PORT_M_R
VREFOUT_M
PORT_N_L
PORT_N_R
VREFOUT_N
PORT_O_L
PORT_O_R
VREFOUT_O
PORT_P_L
PORT_P_R
VREFOUT_P
PORT_Q_L
PORT_Q_R
VREFOUT_Q
PORT_R_L
PORT_R_R
VREFOUT_R
PORT_S_L
PORT_S_R
VREFOUT_S
PORT_T_L
PORT_T_R
VREFOUT_T
PORT_U_L
PORT_U_R
VREFOUT_U
PORT_V_L
PORT_V_R
VREFOUT_V
PORT_W_L
PORT_W_R
VREFOUT_W
PORT_X_L
PORT_X_R
VREFOUT_X
PORT_Y_L
PORT_Y_R
VREFOUT_Y
PORT_Z_L
PORT_Z_R
VREFOUT_Z

DMIC_CLK
DMIC0/VOL-/GPIO1
DMIC1/VOL-/GPIO2
SPDIF_IN/EAPD/GPIO0
SPDIF_OUT

NC_43
NC_44
NC_45
DVDD_CORE_1
DVDD_CORE_9
DVDD_CORE_40
DVDD_IO
AVDD_25
AVDD_38
DVSS
AVSS_26
AVSS_42

CD_L
CD_GND
CD_R
PC_BEEP
MONO_OUT
VREFILT
CAP2

STAC9205X5NBEB1XR

AUD_SENSE_A
AUD_SENSE_B
AUD_HP_OUT_L
AUD_HP_OUT_R
AUD_EXT_MIC_L
AUD_EXT_MIC_R
AUD_INT_MIC_IN
AUD_LINE_OUT_L
AUD_LINE_OUT_R
DOCK_HP_MUTE#
AUD_SPDIF_SHDN

AC97VREFI
CAP2
C273 10U/6.3V
C287 10U/6.3V

Layout Note: Close to Pin 13.

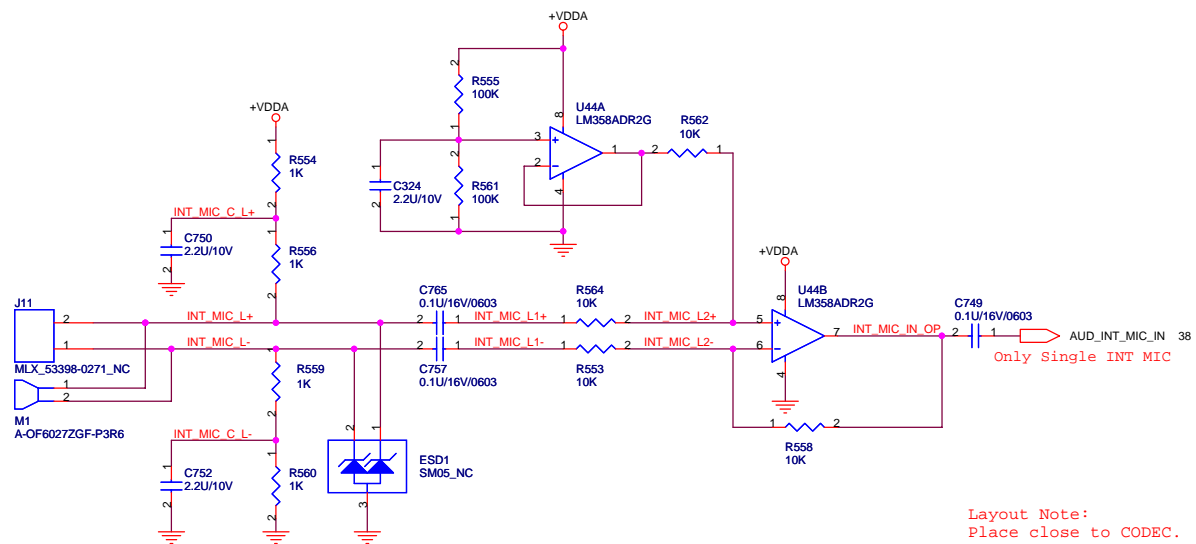
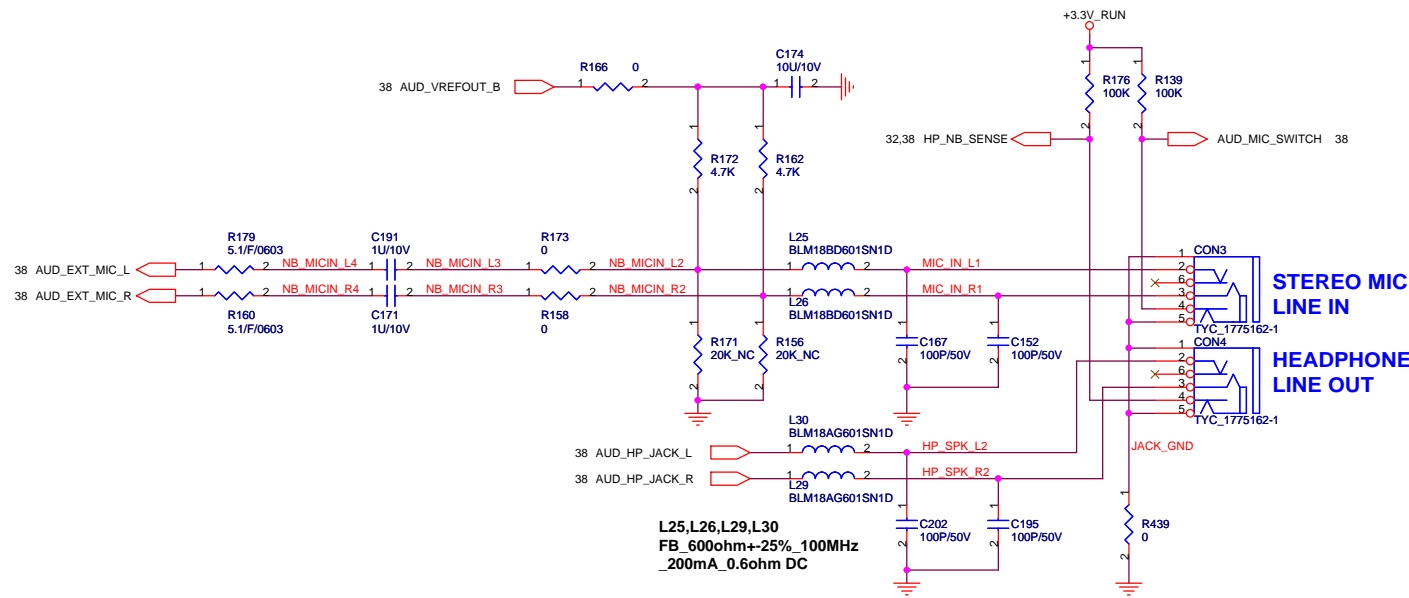
AUD_SENSE_A
R285 5.1K/F
R286 39.2K/F
R288 20K/F
C315 1000P/50V
HP_NB_SENSE
Q42 2N7002W-7-F
Q43 2N7002W-7-F
AUD_MIC_SWITCH

Close to U19.

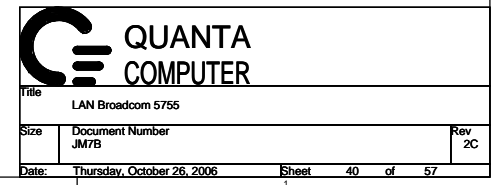
+VDDA
C278 0.1U/16V
AUD_PC_BEEP
C279 0.1U/10V
R261 20K
BEEP2
R264 10K_NC
U18 74LVC1G86GW
BEEP 31
SPKR 13



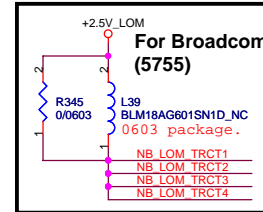
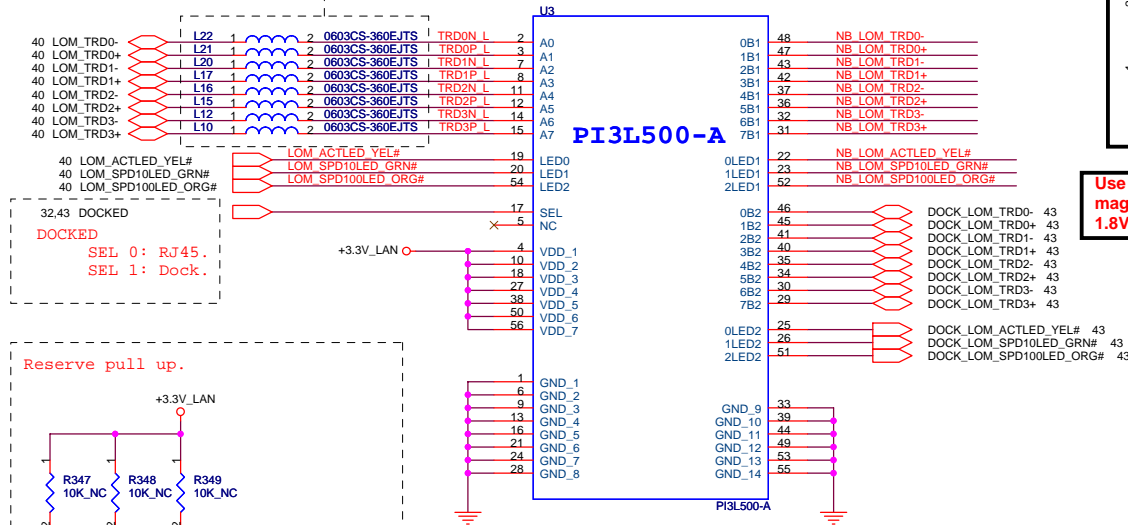
Title	Azalia CODEC
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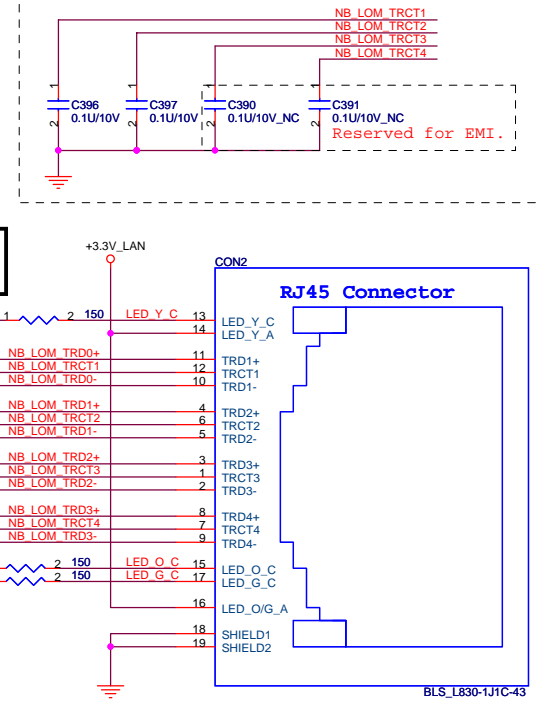
Title			AUDIO CONN
Size	Document Number	Rev	
	JM7B	2C	
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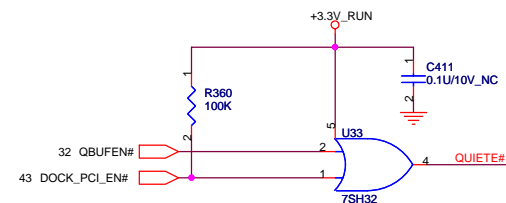


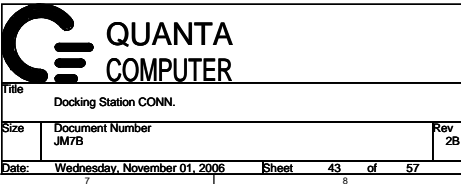
36nH is a suggested value.
Actual value will be system dependent.
Must use 0603 package for lower DC resistance.



Use 2.5V_LOM for center tap on magnetics when using Broadcom;
1.8V_LOM for Intel only







Non-iAMT

48 1.25V_RUN_PWRGD



R373

Discrete

50 GFX_CORE_PWRGD



R159

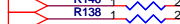
49 1.5V_RUN_PWRGD

48 1.05V_RUN_PWRGD

37 2.5V_RUN_PWRGD



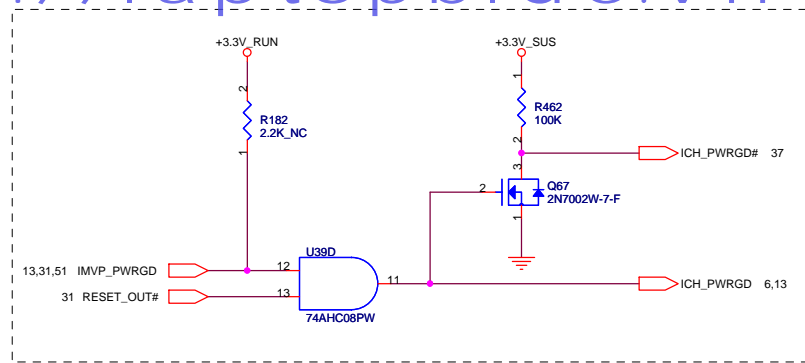
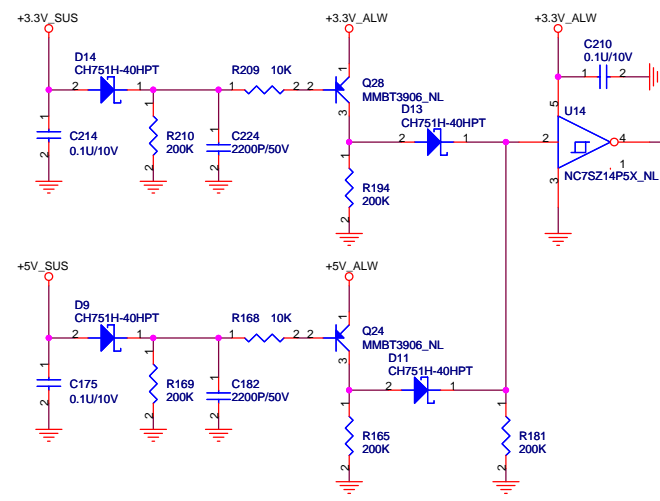
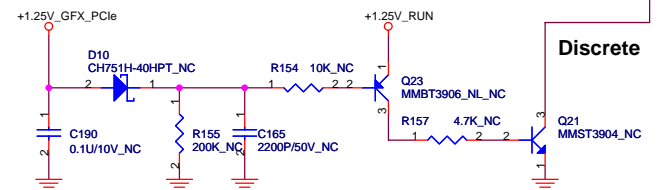
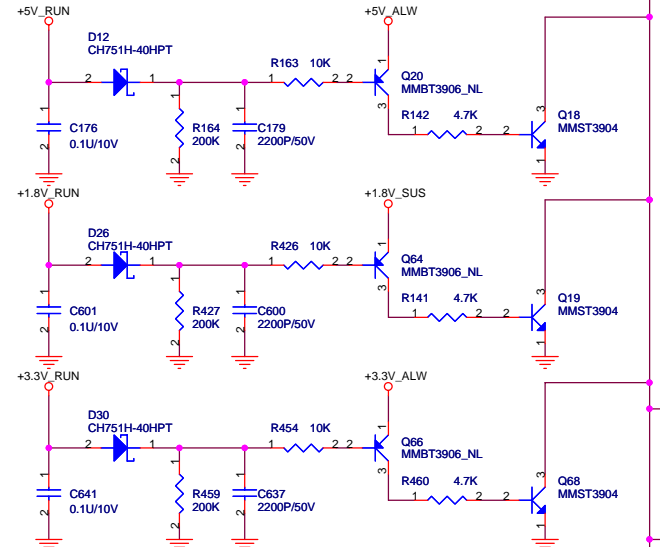
R144



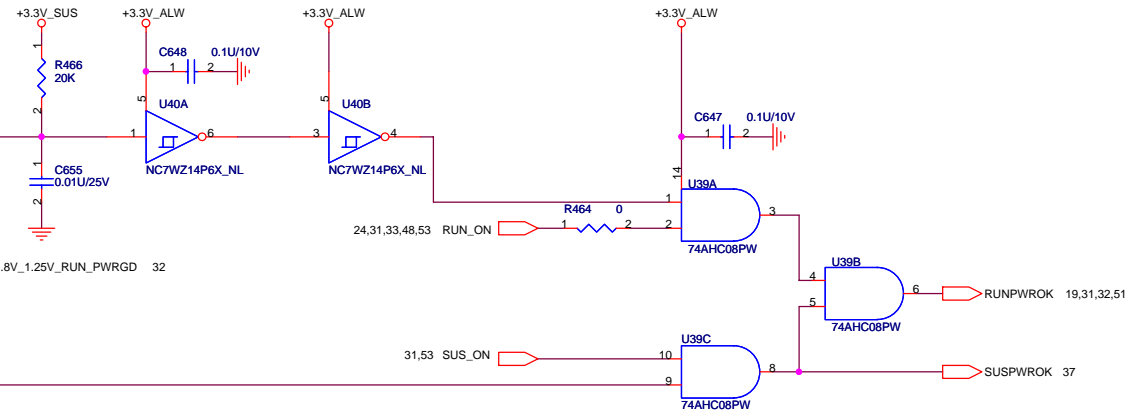
R140



R138



Keep Away from high speed buses



Title

System Reset Circuit

Size

Document Number

JM7B

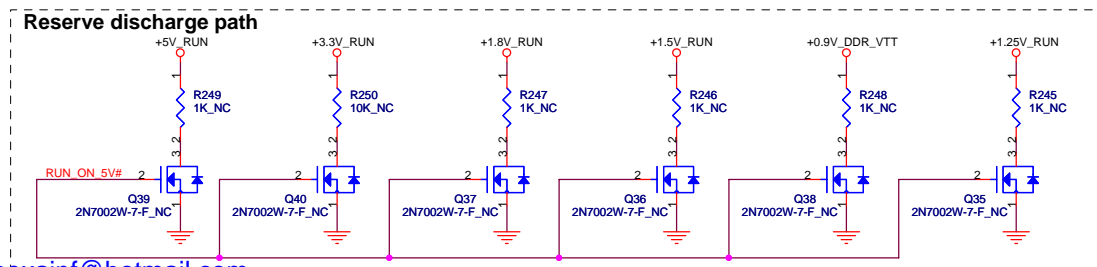
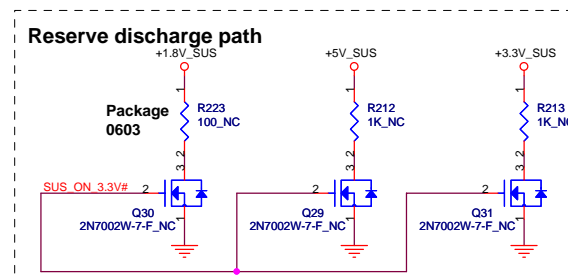
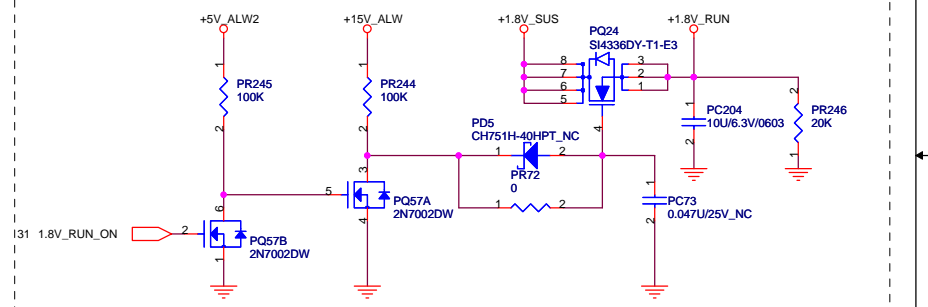
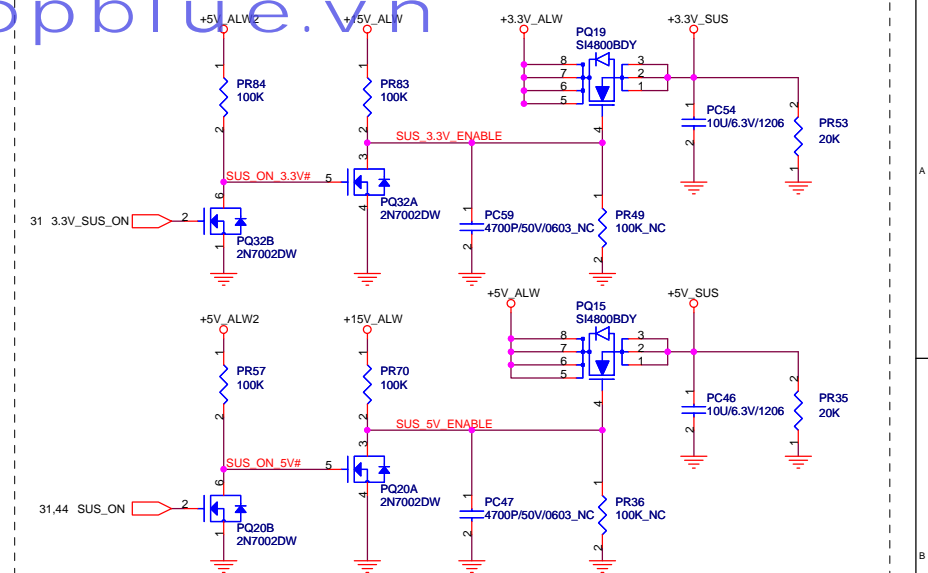
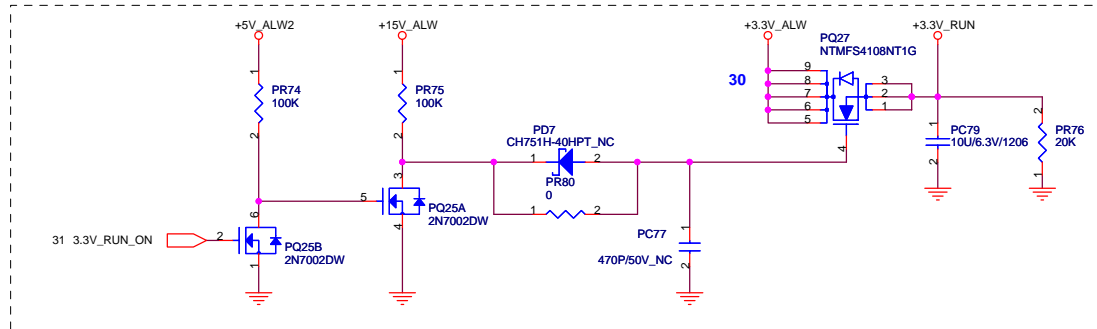
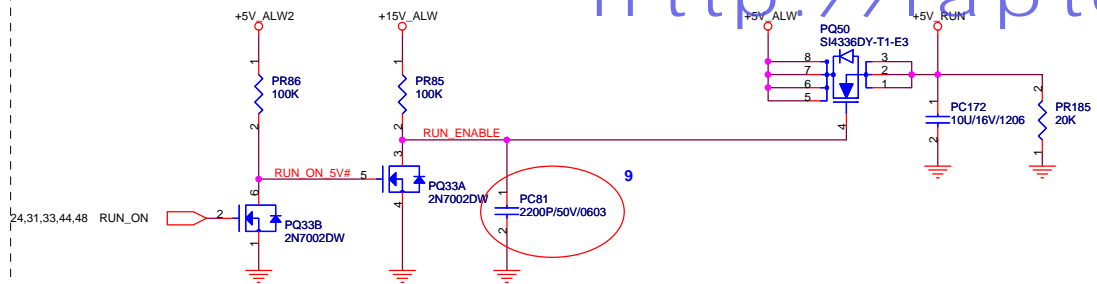
Rev

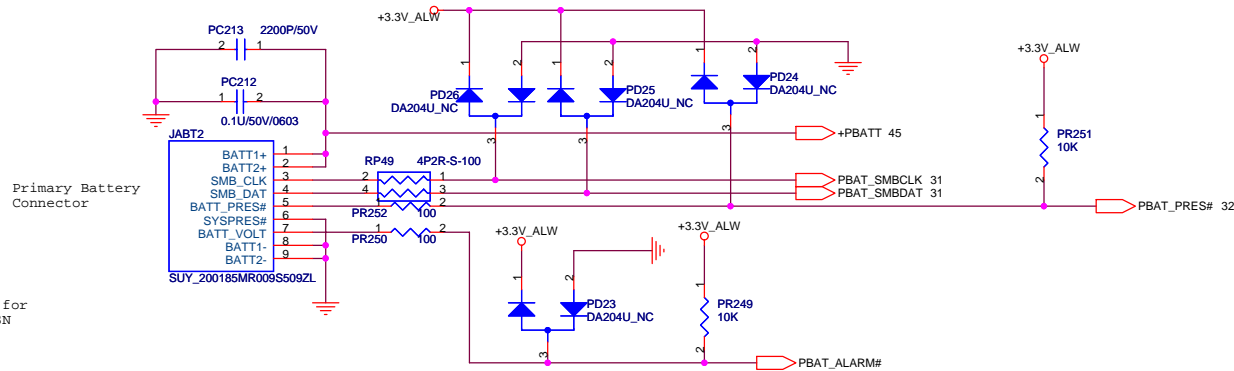
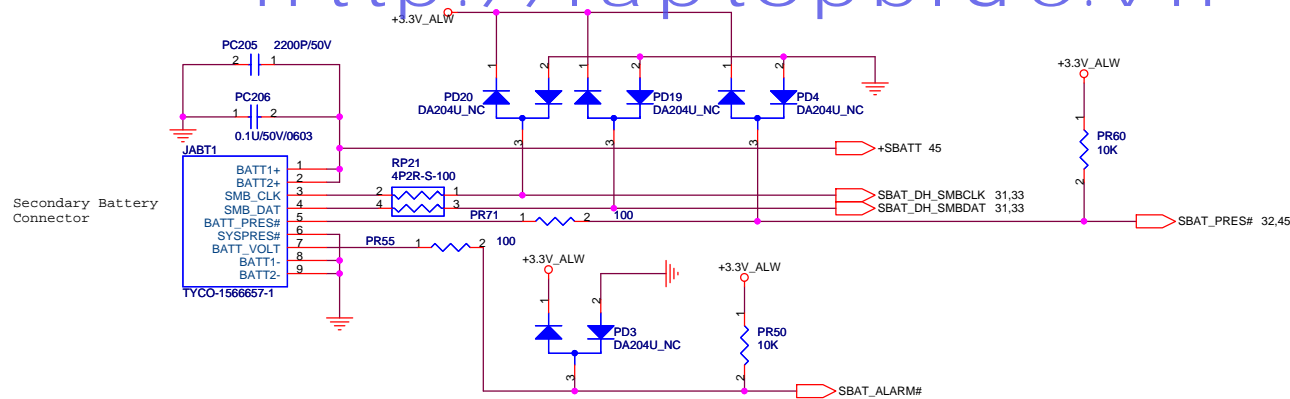
2C

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h t t p : / / l a p t o p b l u e . v n





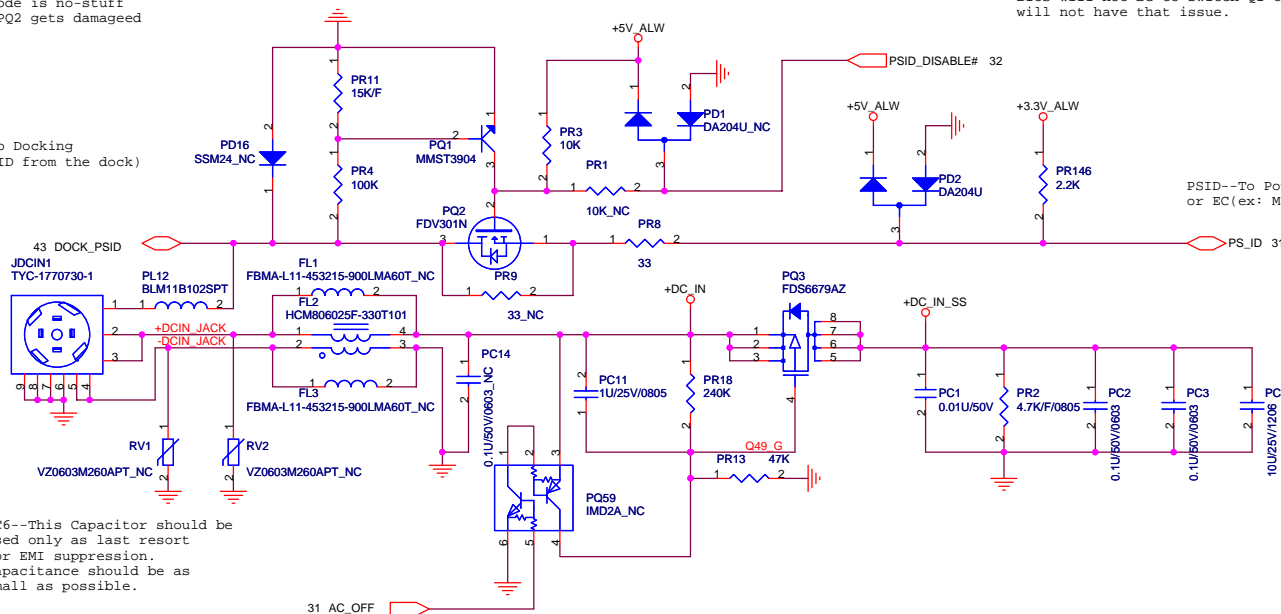
PQ2--Three transistor can be used for PQ2(pin compatible):FDV301N/FDV303N has low Vgs_on w/built-in ESD protection.MMBT100 BJT works in reverse conduction mode.

D12--This diode is no-stuff populate if PQ2 gets damaged by ESD.

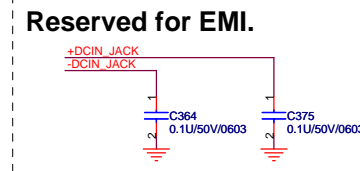
PR1--This resistor must be depopulated if FDV301N/FDV303 are used to avoid a 1.36mA constant current drain from +3VALW. Thus, BIOS will not be to switch Q1 off. MMBT100 will not have that issue.

DOCK_PSID--To Docking connector(PSID from the dock)

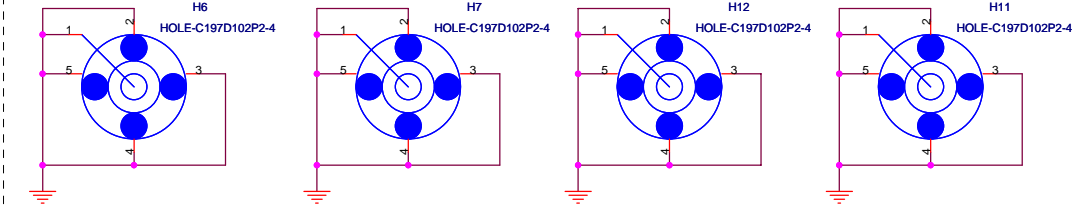
PSID--To Power Management Controller or EC(ex: Macallan3)



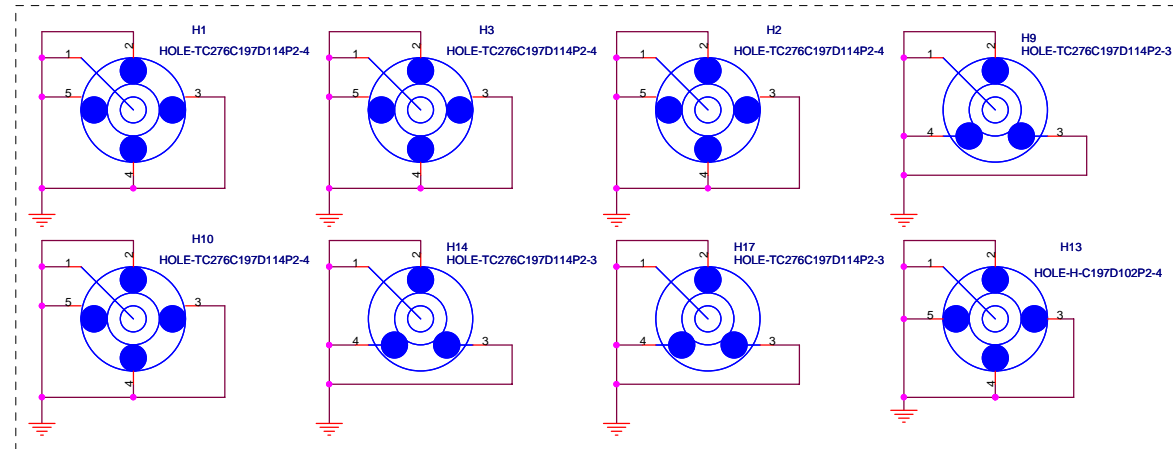
PC6--This Capacitor should be used only as last resort for EMI suppression. Capacitance should be as small as possible.



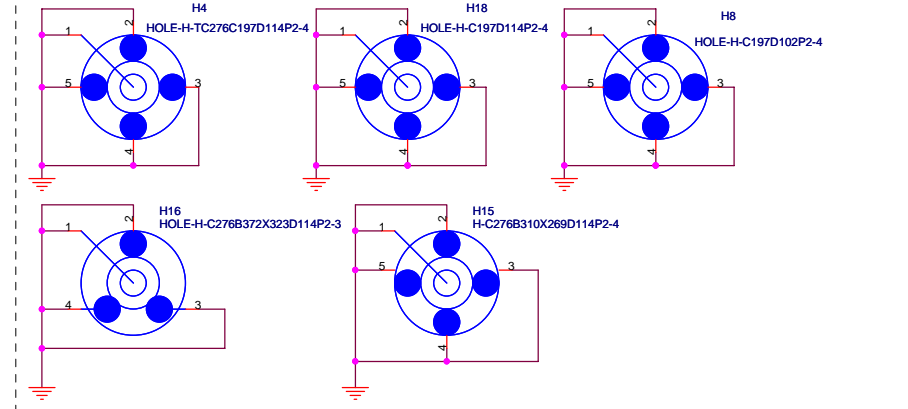
CPU




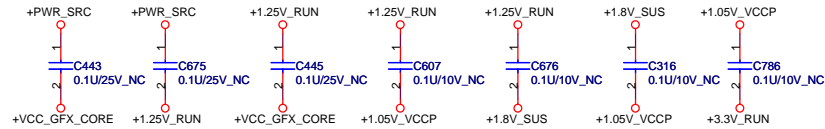
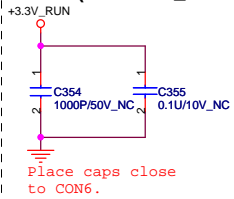
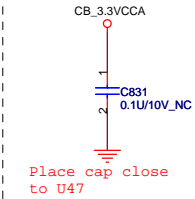
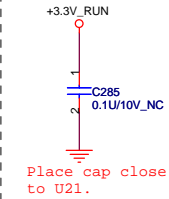
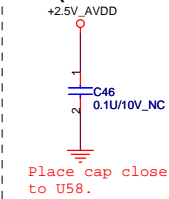
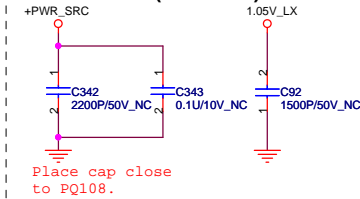
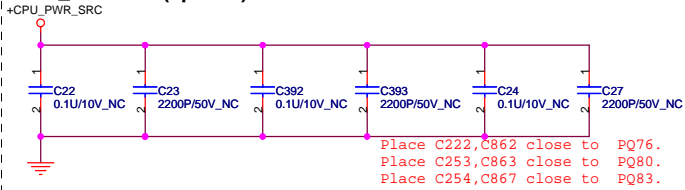
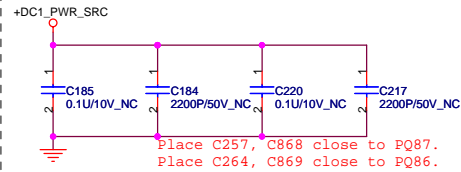
Reserved for EMI.



HDD



 QUANTA COMPUTER		
Title SCREW PAD		
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Stitching caps**Page 26**
SATA (HDD&CD_ROM)**Page 27**
PCCARD /CONN**Page 38**
Azelia CODEC**Page 40**
LAN(BCM5755M)**Page 48**
1.25V & 1.05V(MAX8778)**Page 51**
CPU_MAX8786(3phase)**Page 52**
D/D Power

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ICH8-M

SIO
MEC5025

