COMPAL CONFIDENTIAL

MODEL NAME : ***HAL00***

PCB NO : ***LA-2792***

COMPAL P/N : ***45135731L01***

Travis (DIS) Schematics Document

uFCPGA Mobile Yonah
Intel Calistoga + ICH7M

2006-01-20

REV : 1.0 (DELL: A00)

MB PCB

Part Number	Description
DAA0000050L	PCB ZJX LA-2792 REV0 MB DIS

BOM NO. 45135731L01

PCB P/N: DAA0000051L

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Title: Cover Sheet

Size | Document Number: LA-2792 | Rev: 1.0

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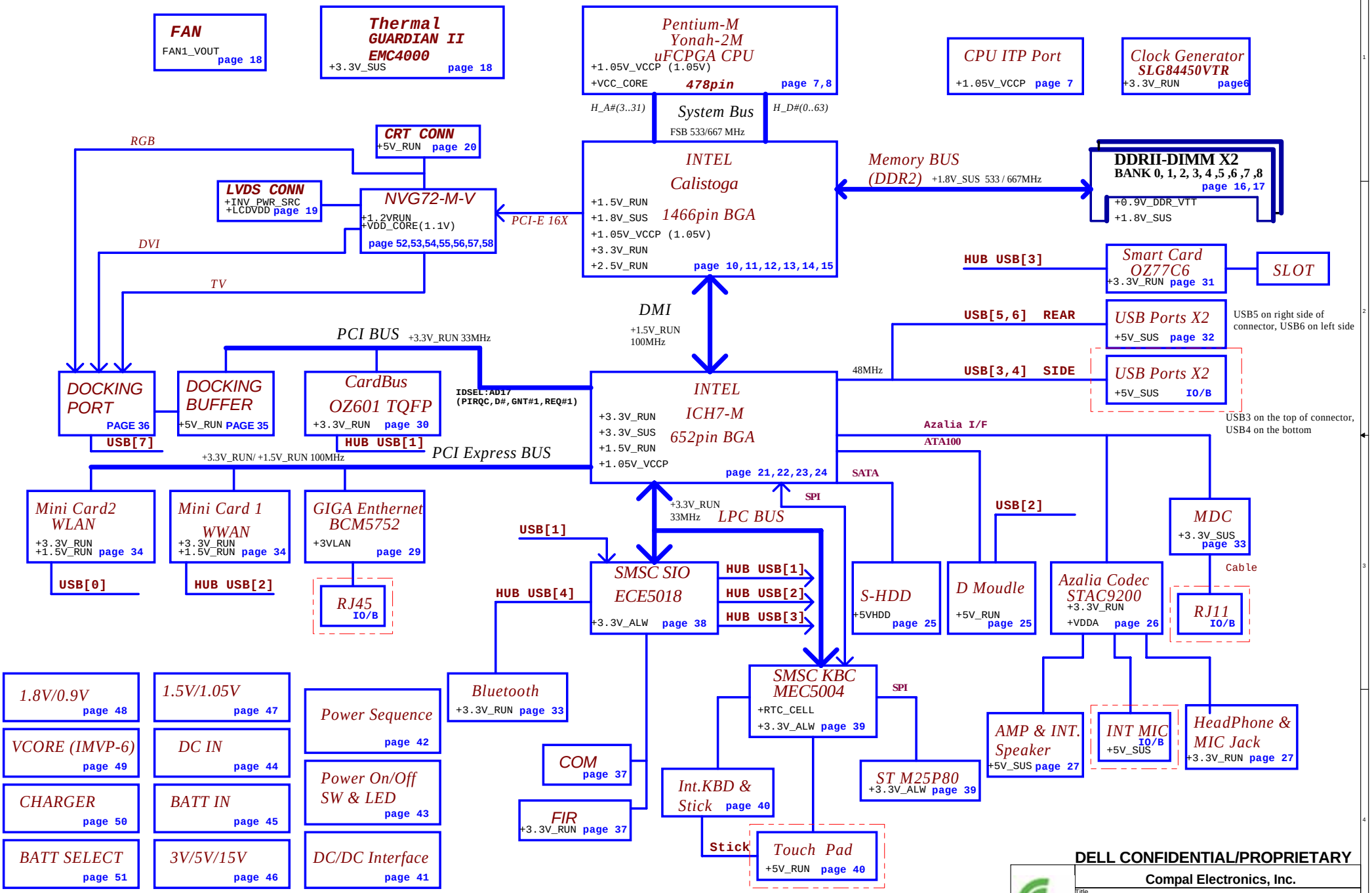
Block Diagram



Compal Electronics, Inc.		
Title: Block Diagram		
Size	Document Number: LA-2792	Rev: 1.0
Date: Tuesday, February 07, 2006	Sheet 2 of 70	

Ceramic Capacitors :

0.1U_0402_6.3VXX

- Tolerance
- Temperature Characteristics
- Rated Voltage
- Package Size
- Value

Tantalum or Polymer Capacitors :

10U_D2_10VX_R45

- Low ESR Mark : 45 m ohm
- Tolerance
- Rated Voltage
- Package Size
- Value

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CARD BUS	AD17	1	C

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW	+3.3V_SRC +15V_SUS +5V_SUS +3.3V_SUS +1.8V_SUS	+5V_RUN +3.3V_RUN +1.8V_RUN +0.9V_DDR_VTT +1.5V_RUN +VCC_CORE +1.05V_VCCP +2.5V_RUN
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

Capacitor Spec Guide:

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7
CODE	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R

8	9	A	B	C	D	E	F	G
NPO	COG	X6S	BJ	CH	CJ	CK	SH	SJ

H	I	J	K
UJ	UK	SL	X5S

Tolerance:

Symbol	A	B	C	D	F	G	H	J
CODE	+-0.05PF	+-0.1PF	+-0.25PF	+-0.5PF	+-1PF	+-2%	+-3%	+-5%

K	M	N	P	Q	V	X	Z	
+-10%	+-20%	+-30%	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	

USB TABLE

USB PORT#	DESTINATION
0	Mini 2(WLAN)
1	USB Hub (5018)
2	D Moudle
3,4	SIDE
5,6	REAR
7	Docking

USB HUB	DESTINATION
1	PC Card Bay
2	Mini 1(WWAN)
3	Smart Card --> BIO
4	Blue tooth

NOTE1:

@XX : Depop component

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Title: Index and Config.

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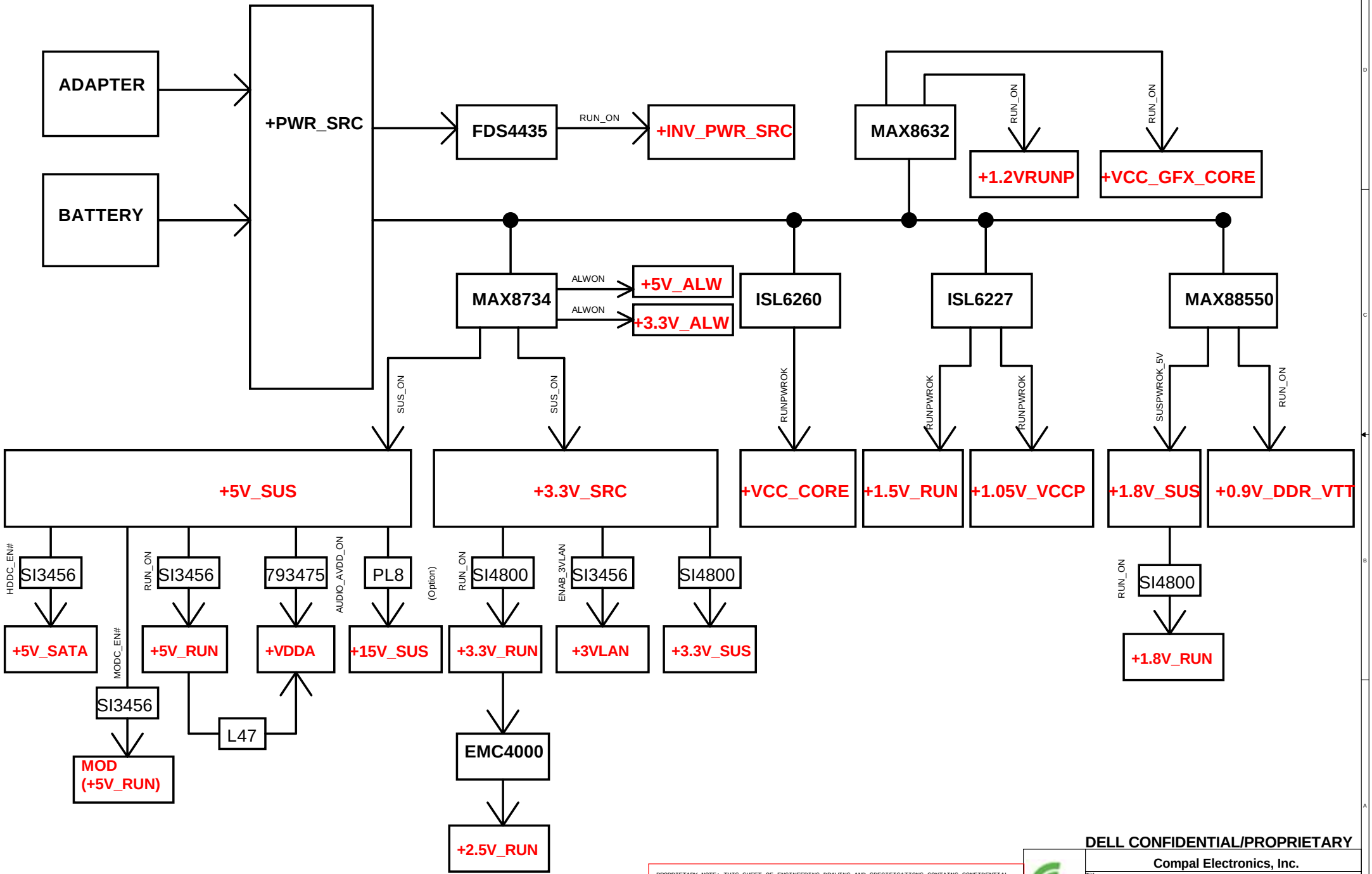

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Title: Power Rail

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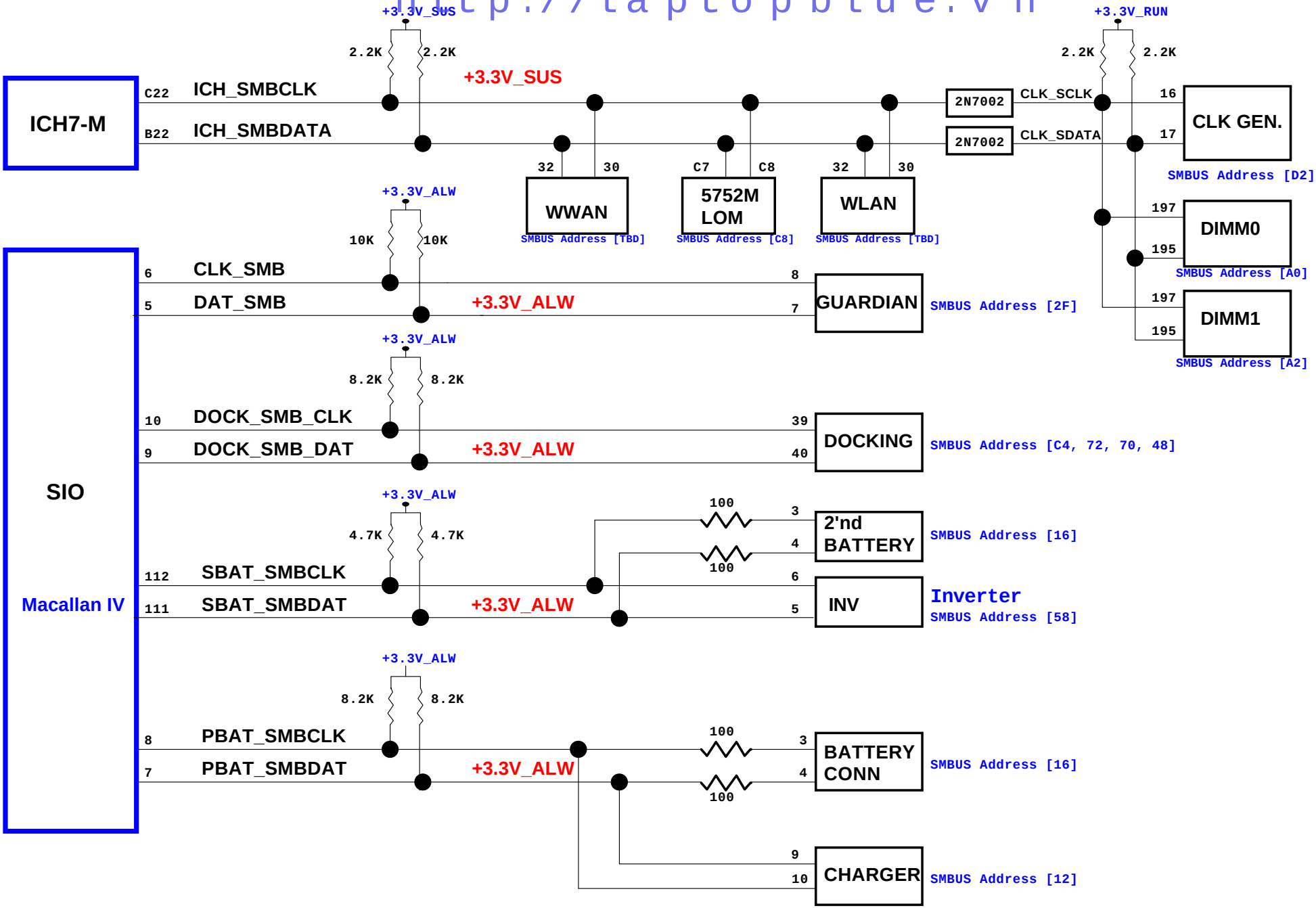
Date: Tuesday, February 07, 2006 | Sheet 4 of 70



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Title: SMBUS TOPOLOGY

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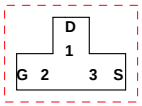

2N7002

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
* 0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	1	Reserve		

Table : ICS954305AK

CPU_BSEL	CPU_BSEL2(FSC)	CPU_BSEL1(FSB)
133	0	0
166	0	1

FCTSEL1	PIN43	PIN44	PIN47	PIN48
0(UMA)	DOT96T	DOT96C	96/100M_T	96/100M_C
* 1(DIS)	27M_out	27M SSout	SRCT0	SRCC0

Solder Thermal Pad to GND. Add min. 4 vias.

NOTE: Place Decoupling as close as physicallly possilble to the VDD pins

Place crystal within 500 mils of CK410

Place near each pin W>40 mil

Place near CK410+

U16

SLG84450VTR_QFN72-D

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Title: Clock Generator

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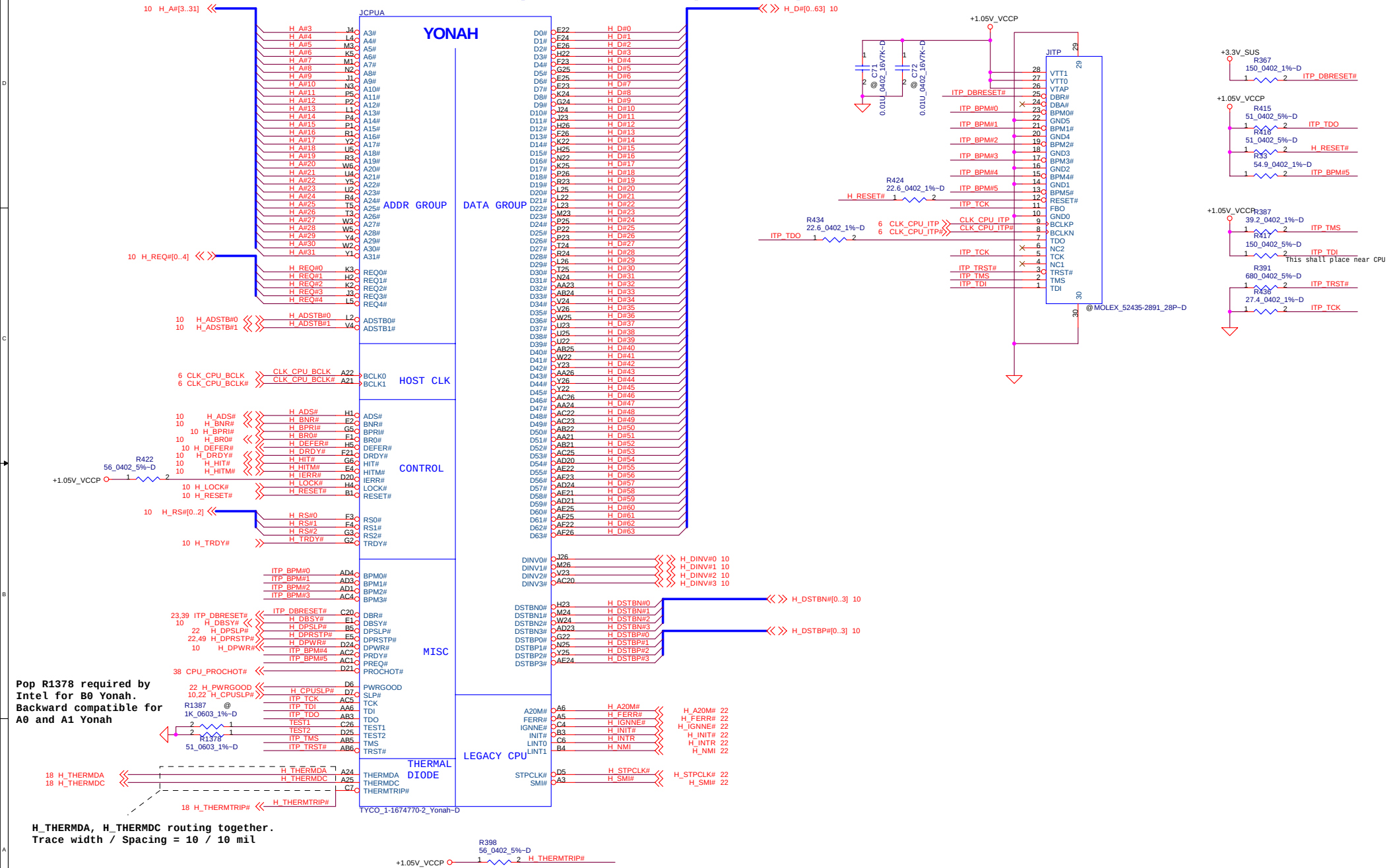

Compal Electronics, Inc.

Title: Yonah in mFCPGA479

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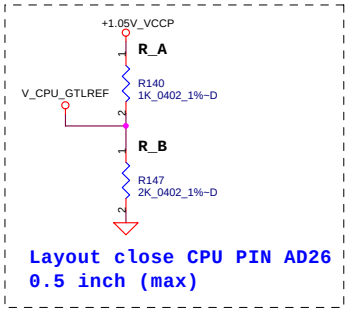
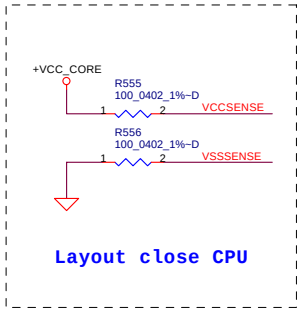
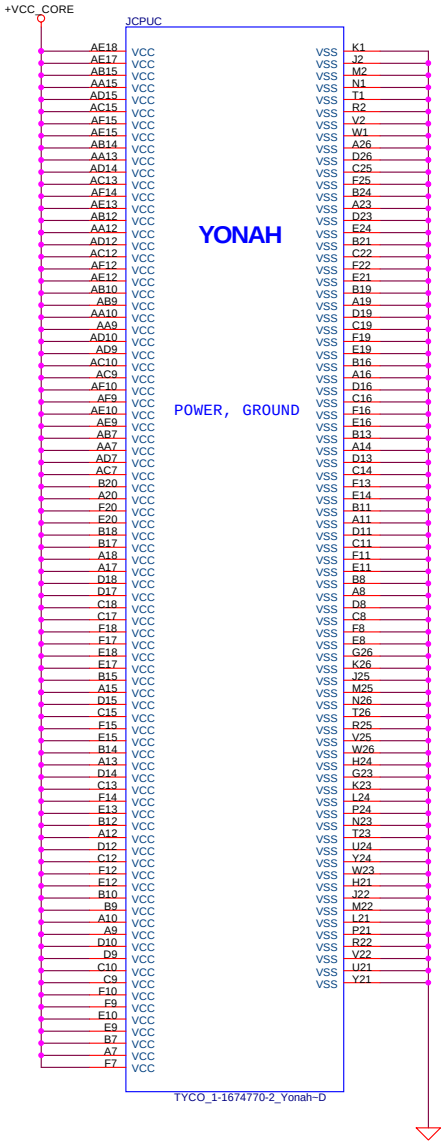
Length match within 25 mils







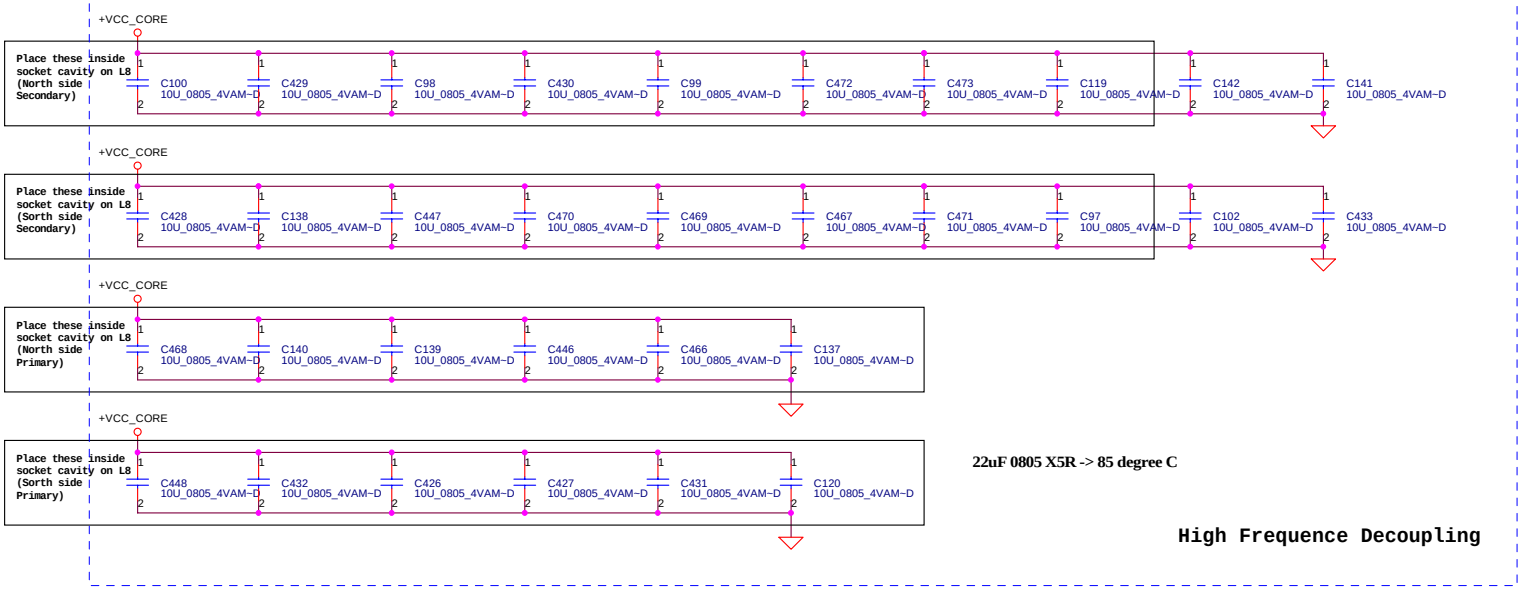
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

Compal Electronics, Inc.

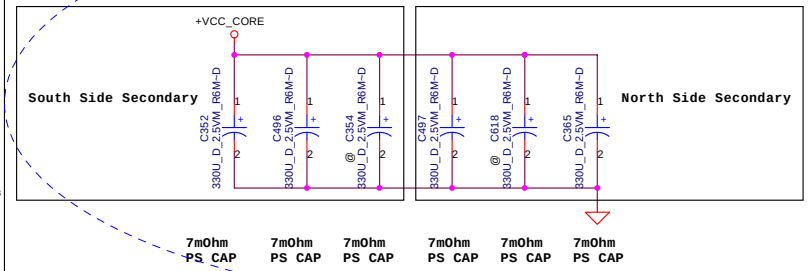
Title: Yonah in mFCPGA479

Size: Document Number: LA-2792 Rev: 1.0

Date: Tuesday, February 07, 2006 Sheet 8 of 70

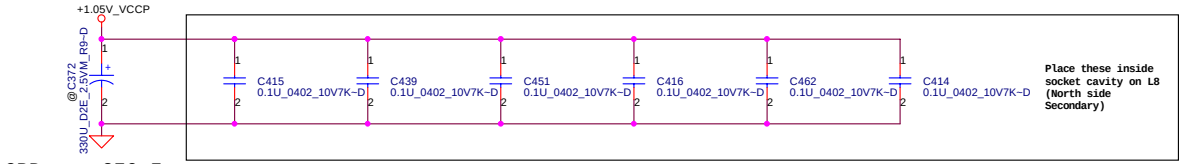


Near VCORE regulator.



The caps need change to ESR=6m ohms

ESR <= 1.5m ohm
Capacitor > 1980uF



CRB was 270uF

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Title: CPU Bypass

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Description at page12

Note :
CFG3:17 has internal pullup,
CFG18:19 has internal pulldown

A

HOST

U40A

CALISTOGA_FCBGA1466-D

U40B

CALISTOGA_FCBGA1466-D

Layout Note:
H_XRCOMP & H_YRCOMP trace width and spacing is 10/20

Layout Note:
Route as short as possible

Stuff R435 & R437 for A1 Calistoga

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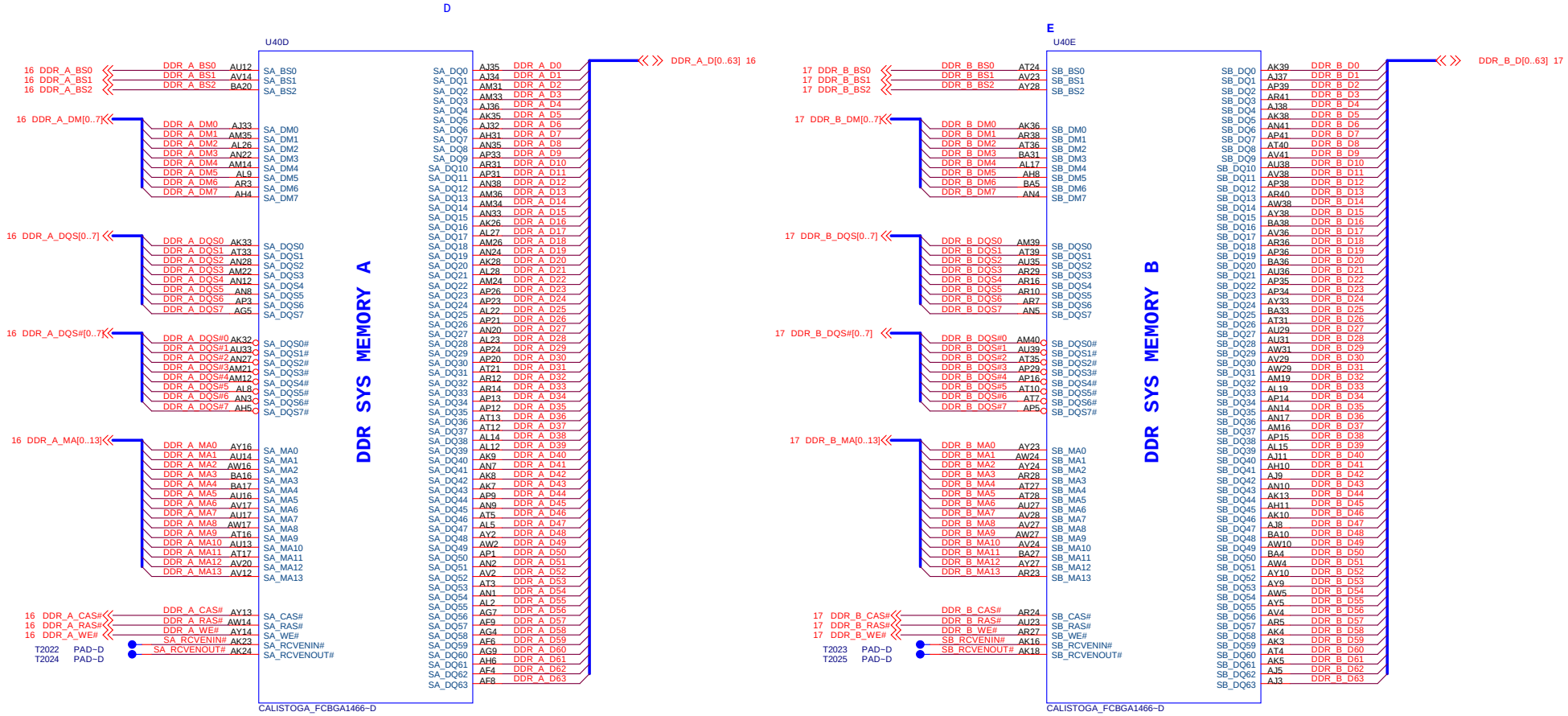
Compal Electronics, Inc.

Title: Calistoga(1 of 6)

Size: | Document Number: LA-2792 | Rev: 1.0

Date: Tuesday, February 07, 2006 | Sheet 10 of 70



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Compal Electronics, Inc.

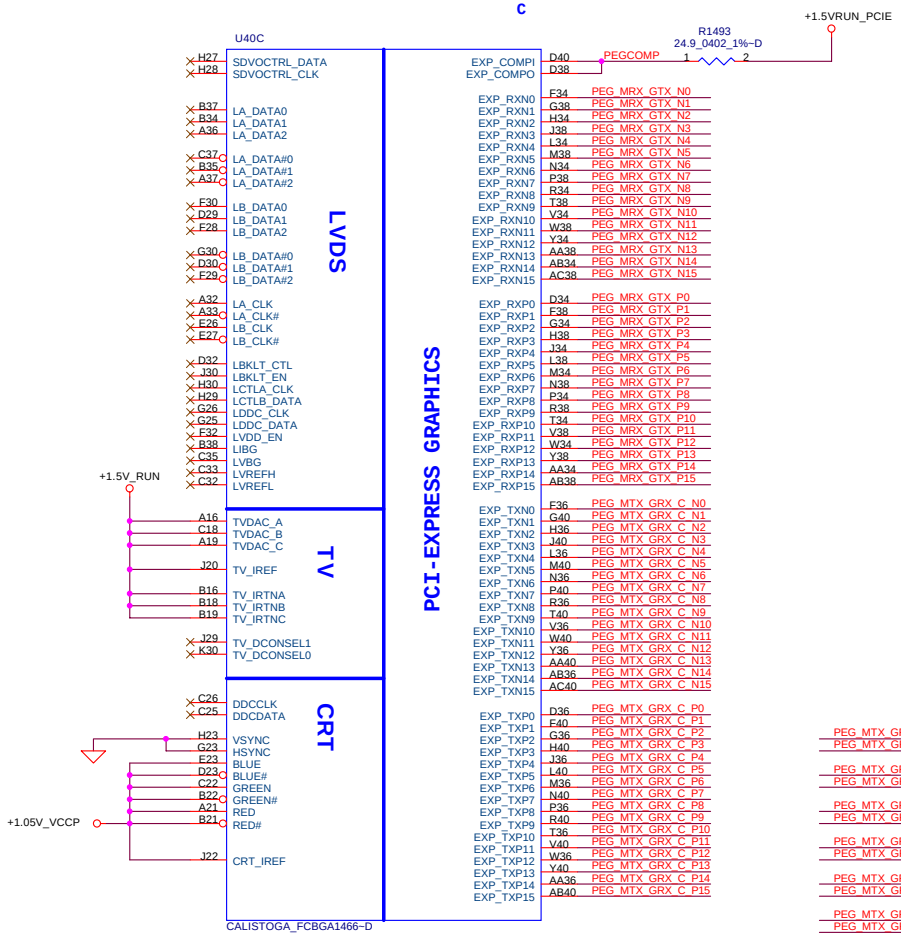
Title: Calistogo(2 of 6)

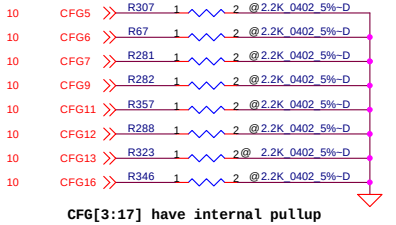
Size | Document Number: LA-2792 | Rev: 1.0

Date: Tuesday, February 07, 2006 | Sheet 11 of 70

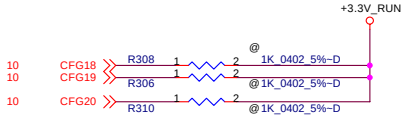
Strap Pin Table

CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	LOW = Moby Dick HIGH = Calistoga *
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG11	
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (DMI Lane Reversal)	Low = Normal * Operation (Default): Lane number in Order High = Reverse Lane
SDVO_CTRLDATA	Low = No SDVO Device Present (Default)* High = SDVO Device Present
CFG20 (PCIE/SDVO select)	Low = Only PCIE or SDVO is operational. (Default)* High = PCIE/SDVO are operating simu.

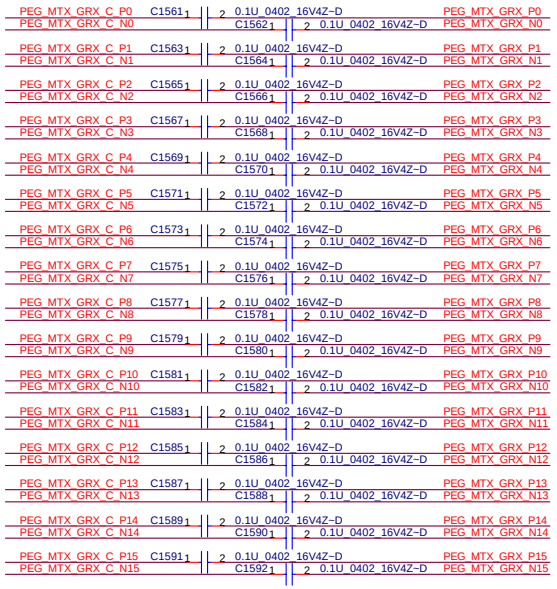


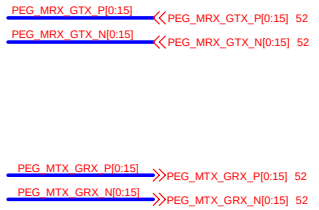


CFG[3:17] have internal pullup



CFG[18:20] have internal pulldown





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Title: Calistoga(3 of 6)

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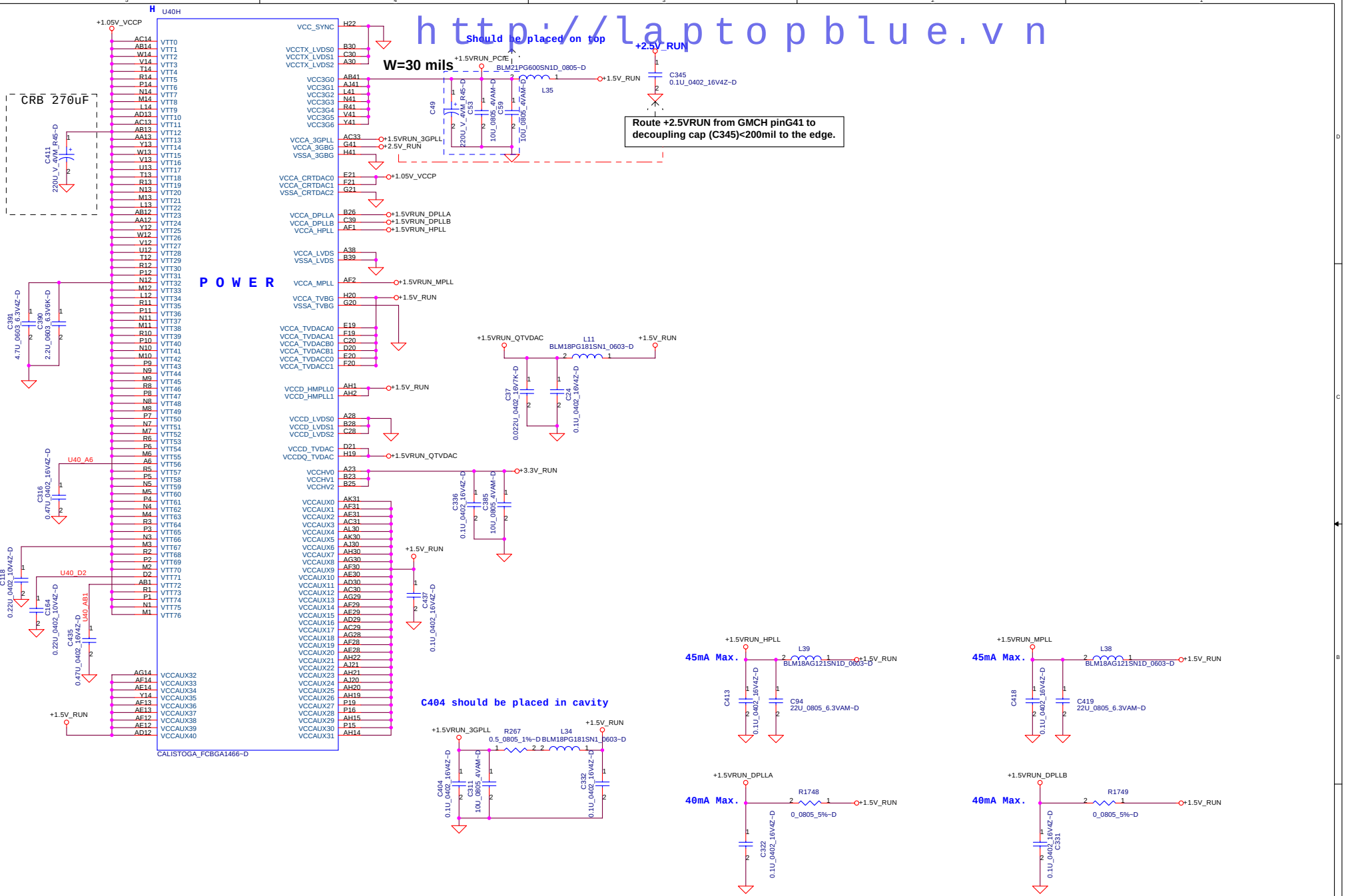

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Title: Calistoga(4 of 6)

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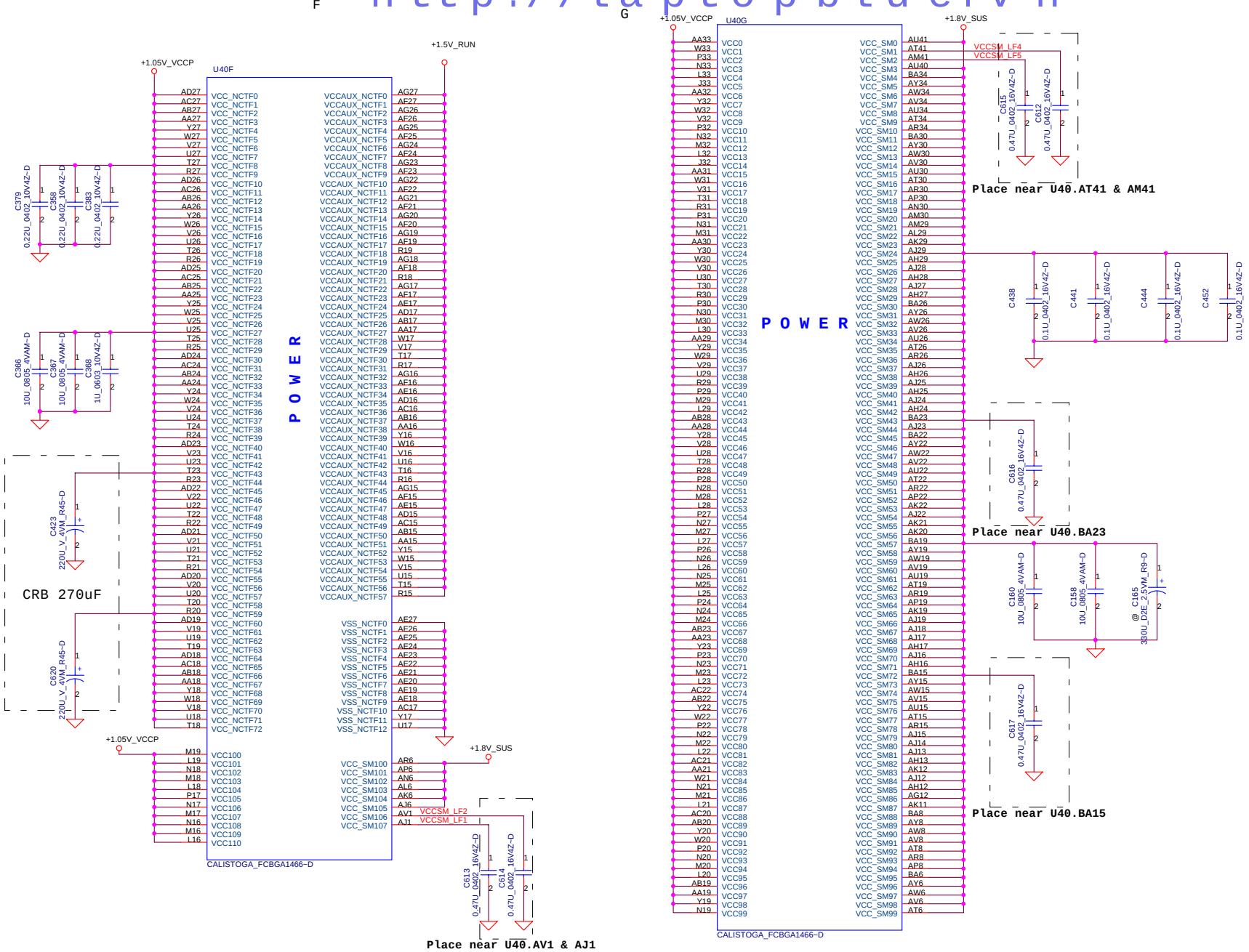

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Title: Calistoga(5 of 6)

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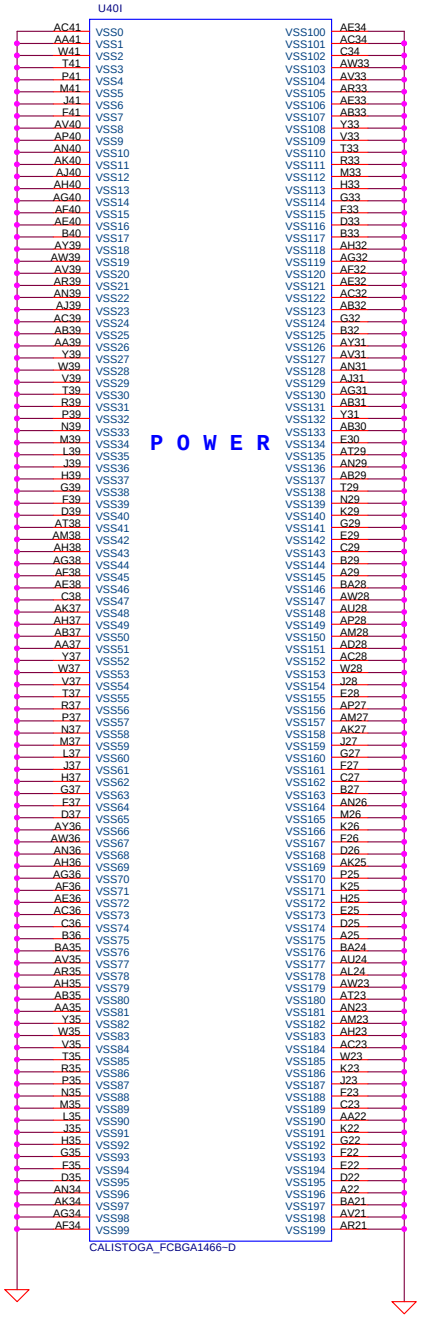

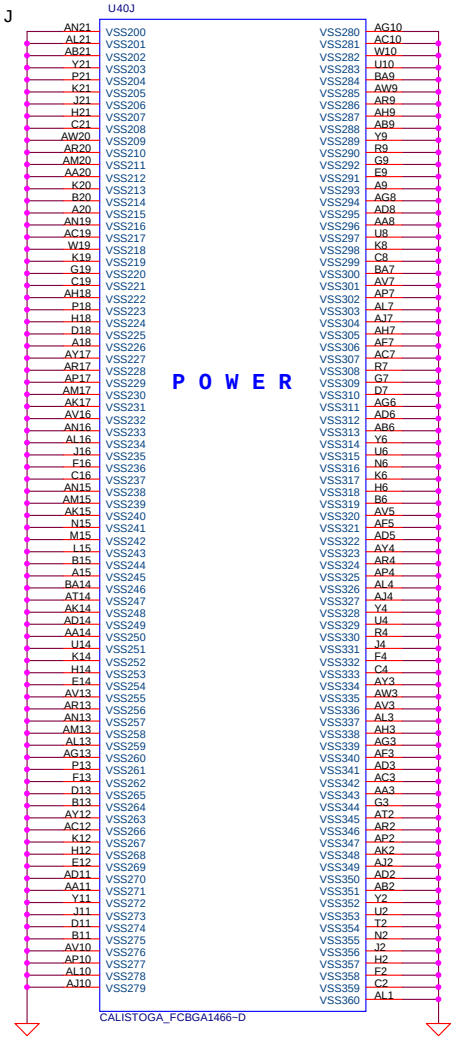

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Title: Calistoga(6 of 6)

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ON TOP SIDE

11 DDR_A_DQS#[0..7]
11 DDR_A_D[0..63]
11 DDR_A_DM[0..7]
11 DDR_A_DQS[0..7]
11 DDR_A_MA[0..13]

Layout Note:
Place near JDIM1

+1.8V_SUS

C213 2.2U_0603_6.3V6K~D
C214 2.2U_0603_6.3V6K~D
C222 2.2U_0603_6.3V6K~D
C225 2.2U_0603_6.3V6K~D
C229 2.2U_0603_6.3V6K~D
C212 0.1U_0402_16V4Z~D
C215 0.1U_0402_16V4Z~D
C223 0.1U_0402_16V4Z~D
C227 0.1U_0402_16V4Z~D

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT

+0.9V_DDR_VTT

C221 C220 C219 C218 C217 C216 C231 C232 C233 C235 C237 C236 C234 (0.1U_0402_16V4Z~D)

+0.9V_DDR_VTT

RN25: DDR_A_MA1, DDR_A_MA3 — RN27: DDR_A_MA9, DDR_A_MA12
RN24: DDR_A_BS0, DDR_A_MA10 — RN19: DDR_A_MA7, DDR_A_MA6
RN16: DDR_A_RAS#, DDR_CS0_DIMMA# — RN26: DDR_A_MA5, DDR_A_MA8
RN23: DDR_A_CAS#, DDR_A_WE# — RN18: DDR_A_MA4, DDR_A_MA2
RN22: M_ODT1, DDR_CS1_DIMMA# — RN17: DDR_A_MA0, DDR_A_BS1
RN15: M_ODT0, DDR_A_MA13
RN21: DDR_CKE0_DIMMA, DDR_A_BS2 — RN20: DDR_CKE1_DIMMA, DDR_A_MA11
56_0404_4P2R_5%~D

Layout Note:
Place these resistor closely DIMM0,all trace length<750 mil

Layout Note:
Place these resistor closely DIMM0,all trace length Max=1.3"

+1.8V_SUS

JDIM2 (TYCO_1470815-2~D)

VREF	1	2	VSS
VSS	3	4	DDR_A_D7 / DDR_A_D4
DDR_A_D0 / DDR_A_D1	5	6	DQ4 / DQ5
DQ0 / DQ1	7	8	VSS
VSS	9	10	DDR_A_DM0
DDR_A_DQS#0 / DDR_A_DQS0	11	12	DM0 / VSS
DQS0# / DQS0	13	14	DDR_A_D6 / DDR_A_D5
VSS	15	16	DQ6 / DQ7
DDR_A_D3 / DDR_A_D2	17	18	VSS
DQ2 / DQ3	19	20	DDR_A_D13 / DDR_A_D12
VSS	21	22	DQ12 / DQ13
DDR_A_D14 / DDR_A_D8	23	24	VSS
DQ8 / DQ9	25	26	DDR_A_DM1 / DM1
VSS	27	28	VSS
DDR_A_DQS#1 / DDR_A_DQS1	29	30	M_CLK_DDR0 / CK0
DQS1# / DQS1	31	32	M_CLK_DDR#0 / CK0#
VSS	33	34	VSS
DDR_A_D11 / DDR_A_D10	35	36	DDR_A_D15 / DDR_A_D9
DQ10 / DQ11	37	38	DQ14 / DQ15
VSS	39	40	VSS
VSS	41	42	VSS
DDR_A_D20 / DDR_A_D17	43	44	DDR_A_D16 / DDR_A_D21
DQ16 / DQ17	45	46	DQ20 / DQ21
VSS	47	48	VSS
DDR_A_DQS#2 / DDR_A_DQS2	49	50	PM_EXTTS#0_R / NC
DQS2# / DQS2	51	52	DDR_A_DM2 / DM2
VSS	53	54	VSS
DDR_A_D22 / DDR_A_D23	55	56	DDR_A_D18 / DDR_A_D19
DQ18 / DQ19	57	58	DQ22 / DQ23
VSS	59	60	VSS
DDR_A_D24 / DDR_A_D29	61	62	DDR_A_D28 / DDR_A_D25
DQ24 / DQ25	63	64	DQ28 / DQ29
VSS	65	66	VSS
DDR_A_DM3 / DM3	67	68	DDR_A_DQS#3 / DQS3#
NC	69	70	DDR_A_DQS3 / DQS3
VSS	71	72	VSS
DDR_A_D31 / DDR_A_D27	73	74	DDR_A_D26 / DDR_A_D30
DQ26 / DQ27	75	76	DQ30 / DQ31
VSS	77	78	VSS
DDR_CKE0_DIMMA / CKE0	79	80	DDR_CKE1_DIMMA / NC/CKE1
VDD	81	82	VDD
NC	83	84	NC/A15
DDR_A_BS2 / BA2	85	86	NC/A14
VDD	87	88	VDD
DDR_A_MA12 / A12	89	90	DDR_A_MA11 / A11
DDR_A_MA9 / A9	91	92	DDR_A_MA7 / A7
DDR_A_MA8 / A8	93	94	DDR_A_MA6 / A6
VDD	95	96	VDD
DDR_A_MA5 / A5	97	98	DDR_A_MA4 / A4
DDR_A_MA3 / A3	99	100	DDR_A_MA2 / A2
DDR_A_MA1 / A1	101	102	DDR_A_MA0 / A0
VDD	103	104	VDD
DDR_A_MA10 / A10/AP	105	106	DDR_A_BS1 / BA1
DDR_A_BS0 / BA0	107	108	DDR_A_RAS# / RAS#
DDR_A_WE# / WE#	109	110	DDR_CS0_DIMMA# / S0#
VDD	111	112	VDD
DDR_A_CAS# / CAS#	113	114	M_ODT0 / ODT0
DDR_CS1_DIMMA# / NC/S1#	115	116	DDR_A_MA13 / NC/A13
VDD	117	118	VDD
M_ODT1 / NC/ODT1	119	120	NC
VSS	121	122	VSS
DDR_A_D35 / DDR_A_D32	123	124	DDR_A_D36 / DDR_A_D37
DQ32 / DQ33	125	126	DQ36 / DQ37
VSS	127	128	VSS
DDR_A_DQS#4 / DDR_A_DQS4	129	130	DDR_A_DM4 / DM4
DQS4# / DQS4	131	132	VSS
VSS	133	134	DDR_A_D39 / DDR_A_D38
DDR_A_D34 / DDR_A_D33	135	136	DQ38 / DQ39
DQ34 / DQ35	137	138	VSS
VSS	139	140	DDR_A_D44 / DDR_A_D40
DDR_A_D43 / DDR_A_D45	141	142	DQ44 / DQ45
DQ40 / DQ41	143	144	VSS
VSS	145	146	DDR_A_DQS#5 / DQS5#
DDR_A_DM5 / DM5	147	148	DDR_A_DQS5 / DQS5
VSS	149	150	VSS
DDR_A_D46 / DDR_A_D47	151	152	DDR_A_D41 / DDR_A_D42
DQ42 / DQ43	153	154	DQ46 / DQ47
VSS	155	156	VSS
DDR_A_D48 / DDR_A_D52	157	158	DDR_A_D49 / DDR_A_D53
DQ48 / DQ49	159	160	DQ52 / DQ53
VSS	161	162	VSS
NC,TEST	163	164	M_CLK_DDR1 / CK1
VSS	165	166	M_CLK_DDR#1 / CK1#
DDR_A_DQS#6 / DDR_A_DQS6	167	168	VSS
DQS6# / DQS6	169	170	DDR_A_DM6 / DM6
VSS	171	172	VSS
DDR_A_D55 / DDR_A_D51	173	174	DDR_A_D50 / DDR_A_D54
DQ50 / DQ51	175	176	DQ54 / DQ55
VSS	177	178	VSS
DDR_A_D60 / DDR_A_D61	179	180	DDR_A_D57 / DDR_A_D56
DQ56 / DQ57	181	182	DQ60 / DQ61
VSS	183	184	VSS
DDR_A_DM7 / DM7	185	186	DDR_A_DQS#7 / DQS7#
VSS	187	188	DDR_A_DQS7 / DQS7
DDR_A_D58 / DDR_A_D59	189	190	VSS
DQ58 / DQ59	191	192	DDR_A_D62 / DDR_A_D63
VSS	193	194	DQ62 / DQ63
CLK_SDATA / SDA	195	196	VSS
CLK_SCLK / SCL	197	198	SAO
+3.3V_RUN / VDDSPD	199	200	SA1
GND	201	202	GND

V_DDR_MCH_REF — V_DDR_MCH_REF 10,17,48
2.2U_0603_6.3V6K~D (C226), 0.1U_0402_16V4Z~D (C224), R51 100K_0402_5%~D
PM_EXTTS#0_R 17 — R177 0_0402_5%~D — PM_EXTTS#0 10
M_CLK_DDR0 10 / M_CLK_DDR#0 10
DDR_CKE0_DIMMA 10 / DDR_CKE1_DIMMA 10
DDR_A_BS2 11 / DDR_A_BS0 11 / DDR_A_WE# 11 / DDR_A_CAS# 11 / DDR_CS1_DIMMA# 10 / M_ODT1 10
DDR_A_BS1 11 / DDR_A_RAS# 11 / DDR_CS0_DIMMA# 10 / M_ODT0 10
6,17 CLK_SDATA / 6,17 CLK_SCLK
R175 100K_0402_5%~D / R176 100K_0402_5%~D
0.1U_0402_16V4Z~D (C228), 2.2U_0603_6.3V6K~D (C230)

DIMMA RESERVE

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Compal Electronics, Inc.

Title: DDRII-SODIMM SLOT1

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ON BOTTOM SIDE

11 DDR_B_DQS#[0..7]
11 DDR_B_D[0..63]
11 DDR_B_DM[0..7]
11 DDR_B_DQS[0..7]
11 DDR_B_MA[0..13]

Layout Note:
Place near JDIM2

+1.8V_SUS

C249 2.2U_0603_6.3V6K-D
C254 2.2U_0603_6.3V6K-D
C261 2.2U_0603_6.3V6K-D
C242 2.2U_0603_6.3V6K-D
C241 2.2U_0603_6.3V6K-D
C240 0.1U_0402_16V4Z-D
C239 0.1U_0402_16V4Z-D
C251 0.1U_0402_16V4Z-D
C255 0.1U_0402_16V4Z-D

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT

+0.9V_DDR_VTT

C248 C247 C246 C245 C244 C243 C269 C268 C267 C266 C265 C264 C263 0.1U_0402_16V4Z-D

+0.9V_DDR_VTT

RN11 RN13 RN10 RN7 RN4 RN12 RN3 RN6 RN9 RN5 RN2 RN8 RN14
56_0404_4P2R_5%-D

DDR_B_MA1 DDR_B_MA3 DDR_B_MA9 DDR_B_MA12 DDR_B_BS0 DDR_B_MA10 DDR_B_MA11 DDR_CKE3_DIMMB DDR_B_MA0 DDR_B_BS1 DDR_B_MA5 DDR_B_MA8 DDR_B_RAS# DDR_CS2_DIMMB# DDR_B_MA7 DDR_B_MA6 DDR_B_CAS# DDR_B_WE# DDR_B_MA4 DDR_B_MA2 DDR_CS3_DIMMB# M_ODT3 DDR_B_BS2 DDR_CKE2_DIMMB M_ODT2 DDR_B_MA13

Layout Note:
Place these resistor closely DIMM0,all trace length<750 mil

Layout Note:
Place these resistor closely DIMM0,all trace length Max=1.3"

+1.8V_SUS +1.8V_SUS

JDIM1

DDR_B_D[0..63] DDR_B_DQS#[0..7] DDR_B_DQS[0..7] DDR_B_DM[0..7] DDR_B_DM0 DDR_B_DM1 DDR_B_DM2 DDR_B_DM3 DDR_B_DM4 DDR_B_DM5 DDR_B_DM6 DDR_B_DM7 DDR_B_DM8

M_CLK_DDR3 10
M_CLK_DDR#3 10
PM_EXTTS#0_R 16
DDR_CKE3_DIMMB 10
M_CLK_DDR2 10
M_CLK_DDR#2 10
DDR_B_BS1 11
DDR_B_RAS# 11
DDR_CS2_DIMMB# 10
M_ODT2 10

10 DDR_CKE2_DIMMB
11 DDR_B_BS2
11 DDR_B_BS0
11 DDR_B_WE#
11 DDR_B_CAS#
10 DDR_CS3_DIMMB#
10 M_ODT3
6,16 CLK_SDATA
6,16 CLK_SCLK

+3.3V_RUN

C549 0.1U_0402_16V4Z-D
C548 2.2U_0603_6.3V6K-D

V_DDR_MCH_REF V_DDR_MCH_REF 10,16,48
C253 2.2U_0603_6.3V6K-D
C252 0.1U_0402_16V4Z-D

+3.3V_RUN
R174 10K_0402_5%-D
R173 100K_0402_5%-D

TYCO_1565917-4-D

DIMMB STANDARD

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Title: DDRII-SODIMM SLOT2

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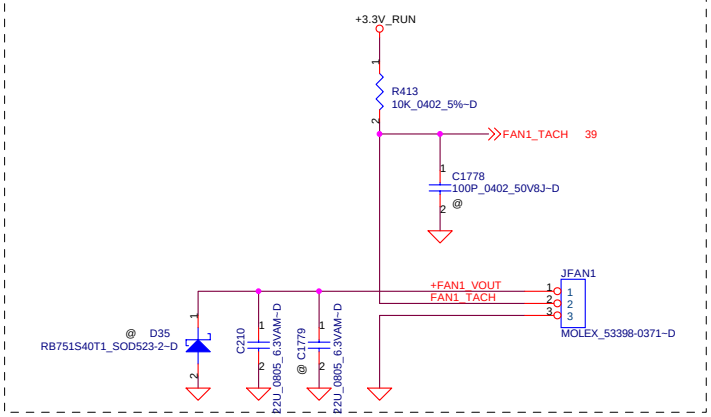
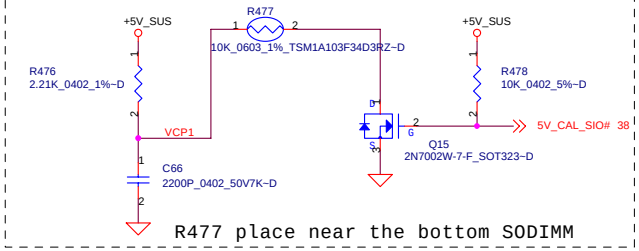
FAN1 Control and Tachometer

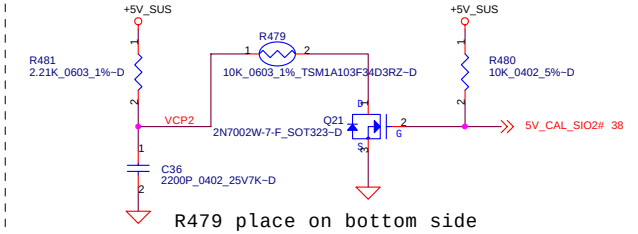


Place near the bottom SODIMM



R477 place near the bottom SODIMM

Place near the bottom SODIMM



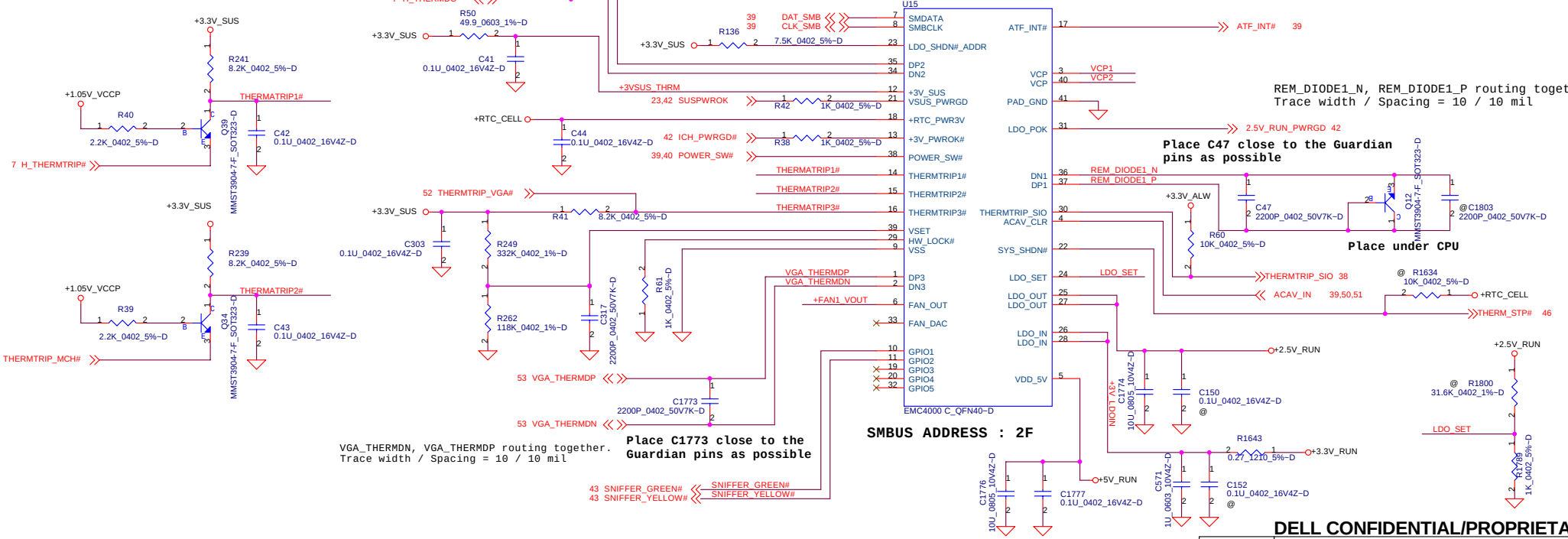
R479 place on bottom side
next to SoDIMM connector

$$VSET = \frac{R262}{R249+R262} \times 3.3V$$

$$VSET = \left(\frac{Tp-70}{21} \right)$$

Place C341 close to the Guardian pins as possible

DP2, DN2 routing together. Trace width / Spacing = 10 / 10 mil



VGA_THERMDN, VGA_THERMDP routing together.
Trace width / Spacing = 10 / 10 mil

Place C1773 close to the Guardian pins as possible

SMBUS ADDRESS : 2F

REM_DIODE1_N, REM_DIODE1_P routing together.
Trace width / Spacing = 10 / 10 mil

Place C47 close to the Guardian pins as possible

Place cap close to the Guardian pins as possible.

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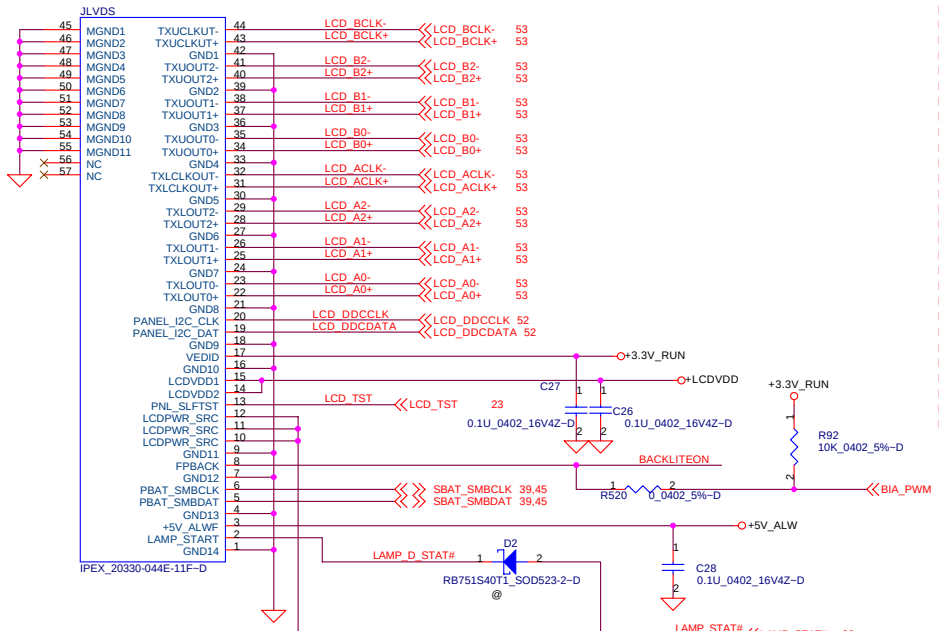
Compal Electronics, Inc.

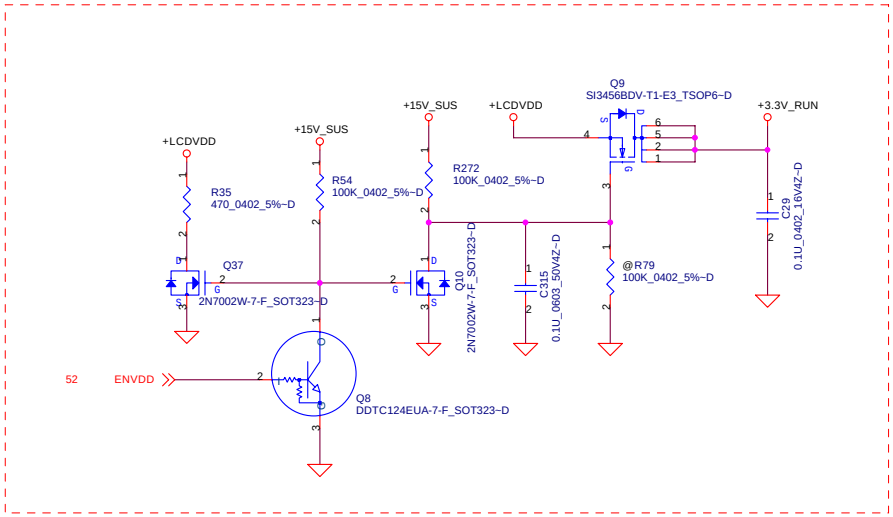
Title: FAN & Thermal Sensor

Size: | Document Number: LA-2792 | Rev: 1.0

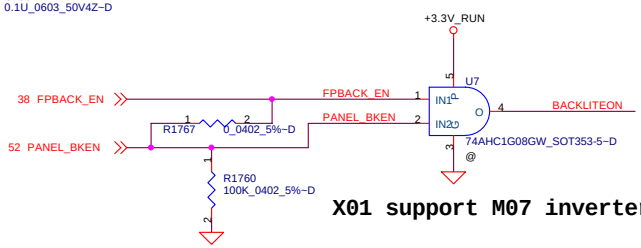
Date: Tuesday, February 07, 2006 | Sheet 18 of 70



M'07 inverter support - Depop D2.
D'05 inverter support - Populate D2

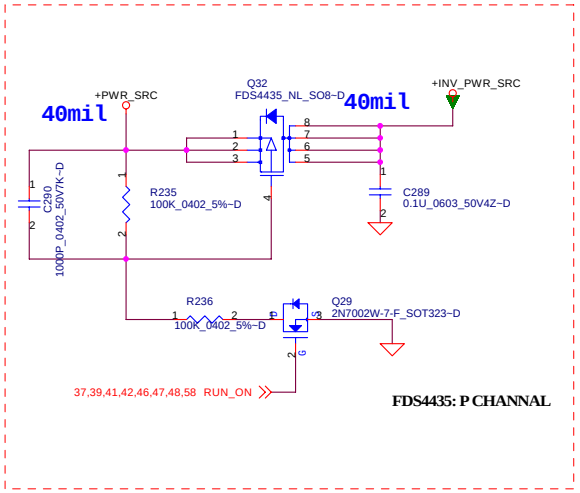


BACKLITEON for D'05;
BIA_PWM for M'07



X01 support M07 inverter

M'07 inverter support - Populate R520,R1767 Depop U7.
D'05 inverter support - Populate U7, Depop R520,R1767



Compal Electronics, Inc.

Title: Internal LVDS

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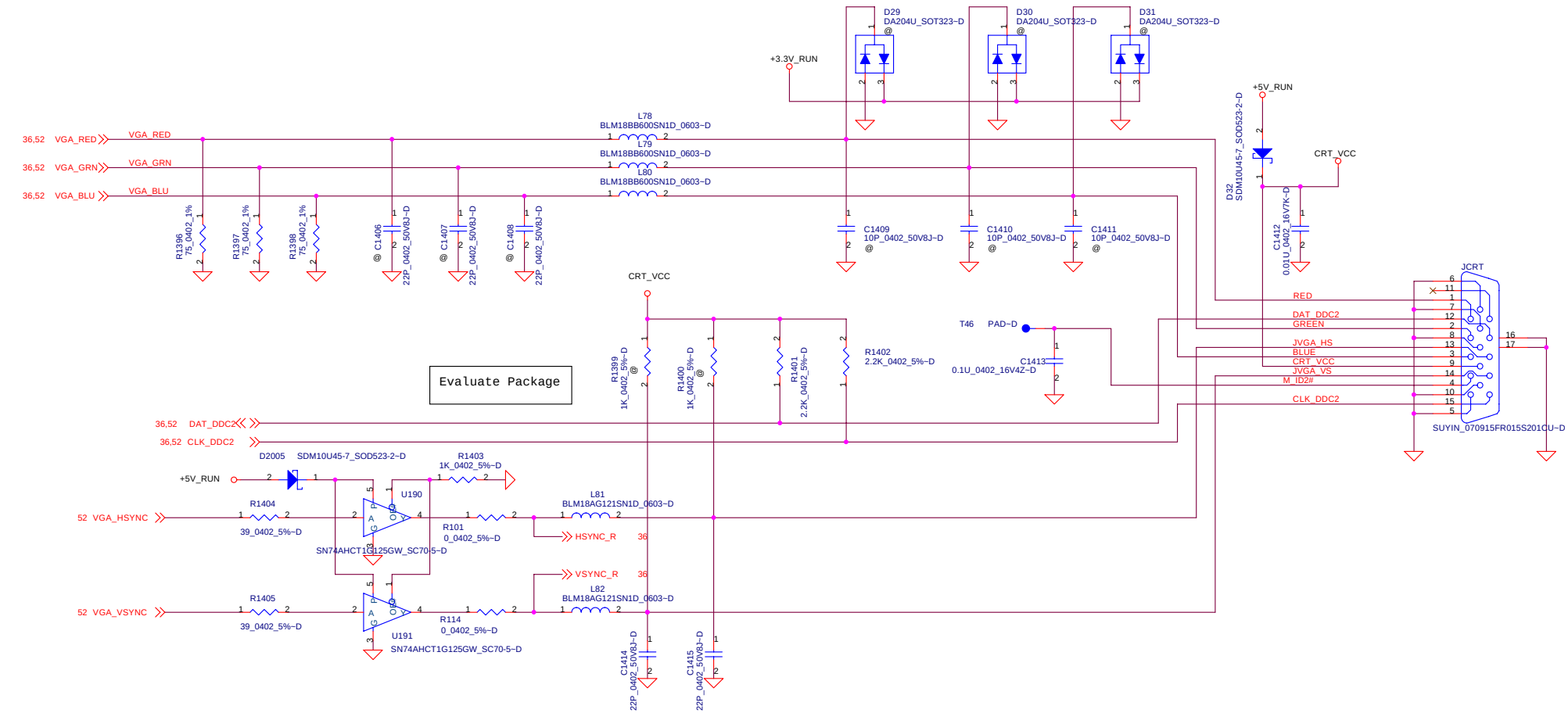

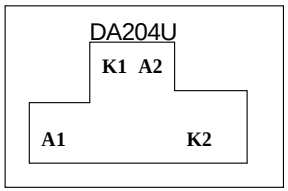

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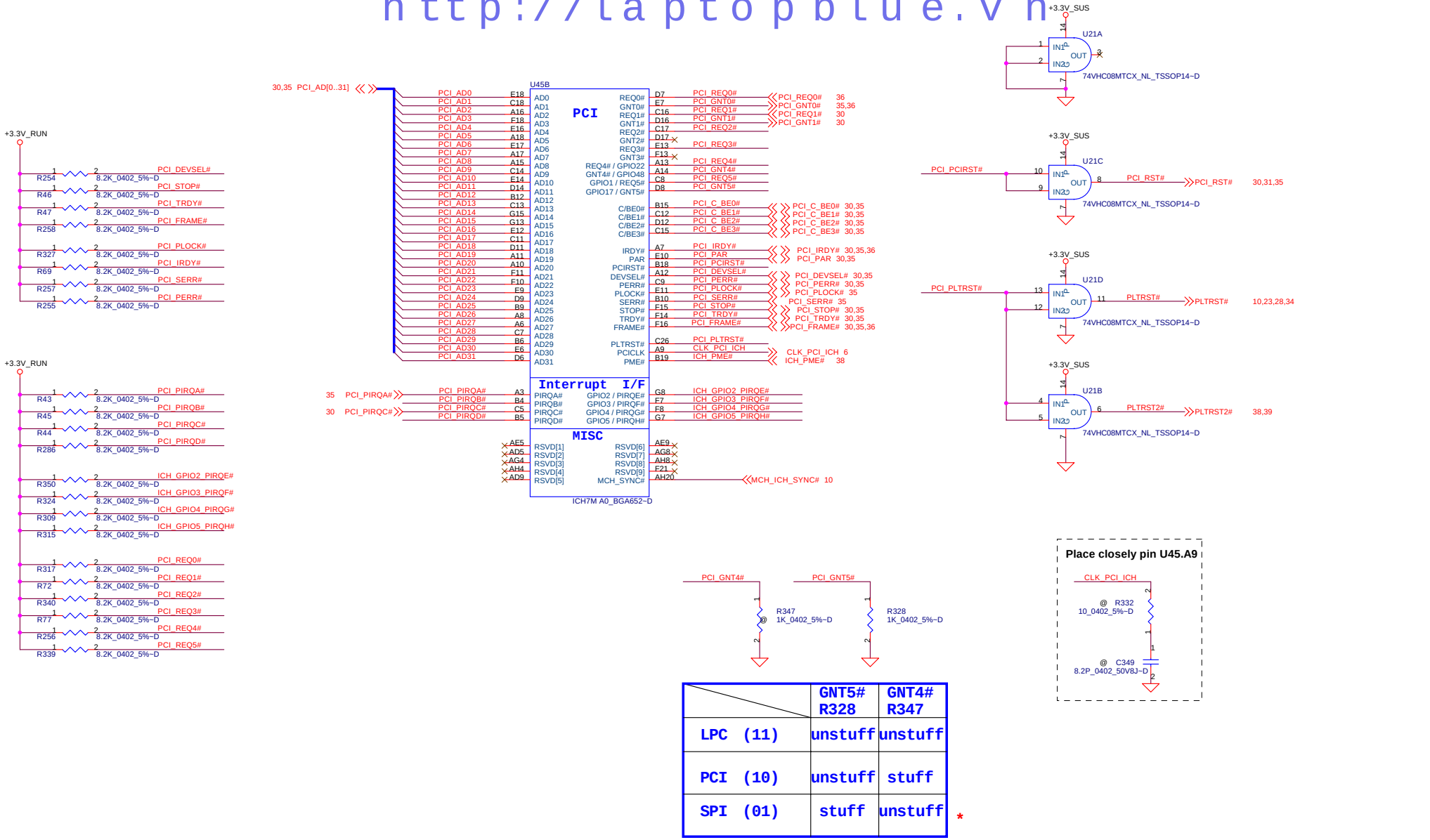
Compal Electronics, Inc.

Title: CRT

Size | Document Number: LA-2792 | Rev: 1.0

Date: Tuesday, February 07, 2006 | Sheet 20 of 70



	GNT5# R328	GNT4# R347
LPC (11)	unstuff	unstuff
PCI (10)	unstuff	stuff
SPI (01)	stuff	unstuff *

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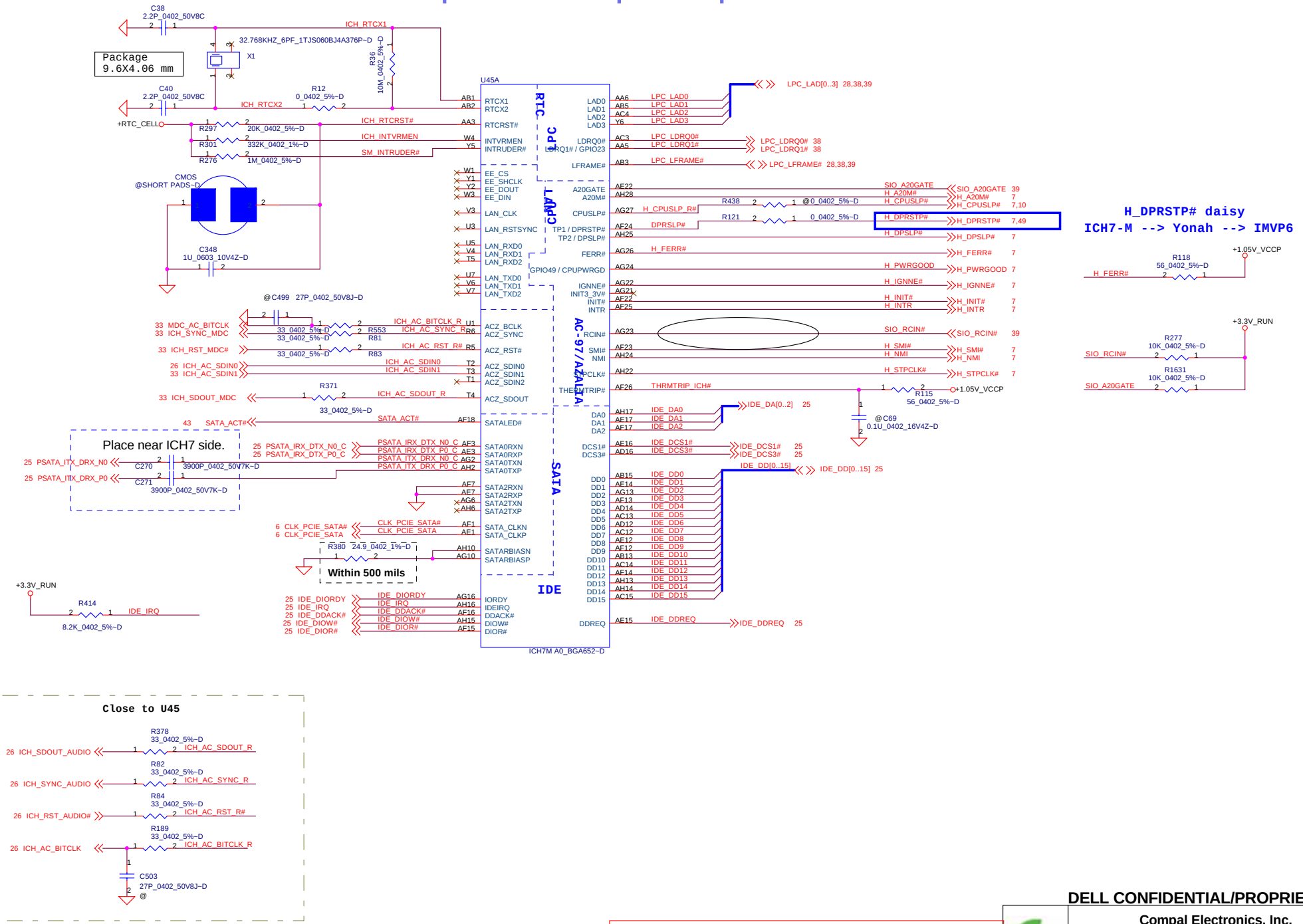
Compal Electronics, Inc.

Title: ICH7(1/4)

Size: | Document Number: LA-2792 | Rev: 1.0

Date: Tuesday, February 07, 2006 | Sheet 21 of 70



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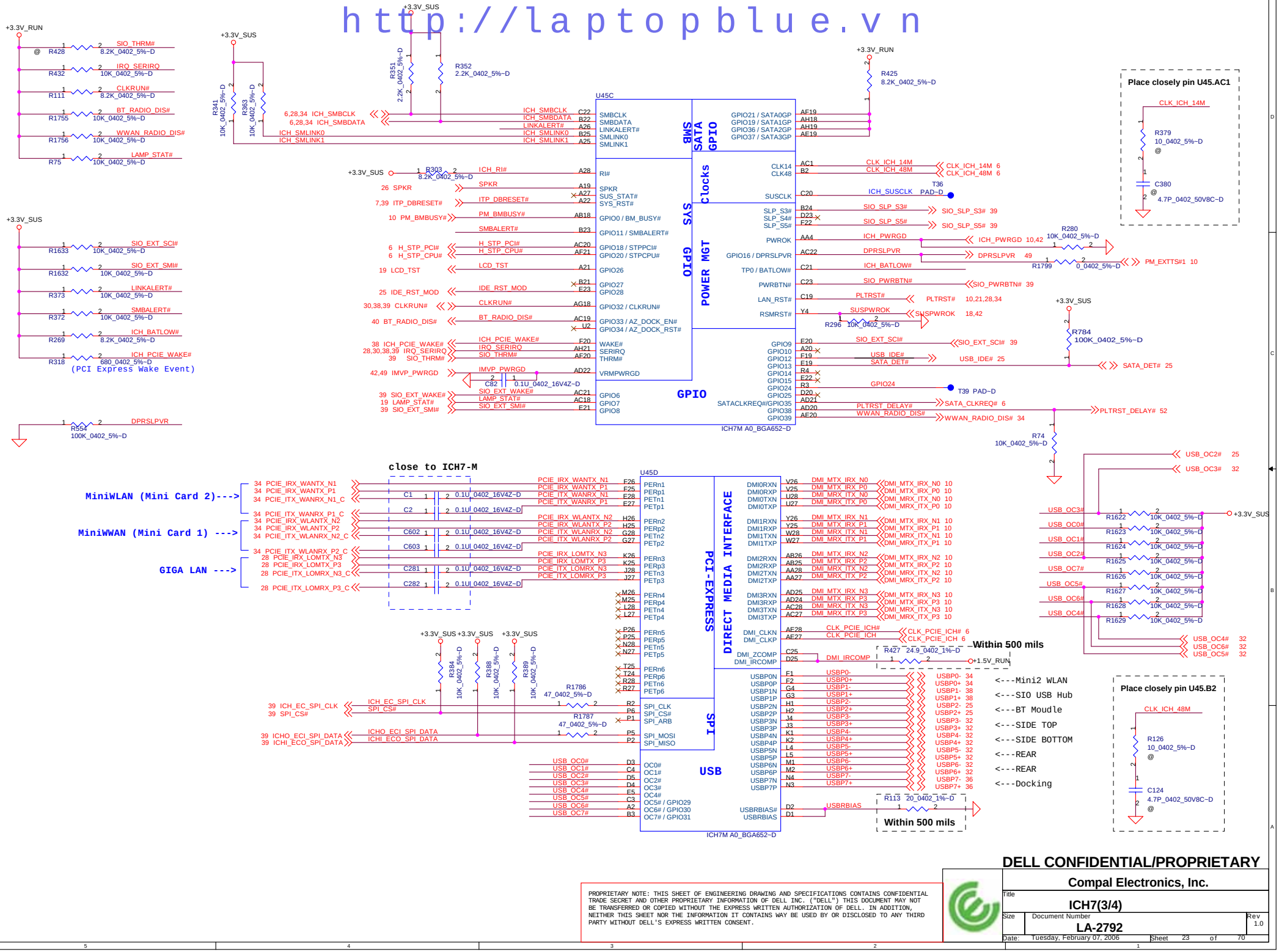
Compal Electronics, Inc.	
Title	ICH7(2/4)
Size	Document Number: LA-2792
Rev	1.0
Date: Tuesday, February 07, 2006	Sheet 22 of 70

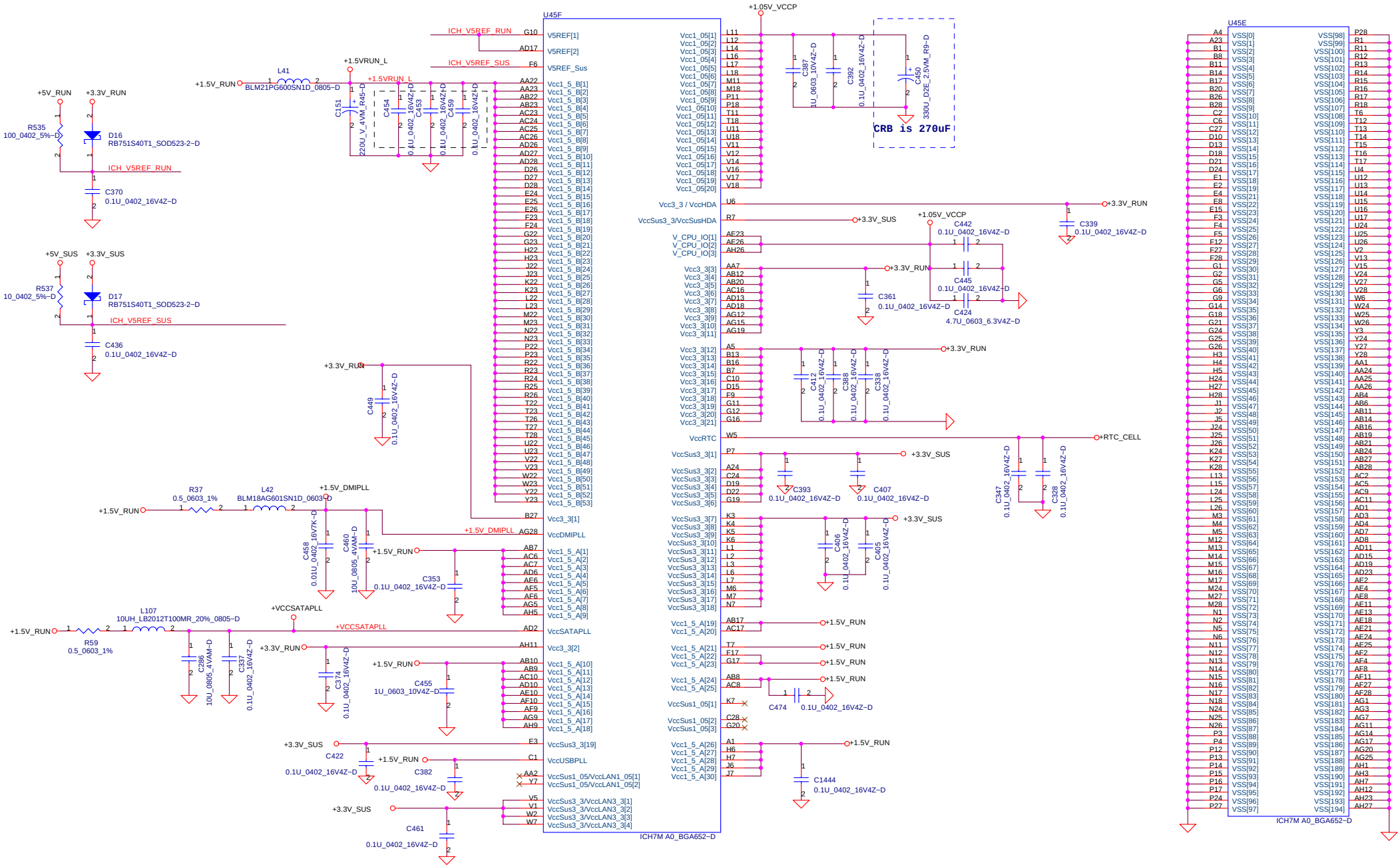


Compal Electronics, Inc.

Title: ICH7(3/4)

Size: | Document Number: LA-2792 | Rev: 1.0

Date: Tuesday, February 07, 2006 | Sheet 23 of 70



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Title: ICH7(4/4)		
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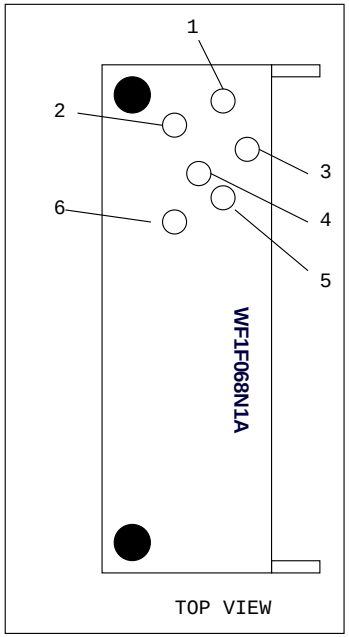

JMOD

TYCO_1770530-1-D

22 IDE_DD[0..15]
IDE_DD0 IDE_DD1 IDE_DD2 IDE_DD3 IDE_DD4 IDE_DD5 IDE_DD6 IDE_DD7 IDE_DD8 IDE_DD9 IDE_DD10 IDE_DD11 IDE_DD12 IDE_DD13 IDE_DD14 IDE_DD15

22 IDE_DA[0..2]
IDE_DA0 IDE_DA1 IDE_DA2

22 IDE_DCS1#
22 IDE_DCS3#
IDE_DCS1# IDE_DCS3#

22 IDE_DDACK#
IDE_DDACK#

22 IDE_DIOR#
22 IDE_DIOW#
22 IDE_DIORDY
22 IDE_DDREQ
22 IDE_IRQ
IDE_DIOR# IDE_DIOW# IDE_DIORDY IDE_DDREQ IDE_IRQ

23 IDE_RST_MOD
IDE_RST_MOD
R1329 33_0402_5%~D
MOD_RST

23 USB_IDE#
USB_IDE#
R1330 100K_0402_5%~D
+3.3V_SUS

38 BAY_MODPRES#
BAY_MODPRES#

+3.3V_ALW
R1331 100K_0402_5%~D

R1328 470_0402_5%~D
CSEL2

IDE_DCS3#
IDE_DA2
IDE_DA0
IDE_DA1
IDE_DIOR#
IDE_DIOW#
IDE_DD15
IDE_DD1
IDE_DD2
IDE_DD12
IDE_DD11
IDE_DD5
IDE_DD6
IDE_DD8

+5VHDD
C1302 4.7U_0603_6.3V4Z~D
C1303 0.1U_0402_16V4Z~D
C1304 0.1U_0402_16V4Z~D
C1305 0.1U_0402_16V4Z~D

SATA_DET# — SATA_DET# 23
USB_OC2# — USB_OC2# 23
USBP2+ — USBP2+ 23
USBP2- — USBP2- 23
DASP#
IDE_DCS1#
PDIAG#
IDE_IRQ
IDE_DDACK#
IDE_DIORDY
IDE_DDREQ
IDE_DD0
IDE_DD14
IDE_DD13
IDE_DD3
IDE_DD4
IDE_DD10
IDE_DD9
IDE_DD7

+3.3V_RUN
R512 4.7K_0402_5%~D
IDE_DIORDY

+5VHDD
C1310 10U_0805_10V4Z~D
C1311 1000P_0402_50V7K~D
C1312 0.1U_0402_16V4Z~D
C1313 1U_0603_10V4Z~D
C1314 0.1U_0402_16V4Z~D
Please near HD CONN

+3.3V_RUN
@ C1315 10U_0805_10V4Z~D
@ C1316 1000P_0402_50V7K~D
@ C1317 0.1U_0402_16V4Z~D
@C1318 1U_0603_10V4Z~D
@ C1345 0.1U_0402_16V4Z~D
Please near HD CONN

C1319 3900P_0402_50V7K~D
22 PSATA_IRX_DTX_N0_C
22 PSATA_IRX_DTX_P0_C
C1323 3900P_0402_50V7K~D
close SATA connector

JSATA
22 PSATA_ITX_DRX_P0
22 PSATA_ITX_DRX_N0
PSATA_ITX_DRX_P0
PSATA_ITX_DRX_N0
PSATA_IRX_DTX_N0
PSATA_IRX_DTX_P0
GND RX+ RX- GND TX- TX+ GND
+3.3V_RUN
3.3V 3.3V 3.3V GND GND GND 5V 5V 5V GND Reserved GND 12V 12V 12V
GND1 GND2
TYCO_1775191-1_RV~D
+5VHDD
Main SATA +5V Default

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Title: DVD MODULE

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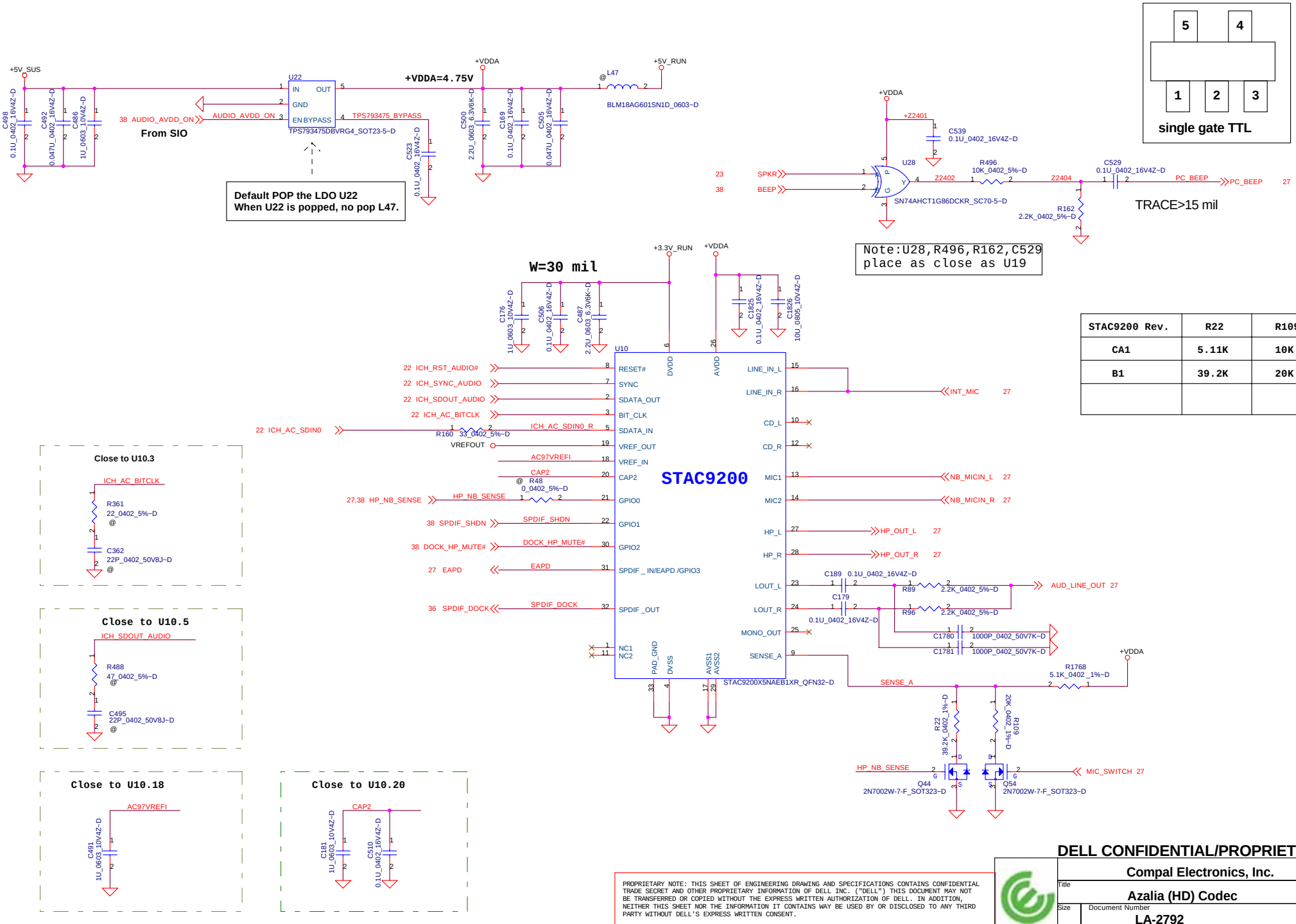

STAC9200 Rev.	R22	R109
CA1	5.11K	10K
B1	39.2K	20K

Compal Electronics, Inc.

Title: Azalia (HD) Codec

Size: | Document Number: LA-2792 | Rev: 1.0

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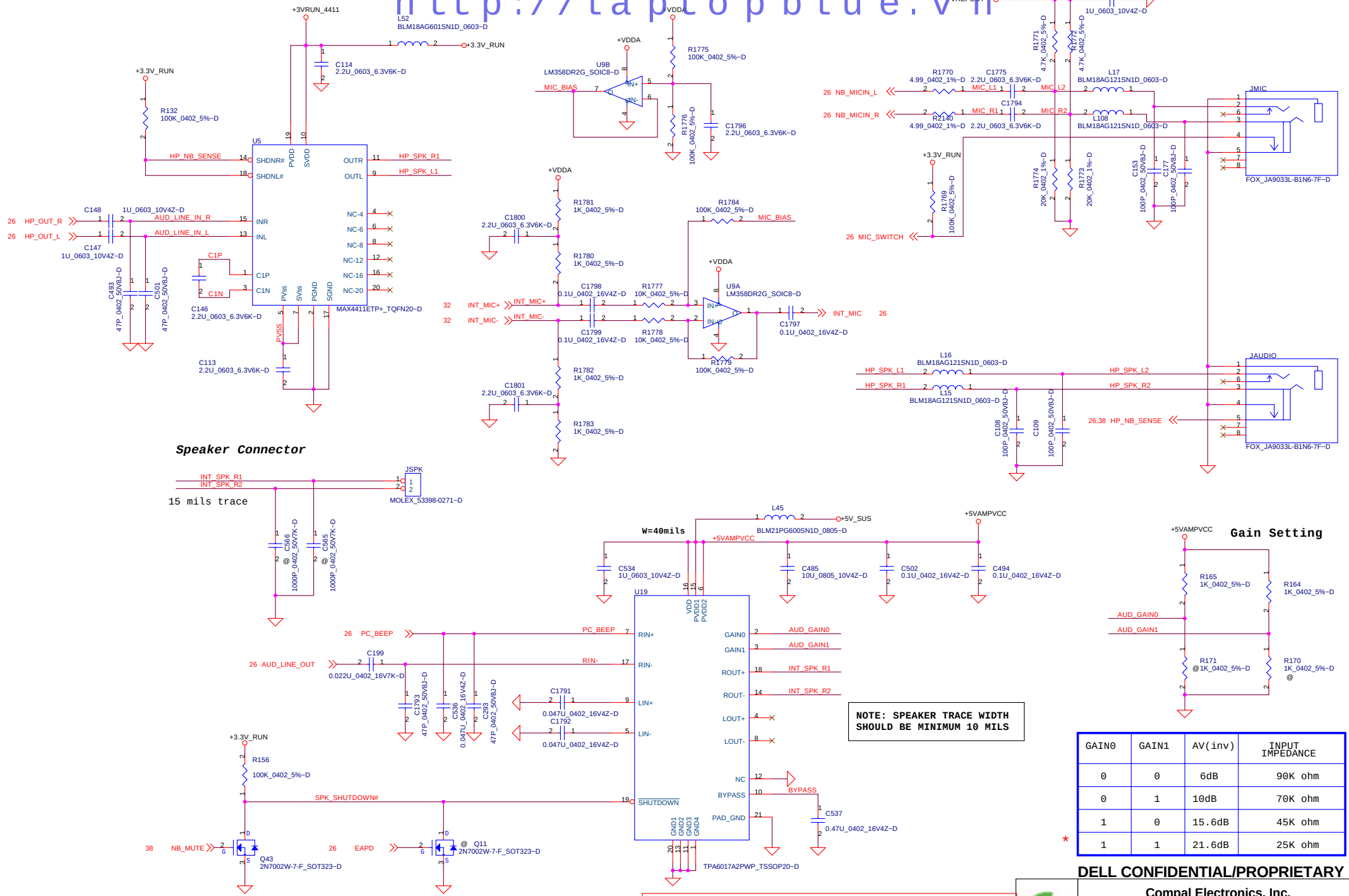

GAIN0	GAIN1	AV(inv)	INPUT IMPEDANCE
0	0	6dB	90K ohm
0	1	10dB	70K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	25K ohm

*

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Compal Electronics, Inc.

Title: AMP and PHONE JACK

Size: | Document Number: LA-2792 | Rev: 1.0

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Layout Notice : Place as close chip as possible.

MMJT9435

R7, R9 are 1/2 W rating

Pop C1375 for 5752-A0,
De-pop for 5752-A1

Layout Notice : 1.2V filter. Place as close chip as possible.

Place closely pin J8

Layout Notice : No high speed signal should be routed near RDAC or on adjacent layer to RDAC

	NV_STRAP1	NV_STRAP0	SO	SI	CS#	SCLK
Atmel AT45BCM021B	0	0	1	0	1	1
ST M45PE20	0	1	1	0	0	1

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Title: BCM5751M

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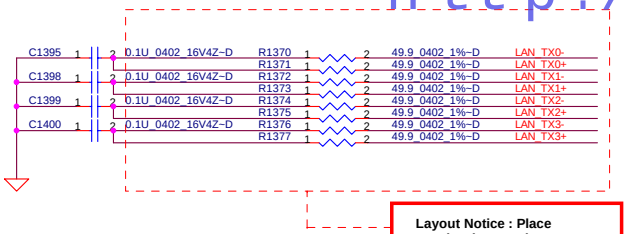
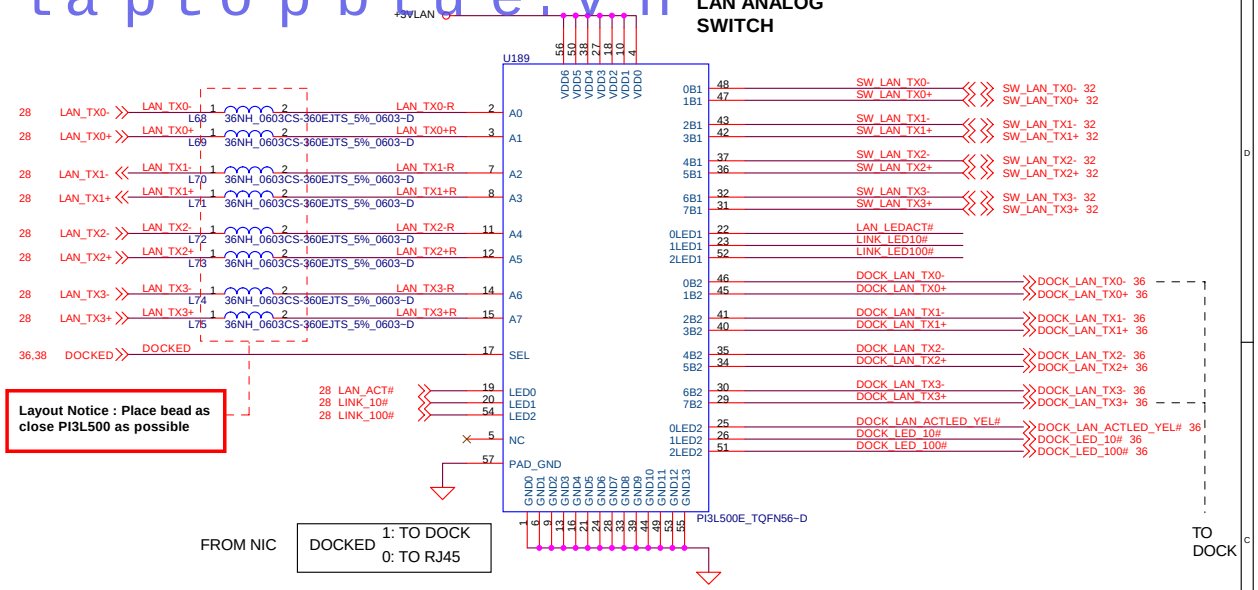


Layout Notice : Place termination as close as ASIC as possible

The resistors need at least 1/16W

LAN ANALOG SWITCH

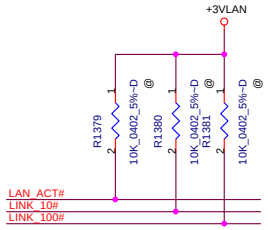


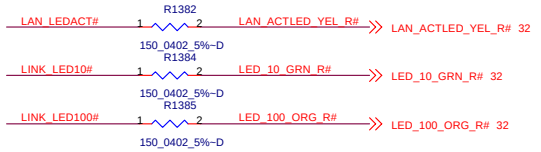
Layout Notice : Place bead as close PI3L500 as possible

FROM NIC

DOCKED 1: TO DOCK 0: TO RJ45

TO DOCK





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Title: **LAN TRANSFOMER**

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NOTE:
THIS PAGE SHOWS THE OZ601B CONFIGURED WITH
EXTERNAL IDSEL AND WITHOUT 12V VPP SUPPORT.

IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)

NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME.
IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE
PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE
REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO
SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS.
THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS
FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY
CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST
BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127

22K TO 47K PULL-UPS MUST BE PLACED
ON INTA#, PME#, SERIRQ# & CLKRUN#.

Place closely pin 26
CLK_PCI_PCM
R88 22_0402_5%~D @
C81 22P_0402_50V8J~D @

U193 OZ601TN_TQFP128~D
U2 OZ2522LN-A1_QFN32~D
JCBUS TYCO_1734648-1~D

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Title: Card Bus OZ601
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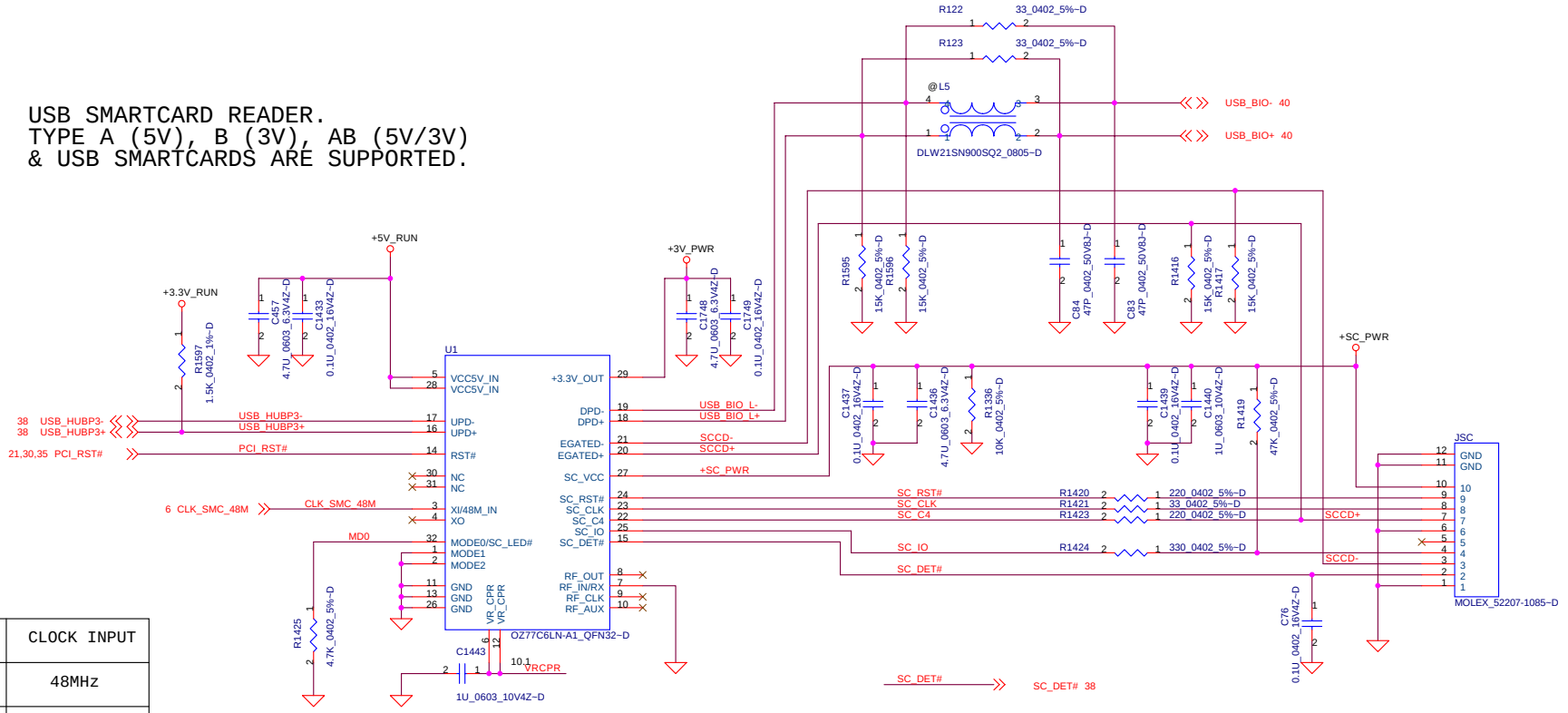
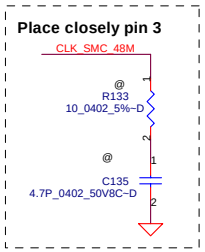
USB SMARTCARD READER.
TYPE A (5V), B (3V), AB (5V/3V)
& USB SMARTCARDS ARE SUPPORTED.



MODE1	CLOCK INPUT
LOW	48MHz
HIGH	6MHz Crystal



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Compal Electronics, Inc.

Title: Smart Card OZ77C6

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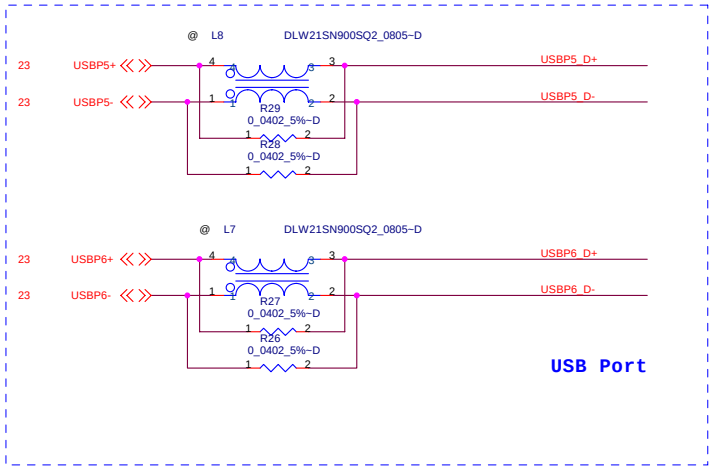

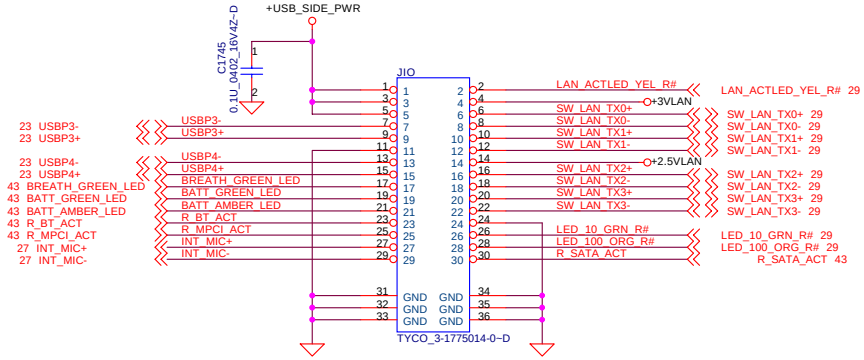

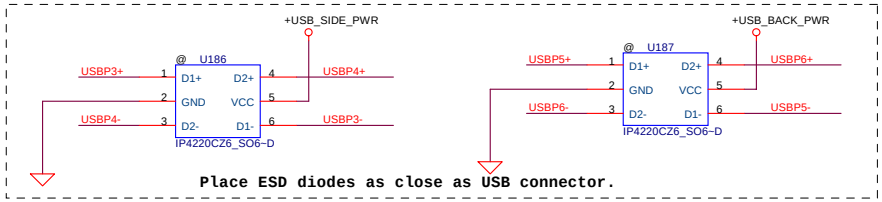

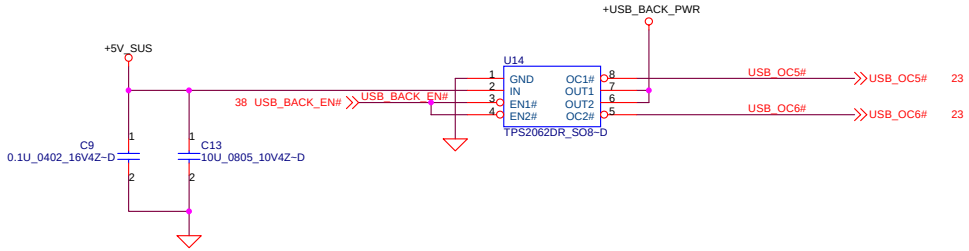

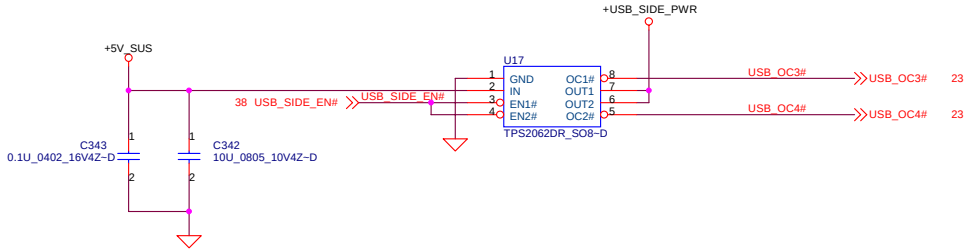

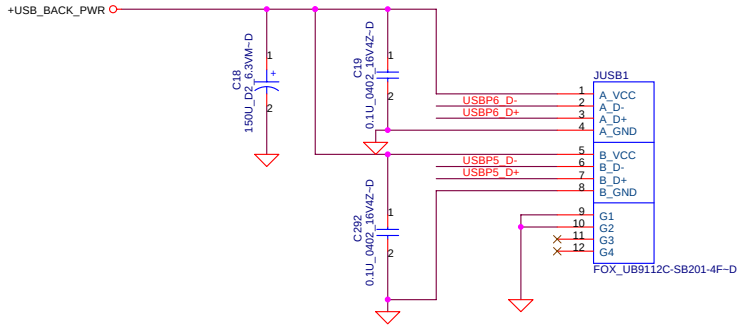

Rear USB Ports

Compal Electronics, Inc.

Title: USB 2.0 Port

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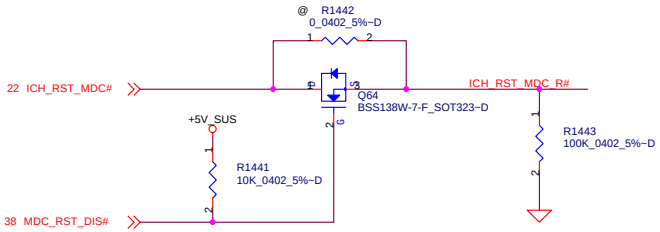
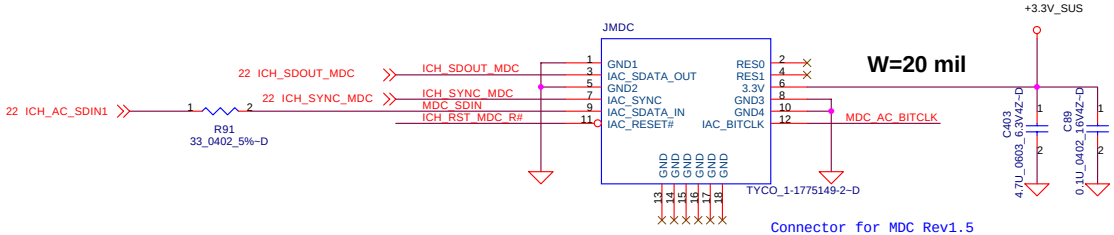
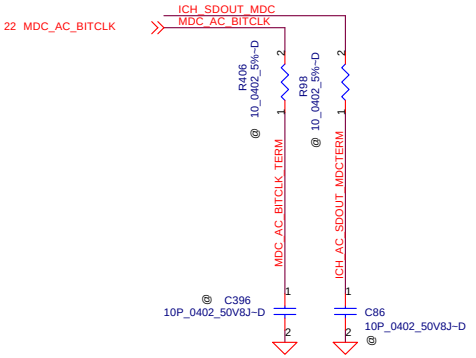


New MDC connector.

1	GND	RES	2
3	IAC_SDATA0	RES	4
5	GND	3.3V	6
7	IAC_SYNC	GND	8
9	IAC_SDATAIN	GND	10
11	IAC_RESET#	IAC_BITCLK	12





Compal Electronics, Inc.

Title: BT PORT and MDC

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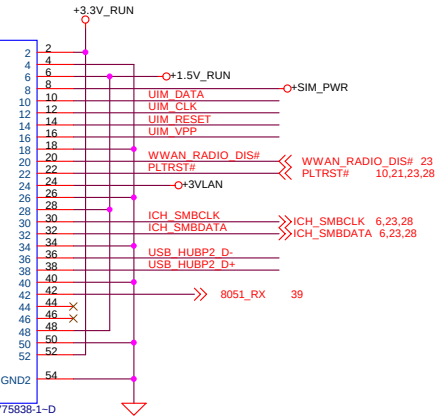
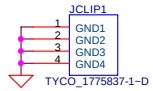
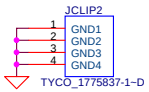
Mini Card
Wire less WAN



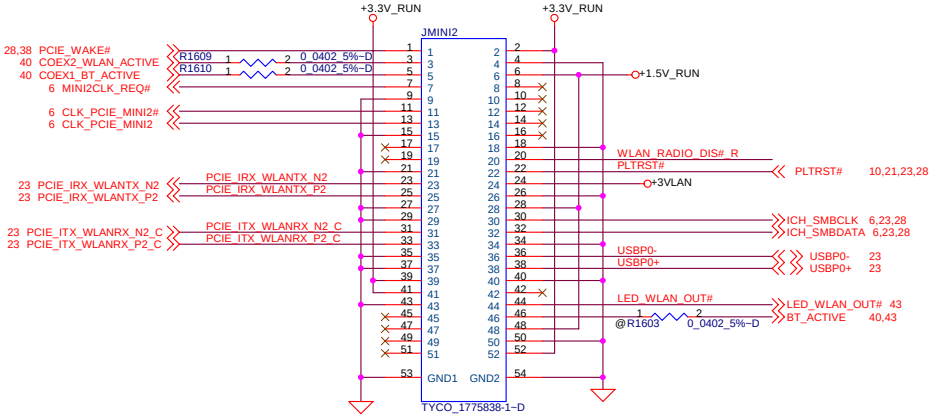


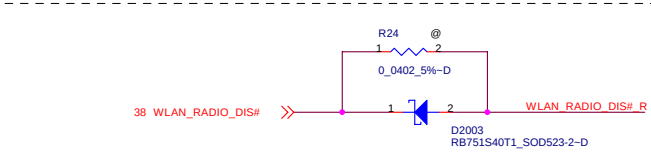
Mini-Card Latch

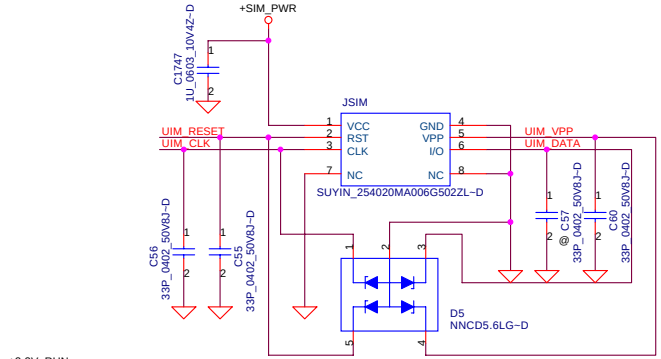


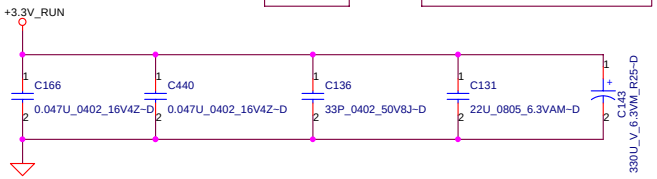
Mini-Card Latch

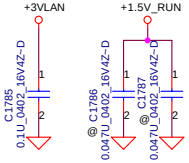
Mini Card
Wire less LAN



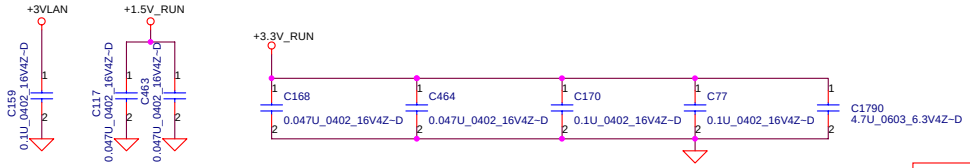








PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA



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Compal Electronics, Inc.

Title: Mini Card

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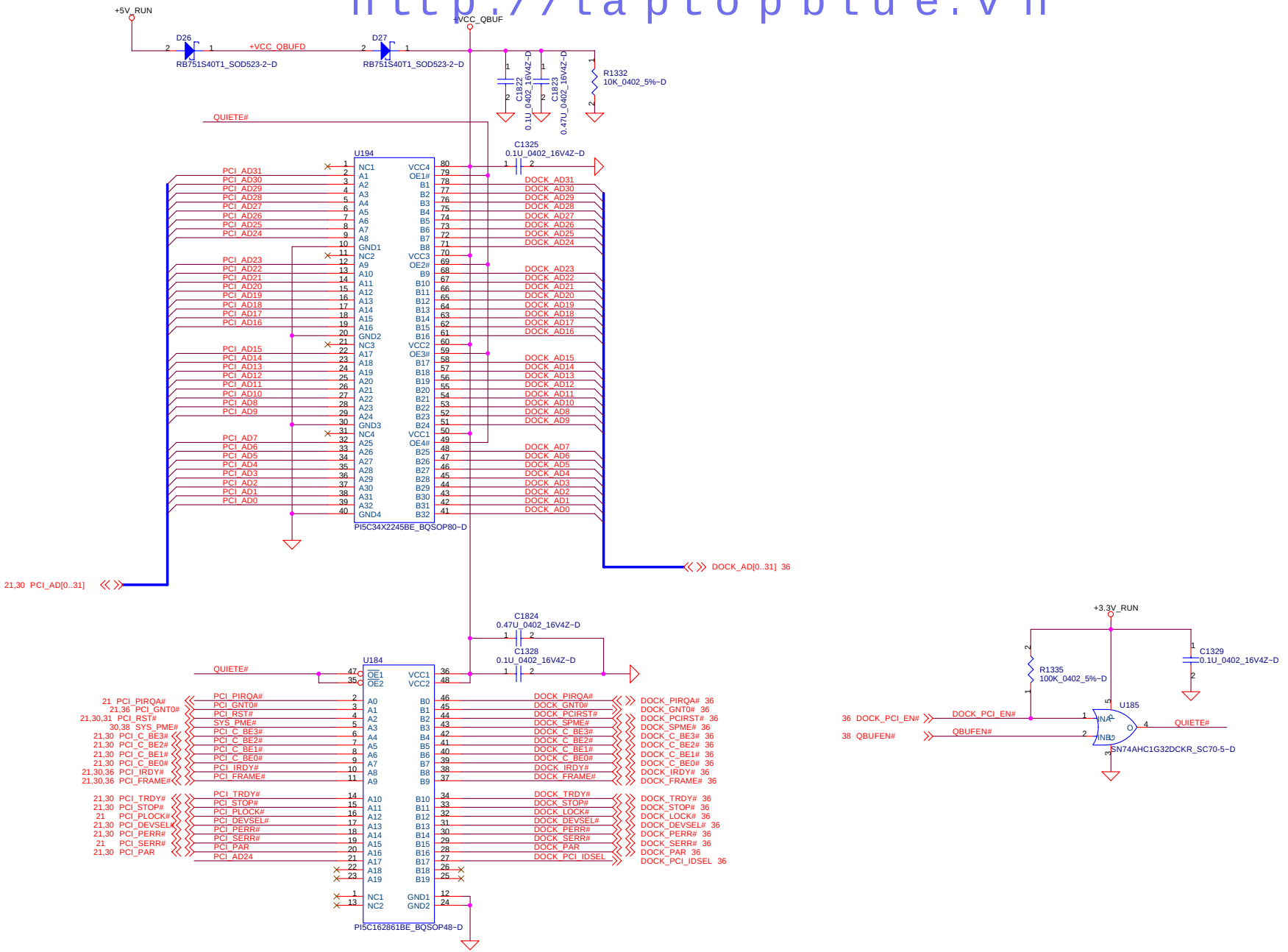

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Title: **DOCKING BUFFER**

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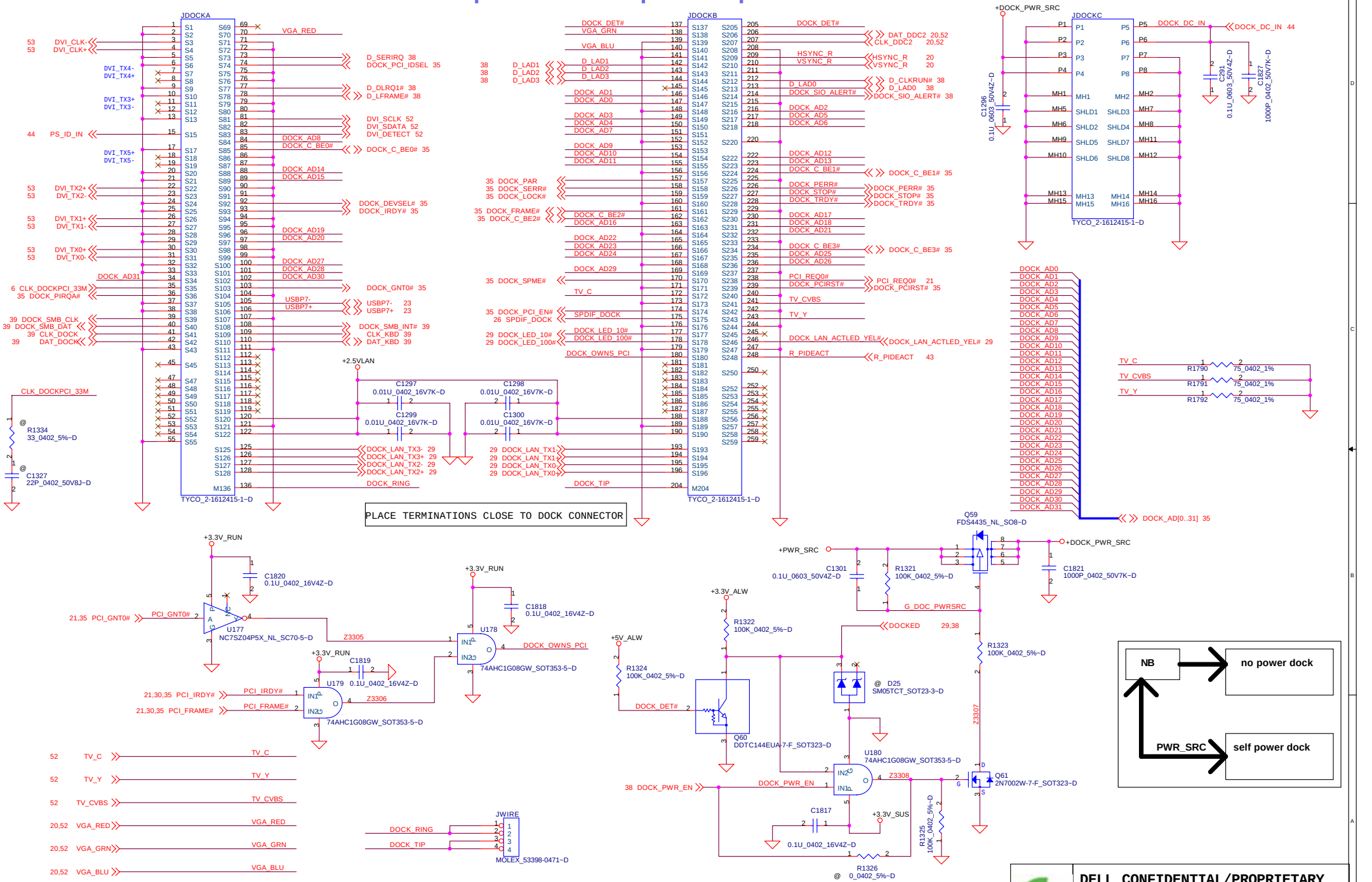

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Title: **DOCKING CONN.**

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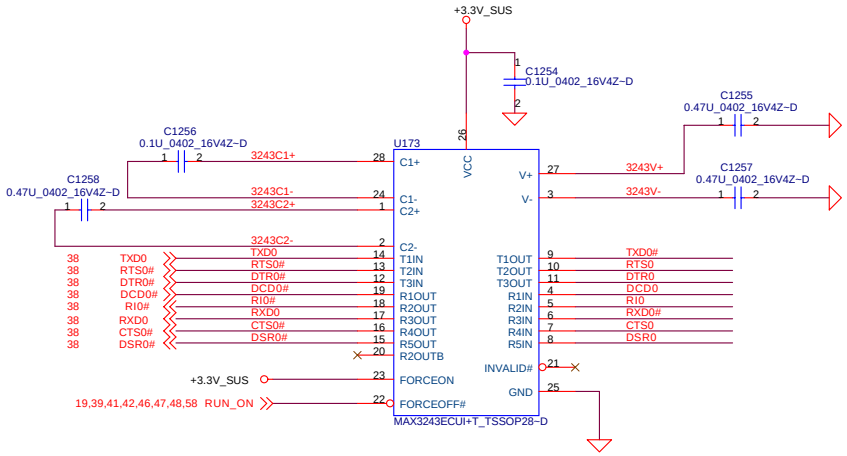

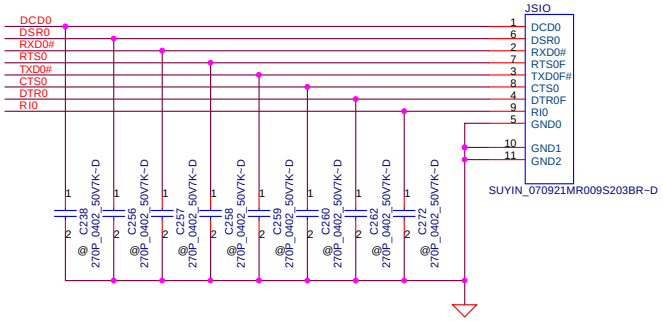

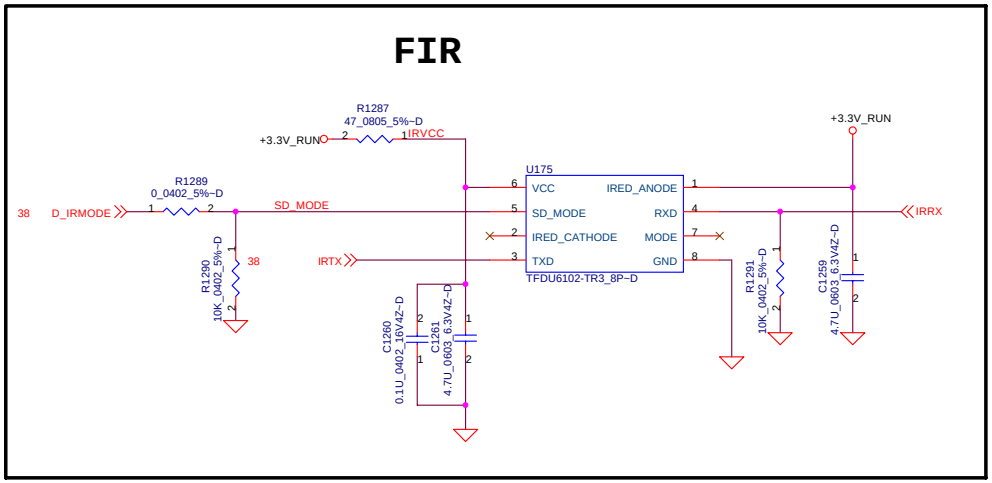

Compal Electronics, Inc.

Title: Serial & FIR

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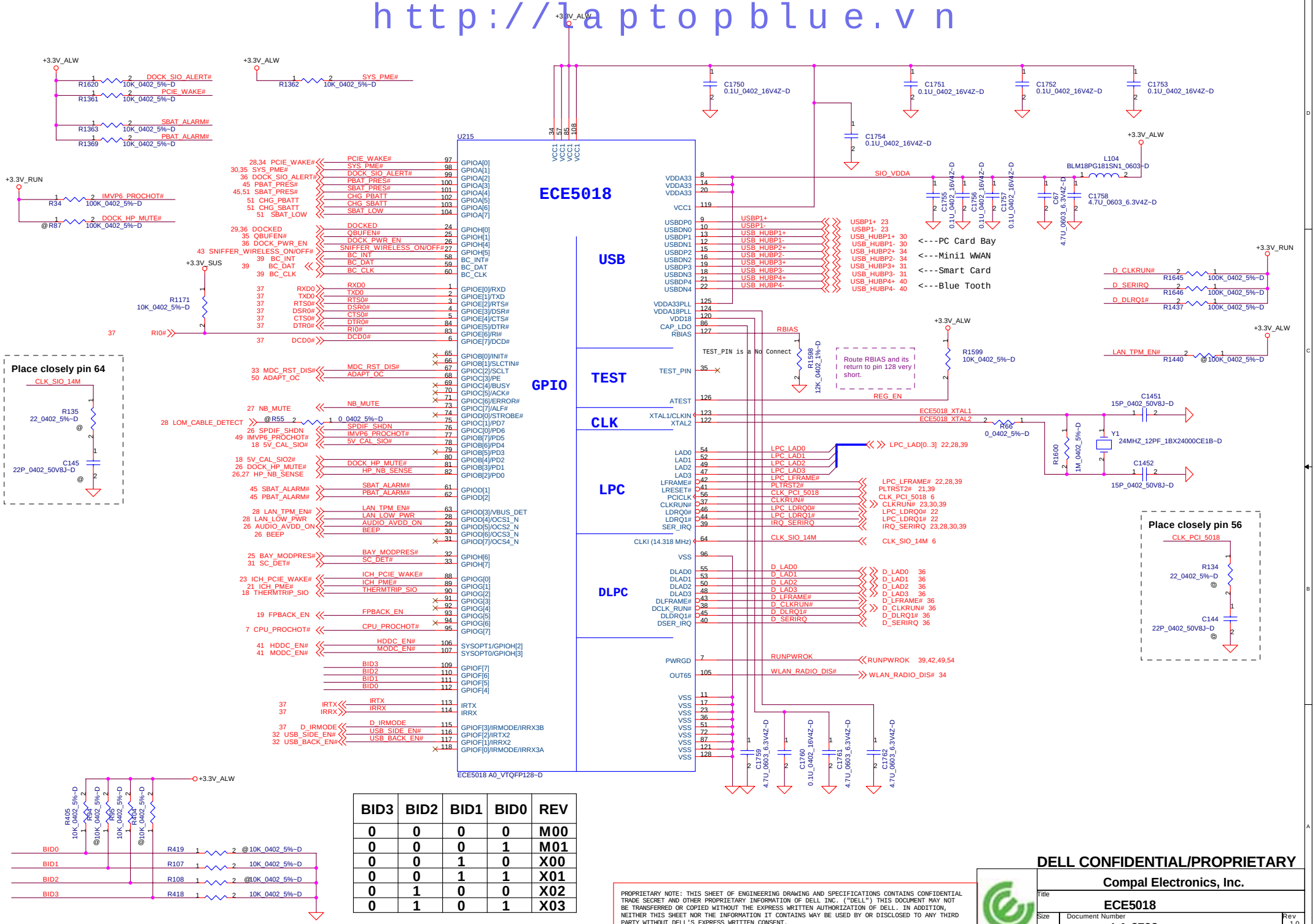

BID3	BID2	BID1	BID0	REV
0	0	0	0	M00
0	0	0	1	M01
0	0	1	0	X00
0	0	1	1	X01
0	1	0	0	X02
0	1	0	1	X03

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Compal Electronics, Inc.

Title: ECE5018

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U216

Keyboard and Mouse Interface

PWR SW

LPC Interface

Host/8051

BC Buss

MEC5004_VTQFP128~D

R1752 no stuff when doing flash recovery

Place closely pin 58

32 KHz Clock

Same as Laguna

Work Around

Bat2 = Amber LED
Bat1 = Green LED
20mA drive pins

1 = Discrete Gfx
0 = UMA

1=Flash Recovery Enabled
0=Flash Recovery Disabled

low=write protected

Flash write protect bottom 4K
of internal bootblock flash

Flash ROM
150 MIL SO8

200 MIL SO8

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Compal Electronics, Inc.

Title: EMC5004

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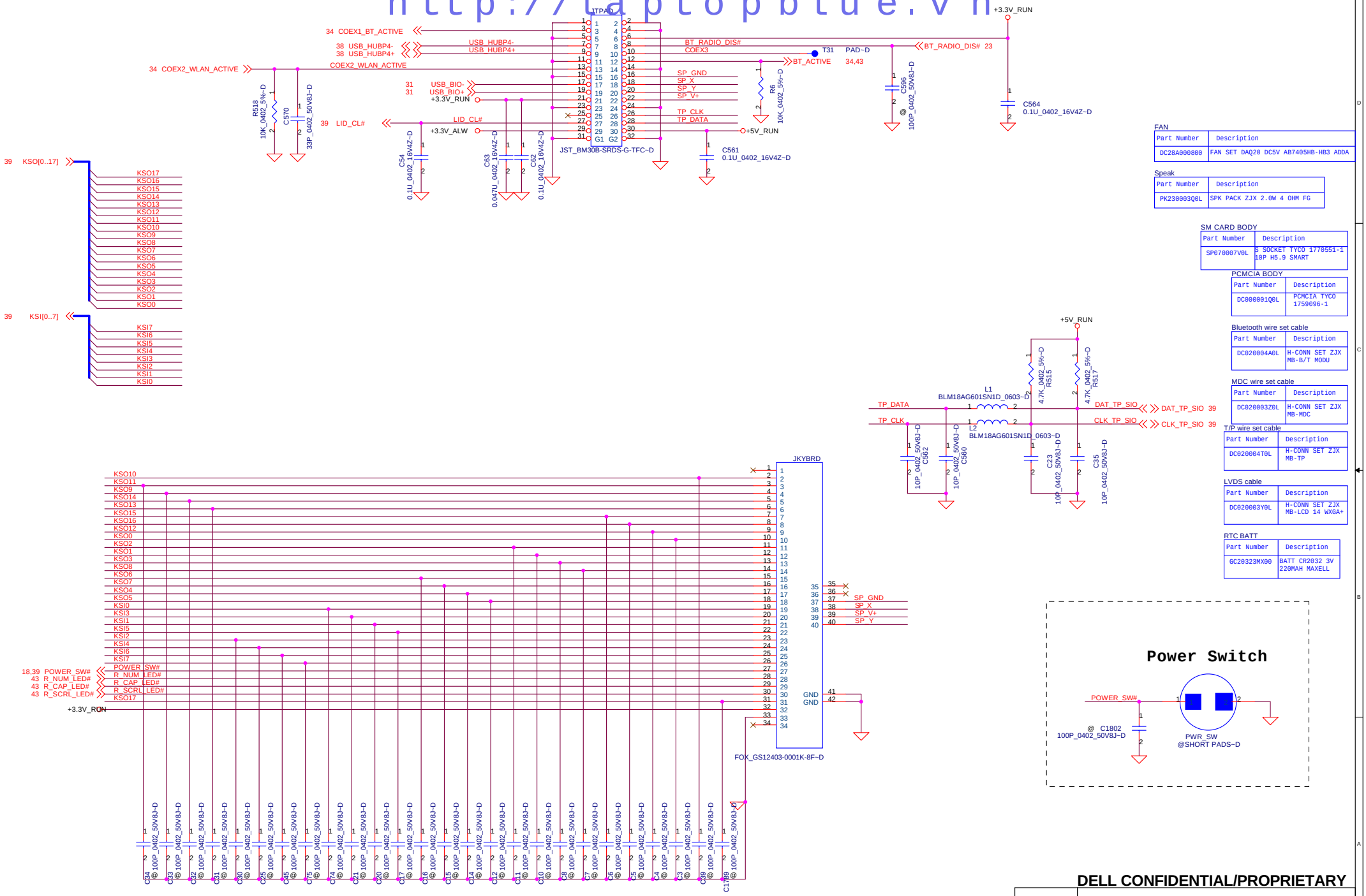

FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

SM CARD BODY

Part Number	Description
SP070007V0L	S SOCKET TYCO 1770551-1 10P H5.9 SMART

PCMCIA BODY

Part Number	Description
DC000001Q0L	PCMCIA TYCO 1759096-1

Bluetooth wire set cable

Part Number	Description
DC020004A0L	H-CONN SET ZJX MB-B/T MODU

MDC wire set cable

Part Number	Description
DC020003Z0L	H-CONN SET ZJX MB-MDC

T/P wire set cable

Part Number	Description
DC020004T0L	H-CONN SET ZJX MB-TP

LVDS cable

Part Number	Description
DC020003Y0L	H-CONN SET ZJX MB-LCD 14 WXGA+

RTC BATT

Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

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Compal Electronics, Inc.

Title	INT KB	
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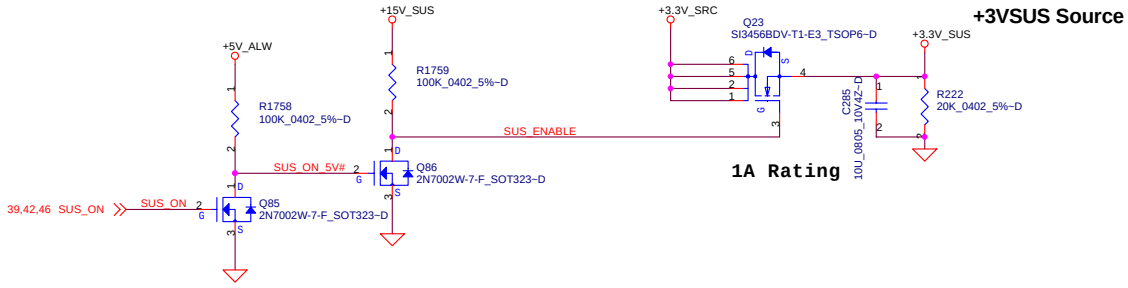
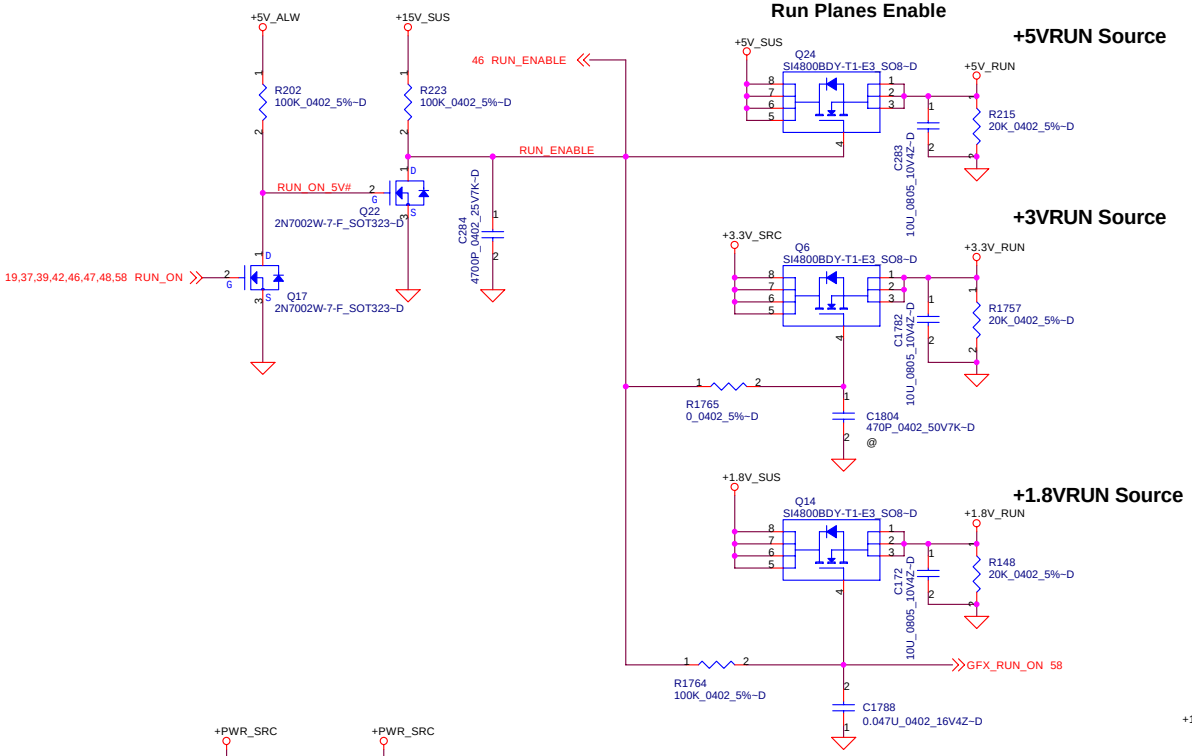
DC/DC Interface

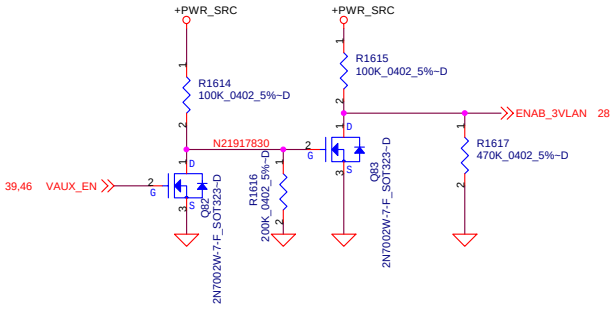
+3VSUS Source

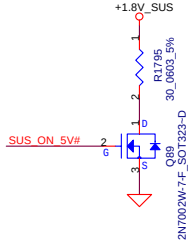


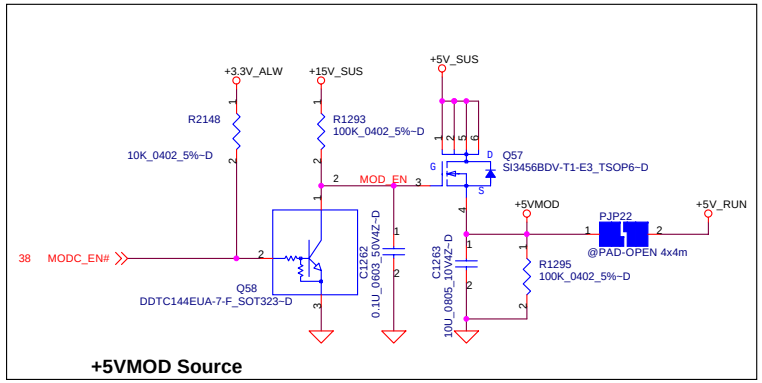
Run Planes Enable

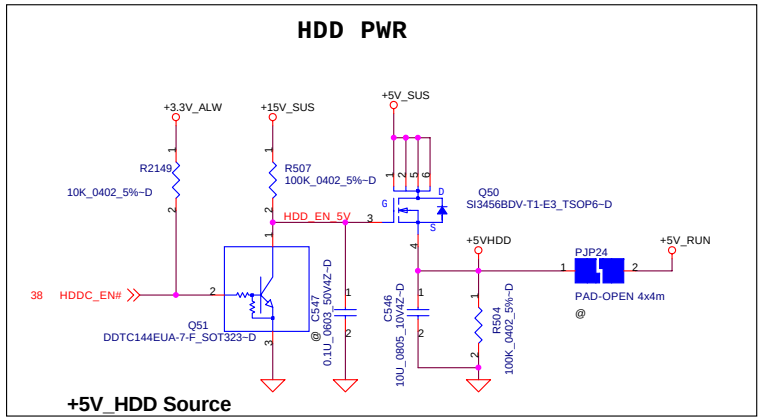
+5VRUN Source



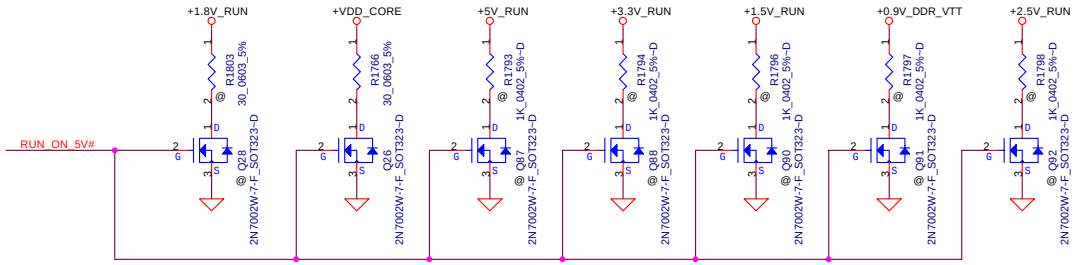








Discharg Circuit



Compal Electronics, Inc.

Title: POWER CONTROL

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For EMI

+3.3V_RUN @C1806 +1.8V_SUS 0.047U_0402_16V4Z~D
+3.3V_RUN @C1807 +3.3V_SUS 0.047U_0402_16V4Z~D
+3.3V_RUN @C1808 +1.5V_RUN 0.047U_0402_16V4Z~D
+1.5V_RUN @C1809 +1.05V_VCCP 0.047U_0402_16V4Z~D
+3.3V_RUN @C1814 +SDC_IN 0.047U_0402_16V4Z~D
+3.3V_RUN @C1812 0.047U_0402_16V4Z~D
+3.3V_RUN @C1813 0.047U_0402_16V4Z~D
+3.3V_RUN C1810 +SDC_IN 0.047U_0402_25V4Z~D
+PWR_SRC C1811 +3.3V_SUS 0.047U_0402_25V4Z~D

18 2.5V_RUN_PWRGD R49 0_0402_5%~D
47 1.5V_RUN_PWRGD R313 0_0402_5%~D
47 1.05V_RUN_PWRGD R319 0_0402_5%~D
48 0.9V_DDR_PWRGD R334 0_0402_5%~D
58 GFX_CORE_PWRGD R2170 0_0402_5%~D
58 GFX_PCIE_PWRGD @ R2171 0_0402_5%~D

+3.3V_RUN R494 20K_0402_5%~D 3VRUNRC
C520 0.01U_0402_16V7K~D
+3.3V_SUS C483 0.1U_0402_16V4Z~D
U24A 74LVC3G14DC_VSSOP8~D
+3.3V_SUS U24B 74LVC3G14DC_VSSOP8~D
+3.3V_SUS C480 0.1U_0402_16V4Z~D
U26A 74VHC08MTCX_NL_TSSOP14~D
19,37,39,41,46,47,48,58 RUN_ON
+3.3V_SUS U26D 74VHC08MTCX_NL_TSSOP14~D
RUNPWROK RUNPWROK 38,39,49,54

48 SUSPWROK_1P8V
+3.3V_ALW R1383 100K_0402_5%~D
R1386 10K_0402_5%~D
Q7 2N7002W-7-F_SOT323~D
C1816 0.1U_0402_16V4Z~D
39,41,46 SUS_ON
+3.3V_SUS U24C 74LVC3G14DC_VSSOP8~D
+3.3V_SUS U26C 74VHC08MTCX_NL_TSSOP14~D
SUSPWROK 18,23

23,49 IMVP_PWRGD IMVP_PWRGD
39 RESET_OUT# RESET_OUT#
+3.3V_SUS U26B 74VHC08MTCX_NL_TSSOP14~D
R463 0_0402_5%~D ICH_PWRGD 10,23

+3.3V_SUS R453 100K_0402_5%~D
ICH_PWRGD# ICH_PWRGD# 18
ICH_PWRGD Q41 2N7002W-7-F_SOT323~D

COIN RTC Battery

+COINCELL R471 1K_0402_5%~D
+3.3VX Z4012
+RTC_CELL
D15 BAT54CW_SOT323~D
C528 1U_0603_10V4Z~D
+COINCELL COINCELL JCOIN MOLEX_53398-0271~D

Compal Electronics, Inc.

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H1 H_T146B217D91 | H2 H_T146B217D91 | H3 @H_C315D110 | H4 H_T256B63D47 | H5 @H_C315D110 | H6 @H_C236B256D110 | H7 @H_C315D110 | H8 @H_T217B315D98 | H9 @H_C315D110 | H10 @H_C315D110

H11 @H_T315B237D118 | H12 @H_C315D118 | H13 @H_C315D118 | H14 @H_T315B237D118 | H15 @H_C315D118 | H16 @H_T217B315D98 | H17 @H_T217B315D98 | H18 @H_C217D91 | H19 @H_C217D91 | H20 @H_T217B315D98

@H_O115X31D115X31N

H31 @H_C24D24N | H32 @H_C24D24N | H26 @H_C472D376 | H27 @H_C472D431X376 | H28 @H_O115X31D115X31N | H29 | H30 @H_O115X31D115X31N

EMI CLIP

CLIP1 @ EMI_CLIP — GND
CLIP2 @ EMI_CLIP — GND
CLIP4 @ EMI_CLIP — GND
CLIP3 @ EMI_CLIP — GND
CLIP5 @ EMI_CLIP — GND
CLIP6 @ EMI_CLIP — GND

Fiducial Mark

FD1 FD2 FD3 FD4 FD5 FD6
FD7 FD8 FD9 FD10 FD11 FD12
FD13 FD14 FD15 FD16 FD17 FD18
FD19 FD20 FD21 FD22 FD23 FD24
FD25
FIDUCIAL MARK~D

39 CAP_LED# — R231 330_0402_5%~D — R_CAP_LED# — R_CAP_LED# 40
39 NUM_LED# — R237 330_0402_5%~D — R_NUM_LED# — R_NUM_LED# 40
39 SCRL_LED# — R21 330_0402_5%~D — R_SCRL_LED# — R_SCRL_LED# 40

Disable HDD LED

+3.3V_RUN
R76 10K_0402_5%~D
R1448 @ 0_0402_5%~D
22 SATA_ACT# — SATA_ACT# — SATA_ACT# R
Q66 BSS138W-7-F_SOT323~D
+3.3V_ALW
R1449 10K_0402_5%~D @
39 SNIFFER_LED_OFF#
+3.3V_RUN
Q1 DDTA114EUA-7-F_SOT323~D
R2 330_0402_5%~D
R_SATA_ACT 32
R_PIDEACT 36

+5V_RUN
Q18 DDTA114EUA-7-F_SOT323~D
R8 1K_0402_5%~D
R_BT_ACT — R_BT_ACT 32
34,40 BT_ACTIVE — BT_ACTIVE
R1434 10K_0402_5%~D
Q4 BSS138W-7-F_SOT323~D
39 SNIFFER_LED_OFF#
Q65 PMST3906_SOT323-3~D

+3.3V_SUS
R3 10K_0402_5%~D
39 BREATH_LED — BREATH_LED_B
Q3 MMST3904-7-F_SOT323~D
R1 56_0402_5%~D
BREATH_GREEN_LED — BREATH_GREEN_LED 32

+3.3V_RUN
34 LED_WLAN_OUT#
Q5 DDTA114EUA-7-F_SOT323~D
R15 100_0402_5%~D
R_MPCI_ACT — R_MPCI_ACT 32

+3.3V_ALW
39 BAT1_LED# — BAT1_LED#
Q2 DDTA114EUA-7-F_SOT323~D
R5 220_0402_5%~D
BATT_GREEN_LED — BATT_GREEN_LED 32

+3.3V_SUS
18 SNIFFER_YELLOW# — SNIFFER_YELLOW#
Q16 DDTA114EUA-7-F_SOT323~D

+3.3V_ALW
R56 10K_0402_5%~D
38 SNIFFER_WIRELESS_ON/OFF# — SNIFFER_WIRELESS_ON/OFF#
JSNIFF
39 SNIFFER# — SNIFFER#
1BS008-13130-7F_4P~D

+3.3V_ALW
39 BAT2_LED# — BAT2_LED#
Q35 DDTA114EUA-7-F_SOT323~D
R265 330_0402_5%~D
BATT_AMBER_LED — BATT_AMBER_LED 32

+3.3V_SUS
18 SNIFFER_GREEN# — SNIFFER_GREEN#
Q13 DDTA114EUA-7-F_SOT323~D
R20 220_0402_5%~D — SNIFFER_Y
R19 220_0402_5%~D — SNIFFER_G
D4 12-22AUYSYGC/S30-A2/TR8_G/Y~D

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Title: PAD and Standoff
Size: | Document Number: LA-2792 | Rev: 1.0
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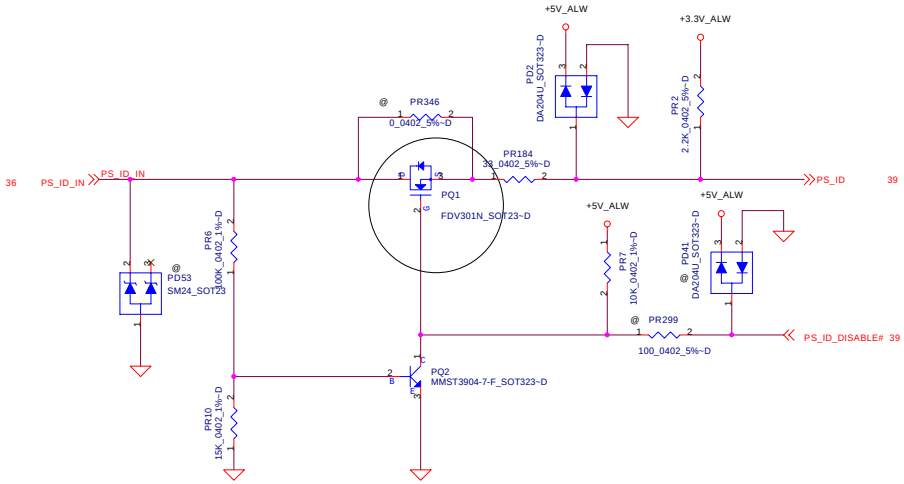
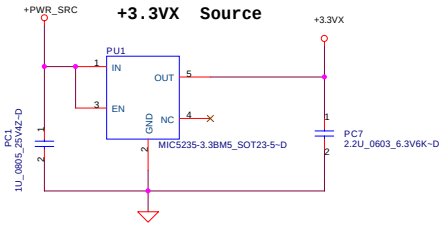
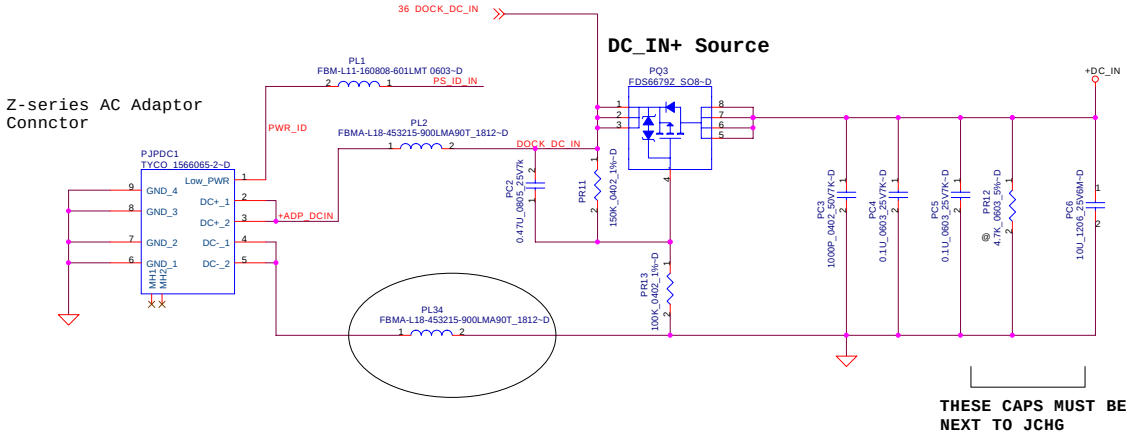
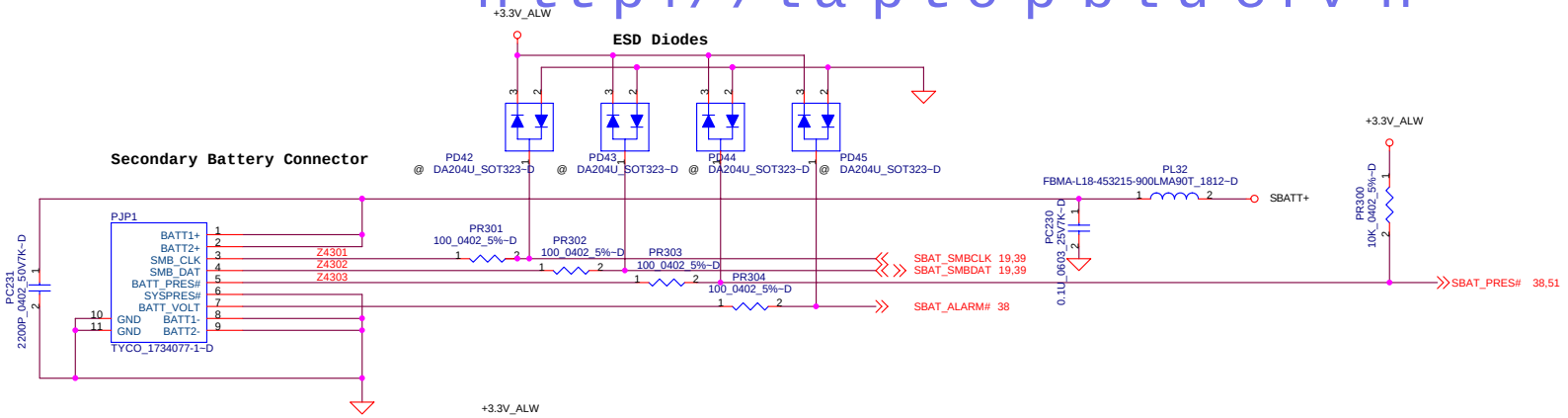


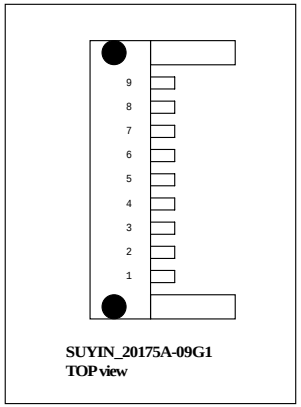




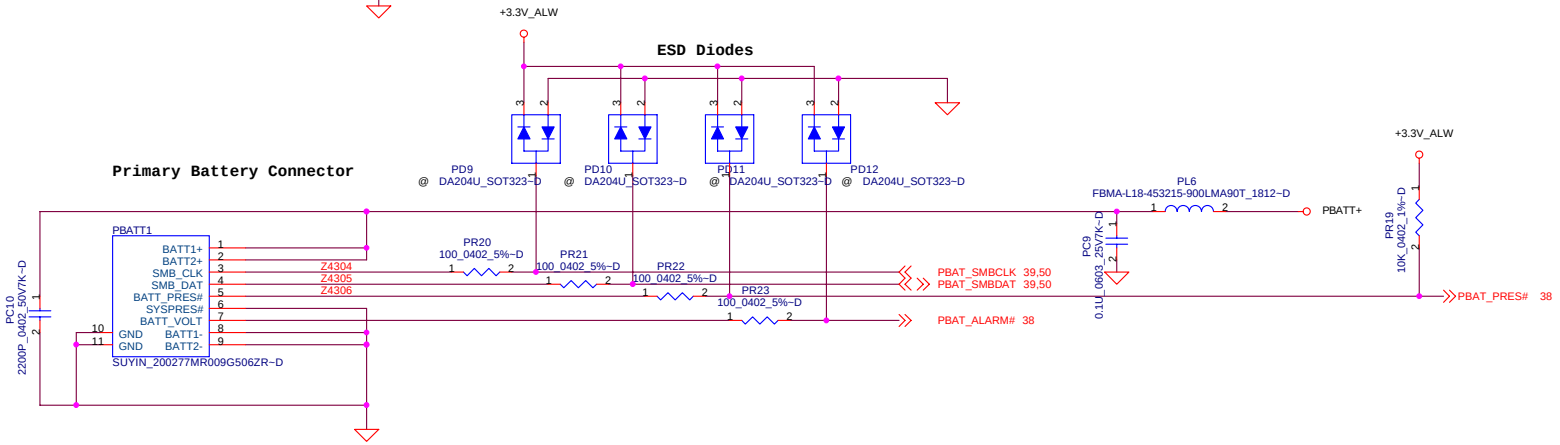
Title: +DCIN
Size: | Document Number: LA-2792 | Rev: 1.0
Date: Tuesday, February 07, 2006 | Sheet 44 of 70

Secondary Battery Connector





Primary Battery Connector



Compal Electronics, Inc.

Title: Battery Conn.

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Date: Tuesday, February 07, 2006 | Sheet 45 of 70

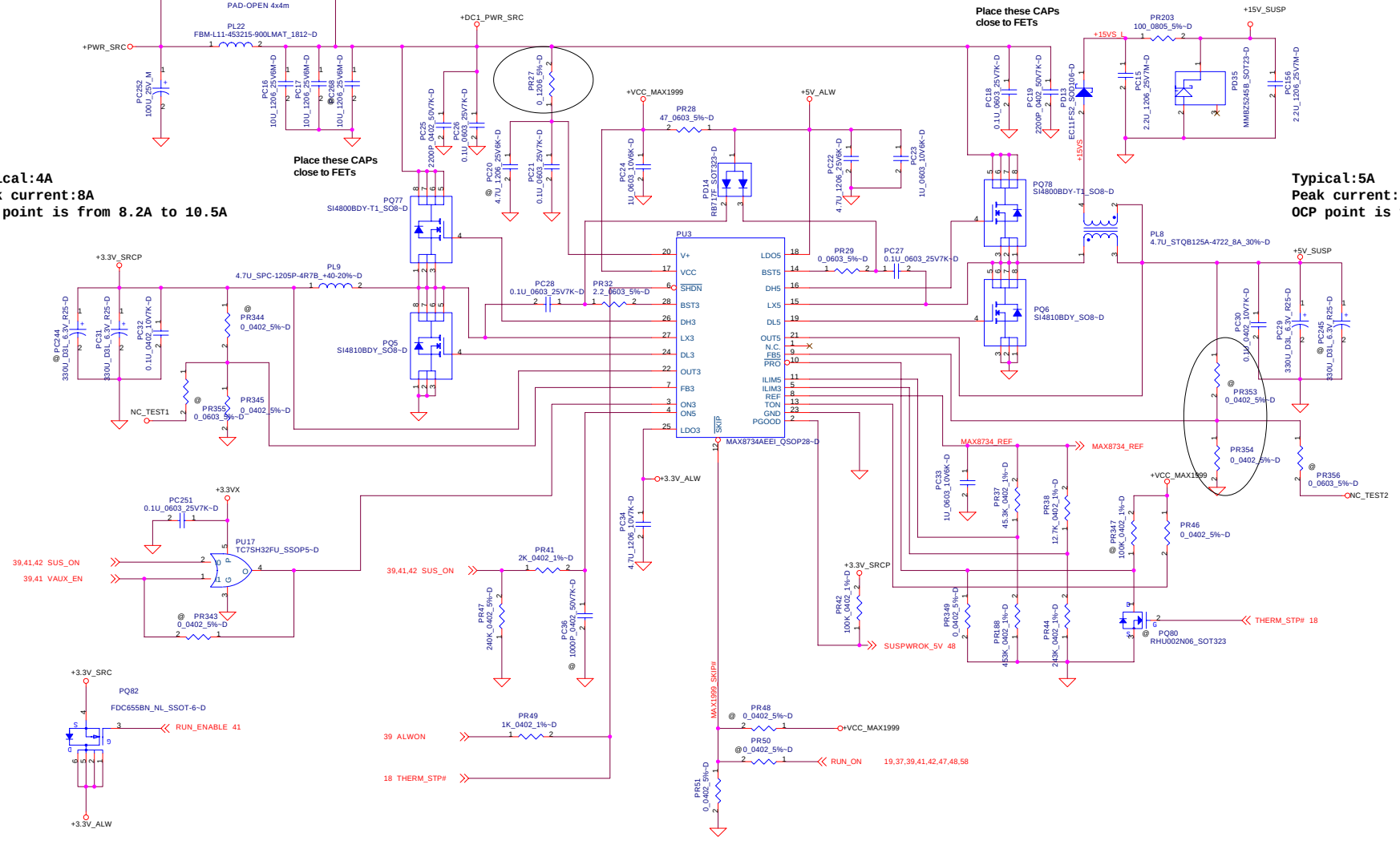
DC/DC +3V/ +5V/ +15V

Typical:4A
Peak current:8A
OCP point is from 8.2A to 10.5A

Typical:5A
Peak current:7A
OCP point is from 8A to 11.2A

Place these CAPs close to FETs

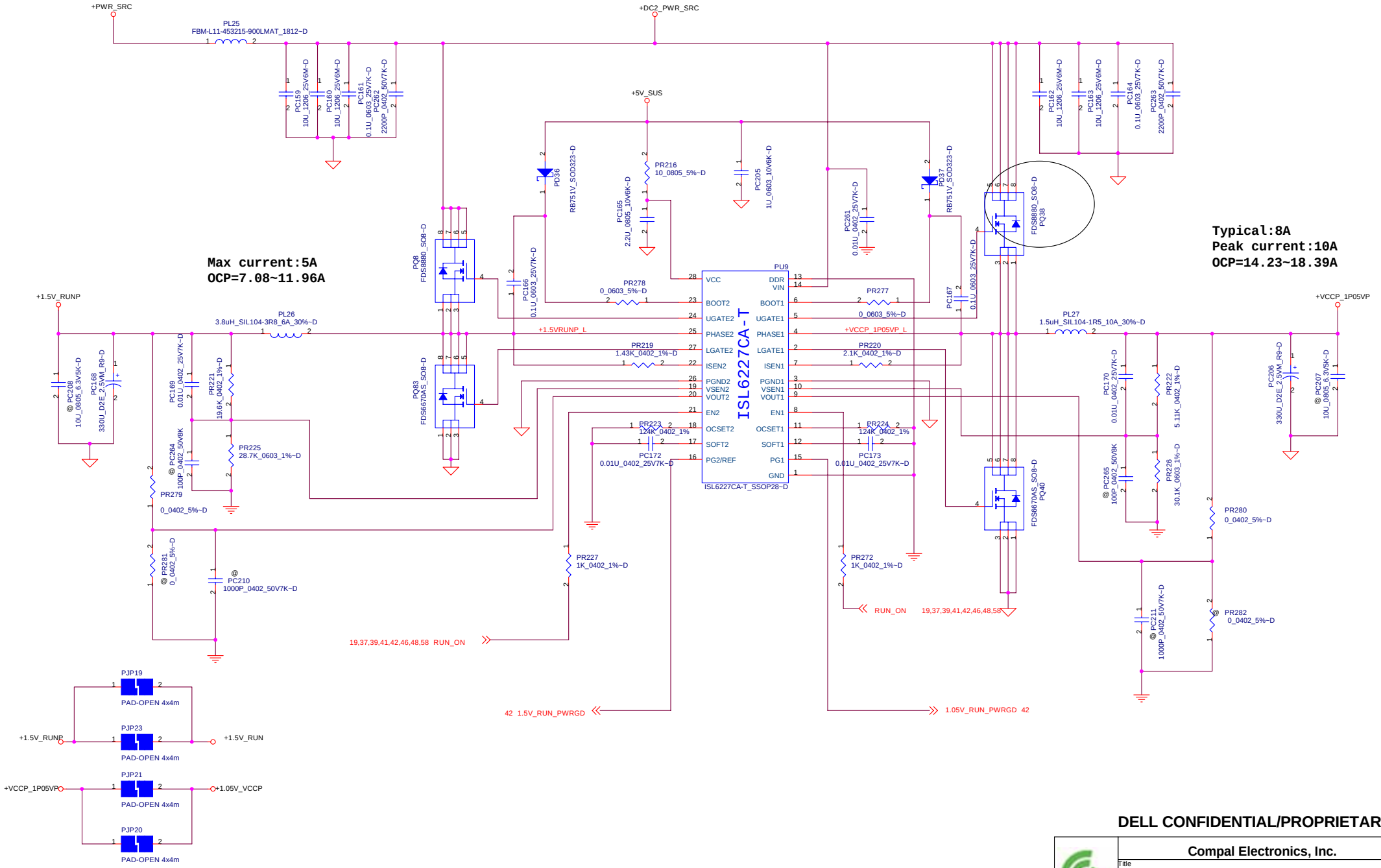
Place these CAPs close to FETs



Compal Electronics, Inc.

Title	+3.3V/+5V/+15V	
Size	Document Number LA-2792	Rev 1.0
Date: Tuesday, February 07, 2006	Sheet 46 of 70	

+1.5VRUNP / +VCCP_1P05VP



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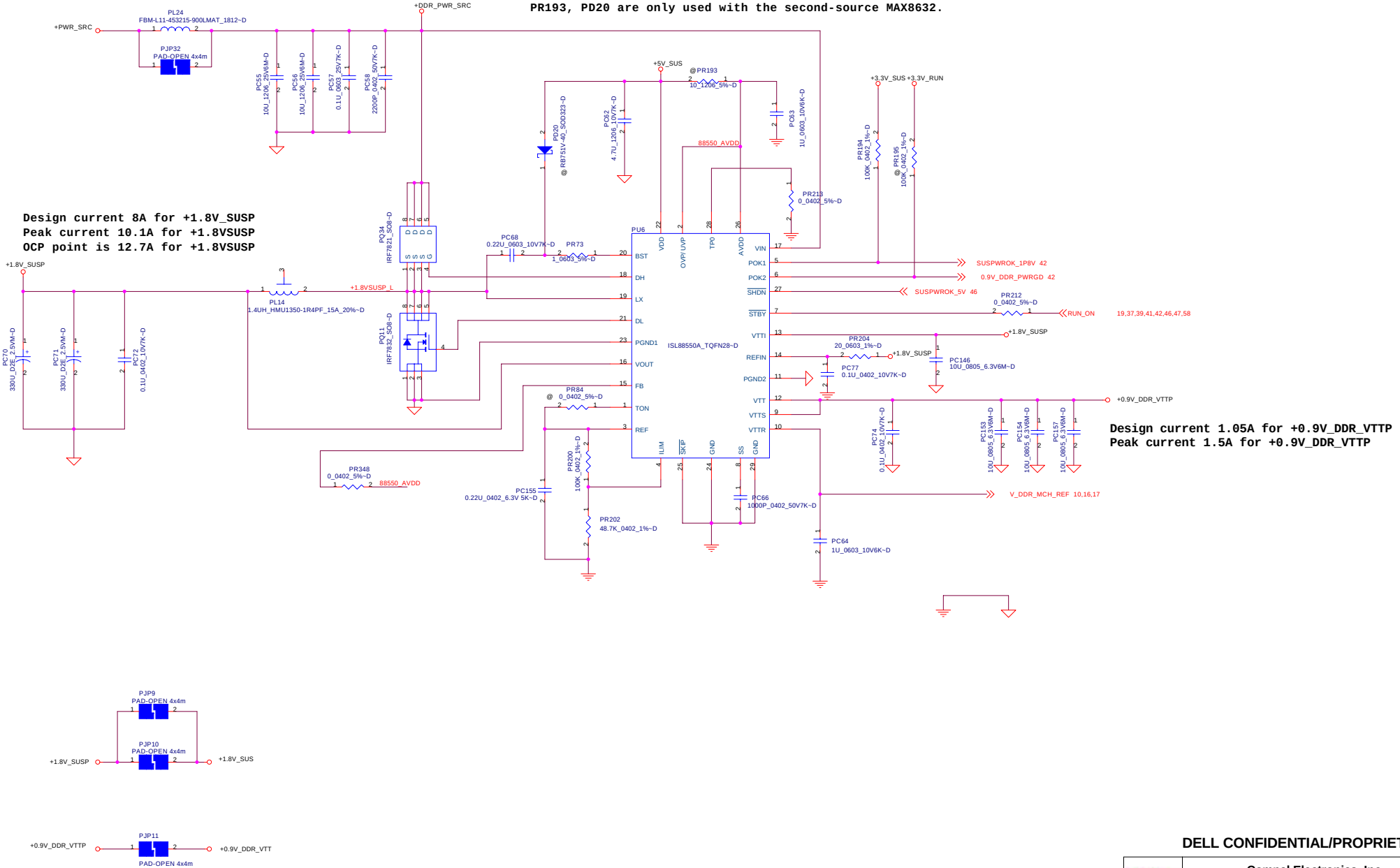
Compal Electronics, Inc.		
Title: +1.5VSUSP /+VCCP_1P05VP		
Size	Document Number: LA-2792	Rev: 1.0
Date: Tuesday, February 07, 2006	Sheet 47 of 70	

+1.8VSUSP/ +0.9V_DDR_VTT

DDR2 Termination

PR193, PD20 are only used with the second-source MAX8632.



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: +1.8VSUSP/ +0.9V_DDR_VT		
Size	Document Number: LA-2792	Rev: 1.0
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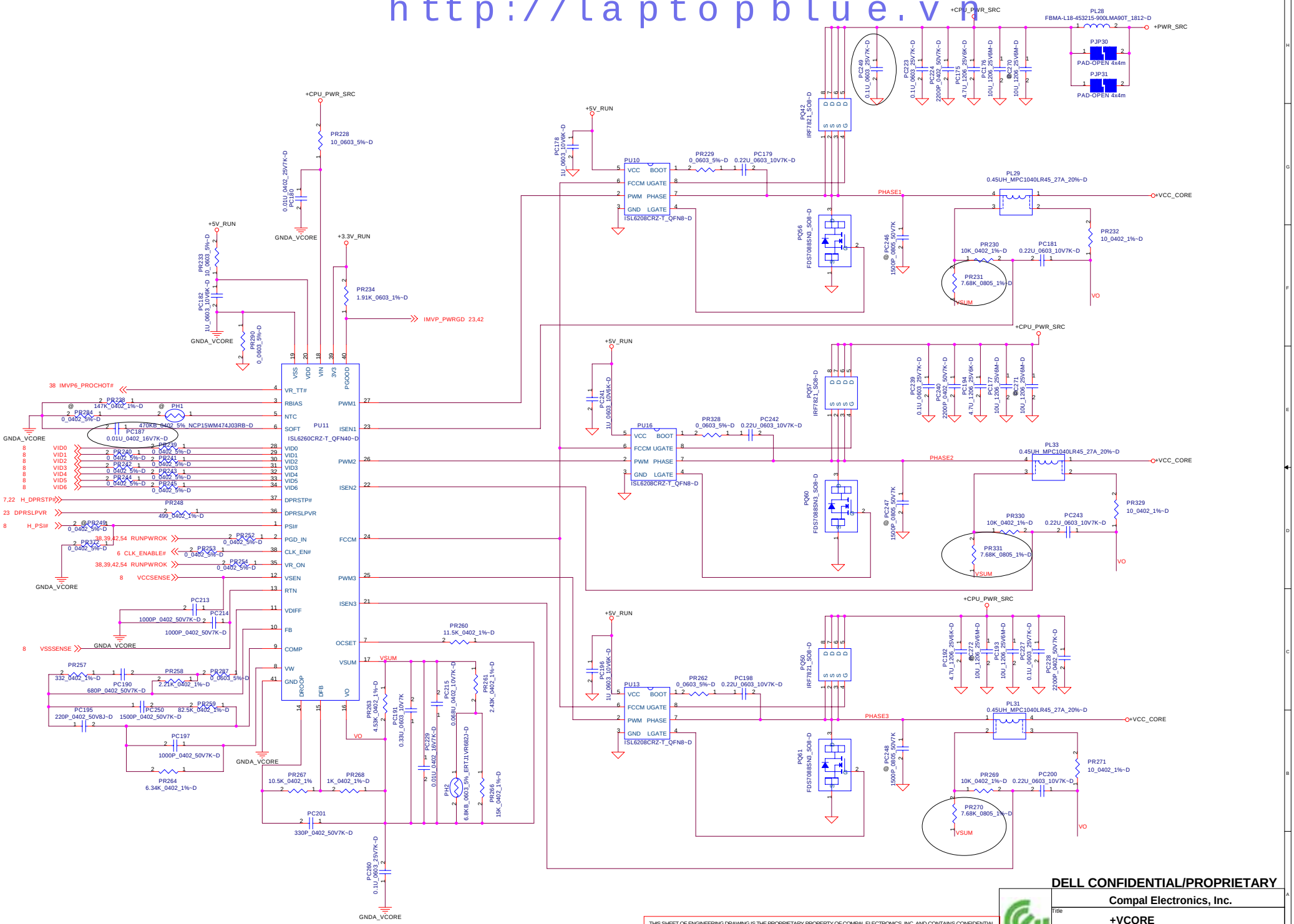

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Compal Electronics, Inc.

Title	+VCORE	
Size	Document Number LA-2792	Rev 1.0
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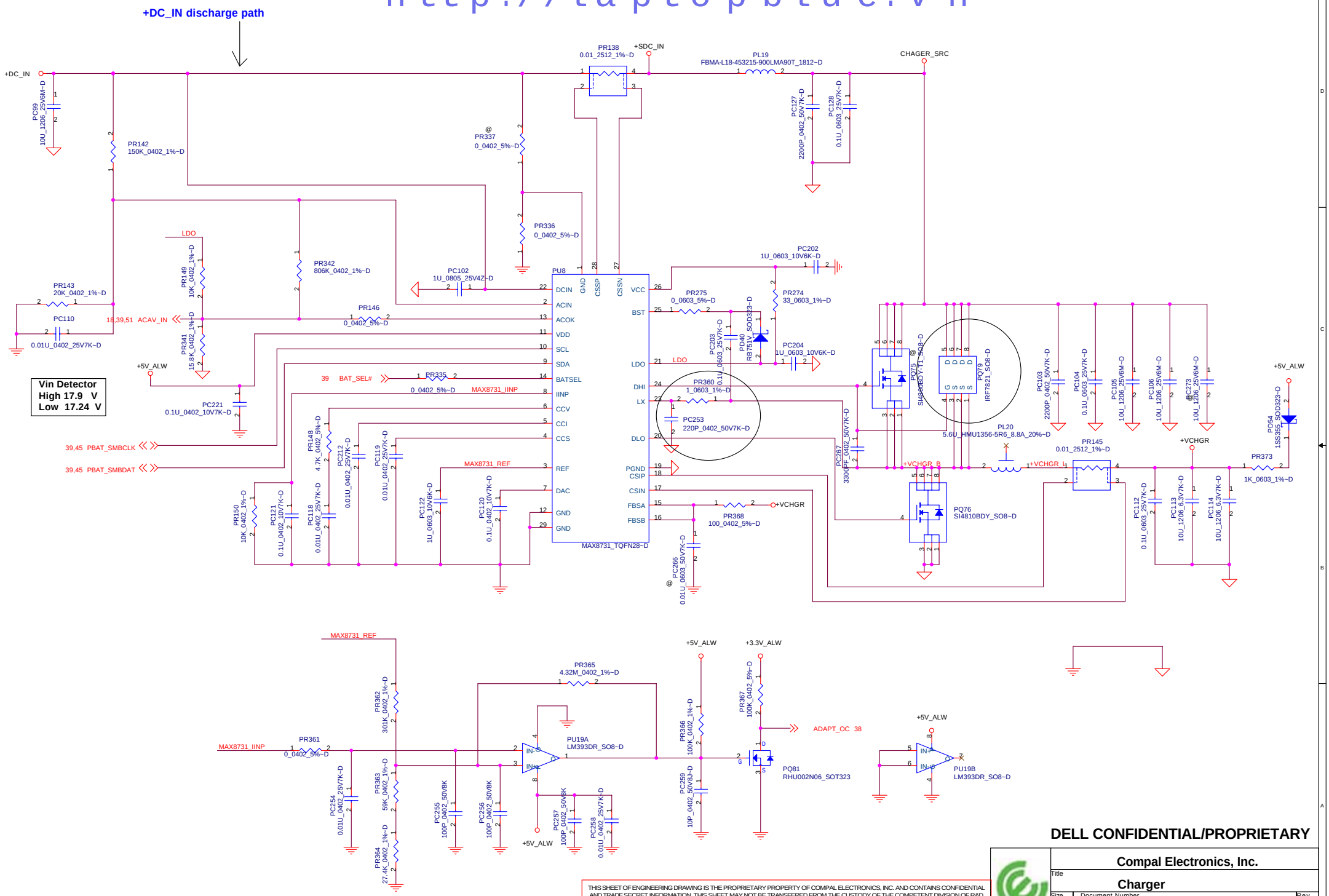
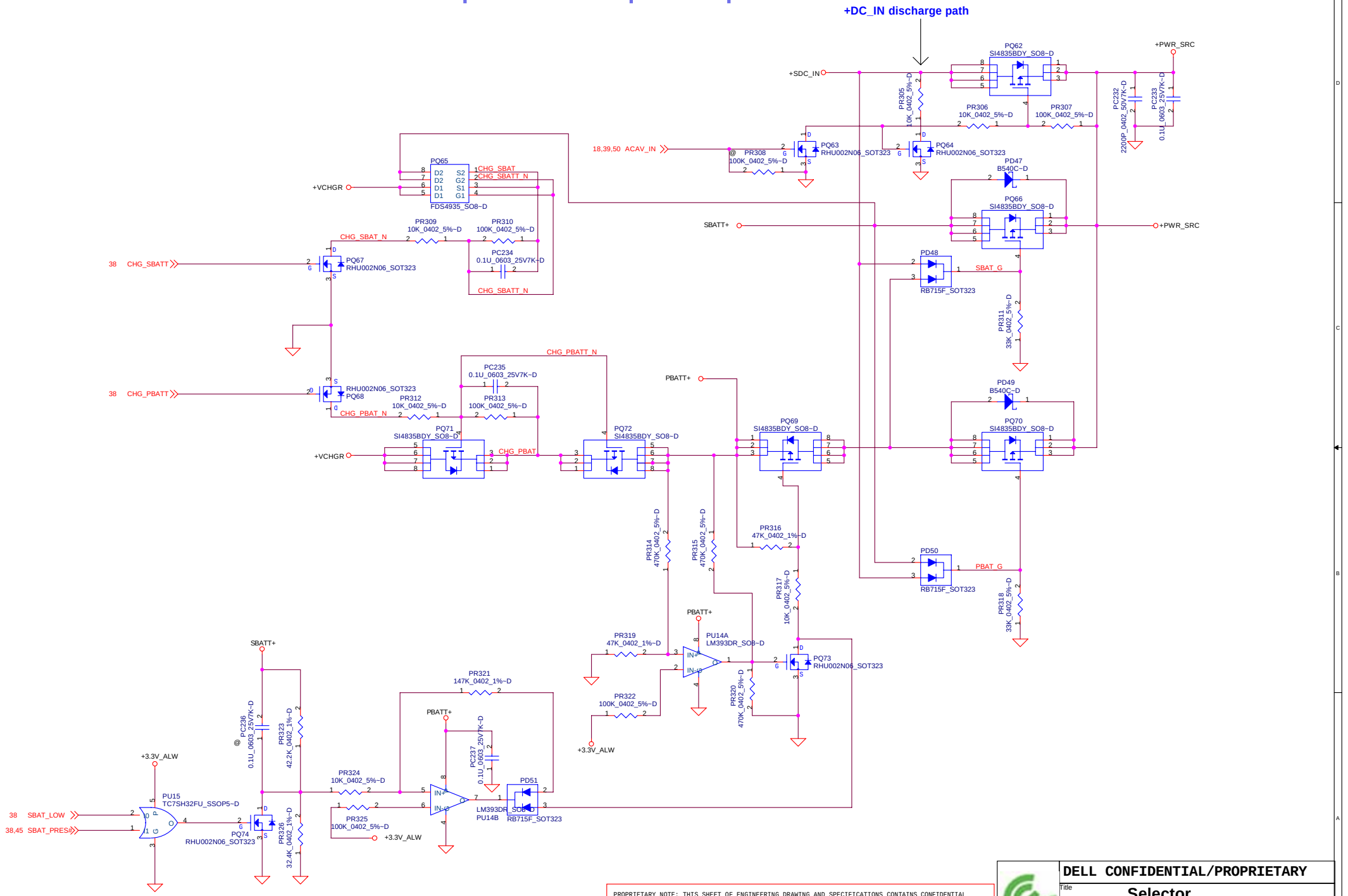


Compal Electronics, Inc.

Title: Charger

Size: | Document Number: LA-2792 | Rev: 1.0

Date: Tuesday, February 07, 2006 | Sheet 50 of 70



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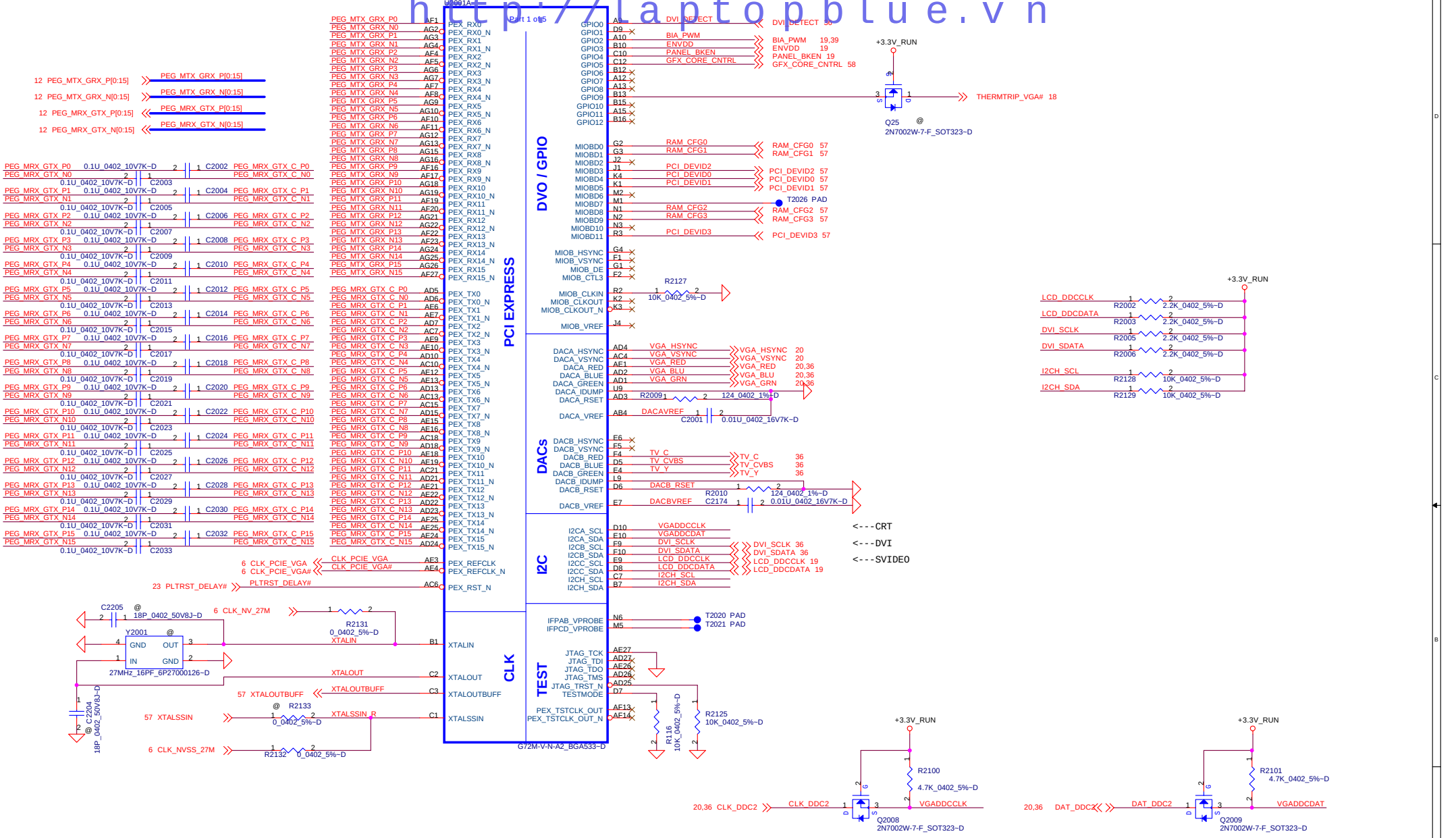
Title: **Selector**

Size	Document Number	Rev
	LA-2792	1.0

Date: Tuesday, February 07, 2006 Sheet 51 of 70



Compal Electronics, Inc.

Title: NVG72M PCIE,GPIO,CLK

Size: | Document Number: LA-2792 | Rev: 1.0

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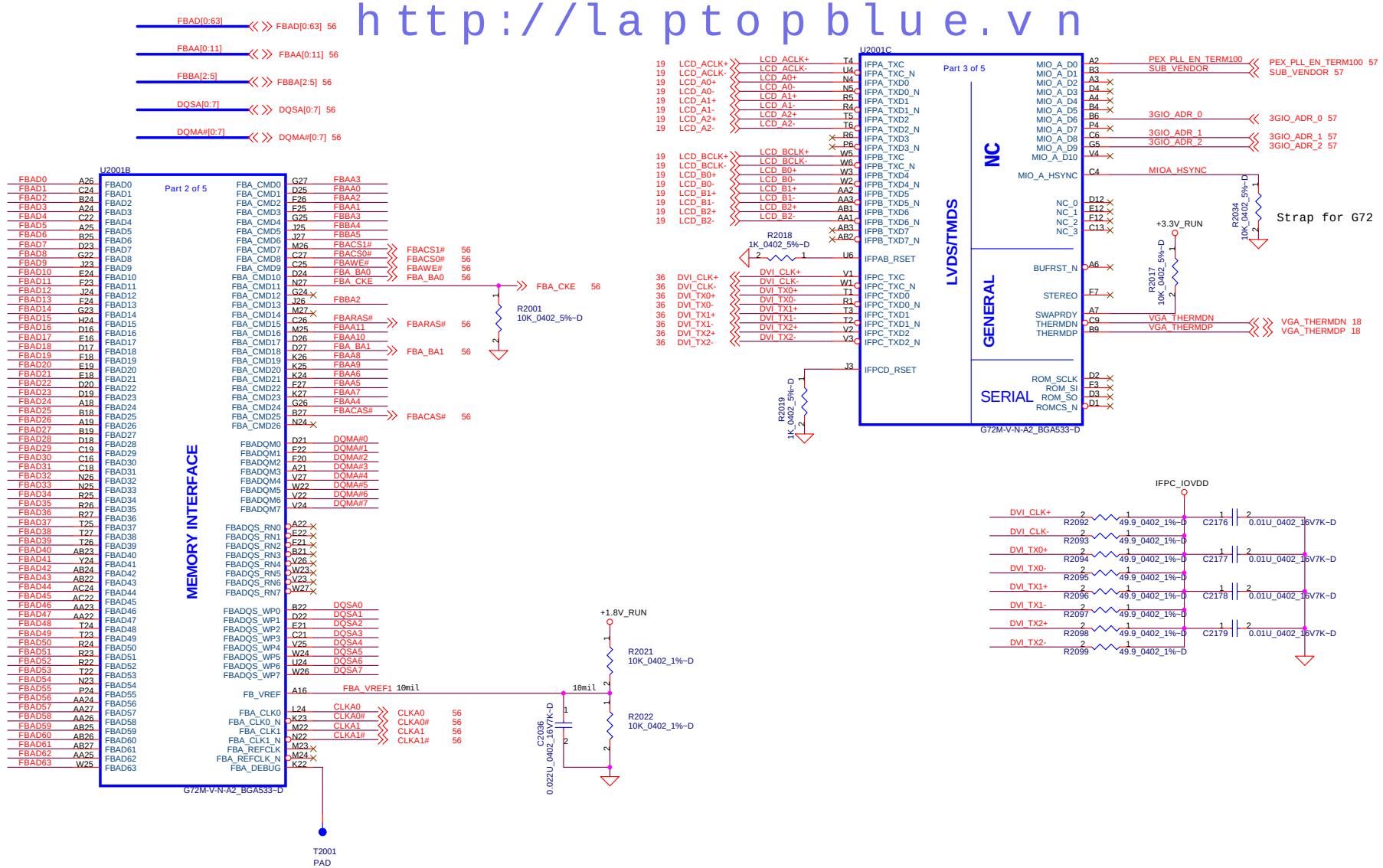

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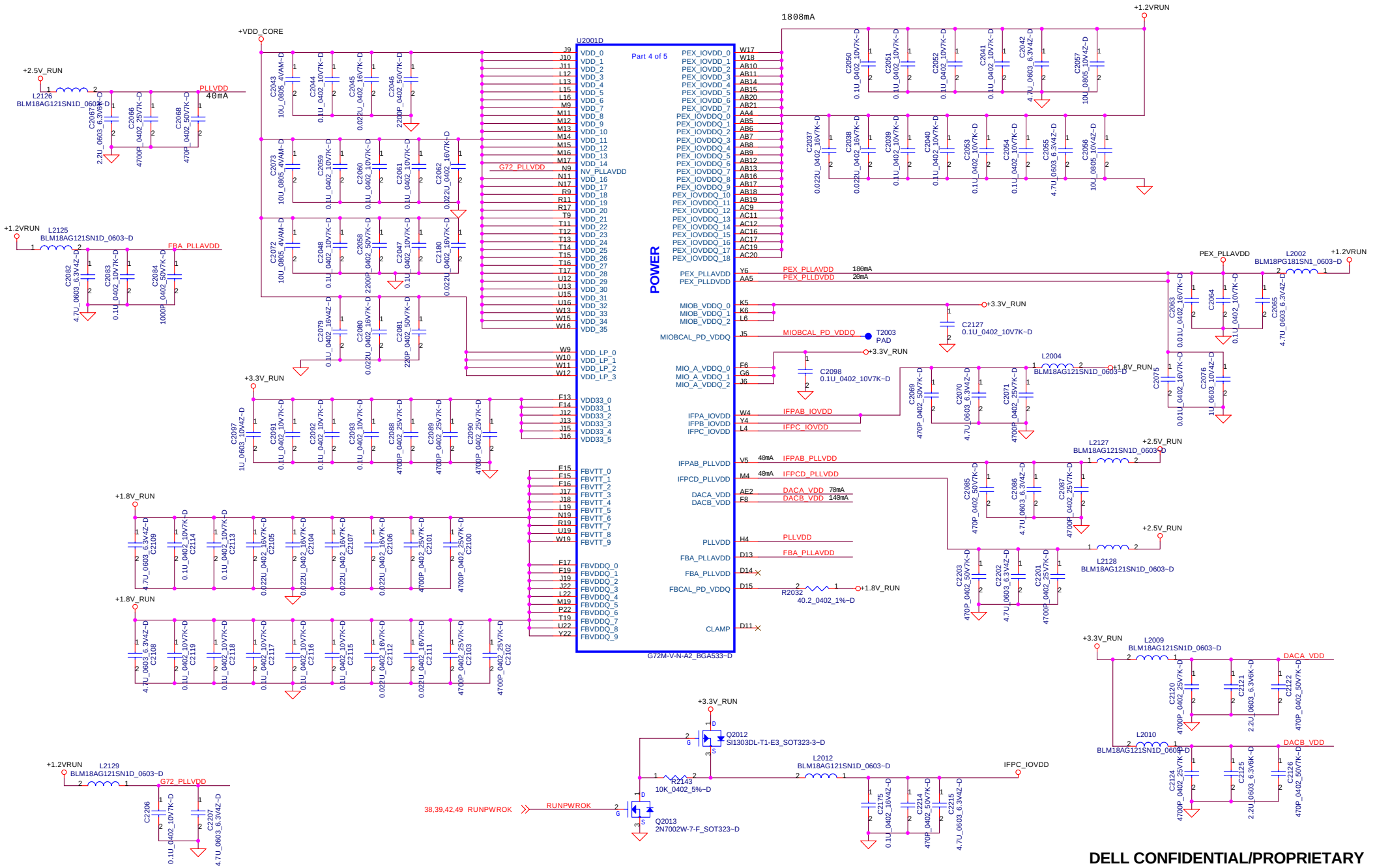
Compal Electronics, Inc.	
Title	NVG72M Memory Interface
Size	Document Number: LA-2792
Rev	1.0
Date:	Tuesday, February 07, 2006
Sheet	53 of 70



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Compal Electronics, Inc.	
Title	NVG72M Power
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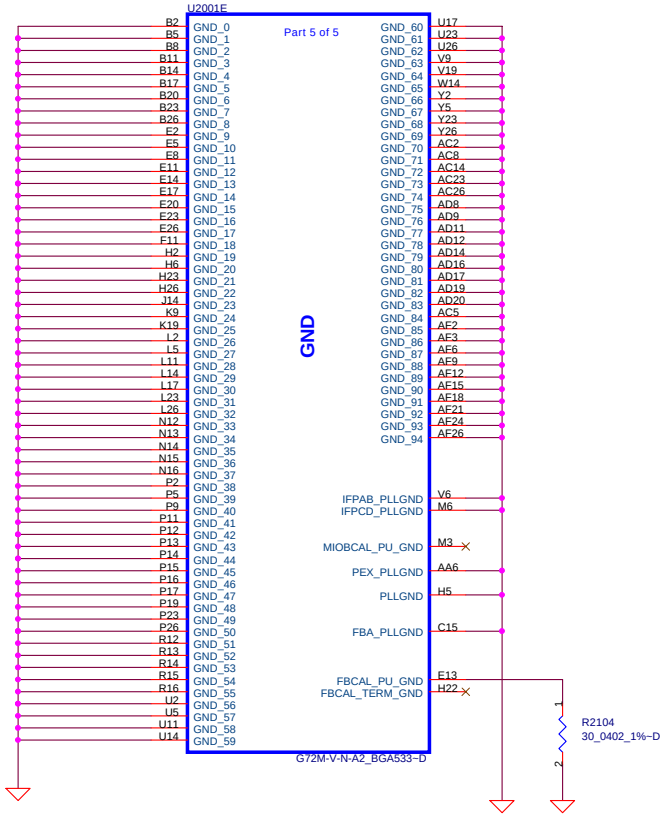

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Compal Electronics, Inc.	
Title	NVG72M Ground
Size	Document Number: LA-2792
Rev	1.0
Date:	Tuesday, February 07, 2006
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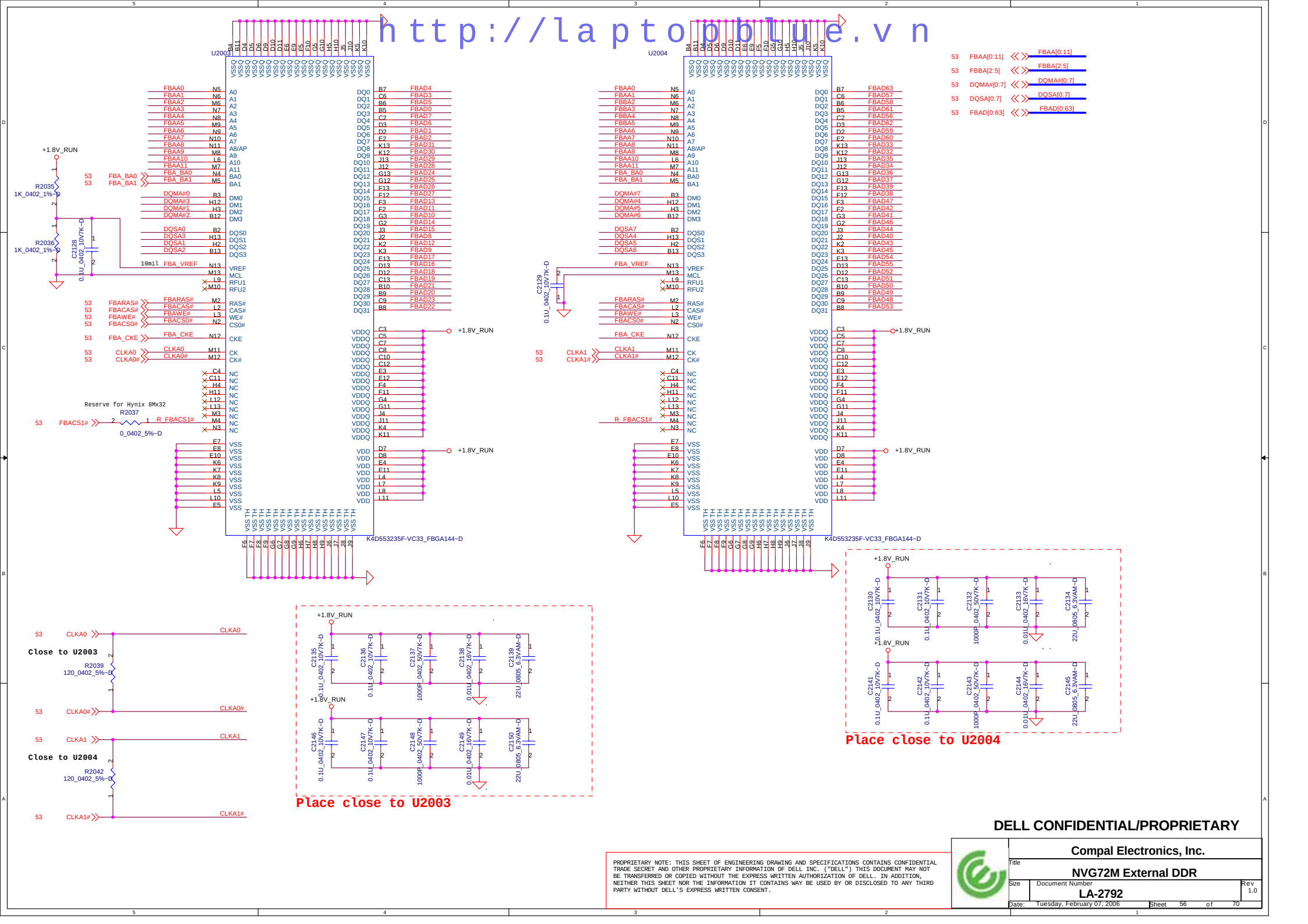
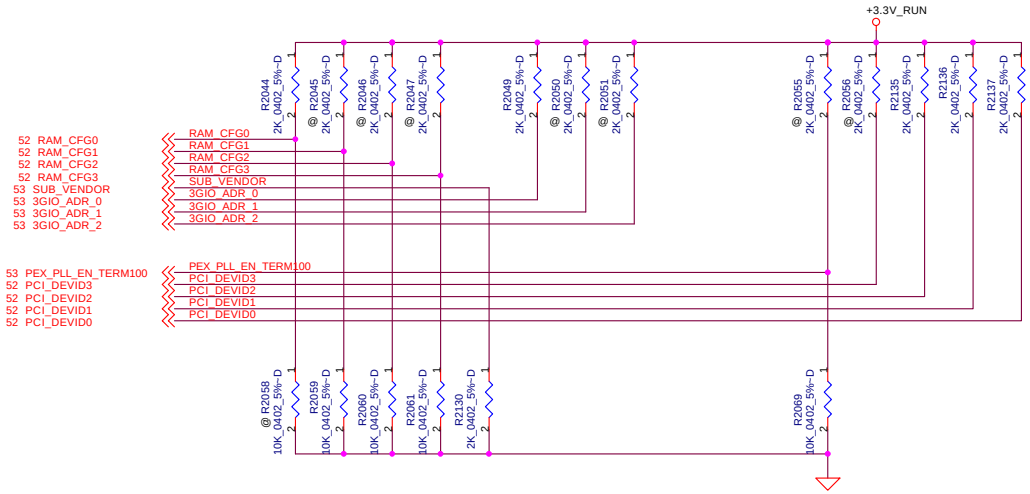
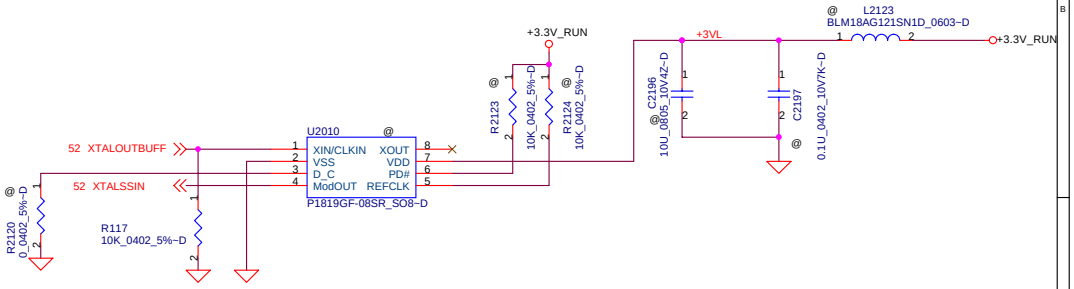


NV44M

STRAPS	PIN	DESCRIPTION	Value	
ROM_TYPE[1:0]	MIOBD10 MIOB_VSYNC	Parallel=00, SERIAL AT25F=01 DEFAULT, Serial SST45VF=10, LPC=11	01	
SUB_VENDOR	MIOAD1	VBIOS on card (pull high) VBIOS with system BIOS (pull down)	0	
PEX_PLL_TERM	MIOAD0		0	
RAM_CFG[3:0]	MIOBD0	8Mx32 DDR monolithic (64bit NV44)	0001	*
	MIOBD1	8Mx32 DDR monolithic (32bit NV44)	1001	
	MIOBD8	8Mx32 DDR (Samsung K4D55323QF-GC)	0010	
	MIOBD9	4Mx32 DDR generic (64bit NV44)	0100	
		4Mx32 DDR generic (32bit NV44)	1100	



STRAPS	CONFIG	DESCRIPTION	Value	
RAM_CFG[3:0]		Reserved	0000	
	8Mx32 DDR	300MHz, 1.8V	0001	
		Reserved	0010	
		350MHz, 1.8V	0011	
	4Mx32 DDR	1.8V I/O	0100	
		Reserved	0101	
	4Mx32 DDR	2.5V I/O	0110	
		Reserved	0111	



	S0
-1.75% (DOWN)	0
±0.875% (CENTER)	1

S0 Internal pull up

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Compal Electronics, Inc.

Title: NVG72M Spread Spectrum & Strapping

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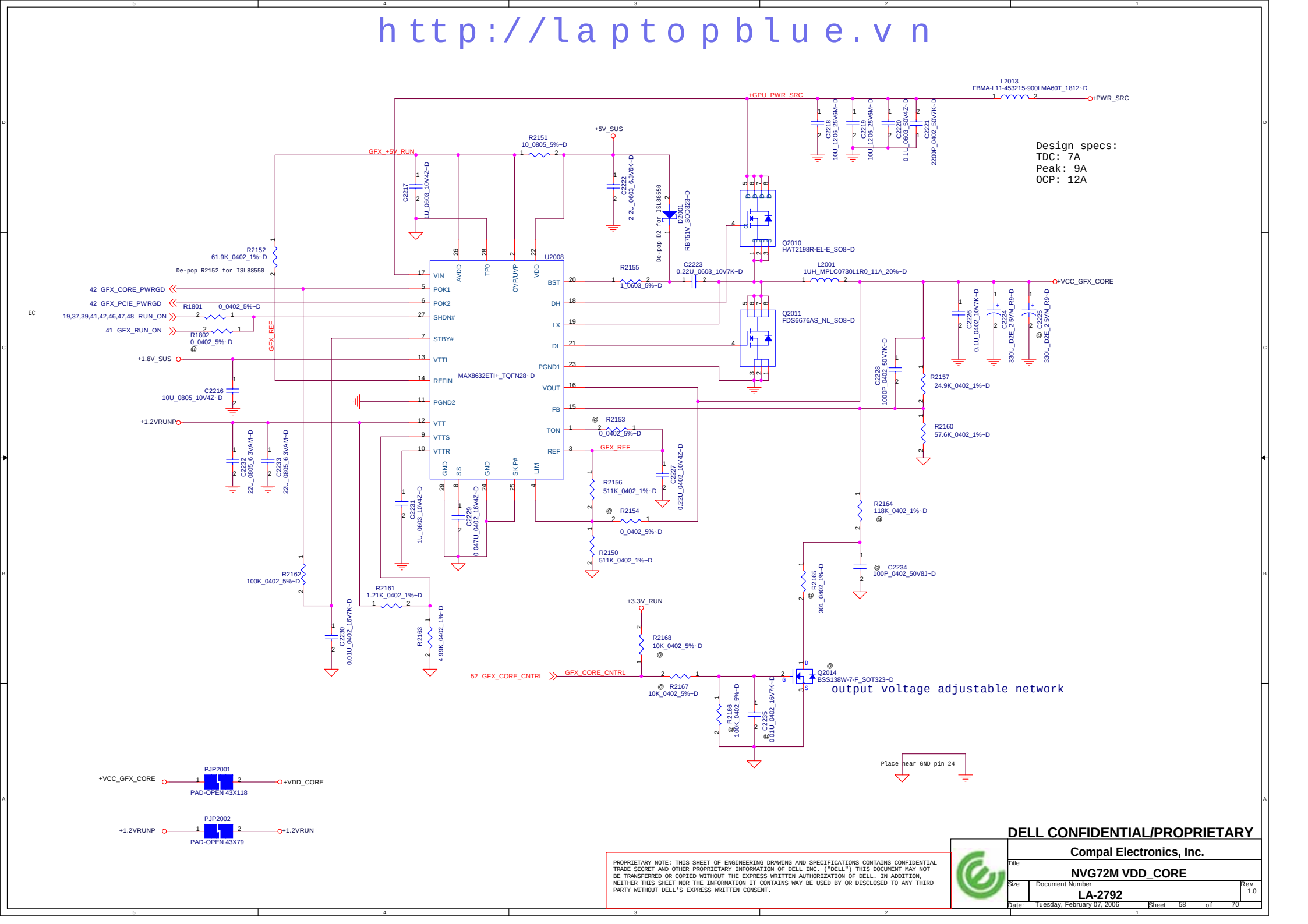

Compal Electronics, Inc.

Title: NVG72M VDD_CORE

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Date: Tuesday, February 07, 2006 | Sheet 58 of 70

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	31	H/W	05/27	Roger	Smart card pin definition not match the cage pin define	Change JSC pin connection, pin1 connect to GND, pin2 connect to SC_DET# ~ pin10 connect to +SC_PWR	0.2
2	52	H/W	05/27	Roger	TV out no out put	Add R1790, R1791, R1792 for 75 ohms	0.2
3	40	H/W	05/27	Roger	Remove power switch to save placement spacing	Remove SW1. Reseve R1793 pad for power switch	0.2
4	20	H/W	05/27	Roger	Docking CRT HSYNC, VSYNC connect to the out put side of buffer	DOCK_HSYNC connect from U190 pin4 to docking connector pin 209, DOCK_VSYNC connect from U191 pin4 to docking connector pin 210	0.2
5	32	H/W	05/27	Roger	Improve RJ45 center tap driving	Connect +2.5VLAN to JIO pin 14 for RJ45 center tap	0.2
6	39	H/W	05/27	Roger	SPI ROM pass trough mode connect error	Change FDATAIN to ICHO_FDATAIN and connect from U216 pin 106 to U213 pin5. Chagne FDATAOUT to ICHI_FDATAOUT and connect from U216 pin 108 to R1788 pin1	0.2
7	39	H/W	05/27	Roger	Flash Recovery strapping issue	Change R474, R475 from 100K to 10K	0.2
8	ALL	H/W	05/30	Brike	To fix MEC5004 VCC1 power lading	Change net from +3VALW to +3VSRC	0.2
9	43	H/W	05/30	Brike	None	Delete H21 and change H4 footprint from H_C176D122to H_C176D102	0.2
10	58	H/W	05/30	Brike	To meet VGA core power rating	Change footprint to JUMP_43X118	0.2
11	39	H/W	06/01	Will	For delay MEC5004 internal 1.8V reg.	Modified C1769 from 4.7UF to 22UF.	0.2
12	23	H/W	06/01	Will	To improve rise time of serial DO from SPI ROM.	Modified R389 from 10K to 1K..	0.2
13	41	H/W	06/01	Will	None	Add pullup R2149 to HDDC_EN# and R2148 MODC_EN#.	0.2
14	39	H/W	06/01	Will	None	Change power on SPI ROM (pins 3 and 8) from +3VALW to +3VSUS	0.2
15	58	H/W	06/01	Brike	None	U2008 pin 16 change pull-up panle to +3VRUN	0.2
16	13	H/W	06/01	Lester	Intel Checklist recommends a 1 nH ferrite which calculates to 200 ohm.	L34 value change to BLM18PG181SN1_0603~D	0.2
17	06	H/W	06/01	Lester	Add resistor for cystal drive current limiting	Add R32 0 ohm resistor	0.2
18	39	H/W	06/01	Will	Correct SPI connection for SMSC recommand	ICH7M.P5 connect to MEC 5004.107, MEC5004.108 connect to SPI ROM.5. ICH7M.P2 connect to MEC 5004.105, MEC5004.106 connect to SPI ROM.2	0.2
19	38	H/W	06/02	Roger	SMSC recommond add VBUS_DET pull up resistor	Add R1440 100K for LAN_TPM_EN# (VBUS_DET)	0.2
20	33	H/W	06/02	Roger	Add MDC disable circuit	Add R1441, R1442, R1443, Q64. ECE5018 pin 67 program MDC_RST_DIS#	0.2
21	34	H/W	06/06	Roger	None	Change U8 NNCD6.8RL-A to D5 NNCD5.6LG	0.2
23	3	H/W	06/06	Roger	None	Fixed USB table	0.2
24	27	H/W	06/14	Roger	U10 (STAC9200) pin21 (GPIO0) is anlog power plane	Change R156 pull up from +3VSUS to +VDDA	0.3

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
25	7	H/W	06/14	Roger	Change ITP debug to XDP debug definition for Yonah CPU	Change R387, R417, R391, R436, R416, R415 to 56 ohms. Add R33 56 ohms. Change R424 to 1K ohms.	0.3
26	39	H/W	06/14	Roger	For easier flash EC code	Add short pad and change R475 to 1K ohms	0.3
27	40	H/W	06/14	Roger	For easier power switch	Change R1793 to a pad like CMOS pad	0.3
28	34	H/W	06/14	Roger	ME change mini card stand off to Latch	Remove H22,H23,H24,H25. Add JCLIP1,JCLIP2	0.3
29	42	H/W	06/14	Roger	EMI reqest add caps for the splite power plane that PCI bus routed	Add C1806,C1807,C1808,C1809,C1810,C1811	0.3
30	41	H/W	06/16	Roger	Reserve discharg circuit for +5VRUN,+3VRUN, +1.8VRUN,+1.5VRUN,+0.9V_DDR_VTT,+2.5VRUN power rails	Add R1793,R1794,R1795,R1796,R1797,R1798,Q87,Q88,Q89,Q90,Q91,Q92	0.3
31	58	H/W	06/20	Roger	Replace ISL6269 and MAX1510 circuits with MAX8632 solution	Remove ISL6269 and MAX1510 circuit. Add MAX8632 circuit	0.3
32	28	H/W	06/21	Gautam	Reserve ST M45PE20 for LOM EEPROM	Add U3 (ST M45PE20) co-layout with U188 (AT45BCM021B)	0.3
33	42	H/W	06/23	Gary	EMI reqest add caps for the splite power plane that PCI bus routed	Add C1812~C184 0.047uF_0402. Change C1810, C1811 from 0603 to 0402 package	0.3
34	38	H/W	06/23	Roger	+3VRUN leakage at AC mode in S5	Change R1362 pull up from +3VSRC to +3VRUN	0.3
35	All	H/W	06/24	Roger	Follow Dell USB assignment recommendation	Update USB table, block diagram and connection	0.3
36	39	H/W	06/24	Will	4.7uF cap for VR_Cap pin of REV B 5504	Change C1769 for 22uF 0805 size to 4.7uF 0603 size	0.3
37	All	H/W	06/24	Will	Change +3V/+5V design to follow Dell recommendation	Change +3VSRC to +3VALW except for LOM	0.3
38	28	H/W	06/24	Gautam	IEEE testing the voltage level are closer to the higher end of IEEE range	Change R1364 from 1.15K to 1.18K_0402_1%	0.3
39	7	H/W	06/24	Lester	Required by Intel for B0 Yonah.	Add R1378 (51_0603_1%) for TEST2 pulldown	0.3
40	39	H/W	06/24	Lester	Required by Intel for B0 Yonah.	Populate R1752 and add note "No stuff when doing flash recovery"	0.3
41	58	H/W	06/27	Joey	Change Gfx VDD_CORE controller power source	Change +5VSUS to +5VRUN. Change +3VSUS to +3VRUN. Depop C2225	0.3
42	33	H/W	06/28	Rossana	MDC signal by pass caps not require	Delete C93, C82, C73	0.3
43	31,40	H/W	06/28	Rossana	Reseved USB port of OZ77C6 for Biometrics reader	Change JTPAD from 10 pins to 20 pins. Add USB_BIO+/- on U1 pin18,19 connect to JPAD pin9,11	0.3
44	30	H/W	06/28	Rossana	Gerber Gate List issue	Remove C1783, C1784	0.3
45	34	H/W	06/28	Rossana	Gerber Gate List issue	Remove L18, R149, and R144 - direct connect USB to Wireless LAN card	0.3
46	34	H/W	06/28	Rossana	Gerber Gate List issue	Add R1603 connect to JMINI2 pin46, outgoing signal BT_ACTIVE	0.3
47	34	H/W	06/28	Rossana	Gerber Gate List issue	Add series 0-ohms R1609, R1610 for pins 3 and 5 of JMINI2	0.3

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
48	34	H/W	06/28	Rossana	Gerber Gate List issue	Change C159 and C1785 from 10uF to 0.1uF	0.3
49	34	H/W	06/28	Rossana	Gerber Gate List issue	Add T1 test point for JMINI1 pin 42	0.3
50	36	H/W	06/28	Rossana	Gerber Gate List issue	Add C1817~1820 for U180,U178,U179,U177	0.3
51	39	H/W	06/28	Rossana	Gerber Gate List issue	Change R30 pull up from +3VSRC to +3VALW	0.3
52	43	H/W	06/28	Rossana	Change sniffer switch type, the active direction swap	WIRELESS_ON/OFF# connection from pin1 to pin 4 of JSNIFF, pin3 connect to GND, pin2 NC, pin 1 connect to SNIFFER#	0.3
53	36	H/W	06/28	Rossana	Gerber Gate List issue	Add C1821 1000pF for +DOCK_PWR_SRC, add C1827 1000pF for DOCK_DC_IN	0.3
54	35	H/W	06/28	Rossana	Gerber Gate List issue	Add C1822 0.1uF_0402 and C1823,C1824 .47uF_0402 for QBUF power	0.3
55	26,27	H/W	06/29	Rossana	Gerber Gate List issue	Follow Dell "Travis_Audio_0628" reference circut design	0.3
56	39	H/W	06/29	Will	Gerber Gate List issue	Change L4 form MURATA BLM11A121S to BLM18PG181SN1	0.3
57	24	H/W	06/30	Will	Gerber Gate List issue	Remove C375, C37 for ICH_V5REF_RUN, remove C420 for ICH_V5REF_SUS	0.3
58	24	H/W	06/30	Will	Gerber Gate List issue	Add R37 0.5 ohm 0603 resistor connect to L42 pin1	0.3
59	24	H/W	06/30	Scott	Gerber Gate List issue	Populate C347 and C442	0.3
60	24	H/W	06/30	Scott	Gerber Gate List issue	Change C450 for 220uF to 330uF poly cap	0.3
61	40	H/W	06/30	Roger	Match Dell JTPAD pinout definition	Match Dell JTPAD pinout definition, add C62, C63 for BIO power rail bypass	0.3
62	26,27	H/W	06/30	Rossana	Gerber Gate List issue	R162 change from 8.2K to 2.2K, remove D33, D34, Change C1800, C1801 from 1uF to 2.2uF, change C534 from 0.1uF to 1uF, del C533.	0.3
63	26	H/W	06/30	Rossana	Gerber Gate List issue	HP_NB_SENSE move from GPIO2 to GPIO0 of U10, add series resistor 0 ohm for this signal	0.3
64	7	H/W	07/07	Roger	Support A1 Yanah CPU	De-pop R513, R514 for A1 yanah CPU	0.3
65	56	H/W	07/25	Roger	Set VRAM VREF to 50% of VDDQ	Change R2035, R2036 to 1K_0402_1%	0.4
66	54	H/W	07/25	Roger	Nvidia G72 design change	De-pop L2008, C2094, C2095, C2096 for FBA_PLLVDD	0.4
67	54	H/W	07/25	Roger	Nvidia G72 design change	Remove C2110 and NC for CLAMP (D11)	0.4
68	54	H/W	07/25	Roger	Nvidia G72 power design change	Remove L2003, L2006, L2007, L2124, L2008, C2094, C2095, C2096	0.4
69	54	H/W	07/25	Roger	Nvidia G72 power design change	Pop L2129, C2206, C2207 for G72_PLLVDD	0.4
70	7	H/W	08/01	Roger	Gerber Gate List issue item 6	Change Change R417 to 150 ohm, R415 to 51 ohm, R387 to 39.2 ohm, R436 to 27.4 ohm, R391 to 680 ohm, R424 to 22.6 ohm	0.4
71	38	H/W	08/01	Roger	Gerber Gate List issue item 8	Change R110 from 68 ohm to 75 ohm for H_PROCHOT# pull up	0.4
72	43	H/W	08/01	Roger	Gerber Gate List issue item 9	Change the voltage rail on sniffer LED pull-ups (at Q13 and Q16) from +3VALW to +3VSUS	0.4

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
73	7	H/W	08/01	Roger	None	Remove unnecessary capacitor C1805	0.4
74	18	H/W	08/01	Roger	Gerber Gate List issue item 12	Remove Q84, C1804. Connect U15 pin1 to VGA_THERMDP, U15 pin2 to VGA_THERMDN	0.4
75	40	H/W	08/01	Roger	Hall switch design on touch pad moudle	Depop U46 and C54	0.4
76	18	H/W	08/01	Roger	Gerber Gate List issue item 13	Add a thermistor circuit to VCP input (pin 3) for the SODIMM temp sensor. Add Q15, R476, R477, R478, C66	0.4
77	57	H/W	08/01	Roger	Gerber Gate List issue item 15	Remove Gxf thermal sensor U2007 (ADM1032), C2181, C2182	0.4
78	38	H/W	08/01	Roger	Gerber Gate List issue item 19	Move NB_MUTE from U215 pin 107 to pin73	0.4
79	16,17	H/W	08/01	Roger	Gerber Gate List issue item 20,21	Remove R178, pop R177	0.4
80	10,23	H/W	08/01	Roger	Gerber Gate List issue item 22,23	Depop R253, populate R1799	0.4
81	38	H/W	08/01	Roger	Change board ID for X01	Depop R419 and populate R405	0.4
82	42	H/W	08/02	Roger	Gerber Gate List issue item3	Connect 2.5V_RUN_PWRGD net to LDO_POK pin. Add depop R49	0.4
83	18	H/W	08/02	Roger	Gerber Gate List issue item11	Add R1800 31.6K ohm resistor for Vmargin circuit.	0.4
84	23	H/W	08/02	Roger	Gerber Gate List issue item5	Change R389 from 1K to 10K	0.4
85	33, 40	H/W	08/04	Steven	Conbine the BT and TP in 30 PIN connector.	Delete JBT and move components to JTAP.	0.4
86	42	H/W	08/04	Steven	Gerber Gate List issue item3	Add Depop resister R2169, R2170, R2171.	0.4
87	22, 23	H/W	08/04	Steven	For intel NAPA platform check list 1.5 request.	Chnage R425 from 33Ohm pull-down to 8.2KOhm pull-up. And add pull-up resister R227 in SIO_RCIN#.	0.4
88	16	H/W	08/09	Roger	V_DDR_MCH_REF discharge issue	Add R51 (100K_0402) connect to V_DDR_MCH_REF	0.4
89	23	H/W	08/09	Roger	Leakage issue when system into S3	Change SIO_EXT_SMI#, SIO_EXT_SCI# pull up to +3VSUS	0.4
90	36	H/W	08/09	Roger	Refer Dell docking reference circuit	Remove R1320, R1319	0.4
91	12	H/W	08/09	Roger	Gerber Gate List issue item 28	Depop R357	0.4
92	38	H/W	08/09	Roger	Follow Dell EC GPIO assignment	Move SPDIF_SHDN from pin31 to pin76, remove R1601, R1602, net SYSOPT0	0.4
93	28	H/W	08/10	Roger	Gerber Gate List issue item 30	Add R53 4.7K resistor for LOM_SO pull down	0.4
94	28	H/W	08/10	Roger	Gerber Gate List issue item 33	Connect BCM5752 pin C4 to ECE5018 pin75 net name LOM_CABLE_DETECT. Series no stuff resistor R55	0.4
95	24	H/W	08/10	Roger	Gerber Gate List issue item 37	Connect BCM5752 pin C4 to ECE5018 pin75 net name LOM_CABLE_DETECT. Series no stuff resistor R55	0.4
96	38	H/W	08/10	Roger	Gerber Gate List issue item 39	R1171 change pull up from +3VRUN to +3VSUS	0.4
97	38	H/W	08/10	Roger	Gerber Gate List issue item 42	Add a 4.7uF cap for ECE5018 VDDA33 coupling	0.4

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98	39	H/W	08/10	Roger	Gerber Gate List issue item 43	Add a 0 Ohm 0402 resistor R62 in series with the RTC_CELL and EMC5004 pin 121	0.4
99	7	H/W	08/10	Roger	Follow Intel CRB circuit	R513, R514 pull up to +VCCP	0.4
100	39	H/W	08/10	Roger	Gerber Gate List issue item 46	Add resistor R63 (0_0402_5%) between the BIA_PWM signal and MEC5004 pin 73	0.4
101	39	H/W	08/10	Roger	Gerber Gate List issue item 47	Change ITP_DBRESET# connection from EMC5004 pin 55 to pin96	0.4
102	22	H/W	08/10	Roger	Gerber Gate List issue item 50	Add no stuff C69 (0.1U_0402_16V4Z) between THRMTRIP_ICH# and GND	0.4
103	41	H/W	08/10	Roger	None	Change R1795 pin 1 connect from +1.8VRUN to +1.8VSUS for discharge	0.4
104	23	H/W	08/10	Roger	Gerber Gate List issue item 51	Move pull-up R388 to pin 1 side of R1787	0.4
105	6	H/W	08/10	Roger	Gerber Gate List issue item 29	Add C70 (0.1U_0402_16V4Z) for +CK_VDD_MAIN decoupling. Remove R291, R343, R329 to save spacing	0.4
106	7	H/W	08/11	Roger	Gerber Gate List issue item 68	Remove R513 and R514 platform no longer use Yonah A00	0.4
107	42	H/W	08/11	Roger	Gerber Gate List issue item 65	Populate 0ohm for R49, R313, R319, R334	0.4
108	41	H/W	08/11	Roger	Gerber Gate List issue item 67	Change R494 to 20K	0.4
109	7	H/W	08/11	Roger	Gerber Gate List issue item 69	Add no stuff C71 and C72 for +VCCP of JITP	0.4
110	7	H/W	08/11	Roger	Gerber Gate List issue item 70	Change R416 and R33 from 56 ohm to 54.9 ohm	0.4
111	12	H/W	08/11	Roger	Gerber Gate List issue item 72	Delete R333 to follow reference schematics	0.4
112	28	H/W	08/11	Roger	Gerber Gate List issue item 34	Add R68 (20K_0402_5%) and R70 (39K_0402_1%) for LAN_LOW_PWR voltage divider connect to pin K5	0.4
113	26,27,38	H/W	08/12	Roger	Gerber Gate List issue item 75	DOCK_HP_MUTE# for GPIO2 of codec connect to ECE5018 pin 81. EAPD for GPIO3 of codec connect to additional Q11 gate	0.4
114	38	H/W	08/15	Roger	Gerber Gate List issue item 38	Chnge SYS_PME# pull up from +3VRUN to +3VALW. Add no stuff R71 in series	0.4
115	38	H/W	08/15	Roger	Gerber Gate List issue item 41	Remove HP_NB_SENSE from ECE5018 pin 106 to pin 82	0.4
106	23	H/W	08/15	Roger	Gerber Gate List issue item 188,189	Depop R428,Change value of R75 to 10k ohms	0.4
107	6	H/W	08/15	Roger	NVidia 27MHz clock has to be 1.2V max	Add R73 150 ohms for CLK_NV_27M voltage divider	0.4
108	52	H/W	08/15	Roger	Gerber Gate List issue item 211	Add R74 0 ohms in series to PLTRST_DELAY#	0.4
109	40	H/W	08/16	Roger	Gerber Gate List issue item 48	Change R1750 and R1751 to L1 and L2	0.4
110	40	H/W	08/16	Roger	Gerber Gate List issue item 48	Change R1750 and R1751 to L1 and L2	0.4
111	39	H/W	08/16	Roger	Gerber Gate List issue item 217	Remove R166. Move R1635 for AFT_INT# move to page 39	0.4
112	39	H/W	08/16	Roger	Add pull up for open drain out put	Add R93 pull up to +3VALW for BAT_SEL#	0.4

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113	38	H/W	08/16	Roger	Mute internal speaker when docking aduio jack plug in	Add pull down resistor for DOCK_HP_MUTE#	0.4
114	58	H/W	09/07	Roger	G72MV VDDCORE fixed to 1.0 V	Depop R2164,R2165,R2166,R2167,R2168,Q2014,C2235. Change R2160 from 69.8K ohms to 57.6K ohms	0.4
115	06	H/W	09/07	Roger	Follow Dell CoE schematics	Change C329, C333 from 33pF to 27pF	0.5
116	43	H/W	09/14	Roger	Blue tooth LED too bright	Change R8 from 3.3K to 1K ohms	0.5
117	41	H/W	09/14	Roger	+1.8VSUS discharge low issue	Populate Q89, R1795	0.5
118	39	H/W	09/14	Roger	LID_CL# can't assert low	Change R482 from 100K to 1M ohms	0.5
119	39	H/W	09/14	Roger	R470 from 10K to 100K is for save the pull up current.	R470 from 10K to 100K	0.5
120	34, 39	H/W	10/13	Steven	Connect 8051TX to WWAN Pin 19 and Connect 8051RX to WWAN Pin 42.	Modified.	0.5
121	22	H/W	10/15	Steven	Gerber Gate List issue item 60. Per M07 ICH reference schematics rev A05.	Add R12 0-ohm tuning resistor between R36 pin2 and X1 pin1	0.5
122	41	H/W	10/17	Steven	Gerber Gate List issue item 66	Change R1795 to a 30 ohm 0603 resistor	0.5
123	52	H/W	10/17	Steven	Gerber Gate List issue item 67. Use 27MHz clock from CK410.	Pop R2131, R2132, and depop Y2001, C2204, C2205, and R2133	0.5
124	19	H/W	10/17	Steven	Gerber Gate List issue item 65. Make sure BIA_PWM logic high level is at +3.3V.	Add R92 pullup to +3VRUN on BIA_PWM	0.5
125	39	H/W	10/18	Steven	MEC5004 per SMSC recommendations to add circuit for improving POR issue.	Add de-pop components R23, R25, R97, R102, R104, Q20, Q19, C22, D2002. And change C1769 to 22U.	0.5
126	38	H/W	10/18	Steven	change board ID to X02	Pop R95, R419 and De-pop R108, R405.	0.5
127	23	H/W	10/18	Steven	Gerber Gate List issue item 78. Pull up LAMP_STAT# to +3VRUN	Change R75 pull-up to +3.3V_RUN.	0.5
128	40	H/W	10/18	Steven	Gerber Gate List issue item 77. add 10pF cap between GND and pin2 of L1/L2.	Add capacitor C23, C35.	0.5
129	6	H/W	10/19	Steven	Gerber Gate List issue item 72. Inductor design follow M07 design on L40,L32 (Size:0805).	Change L32, L40 from 0603 to 0805.	0.5
130	23	H/W	10/19	Steven	Gerber Gate List issue item 79. SATA_DET# is pull up to +3.3V_SUS.	Change R784 pull up to +3.3V_SUS.	0.5
131	9	H/W	10/20	Steven	Gerber Gate List issue item 84	Change the 32 high frequency decoupling caps, 0805 X5R, from 22uF to 10uF. Depop C354 and C618.Change C352, C496, C497, and C365 from 330uF/7mOhm to 330uF/6mOhm SP caps.	0.5
132	34	H/W	10/20	Steven	Gerber Gate List issue item 82	Connect PLTRST# instead of PLTRST_DELAY# to WLAN and WWAN connectors.	0.5
128	23	H/W	10/20	Steven	IMVP_PWRGD glitch issue	Add C82 0.1uF cap on IMVP_PWRGD to filter the glitch	0.5
129	28	H/W	10/21	Steven	Q68 surge current	Add R120 (0603) and C80 0.1uF cap Q68 pin1 for reduce surge current	0.5
130	40,43	H/W	10/21	Steven	BT & HDD LED is on when the SNIFFER is turned on.	Added a circuit (FET and Resistors) to keep the BT LED & HDD LED off when the SNIFFER is turned on	0.5

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131	38	H/W	10/21	Steven	Gerber Gate List issue item 81	Depop R1440	0.5
132	34	H/W	10/22	Steven	Add Intel WoWLAN Support Circuit	Add pop components Q21 and R101, and un-pop componet R24.	0.5
133	18	H/W	10/24	Steven	Gerber Gate List issue item 89. Change OTP trip temperature to 88 deg C.	Change R249 to 332K and R262 to 118K.	0.5
134	39	H/W	10/24	Steven	Gerber Gate List issue item 90. Pop SMSC workround circuit for 11/7 build.	Pop R23, R25, R97, R102, R104, Q20, Q19, C22, D2002.	0.5
135	39	H/W	10/24	Steven	Gerber Gate List issue item 91. Add a 0 ohm pulldown resistor on TEST_PIN.	Add R110 0Ohm resister.	0.5
136	52	H/W	10/24	Steven	Gerber Gate List issue item 94. Connect GPIO9 of G72 to THERMTRIP3# of EMC4000.	Add 0 Ohm resister R112 and connect to EMC4000.	0.5
137	58	H/W	10/24	Steven	Gerber Gate List issue item 95.	Change R2155 from 0 to 1 Ohm.	0.5
138	58	H/W	10/24	Steven	Gerber Gate List issue item 96.	Change +5V_RUN to +5V_SUS at VDD.	0.5
139	58	H/W	10/24	Steven	Gerber Gate List issue item 97.	Change +3.3V_RUN to +3.3V_SUS at R2158.	0.5
140	58	H/W	10/24	Steven	Gerber Gate List issue item 98.	Change +1.8V_RUN to +1.8V_SUS at pin 13.	0.5
141	52	H/W	10/24	Steven	Gerber Gate List issue item 113. Add a 10K pull-down to TESTMODE pin on G72.	Add 10K Ohm resister R116.	0.5
142	43	H/W	10/24	Steven	Gerber Gate List issue item 111. Remove one of the pull-ups on SNIFFER_LED_OFF#.	Remove Pull up resister R1447.	0.5
143	43	H/W	10/24	Steven	Gerber Gate List issue item 111.	More R76 to pin 1 of Q66 and populate	0.5
144	34	H/W	10/24	Steven	Add Intel WoWLAN Support Circuit	Replace Q21 and R101 to D2003.	0.5
145	20	H/W	10/24	Steven	Gerber Gate List issue item 109. Add 39 ohm resistors at output of U190 and U191.	Add resister R101 and R114.	0.5
146	18	H/W	10/24	Steven	Gerber Gate List issue item 93. Add thermistor circuit to VCP2 (pin 40) of EMC4000. Please route to 5V_CAL_SIO2# (pin 80, GPIO B4 on ECE5018).	Add thermistor circuit R479, R480, R481, C36, Q21.	0.5
147	54	H/W	10/24	Steven	Gerber Gate List issue item 106. Change FBCAL_PD_VDDQ terminating resistor.	Change R2032 from 37.4 to 40.2 ohms.	0.5
148	54	H/W	10/24	Steven	Gerber Gate List issue item 105. Change FBCAL_PU_GND terminating resistor.	Change R2104 from 37.4 to 30 ohms.	0.5
149	43	H/W	10/24	Steven	Gerber Gate List issue item 114. Modified SATA_ACT# LED sniffer disable circuit.	Modified the circuit and Add and D2004. Chnage Q1 to 3904, R1149/1448 change to 10K and 1K.	0.5
150	58	H/W	10/25	Steven	Gerber Gate List issue item 120. Pull up R2159 to +3.3V_SUS.	Change R2159 to pull up +3V_SUS.	0.5
151	40	H/W	10/25	Steven	Gerber Gate List issue item 119. For fix the IMVP_PWRGOOD glitch issue.	Change delay circuit R1764 from 200KOhm, C1788 to 470PF to +1.8V_run and +3V_run.	0.5
152	43	H/W	10/25	Steven	Gerber Gate List issue item 104. Modified the SATA_ACT# circuit.	Modified the circuit Pull up R1449 to +5V_SUS and R1445 to +5V_run. R2 move to Q1 pin 3, SNIFFER_LED change to GPIO82.	0.5
153	34	H/W	10/25	Steven	Gerber Gate List issue item 115. Change LTRST_DELAY# to PLTRST# on WLAN.	Chnage PLTRST_DELAY# to PLTRST# on the WLAN connector.	0.5
154	58	H/W	10/25	Steven	Gerber Gate List issue item 117. Modified Vcore voltage switching circuit.	Change R2168 to +3.3V_SUS.	0.5

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155	57	H/W	10/25	Steven	Gerber Gate List issue item 118. Depop the discrete spread spectrum circuit.	Depop R2120, U2010, R2123, R2124, C2196, C2197 and L2123.Add R117 10K pull down resister.	0.5
156	20	H/W	10/25	Steven	Gerber Gate List issue item 116. Add diode HSYNC and VSYNC buffers.	Add D2005 (RB751) in U190, U191 Pin 5.	0.5
157	18	H/W	10/25	Steven	For improving Gerber Gate List issue item 94 leakage issue.	Change 0Ohm resister to Q25.	0.5
158	58	H/W	10/25	Steven	Cancelled Gerber Gate List issue item 97.	Change +3.3V_SUS to +3.3V_RUN at R2159.	0.5
159	40, 43	H/W	10/26	Steven	Modified HDD/BT disable circuit.	Move 40 BT Disable circuit to 43.	0.5
160	58	H/W	10/26	Steven	Gerber Gate List issue item 121. Delete resistors R2158 and R2159 on sheet 58.	Remove R2158 and R2159.	0.5
161	41	H/W	10/29	Steven	For improving power sequence add RC delay and Discharge circuit.	Add R1765, C1804 for delay +3V_run circuit. Add non-populate component. Q26, Q28, R1803, R1766.	0.5
162	58	H/W	10/29	Steven	For pop option 8632 shutdown pin source Add two resister.	Add Non-populate R1802 and Populate component R1801. For Pop option 8632 Enable source.	0.5
163	41	H/W	11/03	Steven	Populate the HDD power switch circuit	Pop Q51, R507, Q50 and Depop PJP24.	0.5
164	31	H/W	11/03	Steven	For passing EMVCo test.	Change R1424 from 220 to 330Ohm.	0.5
165	43	H/W	11/03	Steven	SNIFFER_LED_OFF# is a push/pull signal.	De-pop R1449.	0.5
166	27	H/W	11/03	Steven	To improve audio quality	Change C199 to 0.022uF and pop R164, depop R170.	0.5
167	39	H/W	11/11	Steven	Change SMSC MEC5004 from version C to D.	Change U216 P/N to D version. Depop R102, R97, R25, R23, R104, D2002, Q19, Q20, C22. And chnage C1769 value from 22UF to 4.7UF.	0.5
168	56	H/W	11/11	Steven	Change VRAM parts to K4D553235F-VC33 as DELL request.	Change VRAM P/N to K4D553235F-VC33 (SA55323000L).	0.5
169	39	H/W	11/11	Steven	Change DOCK_SMB_CLK and DOCK_SMB_DAT for consistent with other M07 platforms.	Change R99 and R100 resister from 100K to 8.2K Ohm. And R1618 change to 10K.	0.5
170	42	H/W	11/11	Steven	Provide pull-up resister to GFX_CORE_PWRGD for 1.2Vrun power used.	Pop R2170 for provide pull-up resister.	0.5
171	43	H/W	11/11	Steven	For improve LED brightness issue.	Change R2 value from 56Ohm to 330Ohm. And modified R15 from 150Ohm to 100Ohm.	0.5
172	28	H/W	11/12	Steven	For Q68 broken issue. Modified R120 value for protect base pin.	Change R120 from 0Ohm to 2KOhm.	0.5
173	20	H/W	11/12	Steven	For DELL request change D32 and D2005 to RB500.	Change D32 and D2005 from RB751 to RB500.	0.5
174	27	H/W	11/12	Steven	For improve Audio THD+n performance.	Change C113, C114 and C146 from 1UF to 2.2U.	0.5
175	27	H/W	11/22	Steven	For adjust Audio gain to 15.6DB.	Pop R170, De-pop R164.	0.5
176	42	H/W	12/06	Steven	For improving SUSPWROK turn on issue.	Modified Q7 to 2N7002.	0.6
177	23, 38	H/W	12/06	Steven	For solving HD warn boot parking sound issue.	Change HDDC_EN#, MODC_EN# from ICH7 to ECE5018 Pin 106, 107 (GPIOH2/3), and Depop R2148, R2149.	0.6
178	7	H/W	12/06	Steven	Add a De-pop resister for CPU test 1 PIN.	Add De-pop resister R1387.	0.6
179	39	H/W	12/07	Steven	Add an damping resister for improving SPI_CS# overshoot issue.	Add 47Ohm resister R127.	0.6

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179	39	H/W	12/09	Steven	For solving SBAT_SMBDAT rising time over spec issue.	Change R444 to 4.7KOhm resister.	0.6
180	6	H/W	12/12	Steven	For Gerber Gating list item 14 Depop pullup resistor on ICH_CLKREQ#.	Depop resister R1761.	0.6
181	38	H/W	12/12	Steven	For Gerber Gating list item 17 Update board ID to A00	Pop R405, depop R419.	0.6
182	31	H/W	12/12	Steven	For Gerber Gating list item 11 add 47pF capacitors to the USB_BIO+/- pins to fix bio sensor ESD issue.	Add 2 capaciotr C83, C84 in USB_BIO+/-.	0.6
183	41	H/W	12/14	Steven	For GPIOH[3:2] need, chnage pullup resister power plane to always.	Change pullup resister R2148, R2149 for +3.3V_SUS to +3.3V_ALW.	0.6
184	41	H/W	12/15	Steven	For Gerber Gating list item 18. Change pullup resister to 10K.	Change pullup resister R2148, R2149 for 100K to 10KOhm.	0.6
185	39	H/W	12/19	Steven	For Gerber Gating list item 21. Add 0 ohm series resistor to SPI_CS# at MEC5004.	Add series resister R112 at MEC5004 side.	0.6
186	31	H/W	12/19	Steven	For improving USB BIO sensor EMI issue.	Add Pop L5, and depop resister R122, R123.	0.6
187	40	H/W	12/20	Steven	For DELL EMI request for add a 0.1uF capacitor in JTPAD.	Add 0.1uF capacitor C54.	0.6
188	28	H/W	12/30	Steven	For Q68 damage issue change form BCP69 to MBT35200 as ZRS solution.	Use MBT35200 to replace Q68. Modified.	0.6
189	7	H/W	12/30	Steven	Intel Design Guide 1.0 to change H_RESET pull-up resister to 51Ohm.	Change resister R416 to 51Ohm.	0.6
190	39	H/W	01/04	Steven	For enable MEC5004 BIOS write protect function.	Pop R139 and de-pop R138.	0.6
191	27	H/W	01/07	Benson	For adjust Audio gain to 21.6 DB.	DePop R170, pop R164.	0.6
192	28	H/W	01/09	Steven	For Q68 issue to reserve soft start circuit.	Change R120 to 0Ohm, and depop C80.	0.6
193	58	H/W	01/09	Steven	For avoiding GPU leakage issue.	Change R2168 pull-up from +3.3V_run to +3.3V_sus.	0.6
194	20	H/W	01/20	Steven	For fixing issue with projector using long cable.	Change R101,R114 from 39 ohm to 0 ohm	**0.6**
195	19	H/W	01/20	Steven	For stronger the VGS driving in Battery Mode	Change R235 from 200K ohm to 100K ohm	**0.6**
196	6	H/W	01/20	Steven	The Drive Level too high	Change R32 from 0 ohm to 470 ohm	**0.6**
197	22	H/W	01/20	Steven	The Negative Resistance too low	Change X1 spec from CL=20pF to 6 pF and C38,C40 from 12pF to 2.2pF	**0.6**
198	38	H/W	01/20	Steven	The Frequency too high & Drive Level too high	Change Y1 spec from CL=20pF to 12pF and C1451,C1452 from 22P to 15P	**0.6**
199	31	H/W	01/20	Steven	None	Depop L5 ,pop R122,R123 33 ohm	**0.6**
200	23	H/W	01/20	Steven	To fix PLTRST_DELAY# glitch	Change R74 from 0 ohm to 10K ohm and pull-down it	1.0
201	23	H/W	02/06	Steven	For solving USB strength issue.	Change R113 from 22.6Ohm to 22Ohm.	**0.6**
202	39	H/W	02/07	Steven	For solving primary battery hand issue.	Change R447, R449 to 4.7KOHm; R444, R131 to 2.2KOhm.	**0.6**

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1	46	PWR	06/01	Saha	M4 input current more than MAX8734 LDO3 output 100mA	Delete PU17 SN74AHC1G32DCKR OR GATE(SA00732018L), PR49 1K_0402_1%(SD03410018L) Add PR350 0_0402_5%(SD02800008L) connact LDO3 to ON3 PU18 74AHCT1G08GW AND GATE(SA00000L30L) PR352 1K_0402_1%(SD03410018L) PR351 0_0402_5%(SD02800008L)	0.2 0.2
2	46	PWR	06/01	Saha	MAX8734 LDO soft start issue.	Delete PR27 4.7_1210_5%(SD000007E8L) Un-pop PC20 4.7U_1206_25V6K(SE093106M8L)	0.2
3	46	PWR	06/01	Saha	PWR_SRC noise issue	Un-pop PC252 100U_25V_M(SF10004M008)	0.2
4	44/45	PWR	06/01	Saha	+3VALW change to +3VSRC	Rename net +3VALW to +3VSRC	0.2
5	47	PWR	06/01	Saha	VCCP high/low side MOSFET change from IR to Infineon No-stuff PC207 and PC208	PQ38 change from IR7821(SB57821008L) to BSO072N03S(SB00000418L) PQ40 change from IR7832(SB57832008L) to BSO072N03S(SB00000418L) Un-pop PC207 and PC208 10U_0805_6.3V5K(SE093106M8L)	0.2
6	47	PWR	06/01	Saha	VCCP_1P05VP OCP issue(5A)	PR224 change from 124K_0402_1%(SD03412438L) to 60.4K_0402_1%(SD03460428L)	0.2
7	47/48	PWR	06/01	Saha	Choke height issue.(5.6mm change to 5.0mm)	PL14 and PL27 change from 1.4U_HMU1356-1R4_15.5A H5.6mm(SH04814AM8L) to 1.4U_HMU1350-1R4_15A H5.0mm(SH000004H8L)	0.2
8	44	PWR	06/01	Saha	PSID materiel change by Dell	PQ1 change from BSS138_SOT23(SB50138008L) to FDV301_SOT23(SB50301008L)	0.2
9	50	PWR	06/01	Saha	New version MAX8731 PIN1 define GND	Un-pop PR337 0_0402_5%(SD02800008L),Pop PR336 0_0402_5%(SD02800008L)	0.2
10	50	PWR	06/02	Saha	Add RC filter at pin 23 of MAX8731	Add PR360 1_0603_1%(SD014100B8L) PC253 220P_0402_50V7K(SE074221K8L)	0.2
11	46/48	PWR	06/02	Saha	Add support for Reliability voltage margining tests	Add PR356, PR355 and PR359 0_0603_5%(SD01300008L) PR353 and PR354 0_0402_5%(SD02800008L)	0.2
12	48	PWR	06/16	Saha	Change output capactior rating voltage from 6.3V to 2.5V	PC70 and PC71 change from 330U_D3L_6.3V_R25(SGA00000N8L) to 330U_D2E_2.5VM_R15(SGA19331D0L)	0.3
13	49	PWR	06/22	Saha	Change VCORE DPRSLPVR input resistor value	PR248 change from 0_0402_5%(SD02800008L) to 499_0402_1%(SD03449900L)	0.3
14	50	PWR	06/22	Saha	Add power limit schematic	Depop PR361 80.6K_0402_1%, PR362 200K_0402_1%, PR363 121K_0402_1%, PR364 3.01K_0402_1%, PR365 499K_0402_1%, PR366 100K_0402_1%, PR367 100K_0402_1%, PC254 0.01U_0402_25V8K, PC255 100P_0402_50V8K, PC256 100P_0402_50V8K, PC257 100P_0402_50V8K, PC258 0.01U_0402_25V8K, PC259 10P_0402_50J8K, PQ81 RHU002N06_SOT323, PU19 LM393DR_SO8	0.3
15	46	PWR	06/29	Saha	Discreate 3VALW and 3VSRC.	Add PU17 SN74AHC1G32DCKR OR GATE(SA00732018L), PR49 1K_0402_1%(SD03410018L) PQ82 FDC655BN_NL(SB000004P8L) Delete PR352 1K_0402_1%(SD03410018L) PR351 0_0402_5%(SD02800008L) PR350 0_0402_5%(SD02800008L) PU18 74AHCT1G08GW AND GATE(SA00000L30L)	0.3

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16	46	PWR	06/29	Saha	Add V+ input Resistor	Add PR27 0_1206_5%(SD00100000L)	0.3
17	45/51	PWR	06/29	Saha	Battery conn. and battery selector +3VSRC change to +3VALW	Rename +3VSRC to +3VALW	0.3
18	47	PWR	06/29	Saha	ISL6227 Issue change 1.05V/1.5VHigh/Low side MOSFET change 1.05V choke adjust OCP and ISEN value	VCC Change from +5VRUN to +5VSUS. EN1 and EN2 change from RUNPWROK to RUN_ON. PR221 change from 20K_04-2_1%(SD03420028L) to 19.6K_0402_1%(SD00000358L) PQ8 change from FDS6994S(SB56994008L) to FDS8880(SB000004U8L) Add PQ83 FDS6670AS(SB000004T8L) PQ38 change from BSO072N03S(SB00000418L) to FDS8880(SB000004U8L) PQ40 change from BSO072N03S(SB00000418L) to FDS6670AS(SB000004T8L) PL27 change from 1.4U_HMU1350(SH000004H8L) to 1.5U_SIL104(SH04215A08L) Add PC261 0.01U_0402(SE068103K8) Add PC262 and PC263 2200P_0402(SE074222K8L) PR219 change from 825_0402_1%(SD03482508L) to 1.43K_0402_1%(SD03414318L) PR220 change from 825_0402_1%(SD03482508L) to 2.1K_0402_1%(SD03421018L) PR223 change from 69.8K_0402_1%(SD03469828L) to 124K_0402_1%(SD03412438L) PR224 change from 60.4K_0402_1%(SD03460428L) to 124K_0402_1%(SD03412438L)	0.3
19	49	PWR	06/29	Saha	ISL6260 Issue	Delete PR338, PR339 and PR340 2.7_0603_5% Change PC246, PC247, PC248 to 1500P_0805-----Unpop Change PH1 from ERTJ1VR103J(SL20000020L) to NCP15WM474J03RB(SL20000098L) PR284 change from 15.8K_0402_1%(SD03415828L) to 0_0402_5%(SD02800008L) Add PC260 0.1U_0603(SE042104K8L)	0.3
20	50	PWR	06/29	Saha	Change +VCHGR output CAP from 1206 to 1210	PC113 and PC114 change from 10U_1206(SE142106M8L) to 10U_1210(SE056106K8L)	0.3
21	47	PWR	08/12	Saha	Add VSEN capacitor	Add PC265 and PC264 100P_0402_50V8K(SE071101K8L)	0.4
22	47	PWR	08/12	Saha	Delete PGOOD pull high resistor	Delete PR283 100K_0402_1%(SD03410038L) De-pop PR195 100K_0402_1%(SD03410038L)	0.4
23	48	PWR	08/12	Saha	Delete reliability test resistor	Delete PR283 110K_0603_1%, PR359 0_0603_1%, and PR82 59.6K_0603_1%	0.4
24	49	PWR	08/12	Saha	Adjust VCORE load line	PR267 change from 7.87K_0402_1%(SD03478718L) to 9.09K_0402_1%(SD034909100) PR231, PR331, and PR270 change from 7.68K_0402_1%(SD00000238L) to 7.68K_0805_1%(SD00000B08L)	0.4
25	49	PWR	08/12	Saha	Delete H_PROCHOT# resistor	Delete PR235 0_0402_5%(SD02800008L)	0.4
26	50	PWR	10/17	Saha	Add RC filter in FBSA/B PIN	Add PR368 and PR369 100_0402_5%(SD02810008L) Add PC266 and PC267 0.01U_0603_50V7K(SE025103K8L) Un-pop PR371 and PR370 0_0402_5%	0.5
27	46	PWR	10/17	Saha	EMI request: change BST3 resestor	Change PR32 from 0_0603_5%(SD01300008L) to 2.2_0603_5%(SD013220B8L)	0.5
28	46	PWR	10/17	Saha	change 3V out put CAP height	change PC31 from 330U_6.3V_R25 H1.9(SGA00001C8L) to 330U_6.3V_R25 H2.8(SGA0000089L)	0.5

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29	50	PWR	10/17	Saha	Populate UL circuit	Populate PR361-PR367, PC254-259, PU19, PQ81. Change PR361 from 80.6k to 0. Change PR362 from 200k to 301k. Change PR363 from 121k to 59k. Change PR364 from 3.01k to 27.4k. Change PR365k from 499k to 4.32Meg.	0.5
30	49	PWR	10/20	Saha	Change VCC_CORE OCP, SOFT, and DPRSTP# value	PR260 change from 20K_0402_1%(SD03420028L) to 11.5K_0402_1%(SD03411520L) PC187 change from 0.022U_0402_16V7K(SE076223K8L) to 0.01U_0402_16V7K(SE076103K8L) Add PR372 0_0402_5%(SD02800008L) Delete PR246 0_0402_5%(SD02800008L) Un-pop PR249 0_0402_5%(SD02800008L)	0.5
31	48	PWR	10/20	Saha	Change PU6 BST resistor	PR73 change from 0_0603_5%(SD01300008L) to 1_0603_5%(SD013100B8L)	0.5
32	44	PWR	10/20	Saha	Change PQ2 from RUH002N06 to 3904	PQ2 change from RHU002N06(SB50206008L) to MMST3904(SB000002R0L)	0.5
33	49	PWR	11/12	Saha	Adjust CPU Load Line	PR267 change from 9.09K_0402_1%(SD03490918L) to 10.5K_0402 _1%(SD03410528L) PR261 change from 3.57K_0402_1%(SD03435718L) to 2.47K_0402 _1%(SD03424318L) Add PC252 100U_25V_(6.3X7.7)(SF10004M08L) Add PC215 0.068U_10VX7R_0402 (SE102683K8L)	0.5
34	50	PWR	12/6	Saha	Deeply dischargered battery problem.	Add PD54 1SS355_sod323(SC1SS35500L) Add PR373 1K_0603_1%(SD01410018L)	0.5
35	50	PWR	12/6	Saha	Follow Coe A09 schematic	Add PC267 3300PF_0402_50V7K(SE074332K8L) Depop PC266 0.01U_0603_50V7K(SE025103K8L)	0.5
36	47	PWR	12/15	Saha	Follow GGL 1214 item19.	Depop PR12	0.6
37	49 50 46	PWR	1/7	Saha	For acoustical issue	Add PC270~PC273 and PC268 10U_1206_25V6M(SE142106M8L)	0.6