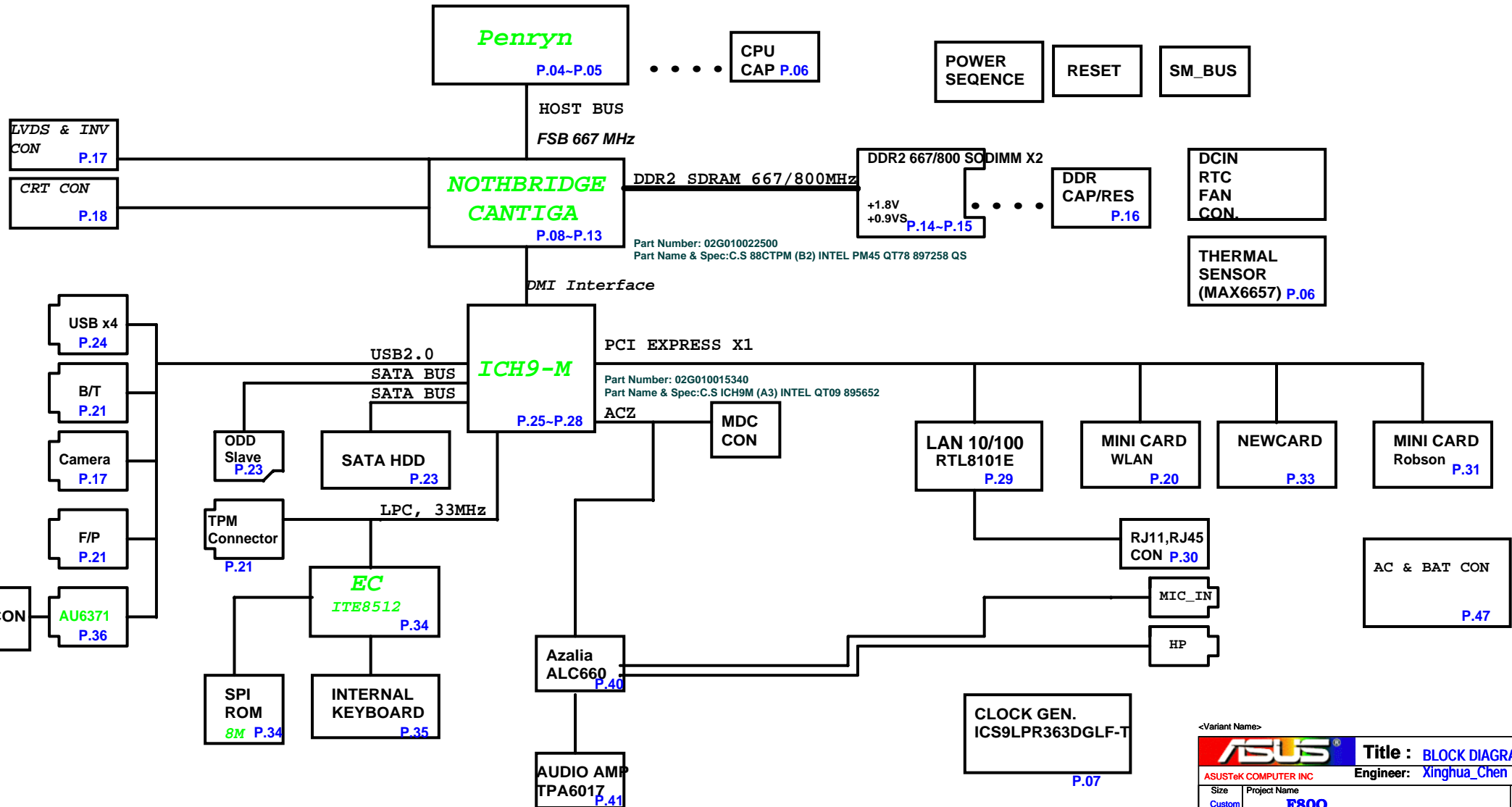
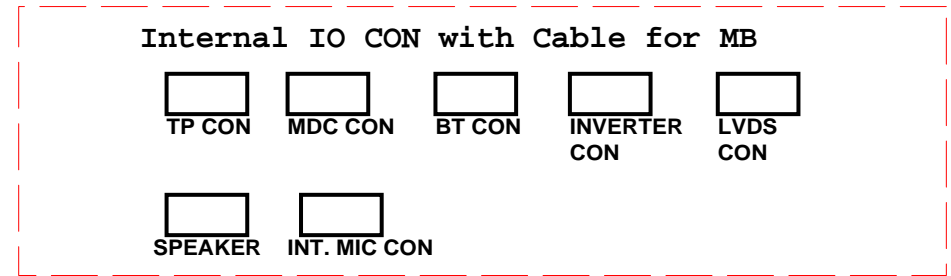
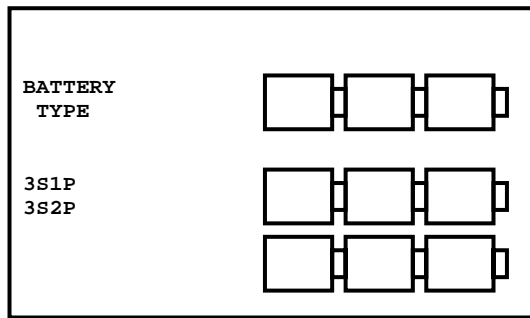


PAGE	Content
	<div><div>SYSTEM PAGE REF.</div><div>CPU-Penryn(1) CPU-Penryn(2) CPU CAP, Thermal Senor CLOCK GEN._ICS9LPR363CGLF NB_-960GL (1)--CPU NB_-960GL (2)--DDR2/PEG NB_-960GL (3)--DDR2 bus NB_-960GL (4)--POWER NB_-960GL (5)--POWER NB_-960GL (6)--GND/Strapping DDR2 SO-DIMM_0 DDR2 SO-DIMM_1 DDR2 ADDRESS TERMINATION LVDS & INVERTER CONN CRT conn. MDC,HDMI conn. PCI-E--MINI CARD--(1)_WLAN B/T,F/P,T/P& TPM B TO B CONN(M) HDD & CD-ROM CONN USB PORT SB_-ICH8M--(1)-CPU,IDE,AUDIO SB_-ICH8M--(2)-PCI,PCI-E,USB SB_-ICH8M--(3)-GPIO SB_-ICH8M--(4)-PWR/GND PCI-E--LAN_RTL8101E TRANSFORMER ROBSON EMPTY NEWCARD EC-IT8752 ISA ROM & KB CARD READER_AU6371 DISCHARGE Instant Key LEDs AZALIA-ALC662 AUDIO-AMPLIFIER MICROPHONE EMPTY EMPTY EMPTY SREW HOLE</div></div>

F80Q BLOCK DIAGRAM



Pin	Pin Name	Signal Name	Type
28	PWM0/GPA0	PWR_LED_UP#	O
29	PWM1/GPA1	CHG_LED_UP#	
32	PWM2/GPA2	BATSEL_3S#	
34	PWM4/GPA4	LCD_BL_PWM	O
35	PWM5/GPA5	FAN_PWM	O
75	GPI1	VSUS_GD	I
76	GPI2	ALL_SYS_PWRGD	
77	GPI3	CPUPWR_GD	O
122	RXD/GPB0	CHG_EN#	O
123	TXD/GPB1	PRECHG	O
126	GPB7	PM_RSMRST#	O
64	GPC3	PM_PWRBTN#	O
136	TMRI0/WUI2/GPC4	AC_IN_OC#	I
65	GPC5	OP_SD#	O
140	TMRI1/WUI3/GPC6	BAT1_IN_OC#	I
20	CK32KOUT/GPC7	RF_ON_SW#	I
22	RI1#/WUI0/GPD0	PWRLIMIT#	
25	RI2#/WUI1/GPD1	PM_SUSC#	O
37	GINT/GPD5	LCD_BACKOFF#	O
53	TACH0/GPD6	FAN0_TACH	O
23	ADC4/GPE0	VSUS_ON	O
94	ADC5/GPE1	SUSC_EC#	O
95	ADC6/GPE2	SUSB_EC1#	I
96	ADC7/GPE3	CPU_VRON	O
141	PWRSW/GPE4	PWR_SW#	I
39	WUI5/GPE5	BAT2_IN_OC#	I
21	LPCPD#/WUI6/GPE6	LID_EC#	I
121	GPJ1	PM_SUSB#	I
105	GPH0	PM_CLKRUN#	
108	GPH3	BAT_LEARN	O
110	GPH5	NUM_LED#	O
111	GPH6	CAP_LED#	O
99	PS2CLK1/GPF2	MARATHON#	I
101	PS2CLK2/GPF4	TP_CLK	O
102	PS2DAT2/GPF5	TP_DAT	I/O
124	SMCLK0/GPB3	SMB0_CLK	O
125	SMDAT0/GPB4	SMB0_DAT	I/O
129	SMCLK1/GPC1	SMB1_CLK	I
130	SMDAT1/GPC2	SMB1_DAT	I/O
131	GPF6	THRO_CPU	O
84	GPJ0	EC_CLK_EN	O
85	GPJ1	ICH8_PWROK	O
87	GPJ3	BATSEL_2P#	O
26	GPD2	PLT_RST_BUF#	I
27	GPD3	EXT_SC#	O
19	GPD4	EXTSM#	O
142	GPB5	A20GATE	O
4	GPB6	RCIN#	O

<i>Pin</i>	<i>Pin Name</i>	<i>Signal Name</i>	<i>Type</i>

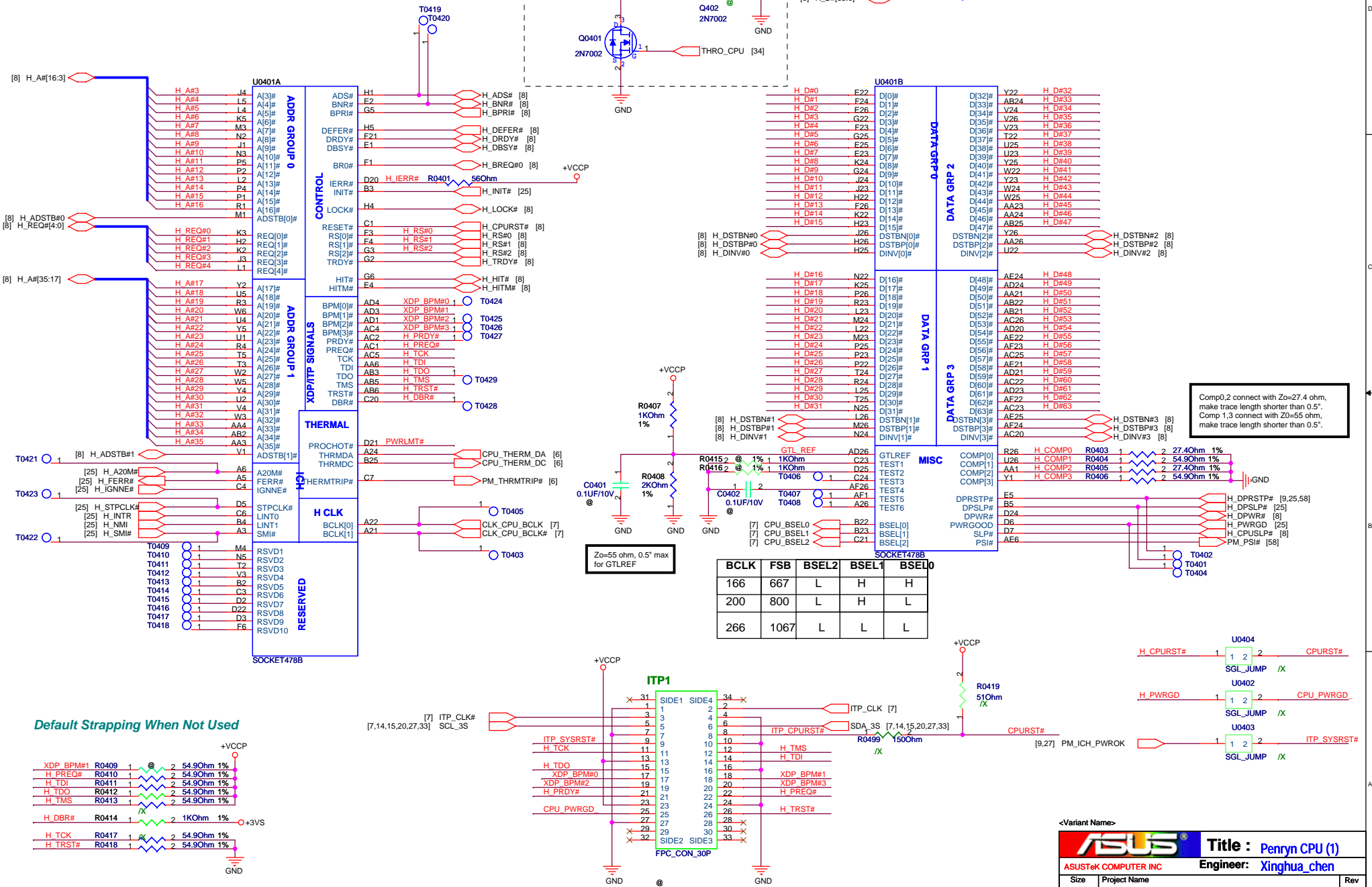
SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor(MAX6657)	1001100x (98)

Pin.	Default	Use As	Signal Name	Power	Mux
GPIO 00	i	GPI	PM_BMBUSY#	+3VS	BM_BUSY#
GPIO 01	i 0	GPI	BT_DET#	+3VS	TACH1
GPIO [5:2]	i H-Z	GPI	PCI_INT[H:E]#	+3VS	PIRQ[H:E]#
GPIO 06	i 0	GPO	BIOS_REC_? (TP)	+3VS	TACH2
GPIO 07	i 0	GPO	802_LED_EN	+3VS	TACH3
GPIO 08	i	GPI	EXTSMI#	+3VSUS	N/A
GPIO 09	i H-Z	GPO	LAN_WOL_EN_? (TP)	+3VSUS	WOL_EN
GPIO 10	i H-Z	GPO	RST#_NEWCARD	+3VSUS	ALERT#
GPIO 11	Nat H-Z	Native	SMB_ALERT#	+3VSUS	SMBALERT#
GPIO 12	i	GPI	KBC_SC#	+3VSUS	GLAN_DOCK#
GPIO 13	Nat	GPI	N/A	+3VSUS	ENERGY_DETECT
GPIO 14	i H-Z	GPI	N/A	+3VSUS	NETDETECT
GPIO 15	Nat 1	Native	STP_PC#	+3VSUS	STP_PC#, No-GP
GPIO 16	Nat 0	Native	PM DPRSLPVR	+3VS	DPRSLPVR
GPIO 17	i 1	GPO	WLAN_ON#	+3VS	TACH0
GPIO 18	0 freq	GPO	N/A	+3VS	N/A
GPIO 19	i H-Z	GPO	CPU_SELECT	+3VS	SATA1GP
GPIO 20	0 1	GPO	BT_LED_EN	+3VS	N/A
GPIO 21	i	GPI	CPPE#_DET	+3VS	SATA0GP
GPIO 22	i	GPI	N/A	+3VS	SCLKCK
GPIO 23	Nat	Native	N/A	+3VS	LDR01#
GPIO 24	0 H-Z	GPO	MSK_PCIRST	+3VSUS	CLKP0Q/MEM_LE
GPIO 25	Nat 1	Native	STP_CPU#	+3VS	STP_CPU#, No-GP
GPIO 26	Nat	GPO	CPPE_EN	+3VSUS	S4_STATE#
GPIO 27	0 0	GPO	BT_ON#	+3VSUS	DRT_STATE0
GPIO 28	0 0	GPO	CB_SD#_? (TP)	+3VSUS	DRT_STATE1
GPIO 29	Nat	Native	USB_OC#5	+3VSUS	OC5#
GPIO 30	Nat	Native	USB_OC#6	+3VSUS	OC6#
GPIO 31	Nat	Native	USB_OC#7	+3VSUS	OC7#
GPIO 32	0 0	Native	PM_CLKRUN#	+3VS	CLKRUN#, No-GP
GPIO 33	0 1	GPO	N/A	+3VS	HDA_DOCK_EN#
GPIO 34	0 0	GPO	N/A	+3VS	HDA_DOCK_RST#
GPIO 35	0 0	GPO	SATACLKREQ#_? (TP)	+3VS	SATACLKREQ#
GPIO 36	i	GPO	EMAIL_LED#_? (TP)	+3VS	SATA2GP
GPIO 37	i 0	GPI	PCB_ID0	+3VS	SATA3GP
GPIO 38	i	GPI	PCB_ID1	+3VS	SLOAD

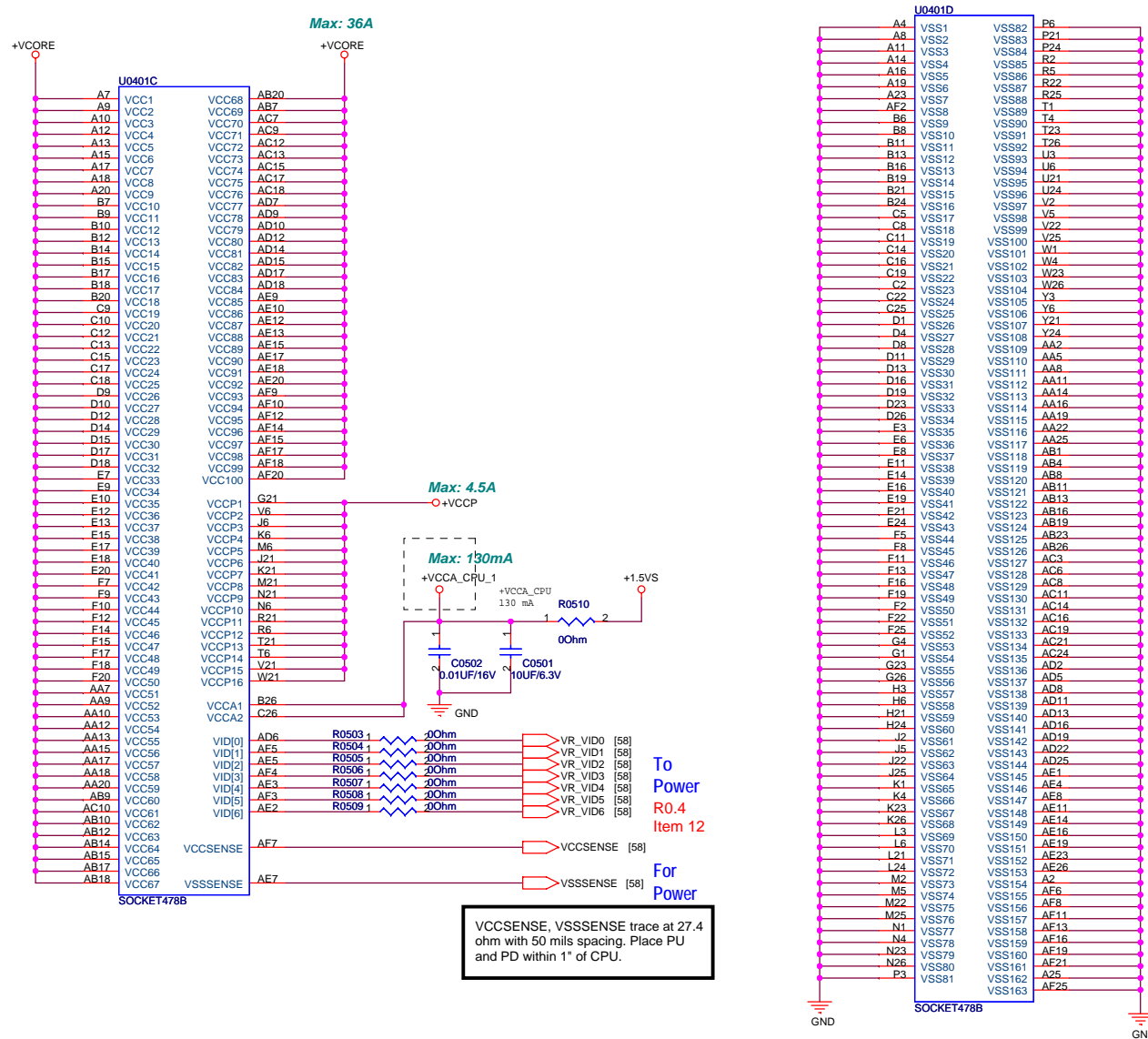
Pin	Use As	Signal Name	Power	Mux
GPIO 39 <small>Default: #57#</small>	GPI	PCB_ID2	+3VS	SDATAOUT0
GPIO [40:43]Native	Native	USB_OC[4:1]#	+3VSUS	OC[4:1]#
GPIO [47:44]n/a	N/A	N/A	N/A	No implement
GPIO 48 <small>Default: #57#</small>	Native		+3VS	SDATAOUT1
GPIO 49 Native	Native	H_PWRGD	+VCORE	CPUPWRGD
GPIO 50 Native	Native	PCI_REQ1#	+5VS	REQ1#
GPIO 51 Native	Native	PCI_GNT1#	+3VS	GNT1#
GPIO 52 Native	Native	PCI_REQ2#	+5VS	REQ2#
GPIO 53 Native	Native	PCI_GNT2#	+3VS	GNT2#
GPIO 54 Native	Native	PCI_REQ3#	+5VS	REQ3#
GPIO 55 Native	Native	PCI_GNT3#	+3VS	GNT3#

0, in Mobile

		Title : <u>Schematic Info.</u>	
ASUSTeK COMPUTER INC		Engineer: <u>CH Lin</u>	
Size <u>Custom</u>	Project Name <u>F80L</u>		Rev <u>2.00</u>
Date: <u>Friday, May 23, 2008</u>		Sheet <u>3</u>	of <u>59</u>



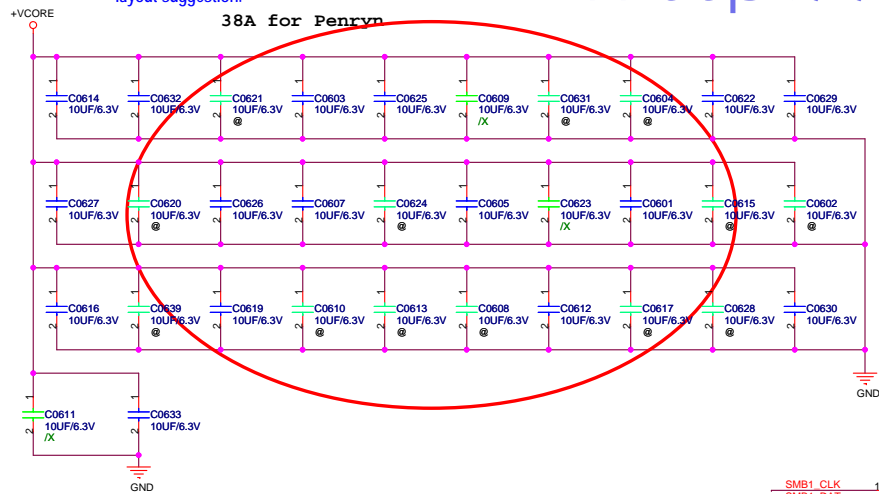
<Variant Name>



Place on L1/L8, upper/lower side of inside socket. according intel layout suggestion.

+VCCP Decoupling Capacitor
(Place near CPU)

38A for Penryn

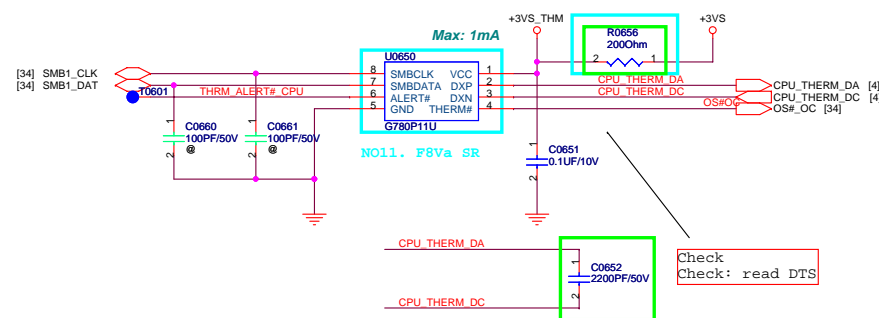


Decoupling guide from INTEL

VCCP	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

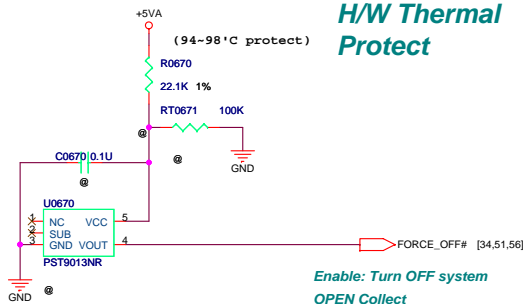
Optimize it !_0907

Thermal Sensor

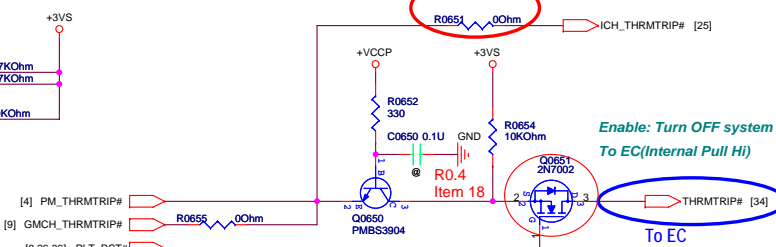


H/W Thermal Protect

(94~98°C protect)



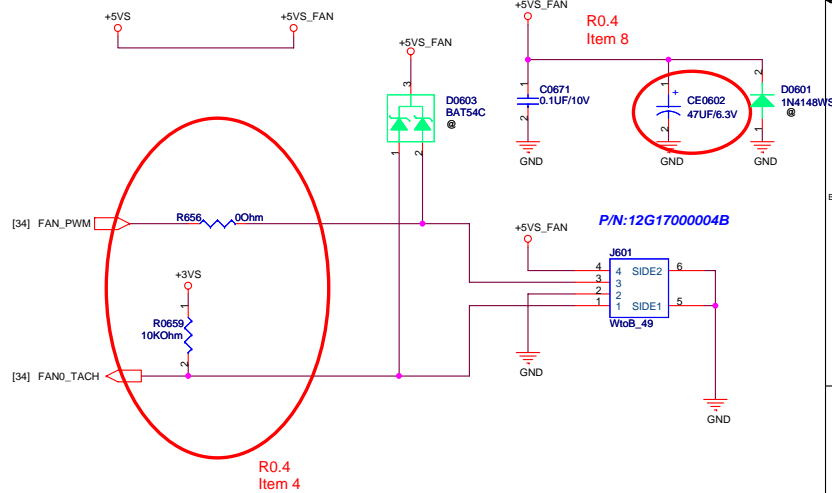
Sub-SYS=CPU



Enable: Turn OFF system
To EC(internal Pull Hi)

To EC

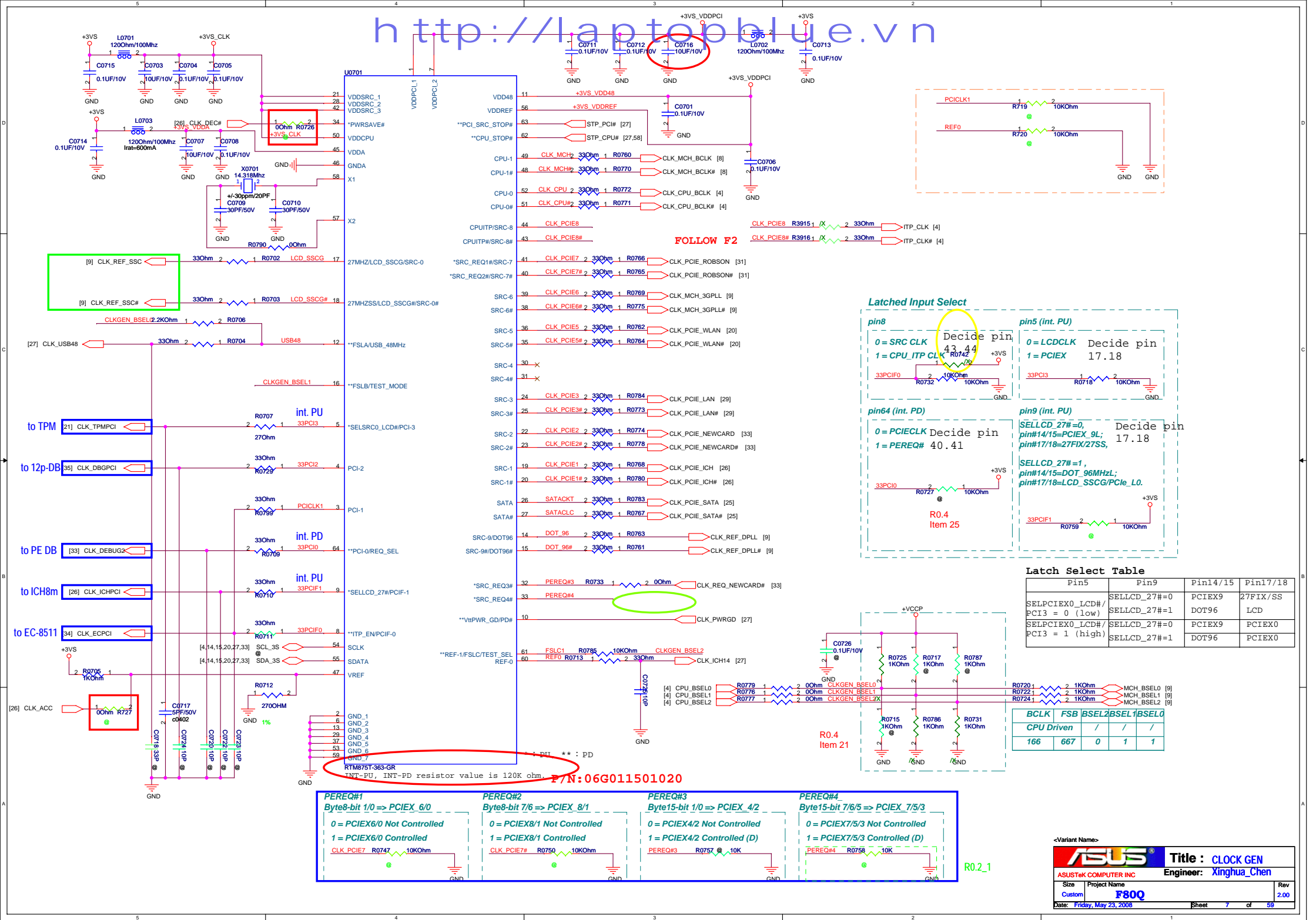
Sub-SYS=FAN



P/N: 12G17000004B

<Variant Name>

ASUS		CPU CAP, Thermal Sensor	
ASUSTek COMPUTER INC		Title :	
Size		Engineer: Xinghua_Chen	
Custom	Project Name	Rev	
F80Q		2.00	
Date: Friday, May 23, 2008		Sheet 6 of 59	



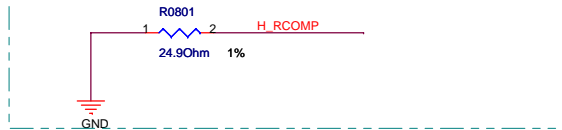
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[4] H_A#[35:3]  H_A#[35:3]

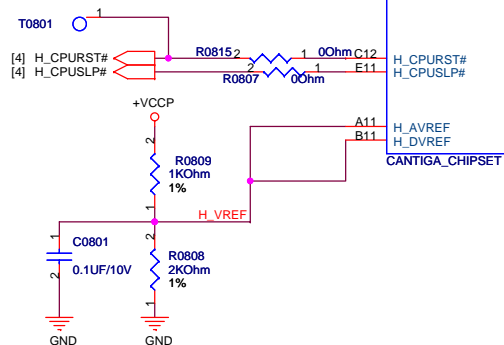
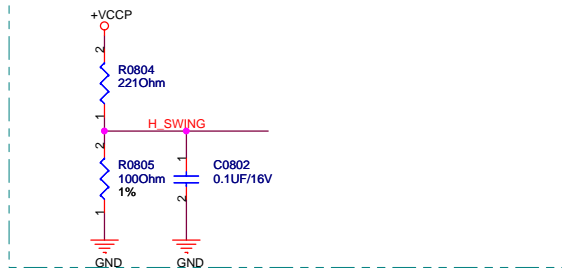
RCOMP

For Calibrating the FSB I/O Buffer



Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits



H_D#0	F2	H_D#_0
H_D#1	G8	H_D#_1
H_D#2	F8	H_D#_2
H_D#3	E6	H_D#_3
H_D#4	G2	H_D#_4
H_D#5	H6	H_D#_5
H_D#6	H2	H_D#_6
H_D#7	F6	H_D#_7
H_D#8	D4	H_D#_8
H_D#9	H3	H_D#_9
H_D#10	M9	H_D#_10
H_D#11	M11	H_D#_11
H_D#12	J1	H_D#_12
H_D#13	J2	H_D#_13
H_D#14	N12	H_D#_14
H_D#15	J6	H_D#_15
H_D#16	P2	H_D#_16
H_D#17	L2	H_D#_17
H_D#18	R2	H_D#_18
H_D#19	N9	H_D#_19
H_D#20	L6	H_D#_20
H_D#21	M5	H_D#_21
H_D#22	J3	H_D#_22
H_D#23	N2	H_D#_23
H_D#24	R1	H_D#_24
H_D#25	N5	H_D#_25
H_D#26	N6	H_D#_26
H_D#27	P13	H_D#_27
H_D#28	N8	H_D#_28
H_D#29	L7	H_D#_29
H_D#30	N10	H_D#_30
H_D#31	M3	H_D#_31
H_D#32	Y3	H_D#_32
H_D#33	AD14	H_D#_33
H_D#34	Y6	H_D#_34
H_D#35	Y10	H_D#_35
H_D#36	Y12	H_D#_36
H_D#37	Y14	H_D#_37
H_D#38	Y7	H_D#_38
H_D#39	W2	H_D#_39
H_D#40	AA8	H_D#_40
H_D#41	Y9	H_D#_41
H_D#42	AA13	H_D#_42
H_D#43	AA9	H_D#_43
H_D#44	AA11	H_D#_44
H_D#45	AD11	H_D#_45
H_D#46	AD10	H_D#_46
H_D#47	AD13	H_D#_47
H_D#48	AE12	H_D#_48
H_D#49	AE9	H_D#_49
H_D#50	AA2	H_D#_50
H_D#51	AD8	H_D#_51
H_D#52	AA3	H_D#_52
H_D#53	AD3	H_D#_53
H_D#54	AD7	H_D#_54
H_D#55	AE14	H_D#_55
H_D#56	AF3	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AE3	H_D#_58
H_D#59	AC3	H_D#_59
H_D#60	AE11	H_D#_60
H_D#61	AE8	H_D#_61
H_D#62	AG2	H_D#_62
H_D#63	AD6	H_D#_63

H_SWING C5
H_RCOMP E3

HOST


H_A#_3	A14	H_A#3
H_A#_4	C15	H_A#4
H_A#_5	F16	H_A#5
H_A#_6	H13	H_A#6
H_A#_7	C18	H_A#7
H_A#_8	M16	H_A#8
H_A#_9	J13	H_A#9
H_A#_10	P16	H_A#10
H_A#_11	R16	H_A#11
H_A#_12	N17	H_A#12
H_A#_13	M13	H_A#13
H_A#_14	E17	H_A#14
H_A#_15	P17	H_A#15
H_A#_16	E17	H_A#16
H_A#_17	G20	H_A#17
H_A#_18	B19	H_A#18
H_A#_19	J16	H_A#19
H_A#_20	E20	H_A#20
H_A#_21	H16	H_A#21
H_A#_22	J20	H_A#22
H_A#_23	A17	H_A#23
H_A#_24	B17	H_A#24
H_A#_25	L16	H_A#25
H_A#_26	C21	H_A#26
H_A#_27	J17	H_A#27
H_A#_28	H20	H_A#28
H_A#_29	B18	H_A#29
H_A#_30	K17	H_A#30
H_A#_31	B20	H_A#31
H_A#_32	F21	H_A#32
H_A#_33	K21	H_A#33
H_A#_34	L20	H_A#34
H_A#_35		
H_ADS#	H12	H_ADS#
H_ADSTB#_0	B16	H_ADSTB#0
H_ADSTB#_1	G17	H_ADSTB#1
H_BNR#	A9	H_BNR#
H_BPRI#	F11	H_BPRI#
H_BREQ#_0	G12	H_BREQ#0
H_DEFER#	E9	H_DEFER#
H_DBSY#	B10	H_DBSY#
HPL_L_CLK	AH7	CLK_MCH_BCLK [7]
HPL_L_CLK#	J11	H_DPWR#
H_DPWR#	F9	H_DRDY#
H_DRDY#	H9	H_HIT#
H_HIT#	E12	H_HITM#
H_LOCK#	H11	H_LOCK#
H_TRDY#	C9	H_TRDY#
H_DINV#_0	J8	H_DINV#0
H_DINV#_1	L3	H_DINV#1
H_DINV#_2	Y13	H_DINV#2
H_DINV#_3	Y1	H_DINV#3
H_DSTBN#_0	L10	H_DSTBN#0
H_DSTBN#_1	M7	H_DSTBN#1
H_DSTBN#_2	AA5	H_DSTBN#2
H_DSTBN#_3	AE6	H_DSTBN#3
H_DSTBP#_0	L9	H_DSTBP#0
H_DSTBP#_1	M8	H_DSTBP#1
H_DSTBP#_2	AA6	H_DSTBP#2
H_DSTBP#_3	AE5	H_DSTBP#3
H_REQ#_0	B15	H_REQ#0
H_REQ#_1	K13	H_REQ#1
H_REQ#_2	F13	H_REQ#2
H_REQ#_3	B13	H_REQ#3
H_REQ#_4	B14	H_REQ#4
H_RS#_0	B6	H_RS#0
H_RS#_1	F12	H_RS#1
H_RS#_2	C8	H_RS#2

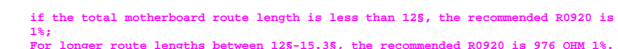
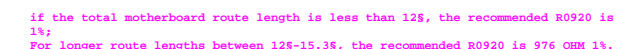
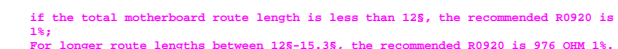
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Part Number: 02G010022500

Part Name & Spec: C.S 88CTPM (B2) INTEL PM45 QT78 897258 QS

<Variant Name>

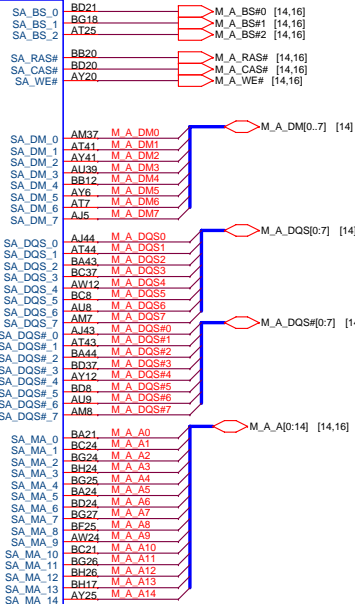
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ASUSTeK COMPUTER INC		Engineer: Xinghua_Chen	
Size Custom	Project Name F80Q	Date: Friday, May 23, 2008	Rev 2.00
Sheet 8 of 59			



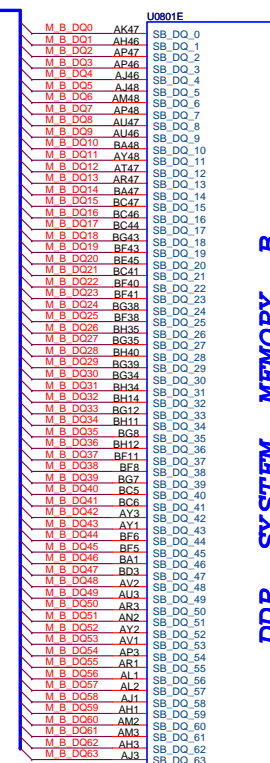
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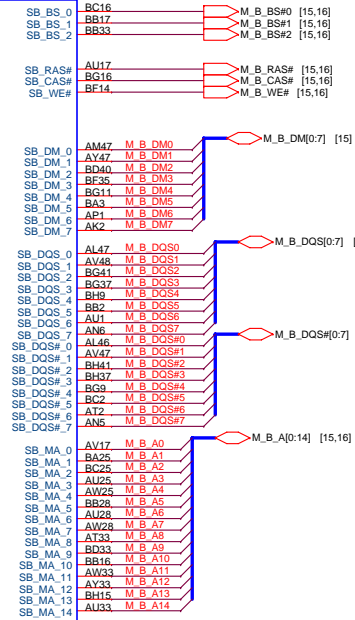
CANTIGA_CHIPSET



[15] M_B_DQ[0:63]

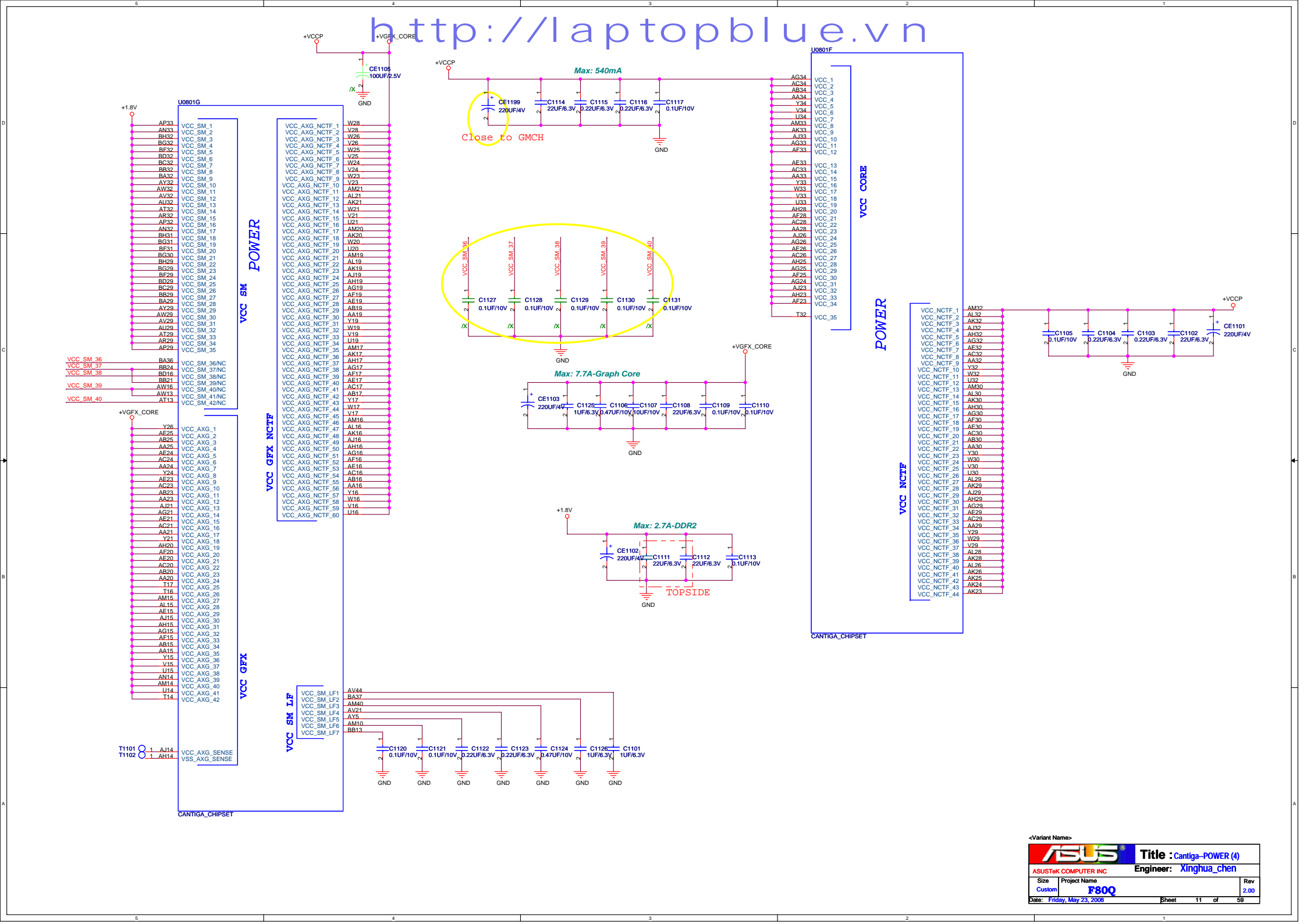


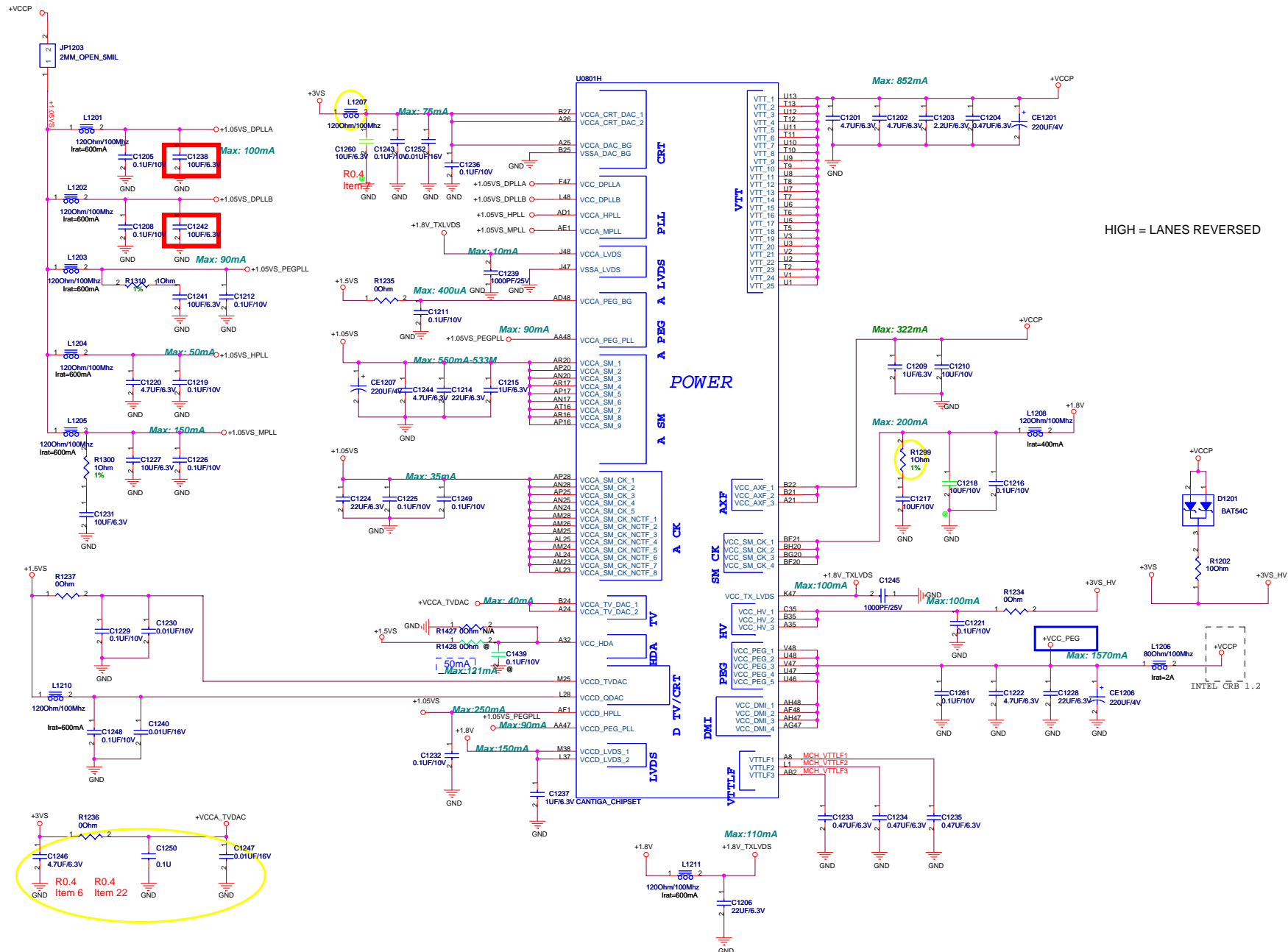
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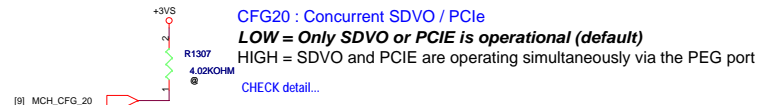
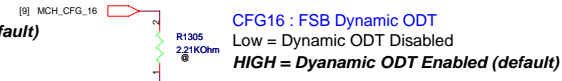
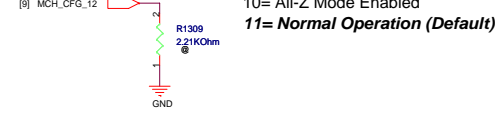
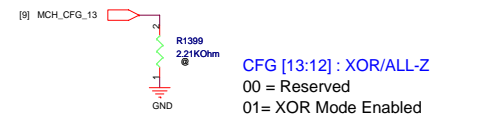
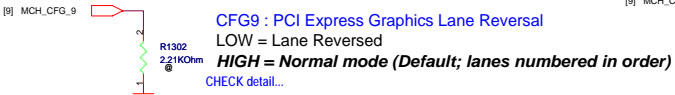
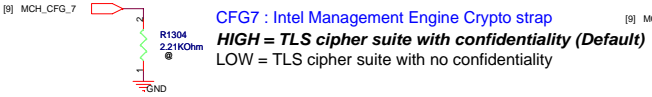
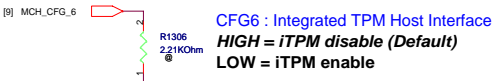
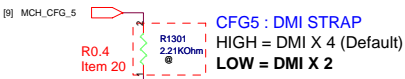
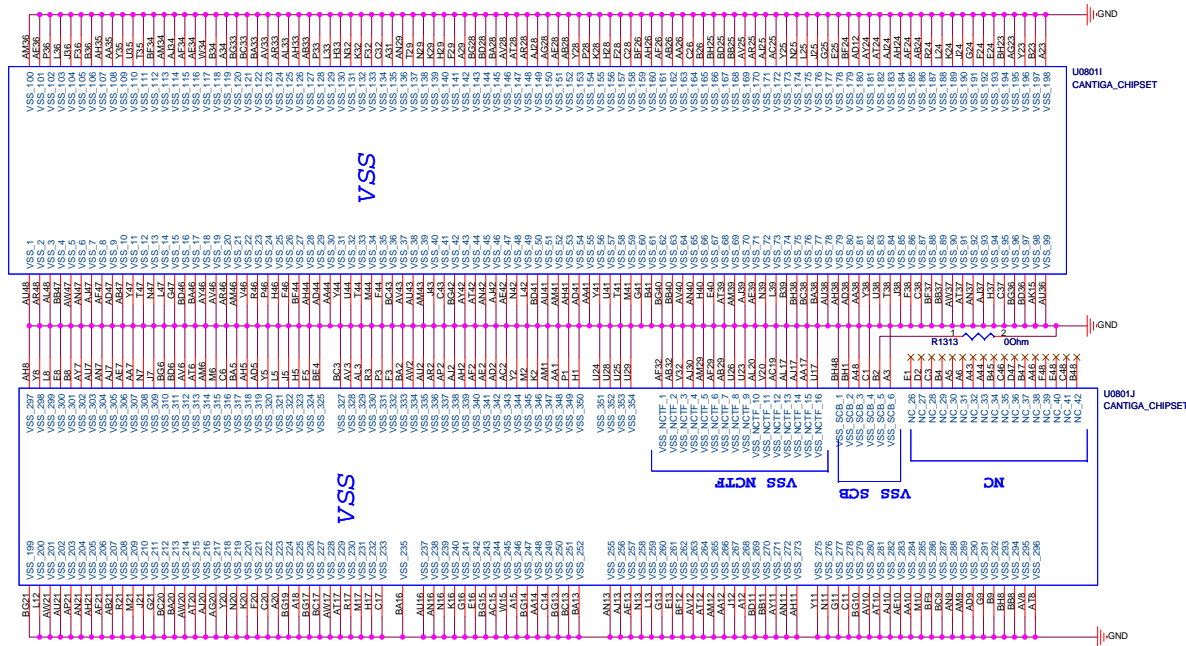


<Variant Name>

ASUS Title : Cantiga-DDR2 bus (3)
ASUSTeK COMPUTER INC Engineer: Xinghua_Chen
Size Project Name Rev
Custom F80Q 2.00
Date: Friday, May 23, 2008 Sheet 10 of 59

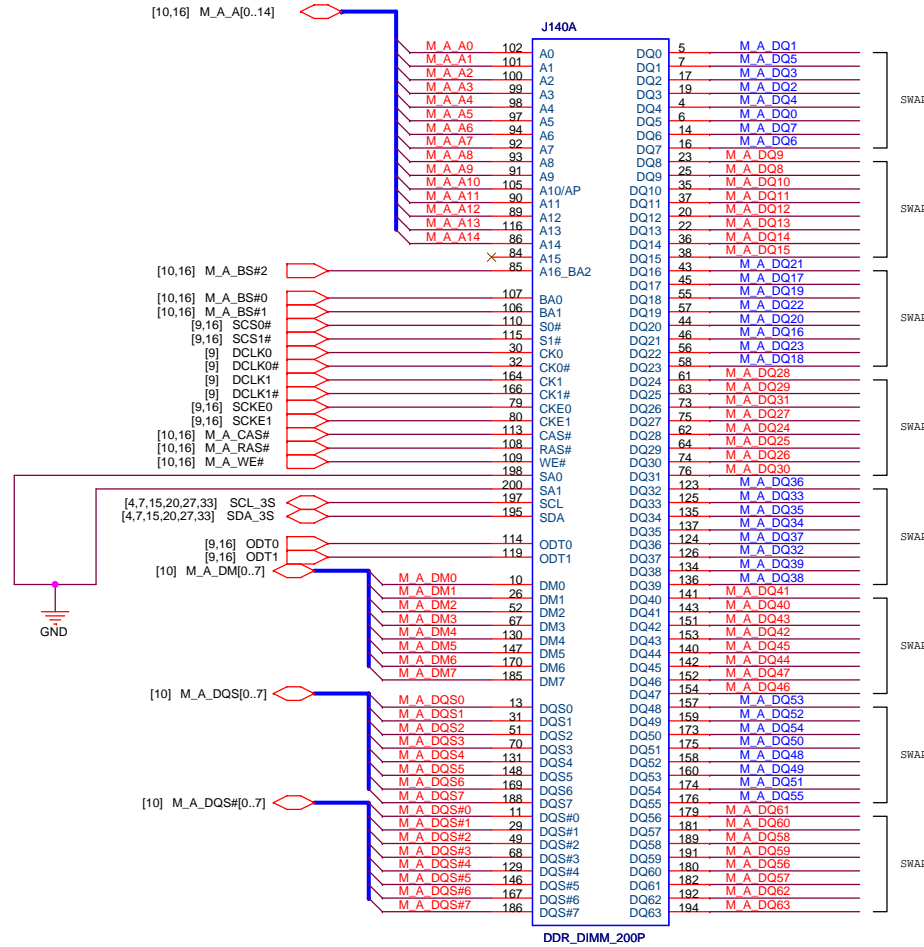




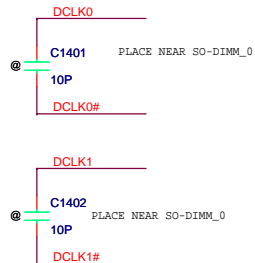
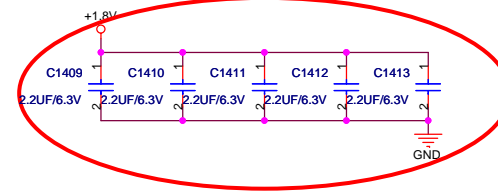
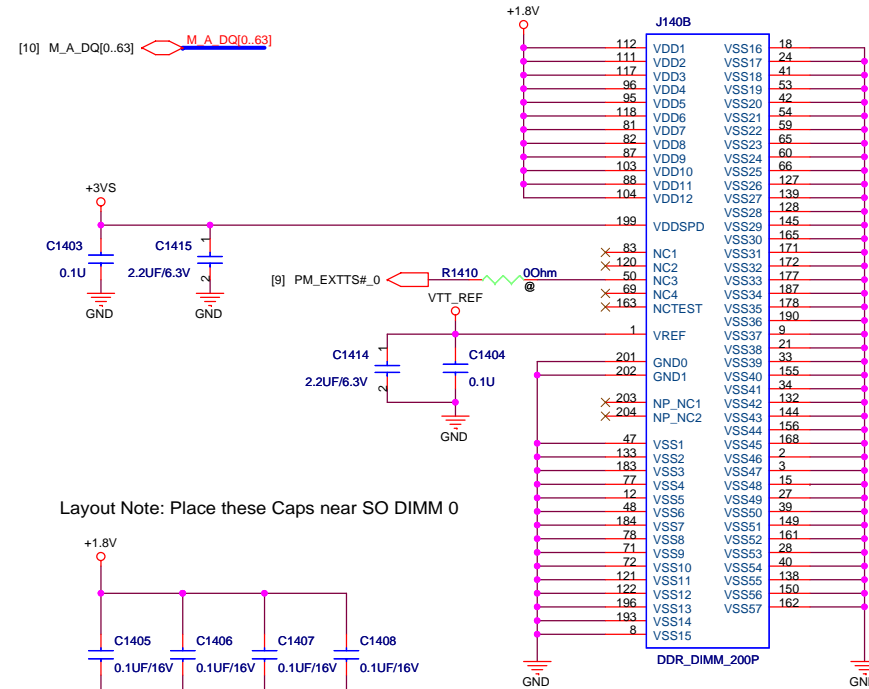


Reverse Type

http://laptopblue.vn

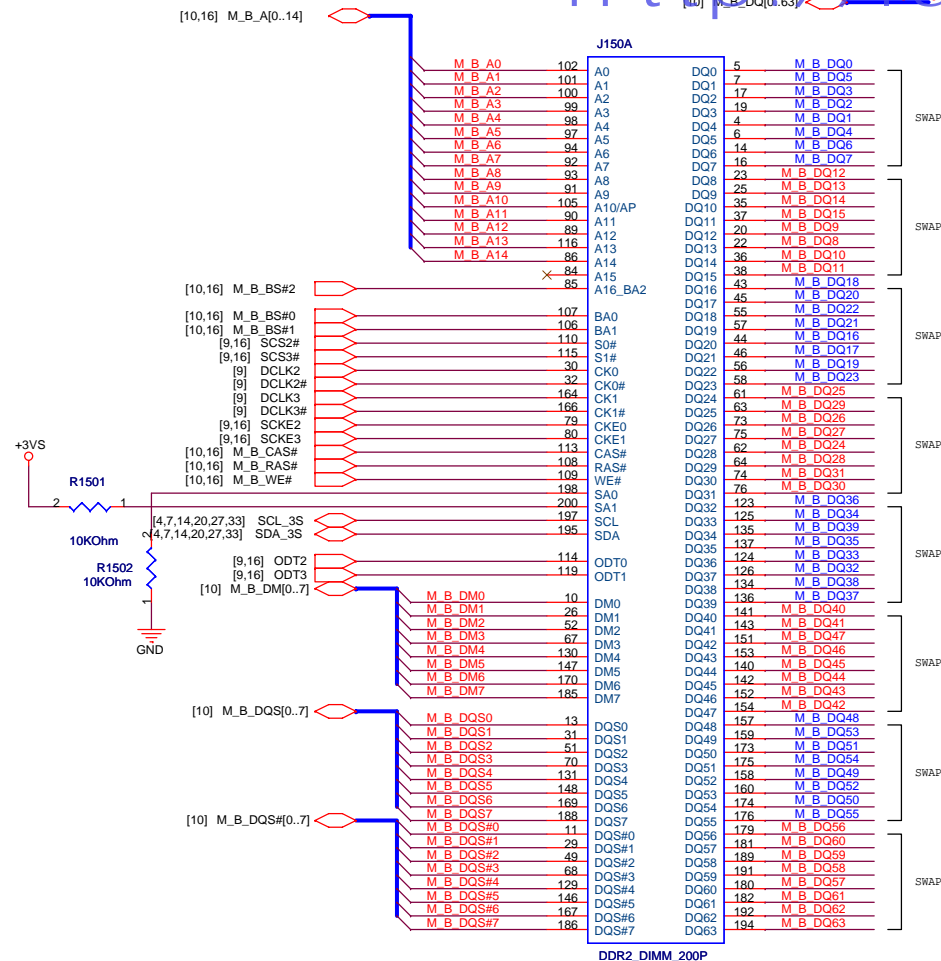


P/N : 12G025122006 H:5.2mm

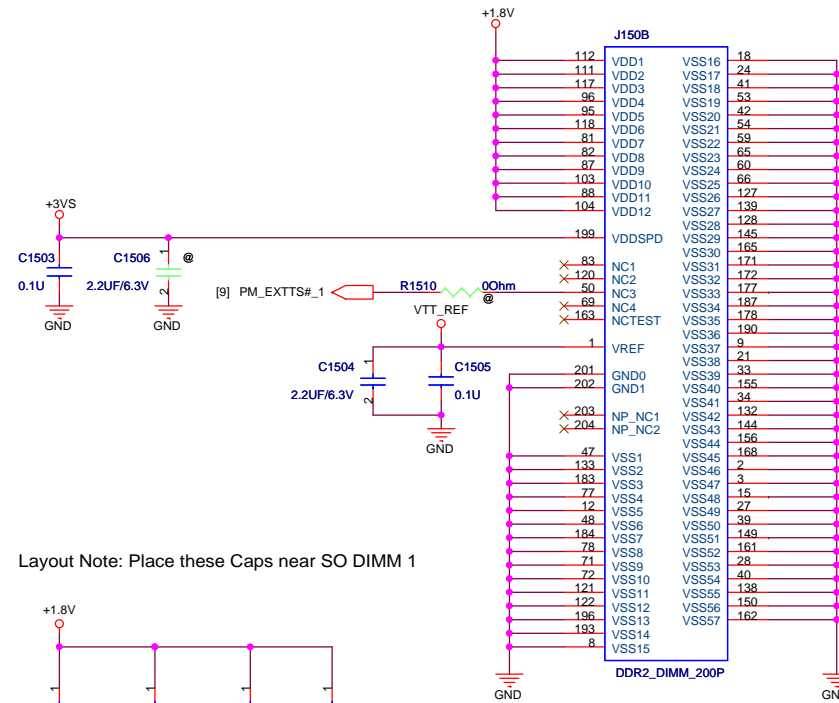


<Variant Name>

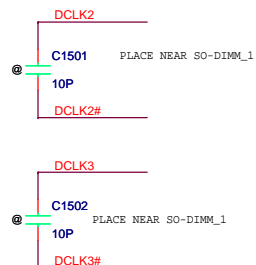
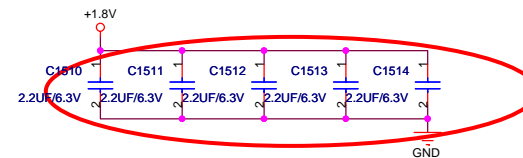
ASUS		Title : DDR SO-DIMM 0	
ASUSTeK COMPUTER INC		Engineer: Xinghua_Chen	
Size	Project Name	Rev	
Custom	F80Q	2.00	
Date: Friday, May 23, 2008		Sheet	14 of 59



P/N : 12G025C22002 H:9.2mm

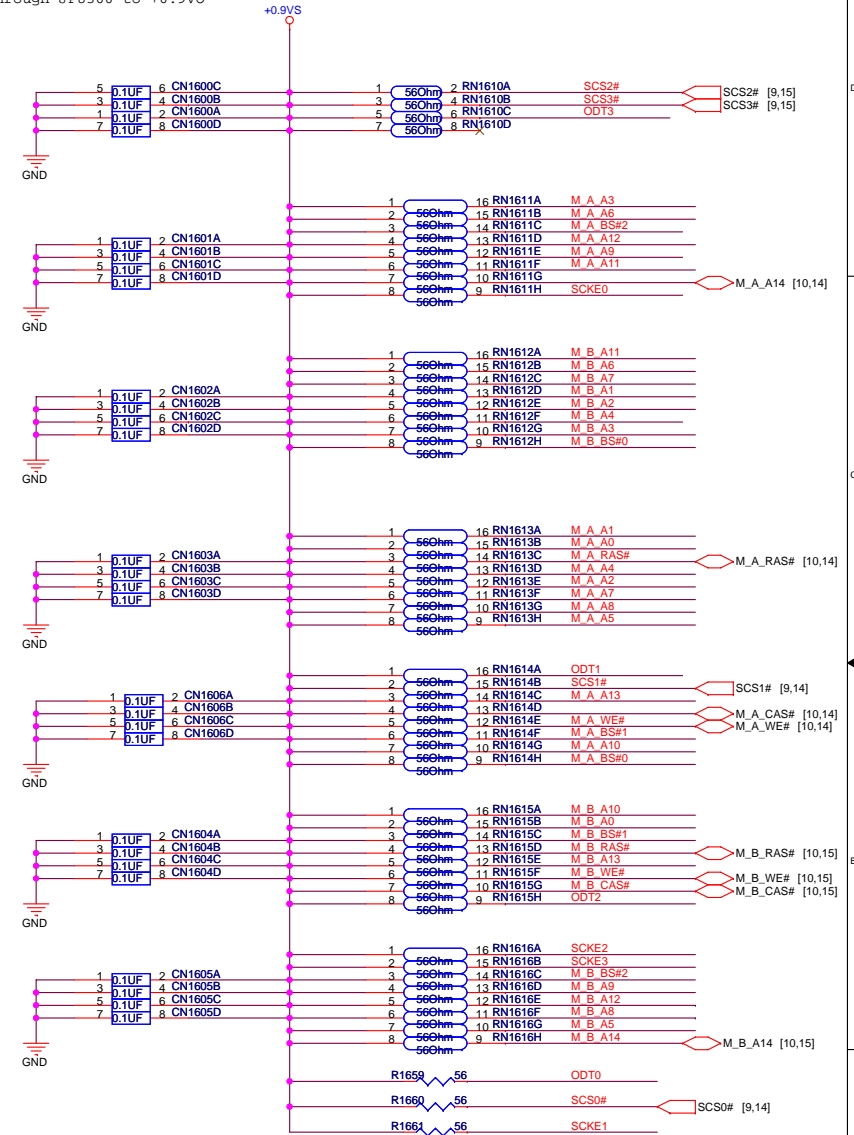
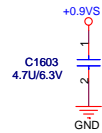
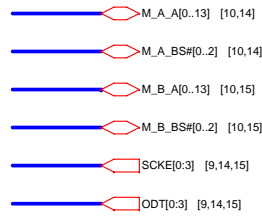
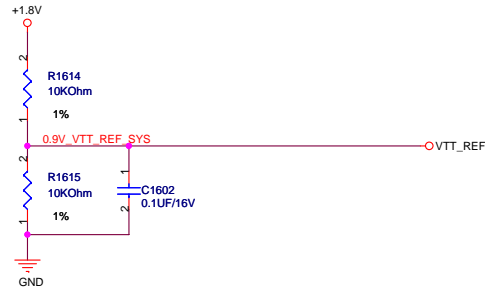


Layout Note: Place these Caps near SO DIMM 1



+0.9VS through JP8300 to +0.9V0

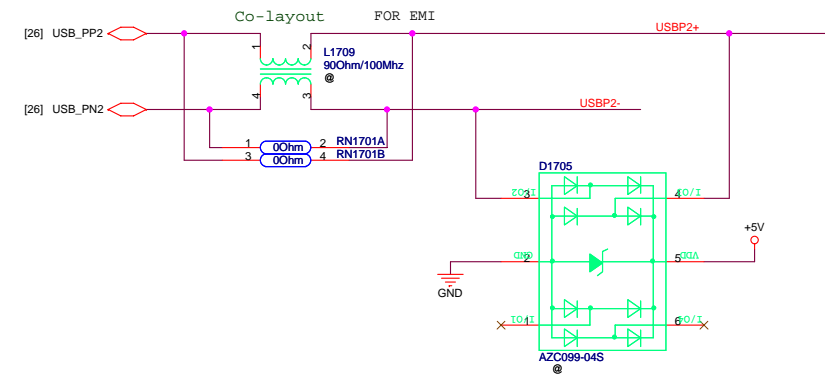
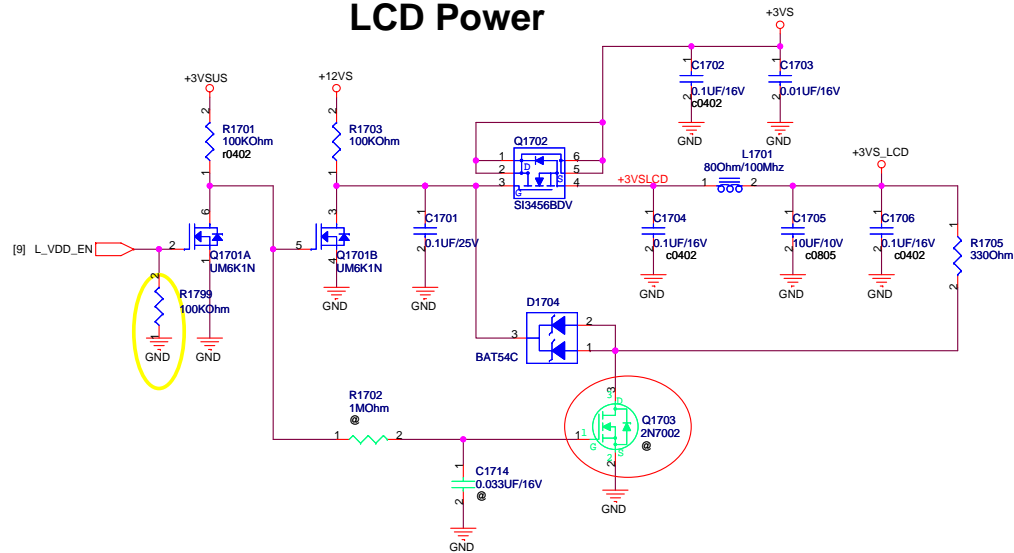
SWAPPED



Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

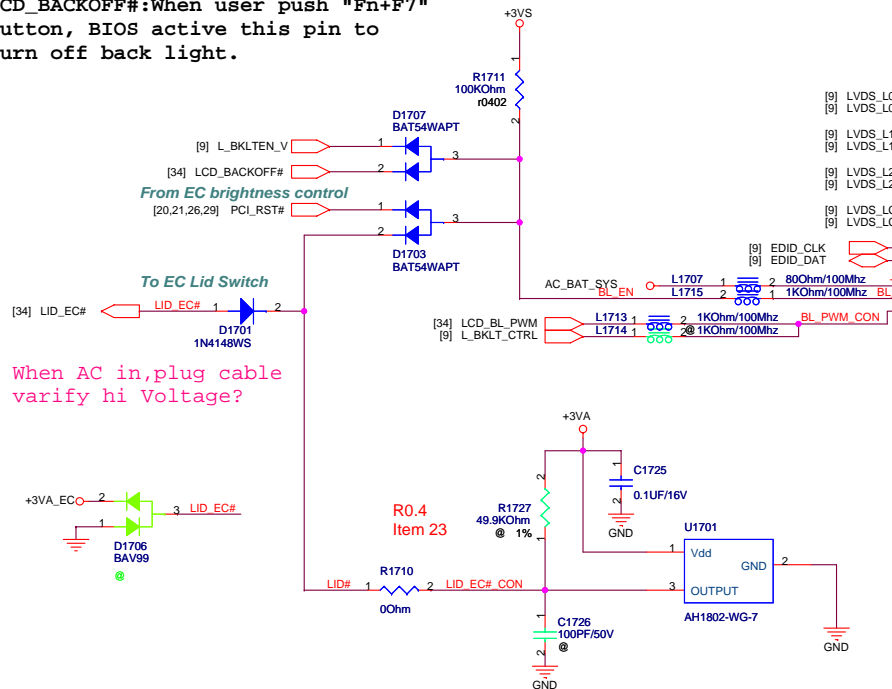
<Variant Name>

LCD Power

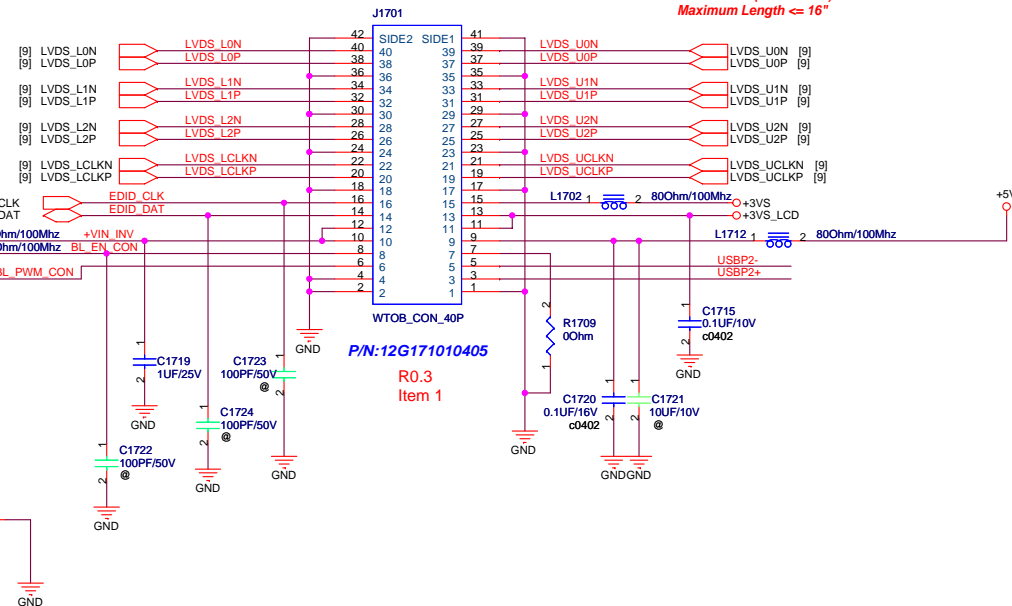


BIOS

LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.



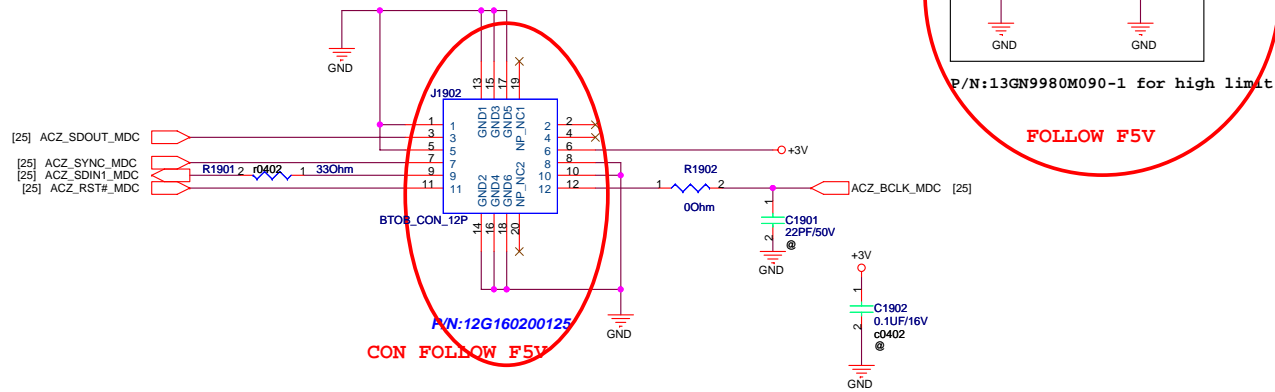
LCD LVDS/Inverter/CCD conn.



Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch \leq 10 mils
Twisted Pair(Not Ribbon)
Maximum Length \leq 16"

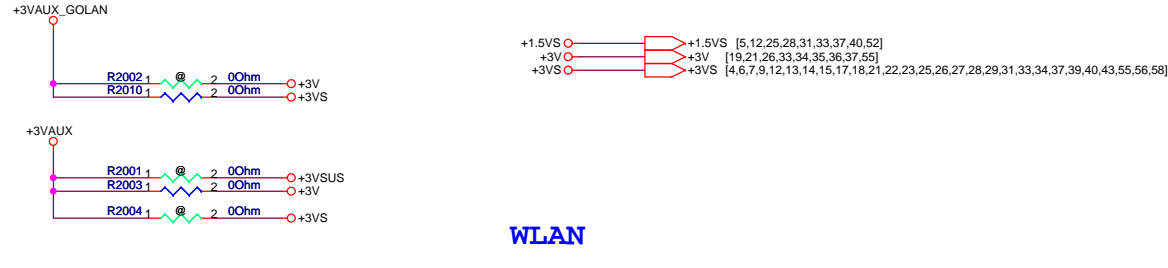
<Variant Name>

MDC CON.

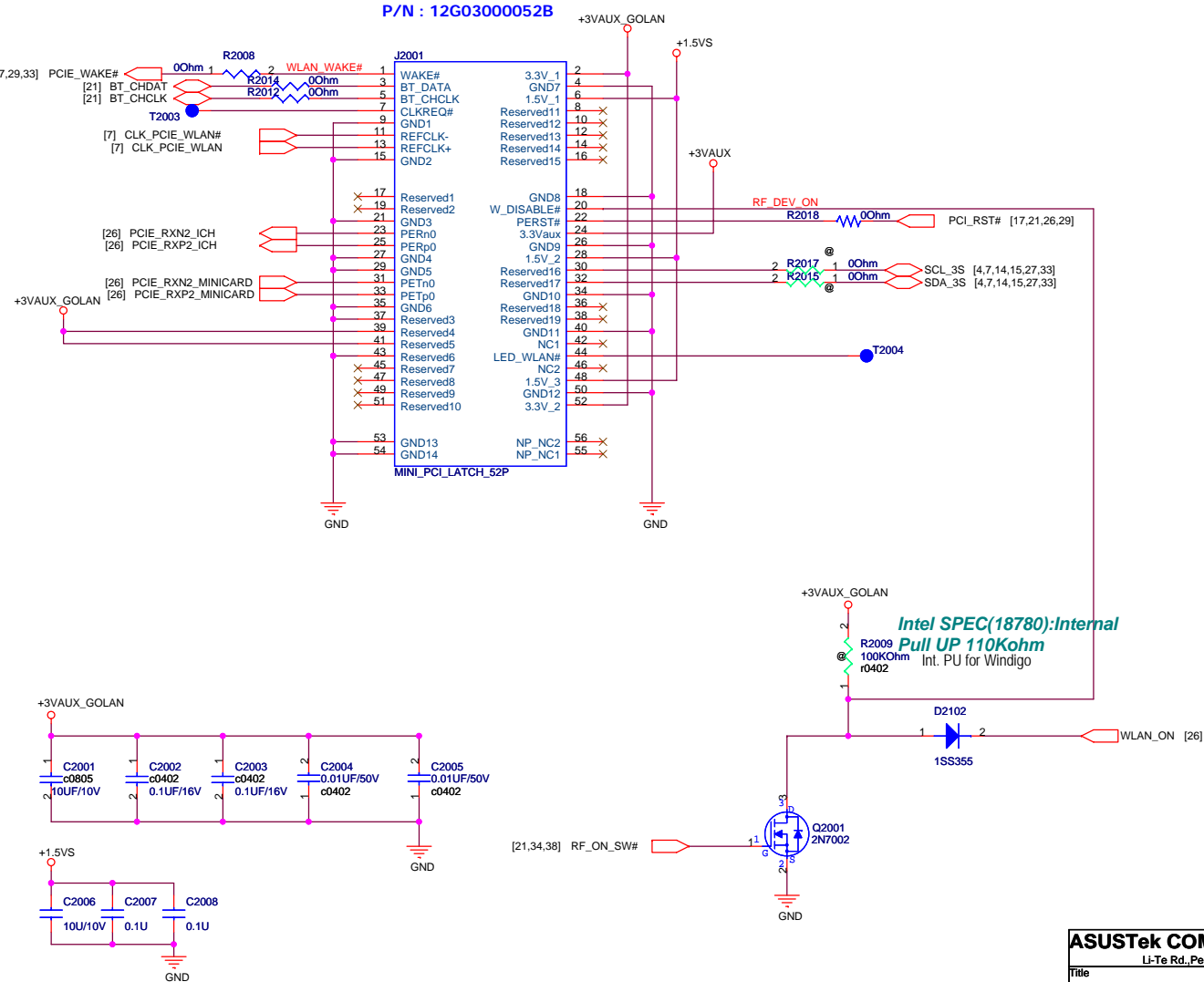
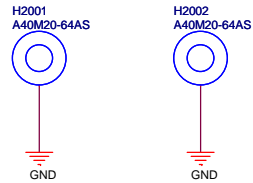


http://laptopblue.vn

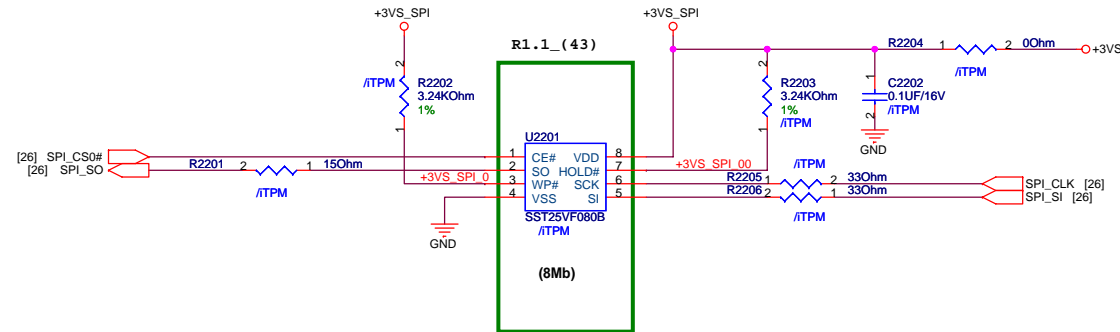
Reserved R to +3VSUS for
Wake on WLAN function!



+3VAUX_GOLAN: +3.003V~+3.597V
Max= 1100 mA
+1.5VS: +1.425V~+1.575V
Max= 375 mA

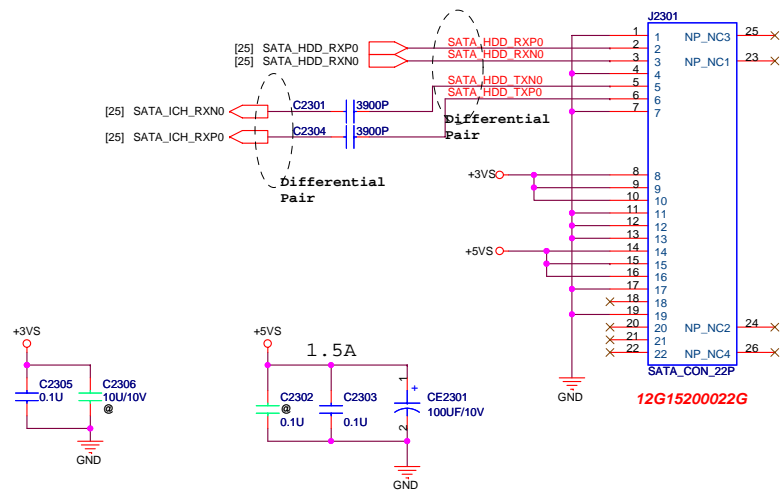


If don't support iTPM, unstuff these



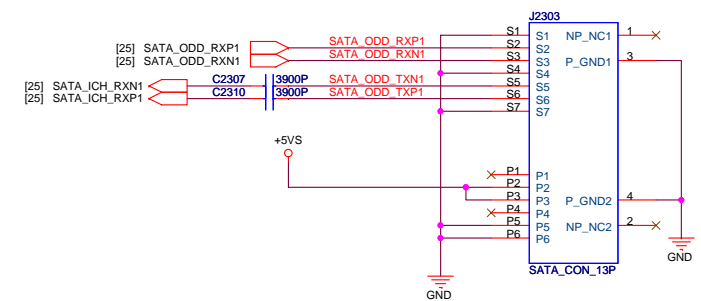
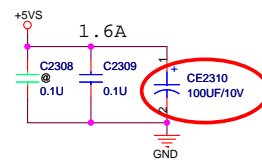
<Variant Name>

SATA HDD CON



SATA CD-ROM CON

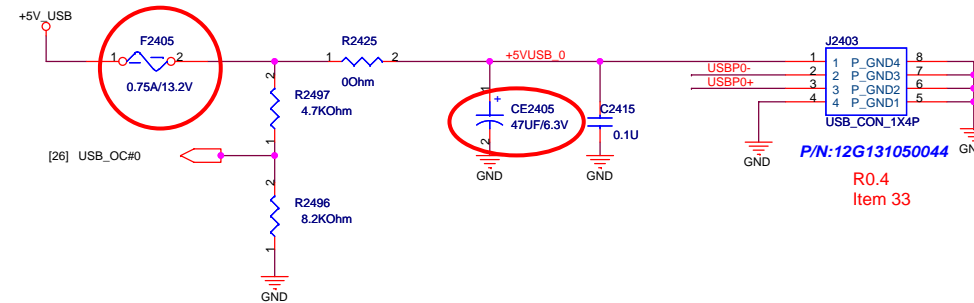
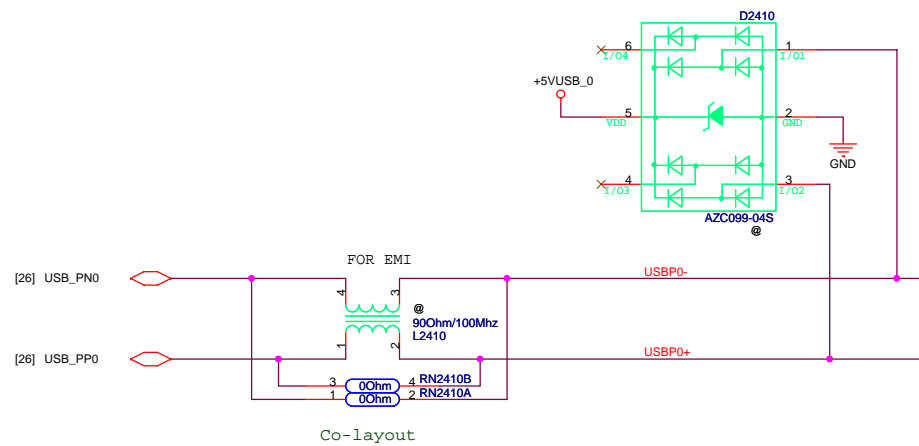
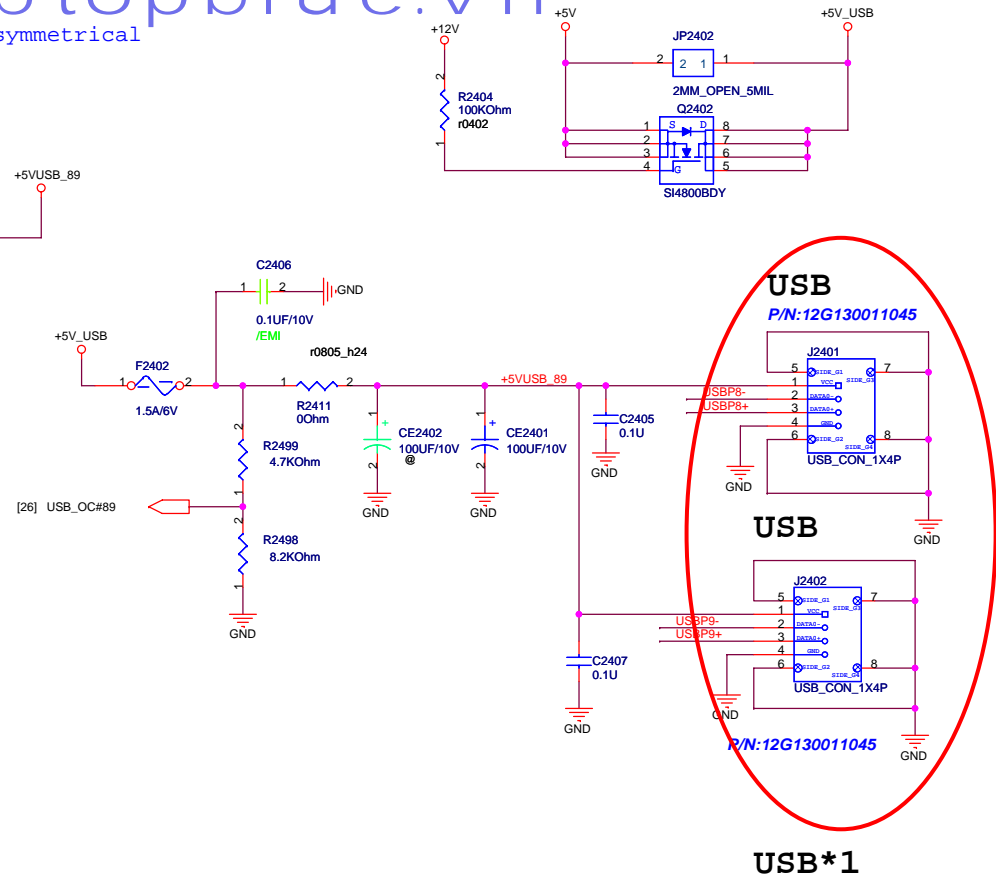
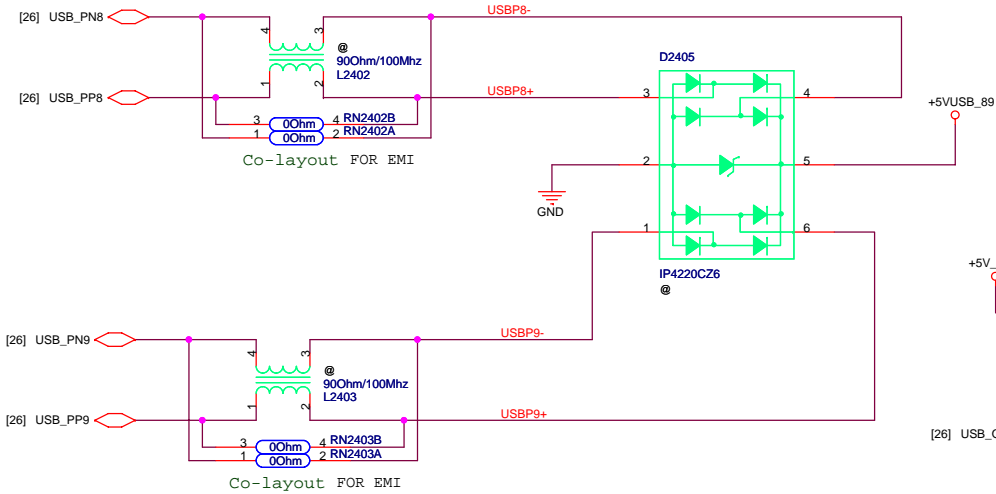
P/N:12G15100013J



PATA ODD:
Mount R2301,R2303,R2304,R2310,R2308,R2306

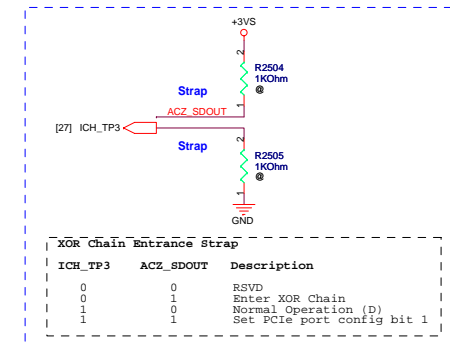
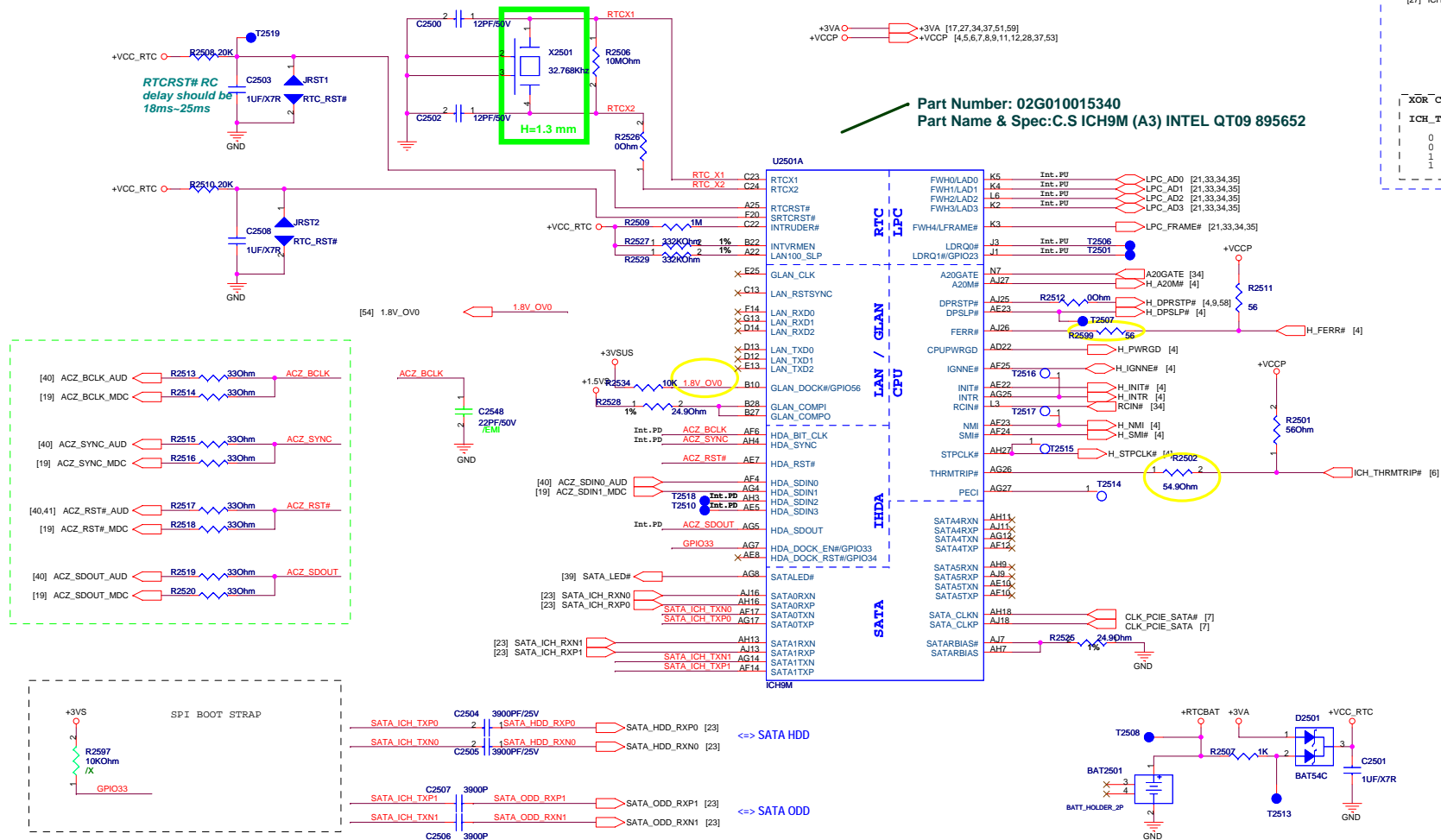
http://laptopblue.vn

Use IP4220CZ6 for layout symmetrical



<Variant Name>

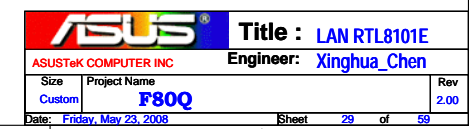
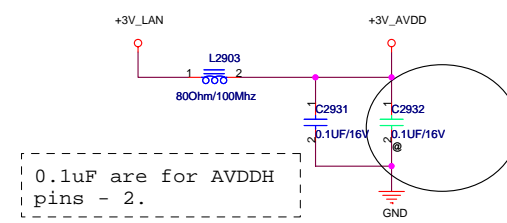
ASUS		Title : USB PORTS	
ASUSTeK COMPUTER INC		Engineer: Xinghua_chen	
Size	Project Name		Rev
Custom	F80Q		2.00
Date: Friday, May 23, 2008		Sheet 24	of 59

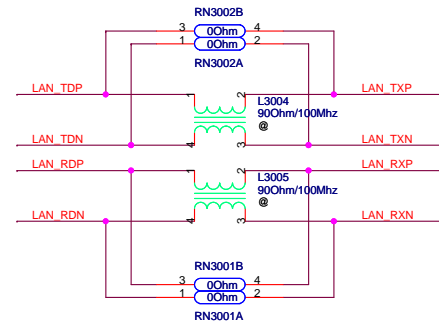
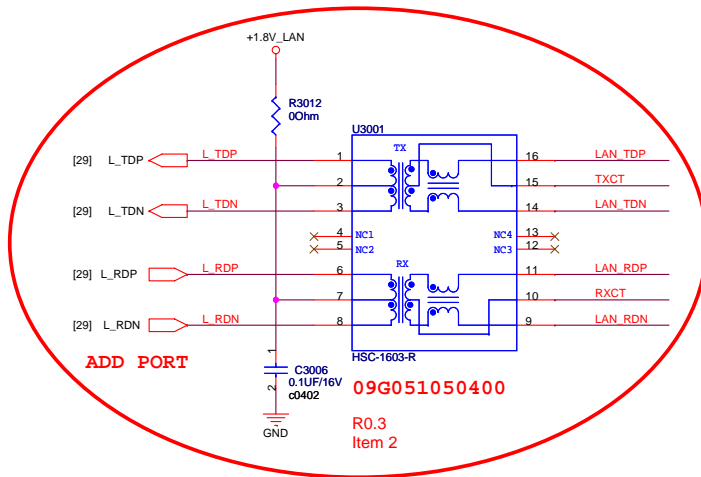


+VCCP

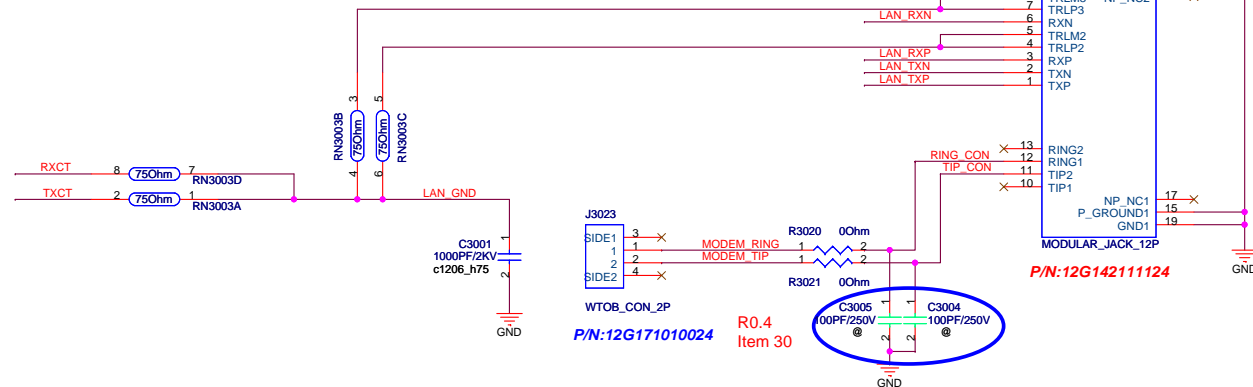
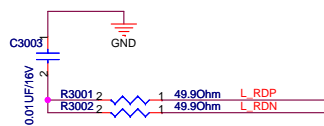
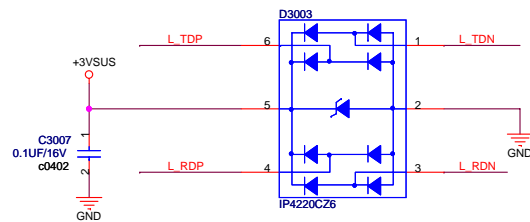


http://laptopblue.vn



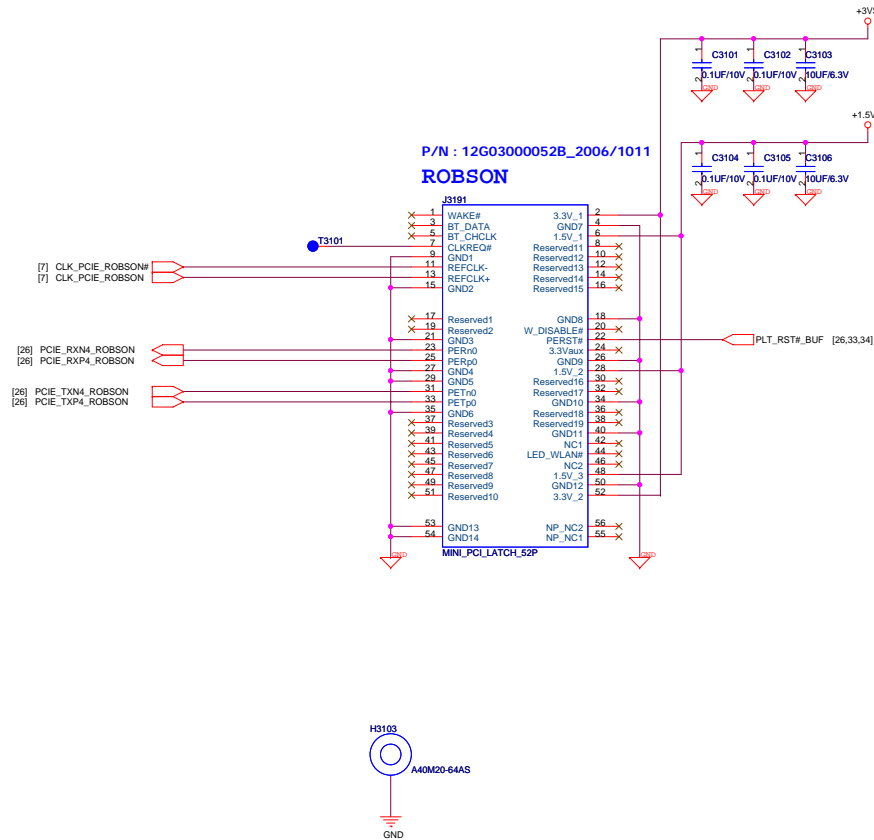


For RJ-45/RJ-11



<Variant Name>

ROBSON
only

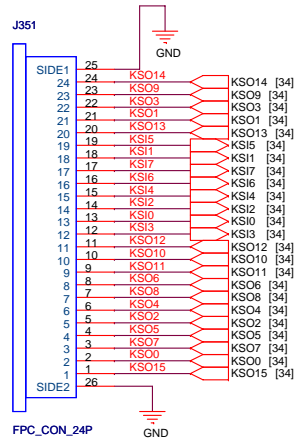


<http://laptopblue.vn>

Size	Document Number	Rev
A	F80L	2.00

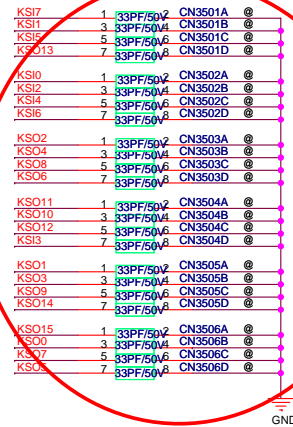
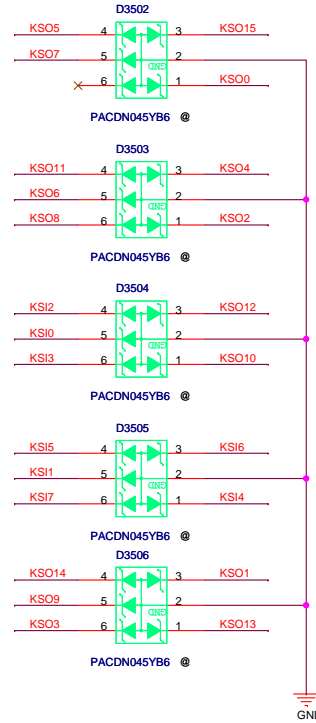
Date: Friday, May 23, 2008 Sheet 32 of 59

For Keyboard

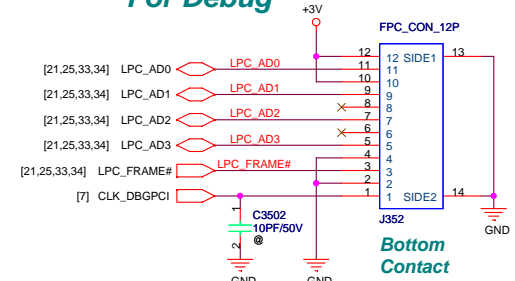


P/N:12G182002408

T53 KB MATRIX



For Debug



<Variant Name>



Stablize +3V_CR, if
+3_CARAD consume large
in-rush current.



Title :

ASUSTeK COMPUTER INC

Size	Project Name
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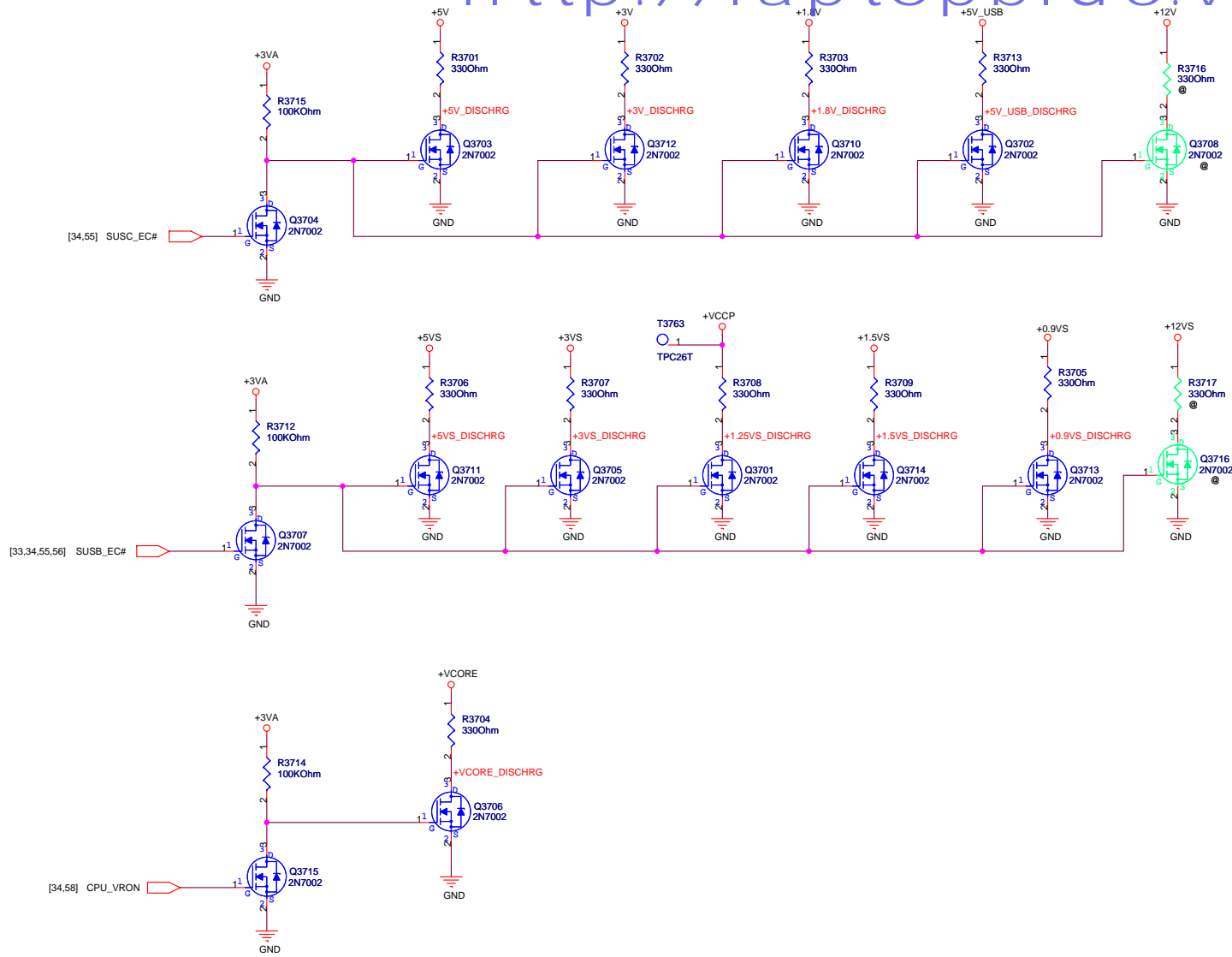
Size	Project Name
Custom	F80L

Engineer:

Date: Friday, May 23, 2008

Sheet

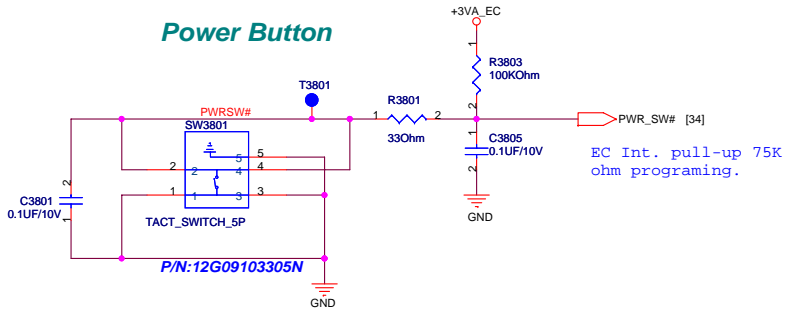
2.00



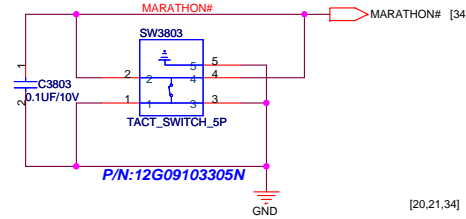
<Variant Name>

ASUS		Title : DISCHARGE	
ASUSTeK COMPUTER INC		Engineer: CH Lin	
Size	Project Name	Rev	
Custom	F80L	2.00	
Date: Friday, May 23, 2008		Sheet	37 of 59

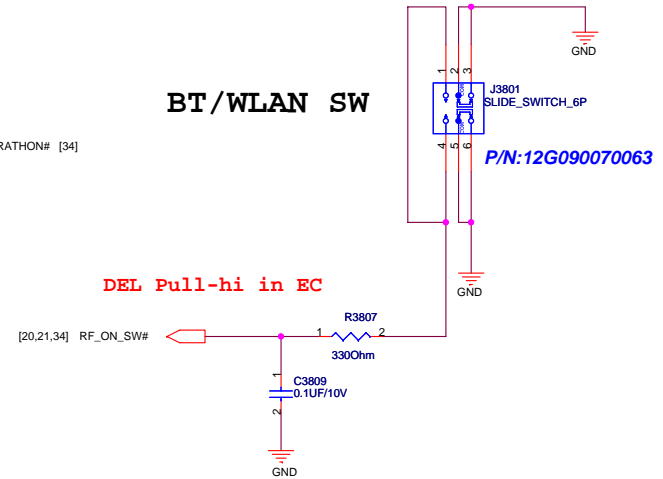
Power Button



MARATHON#

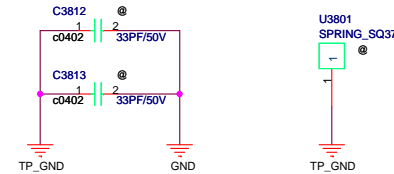
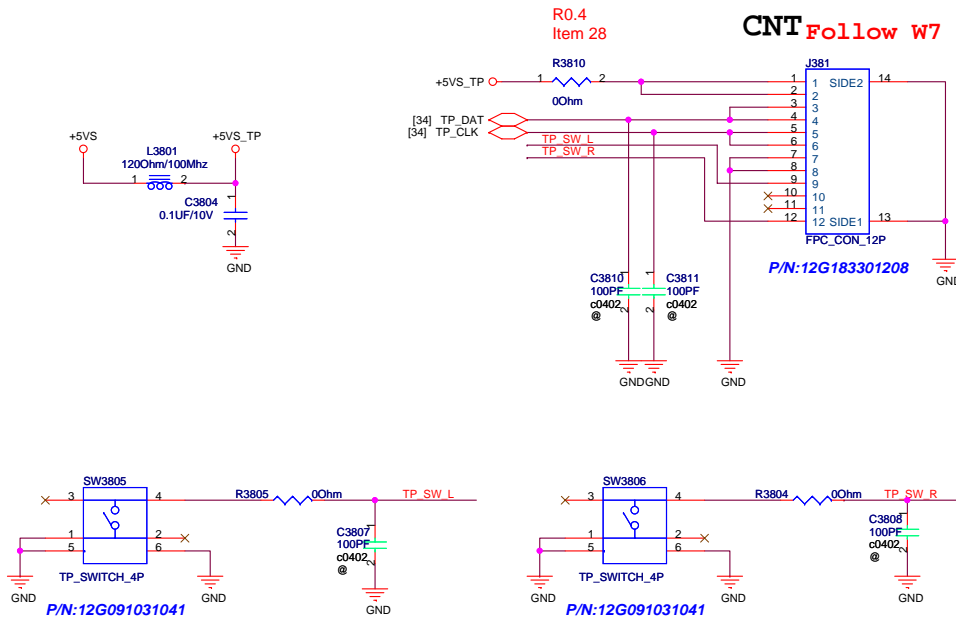


BT/WLAN SW



Touch-Pad

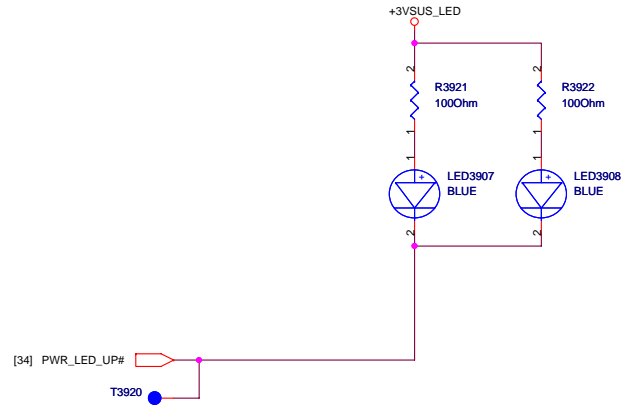
TOUCH PAD CNT Follow W7



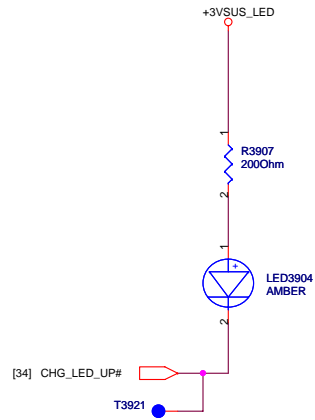
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ASUSTeK COMPUTER INC		Engineer: Xighua_chen	
Size	Project Name	Rev	
Custom	F80Q	2.00	
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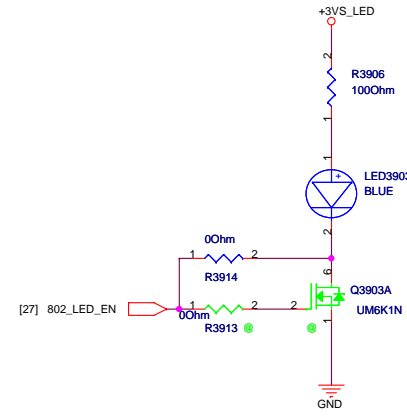
PWR LED



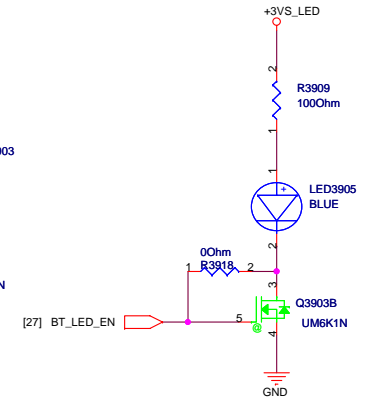
For BATTERY LED



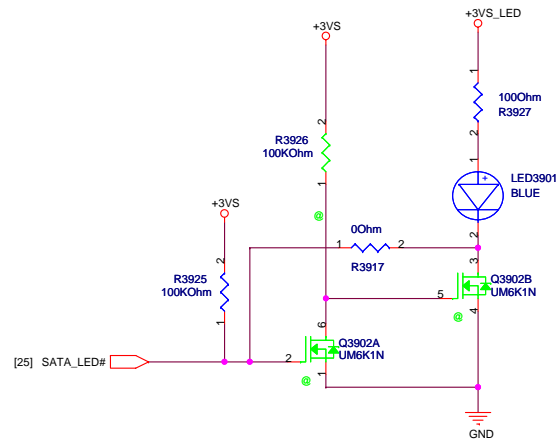
WireLess LED



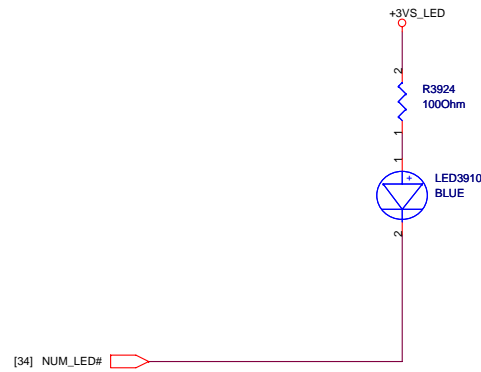
BT LED



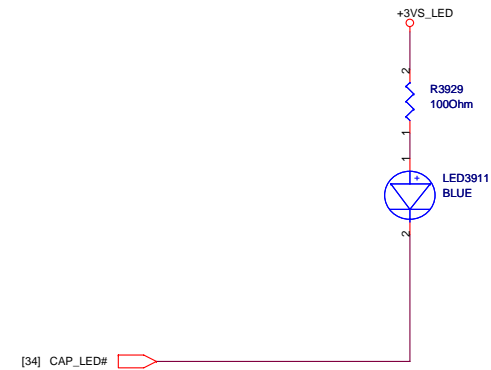
SATA/IDE LED



Num Lock

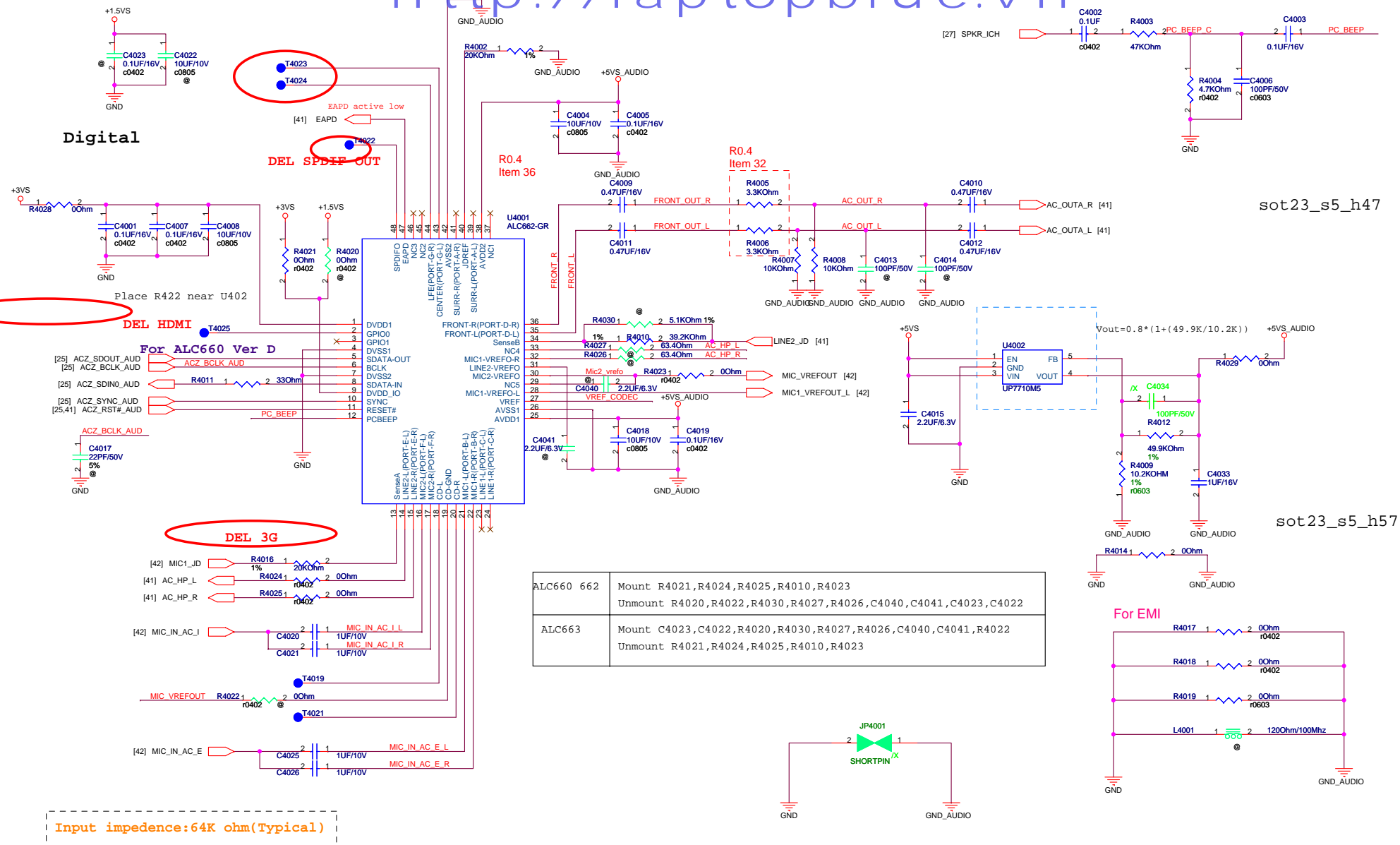


Cap. Lock

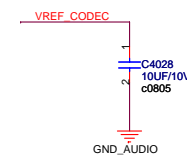
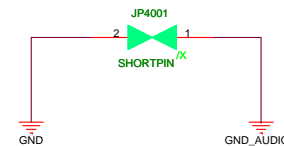


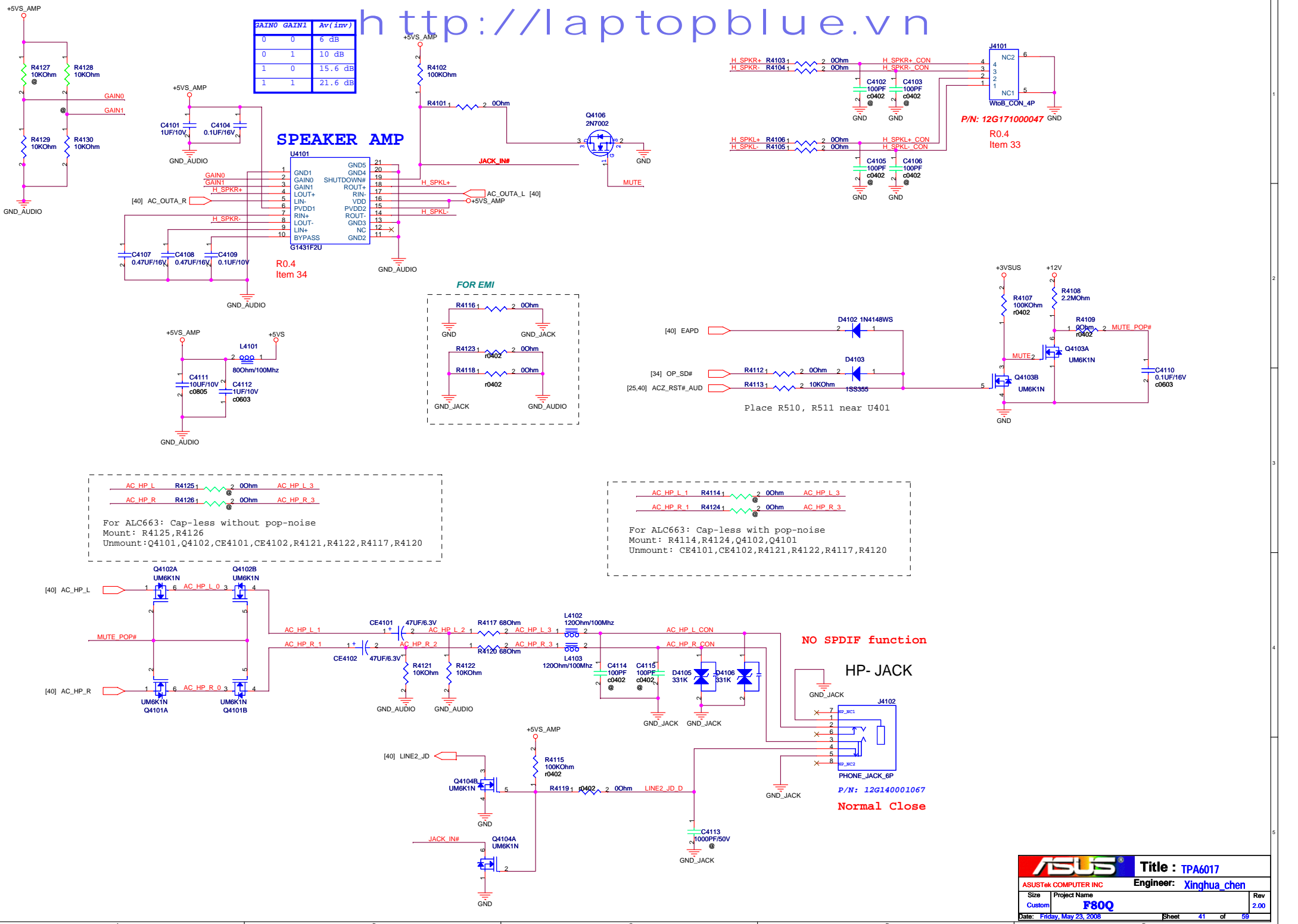
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ASUS		Title : LEDs	
ASUSTeK COMPUTER INC		Engineer: Xinghua_Chen	
Size	Project Name	Rev	
Custom	F80Q	2.00	
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ALC660 662	Mount R4021,R4024,R4025,R4010,R4023 Unmount R4020,R4022,R4030,R4027,R4026,C4040,C4041,C4023,C4022
ALC663	Mount C4023,C4022,R4020,R4030,R4027,R4026,C4040,C4041,R4022 Unmount R4021,R4024,R4025,R4010,R4023





GAIN0	GAIN1	Av(Inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

SPEAKER AMP

R0.4
Item 34

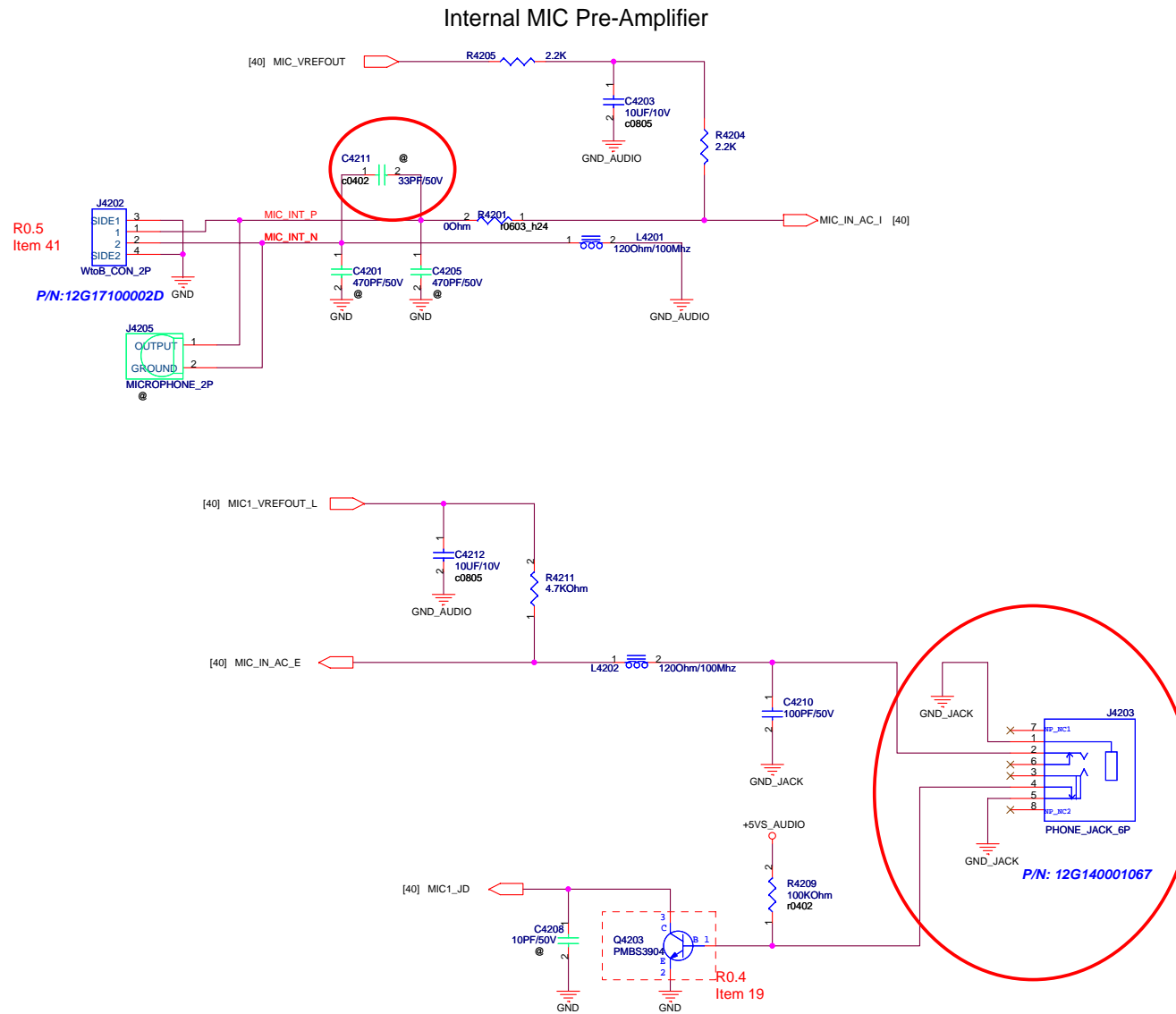
FOR EMI

NO SPDIF function

HP- JACK

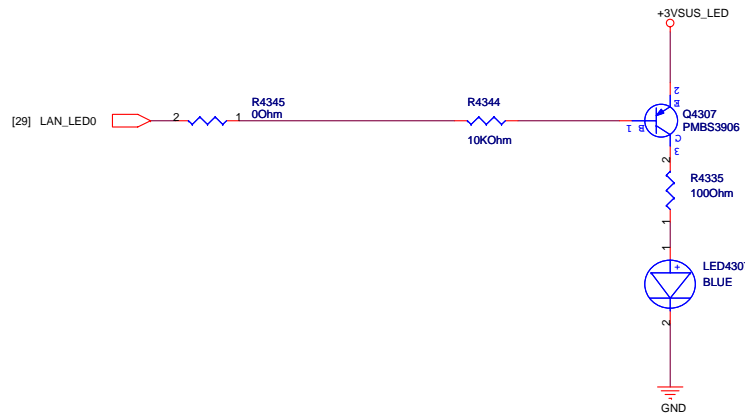
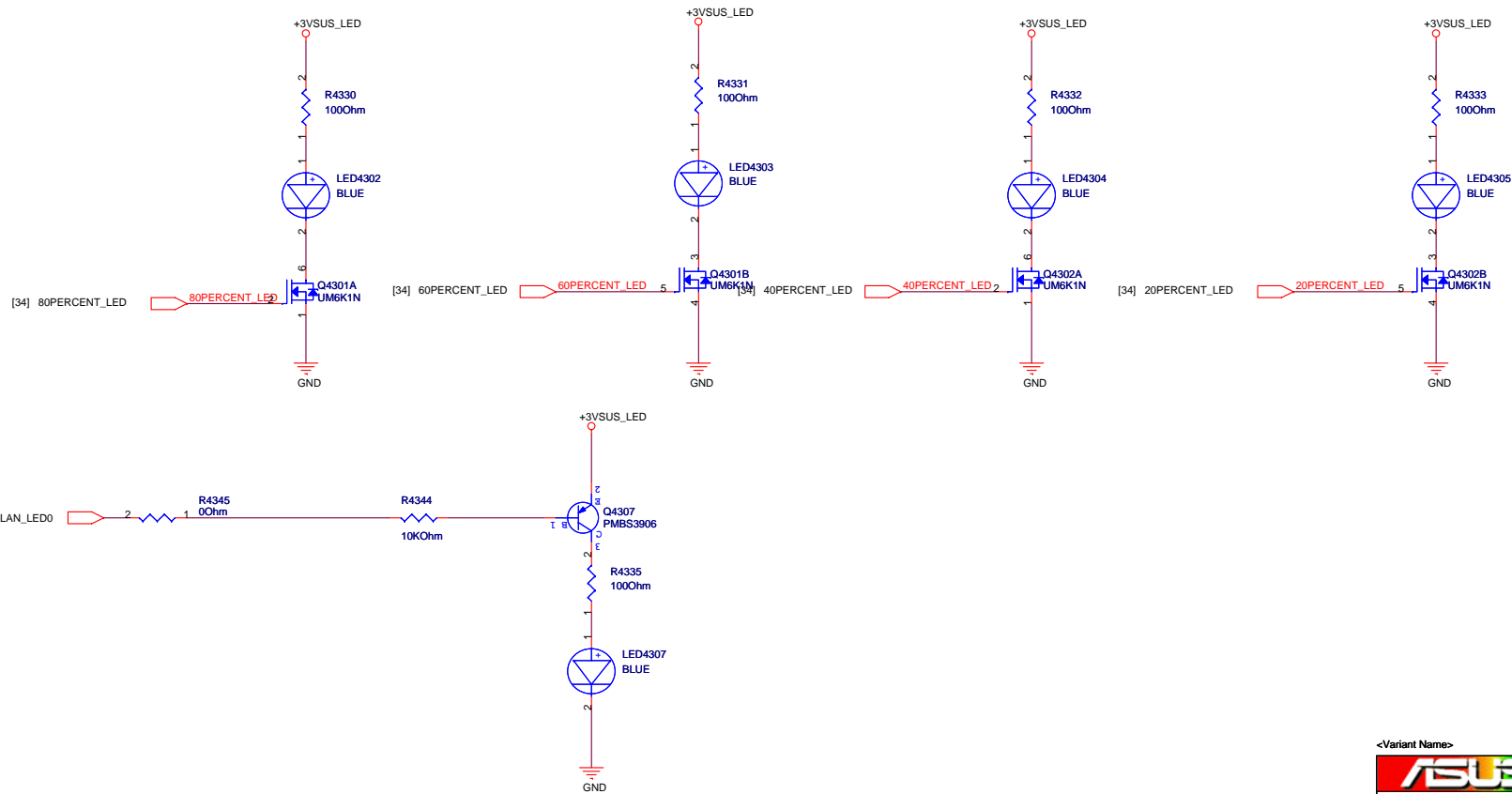
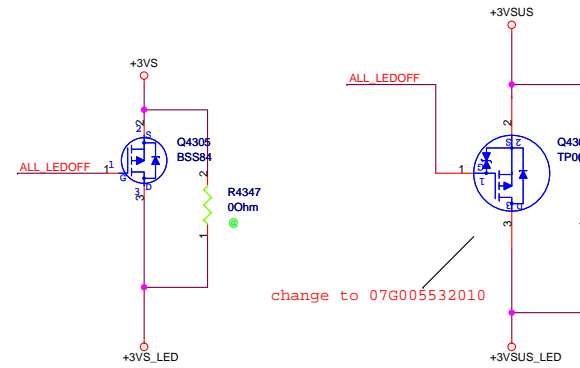
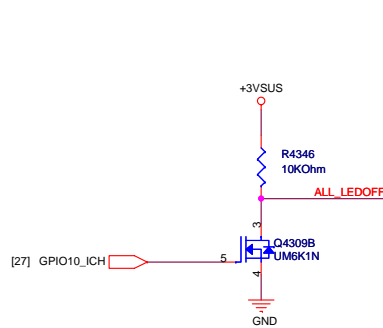
P/N: 12G140001067

Normal Close



<Variant Name>

ASUS		Title : MICROPHONE	
ASUSTeK COMPUTER INC		Engineer: Xinghua_Chen	
Size	Project Name	Rev	
Custom	F80Q	2.00	
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add LED1,LED2,LED3 test points

<Variant Name>

ASUS		Title : BATTERY&LAN LED	
ASUS&K COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	F80Q	2.00	
Date: Friday, May 23, 2008	Sheet	43	of 59

h t t p : / / l a p t o p b l u e . v n

<Variant Name>



Title : empty

ASUSTeK COMPUTER INC

Engineer: Xinghua_chen

Size

Custom

Project Name

F80Q

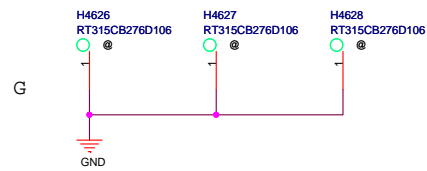
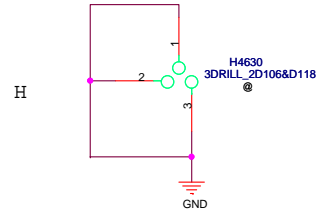
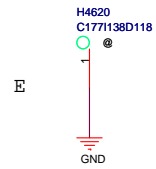
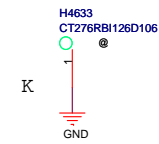
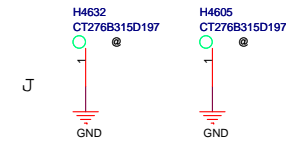
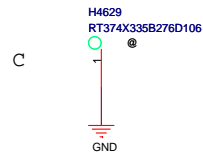
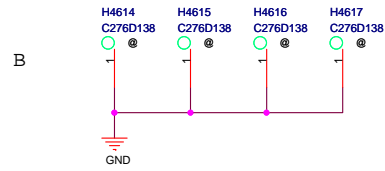
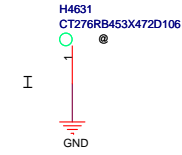
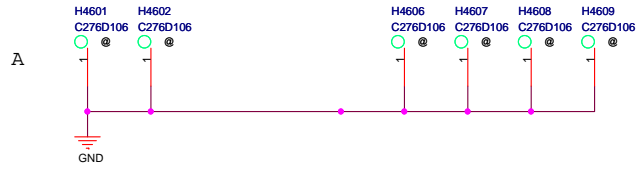
Rev

2.00


Date: Friday, May 23, 2008

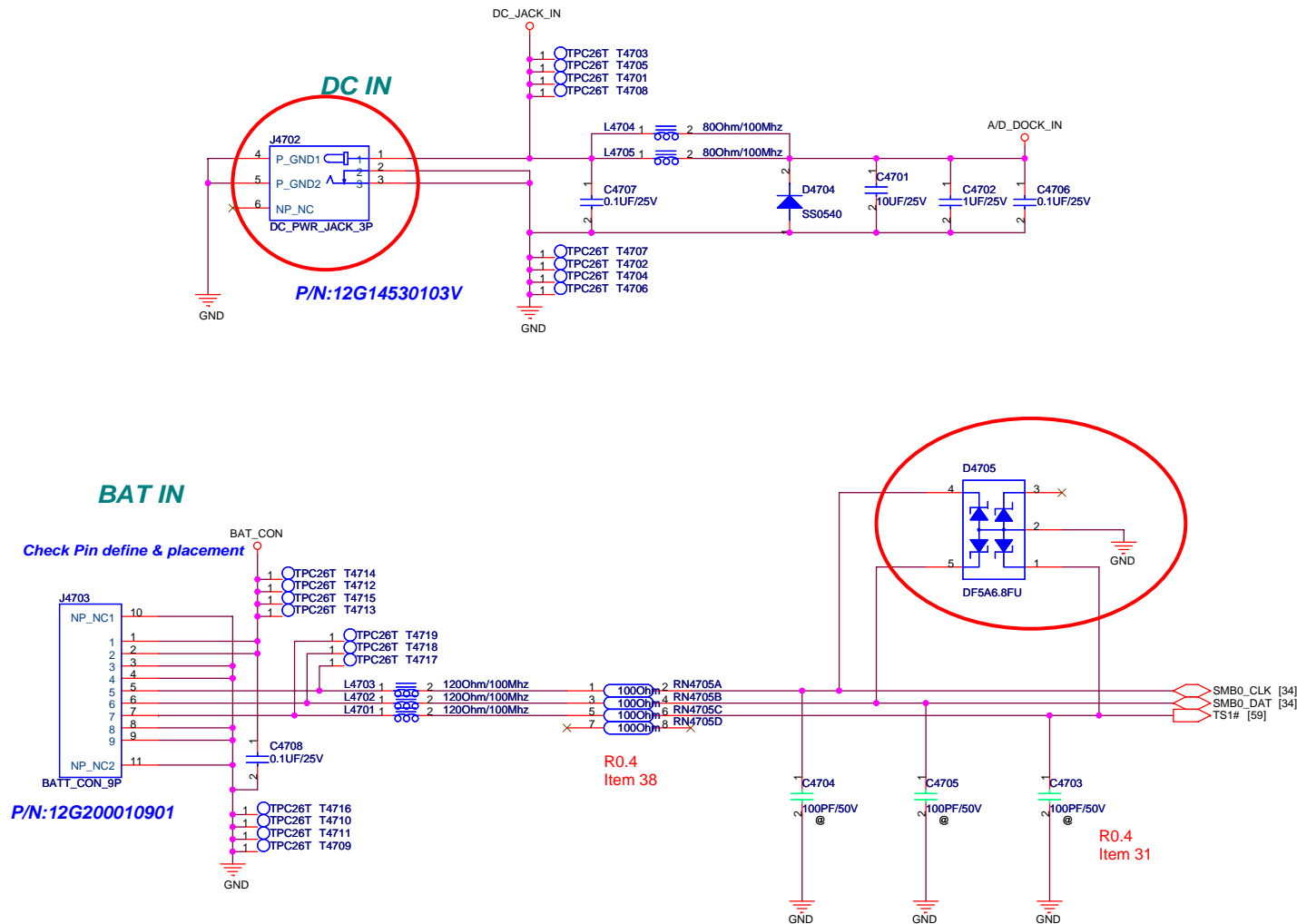
Sheet 44 of 59

h t t p : / / l a p t o p b l u e . v n

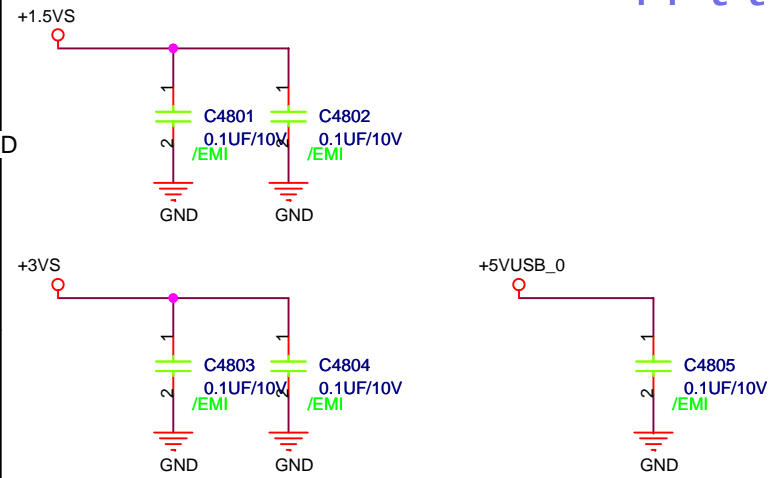


<Variant Name>

		Title : SCREW HOLE	
ASUSTeK COMPUTER INC		Engineer: CHLin	
Size Custom	Project Name F80L		Rev 2.00
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h t t p : / / l a p t o p b l u e . v n

<Variant Name>



ASUSTeK COMPUTER INC

Title : History(2)

Size

Custom

Project Name

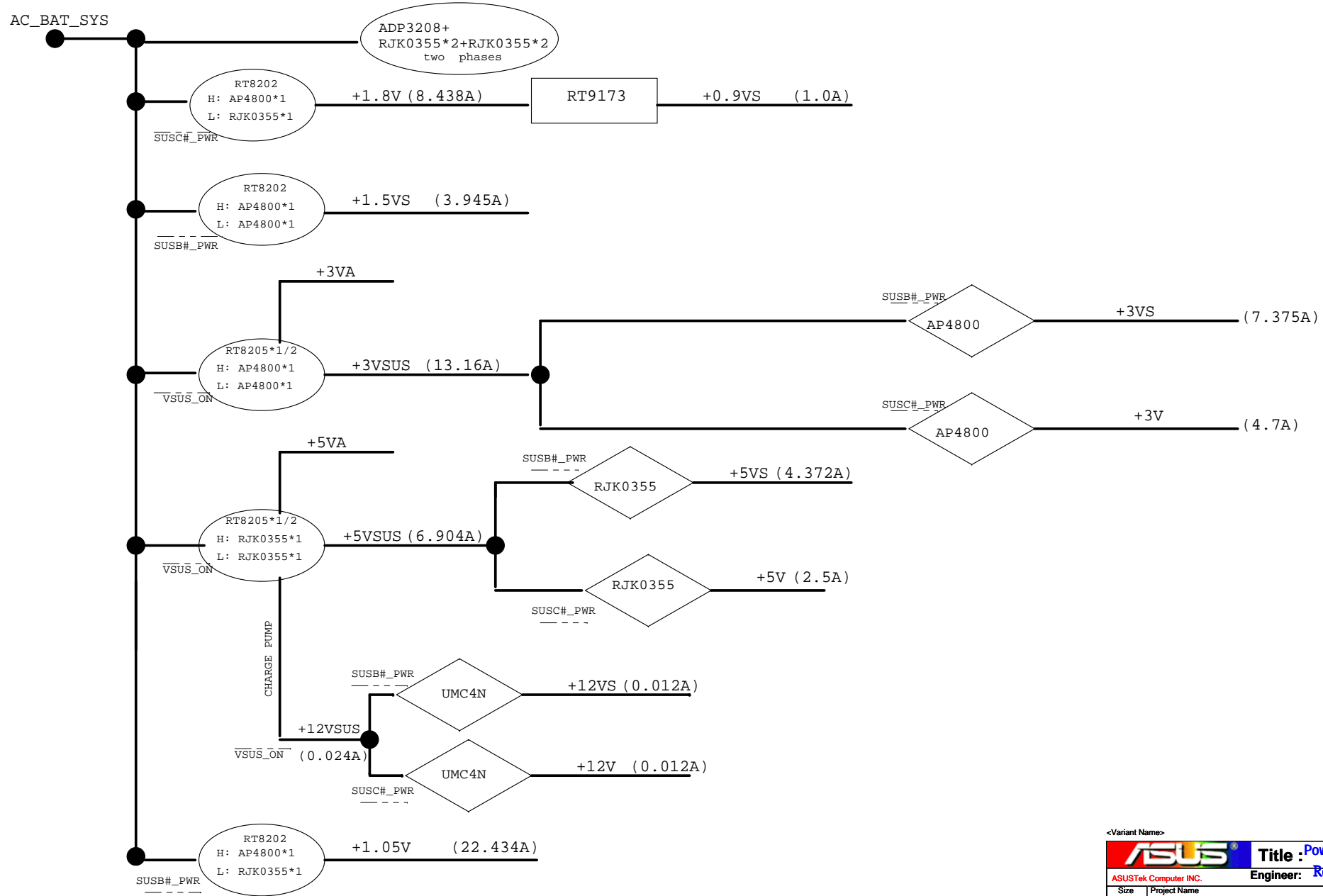
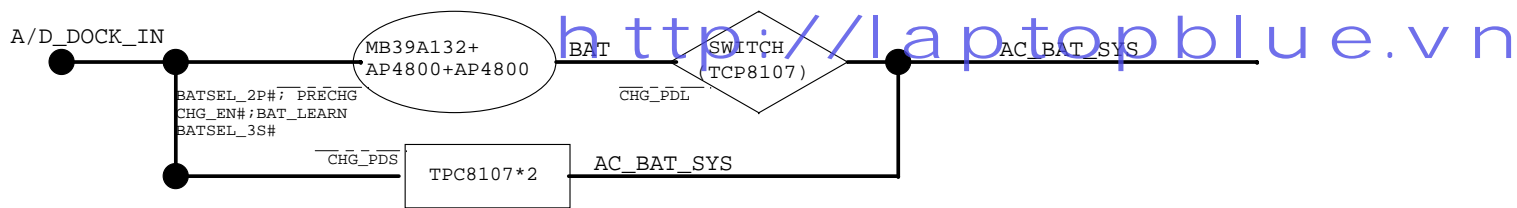
F80L

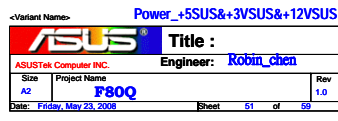
Rev

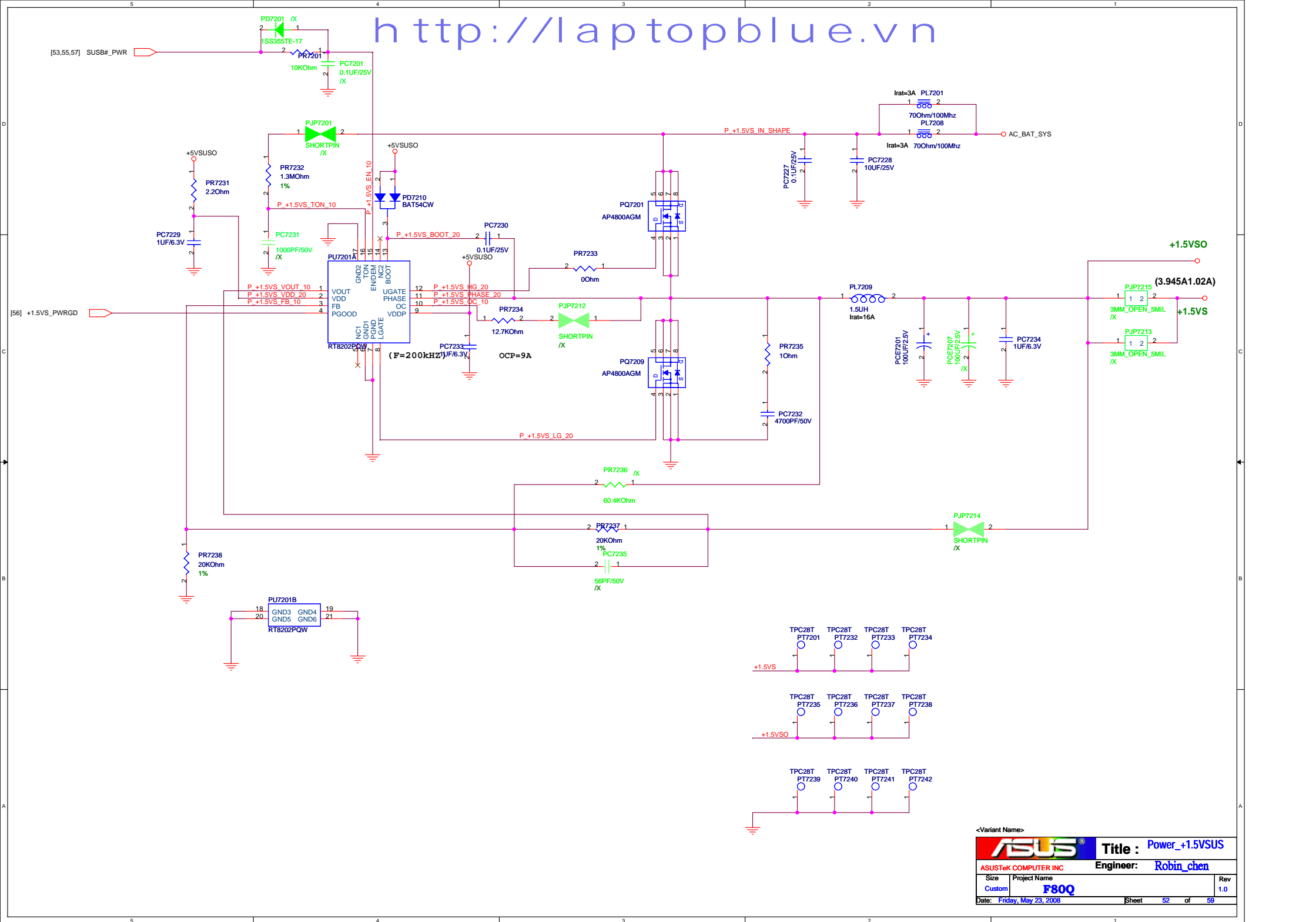
2.00

Date: Friday, May 23, 2008

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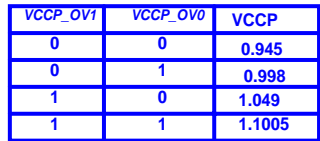




<Variant Name>

ASUS		Title : Power_+1.5VSUS	
ASUSTeK COMPUTER INC		Engineer: Robin_chen	
Size	Project Name	Rev	
Custom	F80Q	1.0	
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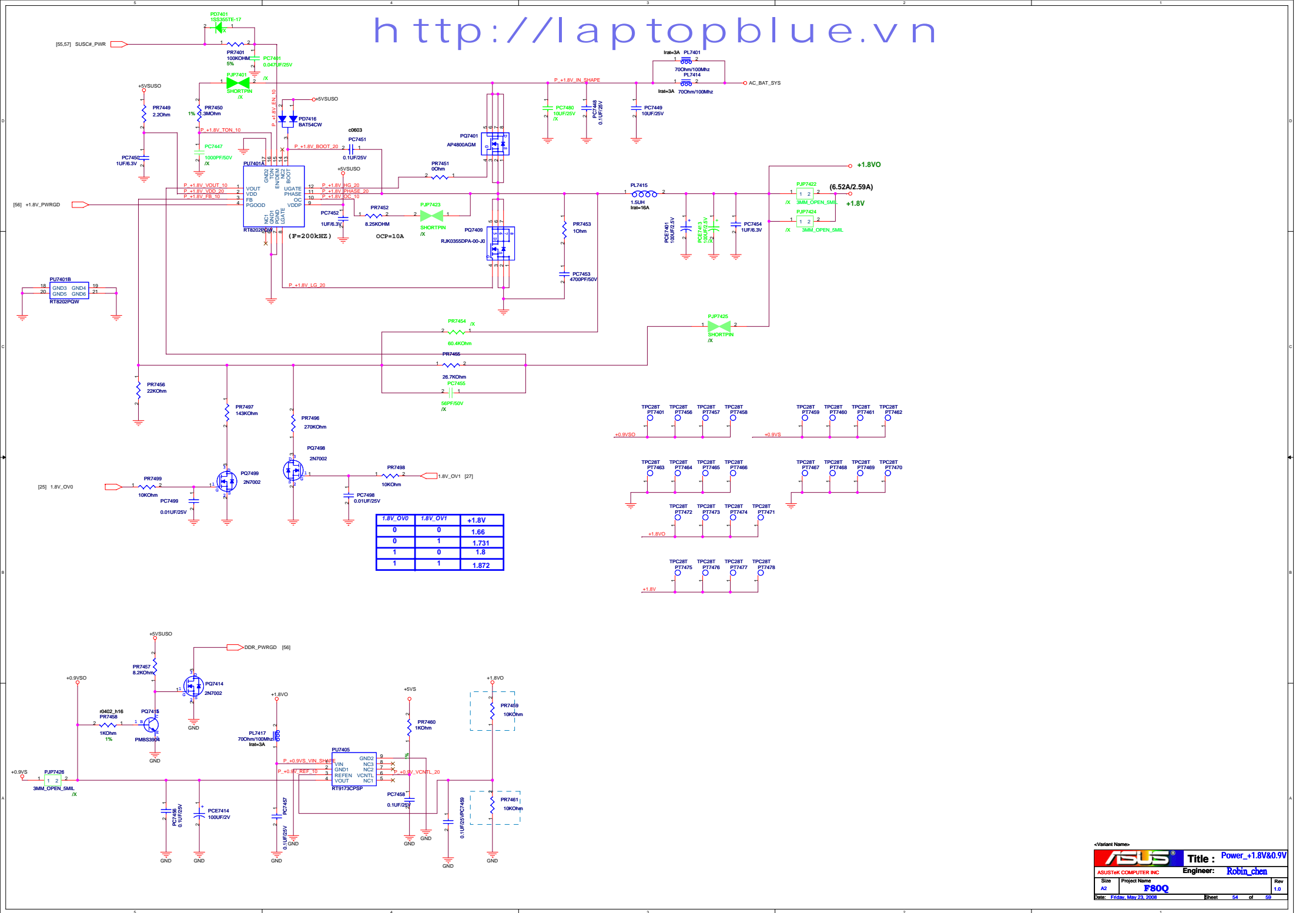
[52,55,57] SUSB#_PWR



The schematic diagram illustrates the electrical connections for the TPC28T array. It is organized into three horizontal rows of components, each connected to a common vertical bus on the left.

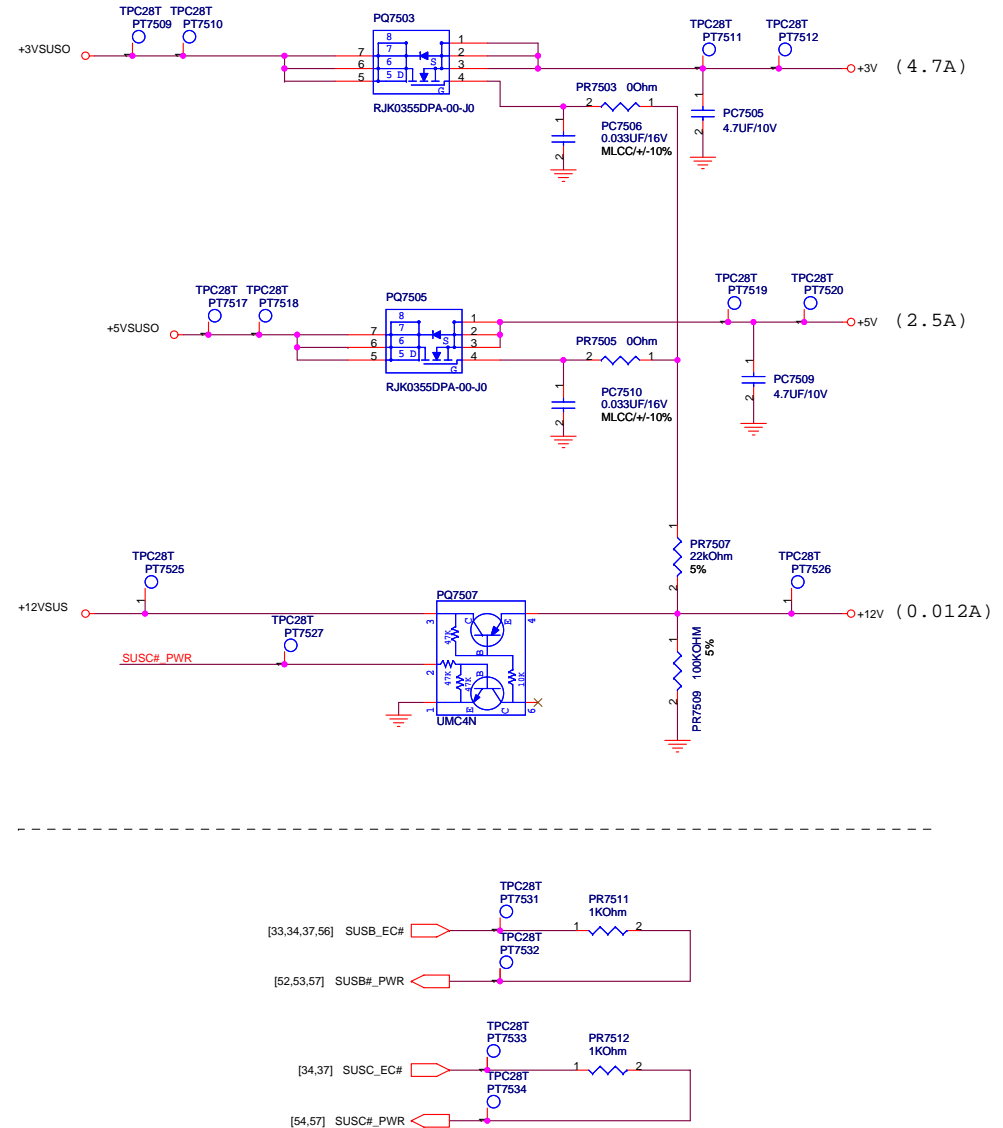
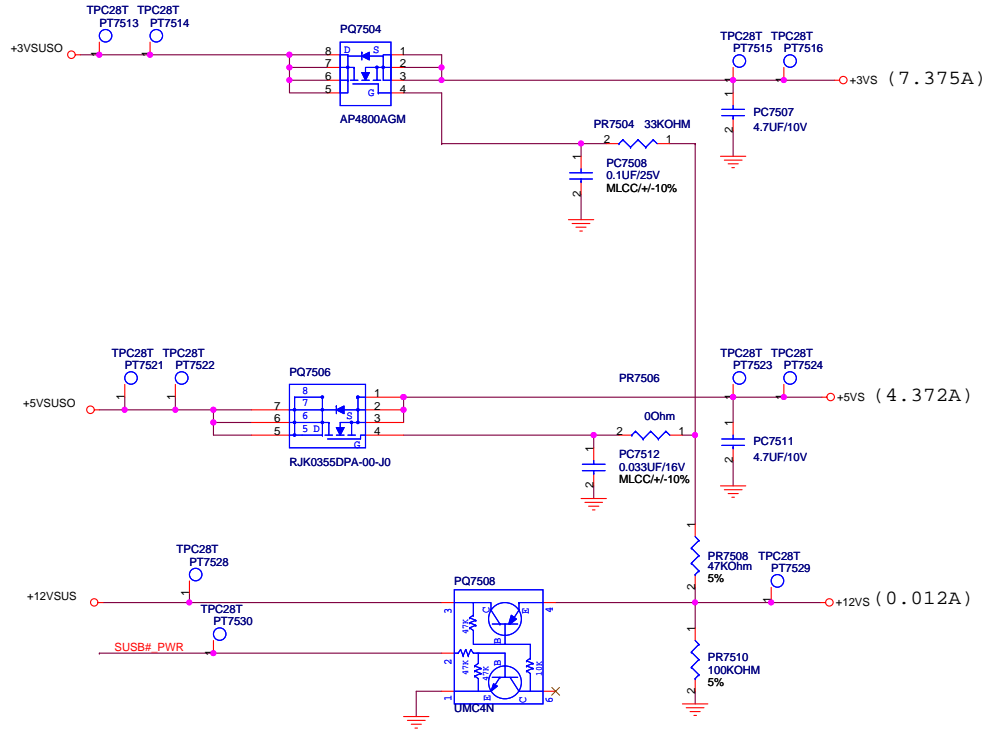
- Top Row:** Four TPC28T components (PT7301, PT7344, PT7345, PT7346) are connected to the **+VCCP** supply line.
- Middle Row:** Four TPC28T components (PT7347, PT7348, PT7349, PT7350) are connected to the **+1.05V0** supply line.
- Bottom Row:** Four TPC28T components (PT7351, PT7352, PT7353, PT7354) are connected to the **ground** line.

Each component is represented by a circle with a vertical line through its center, indicating a connection point. The labels for each component are placed above or below the circle.



SUSB#_PWR POWER

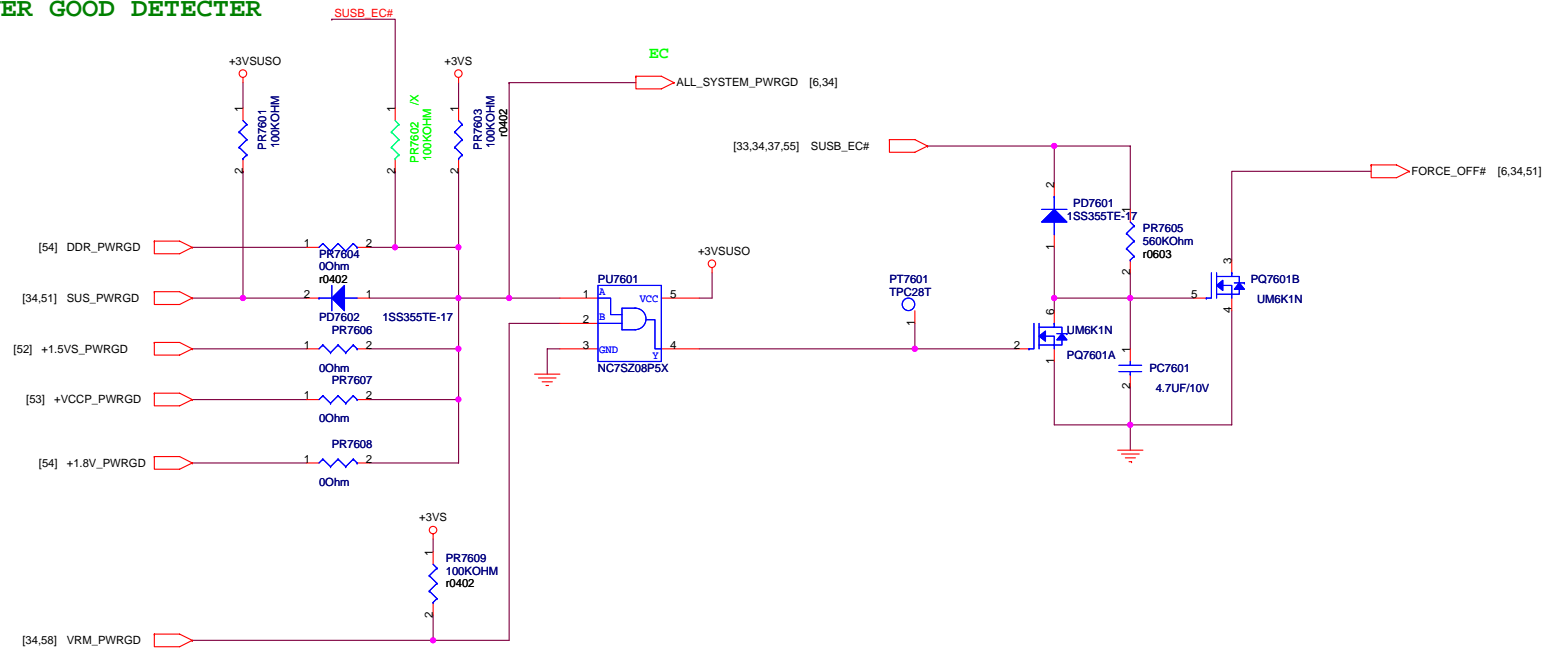
SUSC#_PWR POWER



<Variant Name>

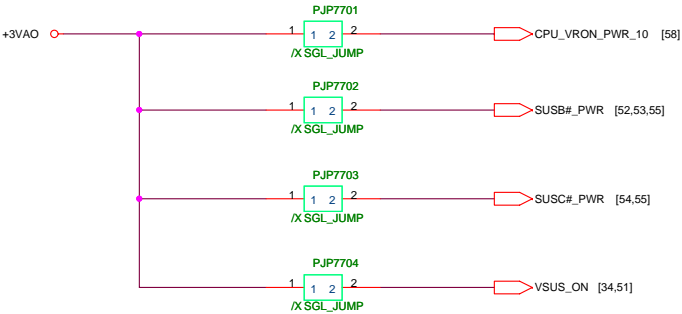
ASUS		Title :Power_Load_Switch	
ASUSTeK COMPUTER INC		Engineer: Robin_chen	
Size	Project Name	Rev	
Custom	F80Q	1.0	
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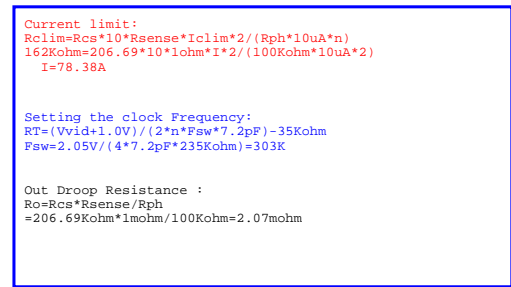
POWER GOOD DETECTER

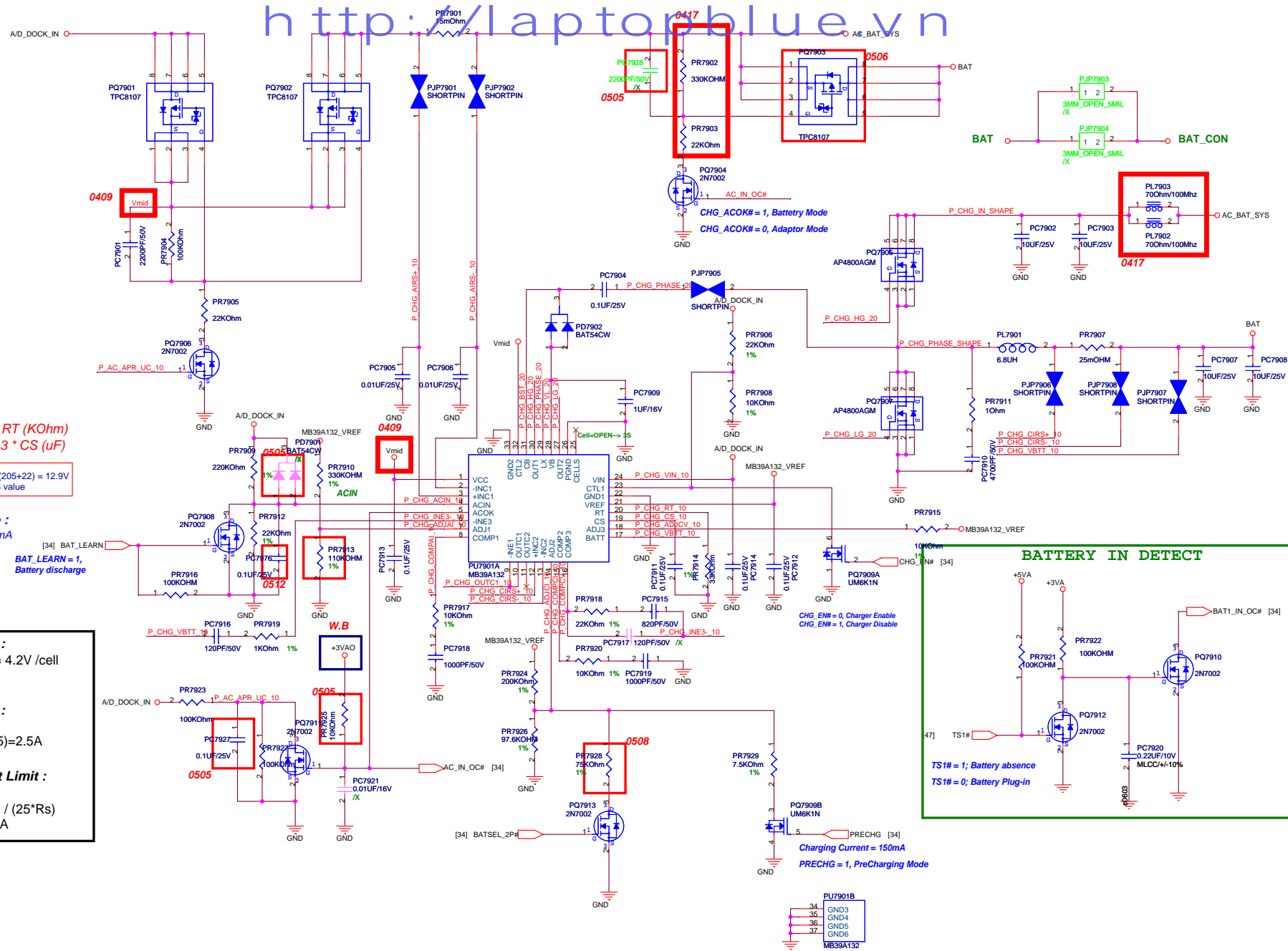


<Variant Name>

		Title: Power_good_detector	
ASUSTeK COMPUTER INC		Engineer: Robin_chen	
Size	Project Name	Rev	
Custom	F80Q	1.0	
Date: Friday, May 23, 2008		Sheet	56 of 59







VREF = 5.0V
 $f_{osc}(KHz) = 17000 / RT (KOhm)$
 Soft start: $t_s(s) = 0.13 * CS (\mu F)$

VTH of ACIN: $1.25V / 22 * (205+22) = 12.9V$
 Change PR607 and PR608 value

Pre-Charging Mode :
 Precharging current = 150mA
 $V_{adj2} = 168.75mV$

BAT_LEARN = 1,
 Battery discharge

Battery Charging Voltage :

$V_{adj3} = V_{ref} \Rightarrow V_{bat} = 4.2V / cell$
 CELLS->open \Rightarrow 3 cells
 $V_{BAT} = 3 * 4.2V = 12.6V$

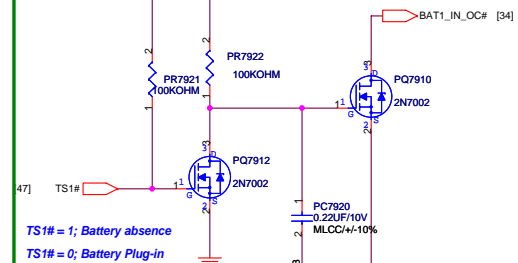
Battery Charging Current :

$I_{chg} = (V_{adj2} - 0.075) / (25 * R_s)$
 $= (1.6375 - 0.075) / (25 * 0.025) = 2.5A$

Input Adaptor Max. Current Limit :

$I_{limit_current} = (V_{adj1} - 0.075) / (25 * R_s)$
 $= (1.25 - 0.075) / (25 * 0.015) = 3.13A$

BATTERY IN DETECT



TS1# = 1; Battery absence
 TS1# = 0; Battery Plug-in

Charging Current = 150mA
 PRECHG = 1, PreCharging Mode

<Variant Name>