

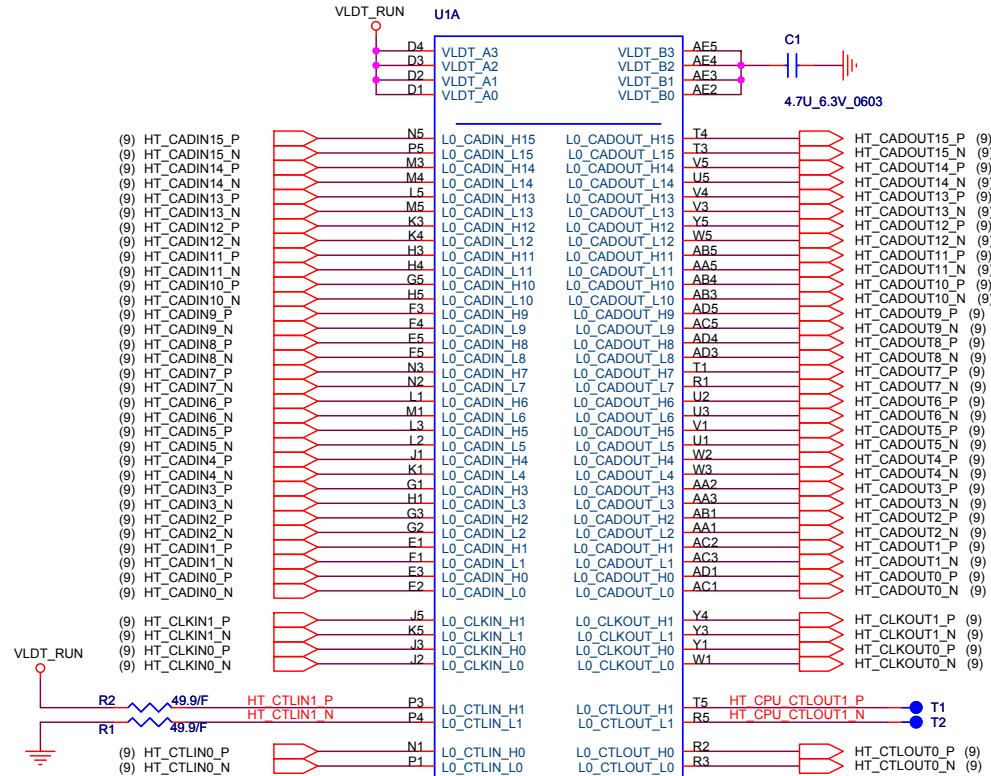
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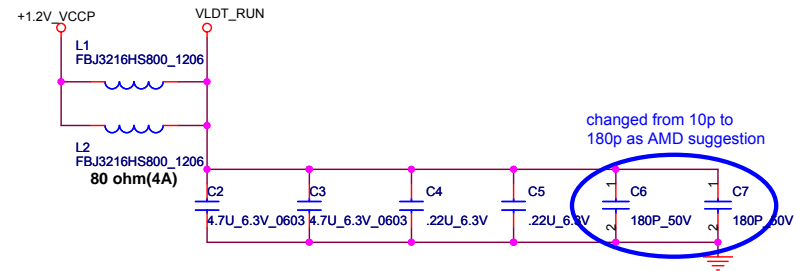


PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Athlon 64 S1
Processor Socket



LAYOUT: Place bypass cap on topside of board



NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS



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Title		
ATHLON64 HT I/F		
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VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

The diagram illustrates the pin connections for the Athlon 64 S1 Processor Socket, which is a 940-pin ZIF package. It shows two SODIMM sockets, A (near) and B (far), with their respective pin assignments and connections to the processor pins.

Socket A (near) Connections:

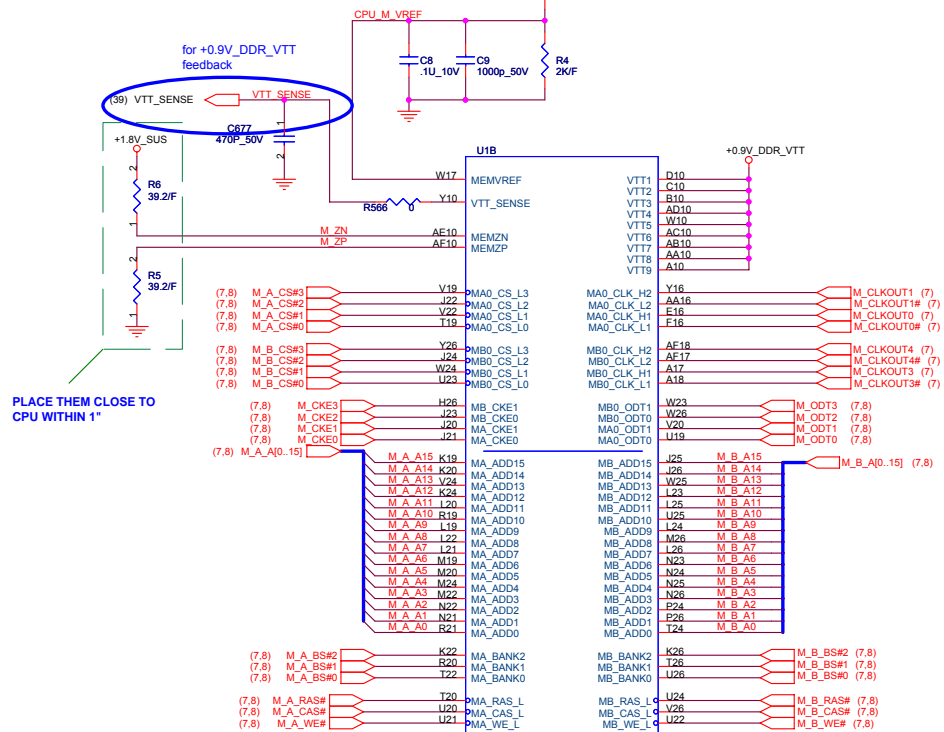
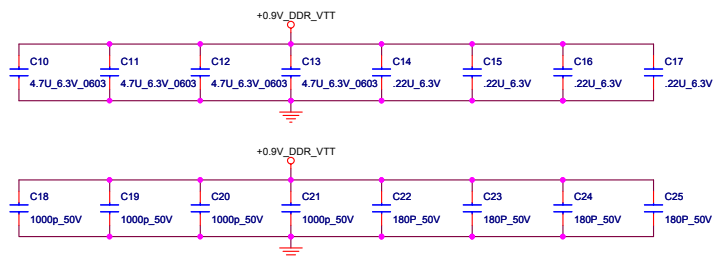
- MA_DQS[0..7] (near):** MA_DQS_0, MA_DQS_1, MA_DQS_2, MA_DQS_3, MA_DQS_4, MA_DQS_5, MA_DQS_6, MA_DQS_7
- M_A_DQ[0..63] (near):** M_A_DQ_0, M_A_DQ_1, M_A_DQ_2, M_A_DQ_3, M_A_DQ_4, M_A_DQ_5, M_A_DQ_6, M_A_DQ_7, M_A_DQ_8, M_A_DQ_9, M_A_DQ_10, M_A_DQ_11, M_A_DQ_12, M_A_DQ_13, M_A_DQ_14, M_A_DQ_15, M_A_DQ_16, M_A_DQ_17, M_A_DQ_18, M_A_DQ_19, M_A_DQ_20, M_A_DQ_21, M_A_DQ_22, M_A_DQ_23, M_A_DQ_24, M_A_DQ_25, M_A_DQ_26, M_A_DQ_27, M_A_DQ_28, M_A_DQ_29, M_A_DQ_30, M_A_DQ_31, M_A_DQ_32, M_A_DQ_33, M_A_DQ_34, M_A_DQ_35, M_A_DQ_36, M_A_DQ_37, M_A_DQ_38, M_A_DQ_39, M_A_DQ_40, M_A_DQ_41, M_A_DQ_42, M_A_DQ_43, M_A_DQ_44, M_A_DQ_45, M_A_DQ_46, M_A_DQ_47, M_A_DQ_48, M_A_DQ_49, M_A_DQ_50, M_A_DQ_51, M_A_DQ_52, M_A_DQ_53, M_A_DQ_54, M_A_DQ_55, M_A_DQ_56, M_A_DQ_57, M_A_DQ_58, M_A_DQ_59, M_A_DQ_60, M_A_DQ_61, M_A_DQ_62, M_A_DQ_63
- M_A_DQ[0..7] (near):** M_A_DQ_0, M_A_DQ_1, M_A_DQ_2, M_A_DQ_3, M_A_DQ_4, M_A_DQ_5, M_A_DQ_6, M_A_DQ_7

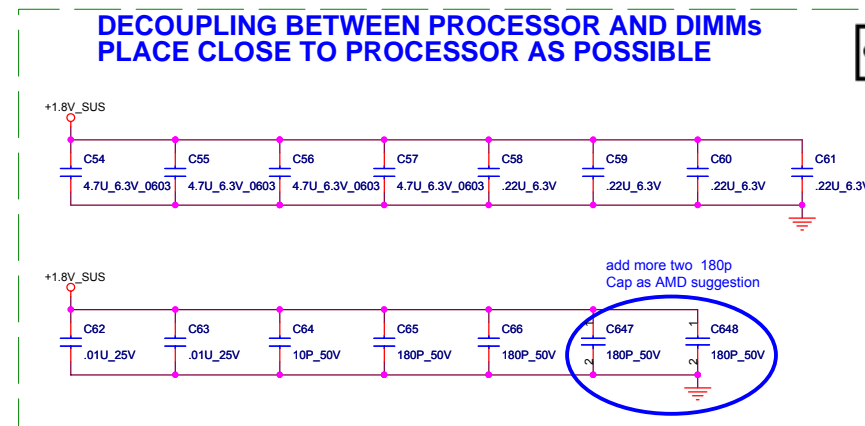
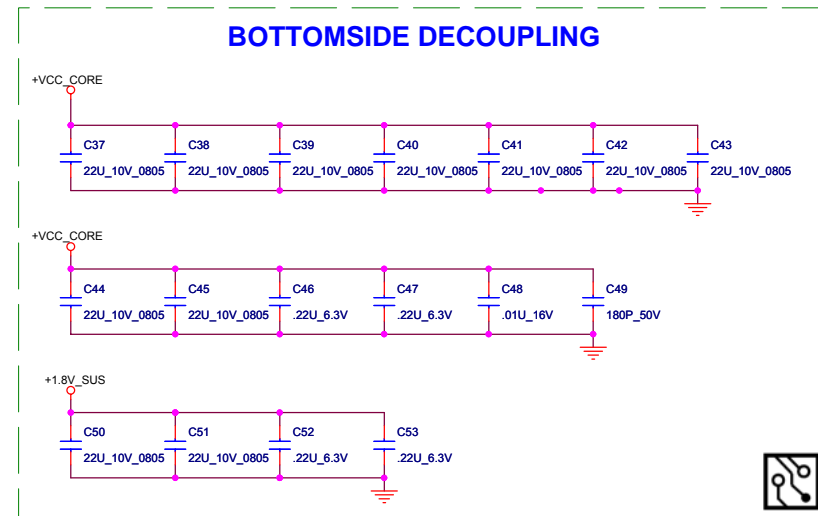
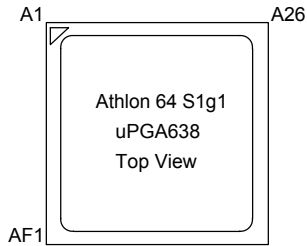
Socket B (far) Connections:

- M_B_DQ[0..63] (far):** M_B_DQ_0, M_B_DQ_1, M_B_DQ_2, M_B_DQ_3, M_B_DQ_4, M_B_DQ_5, M_B_DQ_6, M_B_DQ_7, M_B_DQ_8, M_B_DQ_9, M_B_DQ_10, M_B_DQ_11, M_B_DQ_12, M_B_DQ_13, M_B_DQ_14, M_B_DQ_15, M_B_DQ_16, M_B_DQ_17, M_B_DQ_18, M_B_DQ_19, M_B_DQ_20, M_B_DQ_21, M_B_DQ_22, M_B_DQ_23, M_B_DQ_24, M_B_DQ_25, M_B_DQ_26, M_B_DQ_27, M_B_DQ_28, M_B_DQ_29, M_B_DQ_30, M_B_DQ_31, M_B_DQ_32, M_B_DQ_33, M_B_DQ_34, M_B_DQ_35, M_B_DQ_36, M_B_DQ_37, M_B_DQ_38, M_B_DQ_39, M_B_DQ_40, M_B_DQ_41, M_B_DQ_42, M_B_DQ_43, M_B_DQ_44, M_B_DQ_45, M_B_DQ_46, M_B_DQ_47, M_B_DQ_48, M_B_DQ_49, M_B_DQ_50, M_B_DQ_51, M_B_DQ_52, M_B_DQ_53, M_B_DQ_54, M_B_DQ_55, M_B_DQ_56, M_B_DQ_57, M_B_DQ_58, M_B_DQ_59, M_B_DQ_60, M_B_DQ_61, M_B_DQ_62, M_B_DQ_63
- M_B_DQ[0..7] (far):** M_B_DQ_0, M_B_DQ_1, M_B_DQ_2, M_B_DQ_3, M_B_DQ_4, M_B_DQ_5, M_B_DQ_6, M_B_DQ_7

Processor Pin Connections:

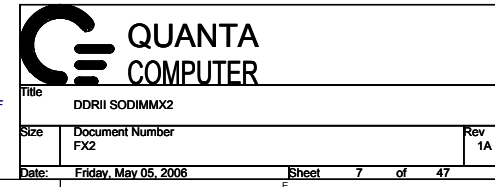
- MA_DAT[0..7] (near):** MA_DAT_0, MA_DAT_1, MA_DAT_2, MA_DAT_3, MA_DAT_4, MA_DAT_5, MA_DAT_6, MA_DAT_7
- M_A_DQ[0..63] (near):** M_A_DQ_0, M_A_DQ_1, M_A_DQ_2, M_A_DQ_3, M_A_DQ_4, M_A_DQ_5, M_A_DQ_6, M_A_DQ_7, M_A_DQ_8, M_A_DQ_9, M_A_DQ_10, M_A_DQ_11, M_A_DQ_12, M_A_DQ_13, M_A_DQ_14, M_A_DQ_15, M_A_DQ_16, M_A_DQ_17, M_A_DQ_18, M_A_DQ_19, M_A_DQ_20, M_A_DQ_21, M_A_DQ_22, M_A_DQ_23, M_A_DQ_24, M_A_DQ_25, M_A_DQ_26, M_A_DQ_27, M_A_DQ_28, M_A_DQ_29, M_A_DQ_30, M_A_DQ_31, M_A_DQ_32, M_A_DQ_33, M_A_DQ_34, M_A_DQ_35, M_A_DQ_36, M_A_DQ_37, M_A_DQ_38, M_A_DQ_39, M_A_DQ_40, M_A_DQ_41, M_A_DQ_42, M_A_DQ_43, M_A_DQ_44, M_A_DQ_45, M_A_DQ_46, M_A_DQ_47, M_A_DQ_48, M_A_DQ_49, M_A_DQ_50, M_A_DQ_51, M_A_DQ_52, M_A_DQ_53, M_A_DQ_54, M_A_DQ_55, M_A_DQ_56, M_A_DQ_57, M_A_DQ_58, M_A_DQ_59, M_A_DQ_60, M_A_DQ_61, M_A_DQ_62, M_A_DQ_63
- M_A_DQ[0..7] (near):** M_A_DQ_0, M_A_DQ_1, M_A_DQ_2, M_A_DQ_3, M_A_DQ_4, M_A_DQ_5, M_A_DQ_6, M_A_DQ_7

Athlon 64 S1
Processor Socket

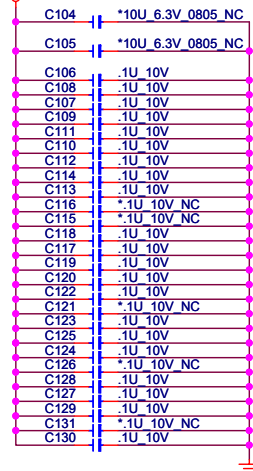


PROCESSOR POWER AND GROUND

- http://laptopblue.~.sus

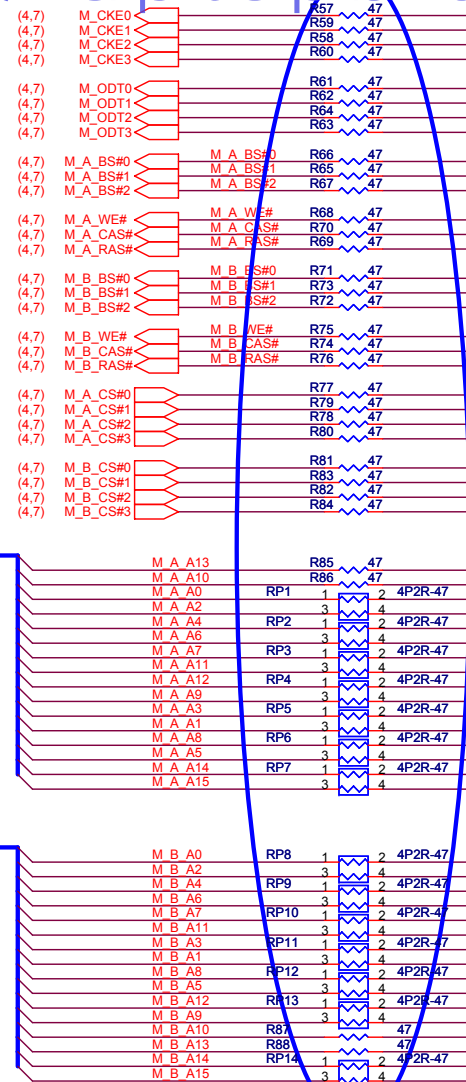


+0.9V_DDR_VTT



(4,7) M_A_A[0..15]

(4,7) M_B_A[0..15]



RTT termination changed from 56 ohm to 47 ohm as AMD suggestion



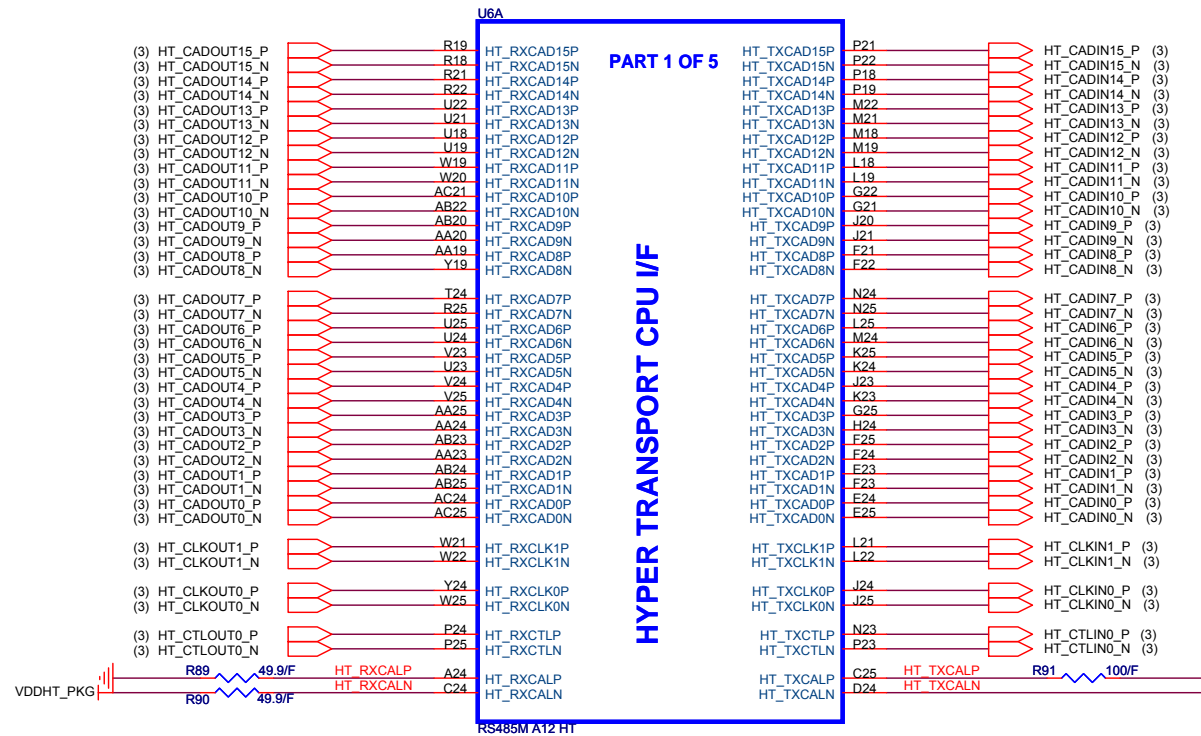
Title
DDRII TERMINATION

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Rev
1A



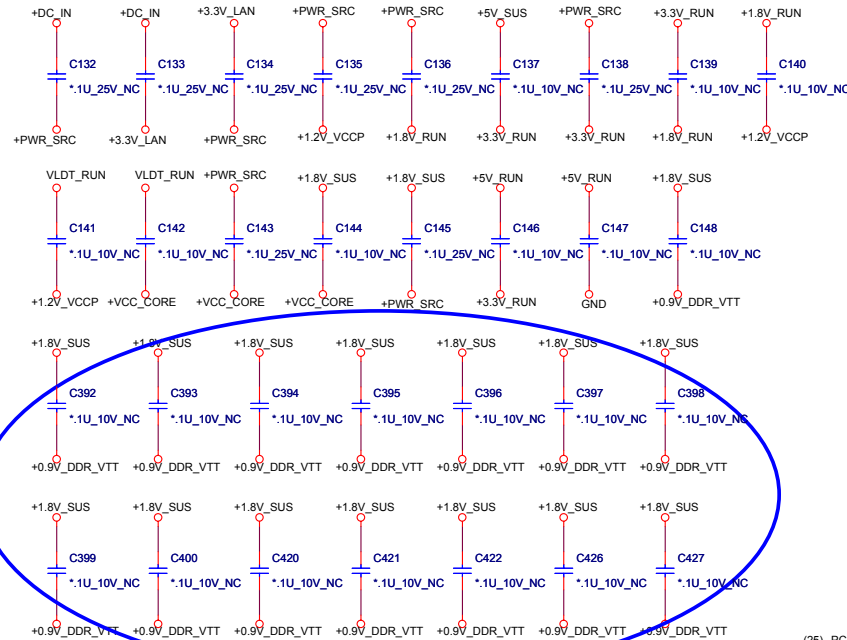
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Size Document Number FX2

Rev 1A

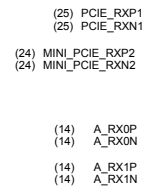
Date: Friday, May 05, 2006

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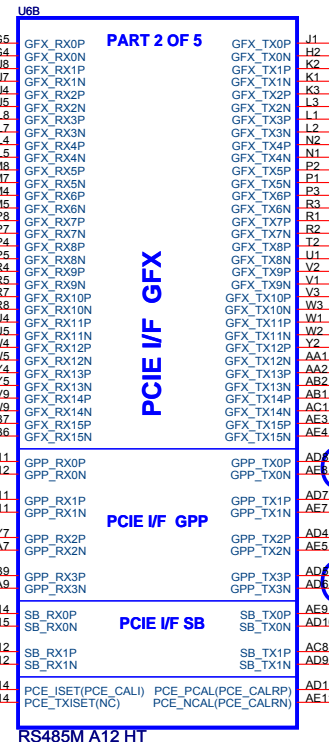


reserve more 14 Cap. between +0.9V_DDR_VTT & +1.8V_SUS

delete PCIE signal , original LAN & Mini Card of ED5



R93: 10KOhm FOR RS485
1.47KOhm FOR RS690
R92: 8.25KOhm FOR RS485
DNI FOR RS690



RS485M A12 HT

R95: 150 Ohm FOR RS485
562 Ohm FOR RS690
R94: Ward update to 100 Ohm FOR RS485
2KOhm FOR RS690



Place these caps close to connector

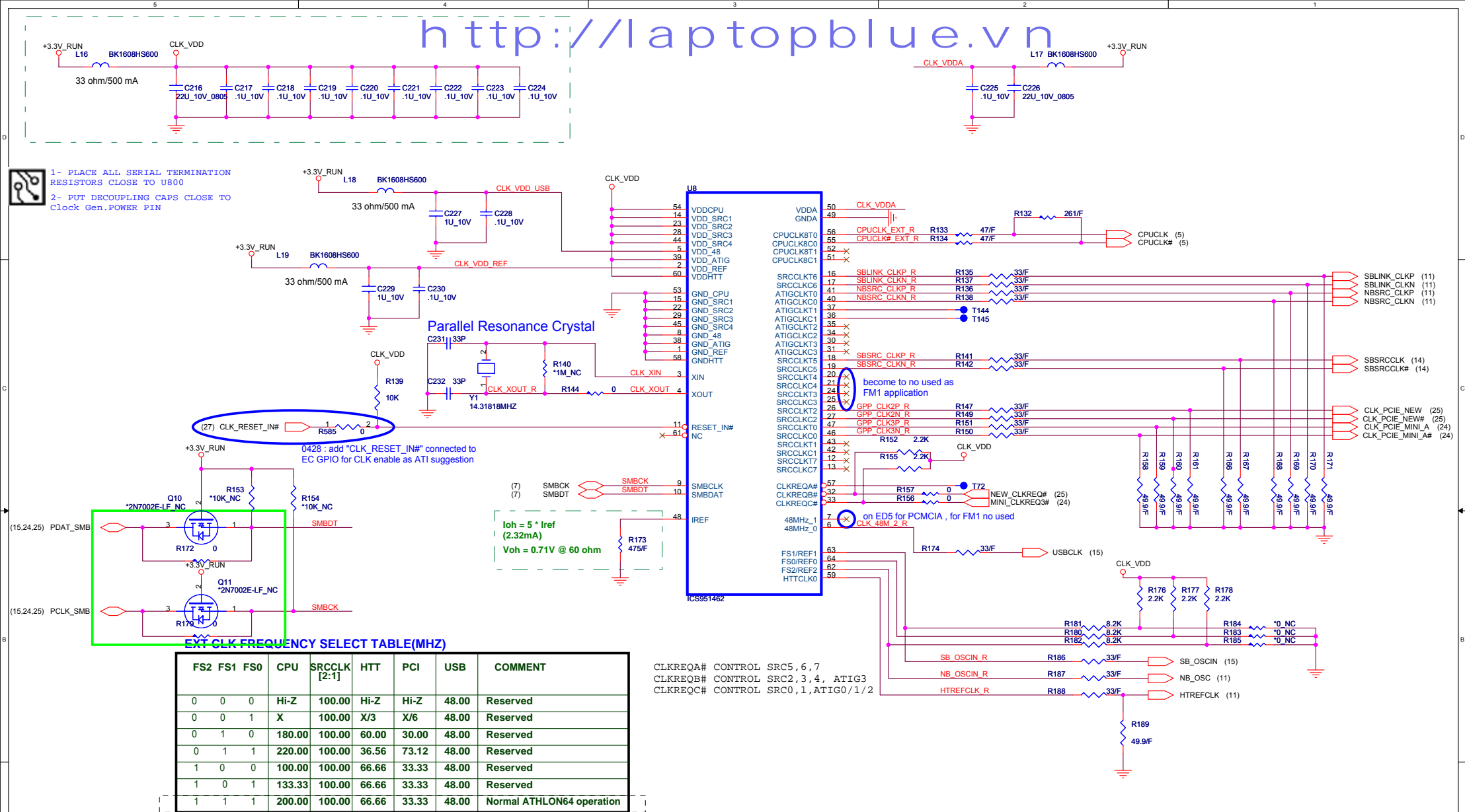


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Title RS485-PCIE LINK I/F			
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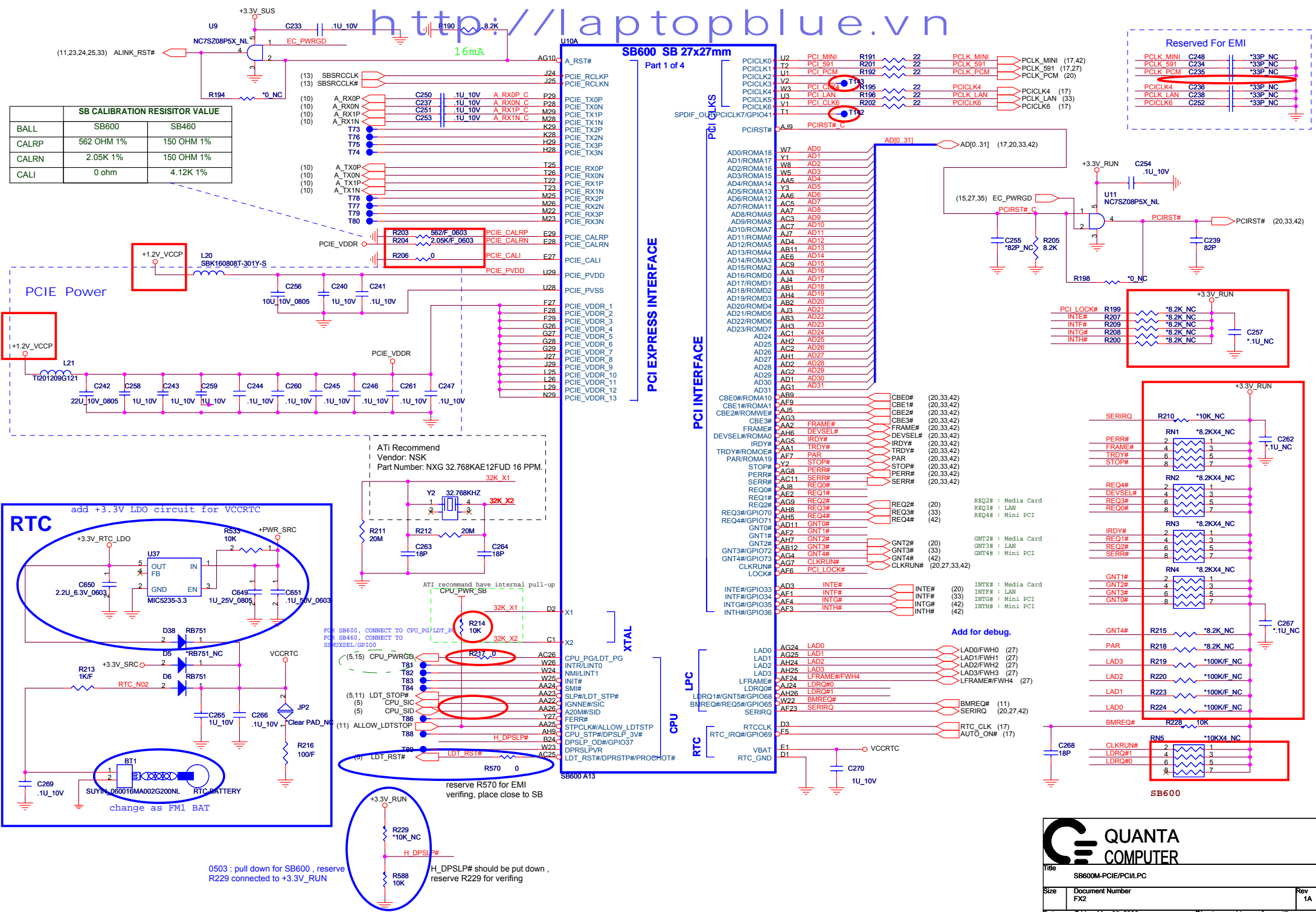


- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO Clock Gen. POWER PIN

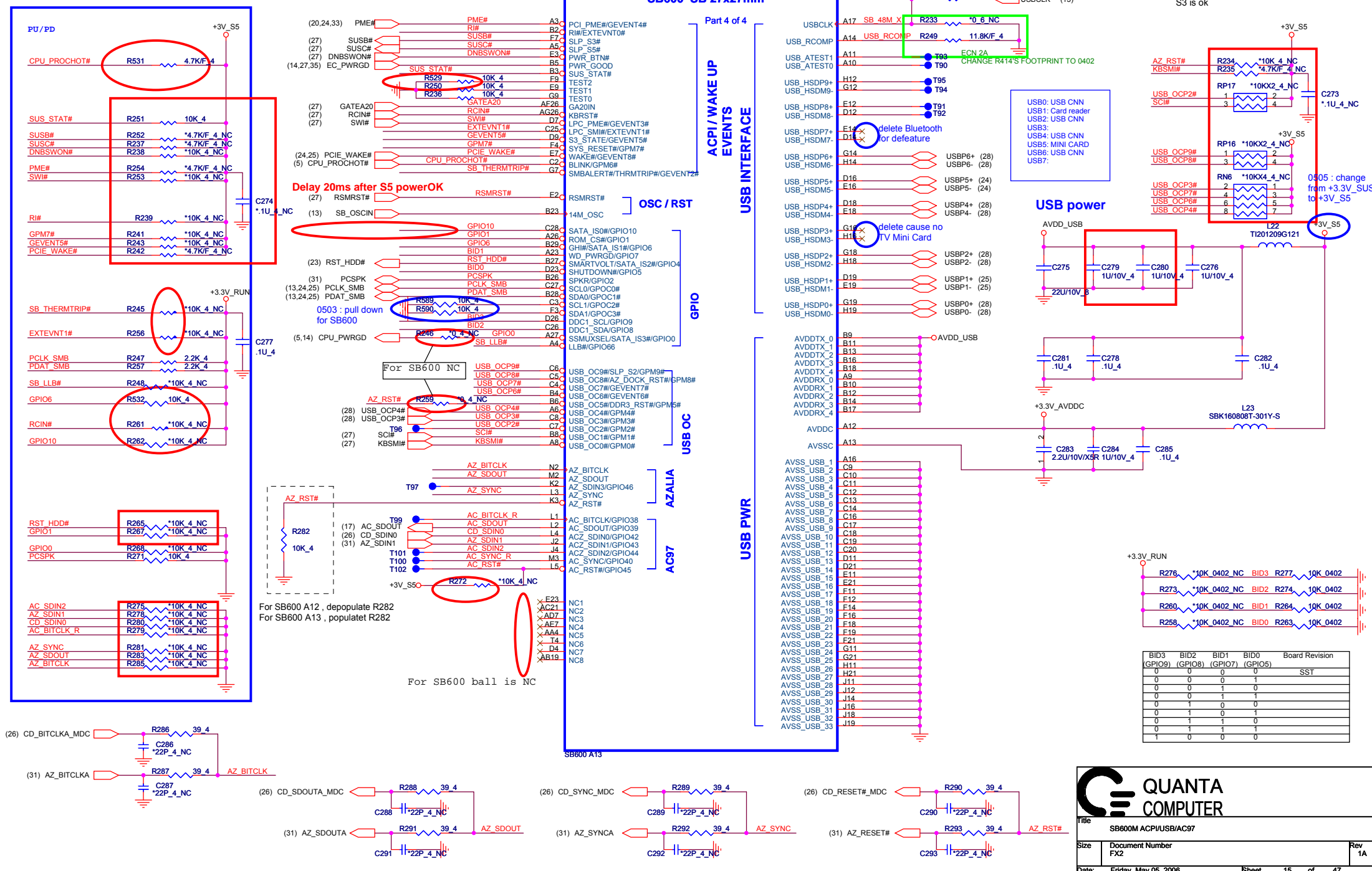


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	SB CALIBRATION RESISTOR VALUE	
BALL	SB600	SB460
CALRP	562 OHM 1%	150 OHM 1%
CALRN	2.05K 1%	150 OHM 1%
CALI	0 ohm	4.12K 1%

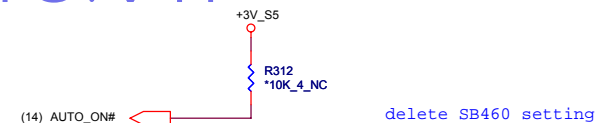
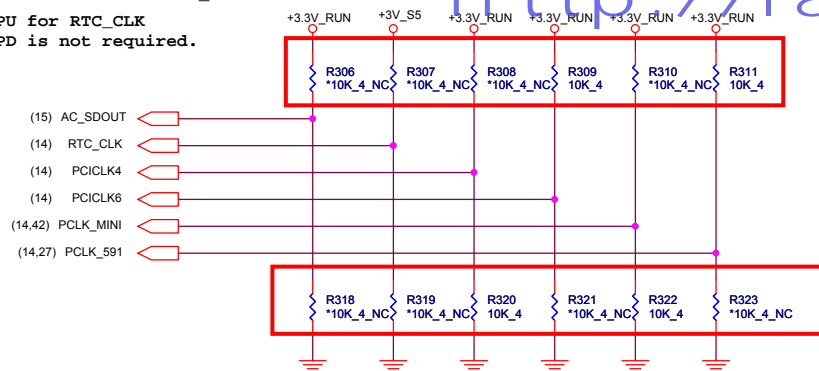


USB0: USB CNN
USB1: Card reader
USB2: USB CNN
USB3:
USB4: USB CNN
USB5: MINI CARD
USB6: USB CNN
USB7:



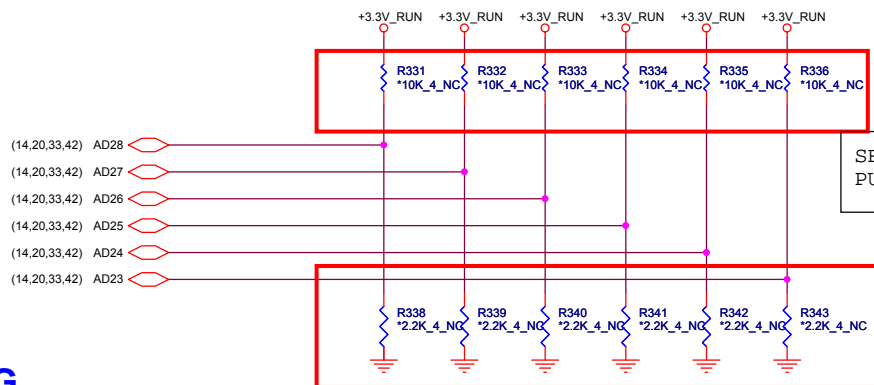
BID3 (GPIO9)	BID2 (GPIO8)	BID1 (GPIO7)	BID0 (GPIO5)	Board Revision
0	0	0	0	SST
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	

SB600 has 15K internal PD for AC_SDOUT
15K internal PU for RTC_CLK
,External PU/PD is not required.



REQUIRED STRAPS

		PCLK_MINI		PCLK_591	
	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INT. PLL48	CPU IF=K8	H, H = PCI ROM H, L = SPI ROM
PULL LOW	IGNORE DEBUG STRAPS	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4	L, H = LPC ROM L, L = FWH ROM



SB600 HAS 15K INTERNAL
PU FOR PCI_AD[28:23]


DEBUG STRAPS

	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET	Use Long Reset	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	boot fail time disabled
PULL LOW	USE SHORT RESET	Use Short Reset	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	boot fail time enabled

SB460
Only

SB600
Only

SB600
Only

 QUANTA COMPUTER		
Title SB600M STRAPS		
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change name as ED5 SB.

(1) LCD_POWER_ON

LID_CL_PRES# need to connected to EC.

LID_CL# is connected to pull high circuit , then EC , as Page of EC.

For Discrete:
De-populate J1,R230,C311,C331,C332,
D16,C333,C329,C341,C324,C326

change name as ED5 SB.

as Tom suggestion , connect
to EC "MBCLK" & "MBDATA".

as Tom suggestion , connect
to EC "MBCLK" & "MBDATA".

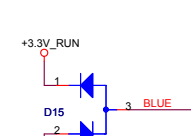
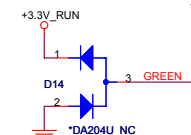
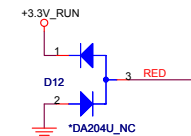
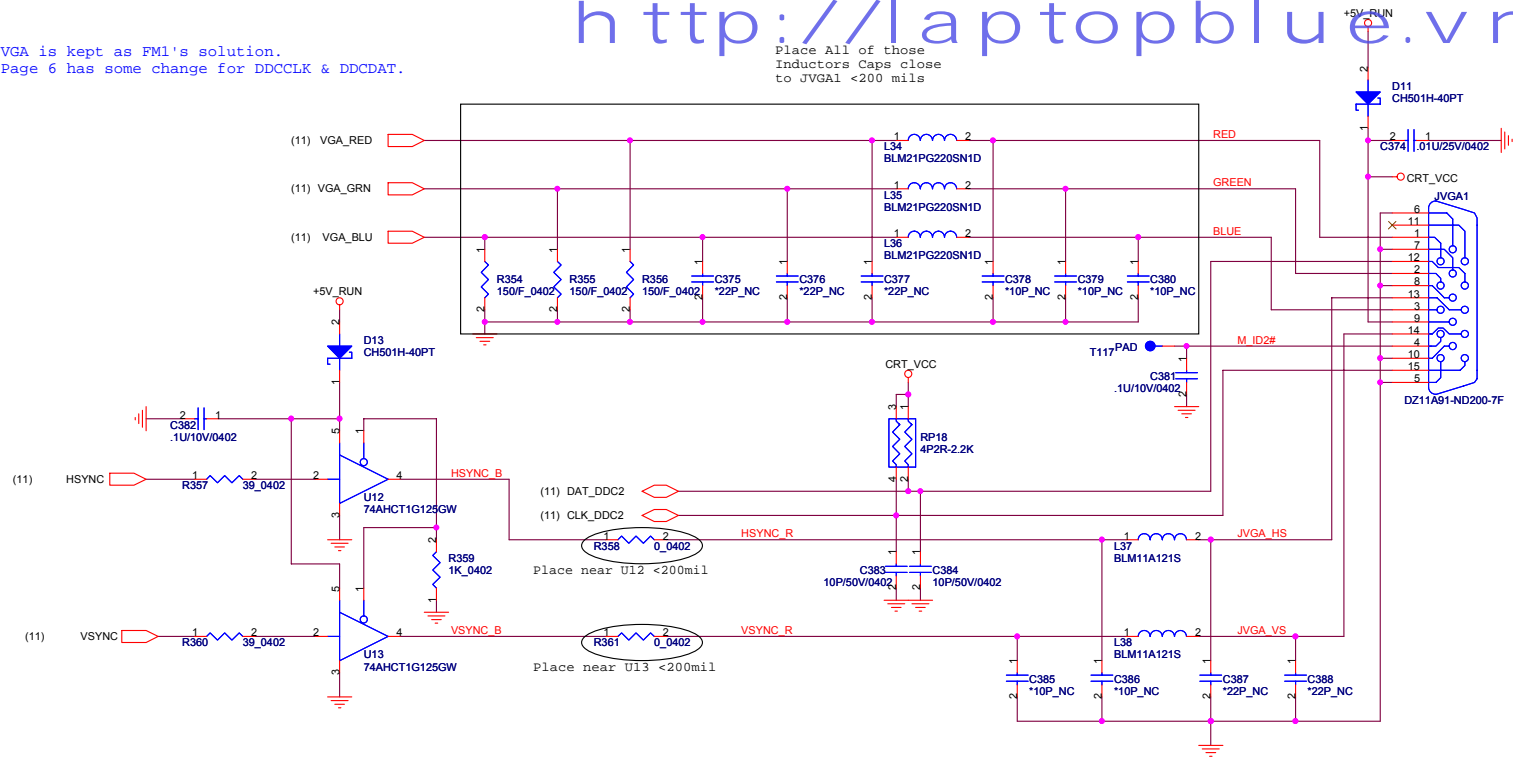


QUANTA
COMPUTER

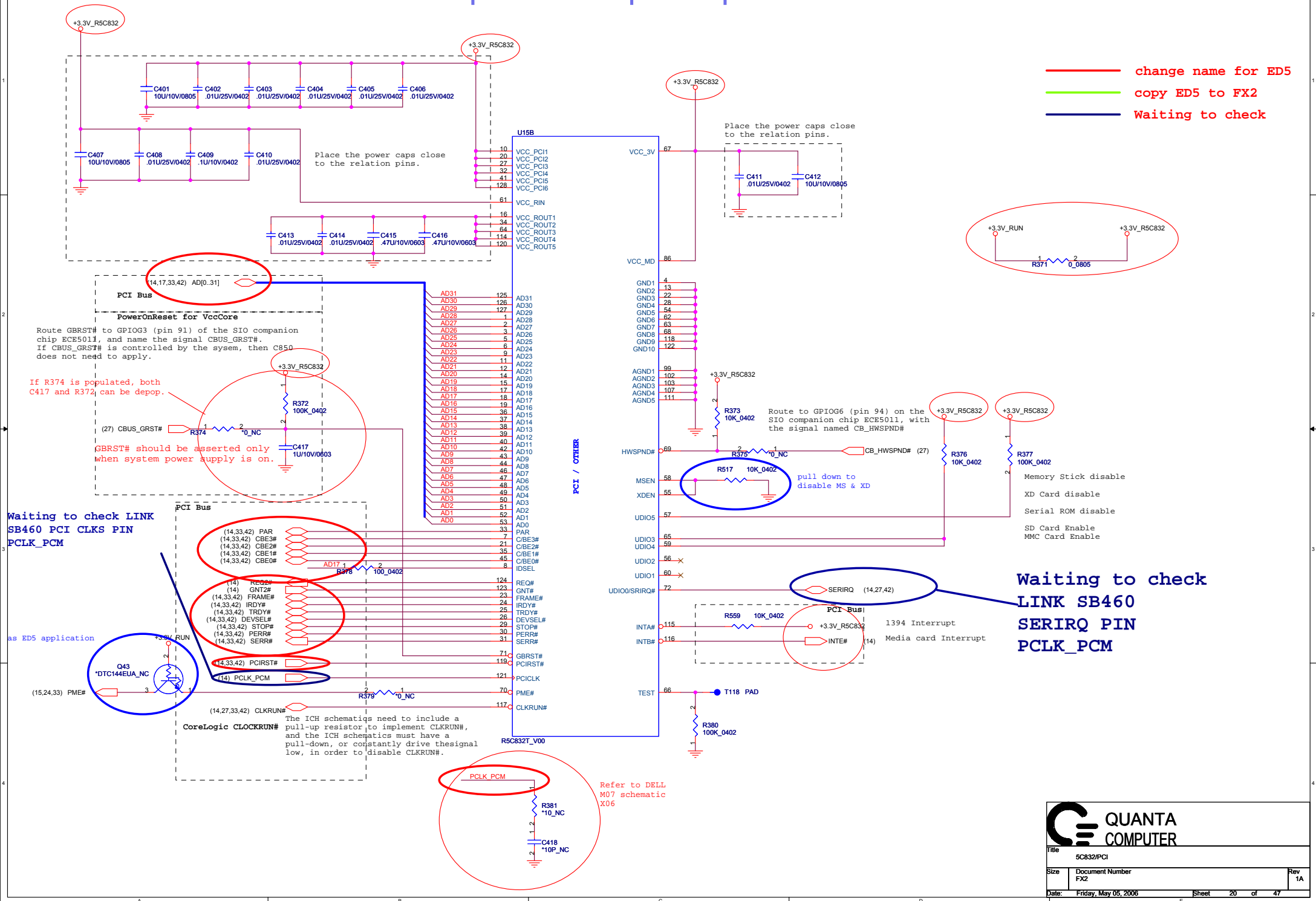
Title LCD CONN		
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VGA is kept as FMI's solution.
Page 6 has some change for DDCCLK & DDCDAT.

Place All of those
Inductors Caps close
to JVGA1 <200 mils

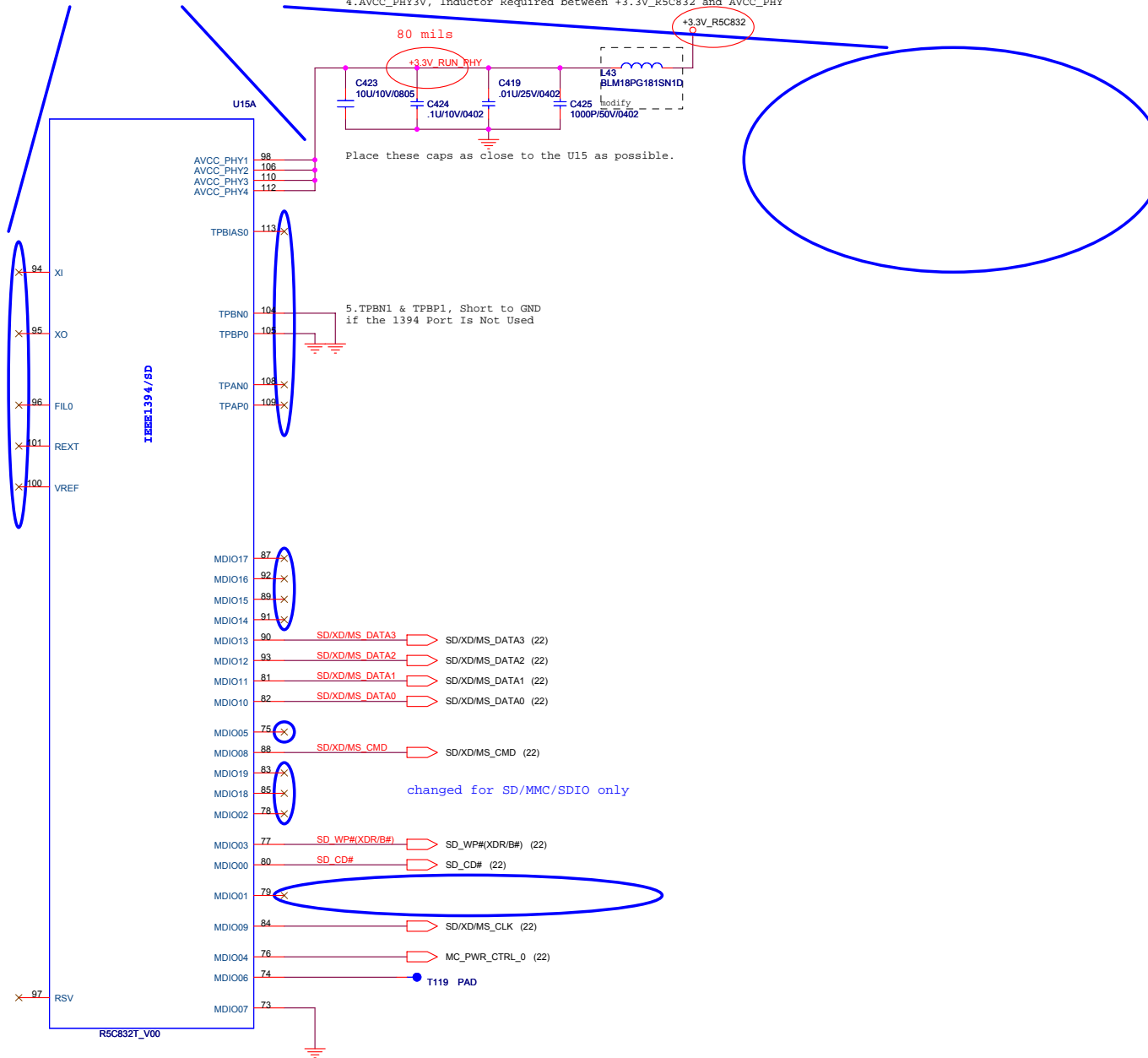


delete Svideo for defeature



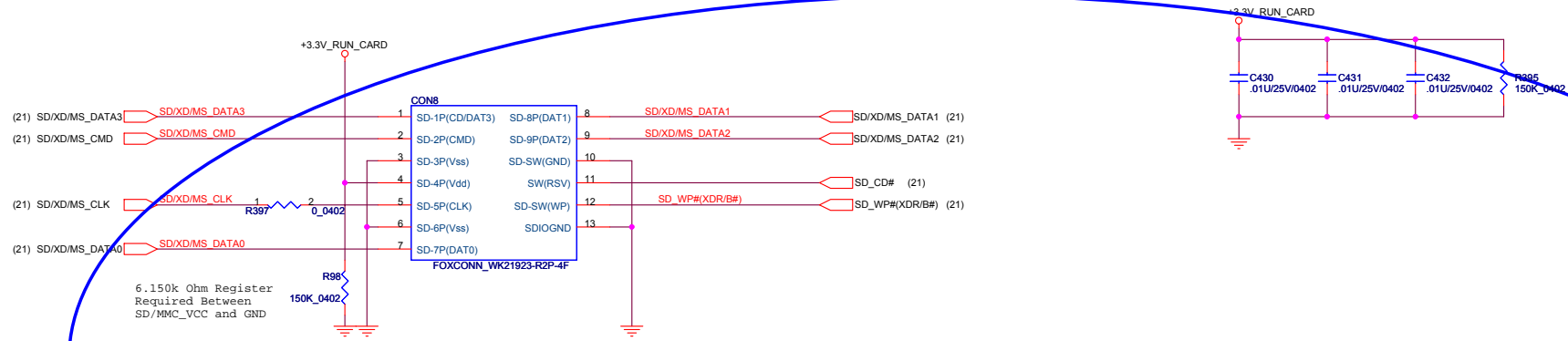
deleted 1394 for defeature

3.AVCC_PHY3V, connection with +3.3V_R5C832 power
4.AVCC_PHY3V, Inductor Required between +3.3V_R5C832 and AVCC_PHY



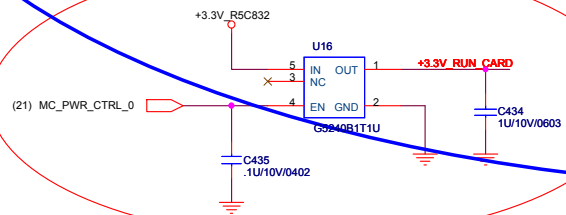
DO NOT INSERT SD/MMC SIMULTANEOUSLY.

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changed for SD/MMC/SDIO only

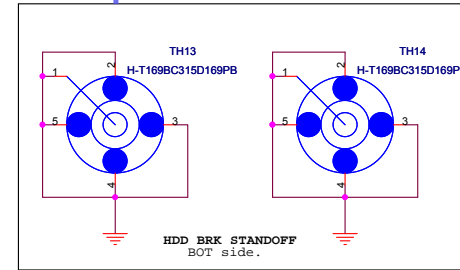


3 IN 1 CARD READER

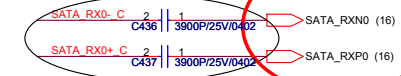
For SD/MS power



SATA HDD



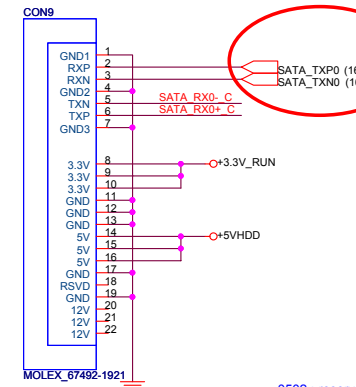
Place close to
connector side



Locate caps C558, C559 near HDL Conn.
Length match SATA_C_RX0- & SATA_C_RX0+ within 20mils.

SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:
SATA drive power consumption estimate at
MobileMark is 1.1W. An additional 150mW
can be saved using Intel's IMST driver.

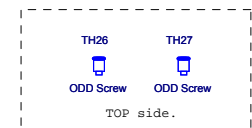


- change name for ED5

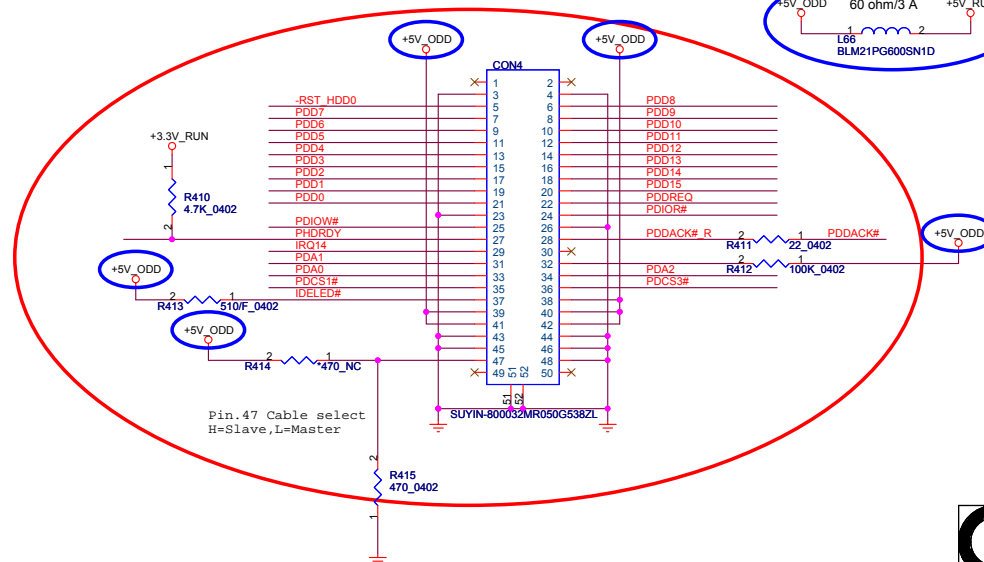
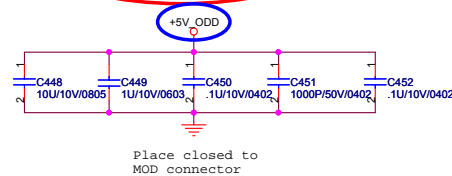
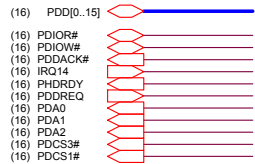
- copy ED5 to FX2

- Waiting to check

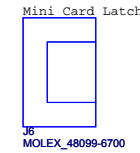
0502 : reserve L66 for current measurement , can be removed and short directly after RTS ; and change +5V_RUN to +5V_ODD for ODD side power



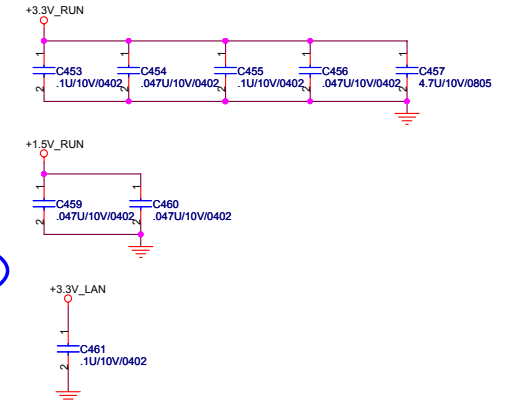
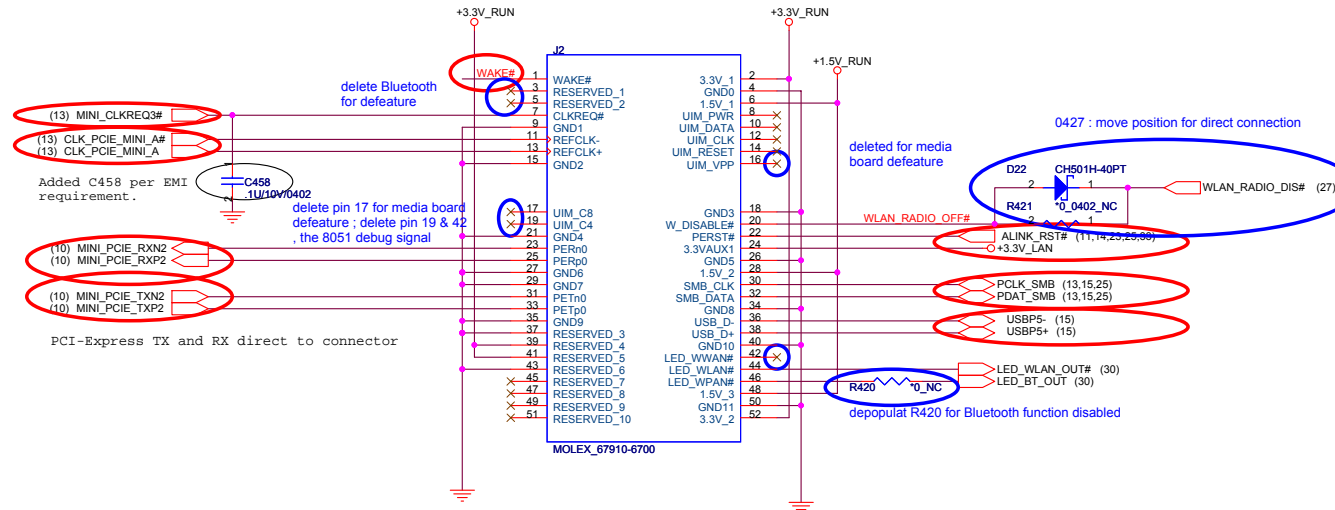
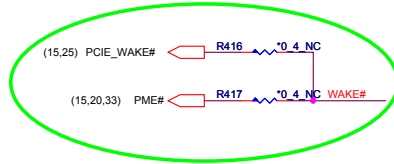
PATA ODD



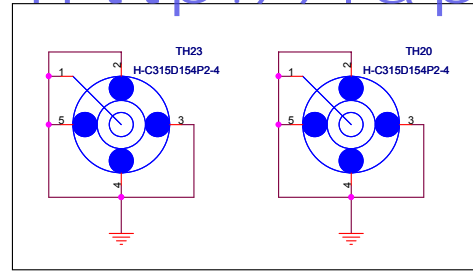
MINI CARD



- change name for ED5
- copy ED5 to FX2
- Waiting to check



Express Card



- change name for ED5
- copy ED5 to FX2
- Waiting to check

NEW CARD GUIDE POST
TOP side.

swap traces as "fx2_swap-0412"

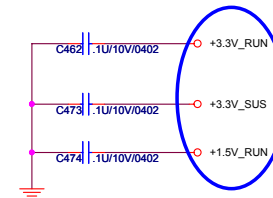
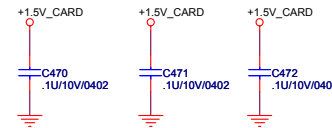
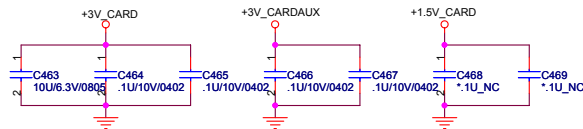
as ED5 application

reserve for pull up

+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

0427 : change from only net
name to symbol "power point"

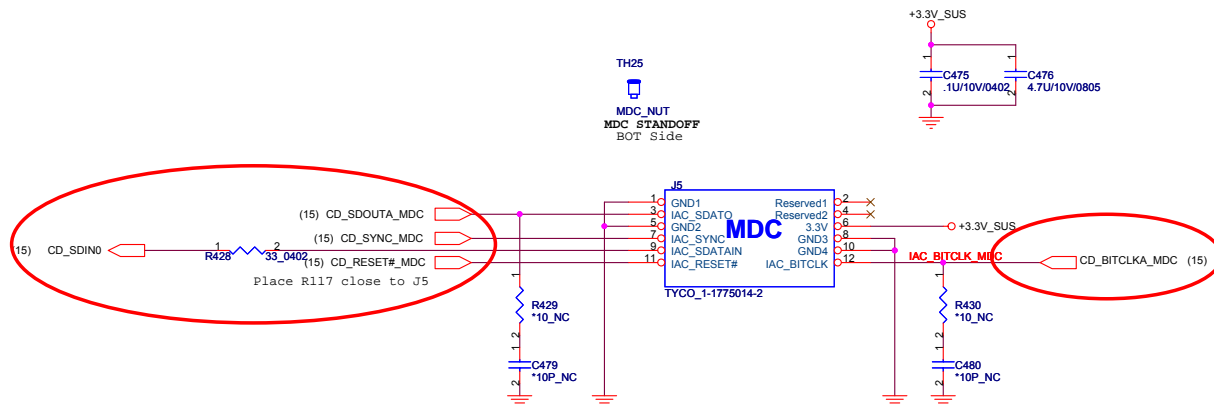


MDC INTERFACE

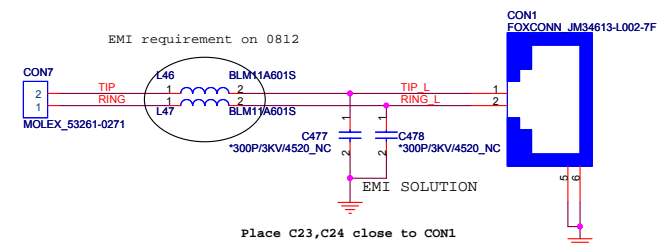
http://laptopblue.vn

MDC Layout Notes

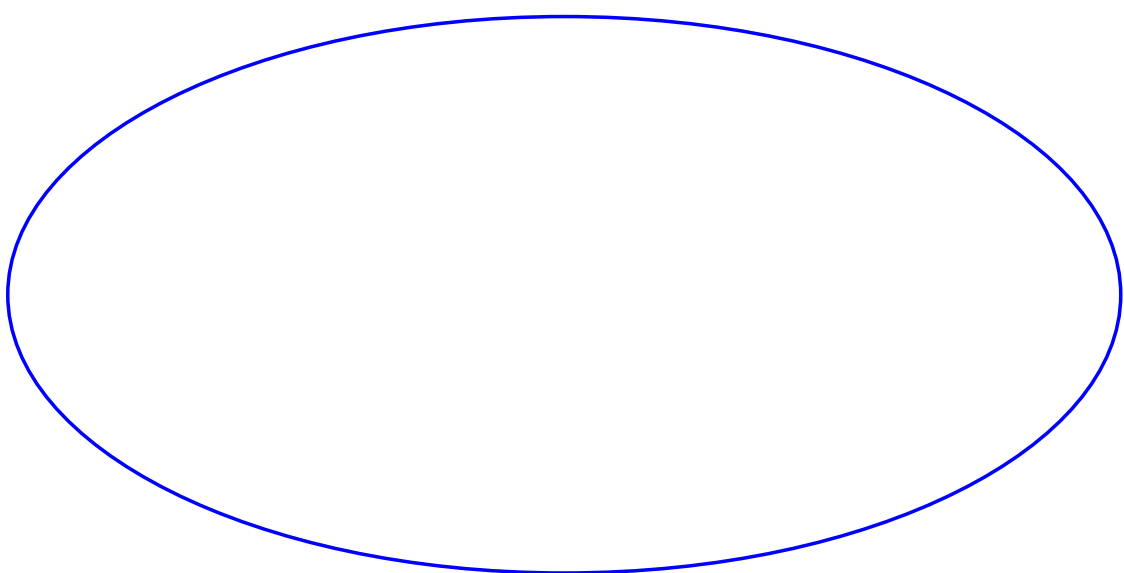
1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Tip and Ring connector pitch = 25 mils
4. Keep out area from Tip and Ring to other signals = 100 mils
5. Power and Ground minimum trace width to connector = 20 mils
6. Route Tip and Ring on one layer only (top or bottom)
7. Modem internal cable wire size = 26 AWG (stranded or twisted pair wire)

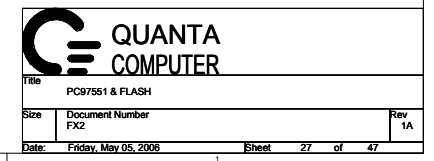


- change name for ED5
- copy ED5 to FX2
- Waiting to check



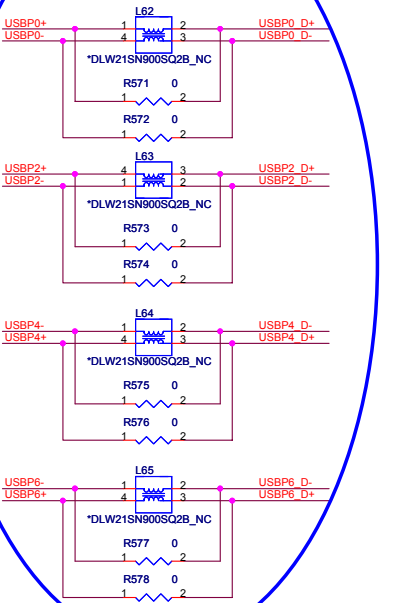
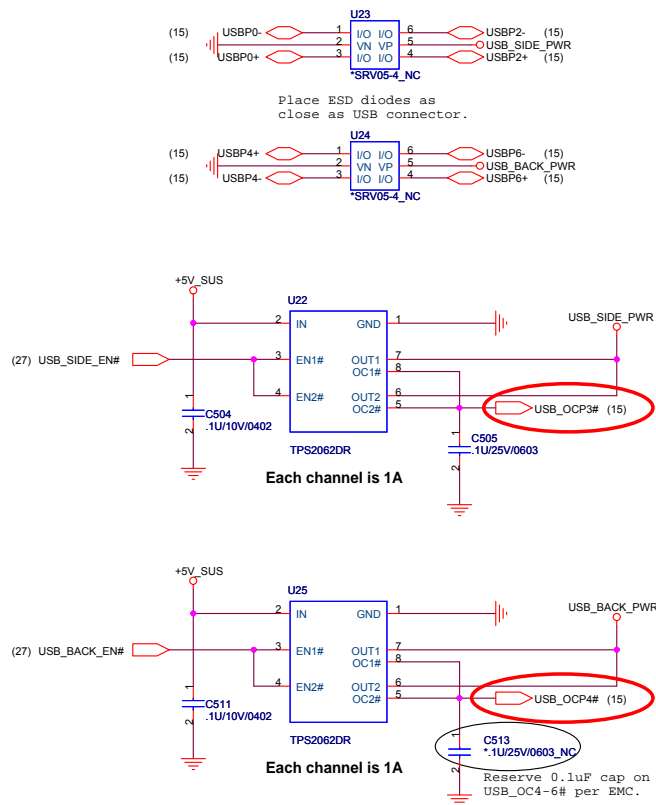
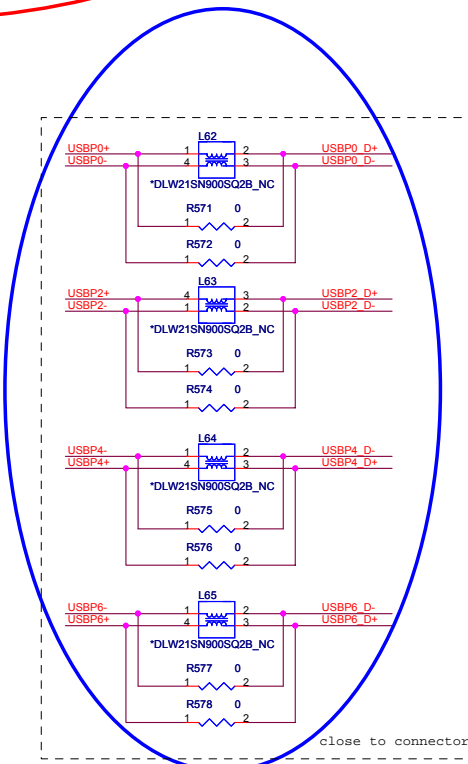
delete Bluetooth
for defeature



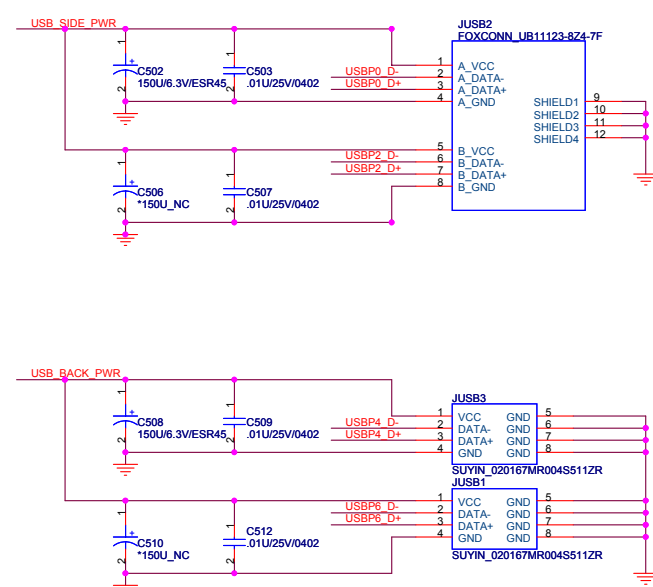


- change name for ED5
- copy ED5 to FX2
- Waiting to check

8Mbit (1M Byte), SPI



add for EMI suggestion ,
0502 : swap P0/P2 traces as "fx2-swap-0502"



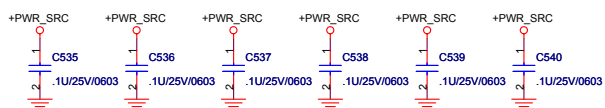
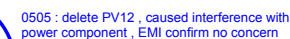
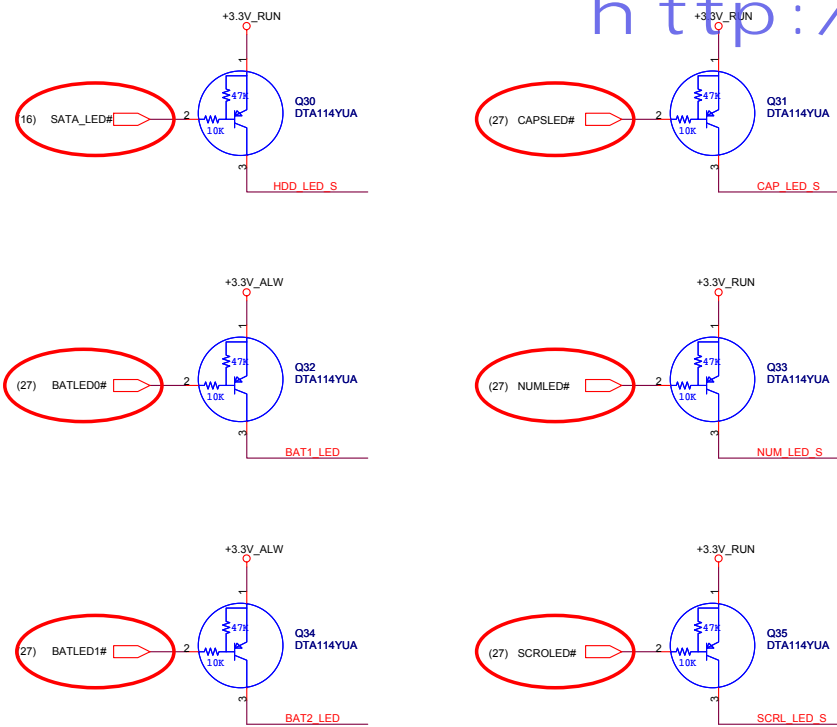
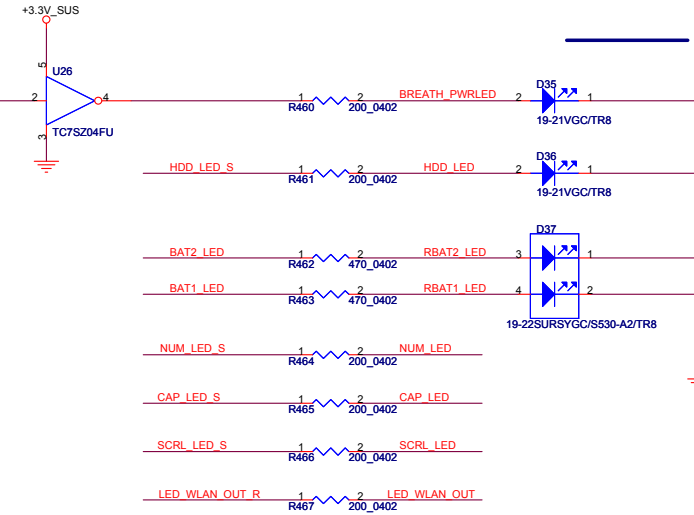


Figure 10 illustrates the recommended decoupling capacitor placement for the CPU and DDR II connector. The diagram shows two rows of capacitors, each connected to a +1.8V_SUS supply and ground. The top row, labeled "place close to CPU", contains capacitors C681 through C688. The bottom row, labeled "place close to DDR II connector", contains capacitors C689 through C700. Each capacitor is connected to a +1.8V_SUS supply and ground. The capacitors are arranged in a staggered pattern between two blue curved lines representing the PCB edges.



0427 : change from
BREATH_LED to BREATH_LED#

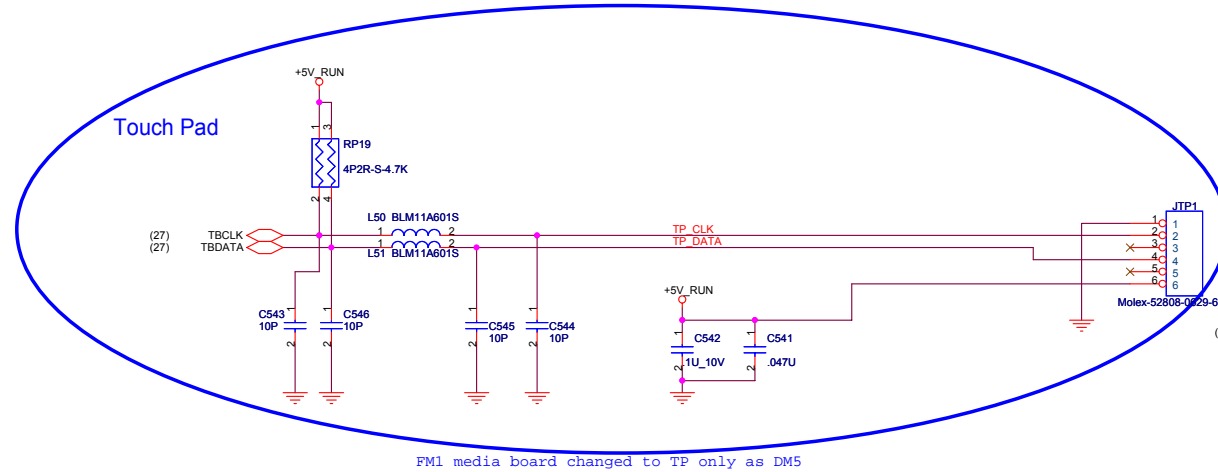
27) BREATH_LED#



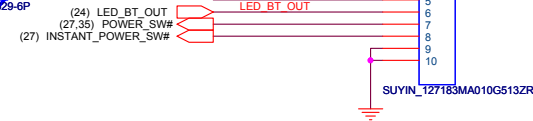
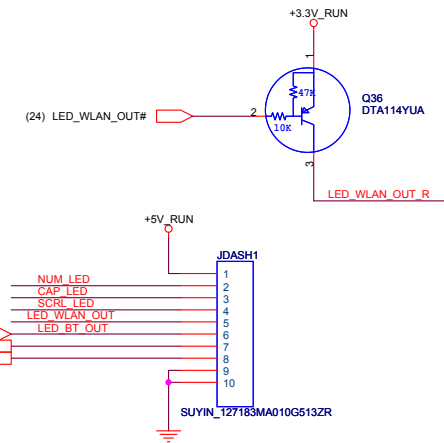
change name for ED5

copy ED5 to FX2

Waiting to check



FM1 media board changed to TP only as DM5



SWITCH & TP & LED

0502 : reserve L67 for current measurement , can be removed and short directly after RTS

name change as ED5

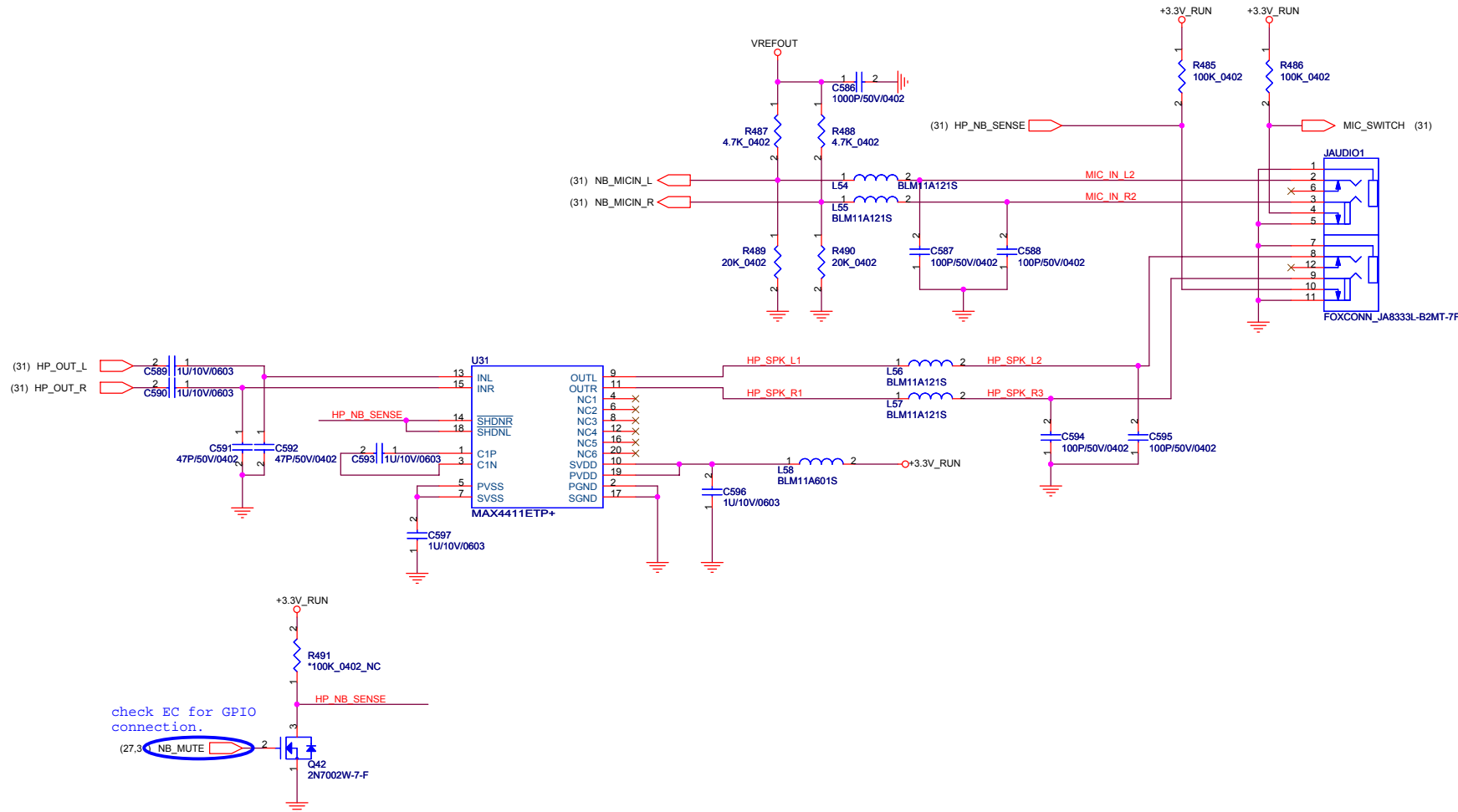
SDIN Res is 33 on FM1 , 22 on ED5 !!

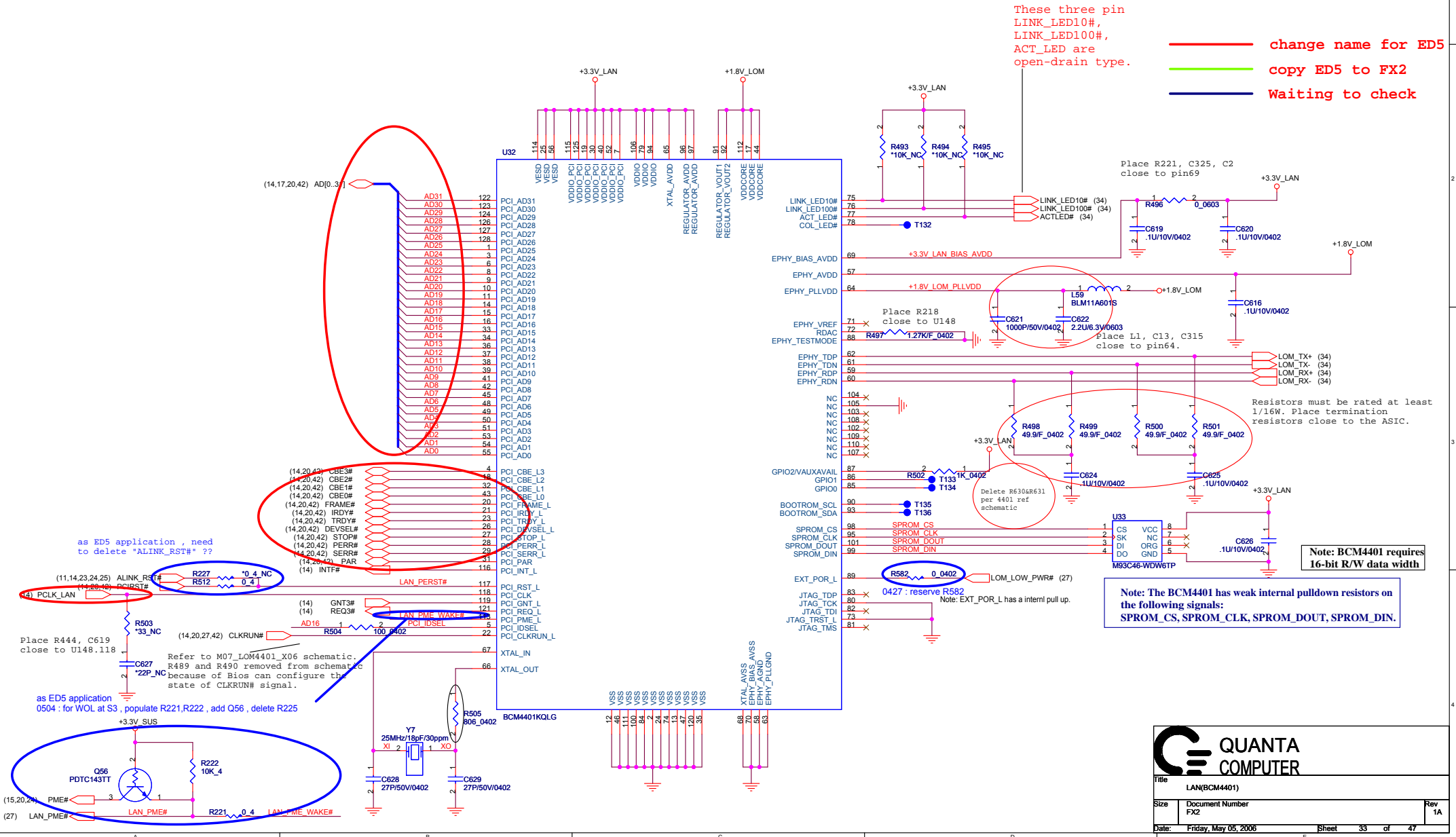
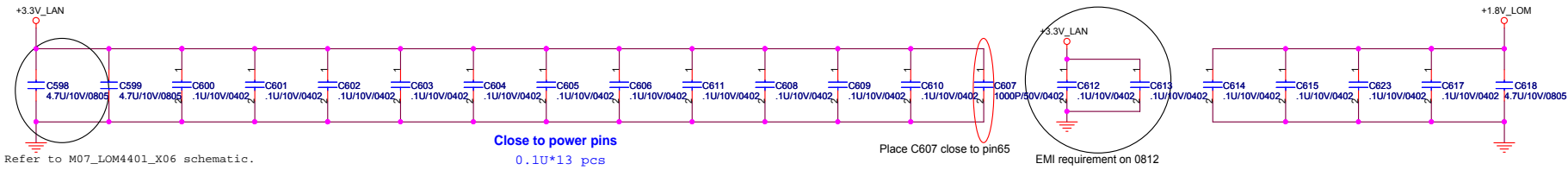
Reserved R463 of HP_NB_SENSE per ref schematic.

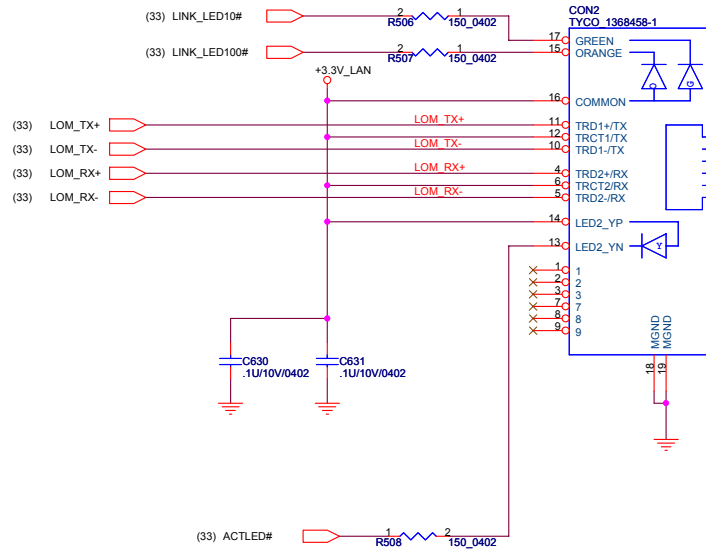
name change from SPKR to PCSPK as ED5.

name change as ED5

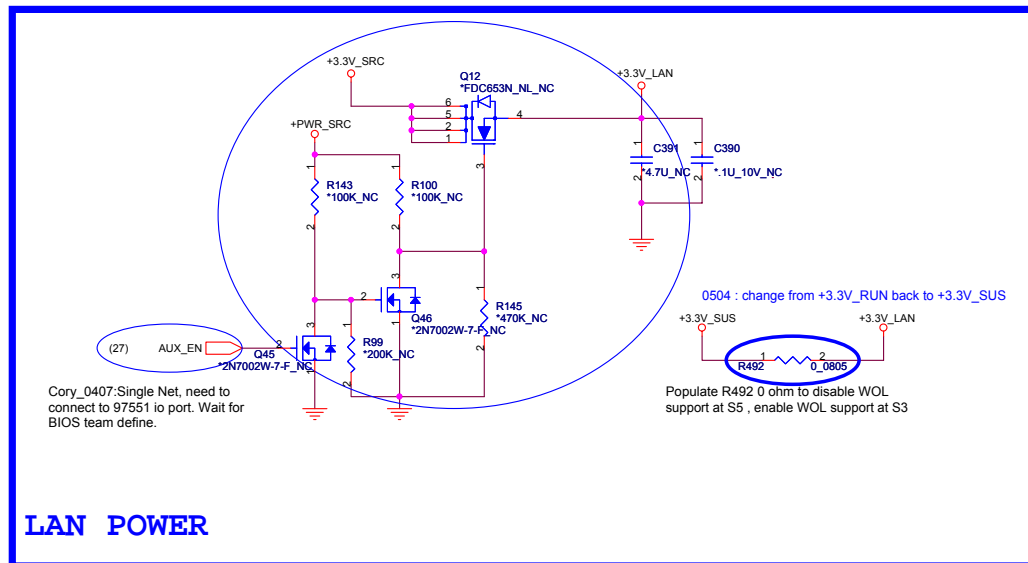
GAIN0	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



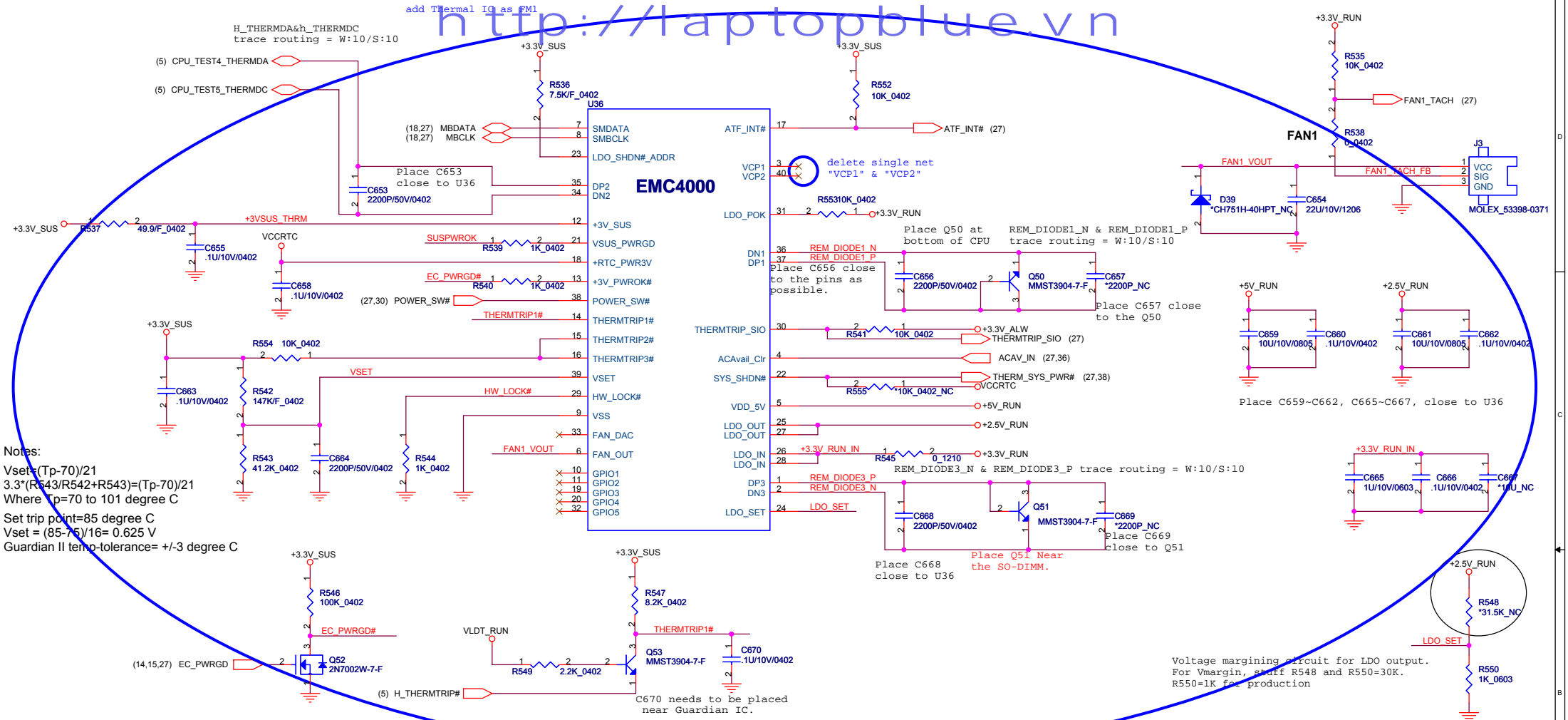




- change name for ED5
- copy ED5 to FX2
- Waiting to check
- copy DM5 to FX2

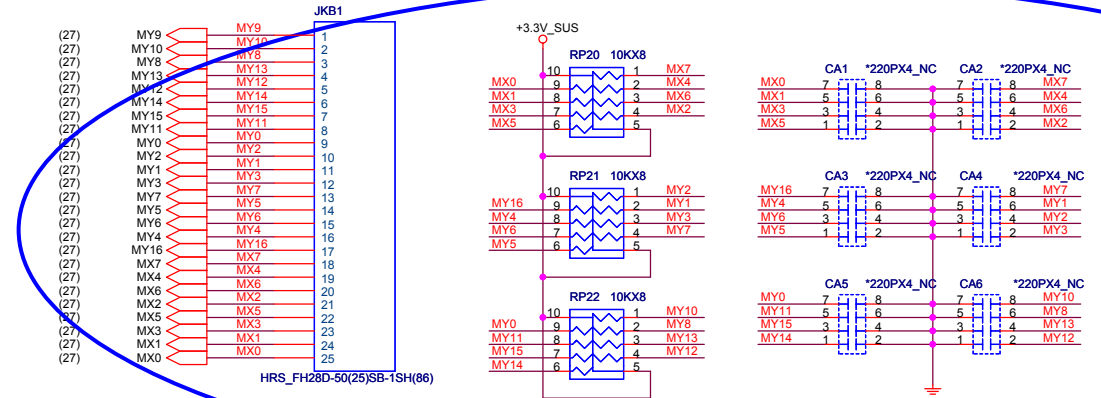


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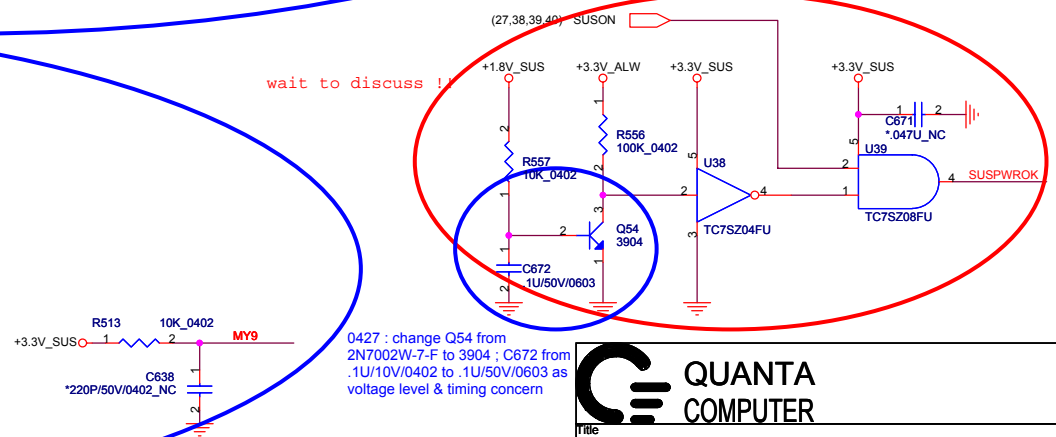



Notes:
Vset=(Tp-70)/21
3.3*(R543/R542+R543)=(Tp-70)/21
Where Tp=70 to 101 degree C
Set trip point=85 degree C
Vset = (85-76)/16= 0.625 V
Guardian II temp-tolerance= +/-3 degree C

as FM1 keyboard matrix & "e0788.1104a_swap-0422"



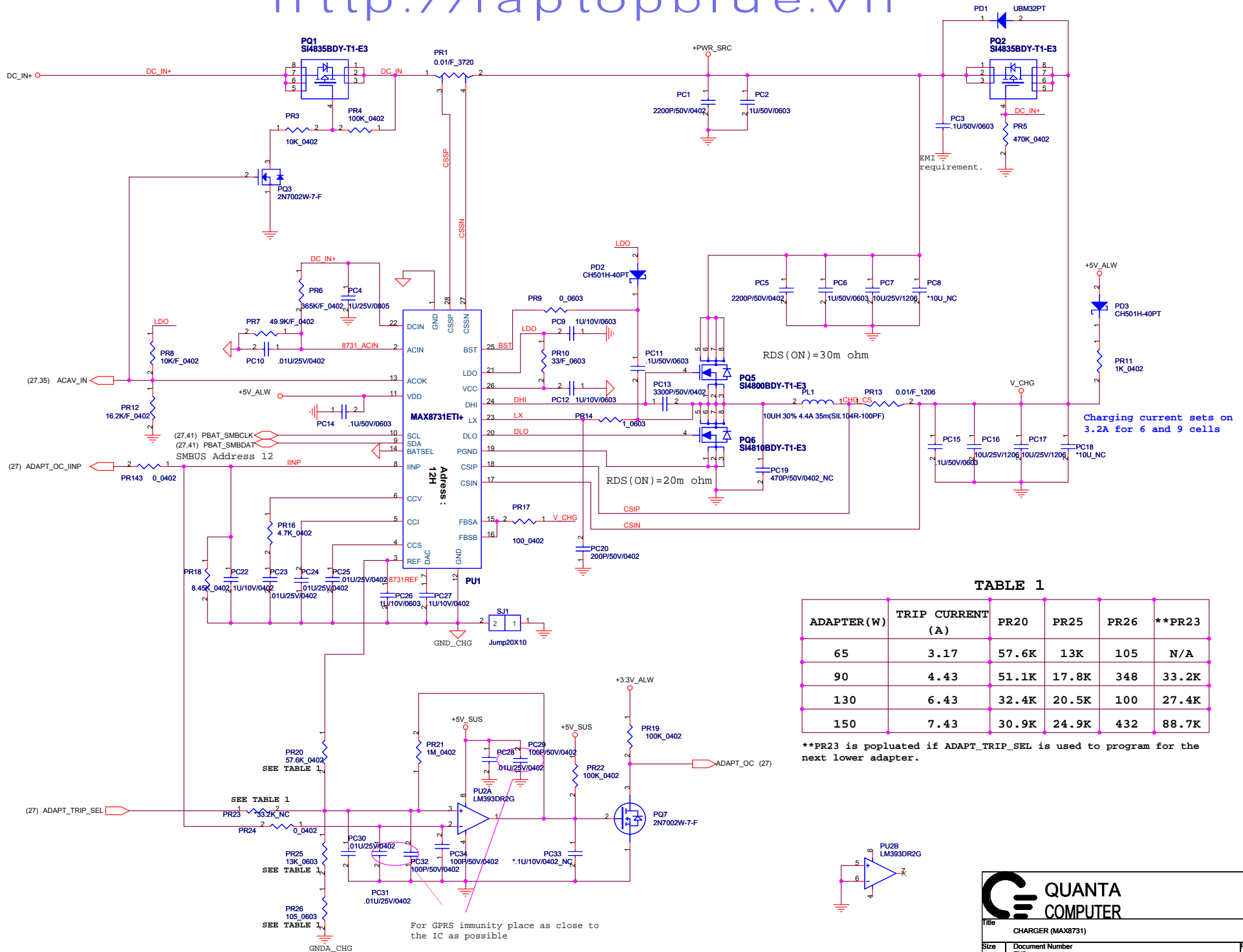
KBC





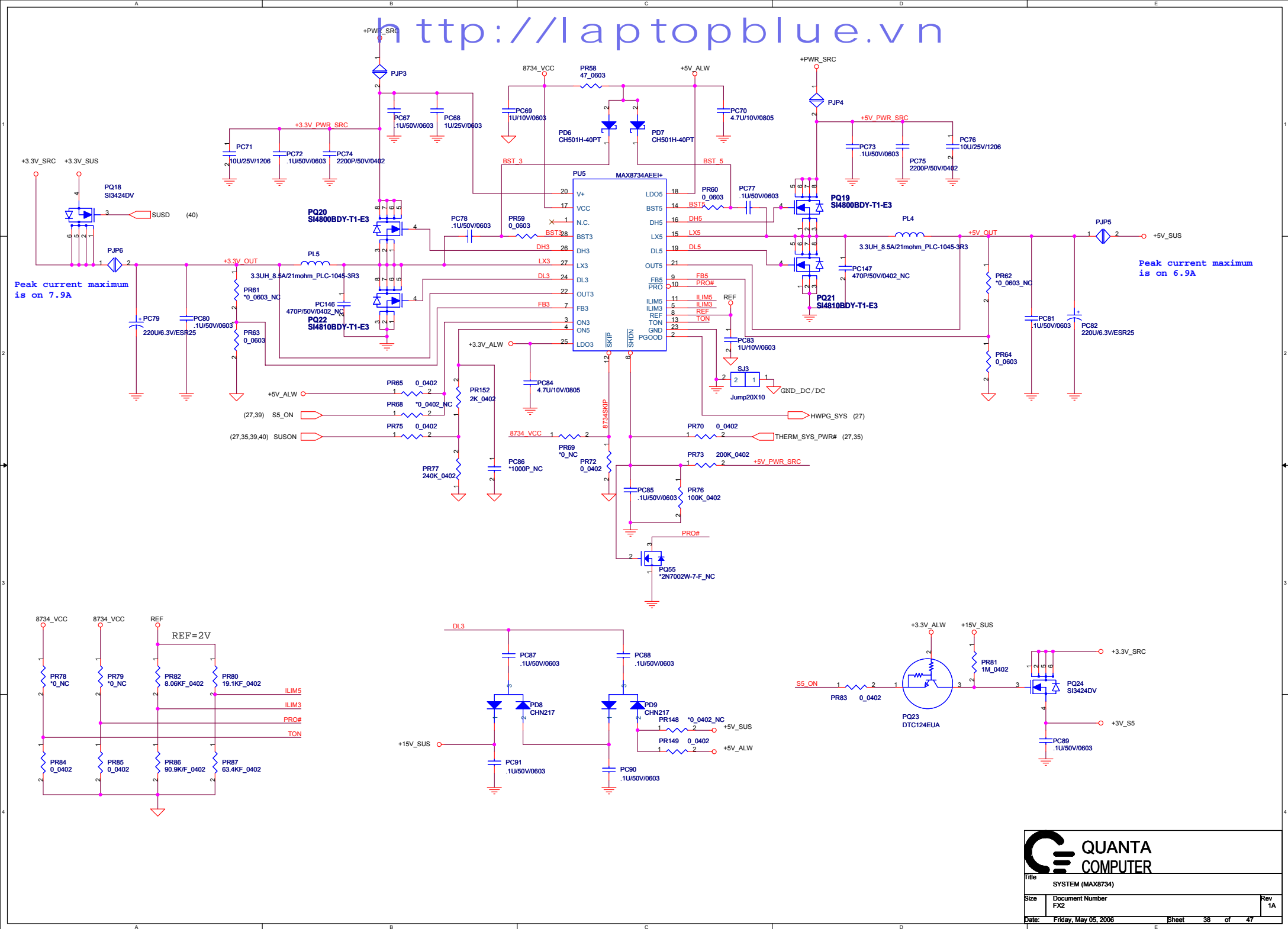
QUANTA
COMPUTER

Title		
KB & THERMAL & FAN		
Size	Document Number	Rev
FX2		1A
Date:	Friday, May 05, 2006	Sheet 35 of 47

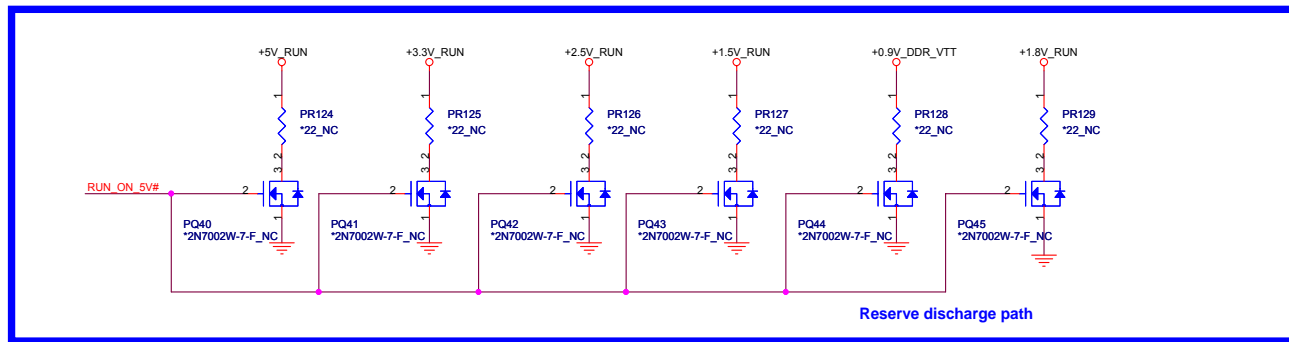
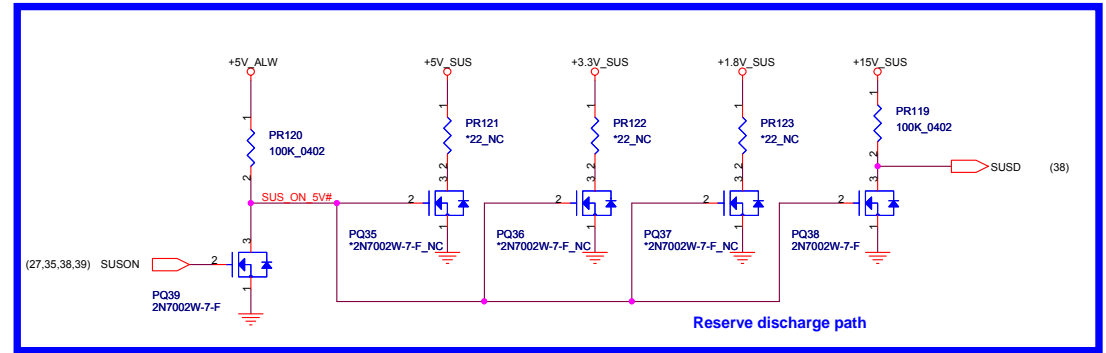
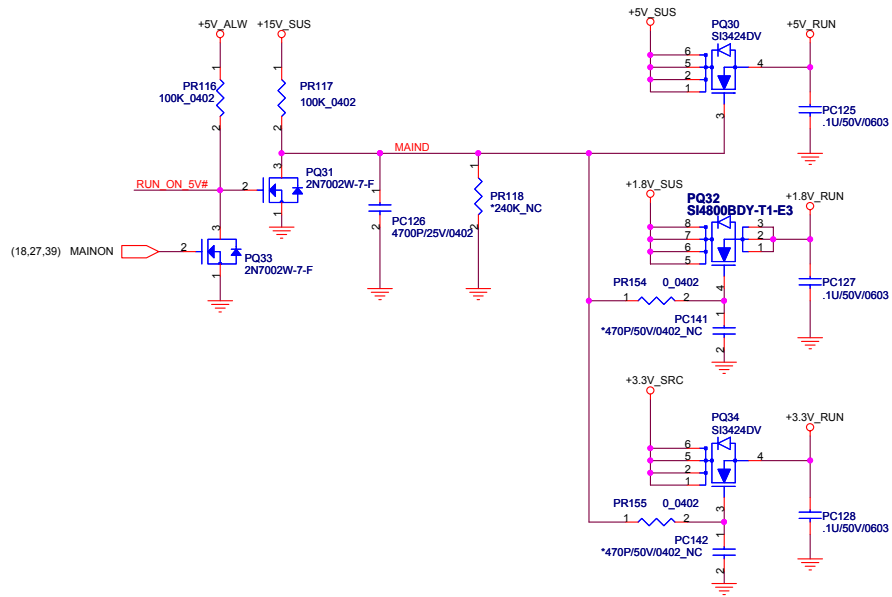


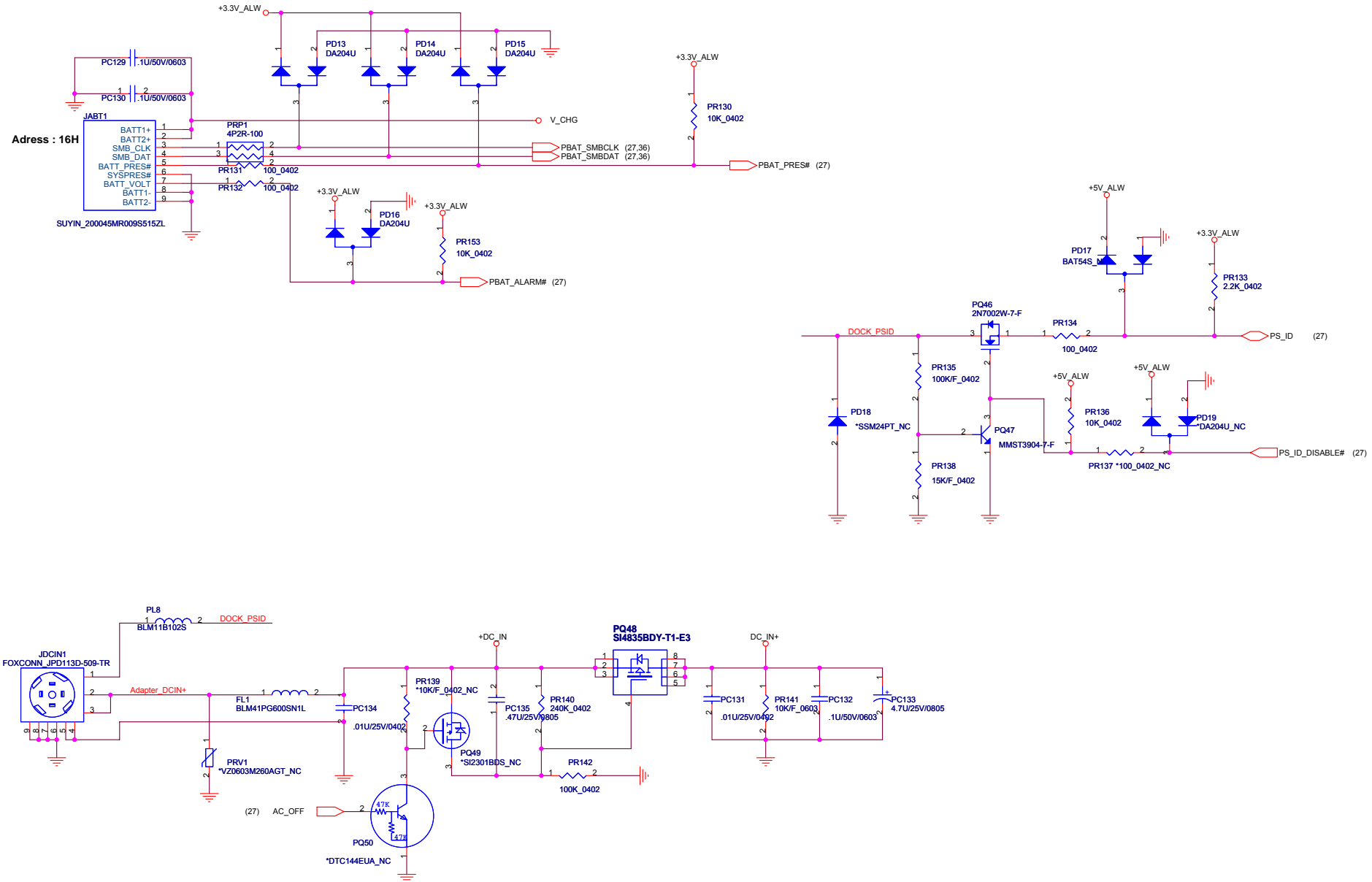


	D5	D4	D3	D2	D1	D0	Output		D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	0	1.5500V	1	0	0	0	0	0	0	0.7625V
0	0	0	0	0	0	1	1.5000V	1	0	0	0	0	0	1	0.7375V
0	0	0	0	0	1	0	1.4500V	1	0	0	0	0	1	0	0.7125V
0	0	0	0	0	1	1	1.4000V	1	0	0	0	0	1	1	0.7000V
0	0	0	0	1	0	0	1.3500V	1	0	0	0	1	0	0	0.6750V
0	0	0	0	1	1	1	1.3000V	1	0	0	1	0	1	0	0.6750V
0	0	0	1	0	0	0	1.2500V	1	0	1	0	0	0	0	0.6500V
0	0	0	1	0	1	0	1.2000V	1	0	1	0	0	1	0	0.6375V
0	0	0	1	0	1	1	1.1500V	1	0	1	0	1	0	0	0.6125V
0	0	1	0	0	0	0	1.1000V	1	0	1	0	1	1	0	0.5875V
0	0	1	0	0	0	1	1.0500V	1	0	1	0	1	1	1	0.5875V
0	0	1	0	0	1	0	1.0000V	1	0	0	0	0	0	0	0.5625V
0	0	1	0	0	1	1	1.1250V	1	0	0	0	0	1	0	0.5500V
0	0	1	0	1	0	0	1.1750V	1	0	0	0	0	1	1	0.5250V
0	0	1	0	1	0	1	1.0750V	1	0	0	0	1	0	1	0.5250V
0	0	1	0	1	1	0	1.0250V	1	0	0	1	0	0	0	0.5000V
0	0	1	0	1	1	1	1.0000V	1	0	0	1	0	1	0	0.4875V
0	0	1	1	0	0	0	0.9750V	1	0	0	1	0	1	1	0.4625V
0	0	1	1	0	0	1	0.9500V	1	0	0	1	0	1	1	0.4625V
0	0	1	1	0	1	0	0.9000V	1	0	1	0	0	0	0	0.4375V
0	0	1	1	0	1	1	0.8750V	1	0	1	0	0	1	0	0.4375V
0	0	1	1	1	0	0	0.8500V	1	0	1	0	1	0	0	0.4125V
0	0	1	1	1	0	1	0.8250V	1	0	1	1	0	1	0	0.4000V
0	0	1	1	1	1	0	0.8000V	1	0	1	1	0	1	1	0.4000V
0	1	1	1	1	1	1	0.7750V	1	0	1	1	1	1	1	0.3750V



[illegible]

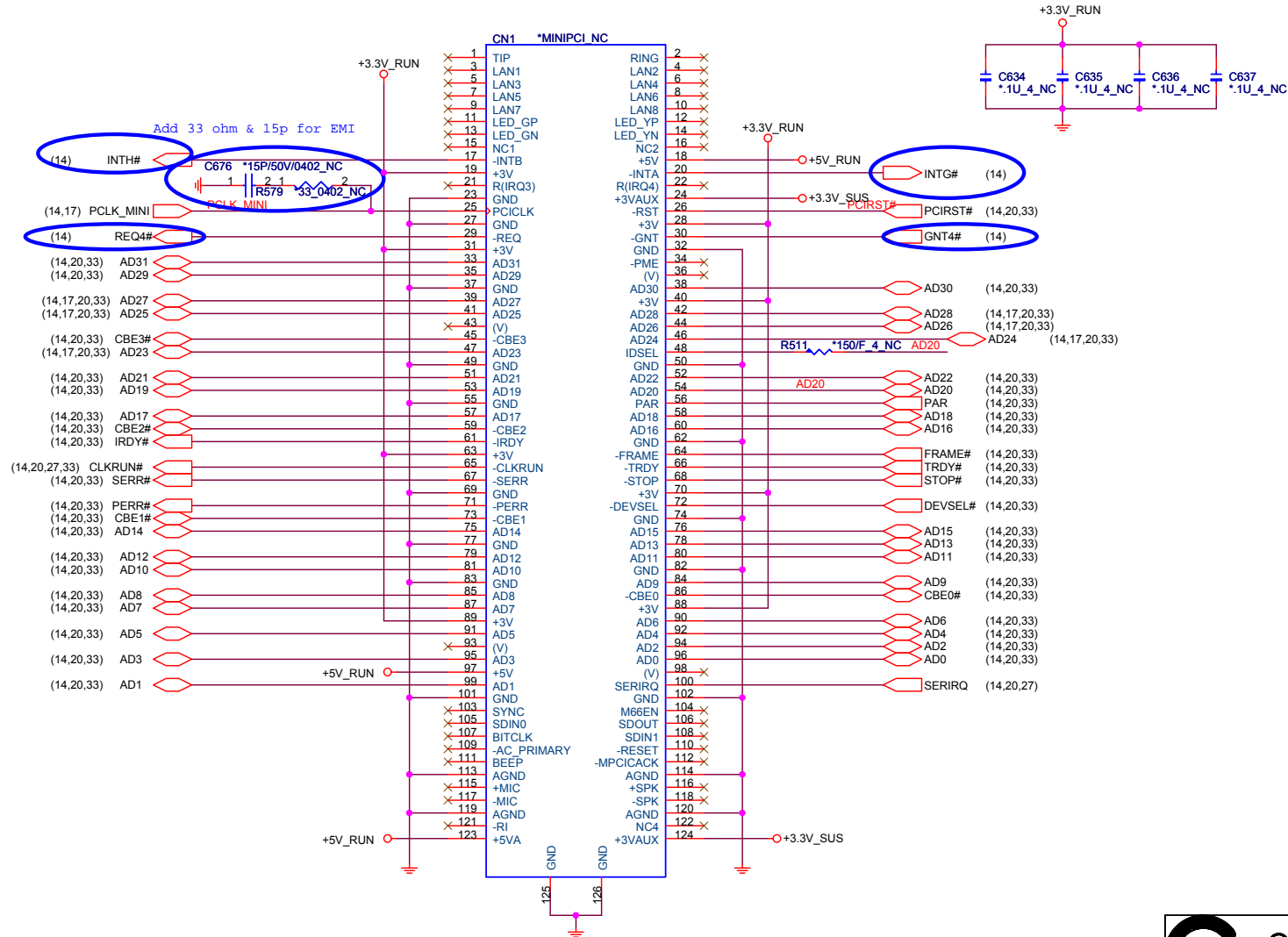




ID Select : AD20
Interrupt Pin : INTG# , INTH#
Request Indicate : REQ4#
Grant Indicate : GNT4#

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DEBUG PURPOSE ONLY



MPC



Title
MINI PCI(for debug)

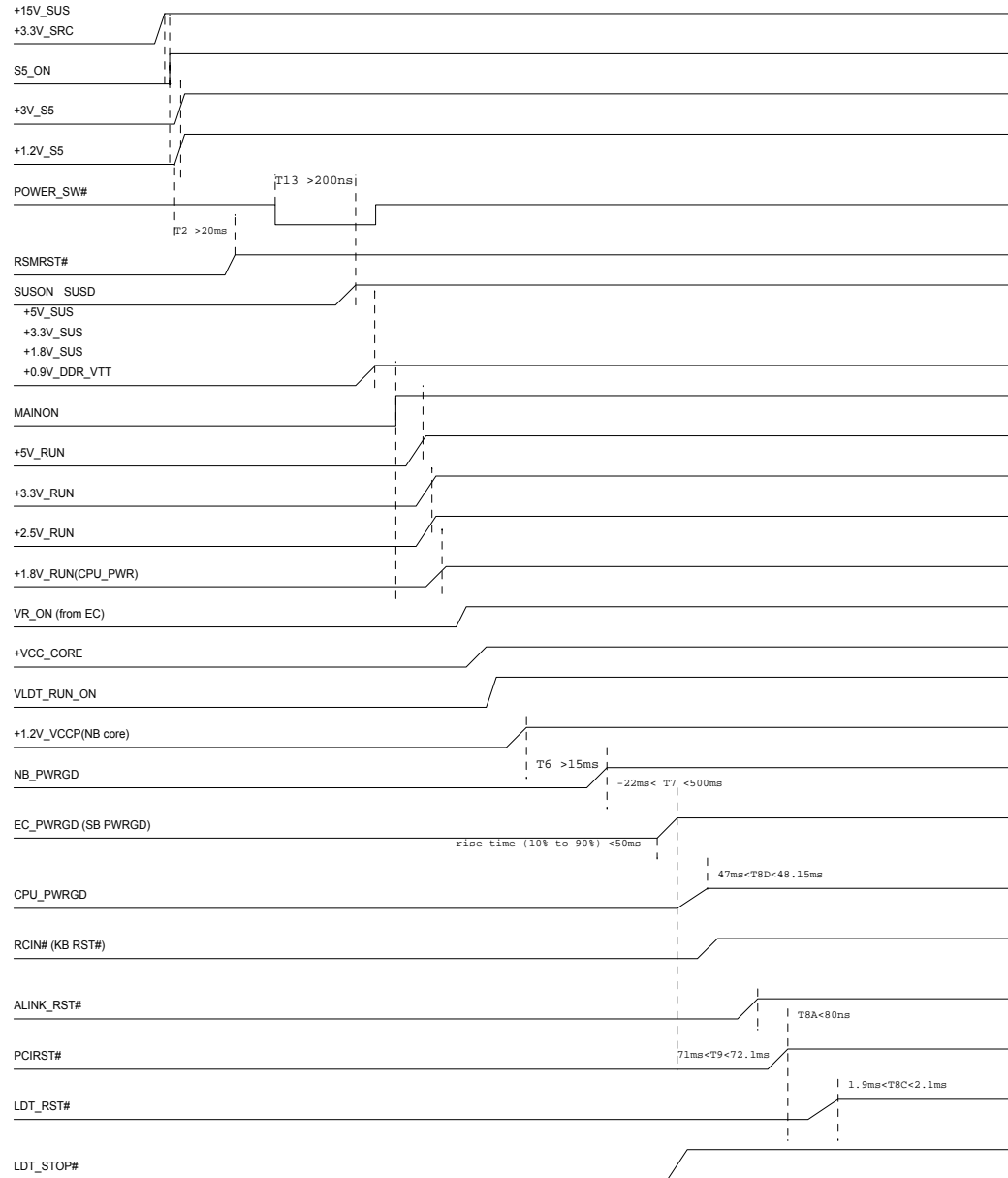
Size
Document Number
FX2

Rev
1A

Date: Friday, May 05, 2006

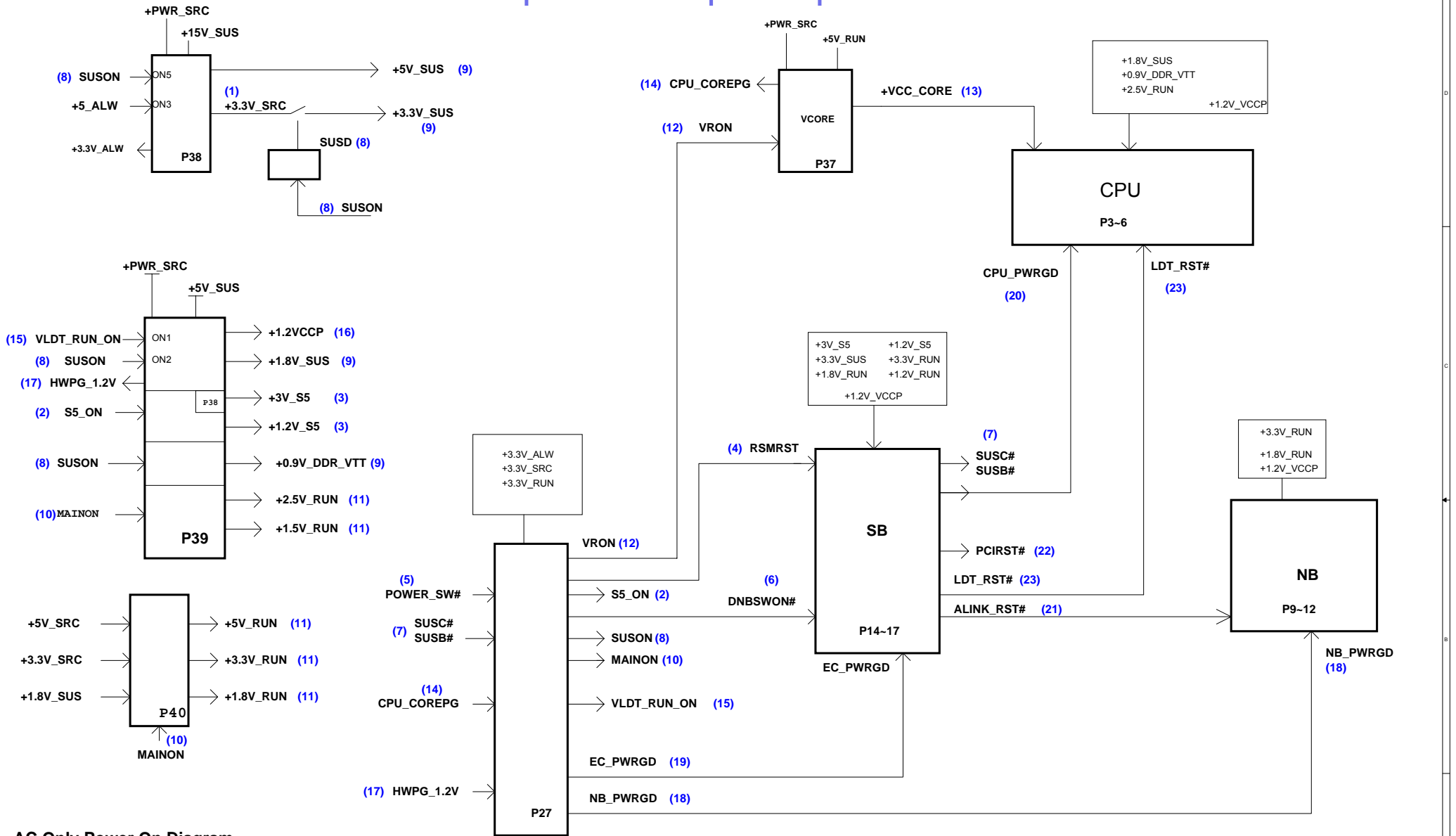
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Power On Sequence



T6: NB core voltage to NB_PWRGD
T7: NB_PWRGD to SB_PWRGD
T8D: SB_PWRGD to CPU_PWRGD

T8A: ALINK_RST# to PCIRST#
T9: SB_PWRGD to PCIRST#
T8C: PCIRST# to LDT_RST#



AC Only Power On Diagram

- | | | | |
|----------------------|-------------------------|------------------|-----------------|
| (1) +3.3V_SRC | (8) SUSON, SUSD | (13) +VCC_CORE | (20) CPU_PWRGD |
| (2) S5_ON | (9) +5V_SUS | (14) CPU_COREPG | (21) ALINK_RST# |
| (3) +3V_S5, +1.2V_S5 | (10) MAINON | (15) VLDT_RUN_ON | (22) PCI_RST# |
| (4) RSMRST | (11) +5V_RUN, +3.3V_RUN | (16) +1.2_VCCP | (23) LDT_RST# |
| (5) POWER_SW# | (12) VRON | (17) HWPG_1.2V | |
| (6) DNBSWON# | | (18) NB_PWRGD | |
| (7) SUSC#, SUBS# | | (19) EC_PWRGD | |

