

# Compal confidential

## Schematics Document

### Mobile Merom uFCPGA with Satna Rosa Platform

2007-07-24

REV: 0.3

|   |            |                    |            |                              |                             |
|---|------------|--------------------|------------|------------------------------|-----------------------------|
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ECB



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## Voltage Rails

| power plane<br>State           | +B | +5VALW<br>+3VALW | +1.8V | +5VS<br>+3VS<br>+1.5VS<br>+1.25VS<br>+0.9V<br>+VCCP<br>+CPU_CORE |
|--------------------------------|----|------------------|-------|--|
| S0                             | O  | O                | O     | O  |
| S1                             | O  | O                | O     | O  |
| S3                             | O  | O                | O     | X  |
| S5 S4/AC                       | O  | O                | X     | X  |
| S5 S4/ Battery only            | O  | X                | X     | X  |
| S5 S4/AC & Battery don't exist | X  | X                | X     | X  |

### Symbol Note :



: means Digital Ground



: means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

## I2C / SMBUS ADDRESSING

| DEVICE                 | HEX | ADDRESS         |
|------------------------|-----|-----------------|
| DDR SO-DIMM 0          | A0  | 1 0 1 0 0 0 0 0 |
| DDR SO-DIMM 1          | A4  | 1 0 1 0 0 1 0 0 |
| CLOCK GENERATOR (EXT.) | D2  | 1 1 0 1 0 0 1 0 |

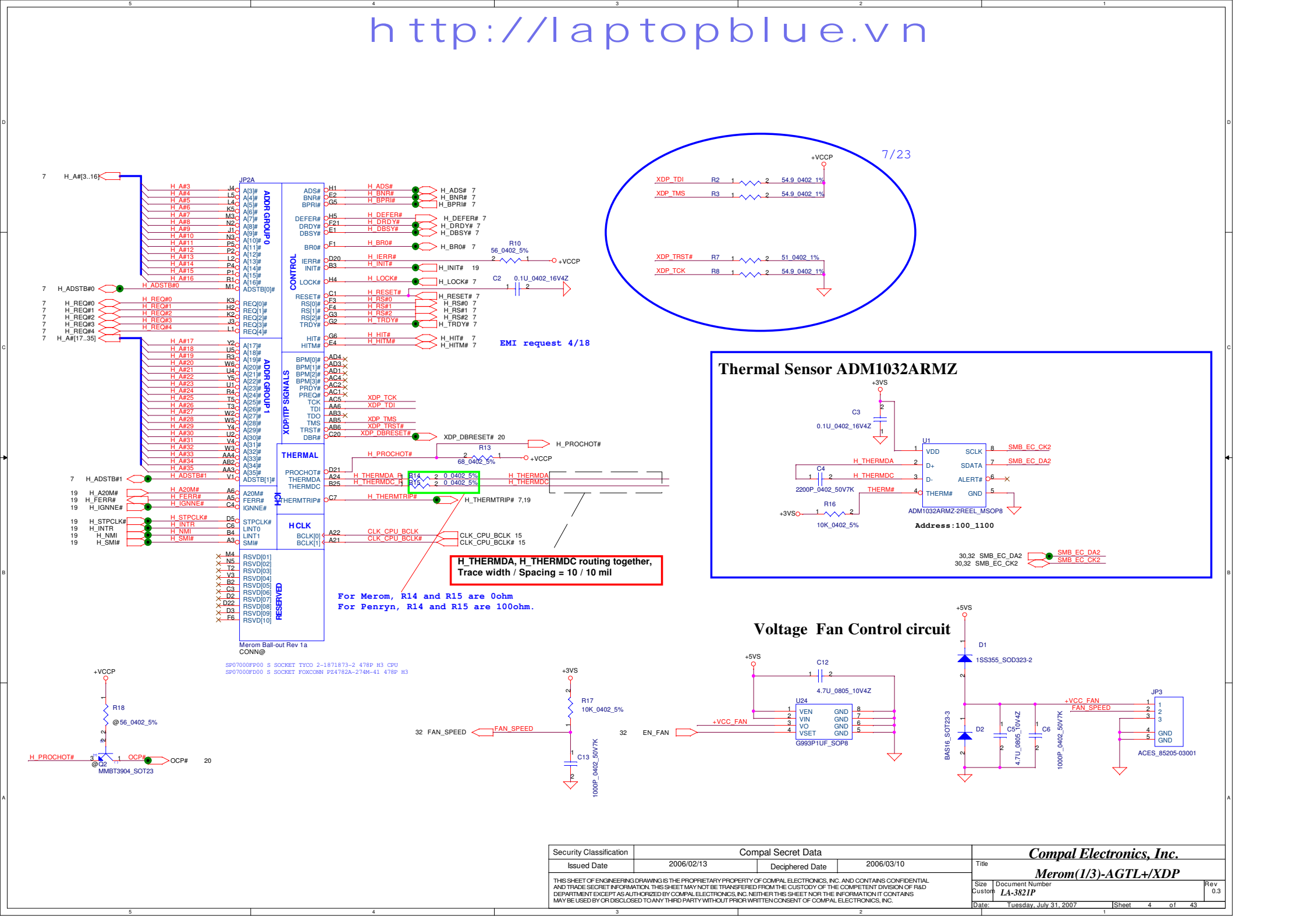
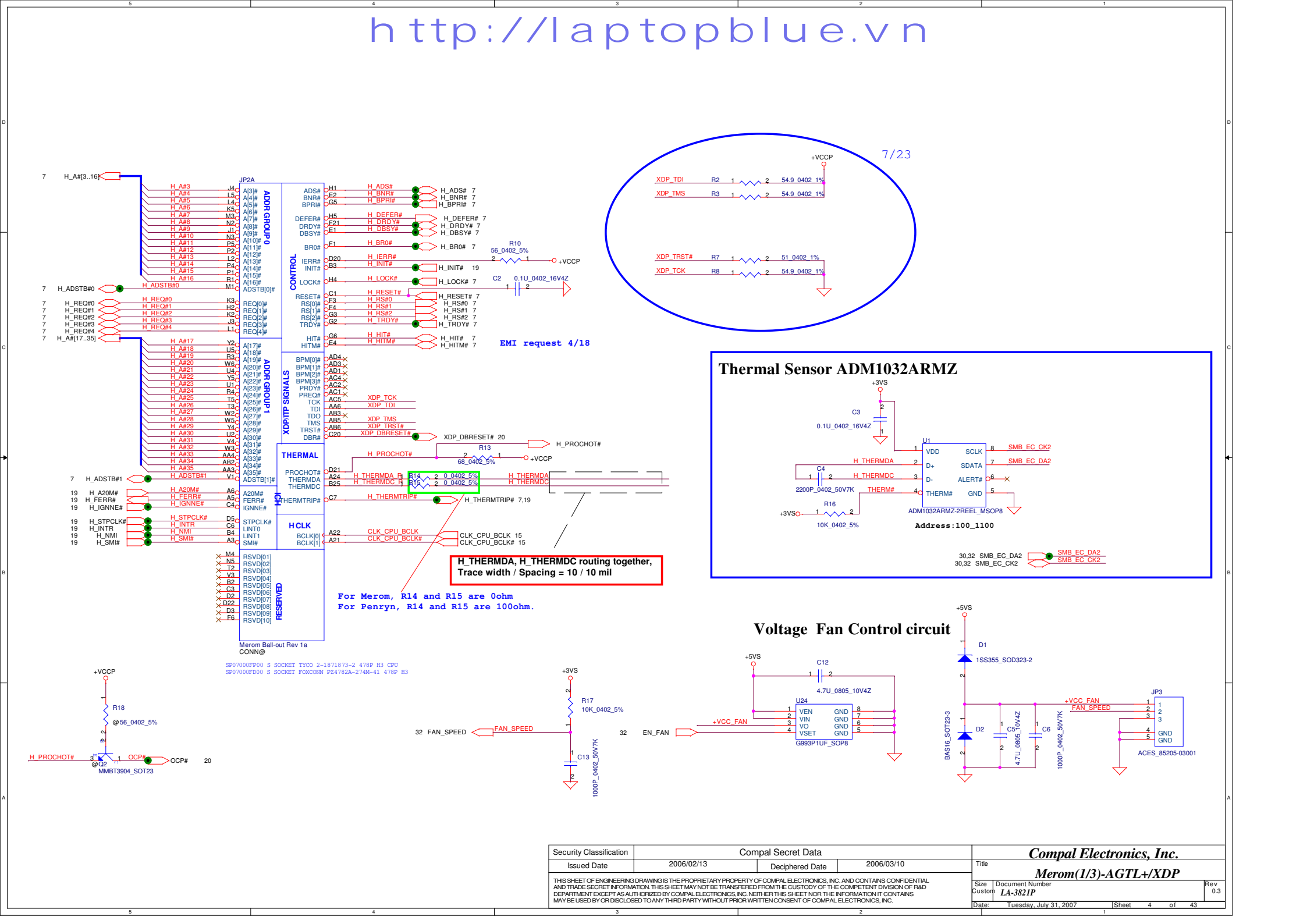
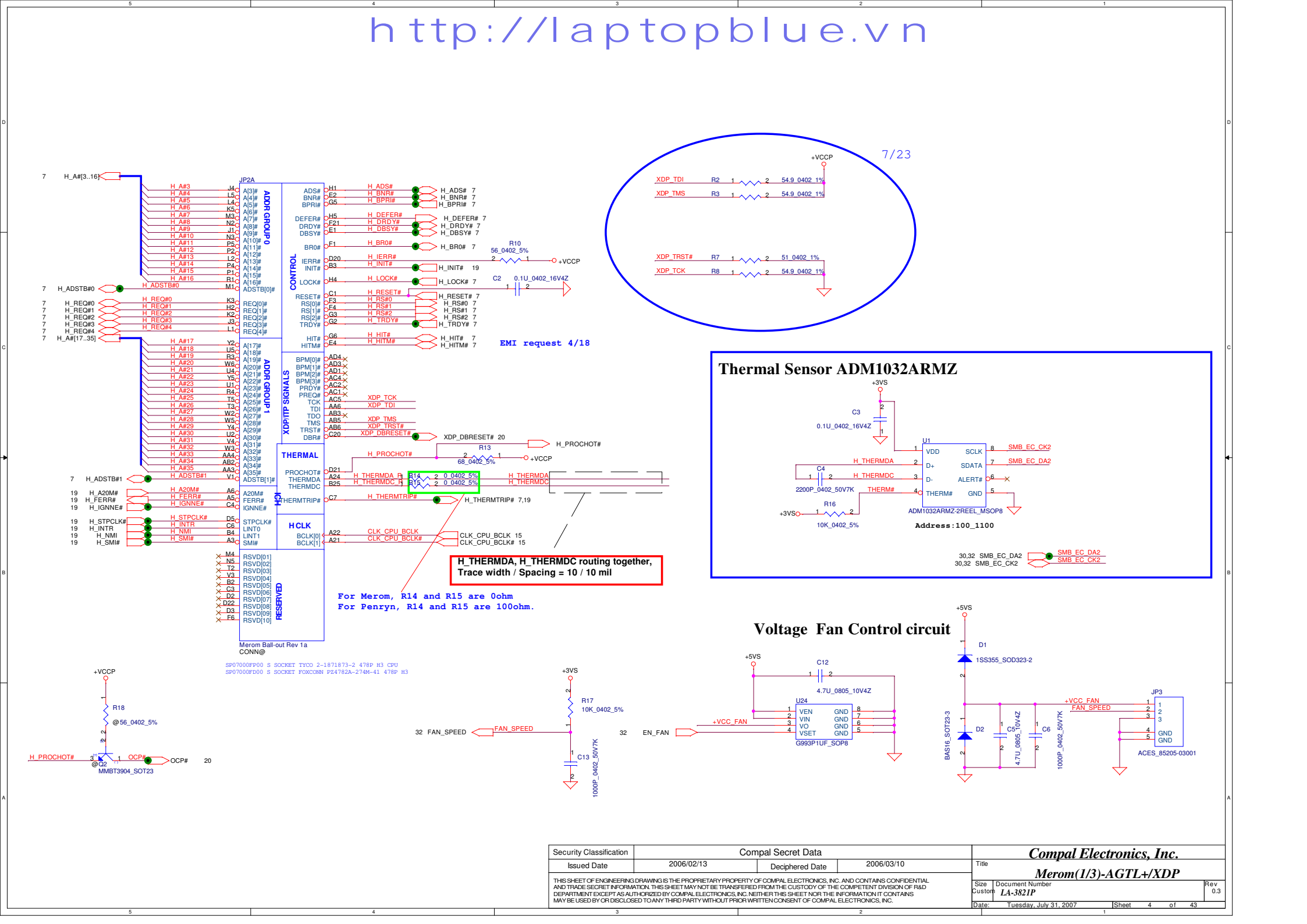
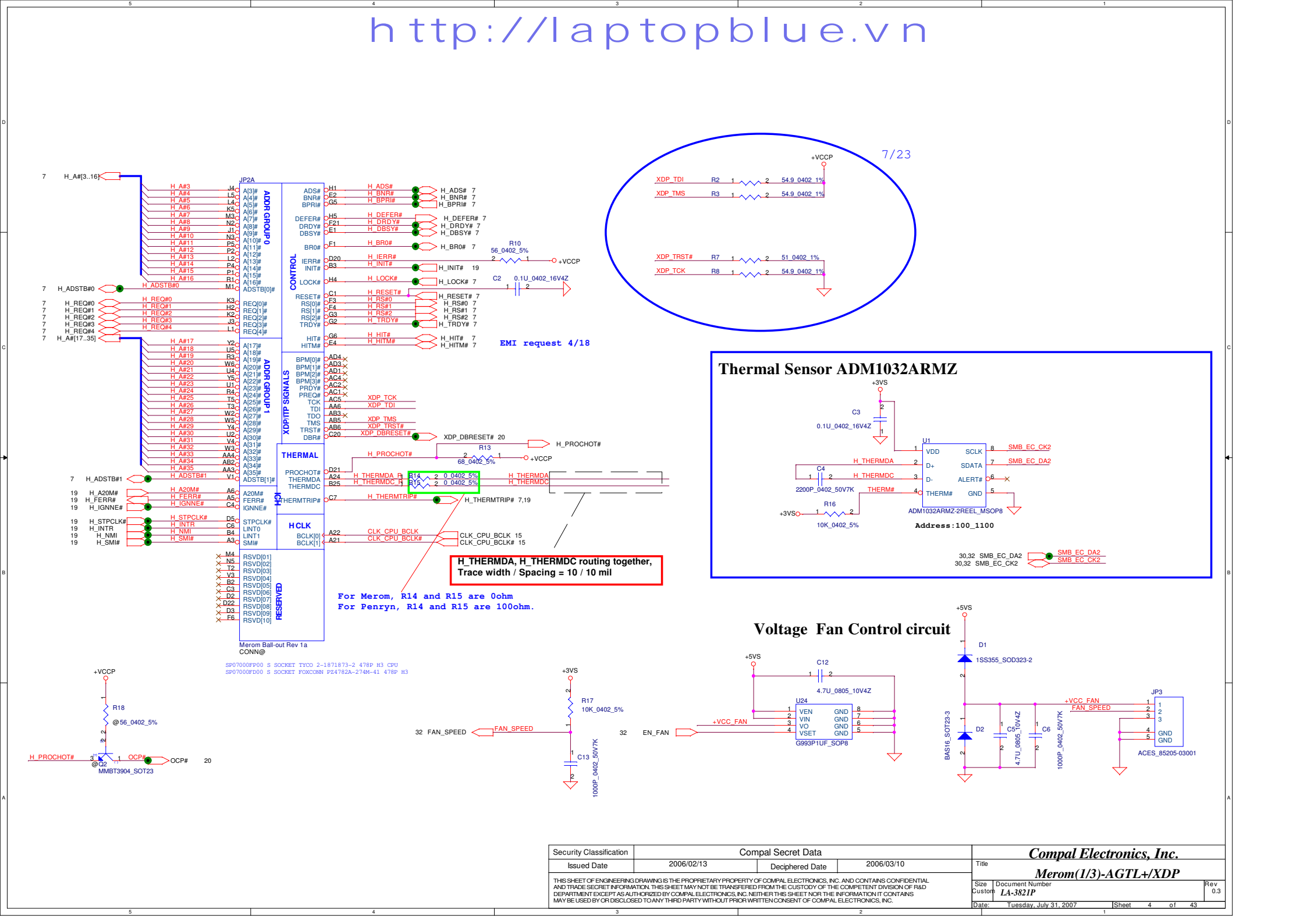
SMBUS Control Table

|                            | SOURCE    | INVERTER | BATT | SERIAL EEPROM | THERMAL SENSOR (CPU)<br>ADM1032 | SODIMM | CLK CHIP | MINI CARD | LCD |
|----------------------------|-----------|----------|------|---------------|---------------------------------|--------|----------|-----------|-----|
| SMB_EC_CK1<br>SMB_EC_DA1   | KB925     | X        | V    | V             | X                               | X      | X        | X         | X   |
| SMB_EC_CK2<br>SMB_EC_DA2   | KB925     | X        | X    | X             | V                               | X      | X        | X         | X   |
| SMB_CK_CLK1<br>SMB_CK_DAT1 | ICH8      | X        | X    | X             | X                               | V      | V        | V         | X   |
| LCD_CLK<br>LCD_DAT         | Crestline | X        | X    | X             | X                               | X      | X        | X         | V   |

**BOM: 43XXXXXX**

**Jump-Short: PJP?**

|   |                    |                 |            |                        |                 |
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# http://laptopblue.vn

The diagram illustrates the PCB layout for the Merom (1/3)-AGTL+/XDP system. It includes various signal and power connections, component footprints, and a detailed callout for the Thermal Sensor ADM1032ARMZ.

**Signal Connections:**

- ADDR GROUP 0:** H\_A# [3..16] to JP2A, H\_A#17 to H\_A#35 to JP2B.
- ADDR GROUP 1:** H\_A#17 to H\_A#35 to JP2B.
- CONTROL:** H\_ADSTB#0 to H\_ADSTB#1, H\_REQ#0 to H\_REQ#4, H\_ADSTB#1 to H\_ADSTB#1, H\_A20M# to H\_A20M#, H\_FERR# to H\_FERR#, H\_IGNNE# to H\_IGNNE#, H\_STPCLK# to H\_STPCLK#, H\_INTR# to H\_INTR#, H\_NMI# to H\_NMI#, H\_SMI# to H\_SMI#.
- STATUS/IO/DP/DP:** H\_A#17 to H\_A#35 to JP2B.
- THERMAL:** H\_PROCHOT# to H\_PROCHOT#, H\_THERMDA# to H\_THERMDA#, H\_THERMDC# to H\_THERMDC#, H\_THERMTRIP# to H\_THERMTRIP#.
- HCLK:** CLK\_CPU\_BCLK# to CLK\_CPU\_BCLK#.
- RESERVED:** RSVD[0] to RSVD[10].

**Power Connections:**

- +VCCP:** R18, R10, R2, R3, R7, R8, R16, R17, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100.
- +VCC:** R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100.
- +VCC\_FAN:** R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100.

**Thermal Sensor ADM1032ARMZ:**

The Thermal Sensor ADM1032ARMZ is shown with its pin connections and component values. The sensor is connected to the +3VS and +VCC\_FAN pins. The sensor's output is connected to the H\_THERMDA and H\_THERMDC pins. The sensor's address is 100\_1100.

**Voltage Fan Control circuit:**

The Voltage Fan Control circuit is shown with its pin connections and component values. The circuit is connected to the +3VS and +VCC\_FAN pins. The circuit's output is connected to the FAN\_SPEED pin.

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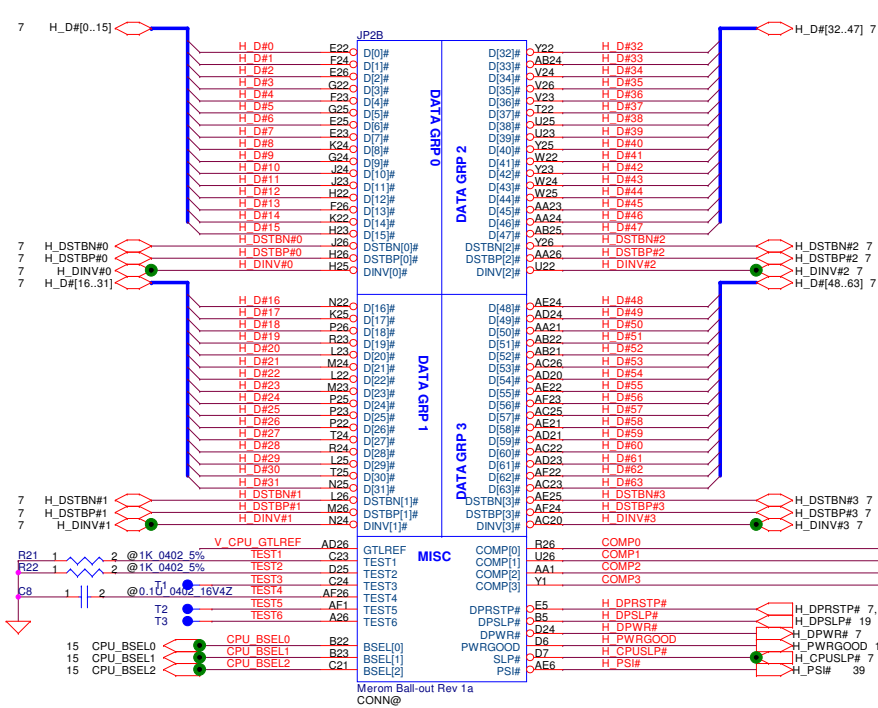
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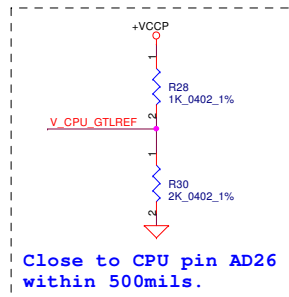
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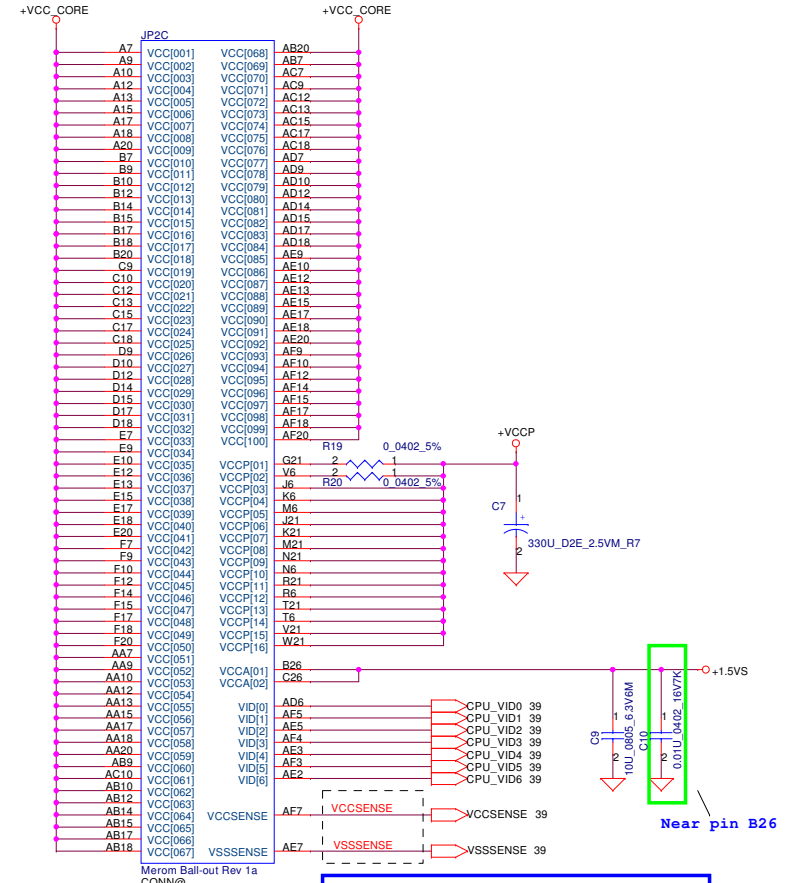


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

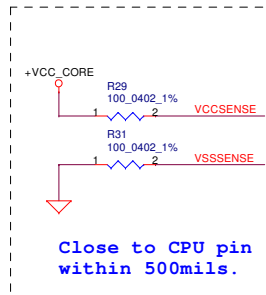
| CPU_BSEL | CPU_BSEL2 | CPU_BSEL1 | CPU_BSEL0 |
|----------|-----------|-----------|-----------|
| 166      | 0         | 1         | 1         |
| 200      | 0         | 1         | 0         |



Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



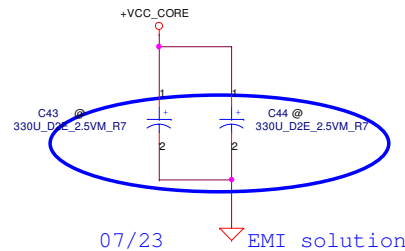
Length match within 25 mils. The trace width/space/other is 20/7/25.



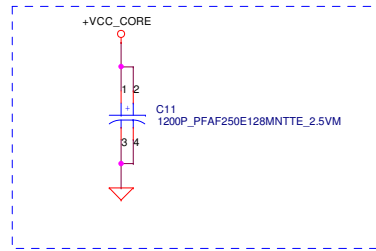
| JP20 |          |      |
|------|----------|------|
| A4   | VSS[001] | P6   |
| A8   | VSS[002] | P21  |
| A11  | VSS[003] | P24  |
| A14  | VSS[004] | R2   |
| A16  | VSS[005] | R5   |
| A19  | VSS[006] | R22  |
| A23  | VSS[007] | R25  |
| AF2  | VSS[008] | T1   |
| B6   | VSS[009] | T4   |
| B8   | VSS[010] | T23  |
| B11  | VSS[011] | T26  |
| B13  | VSS[012] | U3   |
| B16  | VSS[013] | U6   |
| B19  | VSS[014] | U21  |
| B21  | VSS[015] | U24  |
| B24  | VSS[016] | V2   |
| C5   | VSS[017] | V5   |
| C8   | VSS[018] | V22  |
| C11  | VSS[019] | V25  |
| C14  | VSS[020] | W1   |
| C16  | VSS[021] | W4   |
| C19  | VSS[022] | W23  |
| C2   | VSS[023] | W26  |
| C22  | VSS[024] | Y3   |
| C25  | VSS[025] | Y6   |
| D1   | VSS[026] | Y21  |
| D4   | VSS[027] | Y24  |
| D8   | VSS[028] | AA2  |
| D13  | VSS[029] | AA5  |
| D16  | VSS[030] | AA11 |
| D19  | VSS[031] | AA12 |
| D23  | VSS[032] | AA14 |
| D26  | VSS[033] | AA16 |
| E3   | VSS[034] | AA19 |
| E6   | VSS[035] | AA22 |
| E8   | VSS[036] | AA25 |
| E11  | VSS[037] | AB1  |
| E14  | VSS[038] | AB4  |
| E16  | VSS[039] | AB8  |
| E19  | VSS[040] | AB11 |
| E21  | VSS[041] | AB13 |
| E24  | VSS[042] | AB16 |
| F5   | VSS[043] | AB23 |
| F8   | VSS[044] | AB26 |
| F11  | VSS[045] | AC3  |
| F13  | VSS[046] | AC6  |
| F16  | VSS[047] | AC8  |
| F19  | VSS[048] | AC11 |
| F2   | VSS[049] | AC14 |
| F22  | VSS[050] | AC16 |
| F25  | VSS[051] | AC19 |
| G4   | VSS[052] | AC21 |
| G1   | VSS[053] | AC24 |
| G23  | VSS[054] | AD2  |
| G26  | VSS[055] | AD5  |
| H3   | VSS[056] | AD8  |
| H6   | VSS[057] | AD11 |
| H21  | VSS[058] | AD13 |
| H24  | VSS[059] | AD16 |
| J2   | VSS[060] | AD19 |
| J5   | VSS[061] | AD22 |
| J22  | VSS[062] | AD25 |
| J25  | VSS[063] | AE1  |
| K1   | VSS[064] | AE4  |
| K4   | VSS[065] | AE8  |
| K23  | VSS[066] | AE11 |
| K26  | VSS[067] | AE14 |
| L3   | VSS[068] | AE16 |
| L6   | VSS[069] | AE19 |
| L21  | VSS[070] | AE23 |
| L24  | VSS[071] | AE26 |
| M2   | VSS[072] | A2   |
| M5   | VSS[073] | AF6  |
| M22  | VSS[074] | AF8  |
| M25  | VSS[075] | AF11 |
| N1   | VSS[076] | AF13 |
| N4   | VSS[077] | AF16 |
| N23  | VSS[078] | AF19 |
| N26  | VSS[079] | AF21 |
| P3   | VSS[080] | A25  |
|      | VSS[081] | AF25 |
|      | VSS[163] |      |

Merom Ball-out Rev 1a

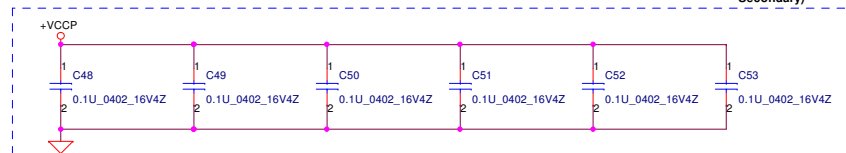
### Near CPU CORE regulator



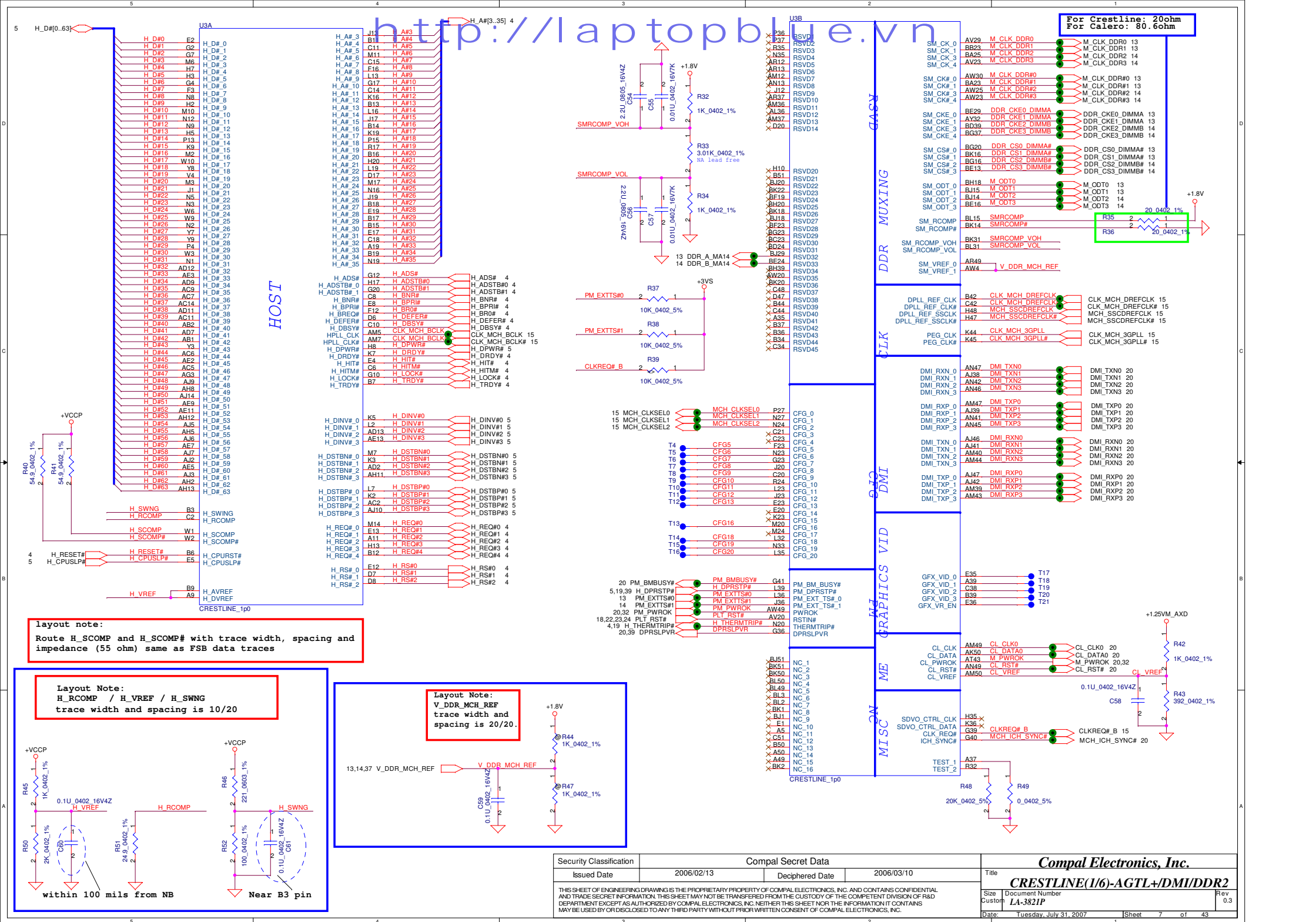
### Proadlizer



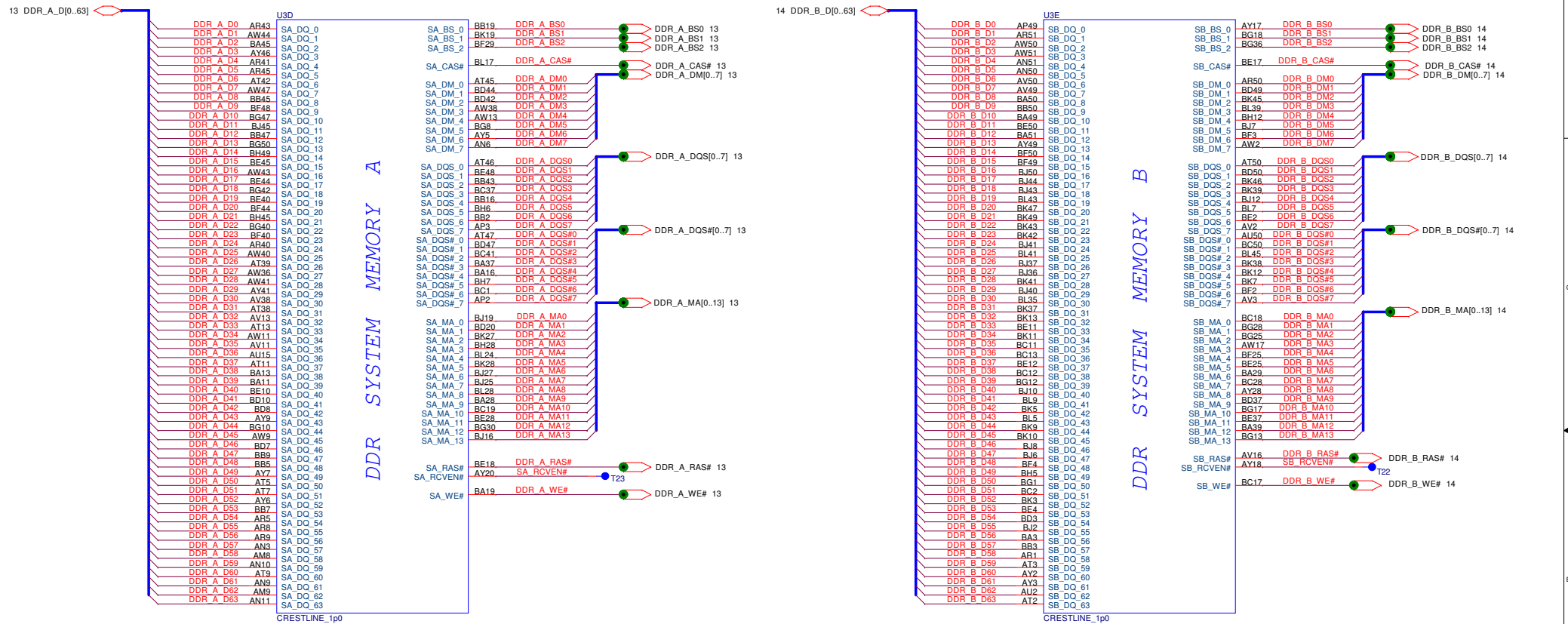
Place these inside  
socket cavity on L8  
(North side  
Secondary)



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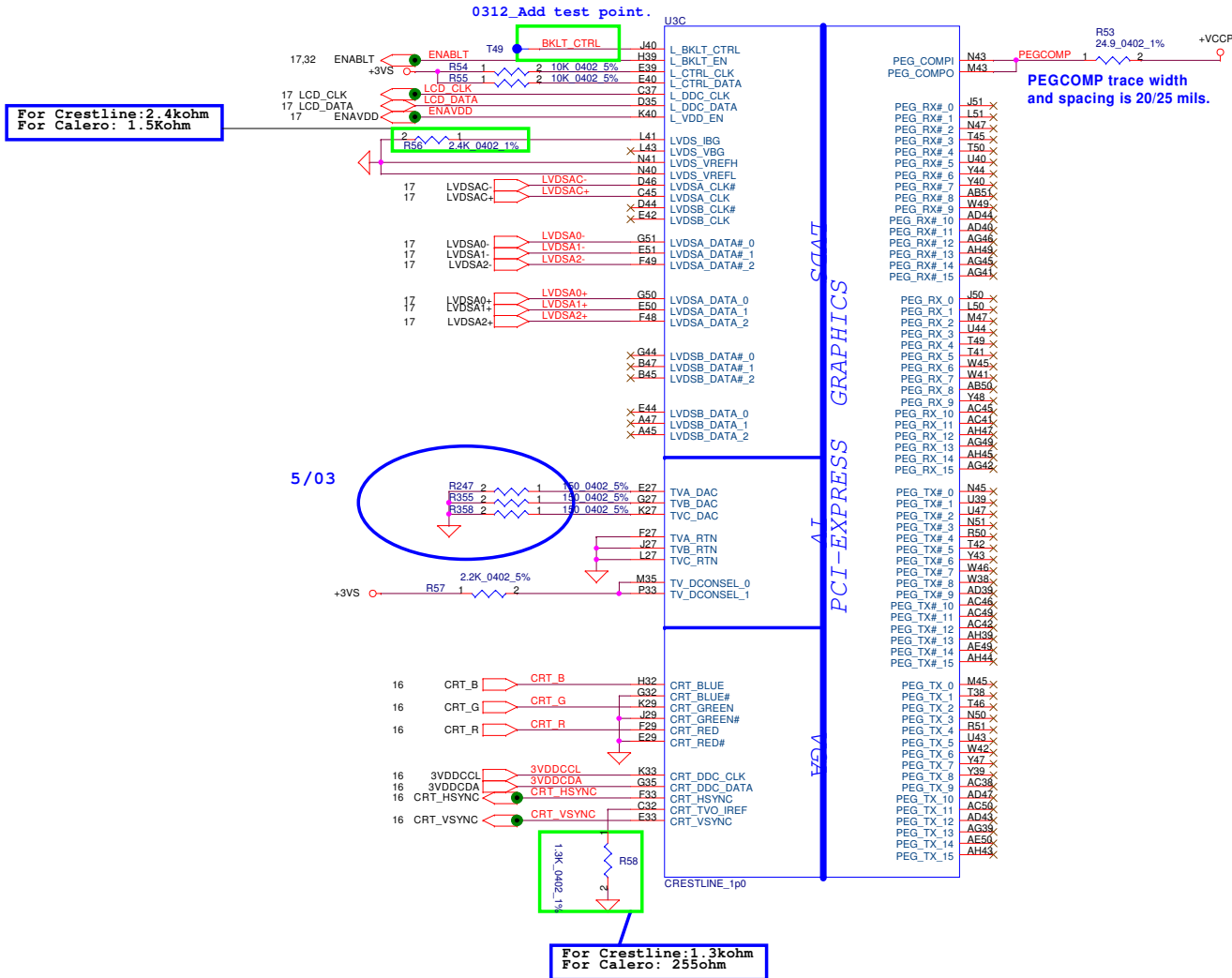






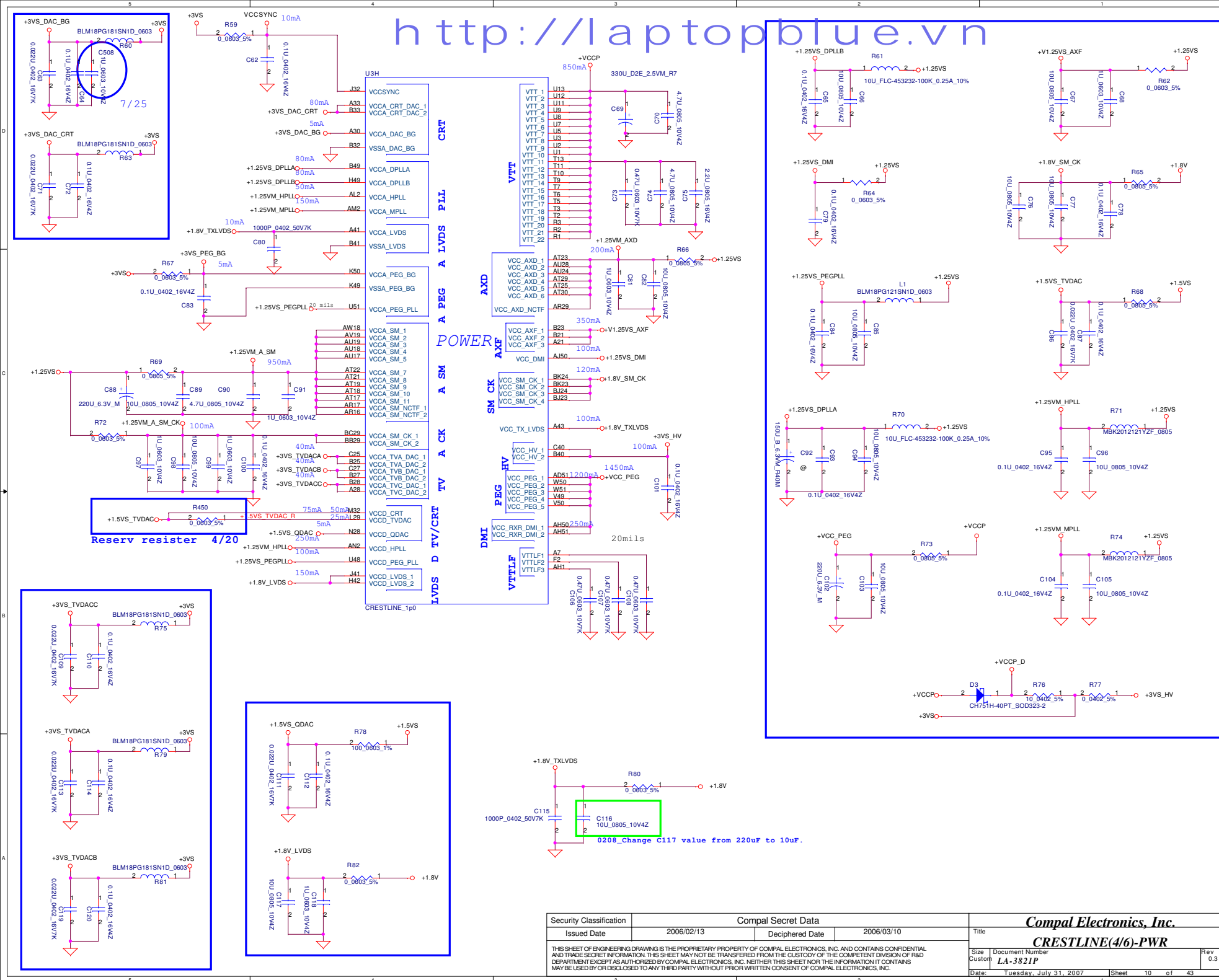
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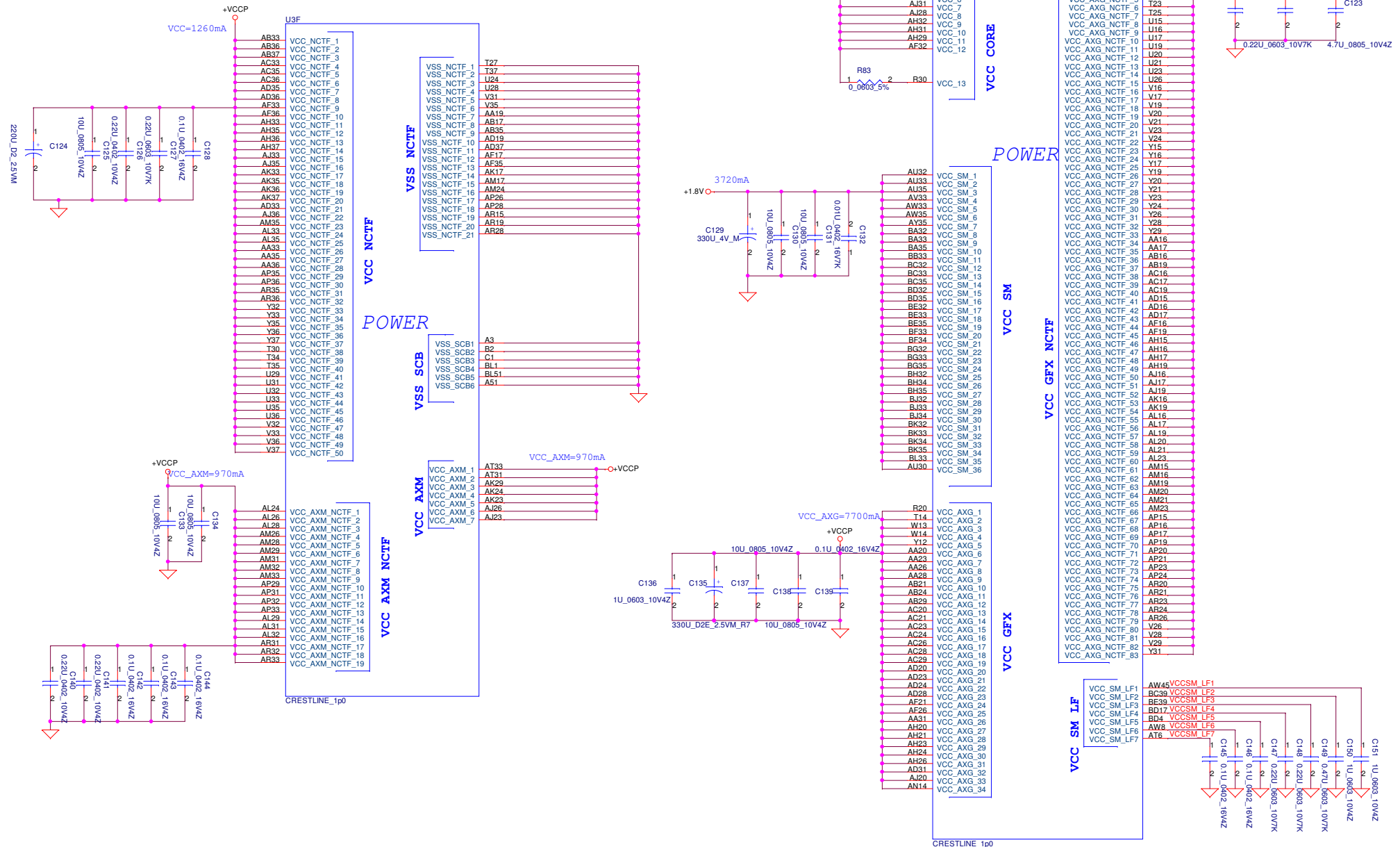


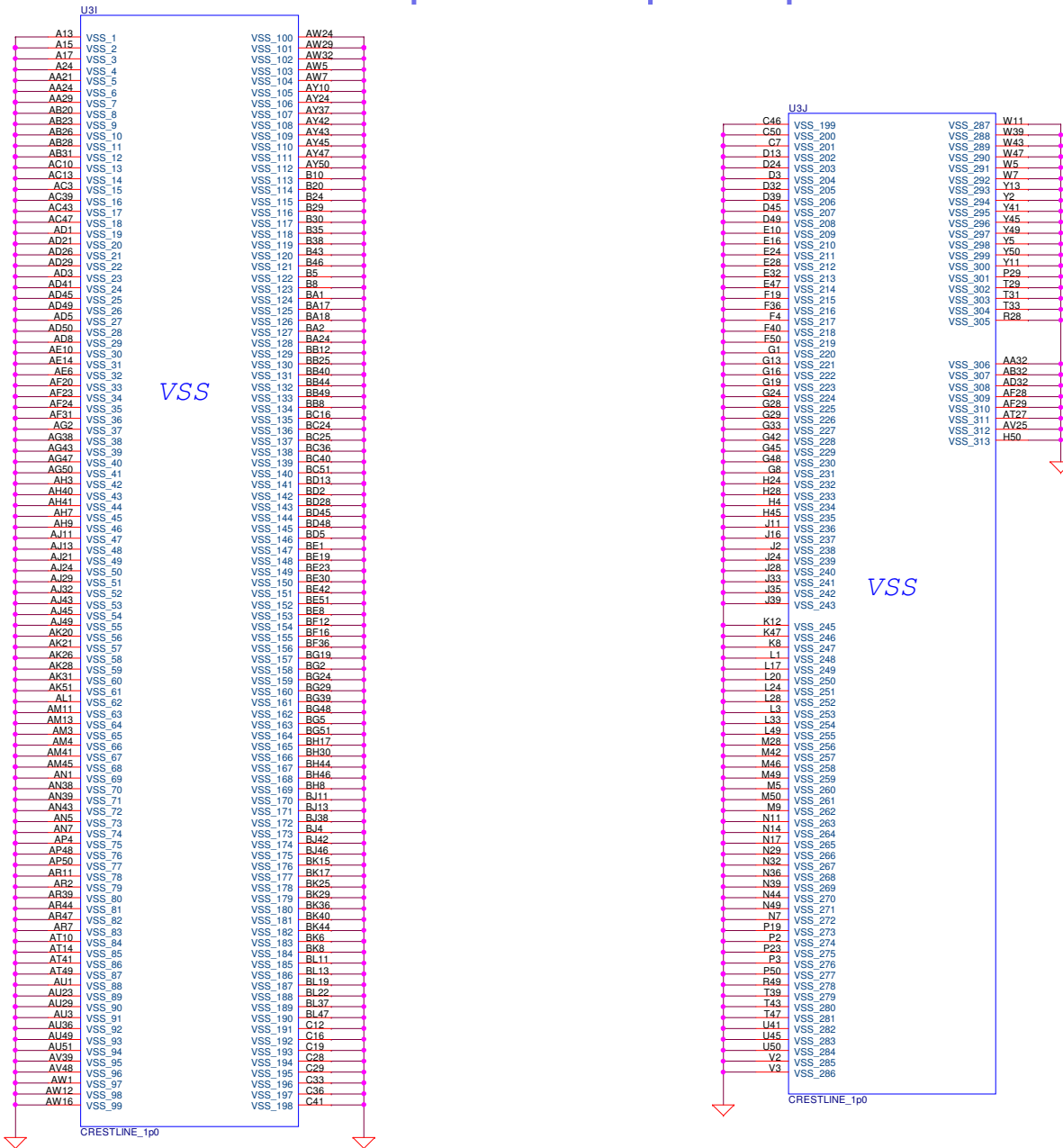
|                                    |   |
|------------------------------------|---|
| CFG[2:0] FSB Freq select           | 010 = FSB 800MHz<br>011 = FSB 667MHz<br>Others = Reserved   |
| CFG5 (DMI select)                  | 0 = DMI x 2<br>1 = DMI x 4 *  |
| CFG6                               | Reserved  |
| CFG7 (CPU Strap)                   | 0 = Reserved<br>1 = Mobile CPU *  |
| CFG8 (Low power PCIE)              | 0 = Normal mode<br>1 = Low Power mode *   |
| CFG9 (PCIE Graphics Lane Reversal) | 0 = Reverse Lane<br>1 = Normal Operation *  |
| CFG[11:10]                         | Reserved  |
| CFG[13:12] (XOR/ALLZ)              | 00 = Reserved<br>01 = XOR Mode Enabled<br>10 = All Z Mode Enabled<br>11 = Normal Operation(Default) * |
| CFG[15:14]                         | Reserved  |
| CFG16 (FSB Dynamic ODT)            | 0 = Disabled<br>1 = Enabled *   |
| CFG[18:17]                         | Reserved  |
| SDVO_CTRLDATA                      | 0 = No SDVO Device Present *<br>1 = SDVO Device Present   |
| CFG19 (DMI Lane Reversal)          | 0 = Normal Operation (Lane number in Order) *<br>1 = Reverse Lane                                     |
| CFG20 (PCIE/SDVO concurrent)       | 0 = Only PCIE or SDVO is operational. *<br>1 = PCIE/SDVO are operating simu.                          |

CFG[17:3] have internal pull up  
CFG[19:18] have internal pull down

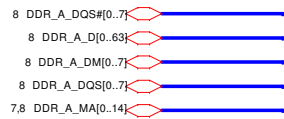


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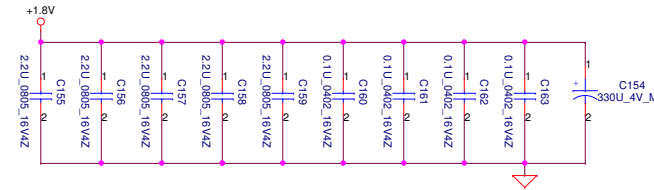




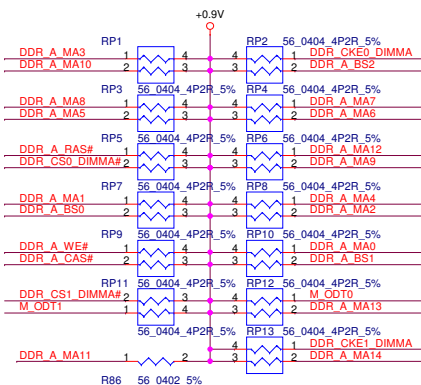
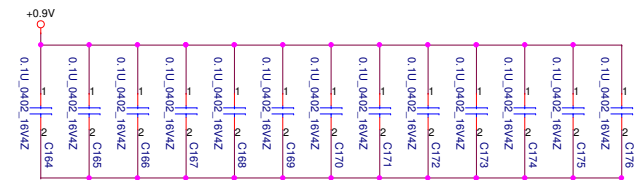
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|   |            |                    |            | Date: Tuesday, July 31, 2007 | Rev<br>0.3                  |
|   |            |                    |            | Sheet 12 of 43               |                             |



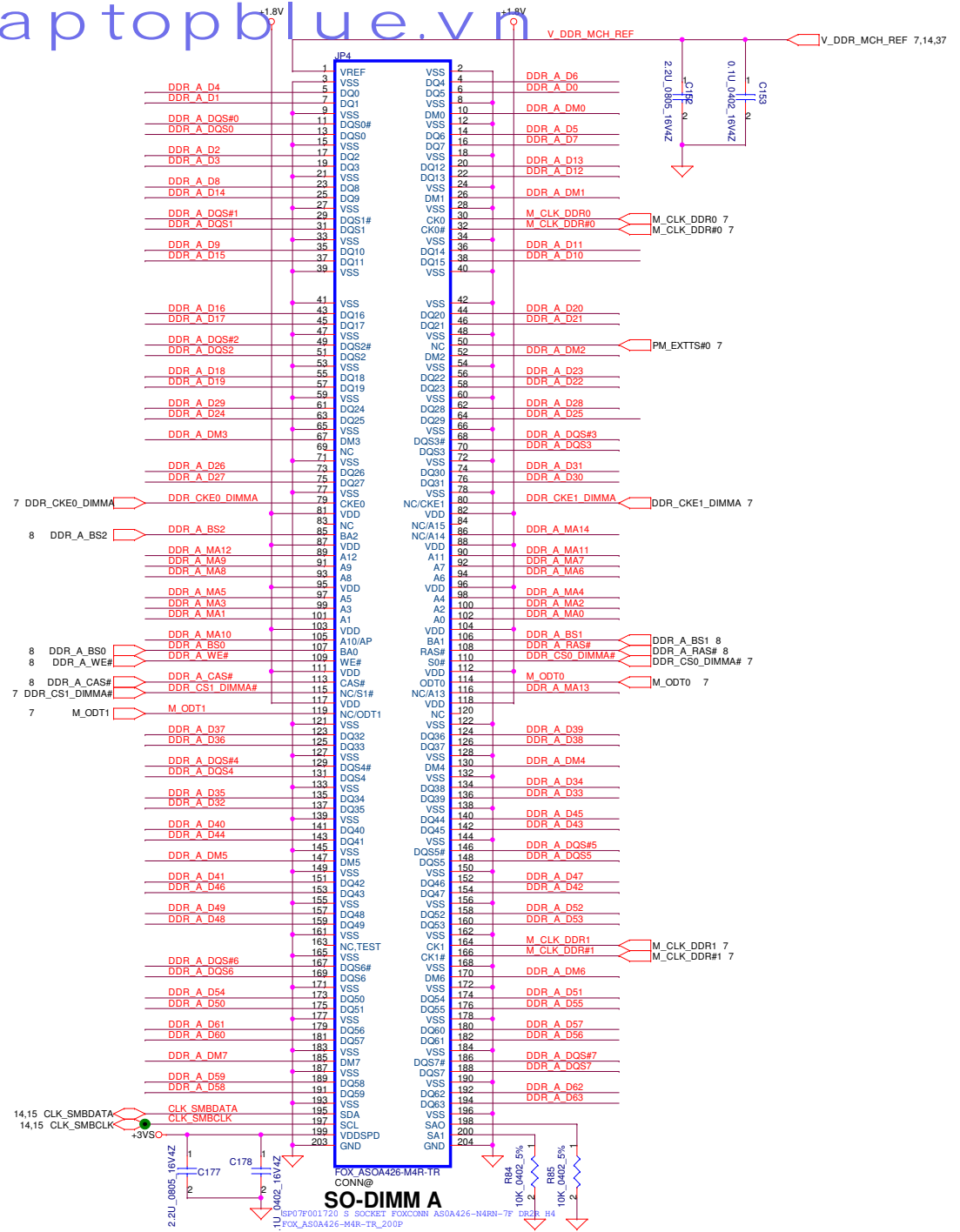
**Layout Note:**  
Place near JP34



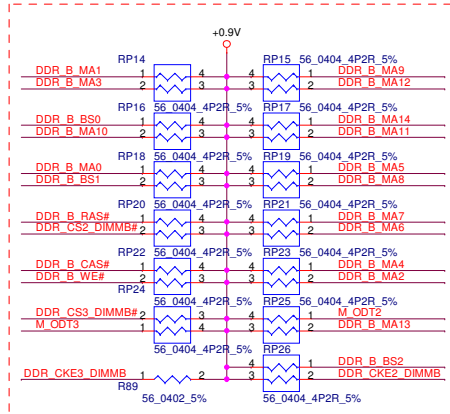
**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



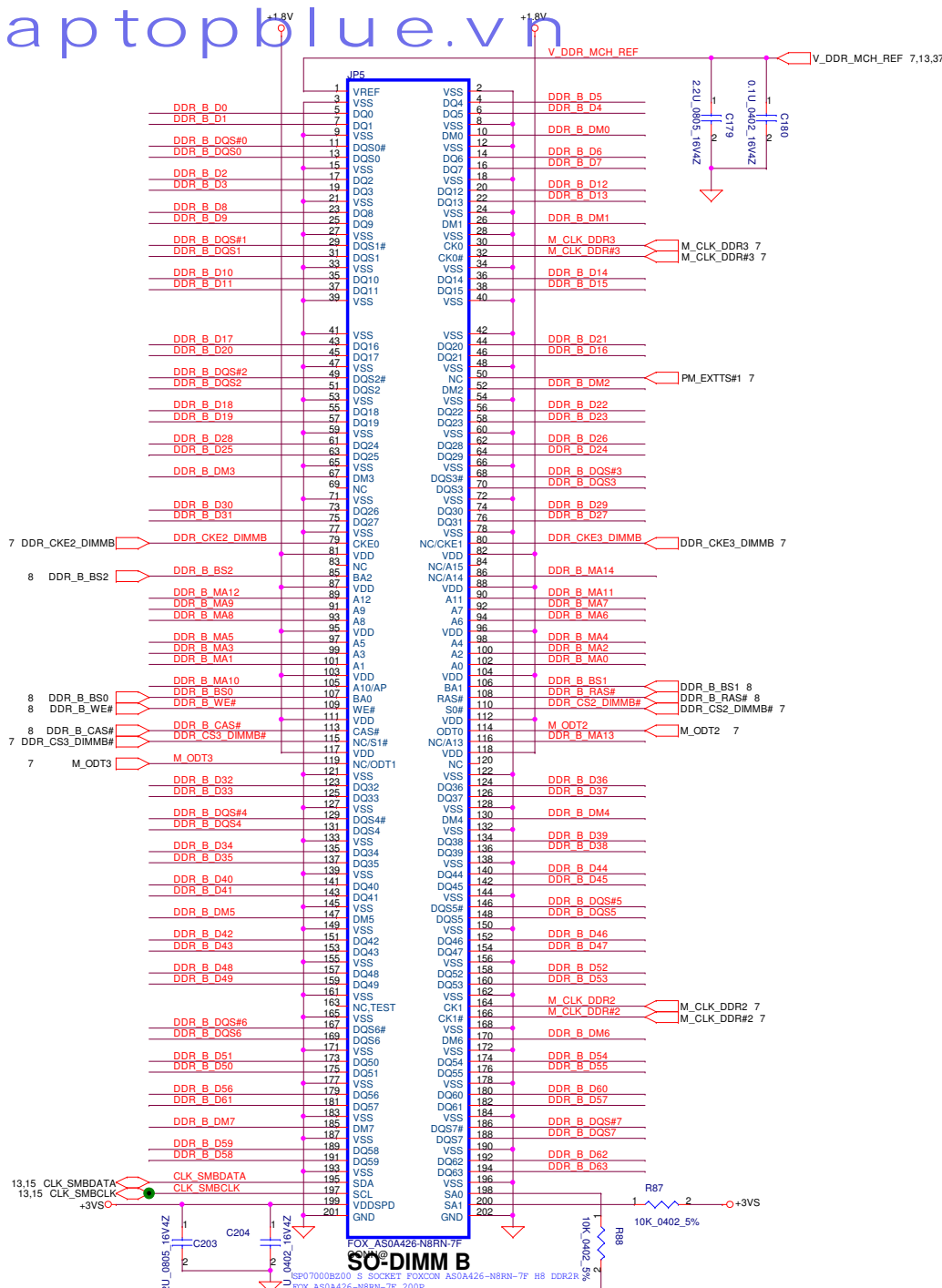
**Layout Note:**  
Place these resistor closely JP34, all trace length Max=1.5"



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|---|------------|--------------------|------------|--------------------------|------------------------|
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|   |            |                    |            | DDRII-SODIMM SLOT1       |                        |
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|   |            |                    |            | Date                     | Tuesday, July 31, 2007 |
|   |            |                    |            | Sheet                    | 13 of 43               |



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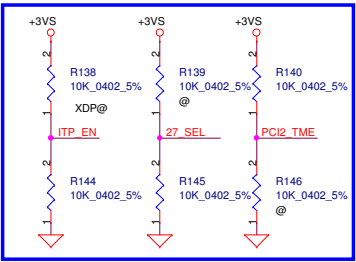
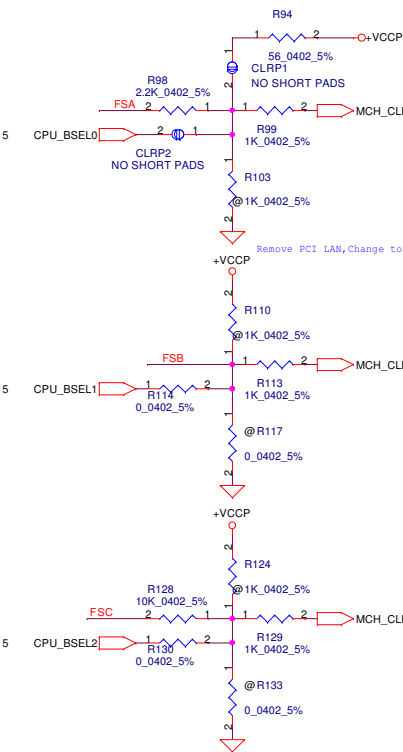
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| Security Classification  | Compal Secret Data |                 |            | <b>Compal Electronics, Inc.</b><br><b>DDRII-SODIMM SLOT2</b> |                        |                |
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|  |                    |                 |            |  | LA-3821P               | 0.3            |
|  |                    |                 |            | Date:  | Tuesday, July 31, 2007 | Sheet 14 of 43 |



| FSLC<br>CLKSEL2 | FSLB<br>CLKSEL1 | FSLA<br>CLKSEL0 | CPU<br>MHz | SRC<br>MHz | PCI<br>MHz |
|-----------------|-----------------|-----------------|------------|------------|------------|
| 0               | 0               | 1               | 133        | 100        | 33.3       |
| 0               | 1               | 0               | 200        | 100        | 33.3       |
| 0               | 1               | 1               | 166        | 100        | 33.3       |

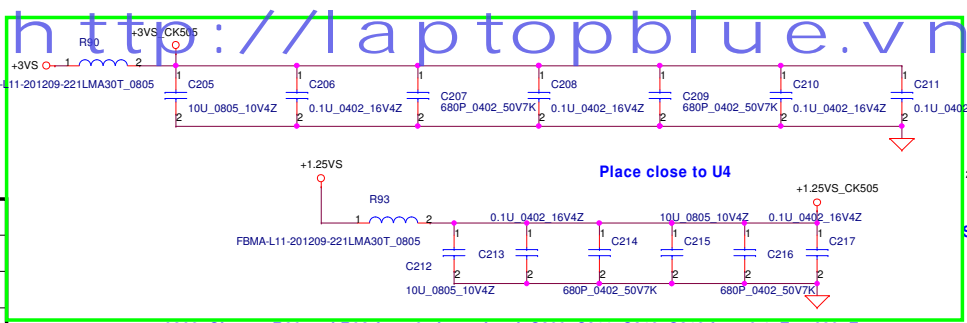
FSB Frequency Selet:

| CPU Driven | Stuff    | R1107 | R1135 | R1083 |
|------------|----------|-------|-------|-------|
| ★(Default) | No Stuff | R1074 | R1086 | R1098 |
|            |          | R1113 | R1128 | R1139 |
|            | Stuff    | R1086 | R1139 | R1135 |
|            |          | R1083 | R1107 | R1128 |
|            |          | R1113 | R1098 |       |
| 667MHz     | No Stuff |       |       |       |
|            | Stuff    | R1135 | R1139 |       |
|            |          | R1083 | R1086 | R1098 |
|            |          | R1074 | R1107 | R1113 |
| 800MHz     | No Stuff |       |       |       |
|            | Stuff    | R1135 | R1139 |       |
|            |          | R1083 | R1086 | R1098 |
|            |          | R1074 | R1107 | R1113 |



For ITP\_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#  
For 27\_SEL, 0 = Enable DOT96 & SRC1,  
1 = Enable SRC0 & 27MHz  
For PCI2\_EN, 0 = Overclocking of CPU and SRC Allowed  
1 = Overclocking of CPU and SRC NOT allowed

For Layout request:  
1. Change MINI\_CLKREQ# from pin 32 to pin 43.  
2. Change CLK\_PCIE\_MCARD from SRC9 to SRC6.

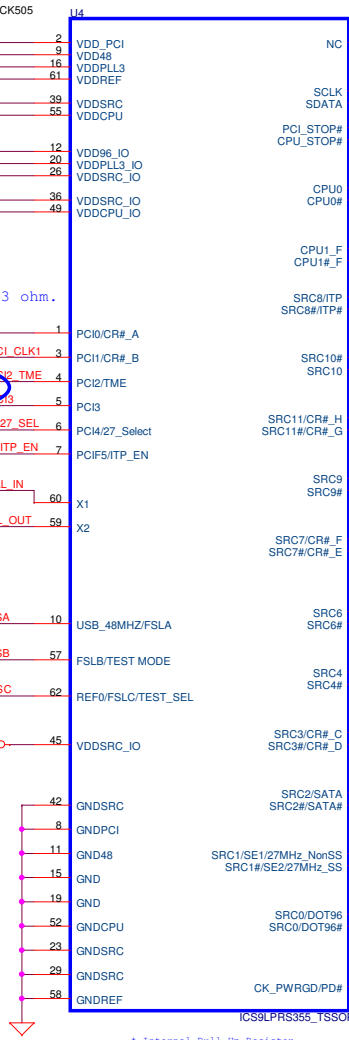


0308\_Change R89 and R92 form 0 ohm to bead, C209, C211, C216, C218 from 0.1uF to 680pF.

CLRP4,CLRP5 for 667/800 FSB select  
SHORT CLRP5, NO SHORT CLRP4 -- CPU option  
SHORT CLRP4, NO SHORT CLRP5 -- FSB 667

0301\_Change R105 from 22 ohm to 0 ohm.  
0312\_Change R106, 107, 109 from 22 to 33 ohm.

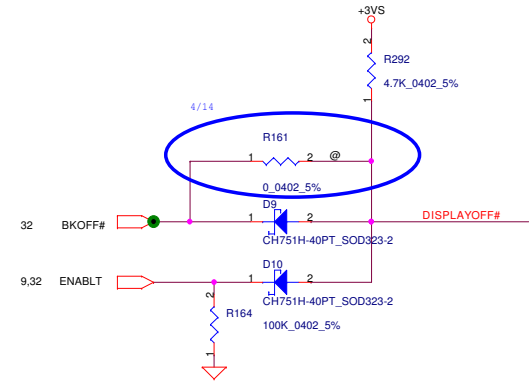
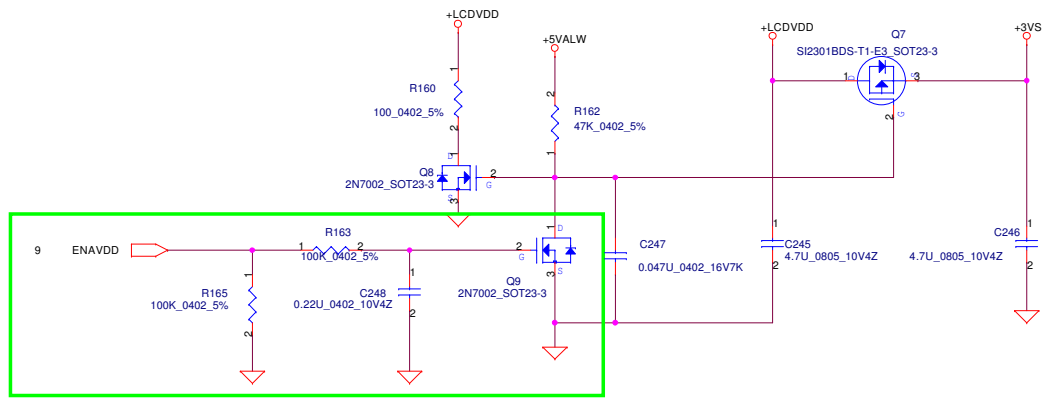
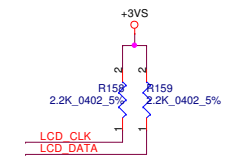
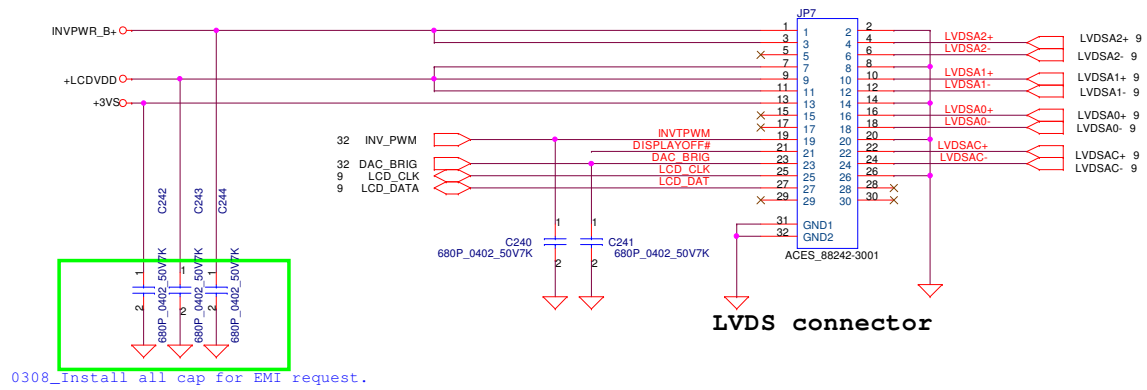
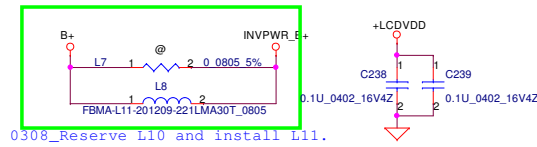
Routing the trace at  
least 10mil







# LVDS CONN



**U7B**

| Signal | U7B Pin | Chip Pin | Function    |
|--------|---------|----------|-------------|
| D20    | AD0     | A4       | PCI REQ0#   |
| E19    | AD1     | D7       | PCI GNT0#   |
| D19    | AD2     | C18      | PCI REQ1#   |
| A20    | AD3     | C18      | PCI REQ1#   |
| D17    | AD4     | B19      | PCI REQ2#   |
| A21    | AD5     | F18      | PCI REQ3#   |
| A19    | AD6     | A11      | PCI GNT3#   |
| C19    | AD7     | C10      | PCI REQ3#   |
| A18    | AD8     |          |             |
| X16    | AD9     | C17      |             |
| A12    | AD10    | E15      |             |
| E16    | AD11    | E16      |             |
| A14    | AD12    | E17      |             |
| G16    | AD13    |          |             |
| A15    | AD14    | C8       | PCI IRDY#   |
| B6     | AD15    | D9       |             |
| C11    | AD16    | G6       | PCI PCIRST# |
| A9     | AD17    | D16      | PCI DEVSEL# |
| D12    | AD18    | A7       | PCI PERR#   |
| B12    | AD19    | B7       | PCI PLOCK#  |
| C12    | AD20    | F10      | PCI SERR#   |
| D10    | AD21    | C16      | PCI STOP#   |
| C9     | AD22    | G9       | PCI TRDY#   |
| F13    | AD23    | A17      | PCI FRAME#  |
| E11    | AD24    |          |             |
| X13    | AD25    | AG24     | PCI PLTRST# |
| E12    | AD26    | B10      | CLK PCI ICH |
| D8     | AD27    | G7       | PCI PME#    |
| A6     | AD28    |          |             |
| D6     | AD29    |          |             |
| A3     | AD30    |          |             |
|        | AD31    |          |             |

**Interrupt I/F**

| Signal     | U7B Pin | Chip Pin | Function   |
|------------|---------|----------|------------|
| PCI PIROA# | F9      | F8       | PCI PIROE# |
| PCI PIROB# | B5      | G11      | PCI PIROF# |
| PCI PIROC# | C5      | F12      | PCI PIROG# |
| PCI PIROD# | A10     | B3       | PCI PIROH# |

ICH8M REV 1.0

**Place closely pin B10**

CLK\_PCI\_ICH

R187

@ 0\_10402\_5%

C249

@8.2P\_0402\_50V

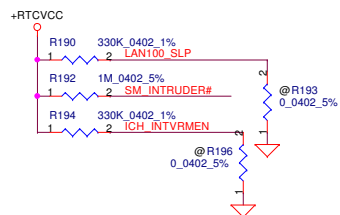
**Boot BIOS St**

| PCI_GNT0# |
|-----------|
| 0         |
| 1         |
| 1         |

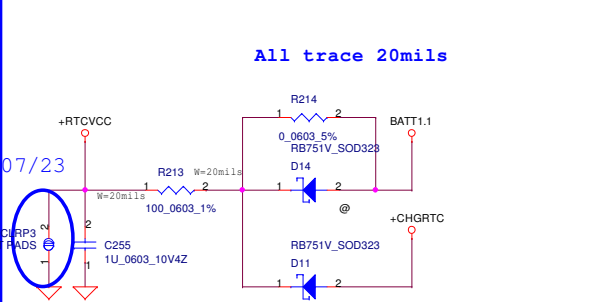
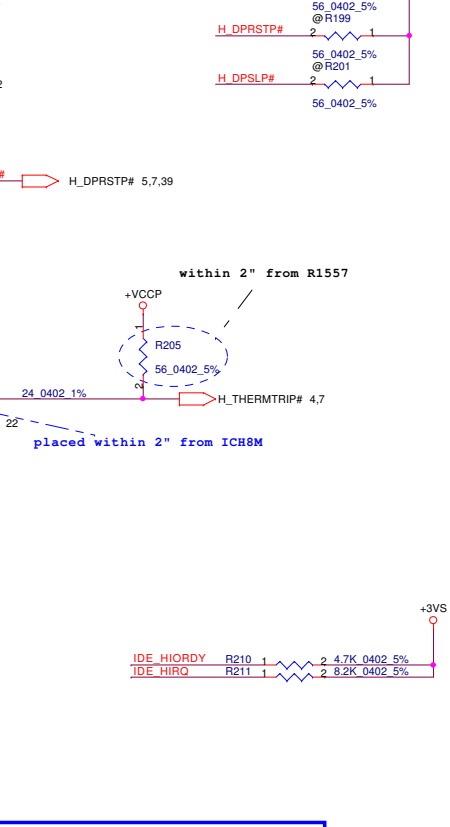
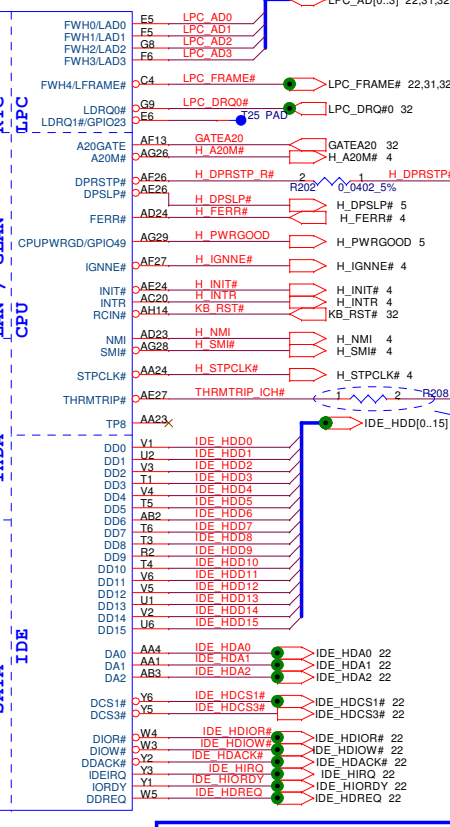
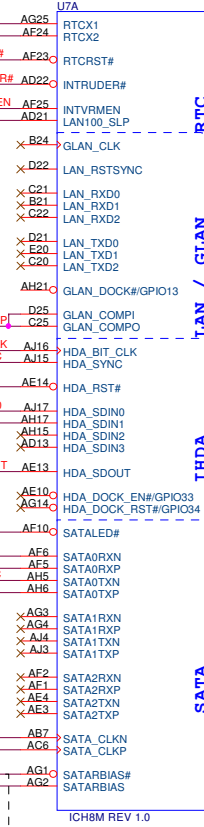
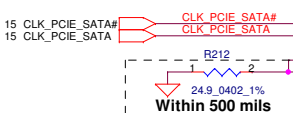
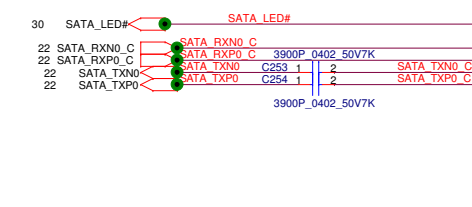
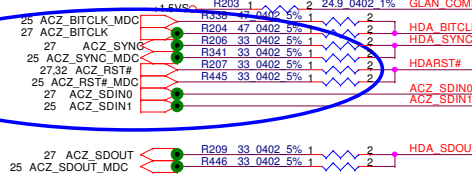
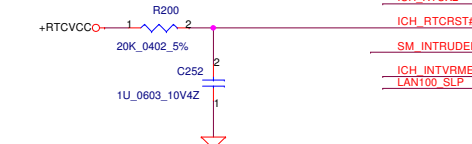
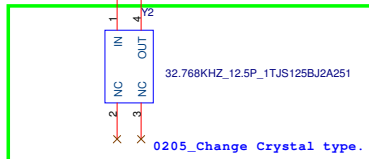
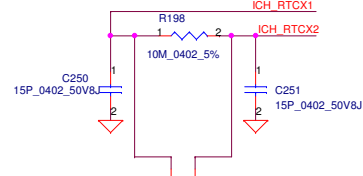
| Boot BIOS Strap |          |                    |
|-----------------|----------|--------------------|
| PCI_GNT0#       | SPI_CS#1 | Boot BIOS Location |
| 0               | 1        | SPI                |
| 1               | 0        | PCI                |
| 1               | 1        | LPC *              |

| A16 swap override Strap |   |
|-------------------------|---|
| PCI_GNT3#               | *Low= A16 swap override Enable<br>High= Default |

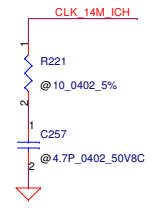
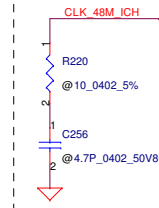


| ICH8M Internal VR Enable Strap<br>(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5) |   |
|---|---|
| ICH_INTVRMEN  | Low = Internal VR Disabled<br>High = Internal VR Enabled(Default) |
| ICH8M LAN100 SLP Strap<br>(Internal VR for VccLAN1.05 and VccCL1.05)                |   |
| ICH_LAN100_SLP  | Low = Internal VR Disabled<br>High = Internal VR Enabled(Default) |

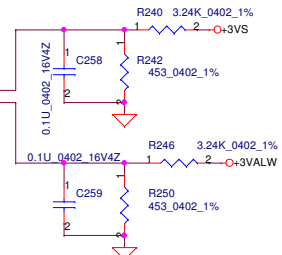


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|   |            |                    |            | Date                     | Tuesday, July 31, 2007 |
|   |            |                    |            | Sheet                    | 19 of 43               |

Place closely pin G5      Place closely pin AG9



0205 Change to connect to GND.

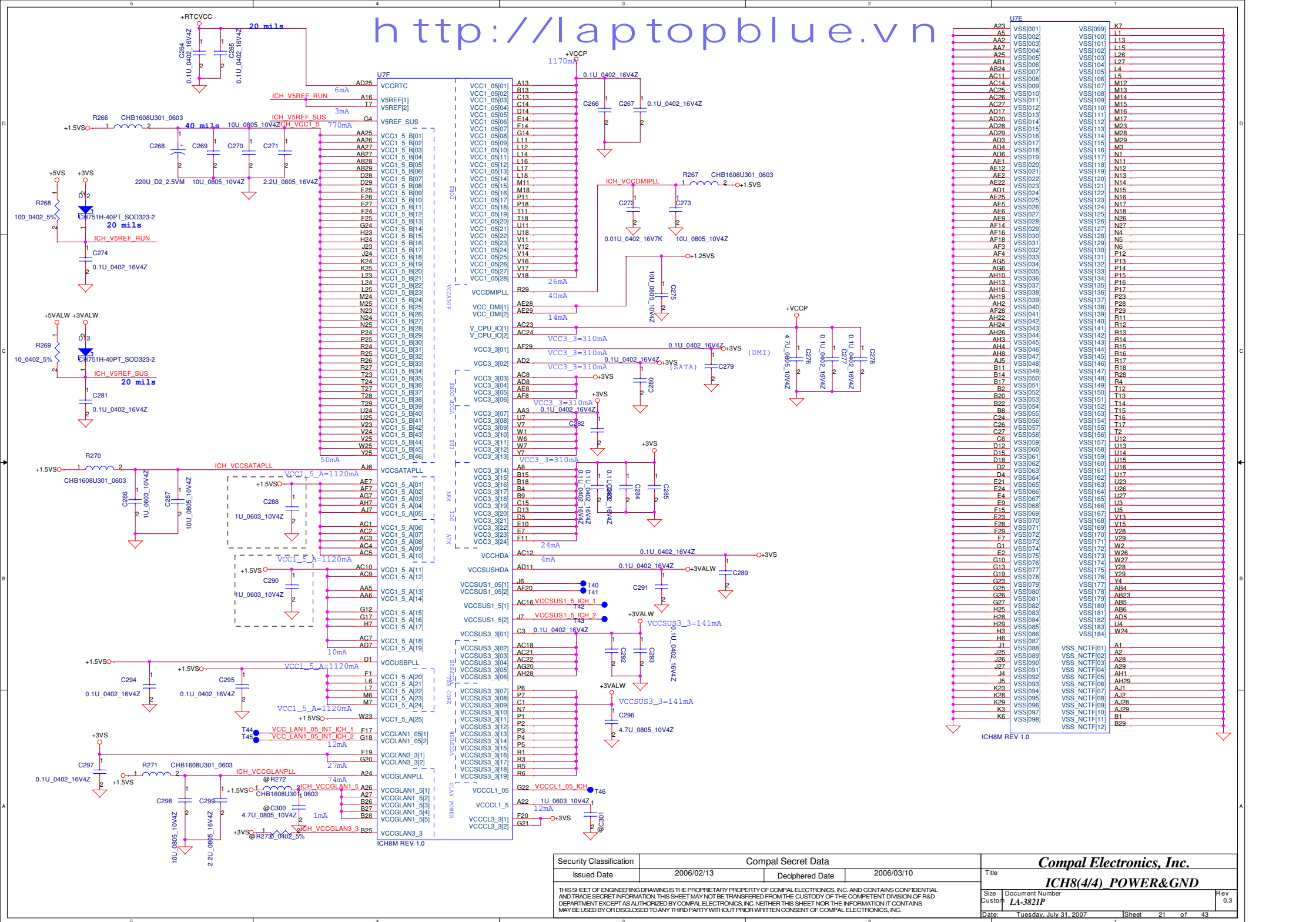


Within 500 mils

- To New Card
- To Card reader/B.
- To Bluetooth
- To PC Camera
- To Finger Printer

**Within 500 mils**

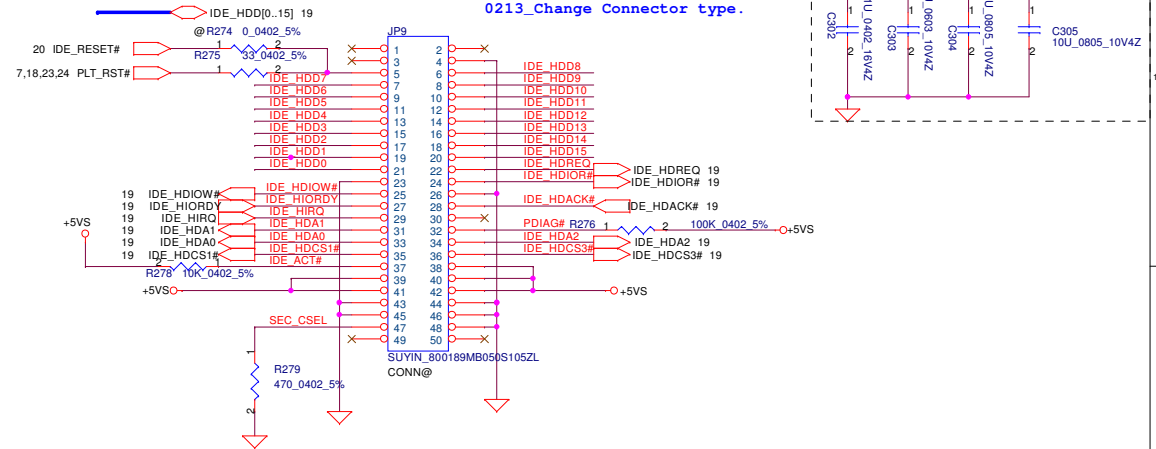
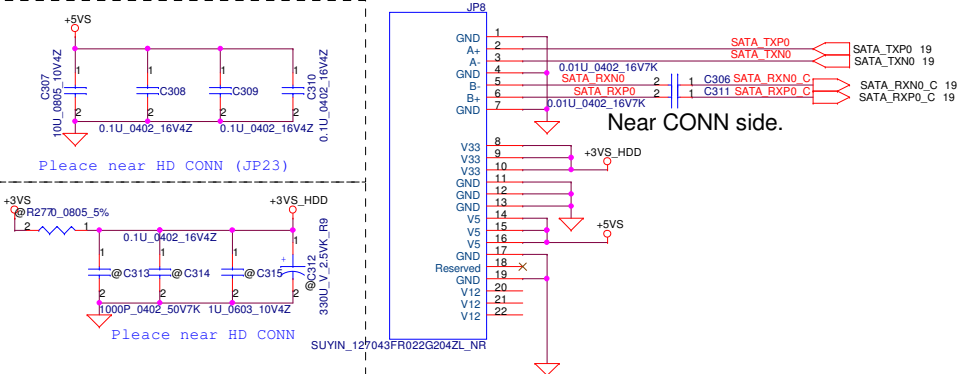
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|---|--------------------|-----------------|------------|---|------------------------|----------------|
| Security Classification   | Compal Secret Data |                 |            | <b>Compal Electronics, Inc.</b><br><b>ICH8(3/4)_PM,USB,GPIO</b> |                        |                |
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|   |                    |                 |            | Custmr  | LA-3821P               | 0.3            |
|   |                    |                 |            | Date:   | Tuesday, July 31, 2007 | Sheet 20 of 43 |



## HDD Connector

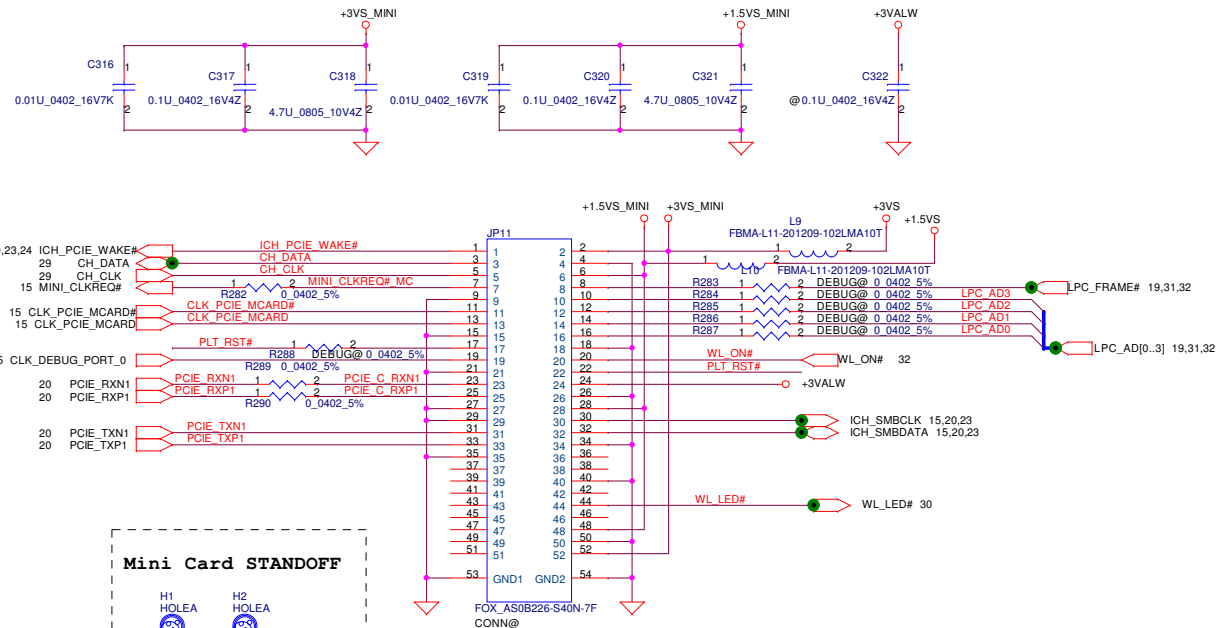
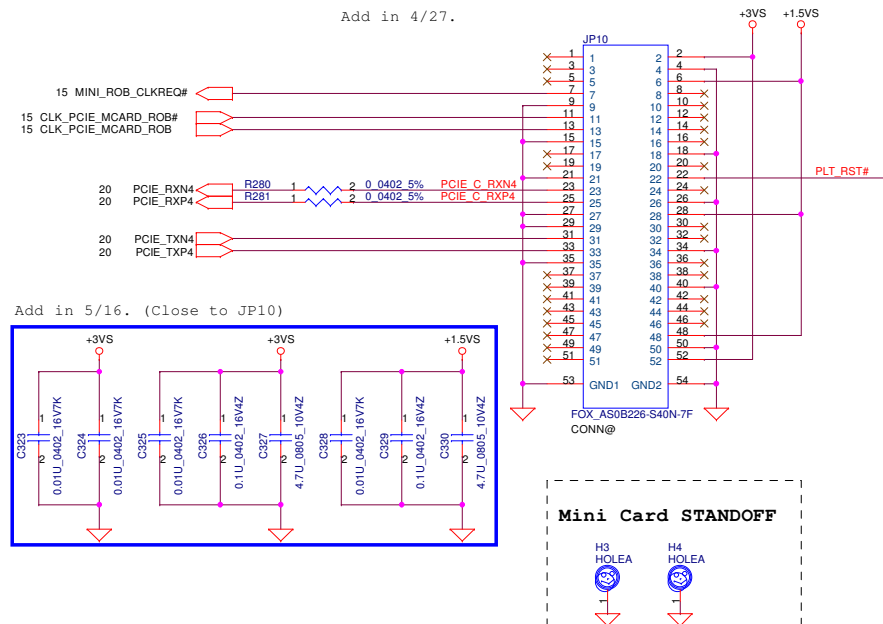
## CD-ROM Connector

Place caps. near ODD CONN.



## NAND mini Card(Robson support)

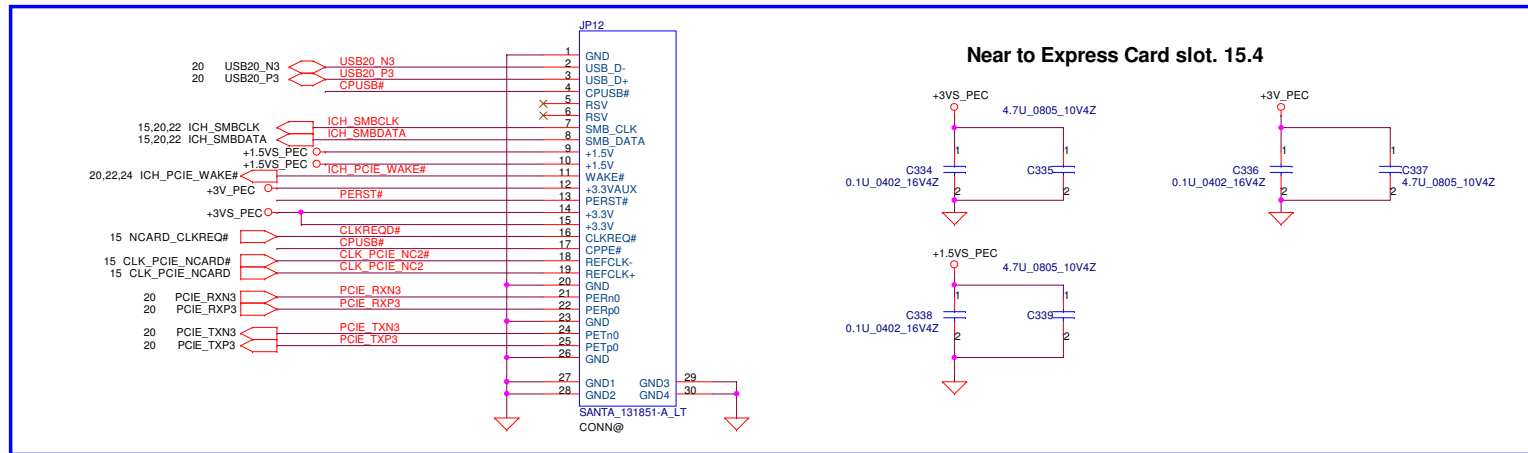
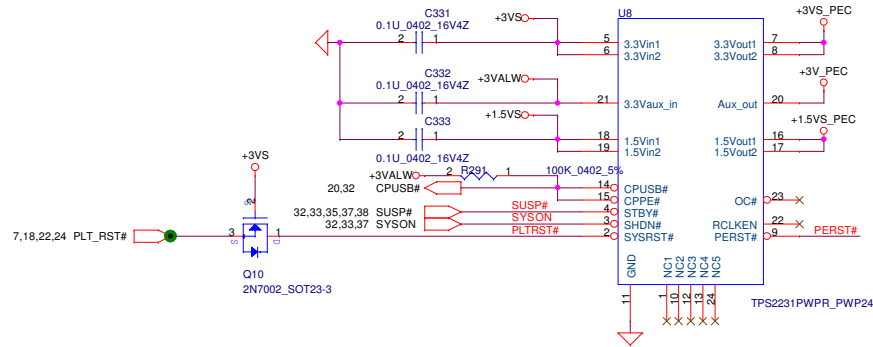
## Mini-Express Card---WLAN



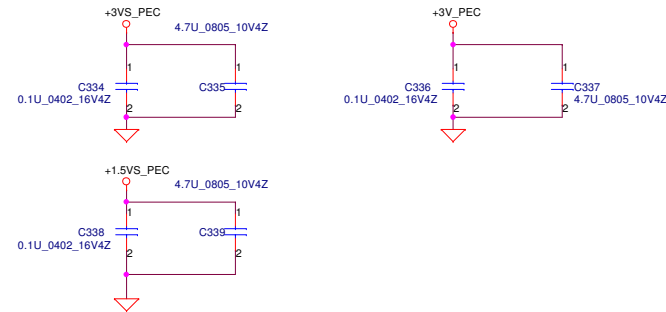
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| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |                 |
| Issued Date   | 2006/02/13 | Deciphered Date    | 2007/08/29 | Title                    |                 |
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|   |            |                    |            | Date                     | Rev             |
|   |            |                    |            | Tuesday, July 31, 2007   | 0.3             |
|   |            |                    |            | Sheet                    | 22 of 43        |



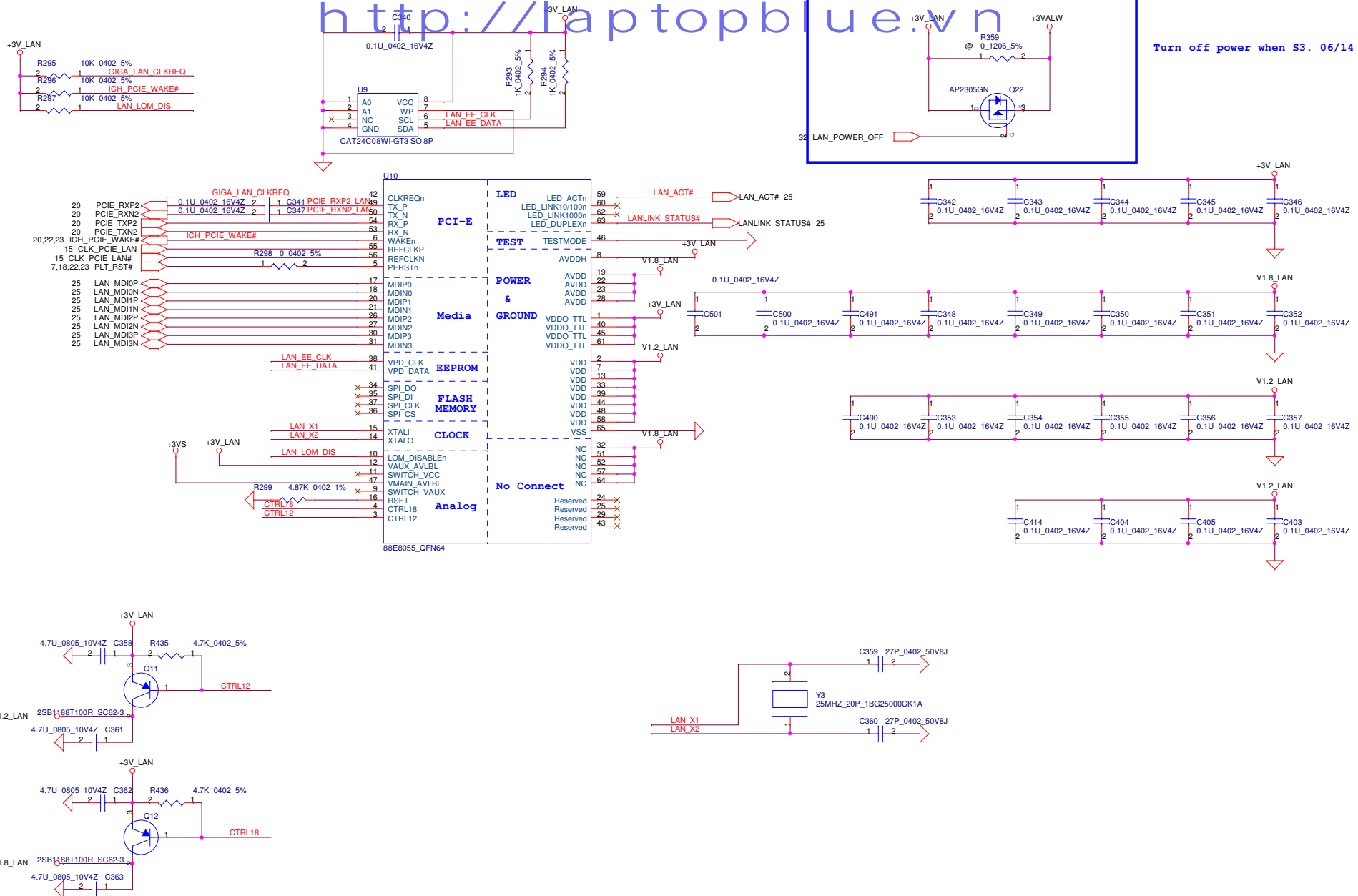
## Express Card Power Switch



### Near to Express Card slot. 15.4

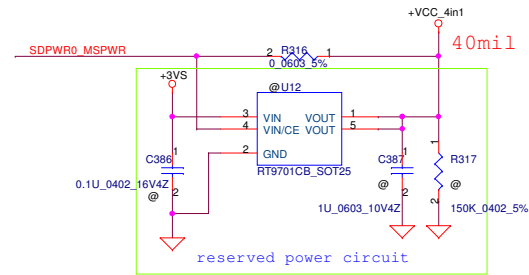


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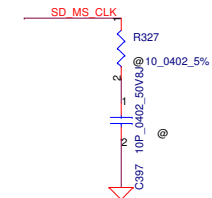
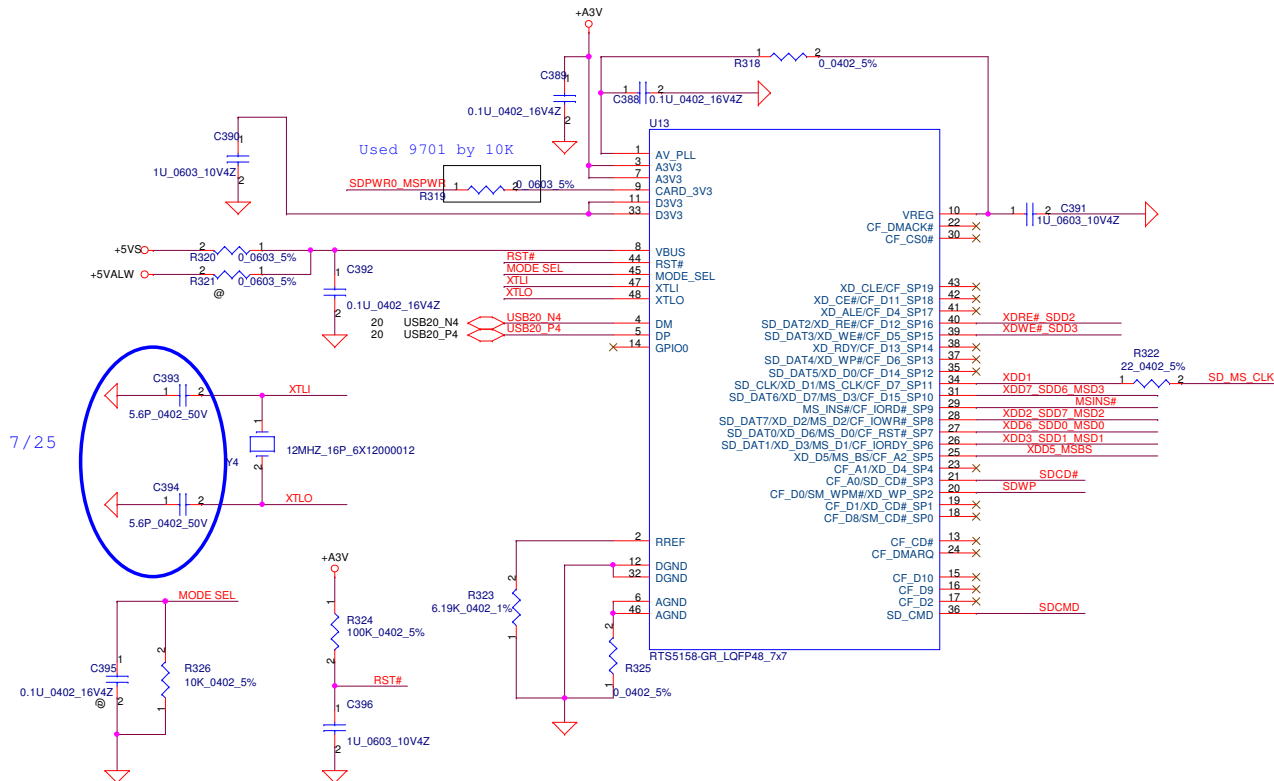
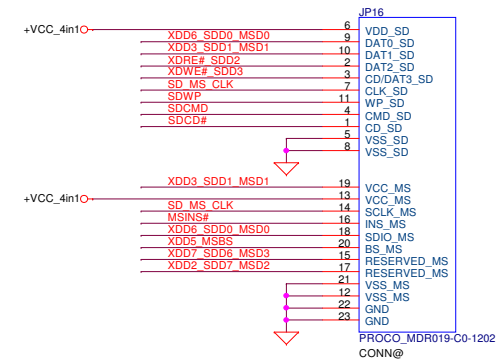


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|---|------------|--------------------|------------|--------------------------|-----------------|
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|   |            |                    |            | Size                     | Document Number |
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| Date: Tuesday, July 31, 2007  |            | Sheet 24 of 43     |            | Rev 0.3                  |                 |





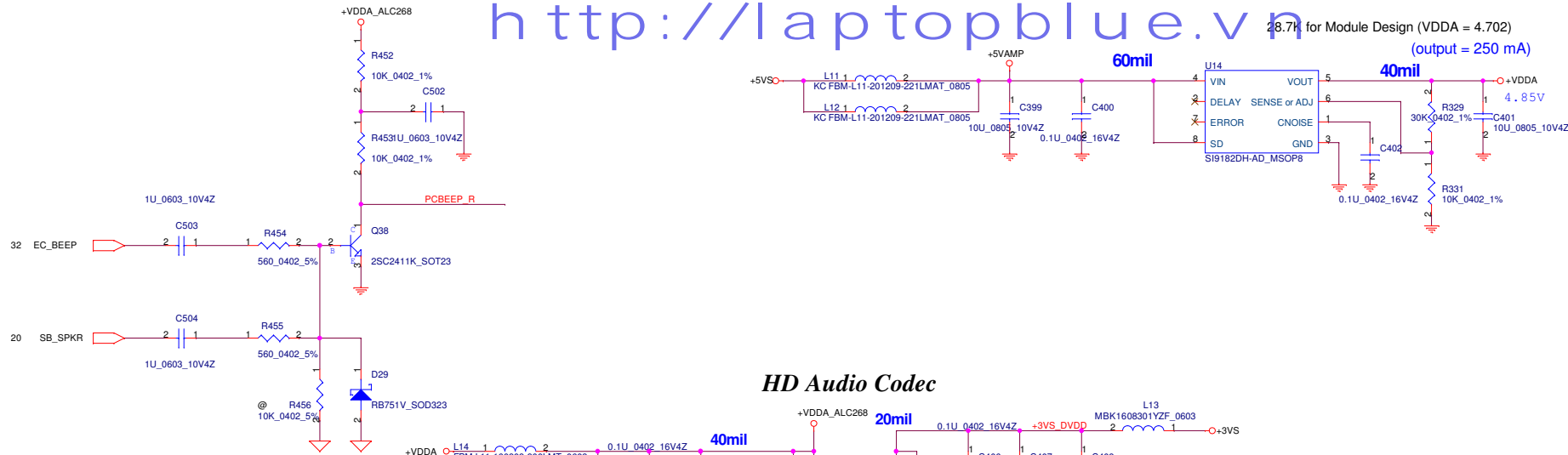
### 3 in 1 Card Reader



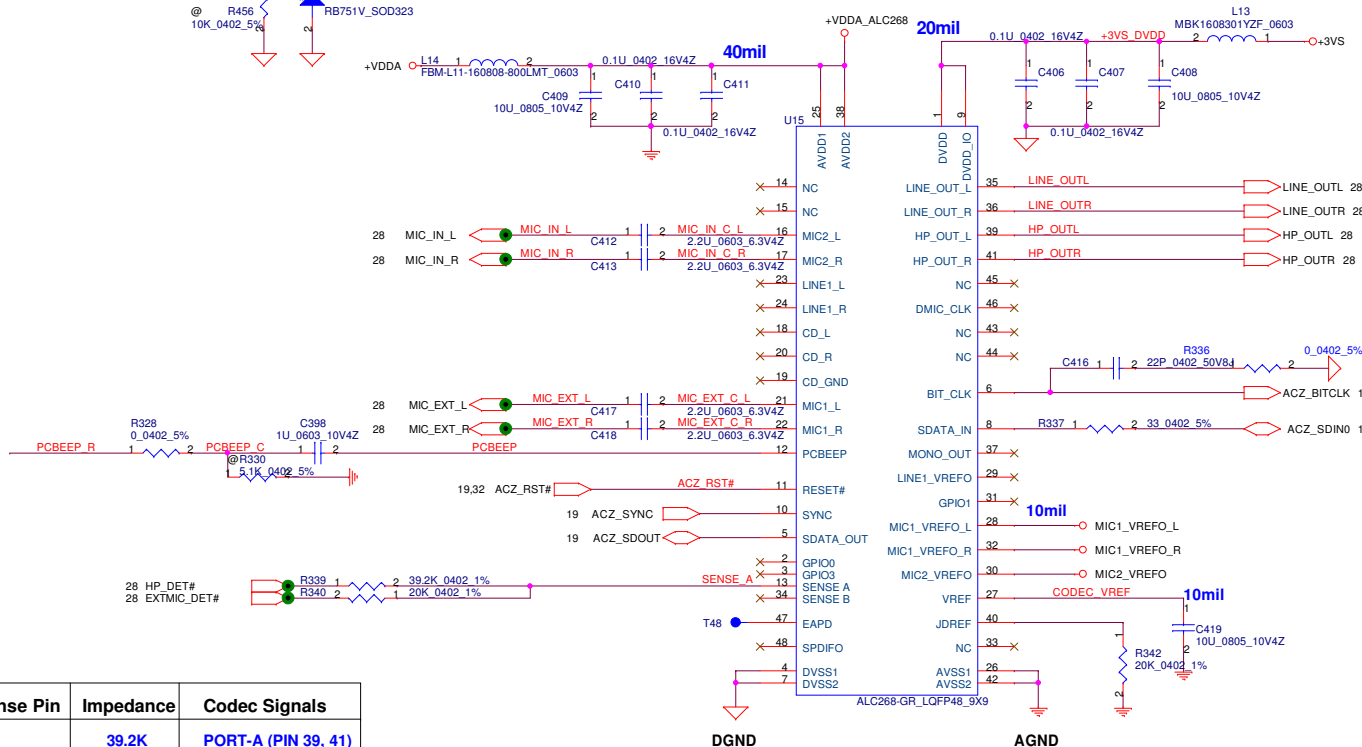
Compal Electronics, Inc.

| Card reader board |                        |       |          |
|-------------------|------------------------|-------|----------|
| Size              | Document Number        | Rev   |          |
|                   | LA-3821P               | 0.3   |          |
| Date:             | Tuesday, July 31, 2007 | Sheet | 26 of 43 |

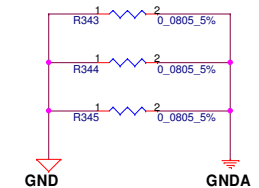
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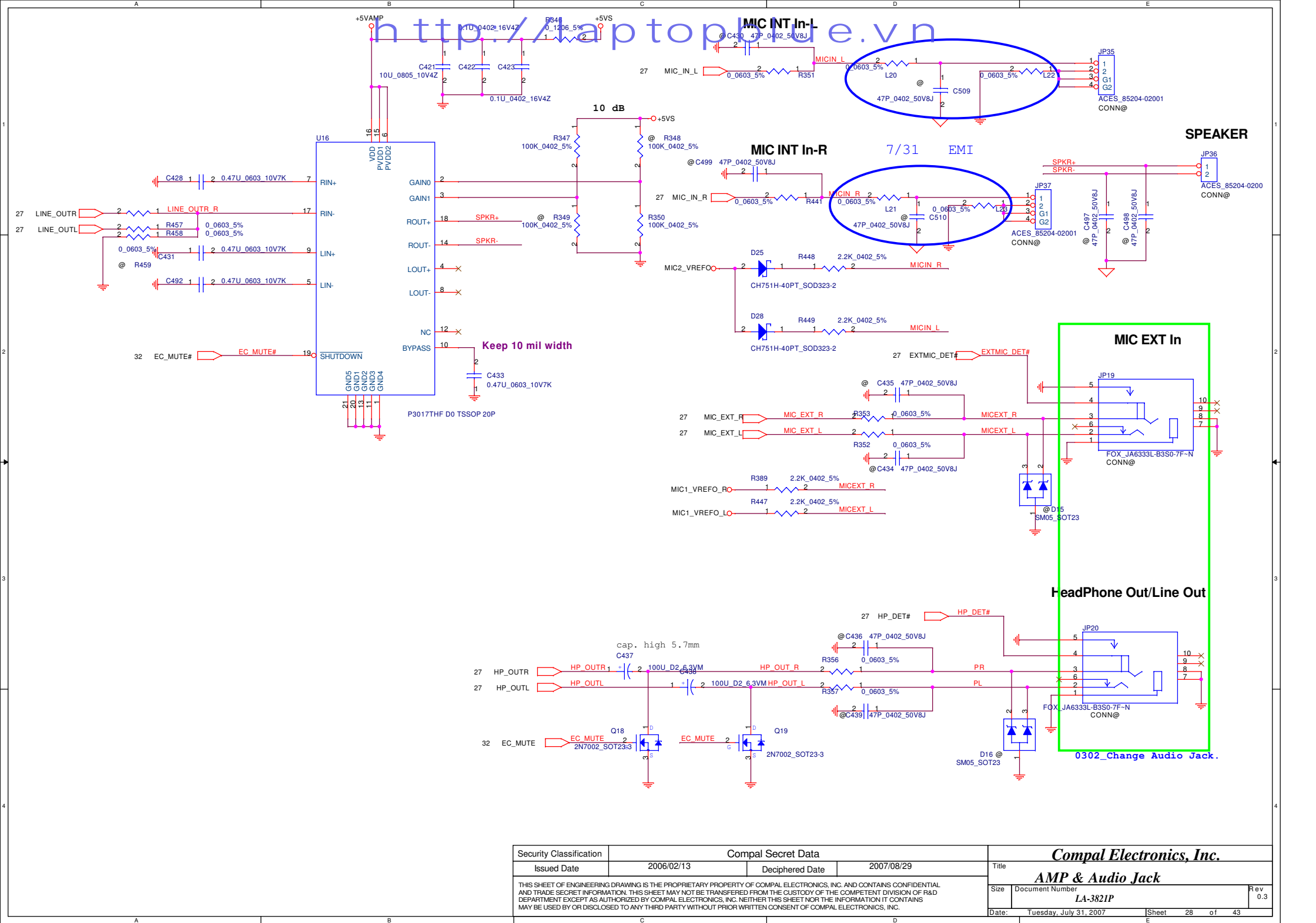


## HD Audio Codec



| Sense Pin | Impedance | Codec Signals       |
|-----------|-----------|---------------------|
| SENSE A   | 39.2K     | PORT-A (PIN 39, 41) |
|           | 20K       | PORT-B (PIN 21, 22) |
|           | 10K       | PORT-C (PIN 23, 24) |
|           | 5.1K      | PORT-D (PIN 35, 36) |
| SENSE B   | 39.2K     | PORT-E (PIN 14, 15) |
|           | 20K       | PORT-F (PIN 16, 17) |
|           | 10K       | PORT-G (PIN 43, 44) |
|           | 5.1K      | PORT-H (PIN 45, 46) |



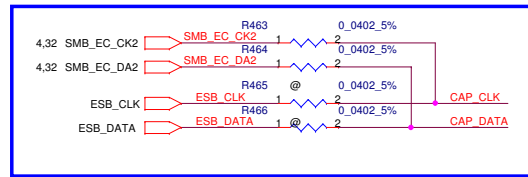
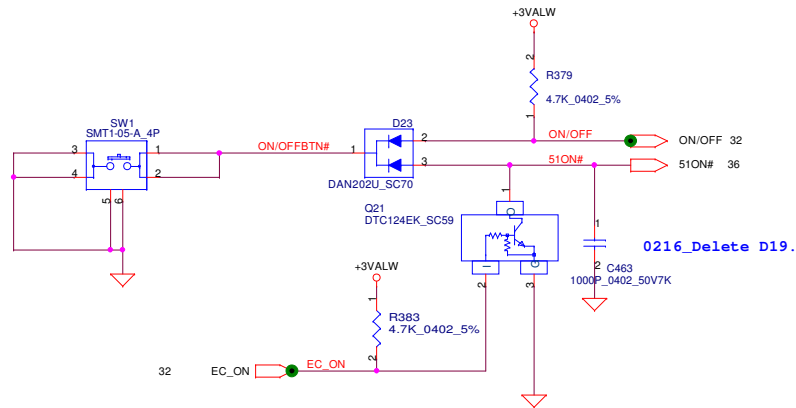




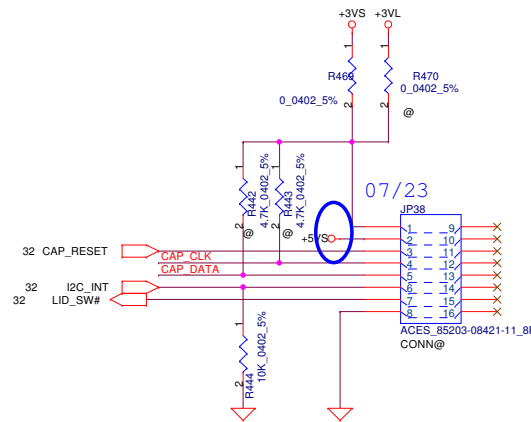


## Power ON/OFF

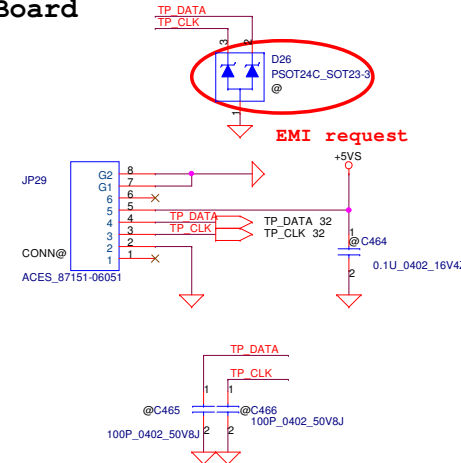
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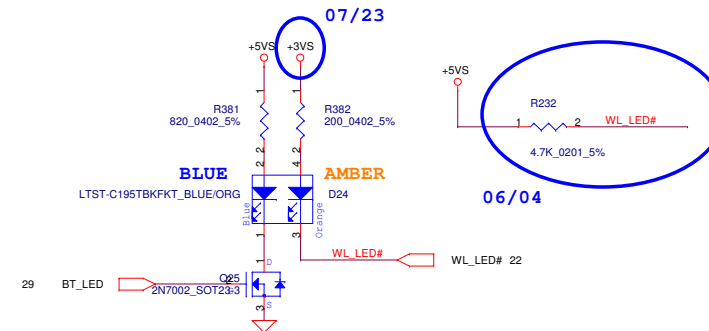
06/15 Change pin define for try ENE cap bottom



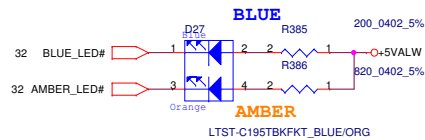
## T/P Board



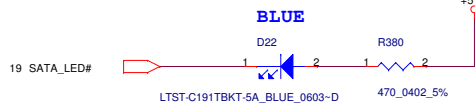
## Wireless ON Amber Bluetooth ON Blue



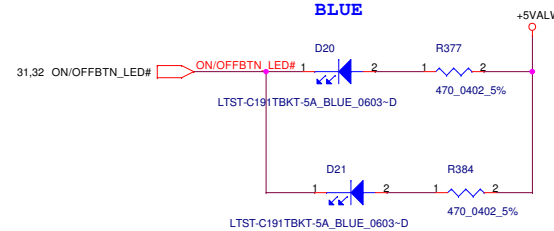
## Battery Charge LED(Left 2)



## HDD LED(Left 3)

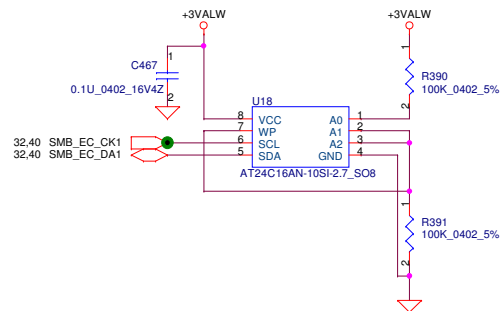


## POWER LED1

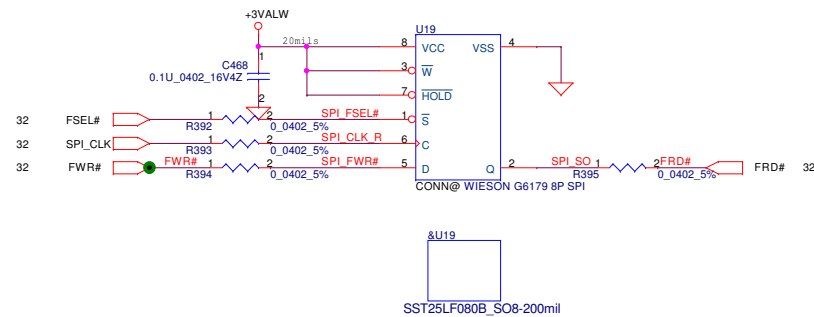


## POWER LED2

|   |                    |                 |            |                          |                        |
|---|--------------------|-----------------|------------|--------------------------|------------------------|
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|   |                    |                 |            | Date:                    | Tuesday, July 31, 2007 |
|   |                    |                 |            | Sheet                    | 30 of 43               |

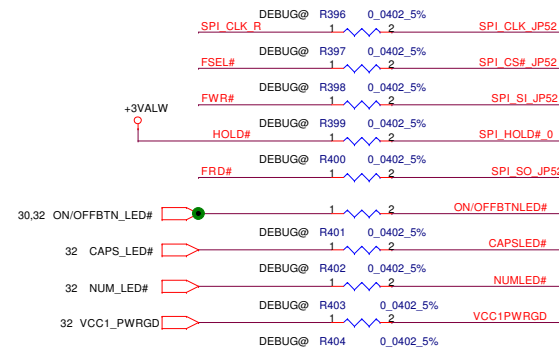
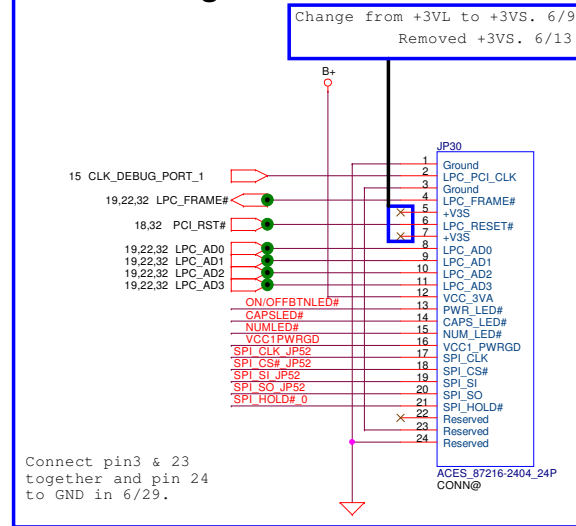


### SPI ROM



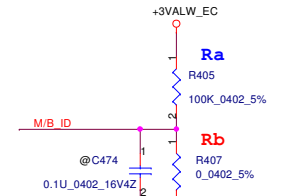
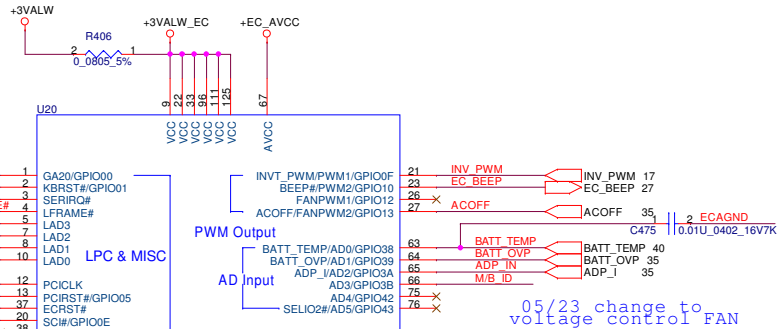
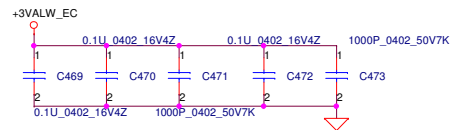
B-Test remove SPI ROM socket

### LPC Debug Port

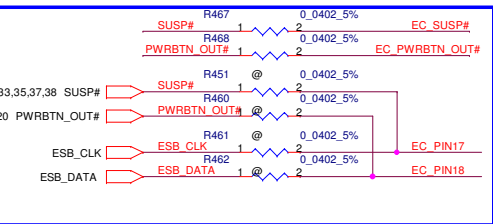
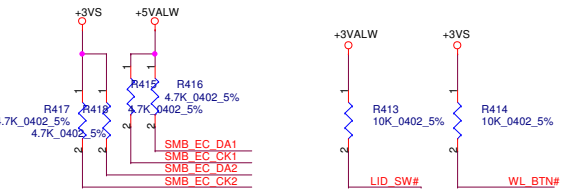
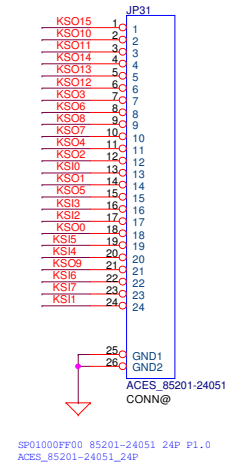
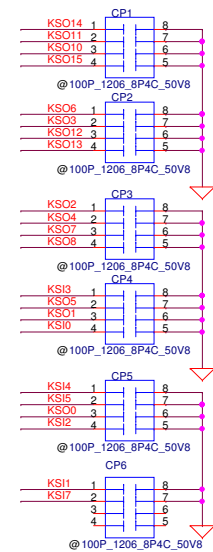
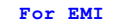
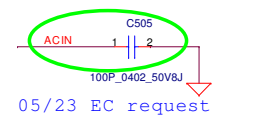
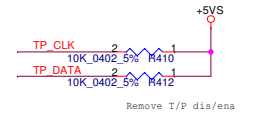


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| Size  |                    | Document Number        |            |                          |    | Rev |
|   |                    | LA-3821P               |            |                          |    | 0.3 |
| Date:   |                    | Tuesday, July 31, 2007 | Sheet      | 31                       | of | 43  |

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|          |           |                         |                         |                         |
|----------|-----------|-------------------------|-------------------------|-------------------------|
| VCC      | 3.3V+/-5% |                         |                         |                         |
| Ra       | 100K+/-5% |                         |                         |                         |
| Board ID | Rb        | V <sub>AD_BID</sub> min | V <sub>AD_BID</sub> typ | V <sub>AD_BID</sub> max |
| 0        | 0         | 0V                      | 0V                      | 0V                      |
| 1        | 8.2K+/-5% | 0.216V                  | 0.250V                  | 0.289V                  |
| 2        | 18K+/-5%  | 0.436V                  | 0.503V                  | 0.538V                  |
| 3        | 33K+/-5%  | 0.712V                  | 0.819V                  | 0.875V                  |
| 4        | 56K+/-5%  | 1.036V                  | 1.185V                  | 1.264V                  |
| 5        | 100K+/-5% | 1.453V                  | 1.650V                  | 1.759V                  |
| 6        | 200K+/-5% | 1.935V                  | 2.200V                  | 2.341V                  |
| 7        | NC        | 2.500V                  | 3.300V                  | 3.300V                  |

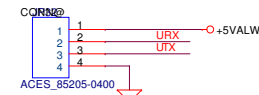


06/15 Change pin define for try ENE cap bottom

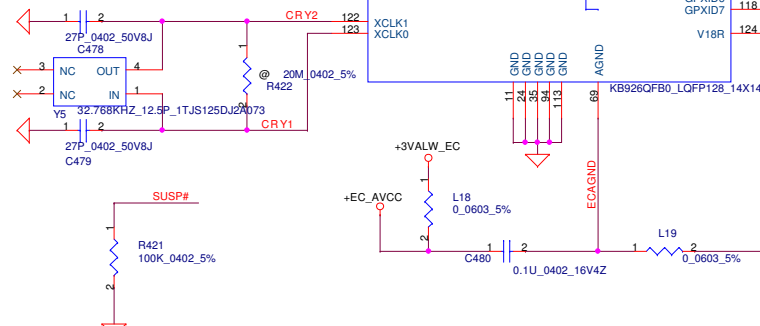
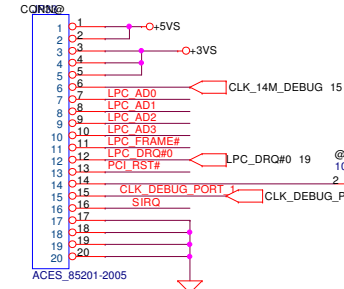


05/23 change to  
voltage control FA

EC DEBUG port

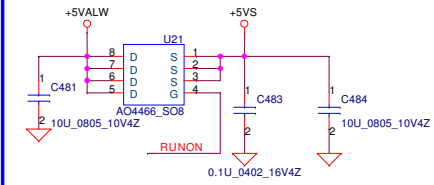


**FOR LPC SIO DEBUG PORT**

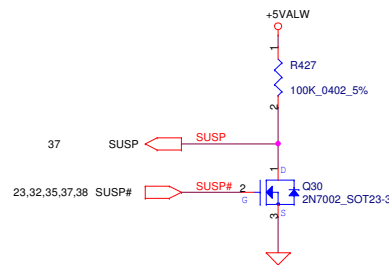
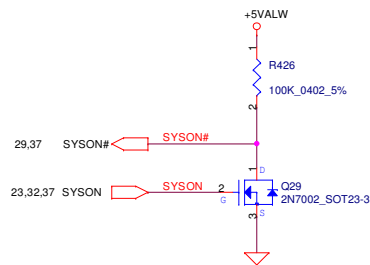
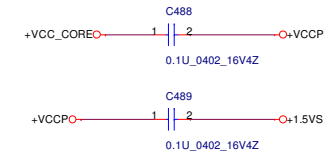
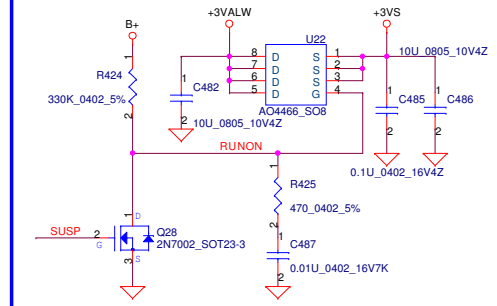


|   |  |                    |                 |                                 |                                  |                |
|---|--|--------------------|-----------------|---------------------------------|----------------------------------|----------------|
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|   |  |                    |                 |                                 | LA-382/P                         | 0.3            |
|   |  |                    |                 | Date:                           | Tuesday, July 31, 2007           | Sheet 32 of 43 |

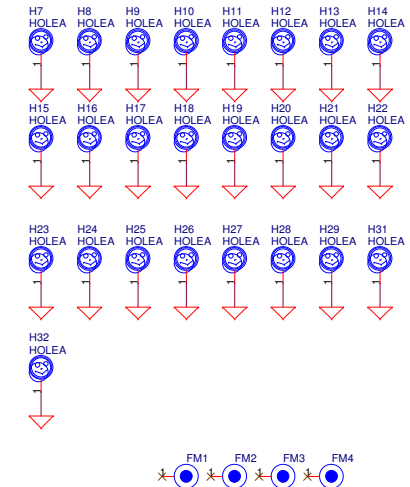
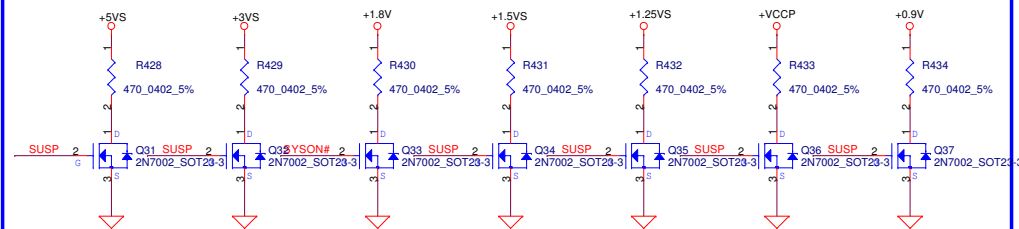
### +5VALW to +5VS Transfer



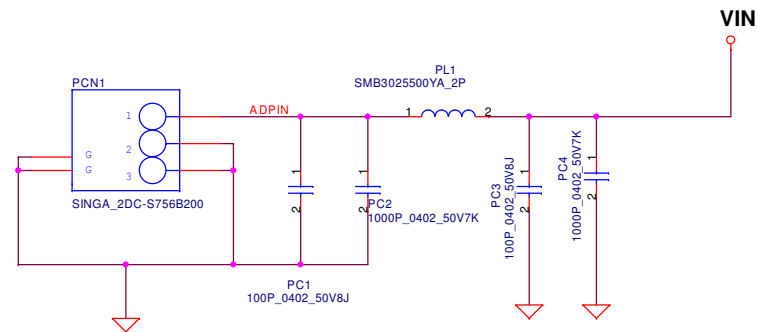
### +3VALW to +3VS Transfer



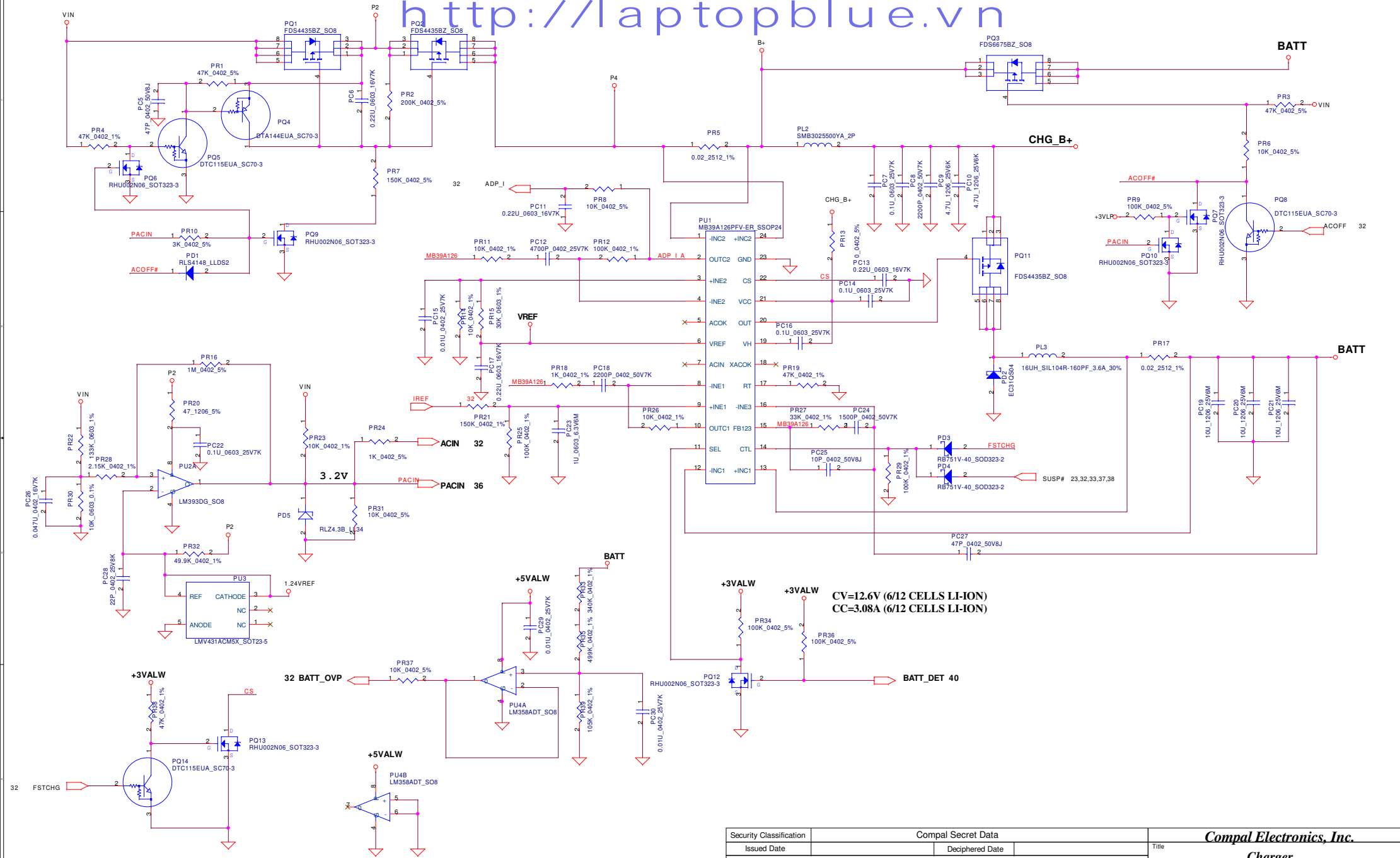
### Discharge circuit

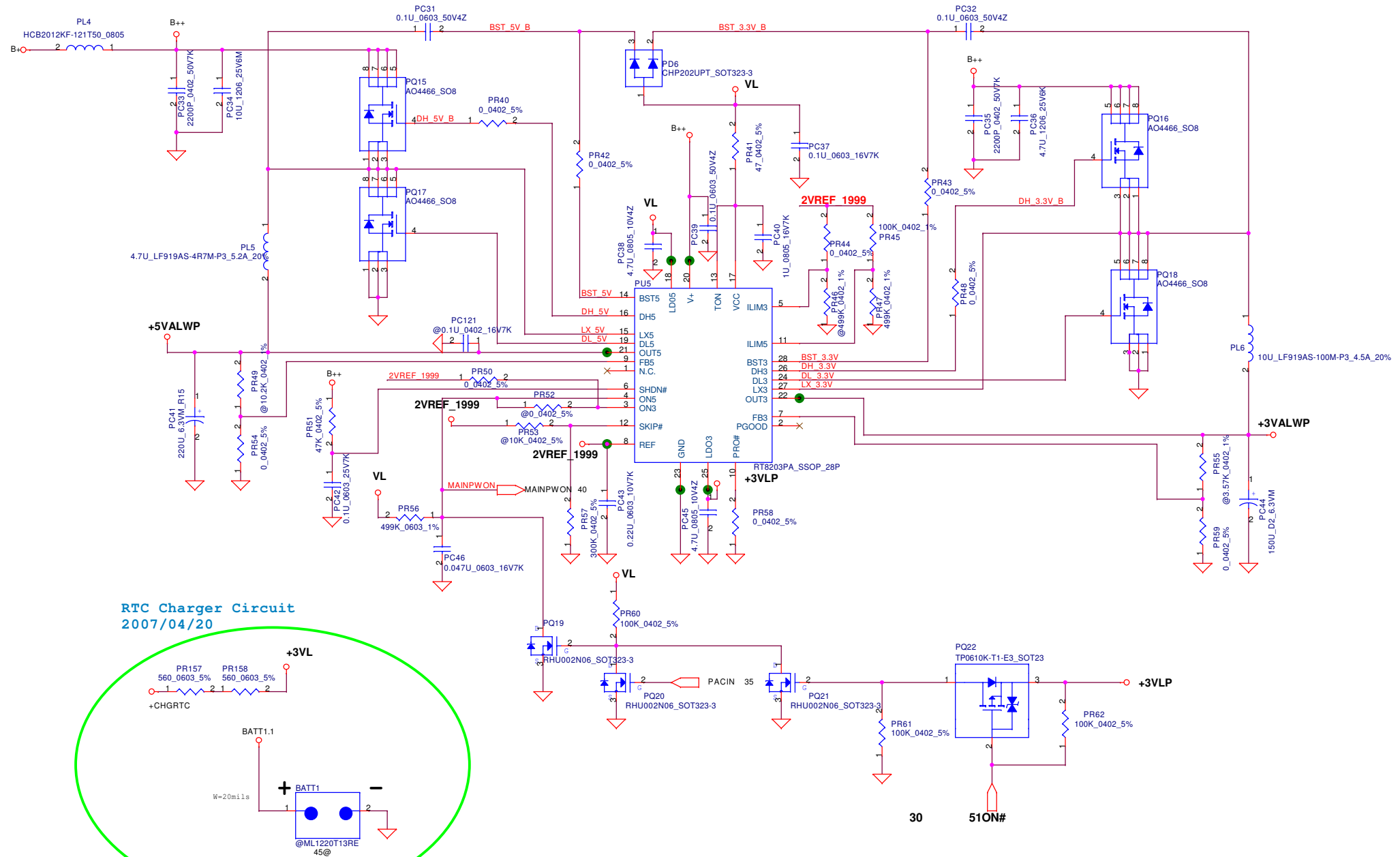


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|---|--------------------|-----------------|------------|--------------------------|-----------------|
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|   |                    |                 |            | Size                     | Document Number |
|   |                    |                 |            | LA-3821P                 |                 |
| Date: Tuesday, July 31, 2007  |                    |                 |            | Sheet                    | 33 of 43        |
|   |                    |                 |            | Rev                      | 0.3             |



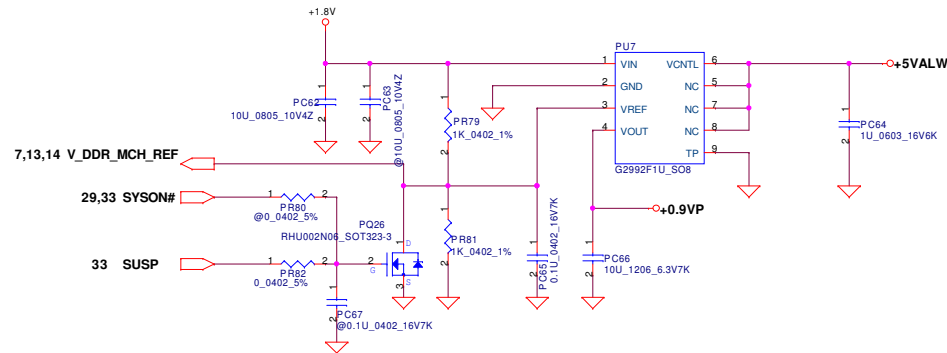
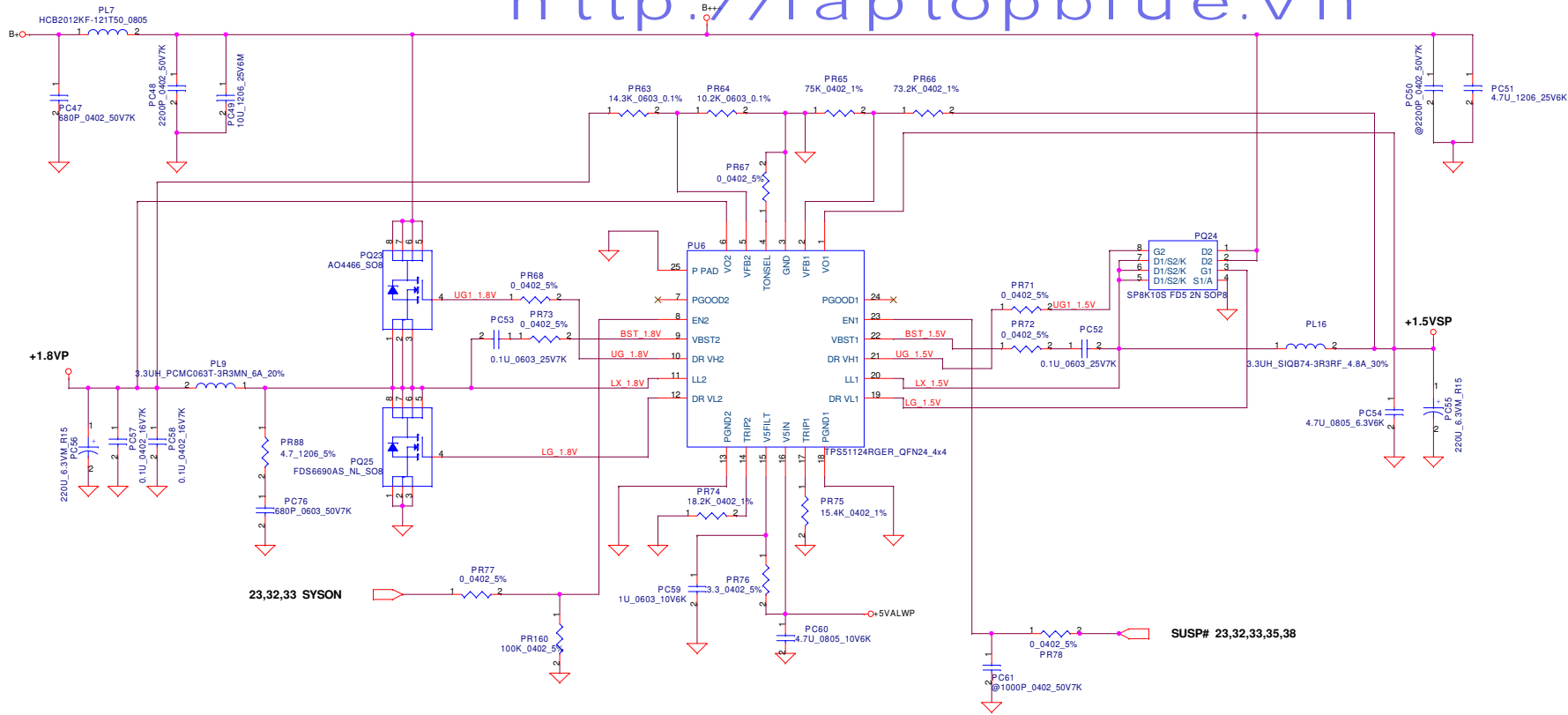
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| Security Classification   |               | Compal Secret Data |                   |                              |                                    |
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|   |               |                    |                   | Size<br>Custom               | Document Number<br><b>LA-3821P</b> |
|   |               |                    |                   | Date: Tuesday, July 31, 2007 | Sheet 34 of 43                     |





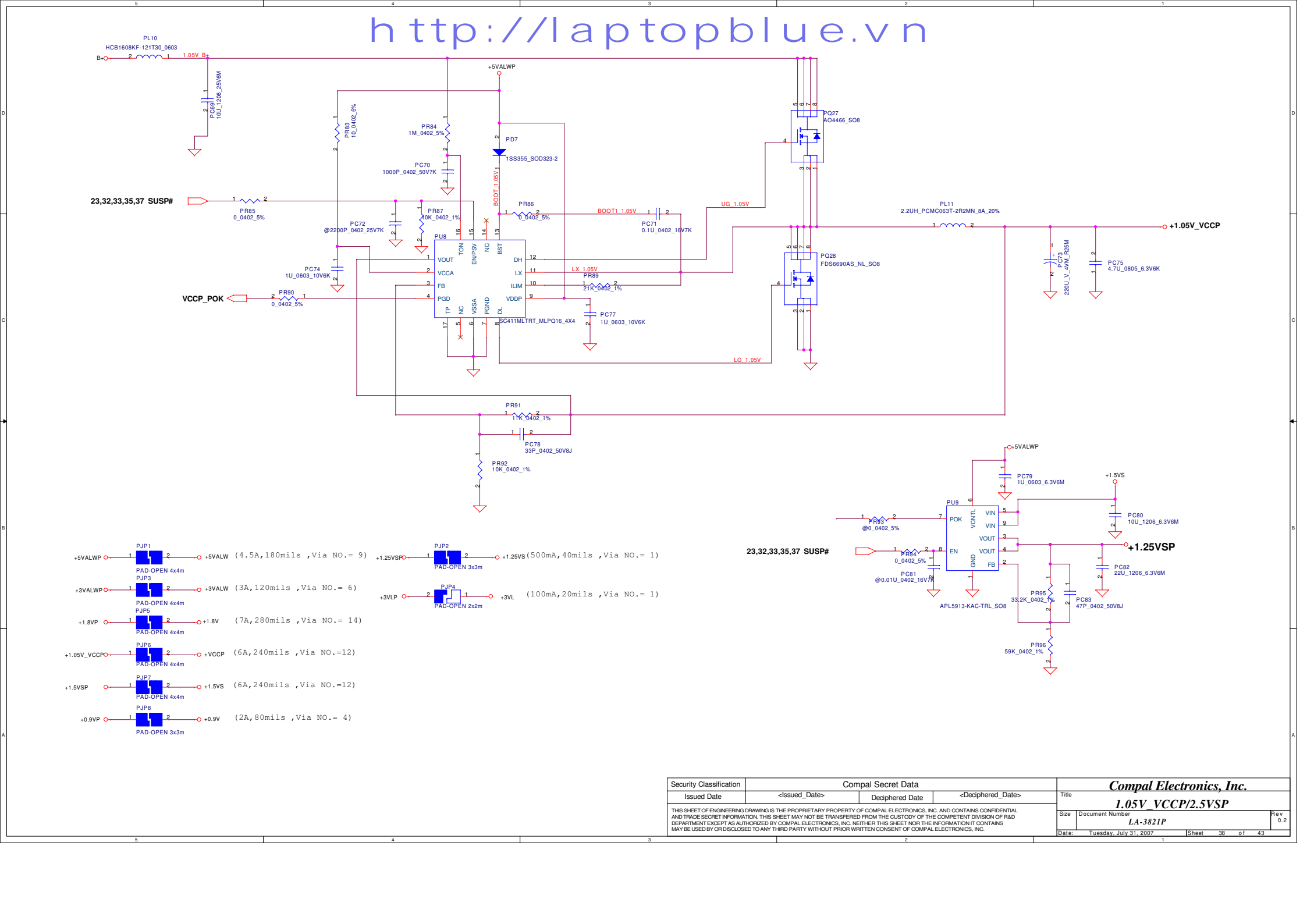
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| Security Classification   |                 | Compal Secret Data |                   | Compal Electronics, Inc.     |  |
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| Size  | Document Number | Rev                |                   | Date: Tuesday, July 31, 2007 |  |
| Sheet   |                 | 36                 |                   | of 43                        |  |



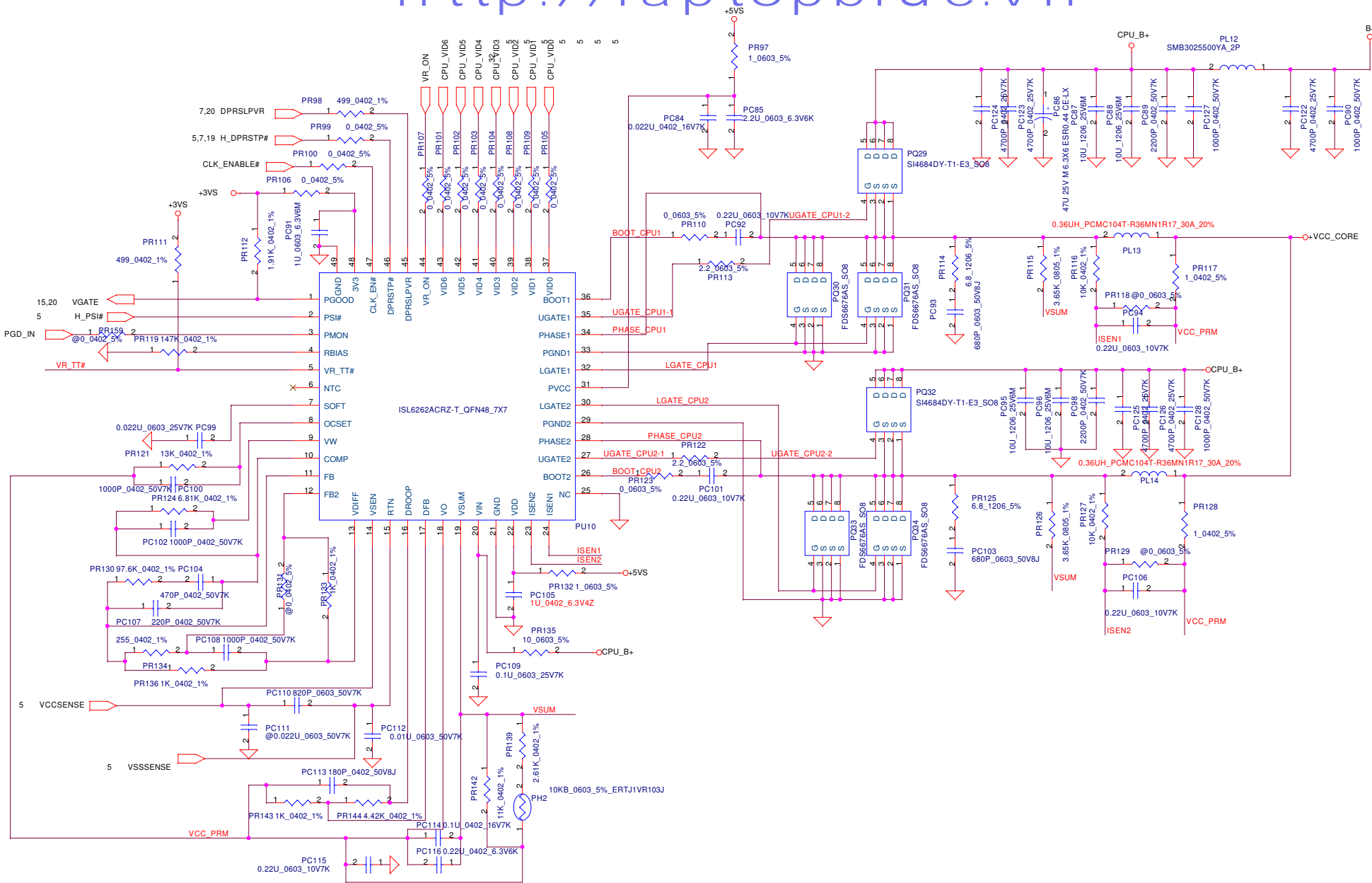


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|---|------------|--------------------|------------|--------------------------|------------------------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |                        |
| Issued Date   | 2006/11/23 | Deciphered Date    | 2007/11/23 | Title                    | 1.8VP/0.9VP/1.5VSP     |
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Compal Electronics, Inc.

+CPU\_CORE

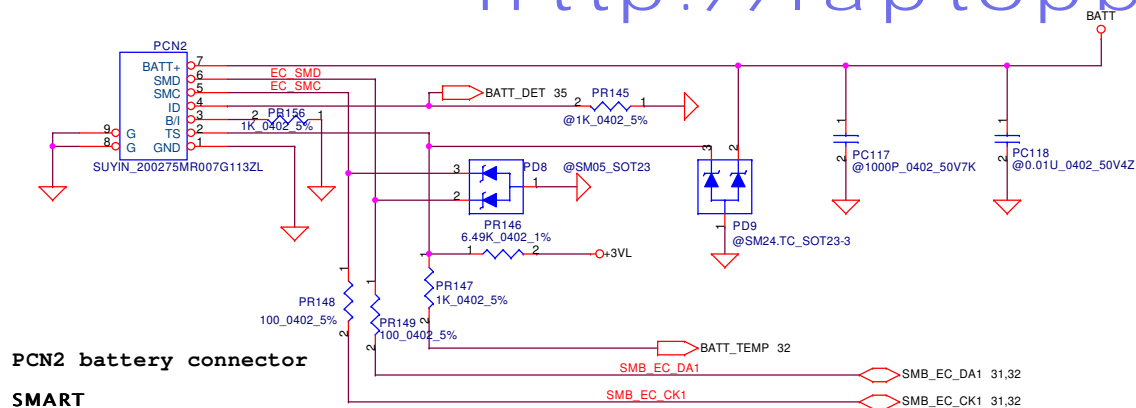
Size Custom Document Number

Date: Tuesday, July 31, 2007

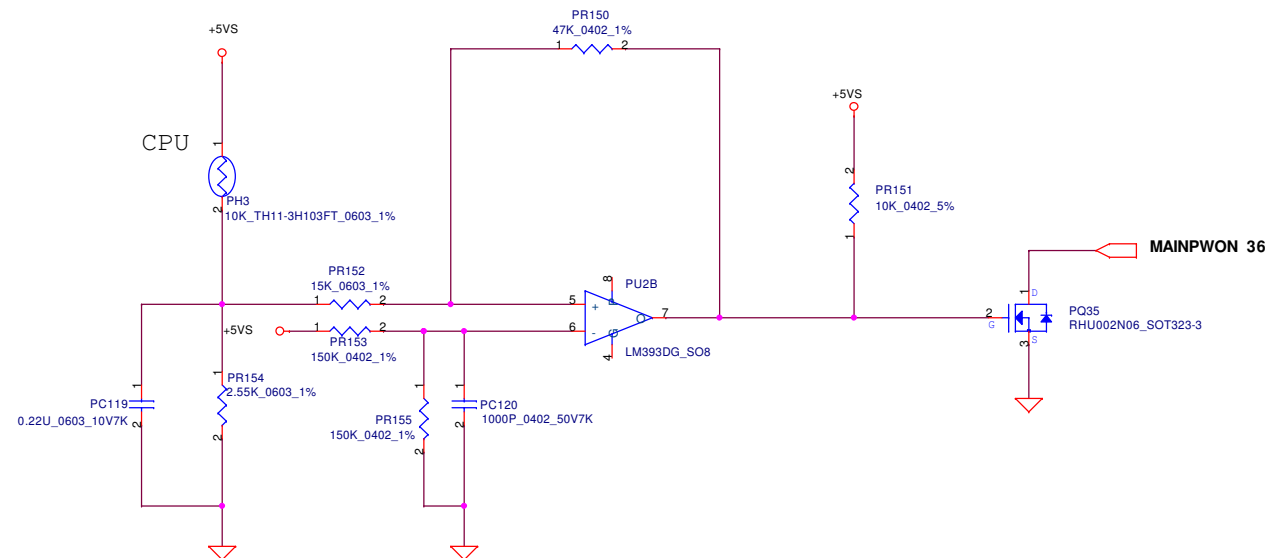
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**PH3 under CPU botten side :**  
CPU thermal protection at 90  $\pm$ 3 degree C  
Recovery at 47  $\pm$ 3 degree C



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|   |               |                    |                   | Sheet                    | 40 of 43               |

| Item | Reason for change              | PG# | Modify List                                   | Date       | Phase |
|------|--------------------------------|-----|---|------------|-------|
| 1    | RT8203 crosstalk issue         | 37  | add PC121 and 0.1uF                           | 2007/05/24 | SI    |
| 2    | PU6 pin8 add a resistor to GND | 38  | add PR160 100K_ohm                            | 2007/05/24 | SI    |
| 3    | remove PL15                    | 36  | remove PL15                                   | 2007/06/12 | SI    |
| 4    | EMI request                    | 39  | add PC122,PC123,PC124,PC125,PC126,PC127,PC128 | 2007/07/23 | PV    |
| 5    |                                |     |   |            |       |
| 6    |                                |     |   |            |       |
| 7    |                                |     |   |            |       |
| 8    |                                |     |   |            |       |
| 9    |                                |     |   |            |       |
| 10   |                                |     |   |            |       |
| 11   |                                |     |   |            |       |
| 12   |                                |     |   |            |       |
| 13   |                                |     |   |            |       |
| 14   |                                |     |   |            |       |
|      |                                |     |   |            |       |

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SizeCustom

Document Number

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## Version change list (P.I.R. List)

## Power section

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| Item | Reason for change                             | PG#   | Modify List   | Date       | Phase |
|------|---|-------|---|------------|-------|
| 1    | EC team request                               | 32    | ACIN add 100P (C505) to GND   | 2007/05/30 | SI    |
| 2    | Change Board ID                               | 32    | R407 from 0 Ohm to 8.2K,R405 install 100K   | 2007/05/30 | SI    |
| 3    | USB power switch fail                         | 29    | U23 & U17 change pin 4 from SLP_S5# to SYSON#   | 2007/05/30 | SI    |
| 4    | FAN use voltage control                       | 4     | del U2,Q1;add U24,C13 for 3 pin FAN   | 2007/05/30 | SI    |
| 5    | USB JP24 fail                                 | 29    | Change pin define   | 2007/05/30 | SI    |
| 6    | Speaker output fail                           | 28    | Add R457,R458,R459 for Line_out   | 2007/05/30 | SI    |
| 7    | MS Pro fail                                   | 26    | Add MS_D1,MS_D2,MS_D3 net   | 2007/06/06 | SI    |
| 8    | WLAN LED fail when disable WLAN               | 30    | Add R232 pull high +5VS   | 2007/06/06 | SI    |
| 9    | +3VALW leakage                                | 30    | Del R387  | 2007/06/06 | SI    |
| 10   | Capacitor board fail                          | 32    | Add net CAP_RESET for Capacitor board reset   | 2007/06/06 | SI    |
| 11   | XDP fail                                      | 15    | XDP clock share in robeson card   | 2007/06/06 | SI    |
| 12   | LAN power consumption is too large when S3    | 24    | Add Q22   | 2007/06/14 | SI    |
| 13   | RJ11' cap is duplicate MDC module.            | 25    | Delete C378,C379  | 2007/06/14 | SI    |
| 14   | Reverse some resister for tring ENE cap board | 30 32 | Add R460~R468,R451  | 2007/06/14 | SI    |
| 15   | +LCDVDD over current when diplay.             | 17    | Change R163 from 47K to 100K<br>Change C248 from 0.1U to 0.22U  | 2007/06/21 | SI    |
| 16   | LAN fail                                      | 24    | Change JP14 pin define  | 2007/06/06 | SI    |
| 17   | WLAN LED (Amber led) issue                    | 30    | WLAN LED need change from +5VS to +3VS  | 2007/07/23 | PV    |
| 18   | 030 project Bluetooth module issue            | 29    | Swap pin5 & pin7  | 2007/07/23 | PV    |
| 19   | change Cap board LED supply voltage           | 30    | from +3VS to +5VS   | 2007/07/23 | PV    |
| 20   | CMOS timing can't reset                       | 19    | SHORT PAD (CLRP3) connect between +RTCVCC and GND   | 2007/07/23 | PV    |
| 20   | EMI issue (CPU core)                          | 5     | add C43 & C44 (330U)  | 2007/07/23 | PV    |
| 21   | EMI/ESD issue (XDO connector)                 | 4     | delete XDP connector  | 2007/07/23 | PV    |
| 22   | EMI/ESD issue (RJ11 connector)                | 25    | add 1000P at RJ11 RING & TIP  | 2007/07/23 | PV    |
|      |   |       | <div>Compal Electronics, Inc.</div> <div>TitlePWR PIR</div> <div>Size Custom Document NumberRev0.3</div> <div>Date: Tuesday, July 31, 2007Sheet 42 of 43</div>  |            |       |
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