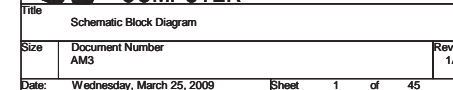


**VER : C3A**




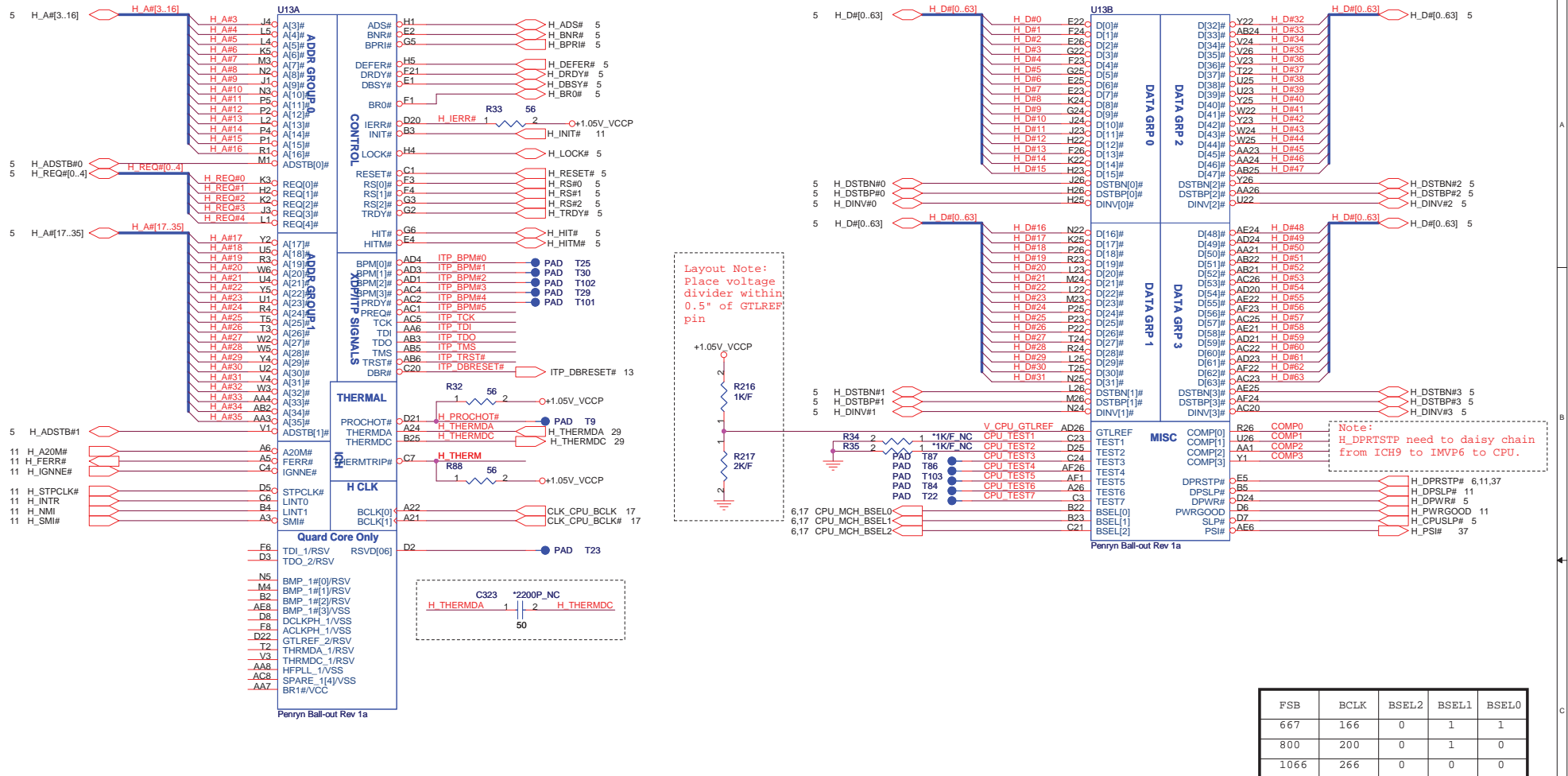
# Table of Contents

PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-4	Penryn
5-10	Cantiga
11-14	ICH9M
15-16	DDRII SO-DIMM(200P)
17	Clock Generator
18	LCD Conn.
19	CRT Conn
20	RTS5158
21	Express card
22	SIO (ITE8502)
23	FLASH/RTC/TPM
24	Mini Card / BT
25	USB
26	SATA Conn HDD and ODD
27	TP / KEYBOARD / FP
28	SWITCH /LED
29	FAN & Thermal
30	Audio CODEC(CX20583)/Phone Jack/Modem
31	LAN / TRANSFORM
32	System Reset Circuit
33	Battery Selector & Charger
34	1.05VCCP / 1.5VRUJN
35	DDR2 1.8VSUS, 0.9V
36	MAX17020 (+5V/+3V ALW)
37	MAX17021 V_CORE
38	RUN Power Switch
39	DCIN,Batt
40	PAD& SCREW
41	EMI CAP
42	SMBUS BLOCK
43	Power Block Dianram

# Power States

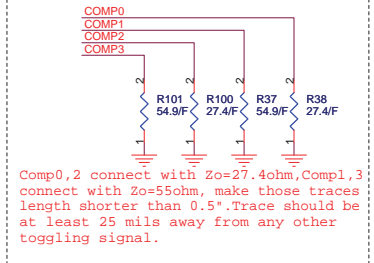
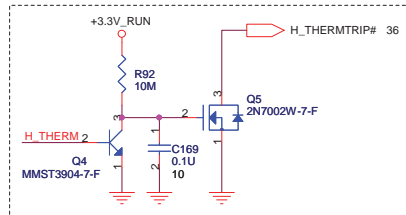
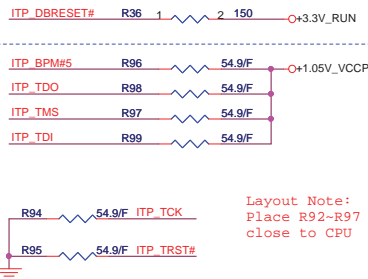
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,46,48,49,51,52,56	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,26,30,37,38,43,48,49,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,53	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,18,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	14,18,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,53,56	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,48,56	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,51,56	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+PBATT	+10V~+17V		MAIN BATTERY	CHG_PBATT	
+SBATT	+10V~+17V		SECOND BATTERY	CHG_SBATT	

GND PLANE	PAGE	DESCRIPTION
 GND	ALL	



### Populate ITP700Flex for bringup

Change ITP\_DBRESET# design circuit No2 1/5

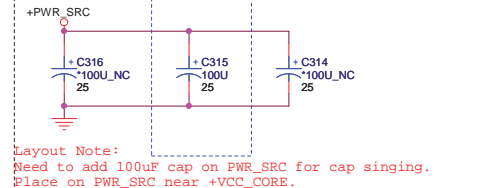
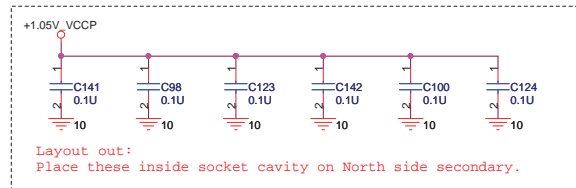
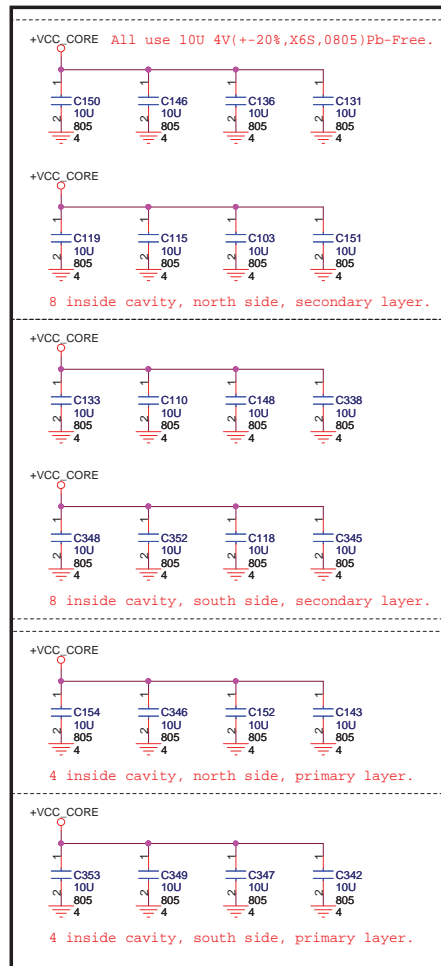


**QUANTA COMPUTER**

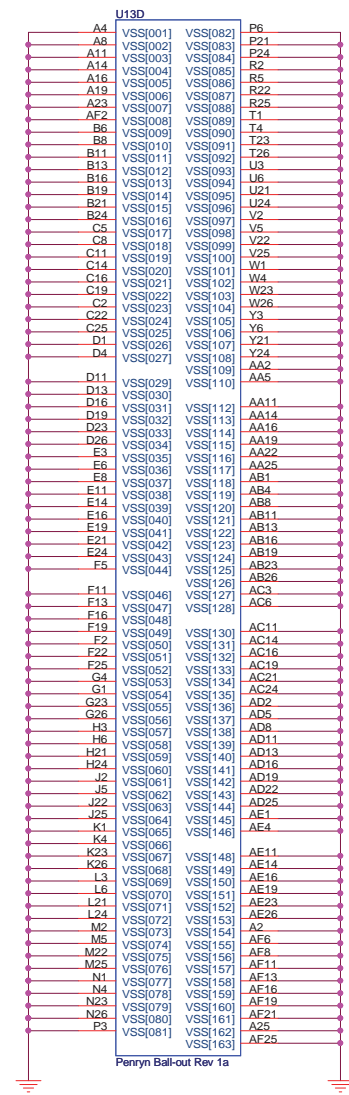
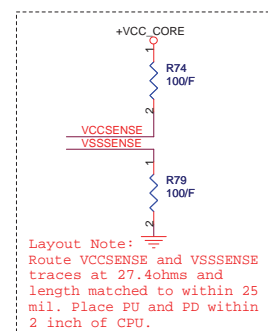
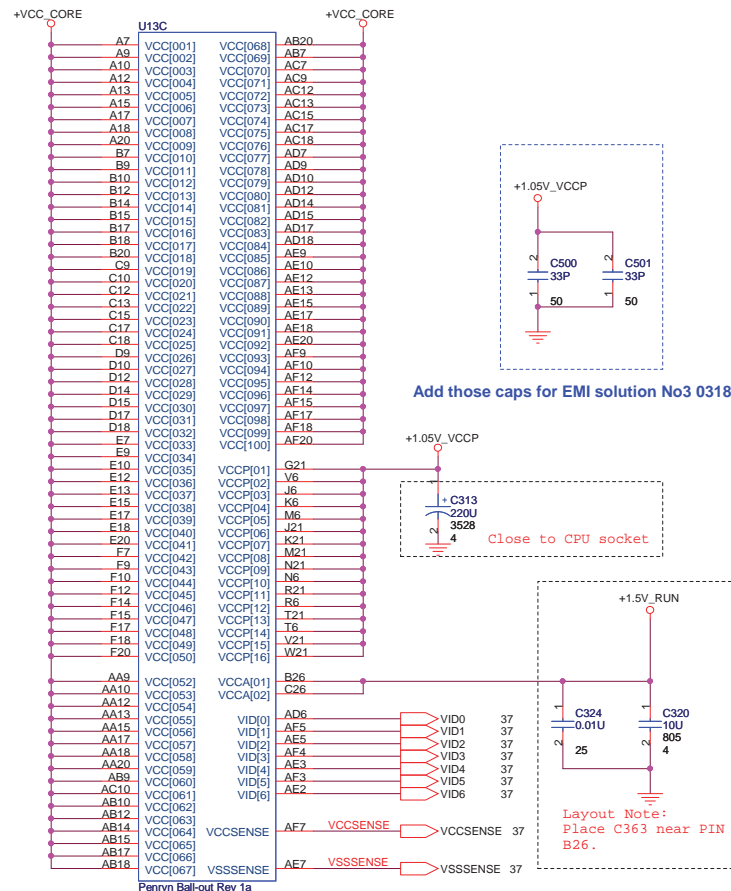
Title: Penryn Processor (HOST BUS)

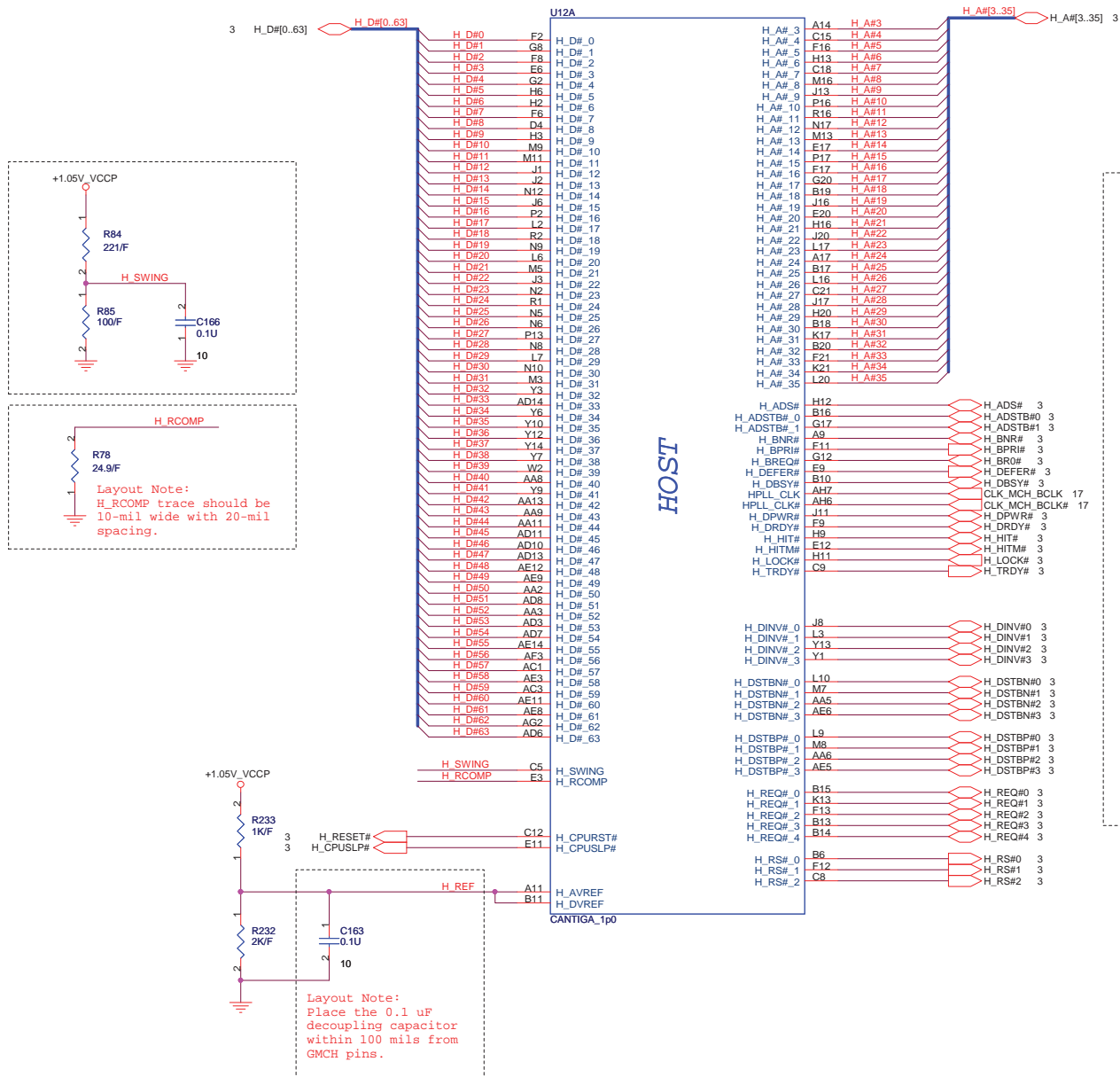
Size: Document Number AM3 Rev 1A

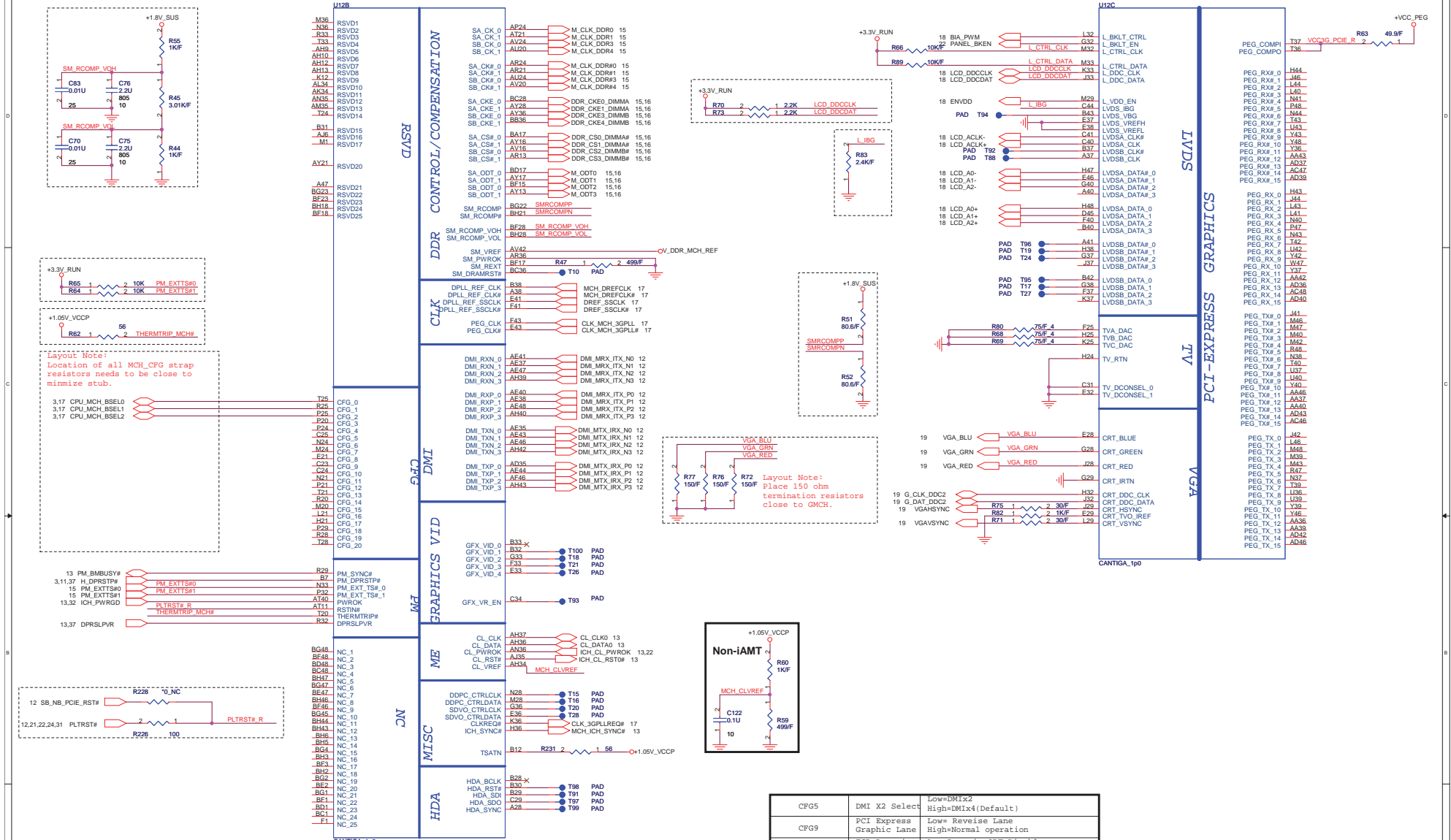
Date: Wednesday, March 25, 2009 Sheet 3 of 45



Add C315 for Acoustic No1 0220

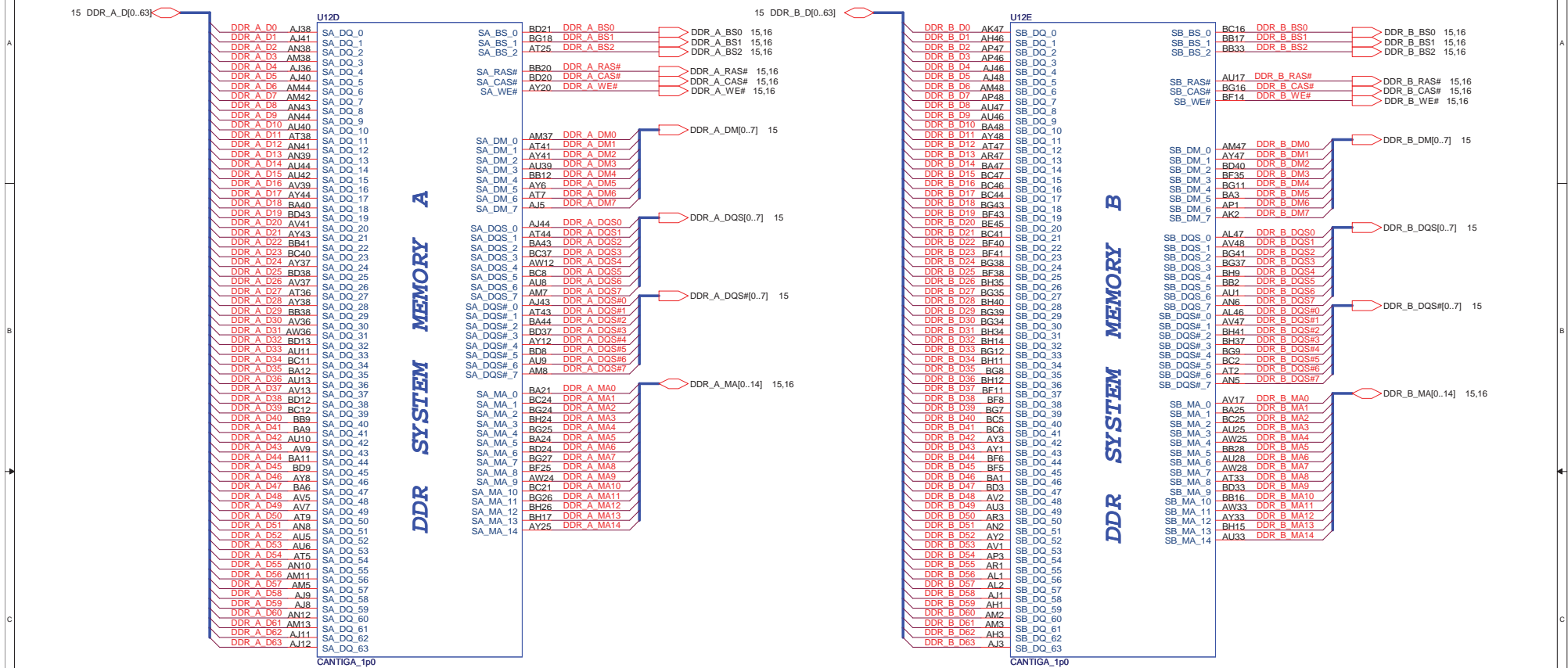






CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCI-E Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (default). High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present

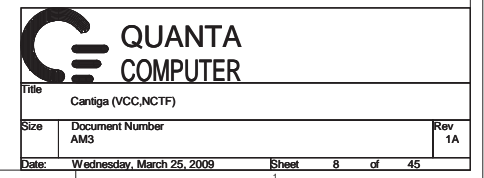




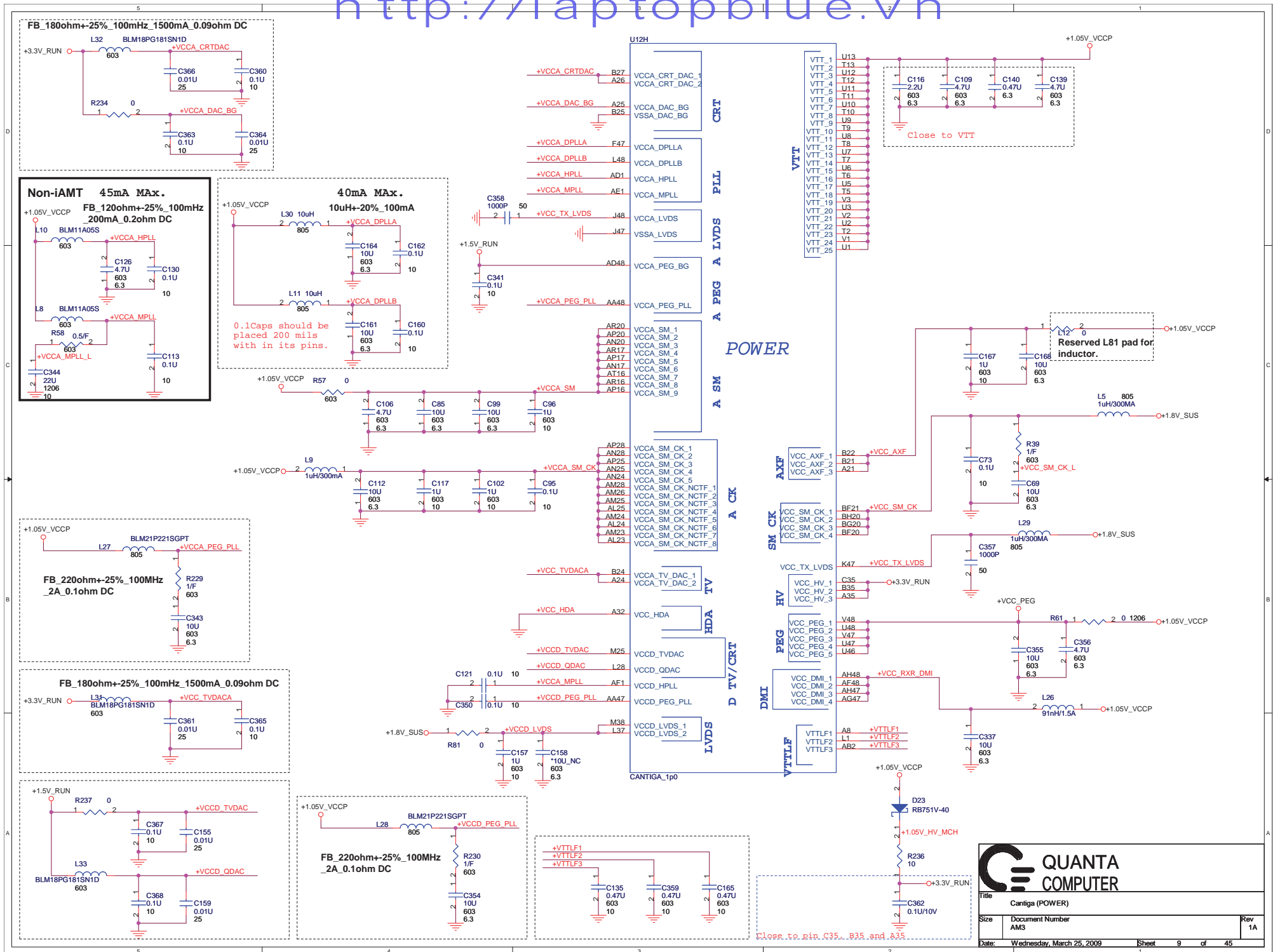
CANTIGA\_1p0

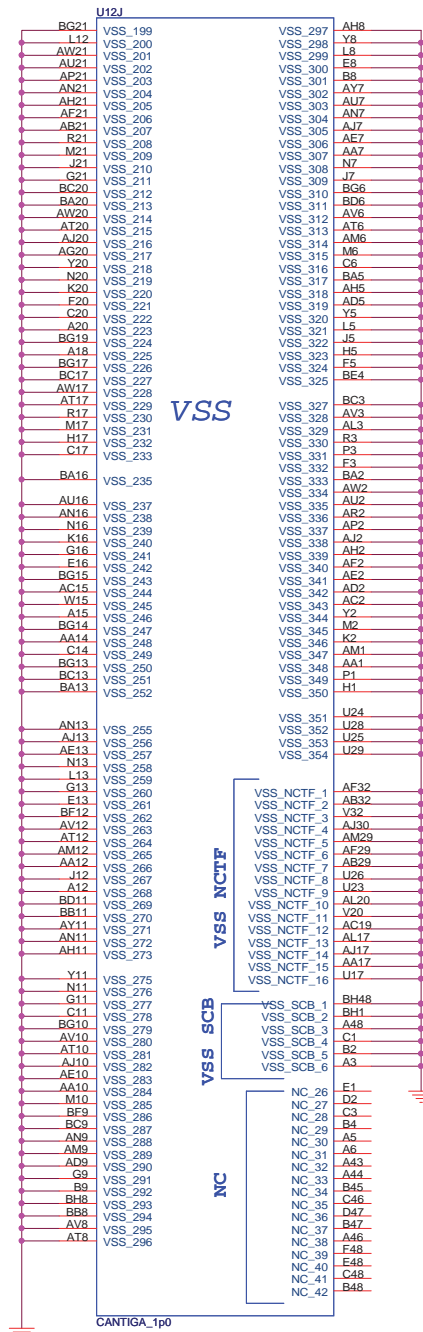
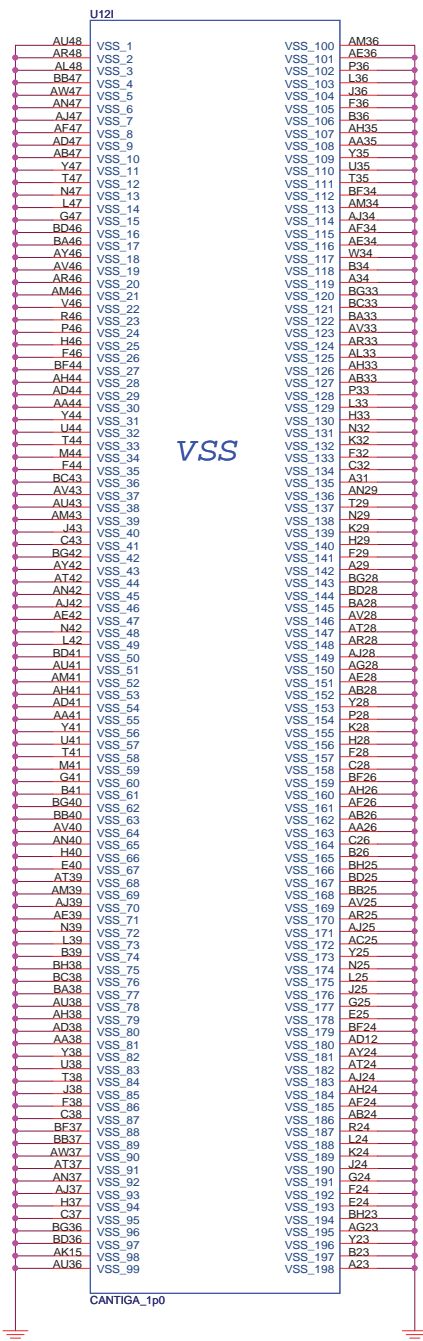
CANTIGA\_1p0

Title Cantiga (DDR2)		
Size	Document Number AM3	Rev 1A
Date:	Wednesday, March 25, 2009	Sheet 7 of 45



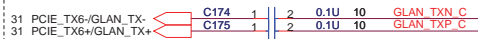






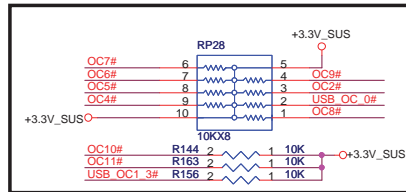


Place TX DC blocking caps close ICH9.



Boot BIOS Strap			
		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

Update USB OC circuit No24 11/17



#### MiniWWAN



#### Express Card



#### Giga Bit LOM



#### U16D

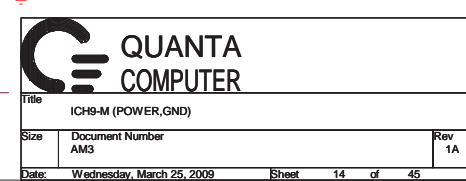


#### Direct Media Interface

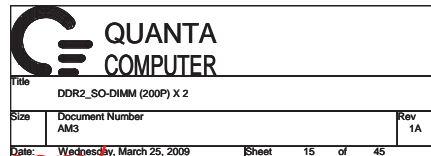


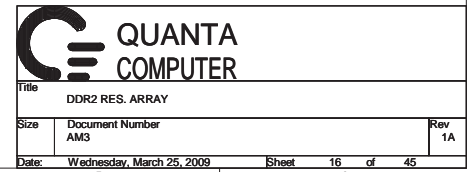
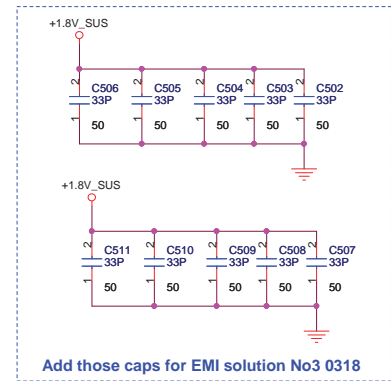





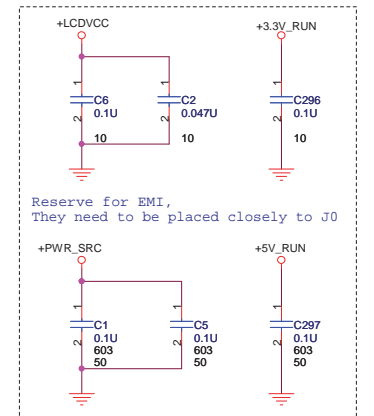
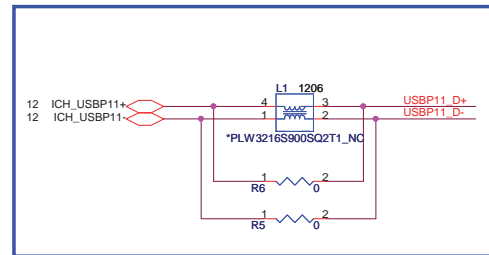
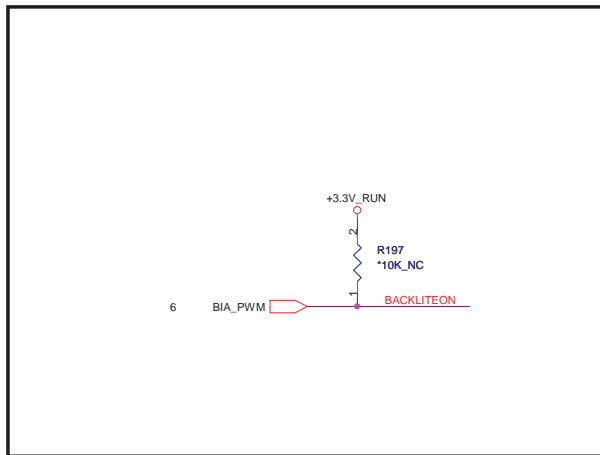
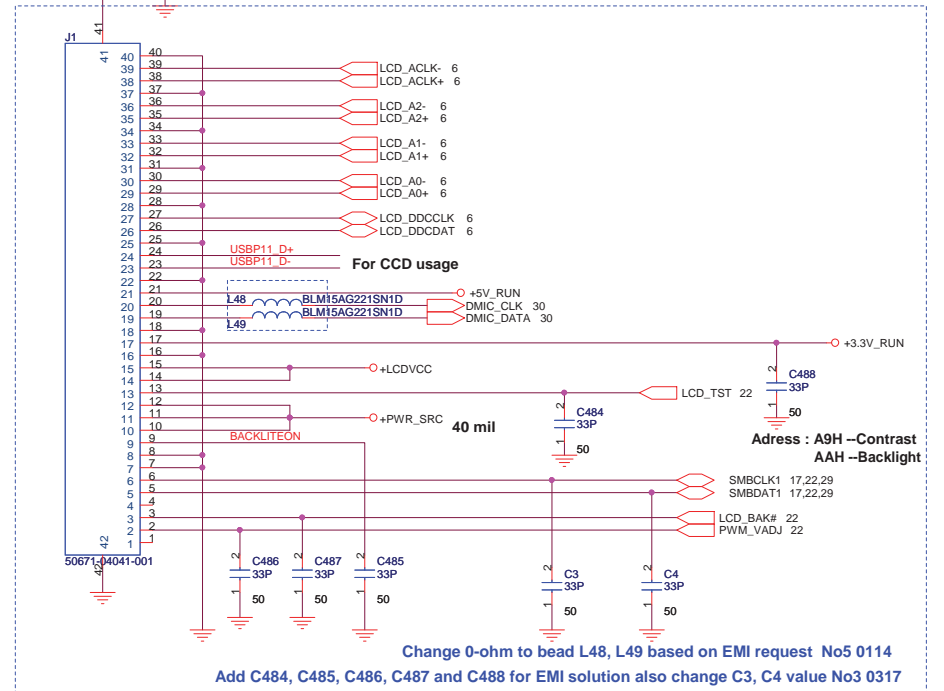
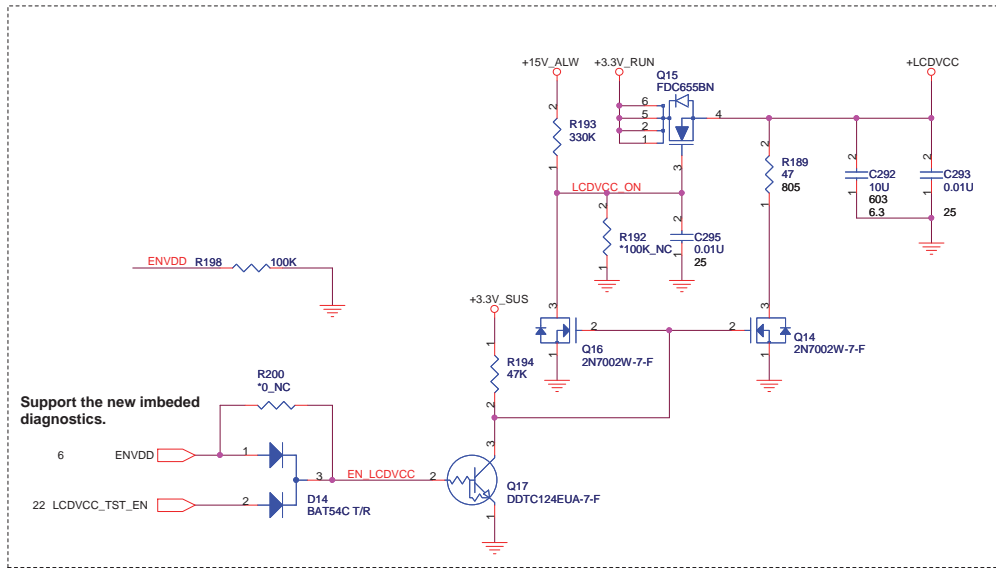


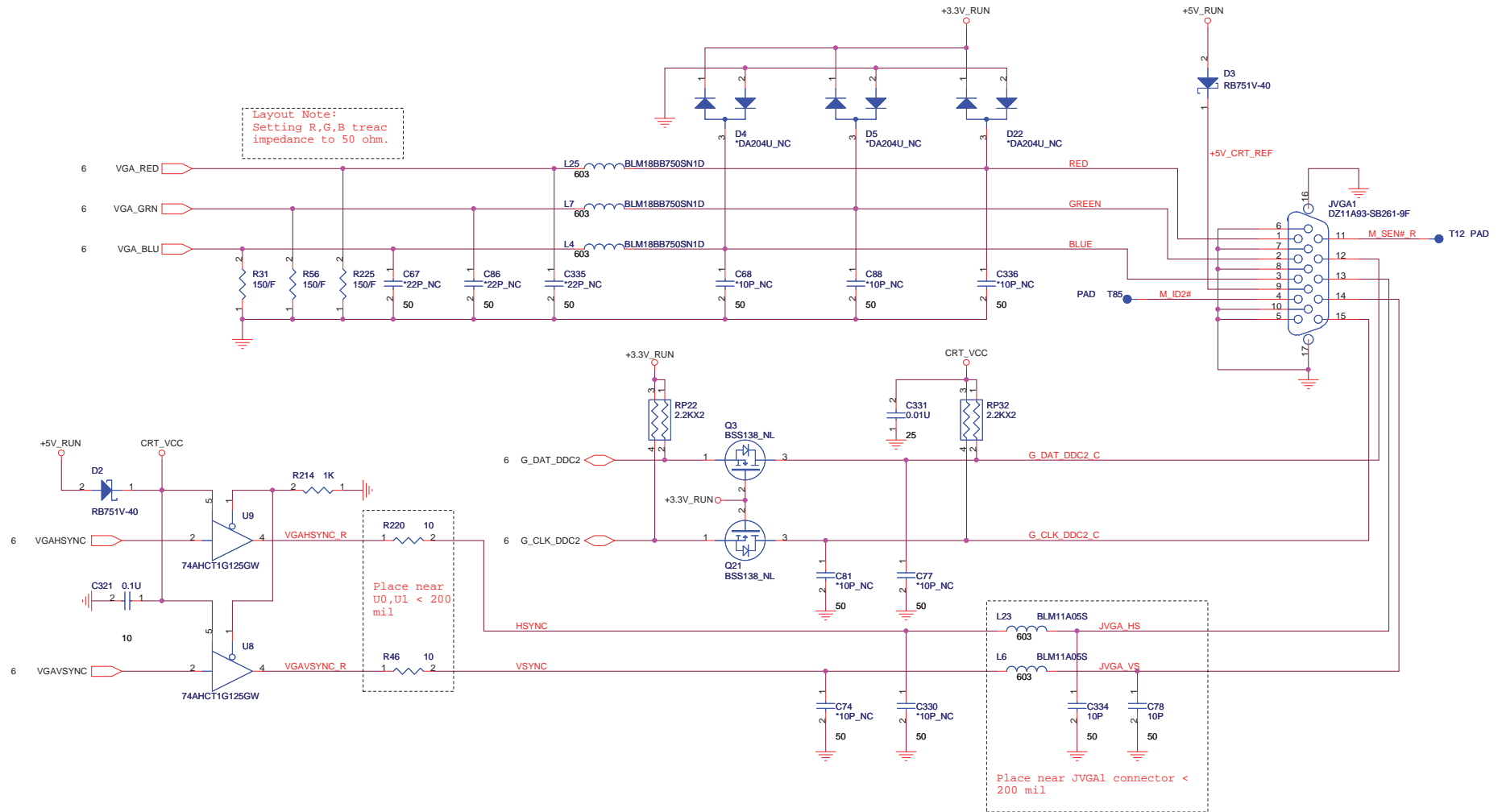


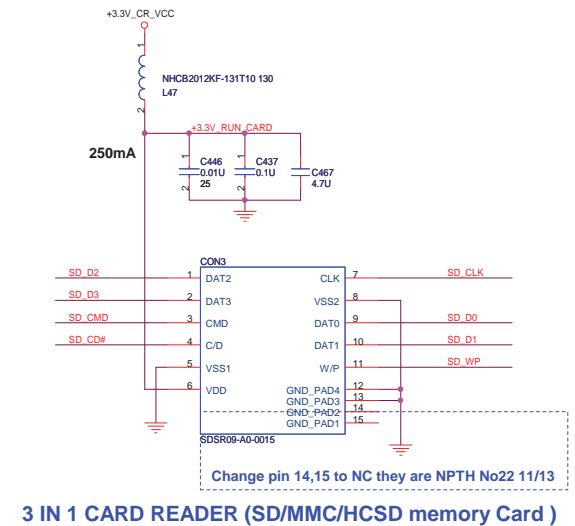




 <div> <h1>QUANTA</h1> <h2>COMPUTER</h2> </div>				
Title				
CLOCK GENERATOR				
Size	Document Number AM3			Rev 1A
Date:	Wednesday, March 25, 2009	Sheet	17	of 45

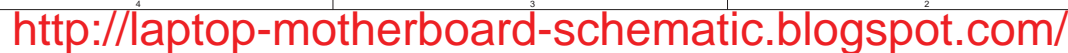




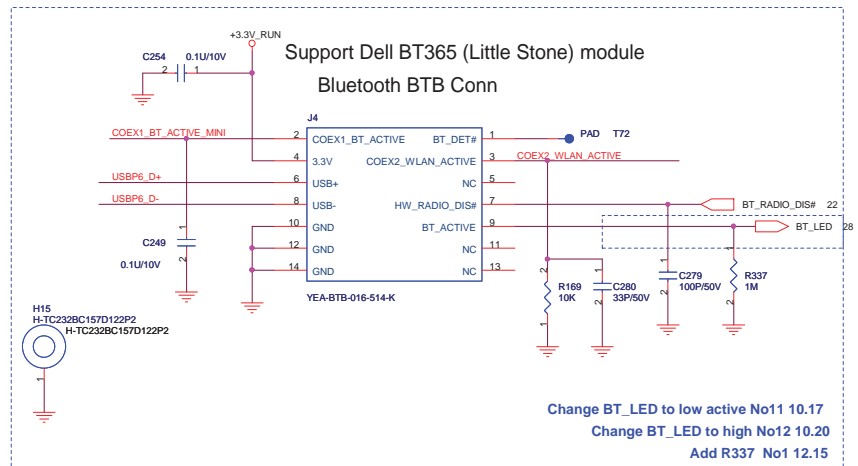
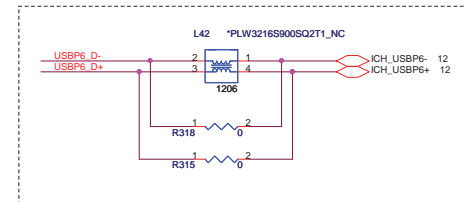


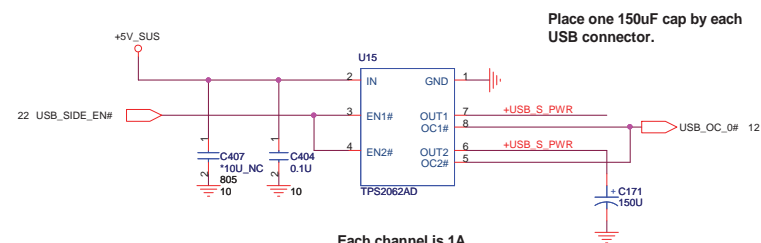
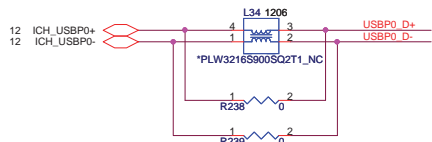
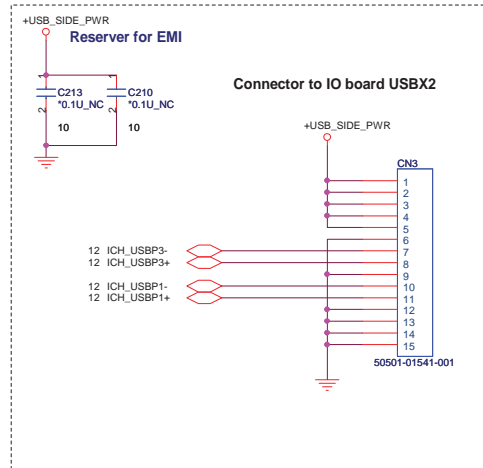
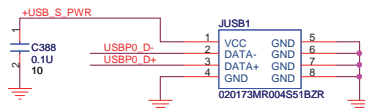
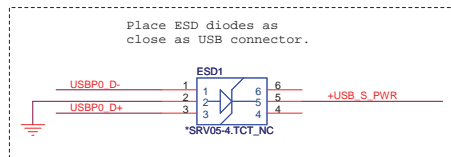


<http://laptop-motherboard-schematic.blogspot.com/>

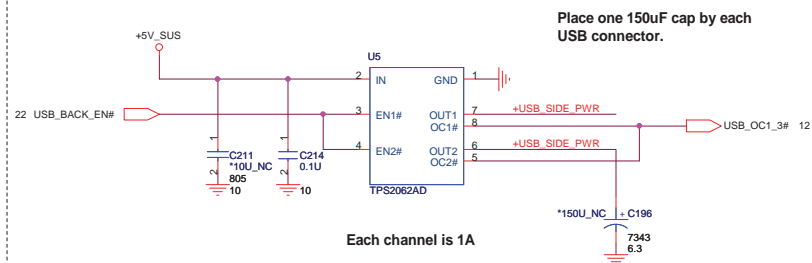


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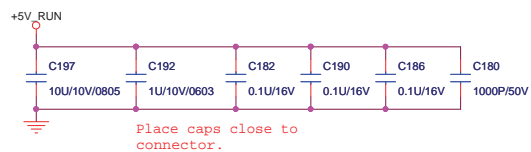
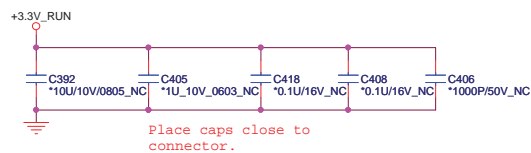
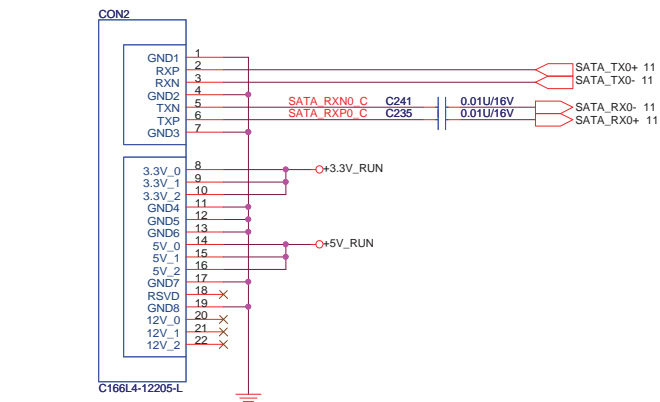


Update USB OC circuit No24 11/17  
Change C171 PN No1 0220

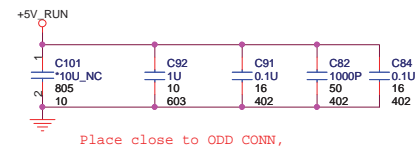
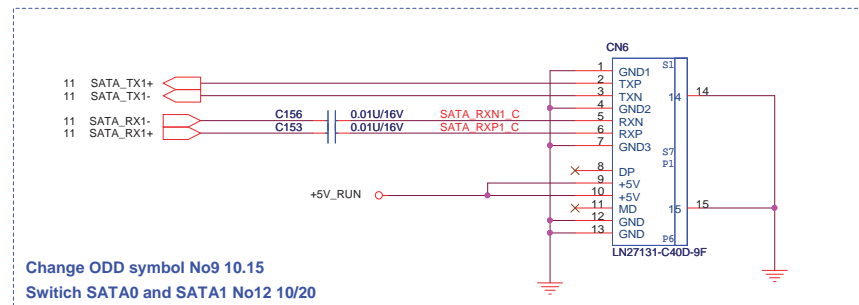


Move 2062 from IO to MB No13 10.21

## SATA HDD Connector.

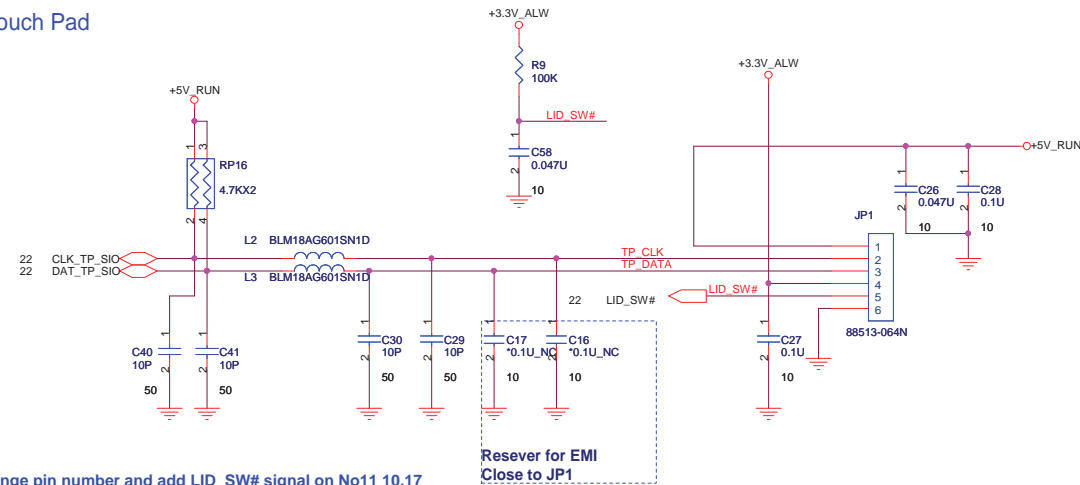


## SATA ODD Connector.





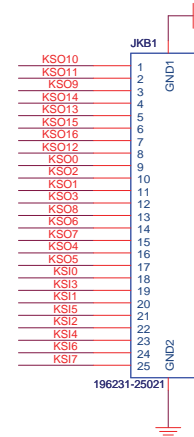
## Touch Pad



Change pin number and add LID\_SW# signal on No11 10.17  
 Change pin define No14 10/22  
 Change touch pad pn and footprint No14 10/22  
 Change Touch pad pin define, avoiding power and ground pin close to each other

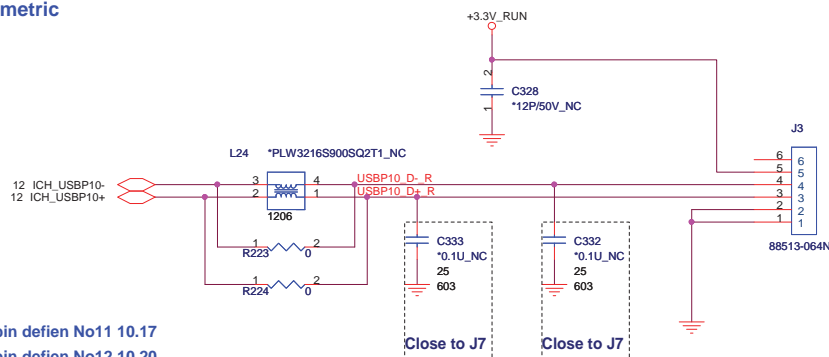
## KEYBOARD CONNECTOR

22 KSO[0..16]  
 22 KSI[0..7]

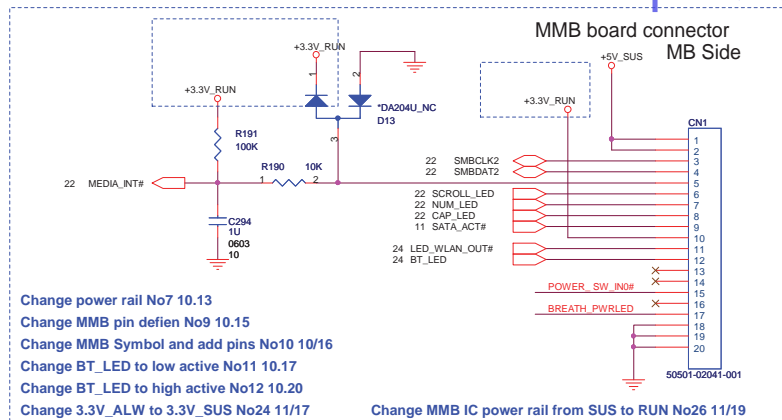


Change pin define No14 10/22  
 Change pin define No22 11/13

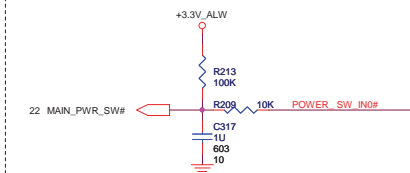
## Biometric



Change pin define No11 10.17  
 Change pin define No12 10.20  
 Change touch pad pn and footprint No14 10/22  
 Change FP pin define No15 10/24  
 Change FP pin define No23 11/14



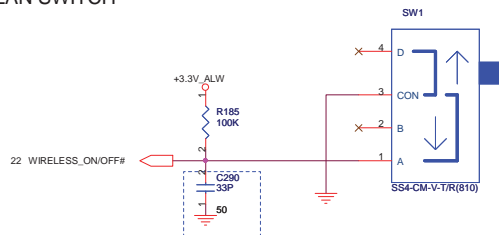
#### Power Switch



#### Blacktop Switch

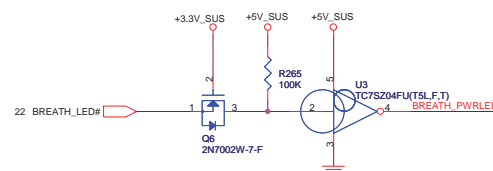
Add Blacktop switch function No9 10/15  
 Del Blacktop switch function No19 11/06  
 Add Blacktop switch function No19 11/06  
 Del Blacktop switch function No23 11/14

#### WLAN SWITCH



Change C290 PN and size No3 0318

#### Power & Suspend.



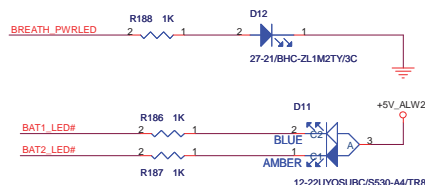
#### Battery status.



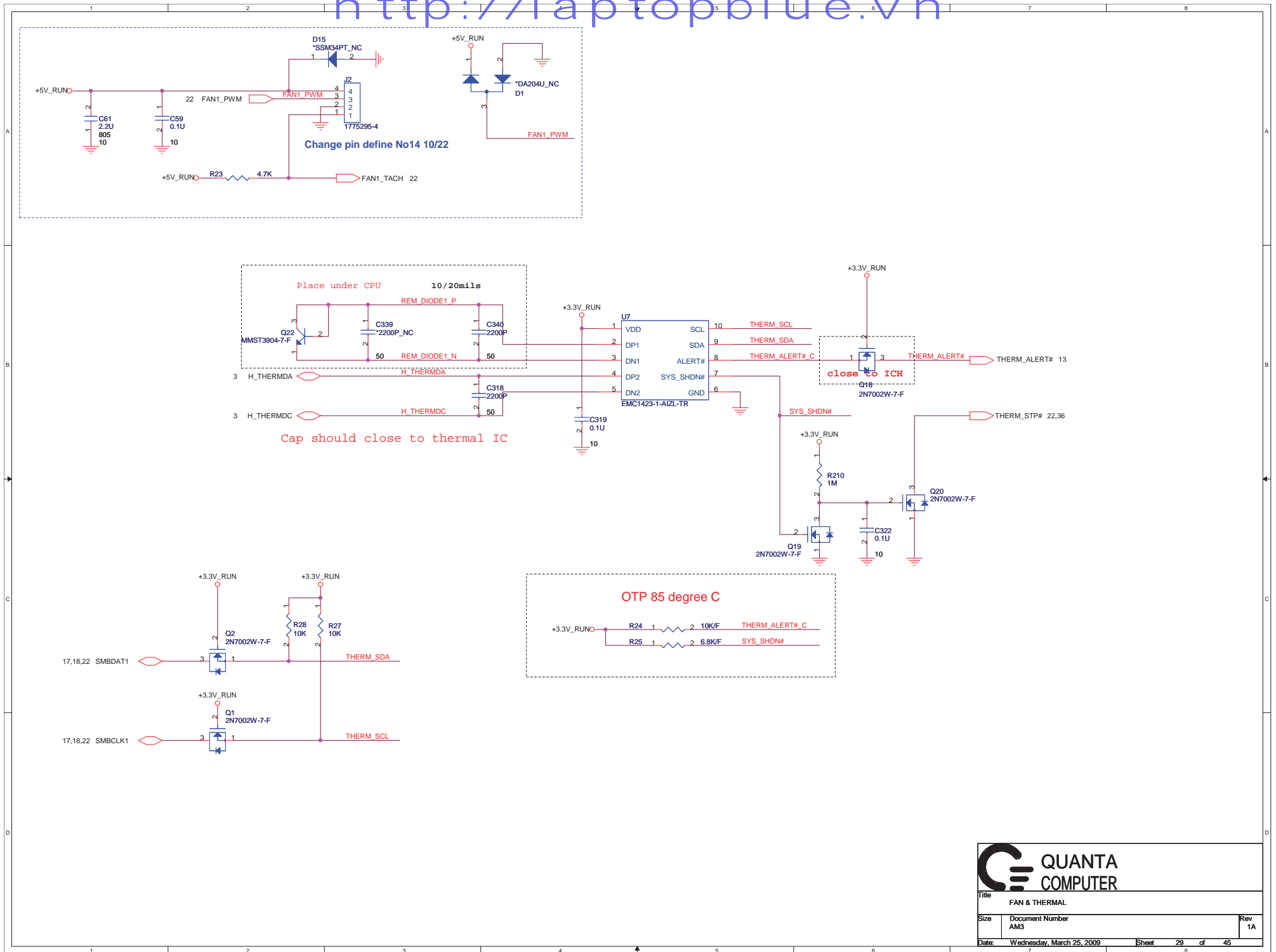
Change Battery setting NO20. 11/11  
 Change Battery setting NO24. 11/17

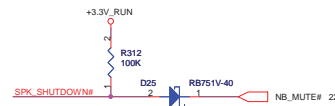
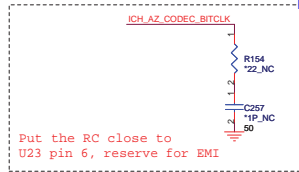
Add WLAN LED on MB NO7. 10/13  
 Del WLAN LED on MB No9 10/15

#### Right angle LED



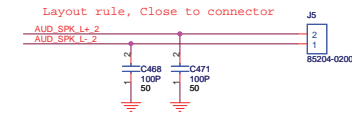
Change Battery setting NO20. 11/11  
 Change Battery setting NO24. 11/17  
 Change R186., R187 and R188 value NO6. 03/24





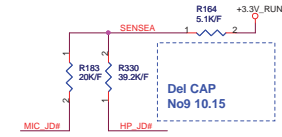
Add PC beep for system error circuit No9 10.14  
Del PC beep No9 10.15

#### Speakers conn



Add ESD2 for ESD concern No6 1/19  
Remove ESD2 for ESD concern No8 1/21

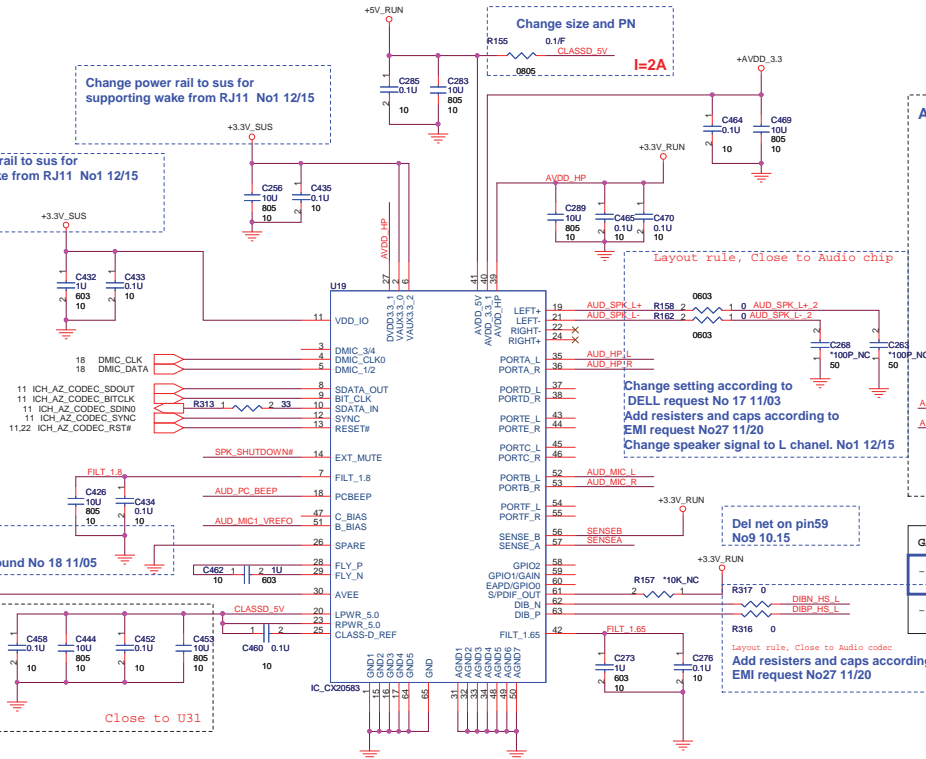
#### Jack Sense

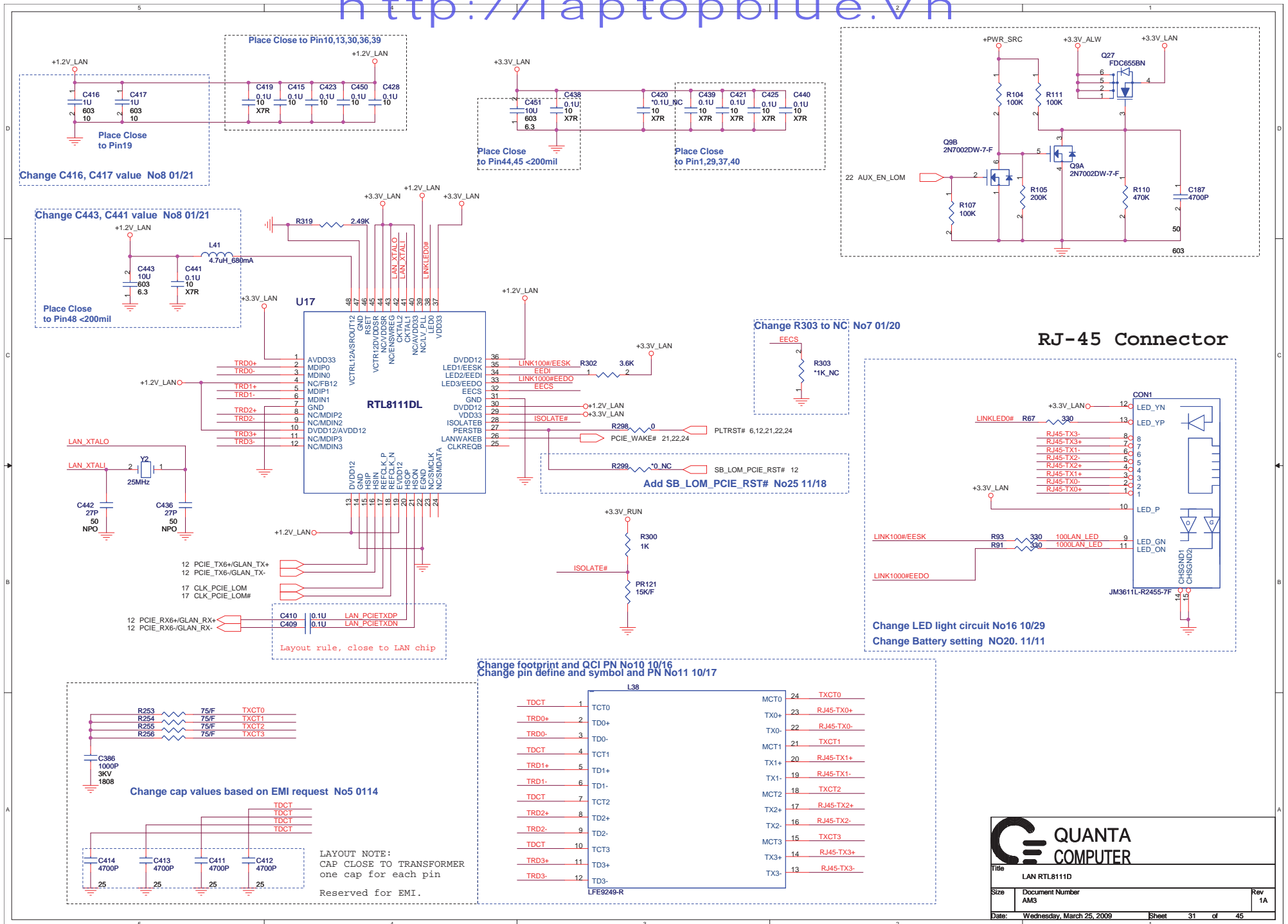


### AUDIO CODEC

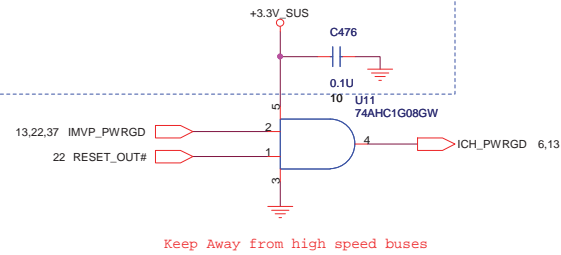
Change power rail to sus for supporting wake from RJ11 No1 12/15

Change power rail to sus for supporting wake from RJ11 No1 12/15

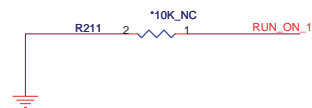
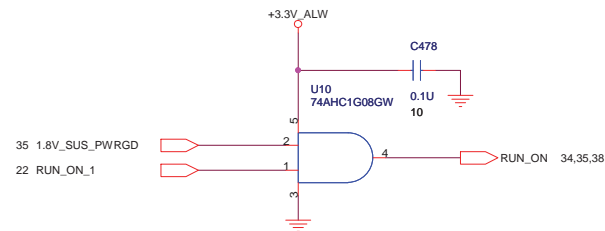
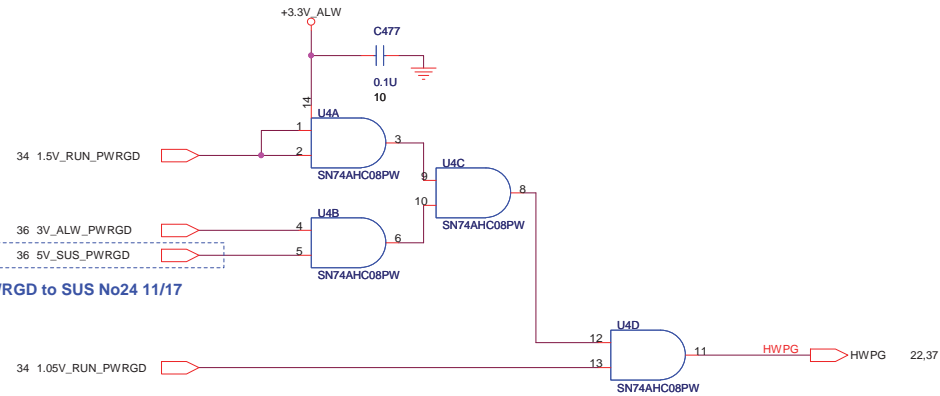





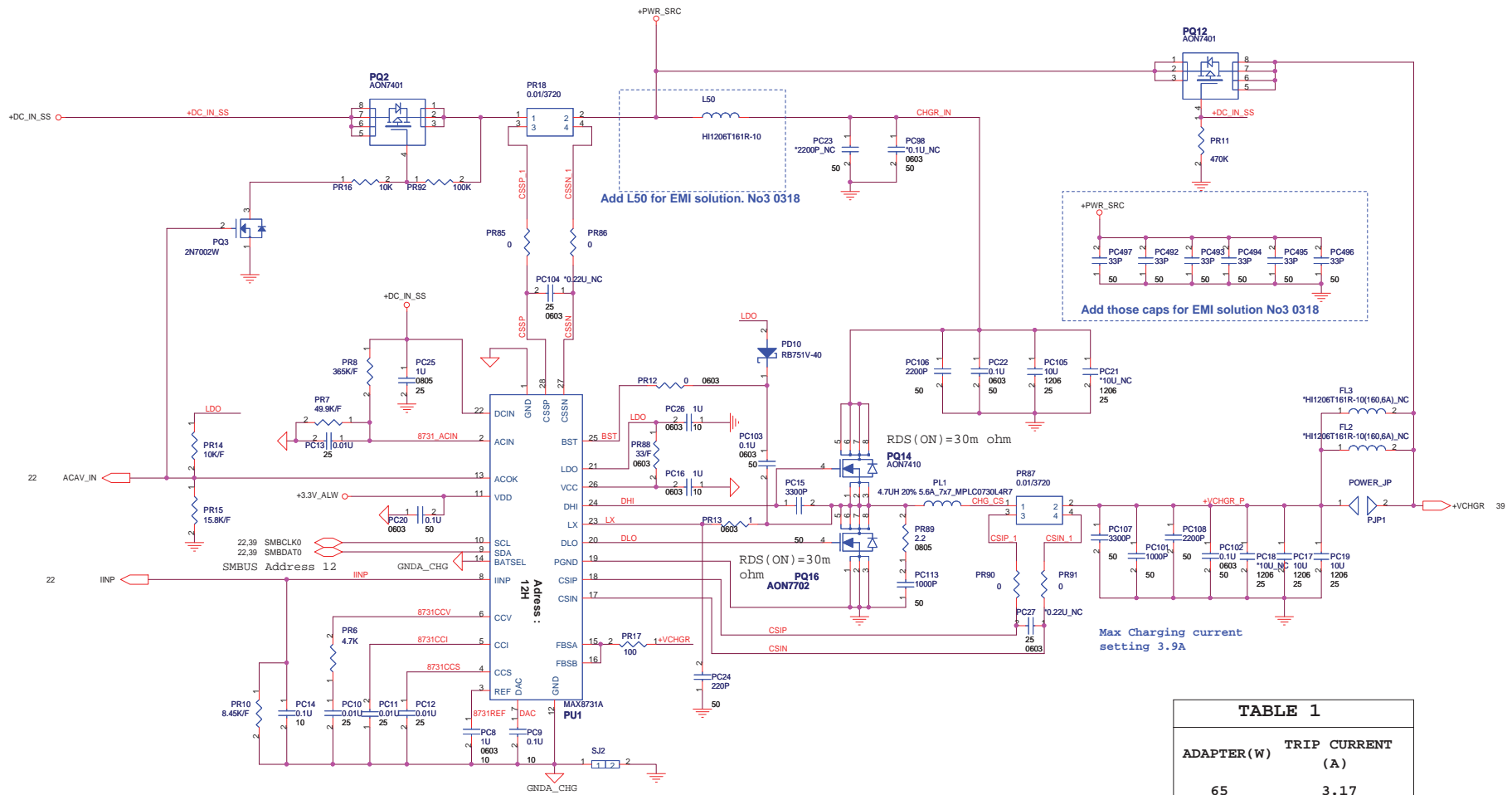
Change power source No22 11/13  
Remove 0-ohm resistor and 3.3V\_ALW power rail No3 01/06



Change from 5V\_ALW\_PWRGD to SUS No24 11/17



 <b>QUANTA COMPUTER</b>		
Title System Reset Circuit		
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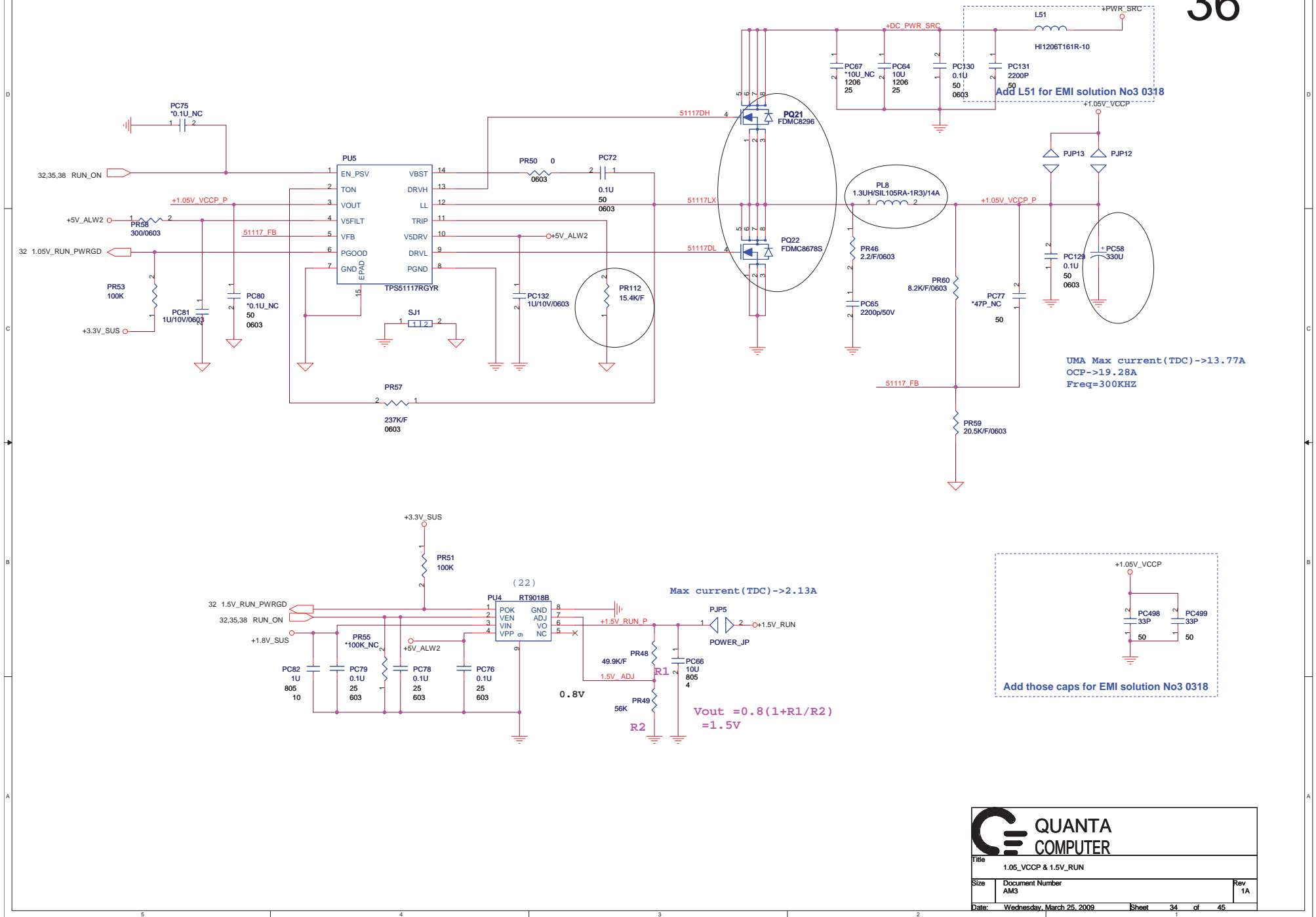
ADAPTER (W)	TRIP CURRENT (A)
65	3.17
90	4.43
130	6.43
150	7.43
200	9.75
230	(see note3)



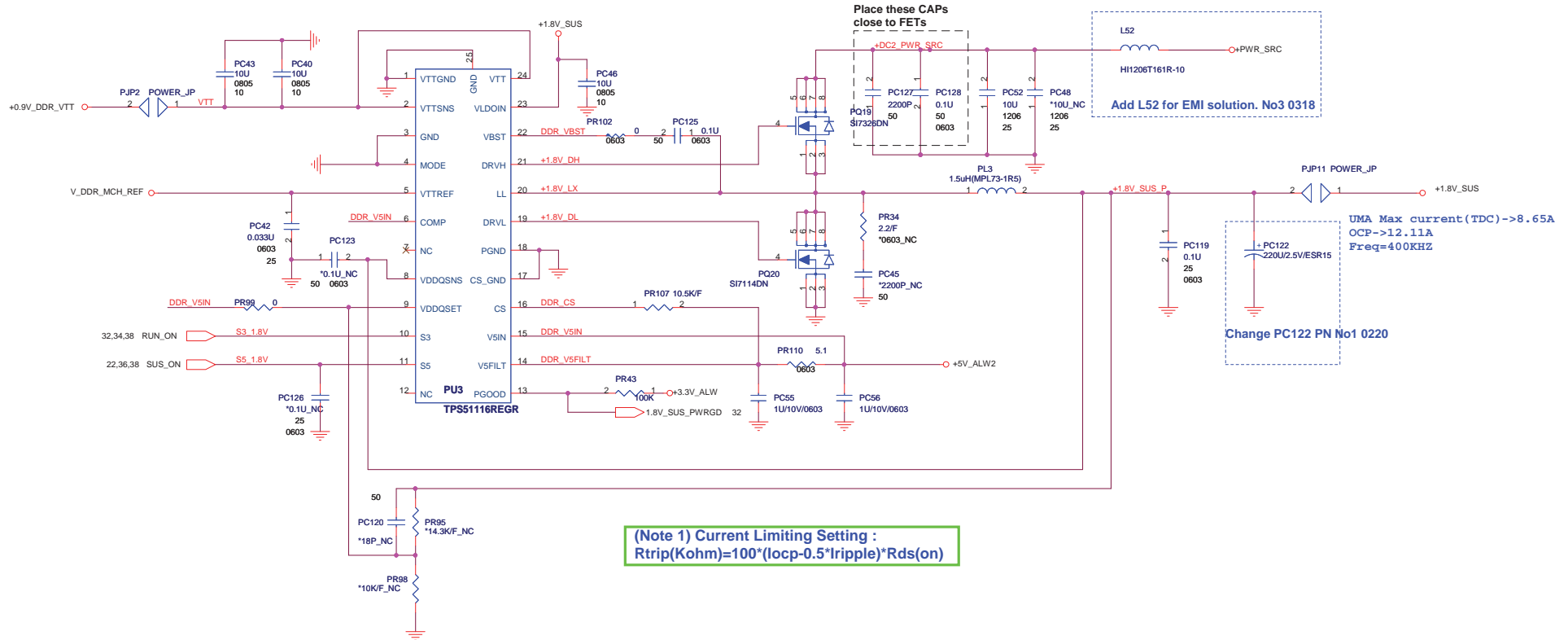
QUANTA  
COMPUTER

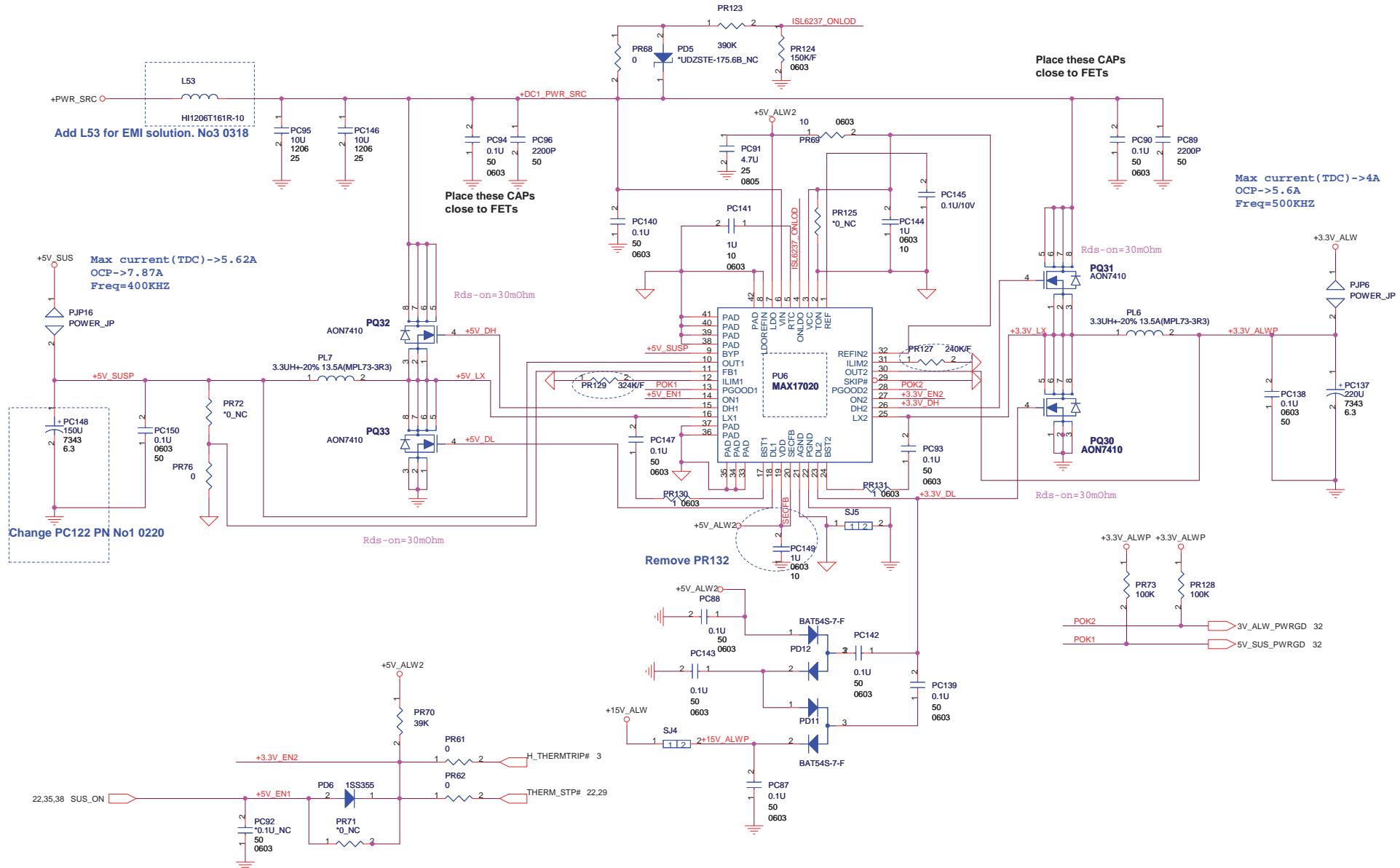
Title: Charger (MAX8731A)		
Size: Document Number: AM3	Rev: 1A	
Date: Wednesday, March 25, 2009	Sheet: 33	of 45

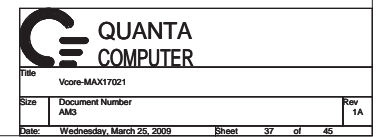


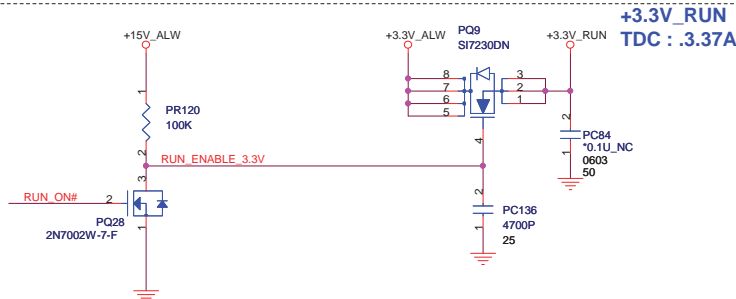
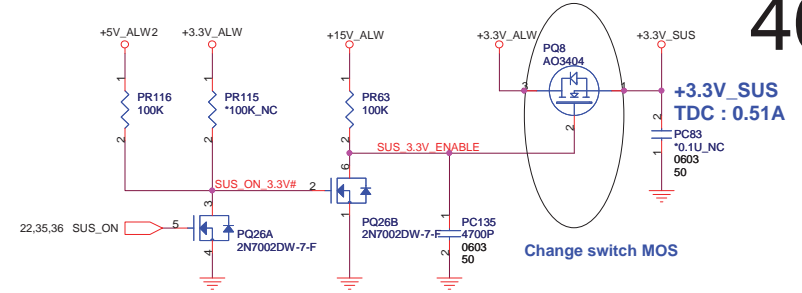
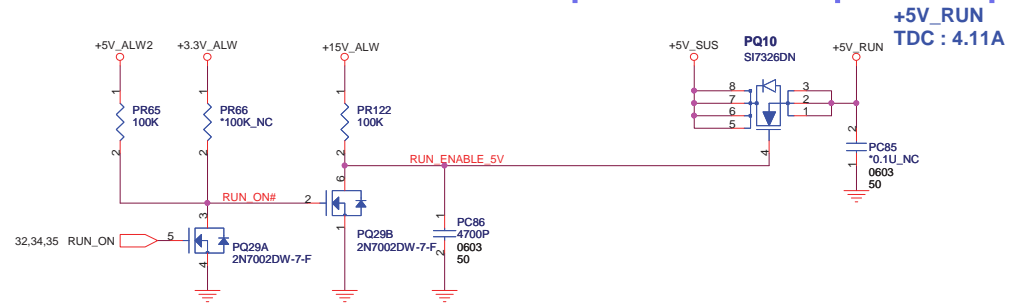


<b>QUANTA COMPUTER</b>	
Title: 1.05_VCCP & 1.5V_RUN	
Size: AM3	Document Number: Rev 1A
Date: Wednesday, March 25, 2009	Sheet 34 of 45

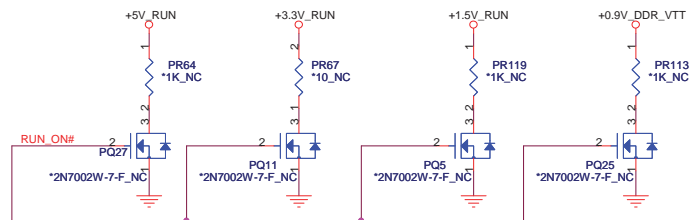




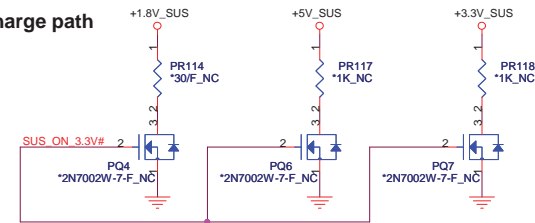




#### Reserve discharge path

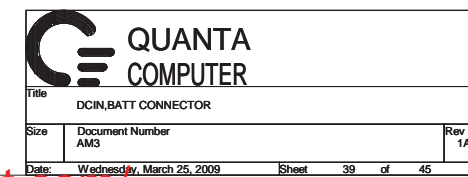


#### Reserve discharge path



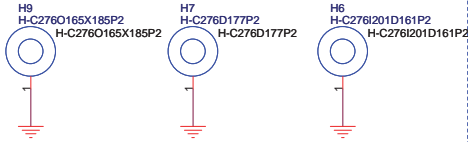
QUANTA  
COMPUTER

Title		
RUN POWER SW		
Size	Document Number	Rev
AM3		1A
Date:	Wednesday, March 25, 2009	Sheet 38 of 45

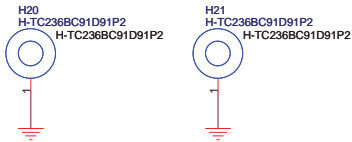


Create hole footprints No9 10.15

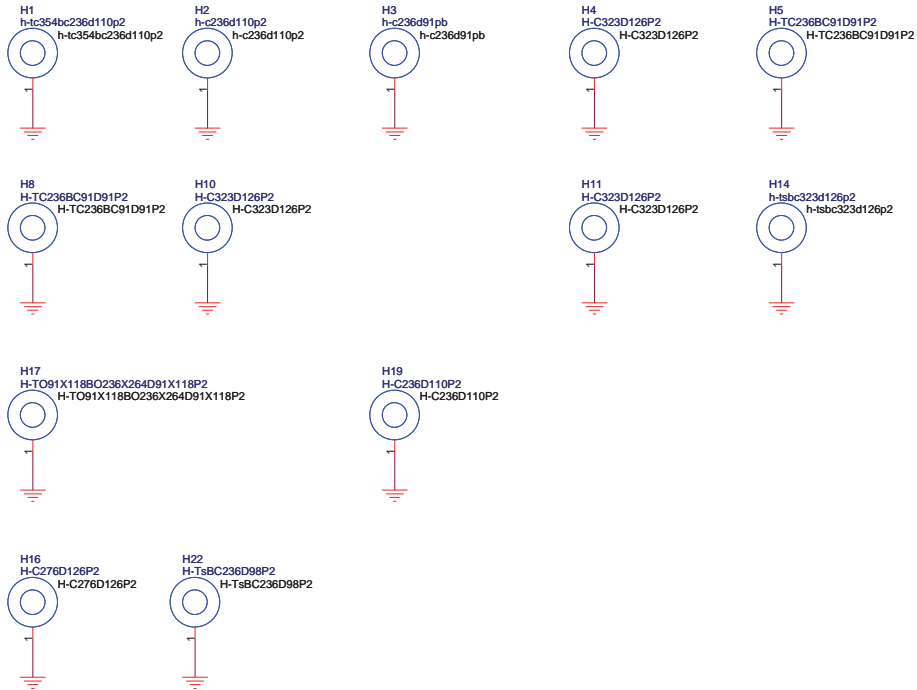
For CPU use



For ODD use



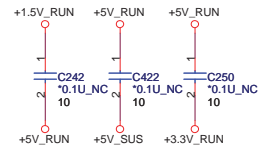
Add Screw hole No6 0119





Reserved for EMI.

### Stitching caps for PCI bus.



### Stitching caps for PCI EMC.

