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Schematic Document

Crestline + ICH8

2007 / 11 / 14 Rev:0.2

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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	Cover Sheet
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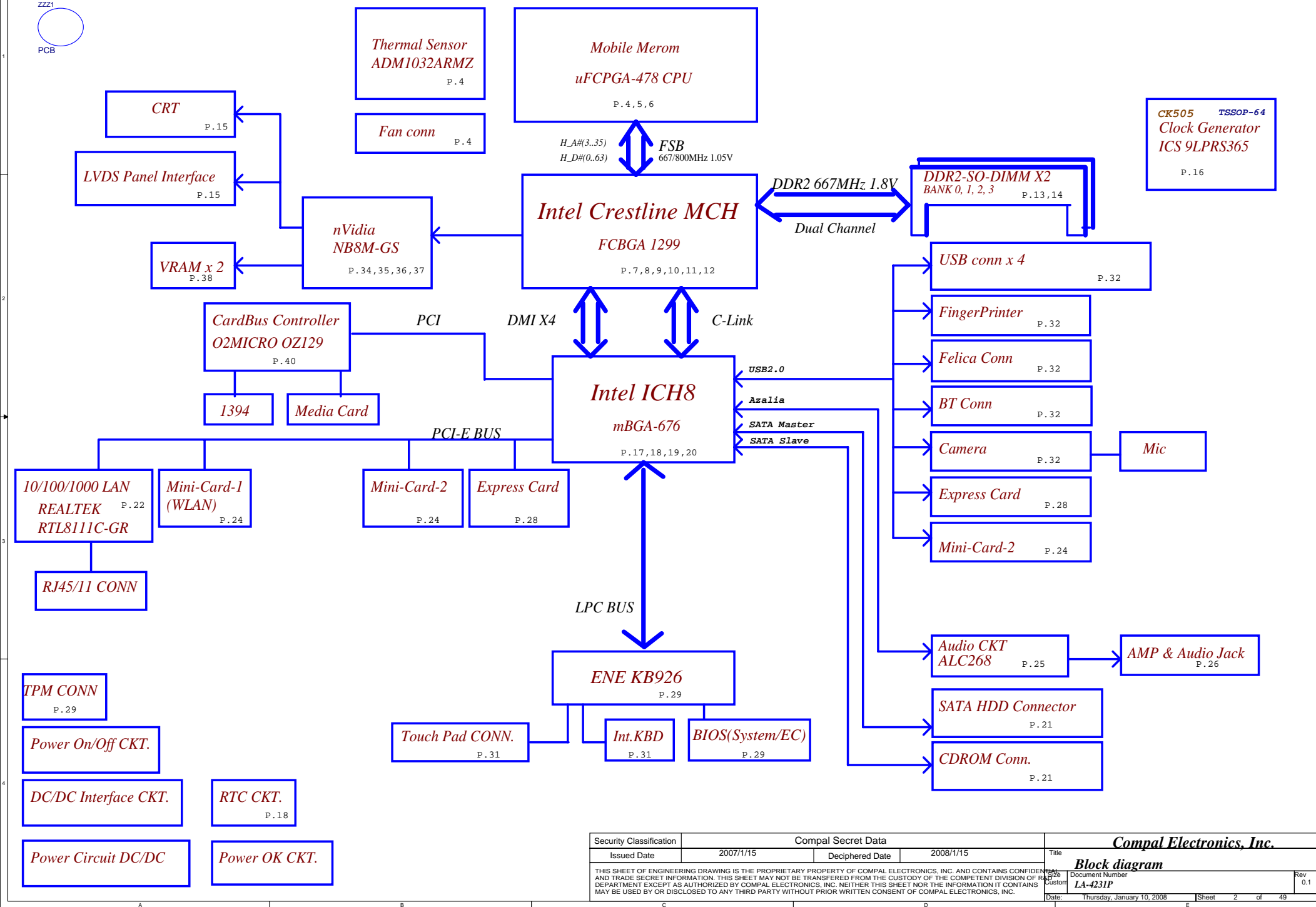
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File Name : LA-4231P

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PCB



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	Block diagram
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O MEANS ON X MEANS OFF

power plane State	+B	+5VALW +3VALW	+3V +1.8V	+5VS +3VS +1.8VS +1.5VS +1.25VS +CPU_CORE +VCCP	CLOCK
S0	O	O	O	O	O
S3	O	O	O	X	O
S5 S4/AC	O	O	X	X	O
S5 S4/ Battery only	O	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

O MEANS ON

X MEANS OFF

S3 : STR

S4 : STD

S5 : SOFT OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD21	0	PIRQE/PIRQF/PIRQG

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b?	ADM1032	4D
EEPROM(24C16/02)	1010 000X b?		
(24C04)	1011 000Xb?		

EC SM Bus2 address

Device	Address
ADM1032	4D

ICH7 SM Bus address

Device	Address
Clock Generator (ICS IC59LPR310)	1101 001Xb?
DDRII DIMM0	1001 000Xb?
DDRII DIMM2	1001 010Xb?

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	-VAL#	+V	+VS	CLOCK
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

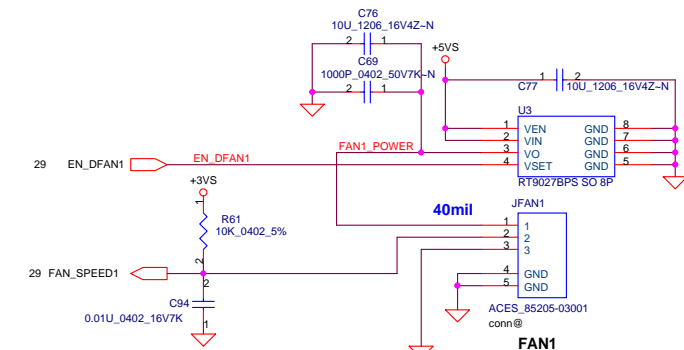
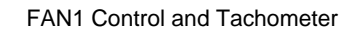
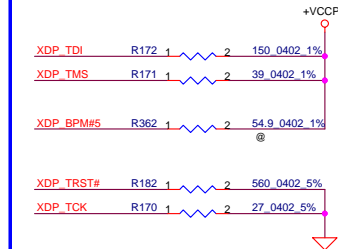
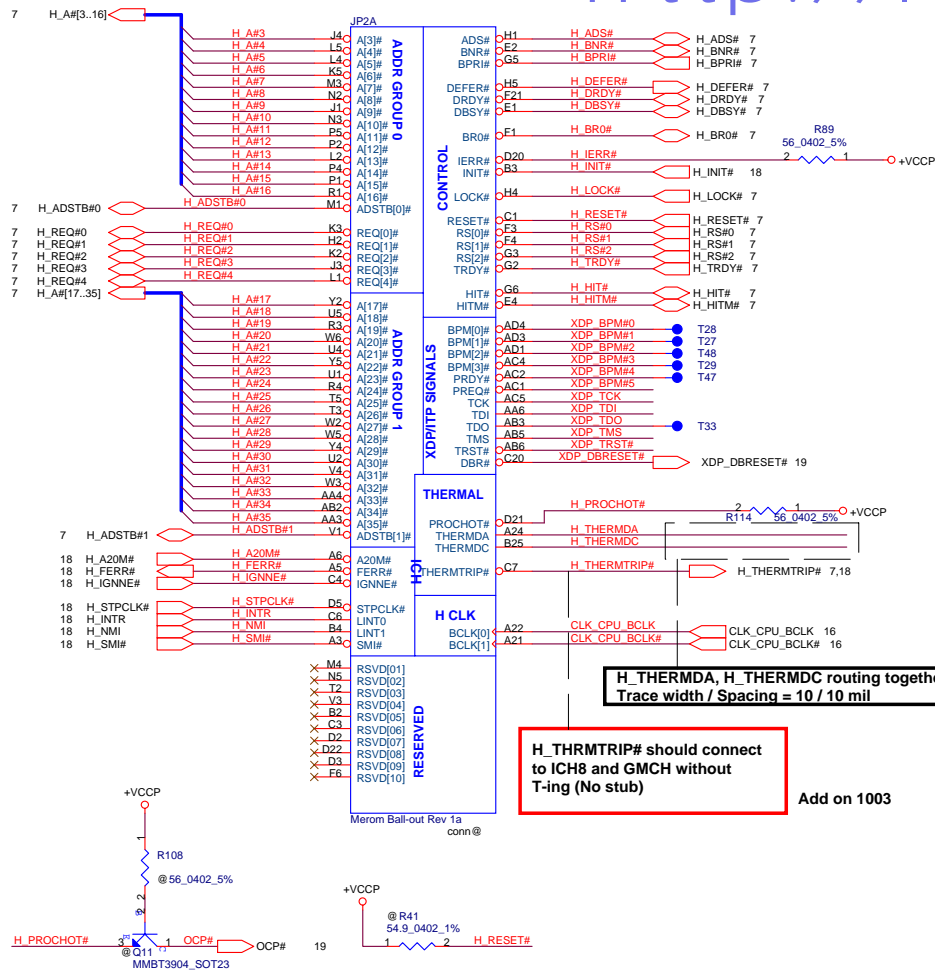
BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

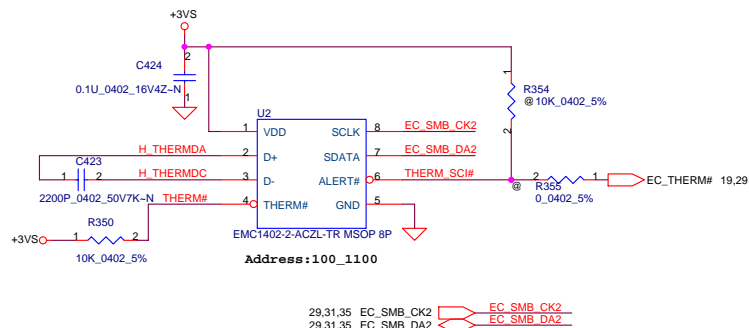
BTO Option Table

[illegible]

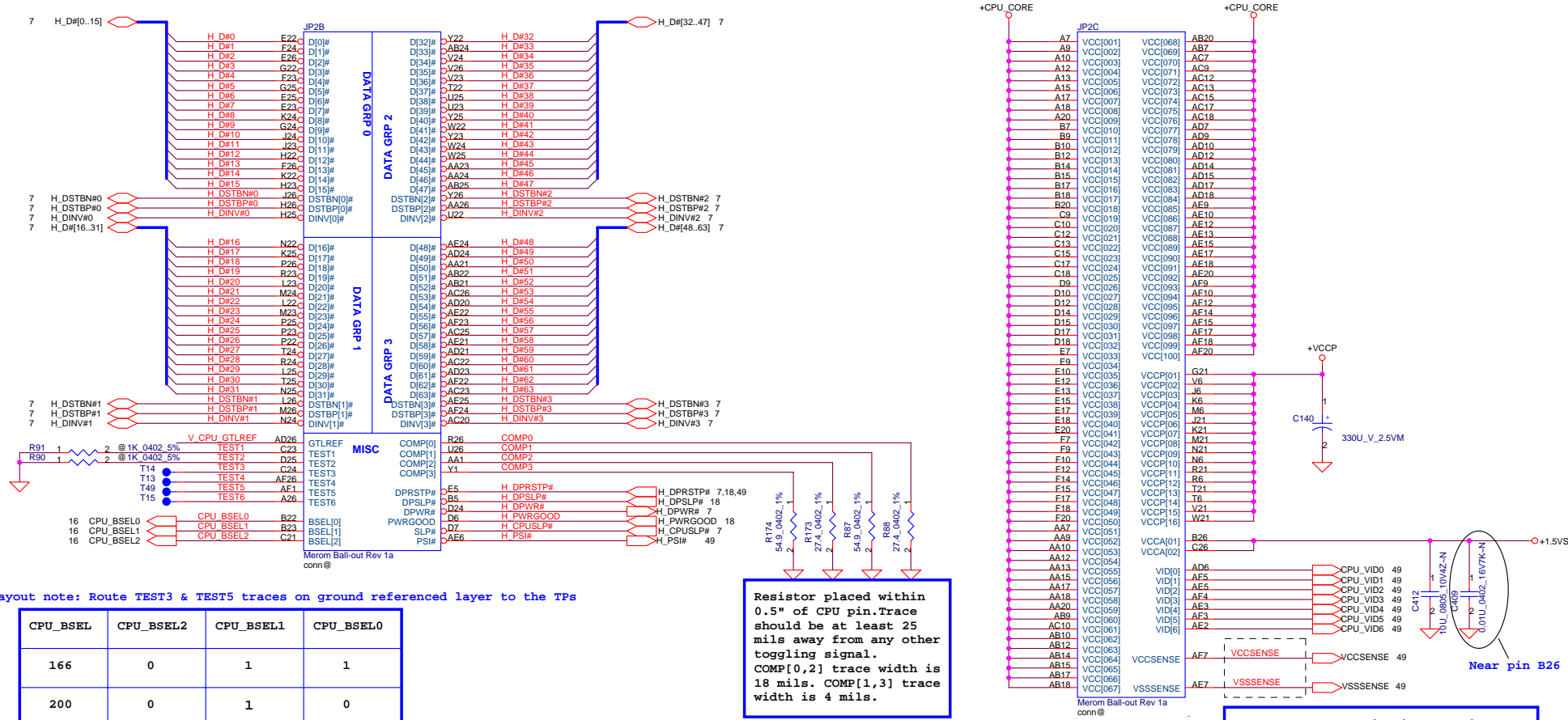
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				Document Number <div style="text-align: center;">LA-4231P</div>	
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Thermal Sensor EMC1402-1-ACZL-TR

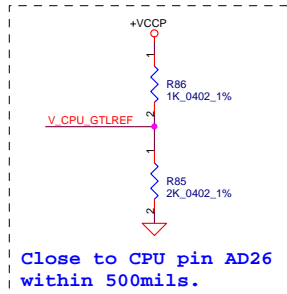


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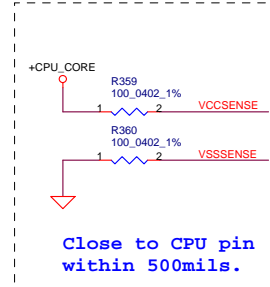


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0



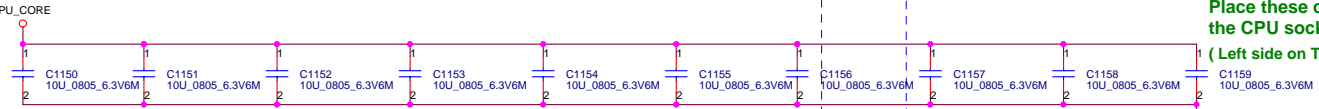
Length match within 25 mils. The trace width/space/other is 20/7/25.



High Frequency Decoupling

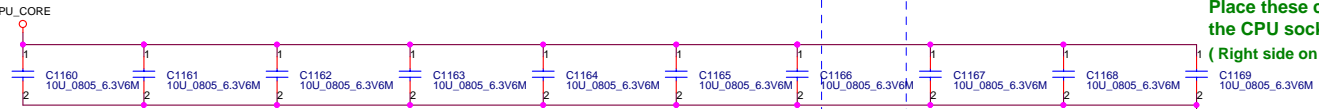
10uF 0805 X5R -> 85 degree.

Place these caps inside the CPU socket cavity. (Left side on Top).



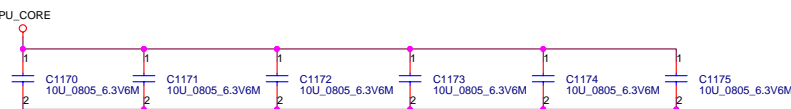
Place these caps inside the CPU socket. (Left side on Top).

Place these caps inside the CPU socket cavity. (Right side on Top side).

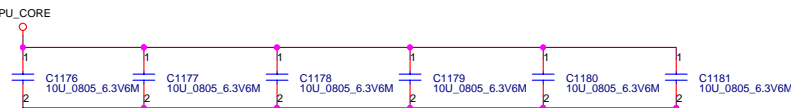


Place these caps inside the CPU socket. (Right side on Top).

Place these caps inside the CPU socket cavity. (Left side on Bottom).

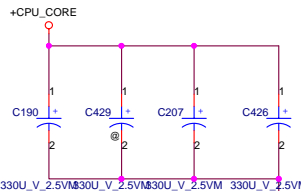


Place these caps inside the CPU socket cavity. (Right side on Bottom).

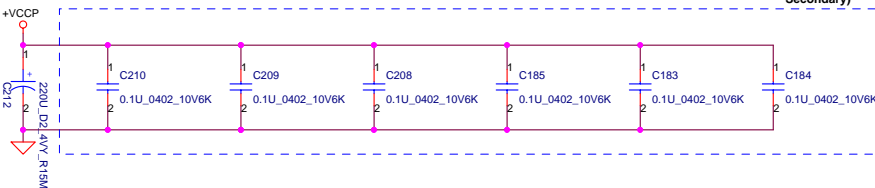


Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF

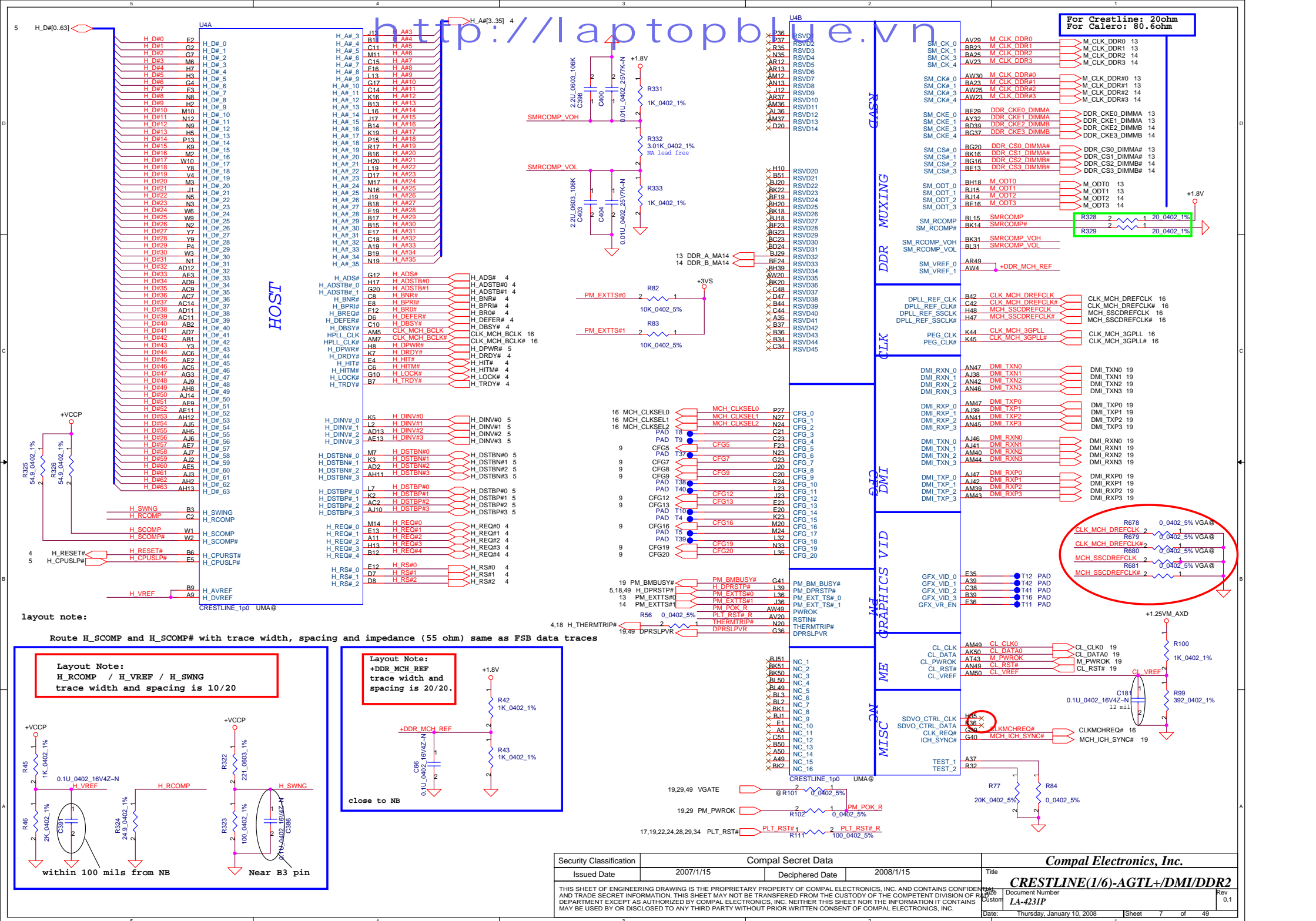


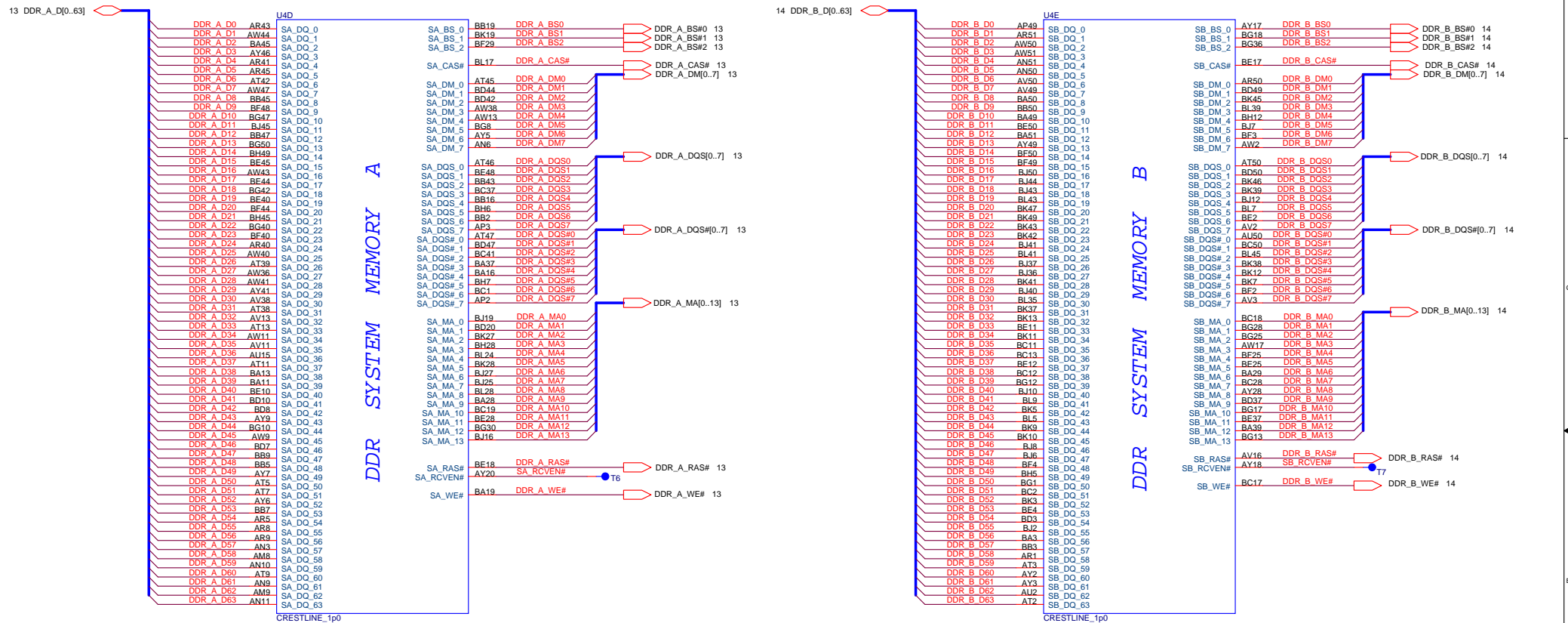
Place these inside socket cavity on L8 (North side Secondary)



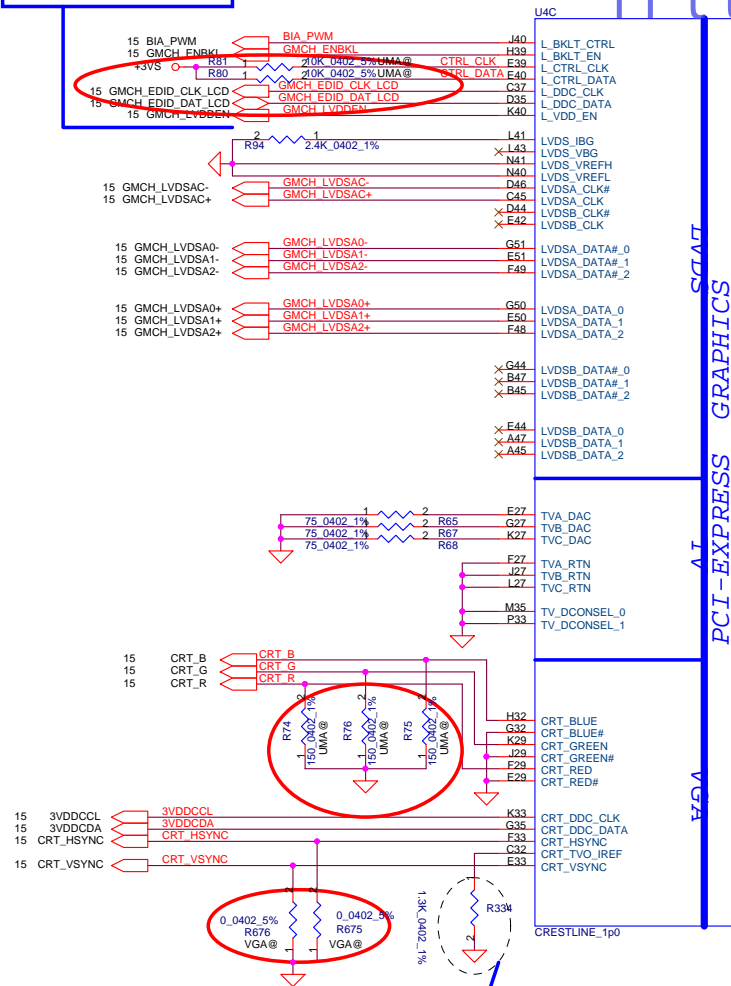
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
A27	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D13	VSS[029]	VSS[110]	AA5
D16	VSS[030]	VSS[111]	AA11
D19	VSS[031]	VSS[112]	AA14
D23	VSS[032]	VSS[113]	AA16
D26	VSS[033]	VSS[114]	AA18
E3	VSS[034]	VSS[115]	AA19
E6	VSS[035]	VSS[116]	AA22
E8	VSS[036]	VSS[117]	AA25
F11	VSS[037]	VSS[118]	AB1
F14	VSS[038]	VSS[119]	AB4
F16	VSS[039]	VSS[120]	AB8
F19	VSS[040]	VSS[121]	AB11
F21	VSS[041]	VSS[122]	AB13
F24	VSS[042]	VSS[123]	AB16
F5	VSS[043]	VSS[124]	AB19
F8	VSS[044]	VSS[125]	AB23
F11	VSS[045]	VSS[126]	AB26
F13	VSS[046]	VSS[127]	AC3
F16	VSS[047]	VSS[128]	AC6
F19	VSS[048]	VSS[129]	AC8
F2	VSS[049]	VSS[130]	AC11
F22	VSS[050]	VSS[131]	AC14
F25	VSS[051]	VSS[132]	AC16
G4	VSS[052]	VSS[133]	AC19
G1	VSS[053]	VSS[134]	AC21
G23	VSS[054]	VSS[135]	AC24
G26	VSS[055]	VSS[136]	AD2
H3	VSS[056]	VSS[137]	AD5
H6	VSS[057]	VSS[138]	AD8
H21	VSS[058]	VSS[139]	AD11
H24	VSS[059]	VSS[140]	AD13
J2	VSS[060]	VSS[141]	AD16
J5	VSS[061]	VSS[142]	AD19
J22	VSS[062]	VSS[143]	AD22
J25	VSS[063]	VSS[144]	AD25
K1	VSS[064]	VSS[145]	AE1
K4	VSS[065]	VSS[146]	AE4
K23	VSS[066]	VSS[147]	AE8
K26	VSS[067]	VSS[148]	AE11
L3	VSS[068]	VSS[149]	AE14
L6	VSS[069]	VSS[150]	AE16
L21	VSS[070]	VSS[151]	AE19
L24	VSS[071]	VSS[152]	AE23
M2	VSS[072]	VSS[153]	AE26
M5	VSS[073]	VSS[154]	A2
M22	VSS[074]	VSS[155]	AF6
M25	VSS[075]	VSS[156]	AF8
N1	VSS[076]	VSS[157]	AF11
N4	VSS[077]	VSS[158]	AF13
N23	VSS[078]	VSS[159]	AF16
N26	VSS[079]	VSS[160]	AF19
P3	VSS[080]	VSS[161]	AF21
	VSS[081]	VSS[162]	A25
		VSS[163]	AF25

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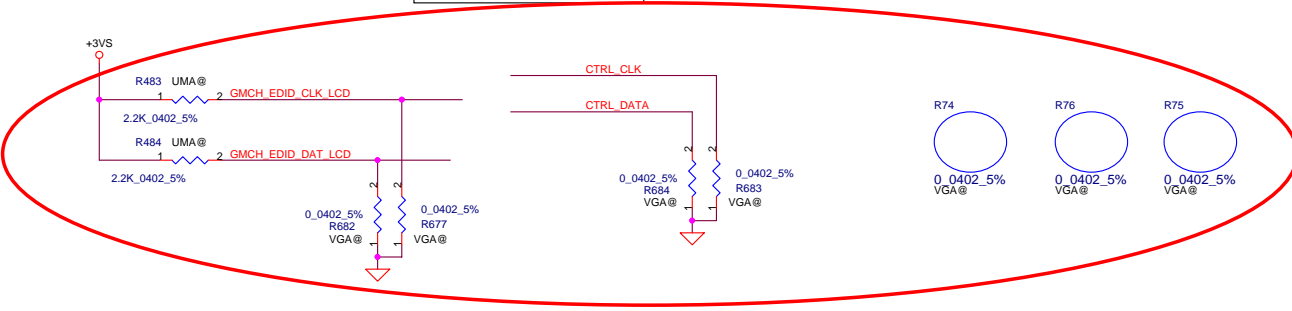




For Crestline: 2.4kohm
For Calero: 1.5kohm



For Crestline: 1.3kohm
For Calero: 255ohm



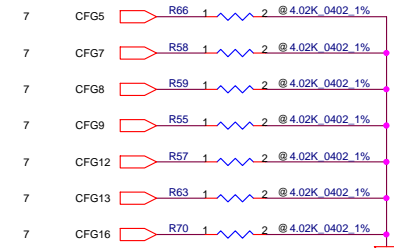
Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

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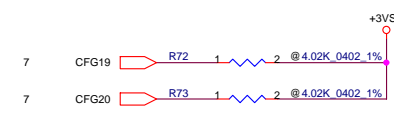
PEGCOMP trace width
and spacing is 20/25 mils.

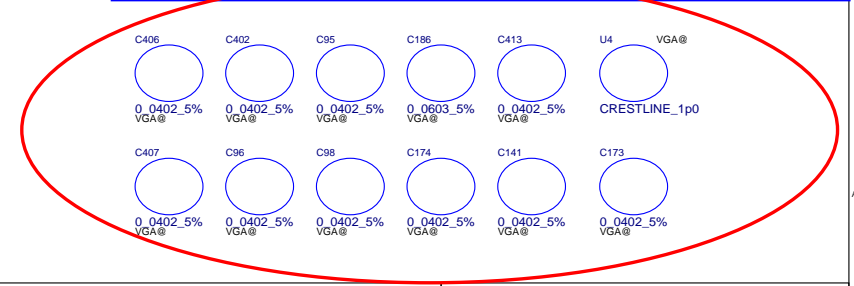
Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu. *

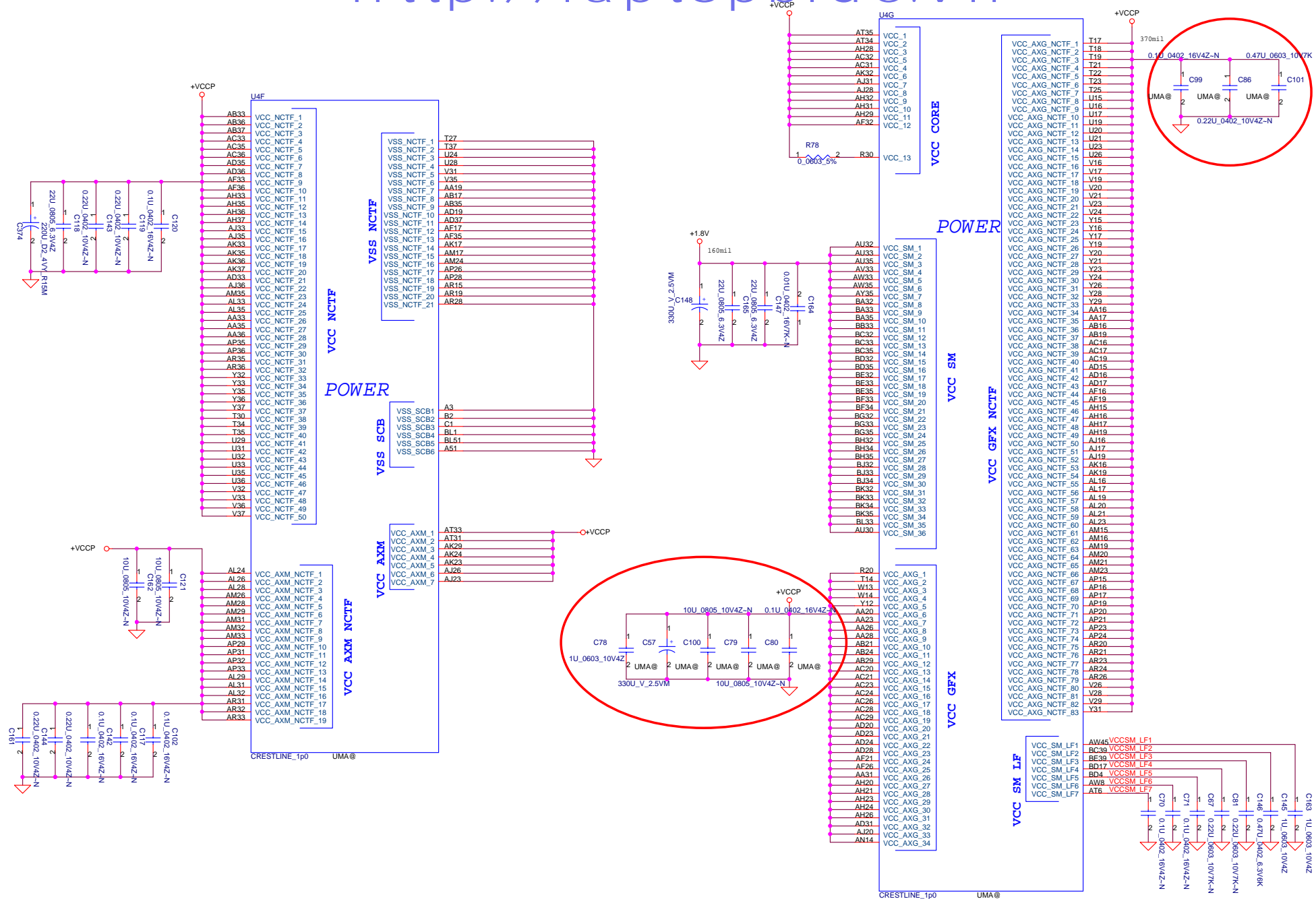


CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

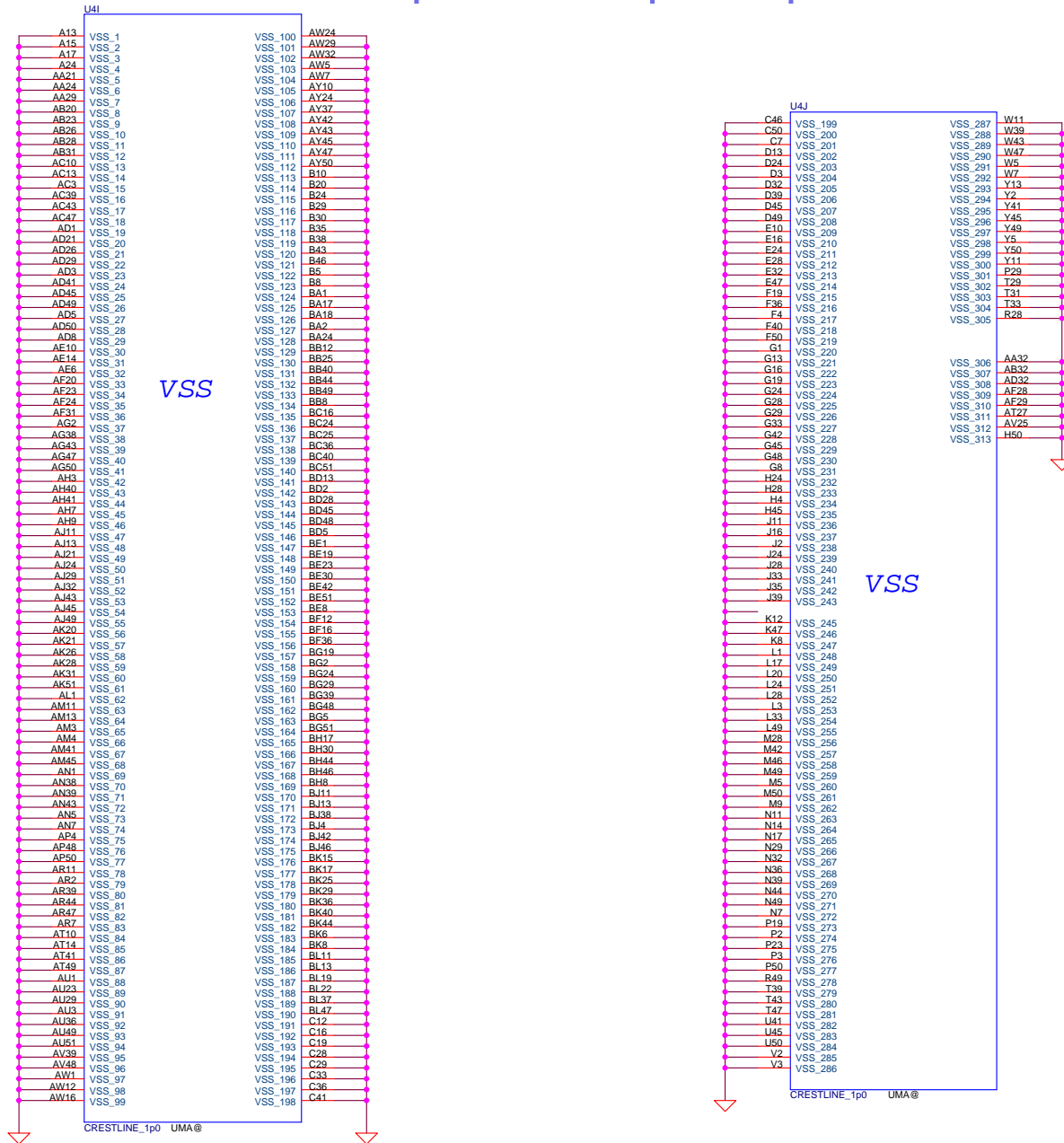




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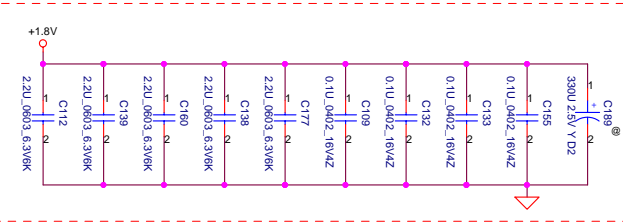
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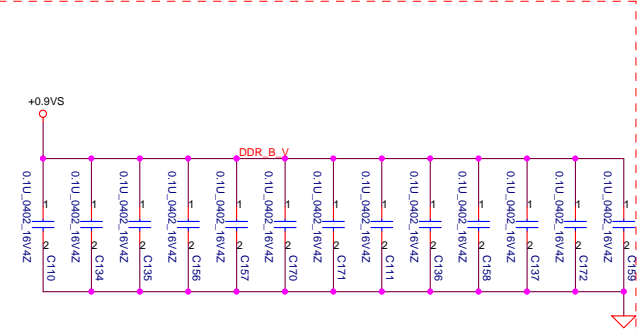
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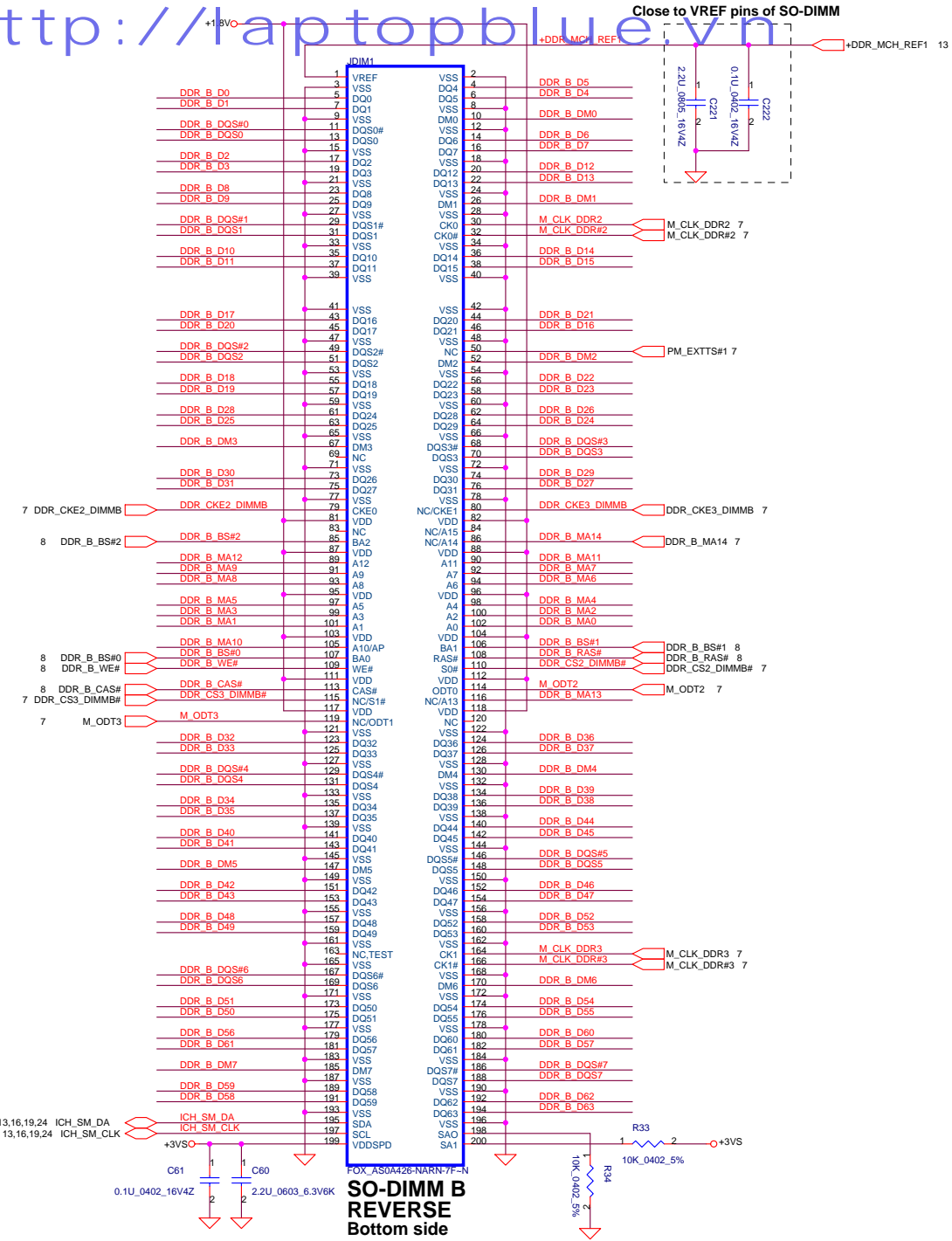
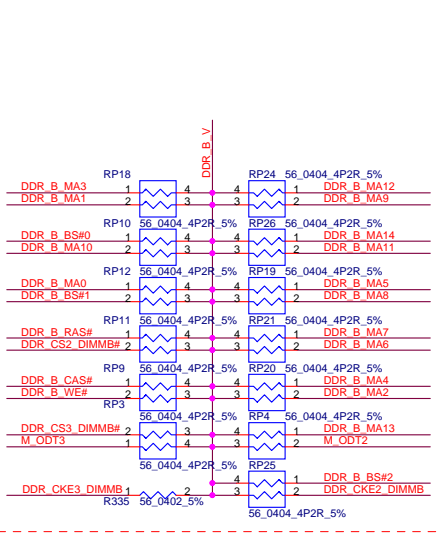
Layout Note:
Place near JDIM2



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS

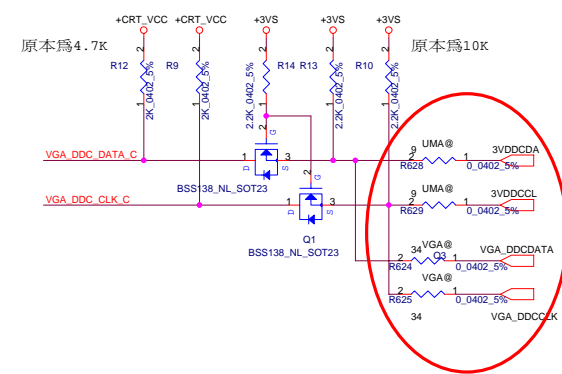


Layout Note:
Place these resistor
closely JP42,all
trace length Max=1.5"



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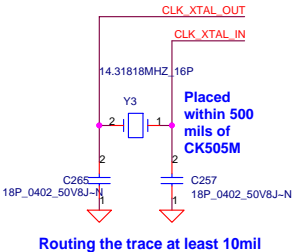
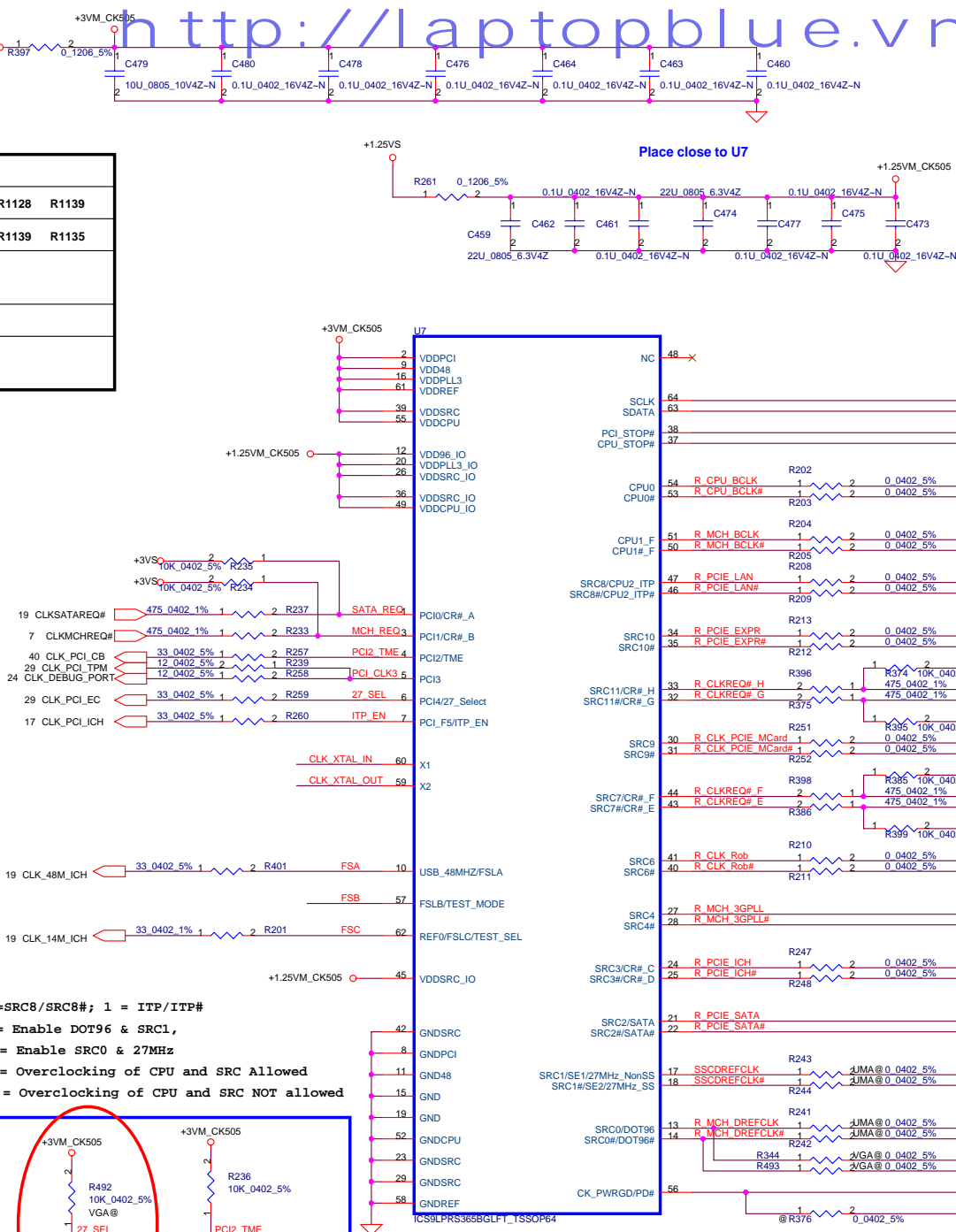
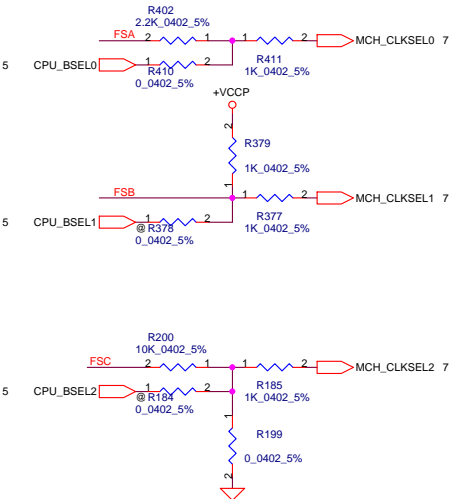


Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i>		
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	CRT CONN/LCD CONN	
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				Custom	LA-423IP	0.1
				Date:	Thursday, January 10, 2008	Sheet 15 of 49

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

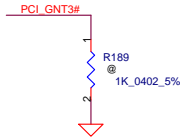
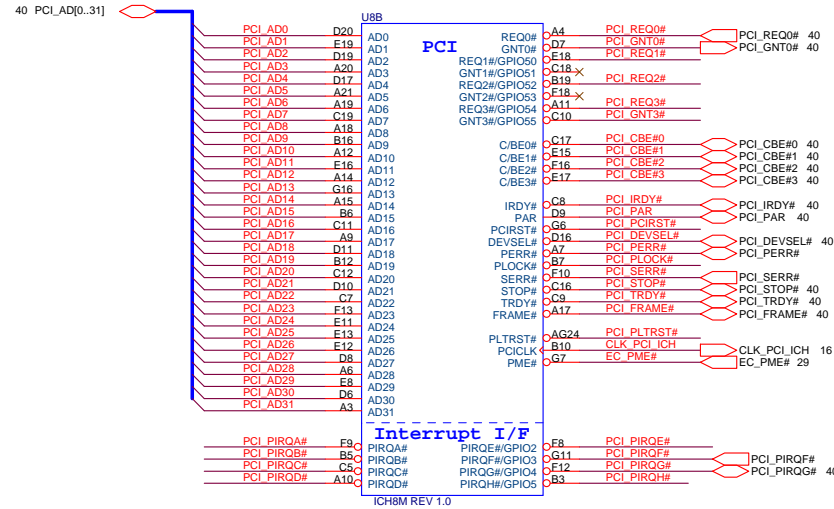
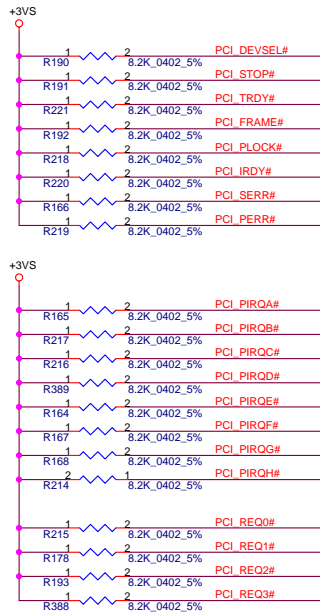
FSB Frequency Selet:

CPU Driven	Stuff	R1107	R1135	R1083
*(Default)	No Stuff	R1074	R1086	R1098
	Stuff	R1086	R1139	R1135
667MHz	No Stuff	R1083	R1107	R1128
	Stuff	R1135	R1139	
800MHz	No Stuff	R1083	R1086	R1098
	Stuff	R1074	R1107	R1113



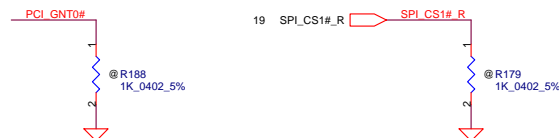
For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1 = Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed

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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	Clock generator
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				Document Number	LA-4231P
				Date	Thursday, January 10, 2008
				Sheet	16 of 49

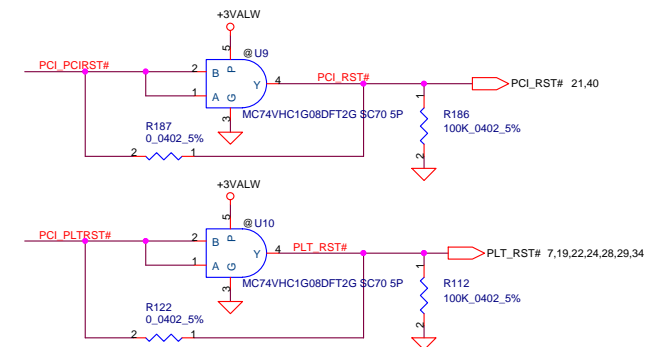
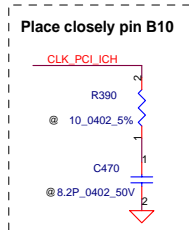


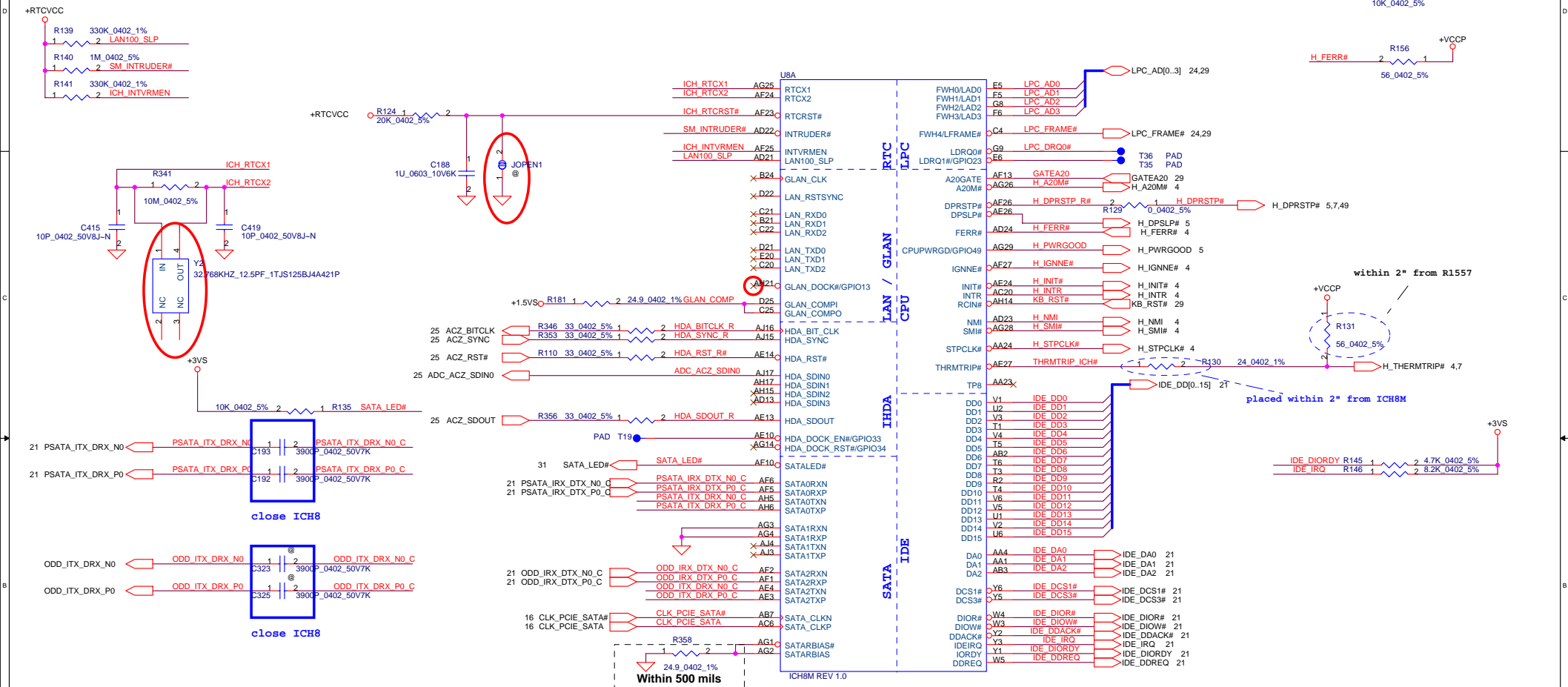
Check if use LPC?

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

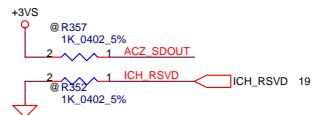


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*



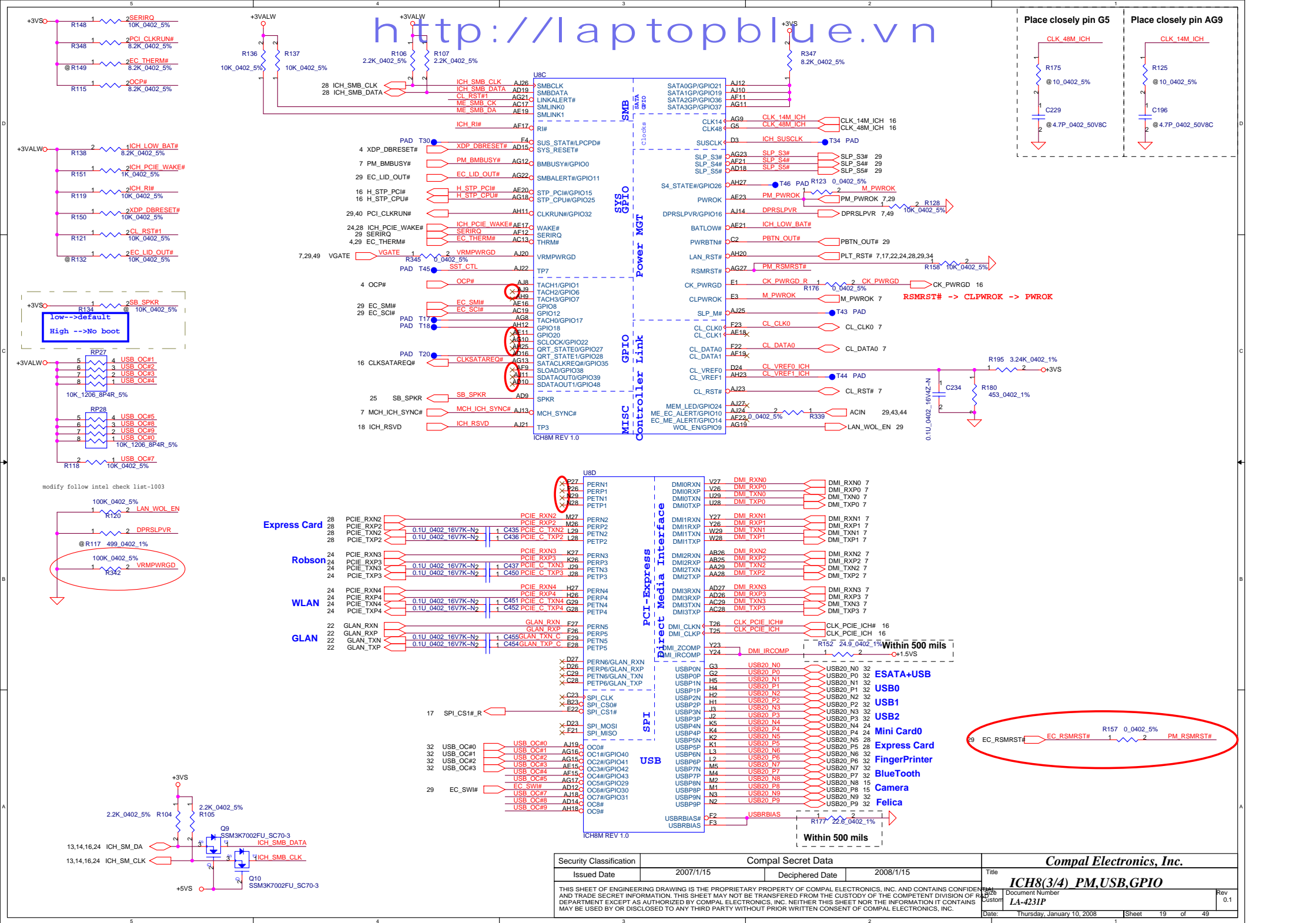


XOR CHAIN ENTRANCE STRAP:RSVD



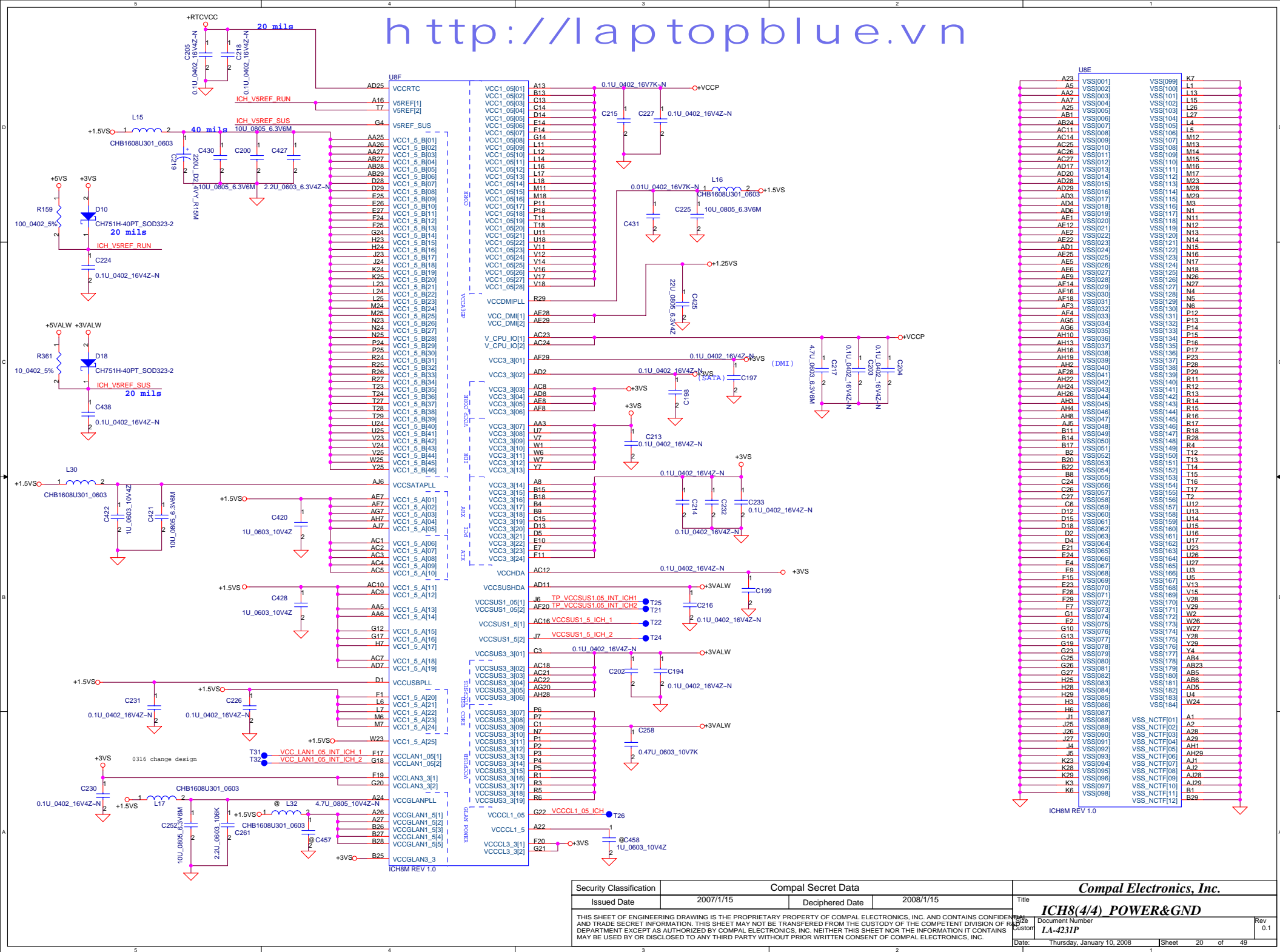
XOR Chain Entrance Strap		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	ICH8(2/4) LAN,HD,IDE,LPC
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				LA-4231P	0.1
Date	Thursday, January 10, 2008		Sheet	18	of 49

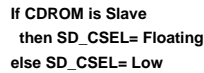


Security Classification		Compal Secret Data		Compal Electronics, Inc. ICH8(3/4) PM,USB,GPIO	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	
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Date: Thursday, January 10, 2008				Sheet	20 of 49



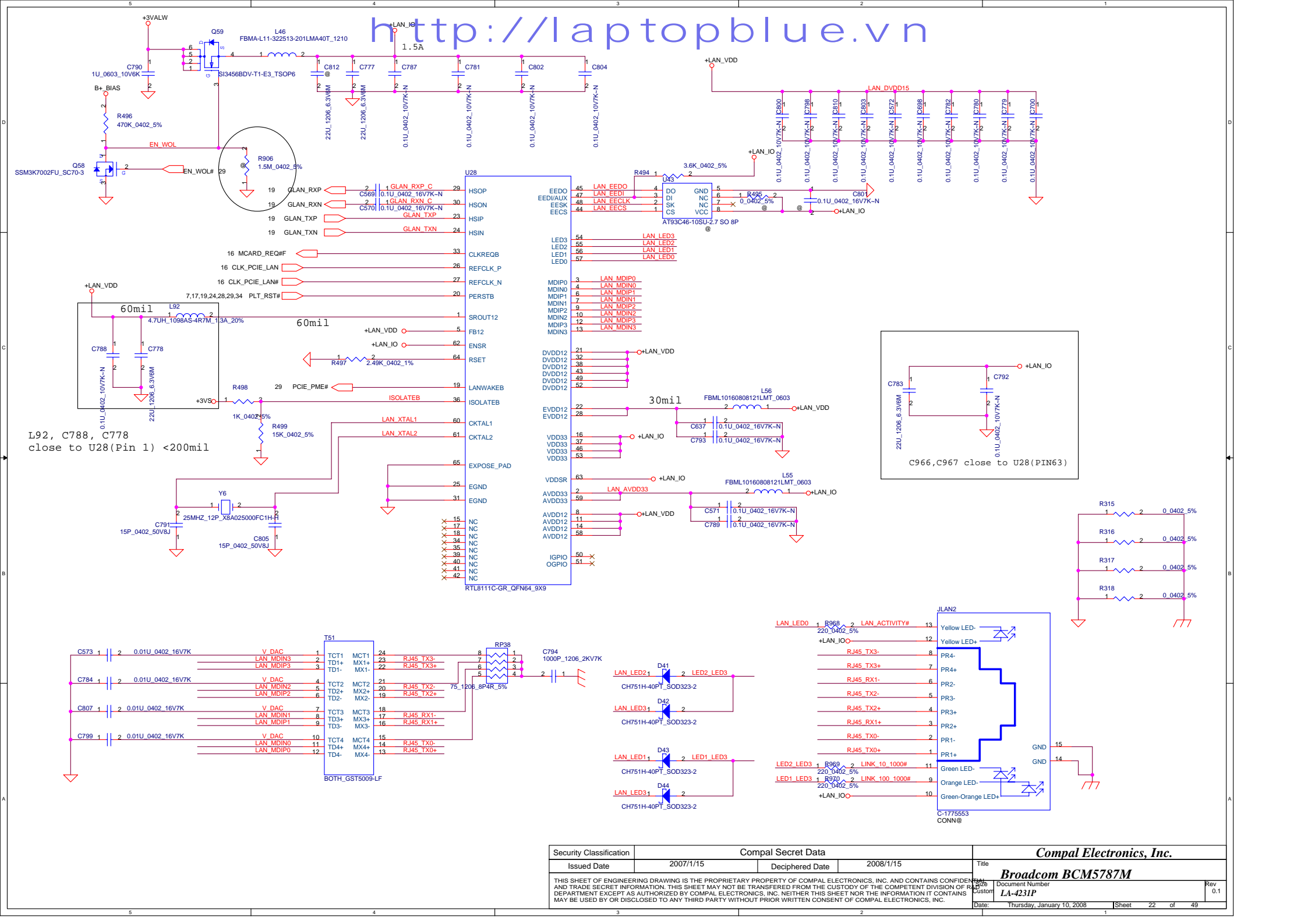
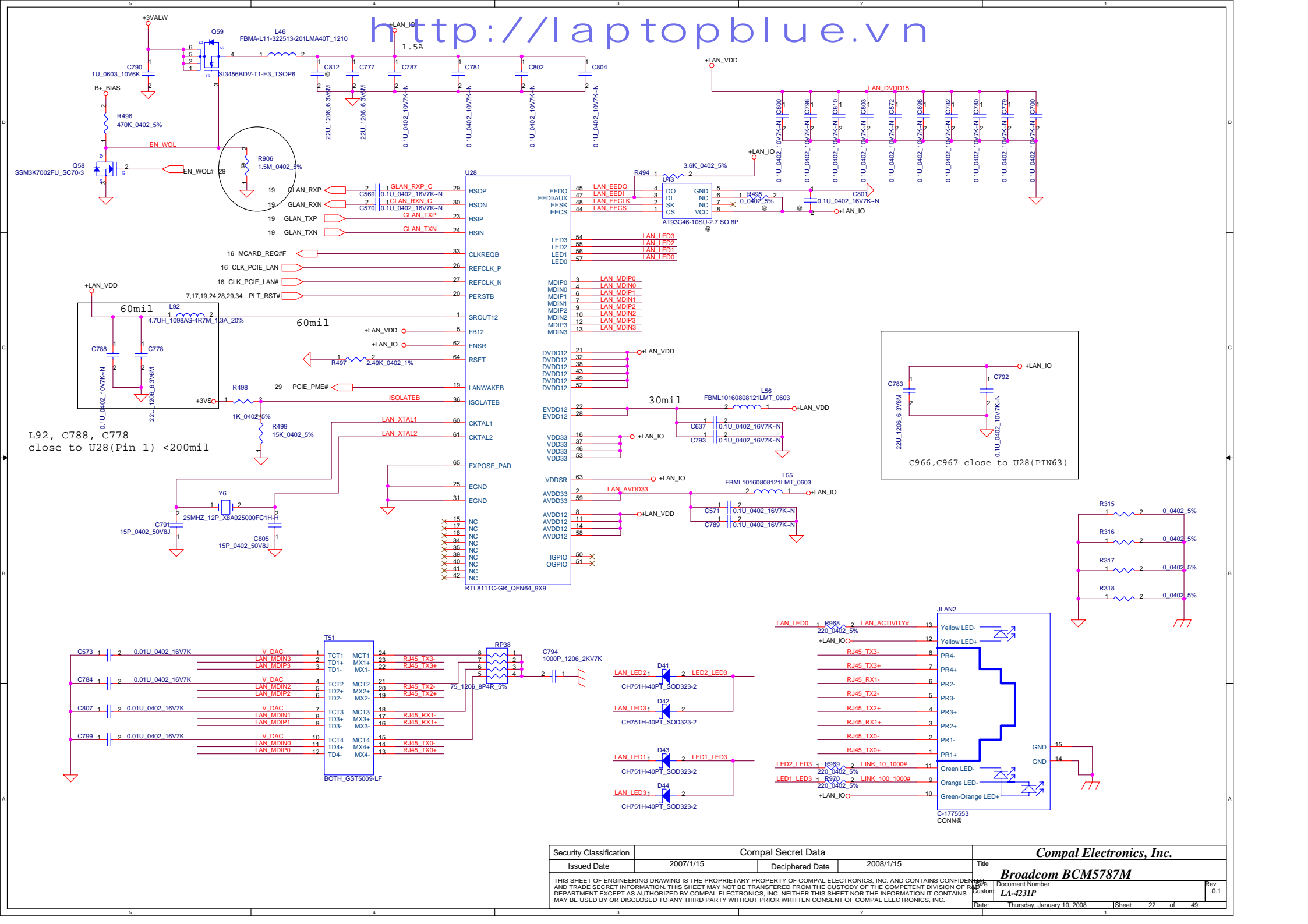
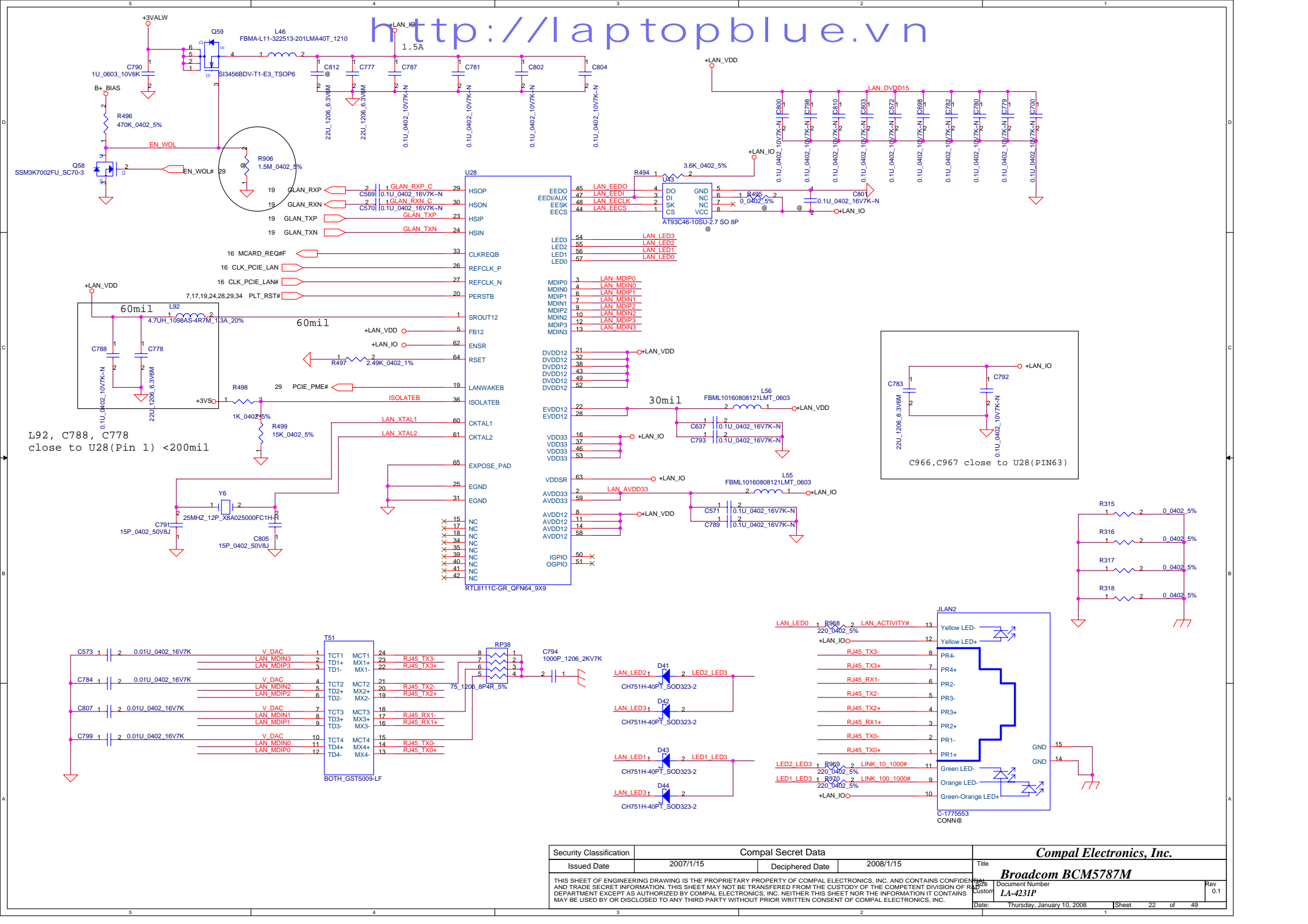
SATA HDD CONN



RESERVE(SATA ODD NET)



Title	<i>HDD/CDROM</i>	
	Size	Document Number
Custom		<i>LA-423IP</i>

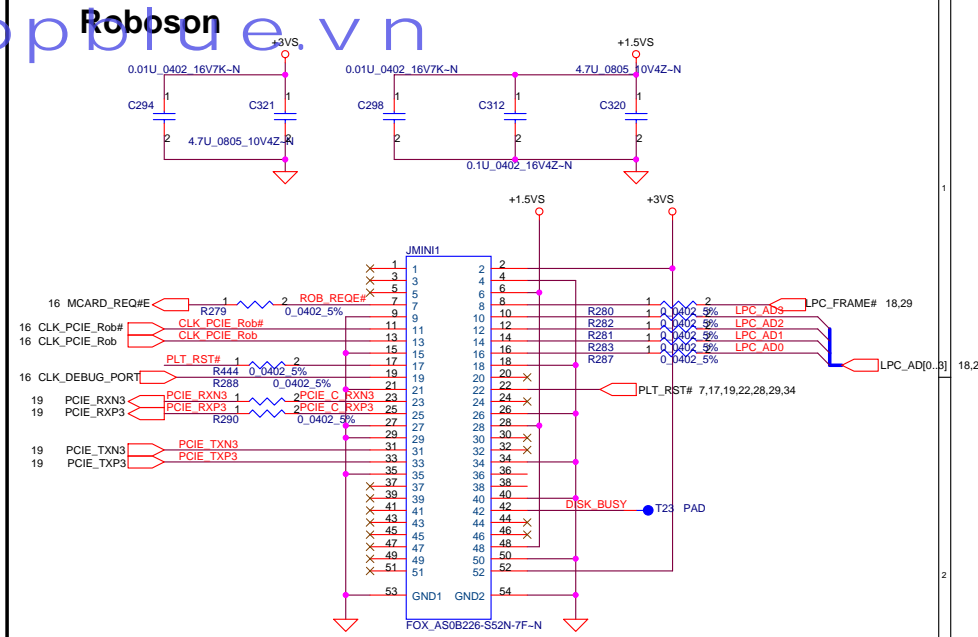
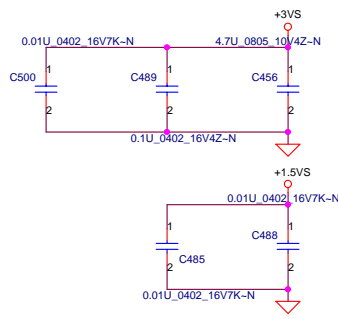
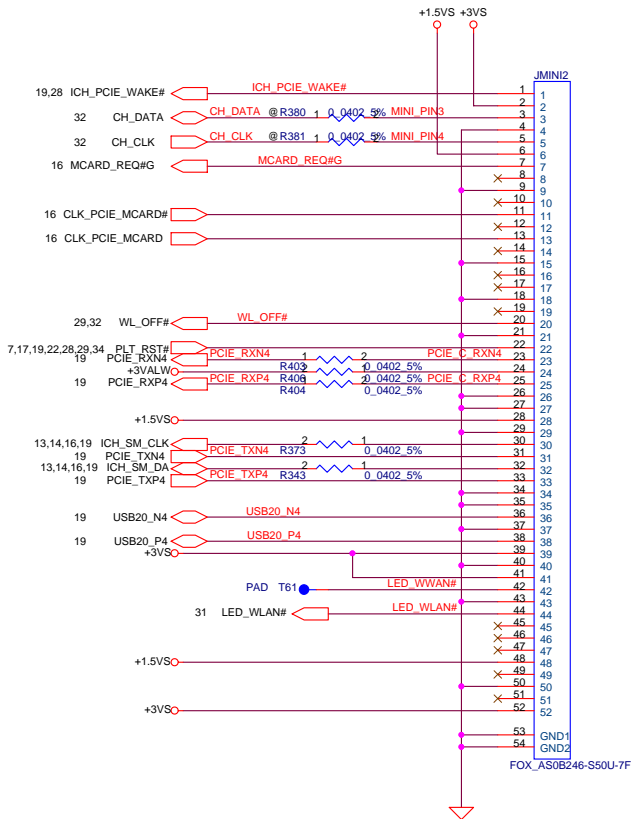


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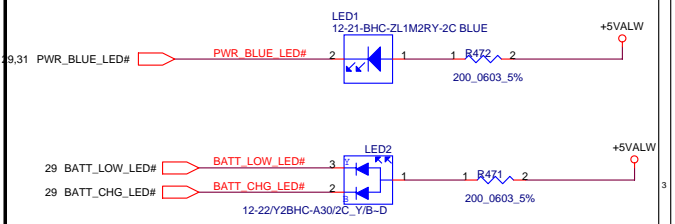
Mini-Express Card---WLAN

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Roboson



Power status(Left)

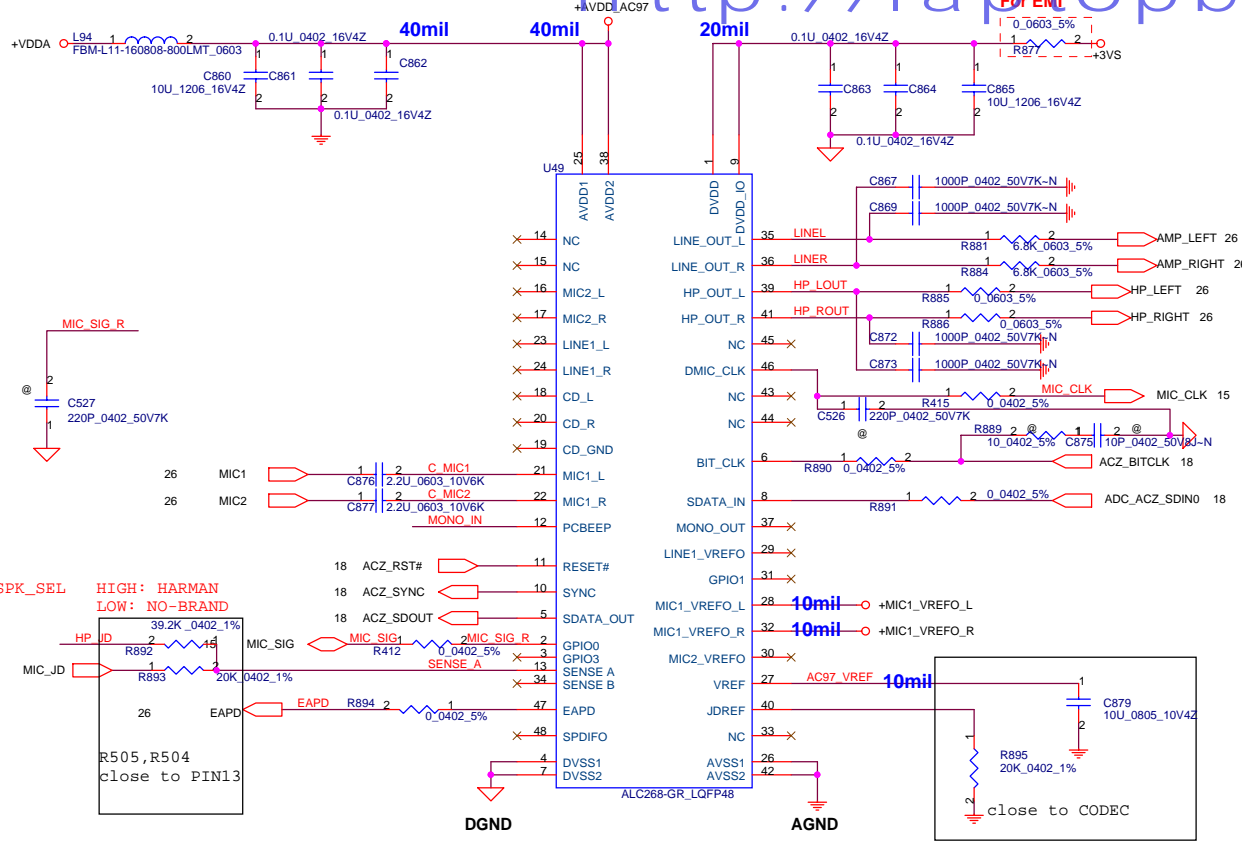


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						Document Number		Rev	
						LA-4231P		0.1	
						Date:		Thursday, January 10, 2008	
C		D		E		Sheet		24 of 49	

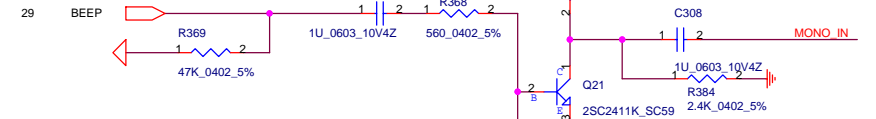
HD Audio Codec

http://laptopblue.vn

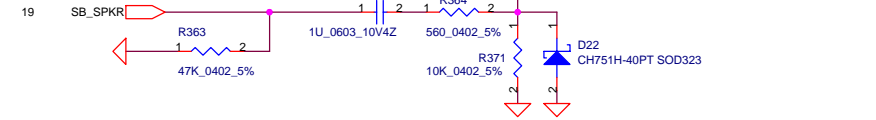
For ENI



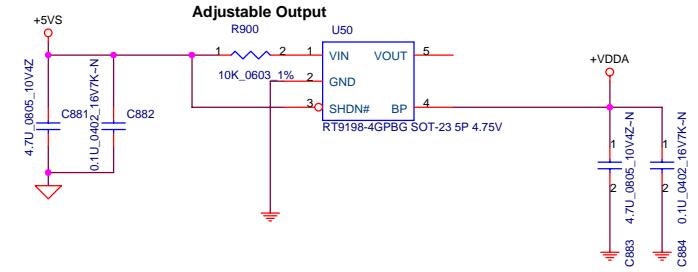
EC Bleep



ICH Bleep

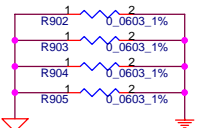


Regulator for CODEC

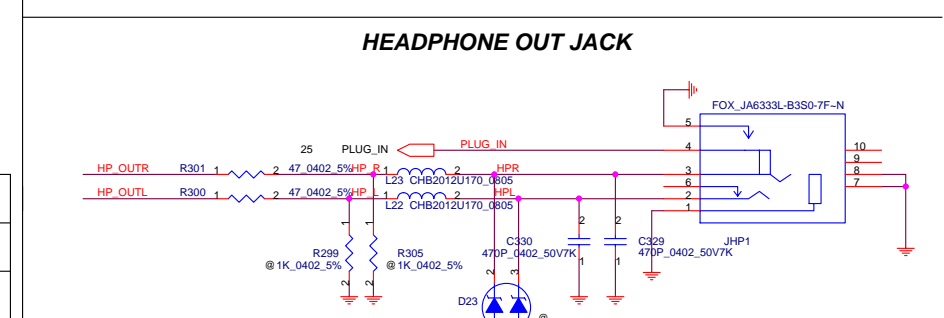
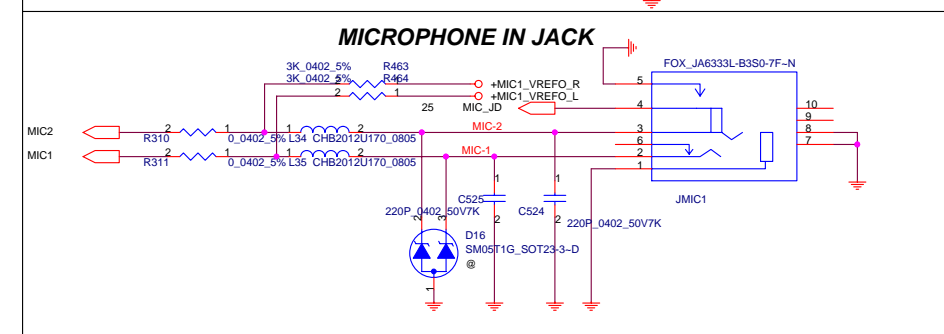
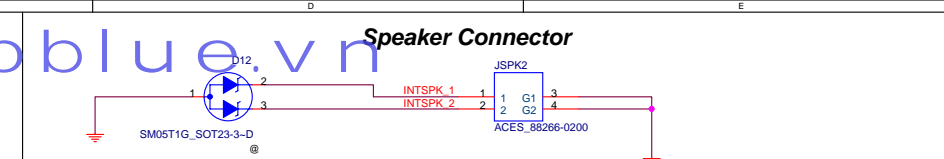
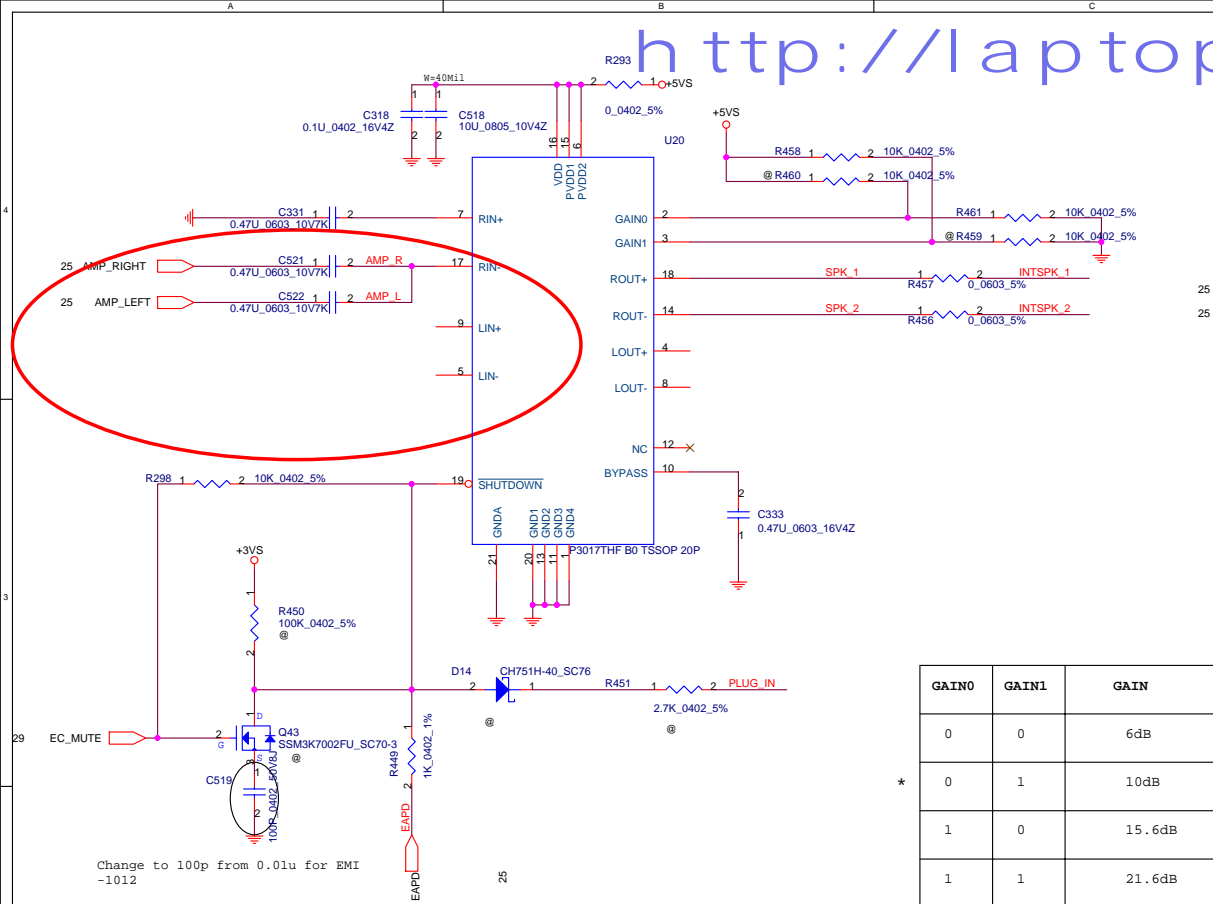


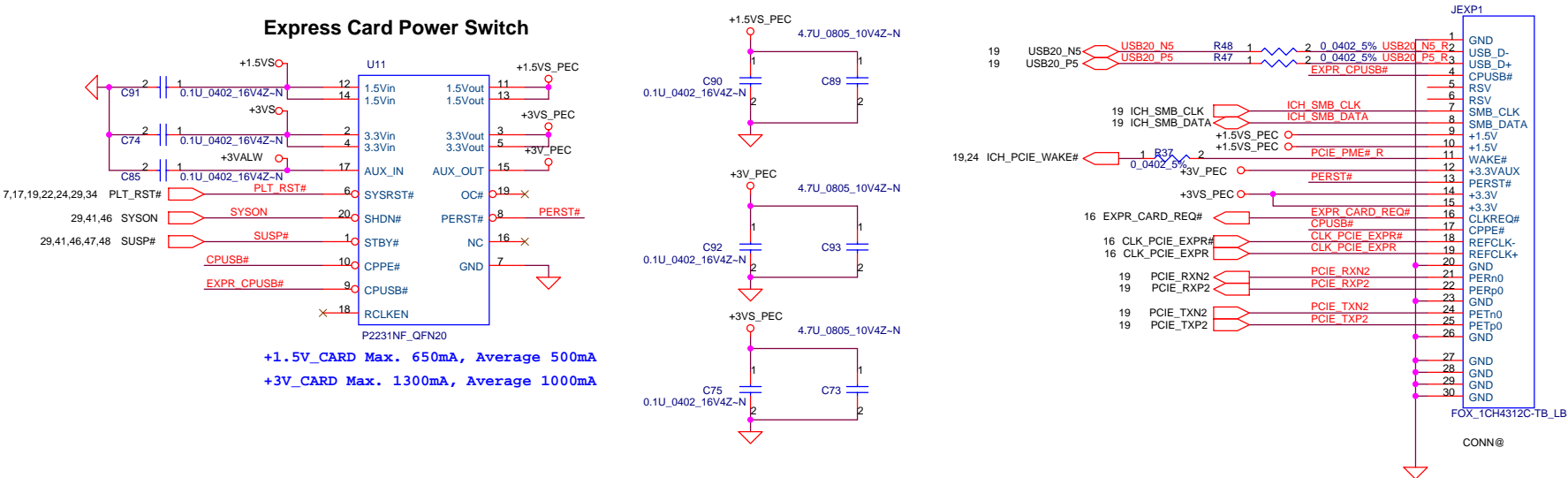
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Moat Bridge



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Issued Date	2006/08/05	Deciphered Date	2007/08/05	HD Audio Codec_ALC268		
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Security Classification	Compal Secret Data			0 5A per Compal Electronics, Inc.	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	BIOS & EC I/O Port
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				Customer	0.1
Date:	Thursday, January 10, 2008	Sheet	29	of	49

[illegible]

INT_KBD_CONN.

29 KS10[0..7] KS10[0..7]

29 KS00[0..15] KS00[0..15]

1 KS10 1

2 KS11 2

3 KS12 3

4 KS13 4

5 KS14 5

6 KS15 6

7 KS16 7

8 KS17 8

9 KS00 9

10 KS01 10

11 KS02 11

12 KS03 12

13 KS04 13

14 KS05 14

15 KS06 15

16 KS07 16

17 KS08 17

18 KS09 18

19 KS010 19

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21 KS012 21

22 KS013 22

23 KS014 23

24 KS015 24

25 25

26 26

27 27

28 28

GND1

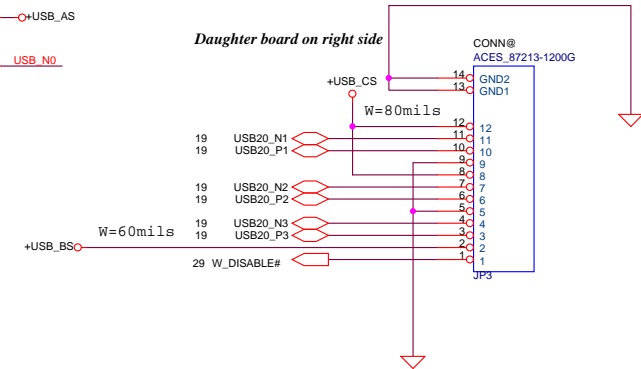
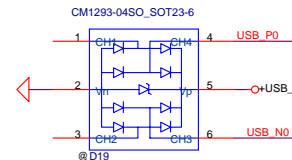
GND2

ACES_88514-2601

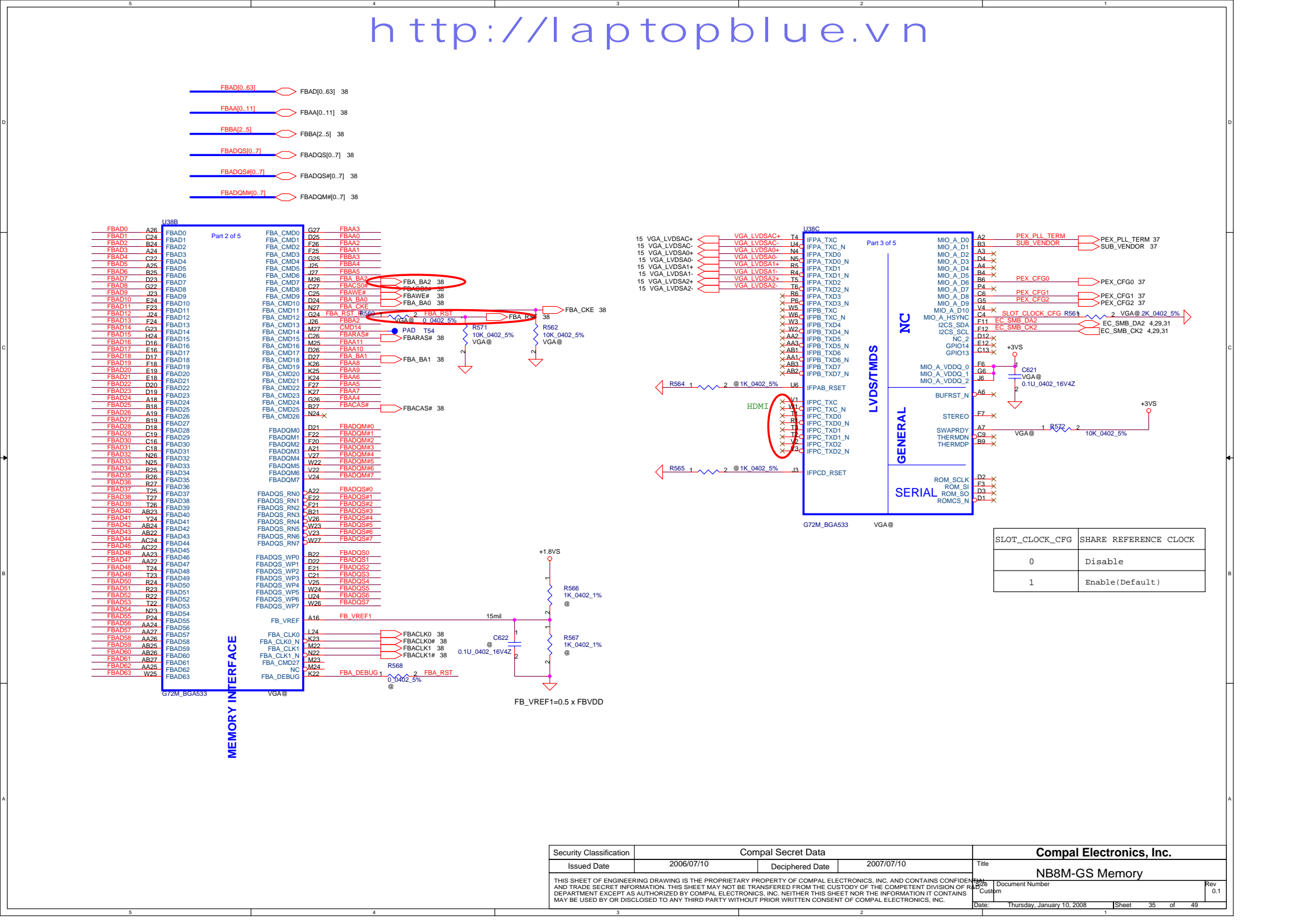
For EMI

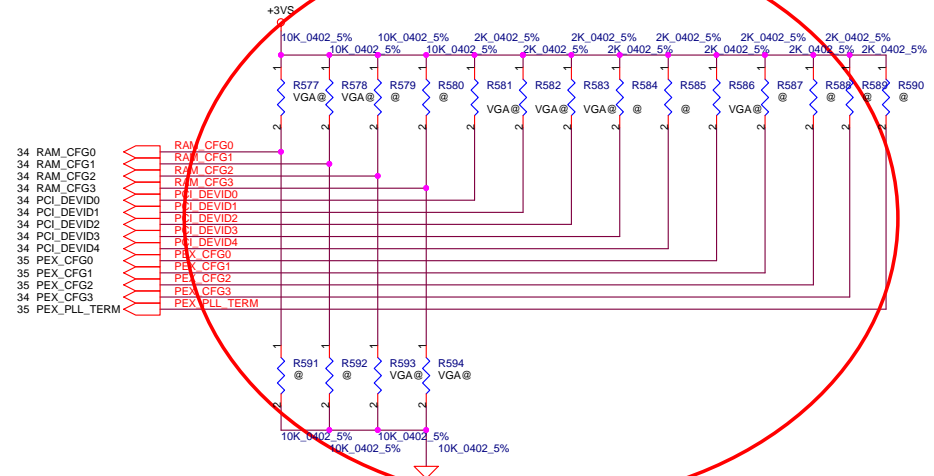
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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	Rev 0.1
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				Date: Thursday, January 10, 2008	Sheet 31 of 49



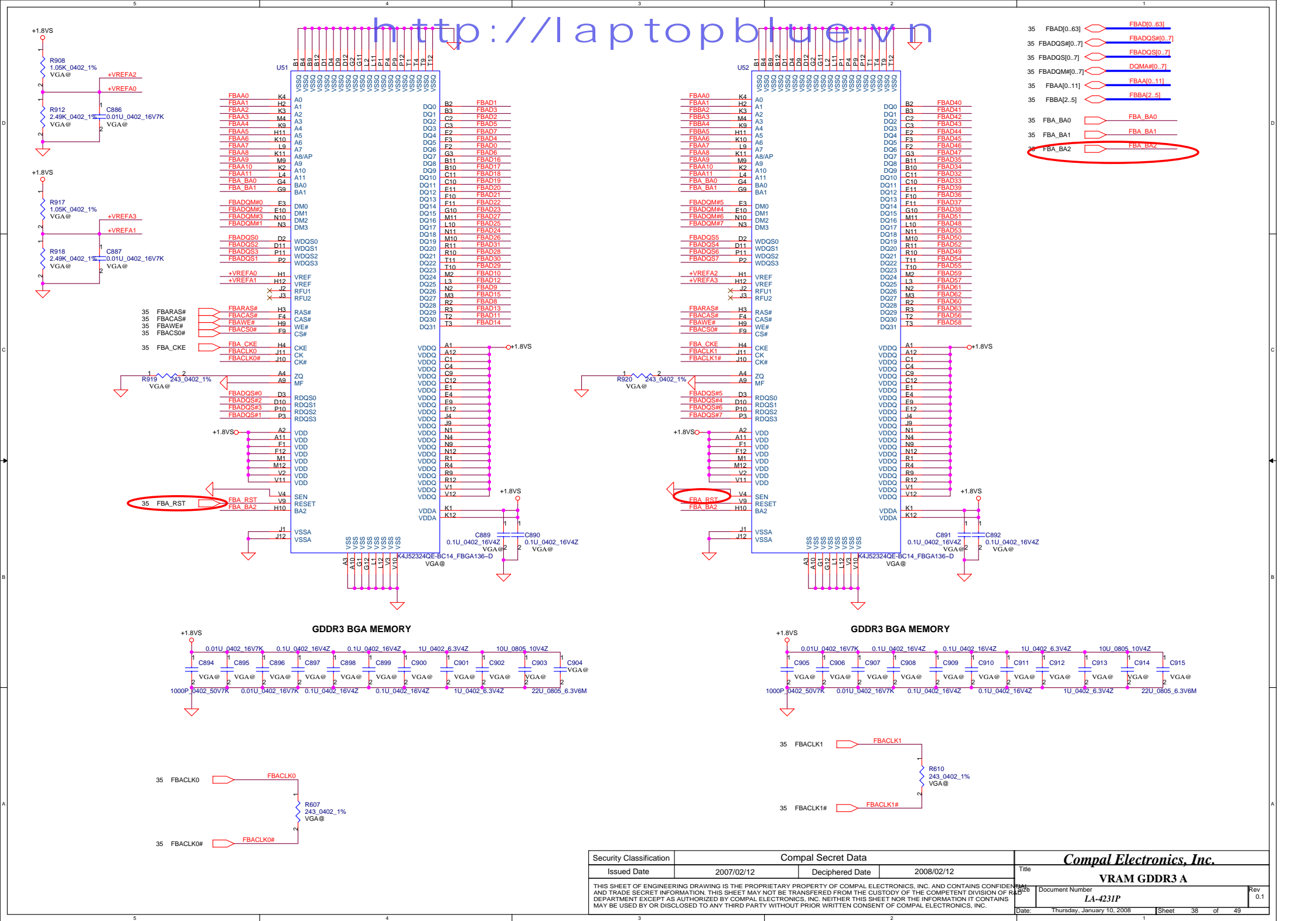
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	<i>USB/BlueTooth/FP/Felcia</i>
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				Document Number	0.1
				LA-4231P	
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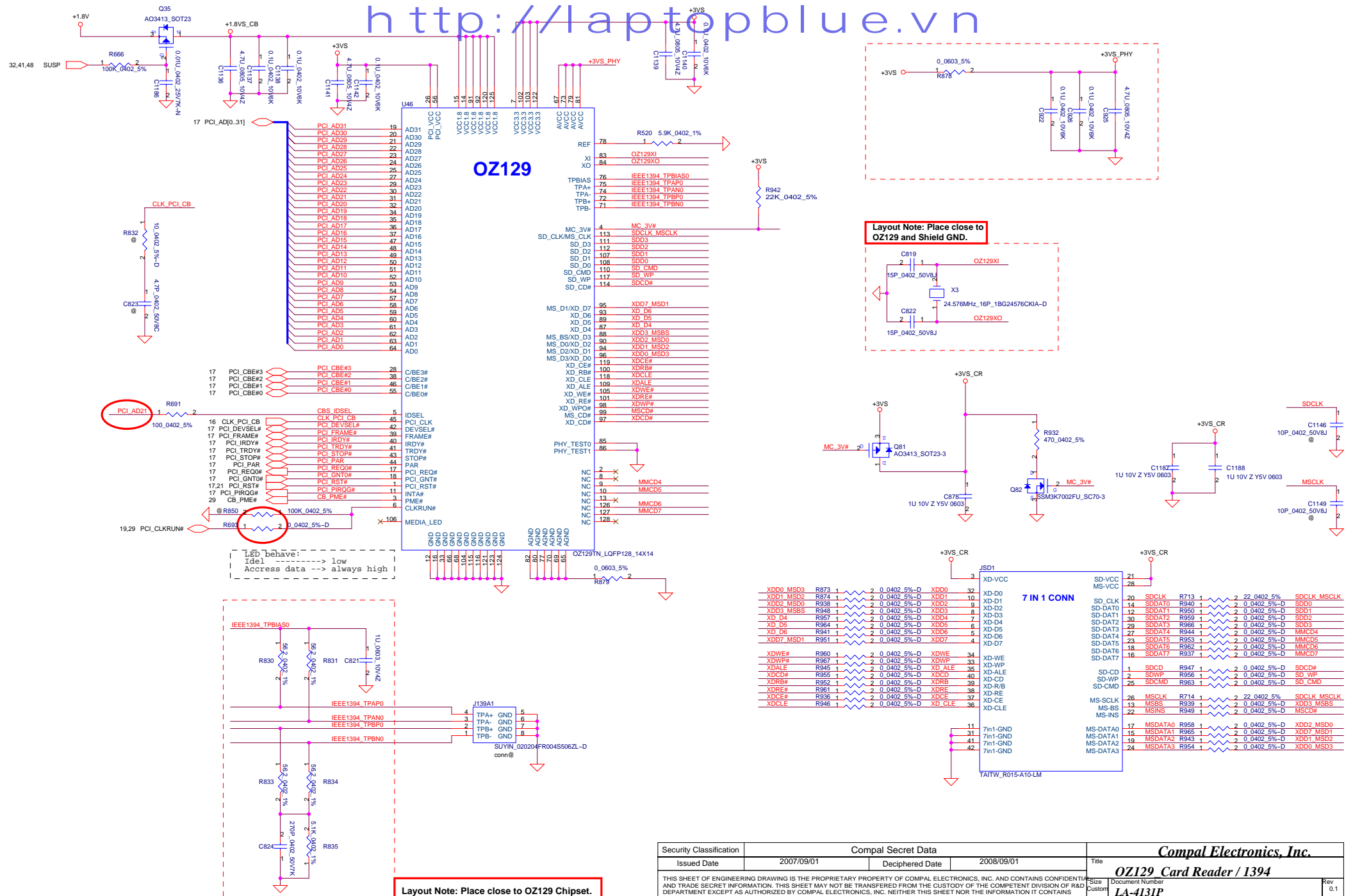
[illegible]



Package		
(10*12.5)	Infineon GDDR2(400): SA00000S800 (HYB18T256161AF-25)	Infineon GDDR2(350): SA00000T700 (HYB18T256161AF-28)
(11*13)	Samsung GDDR2 (400): SA00000FG10 (K4N56163QF-ZC25)	Samsung GDDR2 (350): SA00000TB00 (K4N56163QF-ZC2A)
(8*13)	Hynix GDDR2 (400): SA00000FF10 (HY5PS561621AFP-25)	Hynix GDDR2 (350): SA00000TJ00 (HY5PS561621AFP-28)

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Issued Date	2006/07/10	Deciphered Date	2007/07/10	Title	NB8M-GS GND & STRAP	
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				Custom	0.1	
Date: Thursday, January 10, 2008				Sheet	37	of 49



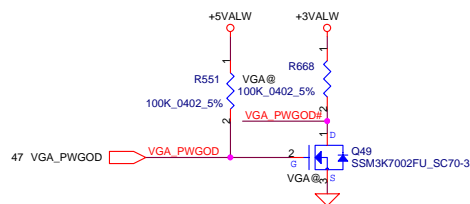
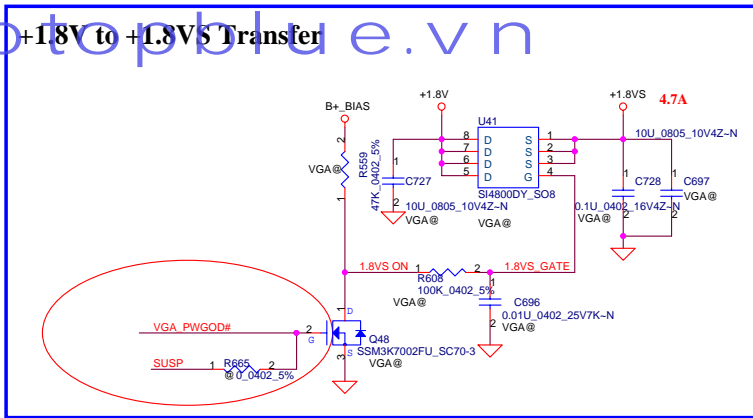
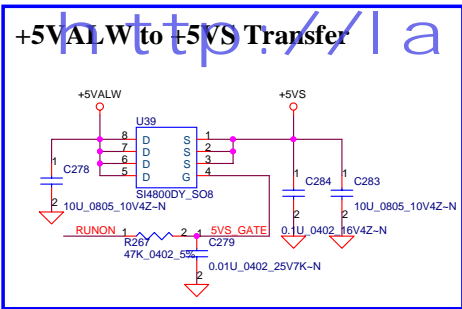


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				Size	Document Number
				Rev	0.1
				LA-4131P	
Date		Thursday, January 10, 2008		Sheet	40 of 40

+3VALW to +3VS Transfer

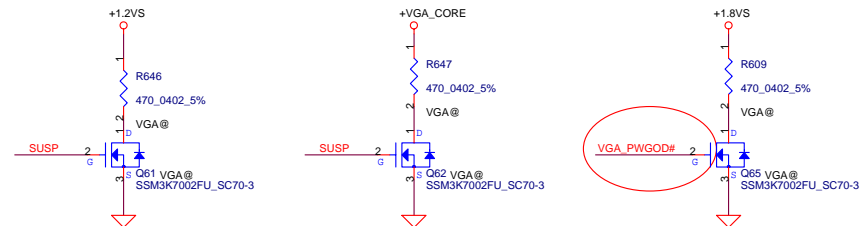
The diagram illustrates the +3VALW to +3VS Transfer circuit. It includes the following components and connections:

- Power Sources:** +3VALW, +3VS, and B+ (BIAS).
- Resistors:**
 - R198: 330K_0402_5% (connected to B+).
 - R197: 100K_0402_5% (connected to +3VALW).
 - R199: 100K_0402_5% (connected to +3VS).
- Capacitors:**
 - C271: 10U_0805_10V4Z-N (connected to +3VALW).
 - C465: 10U_0805_10V4Z-N (connected to +3VS).
 - C256: 0.1U_0402_16V4Z-N (connected to B+).
 - C18: 0.01U_0402_25V7K-N (connected to SUSP).
- Transistor:** U40 (S4800DY_S08) MOSFET.
- Connections:**
 - Gate: +3VALW through R197 and C271.
 - Source: +3VS through R199 and C465.
 - Drain: B+ through R198 and C256.
 - Body: SUSP through C18.

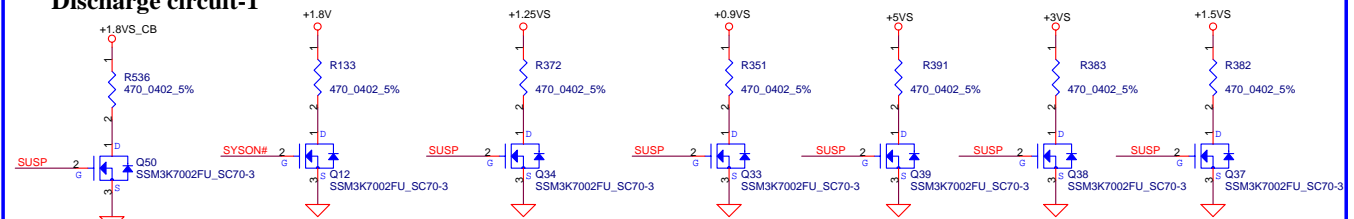


SYSON -> SUSP# -> VGA_ON->VGA_PWGOD

VGA Discharge circuit



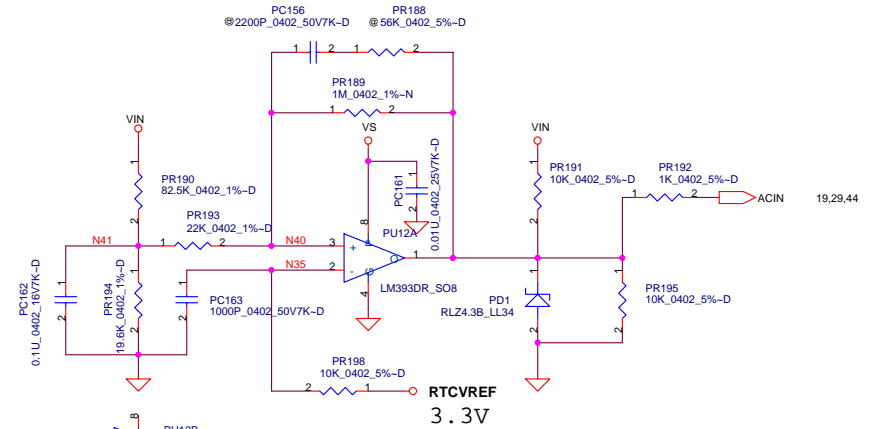
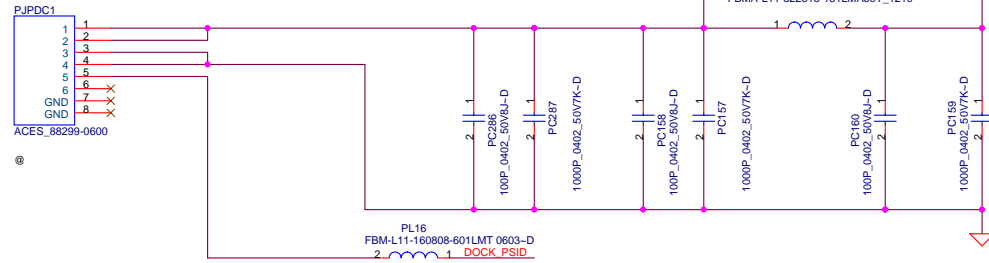
Discharge circuit-1



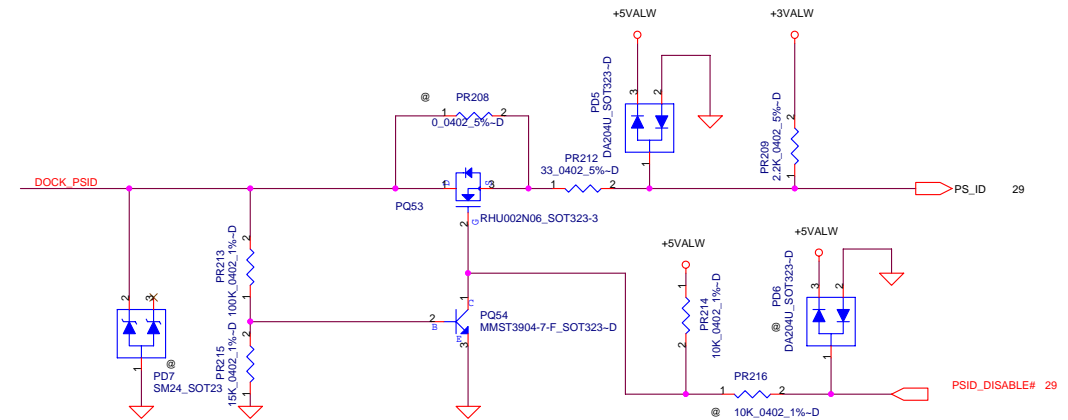
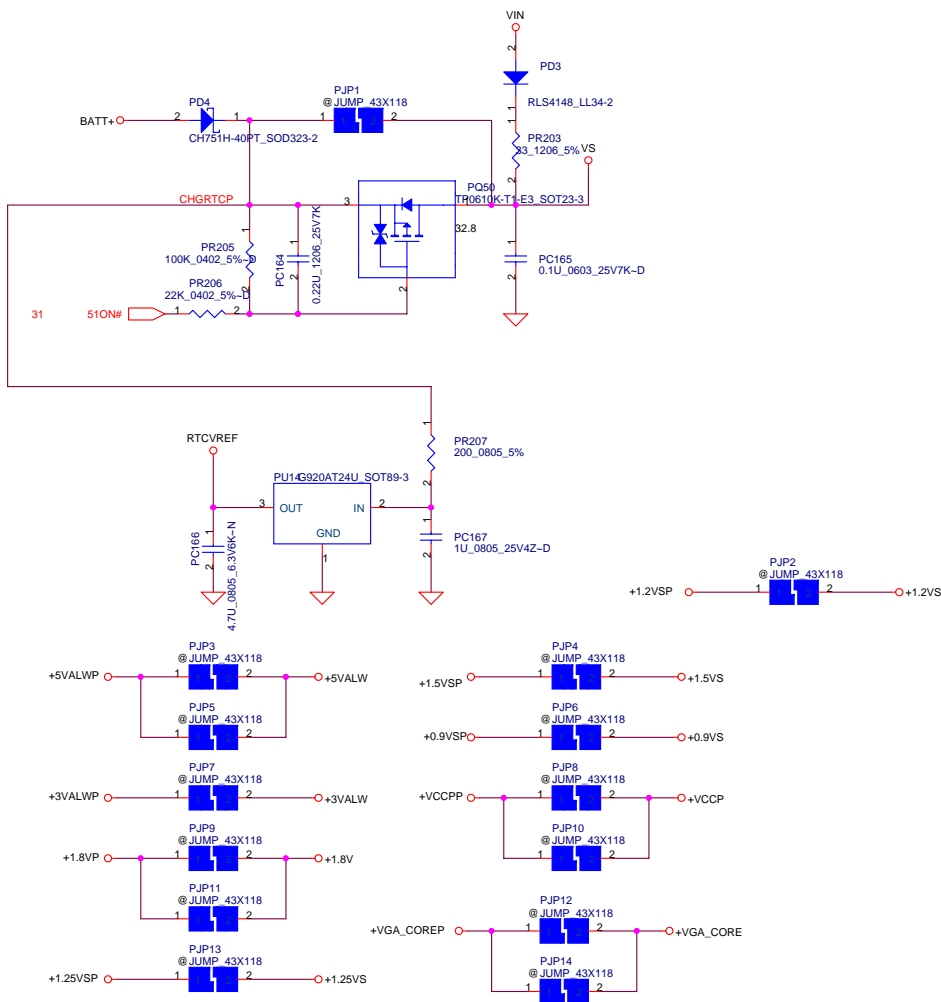
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Issued Date		2007/1/15	Deciphered Date		2008/1/15	Title
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						Document Number
LA-4231P						0.1
Date:		Thursday, January 10, 2008			Sheet 41 of 49	

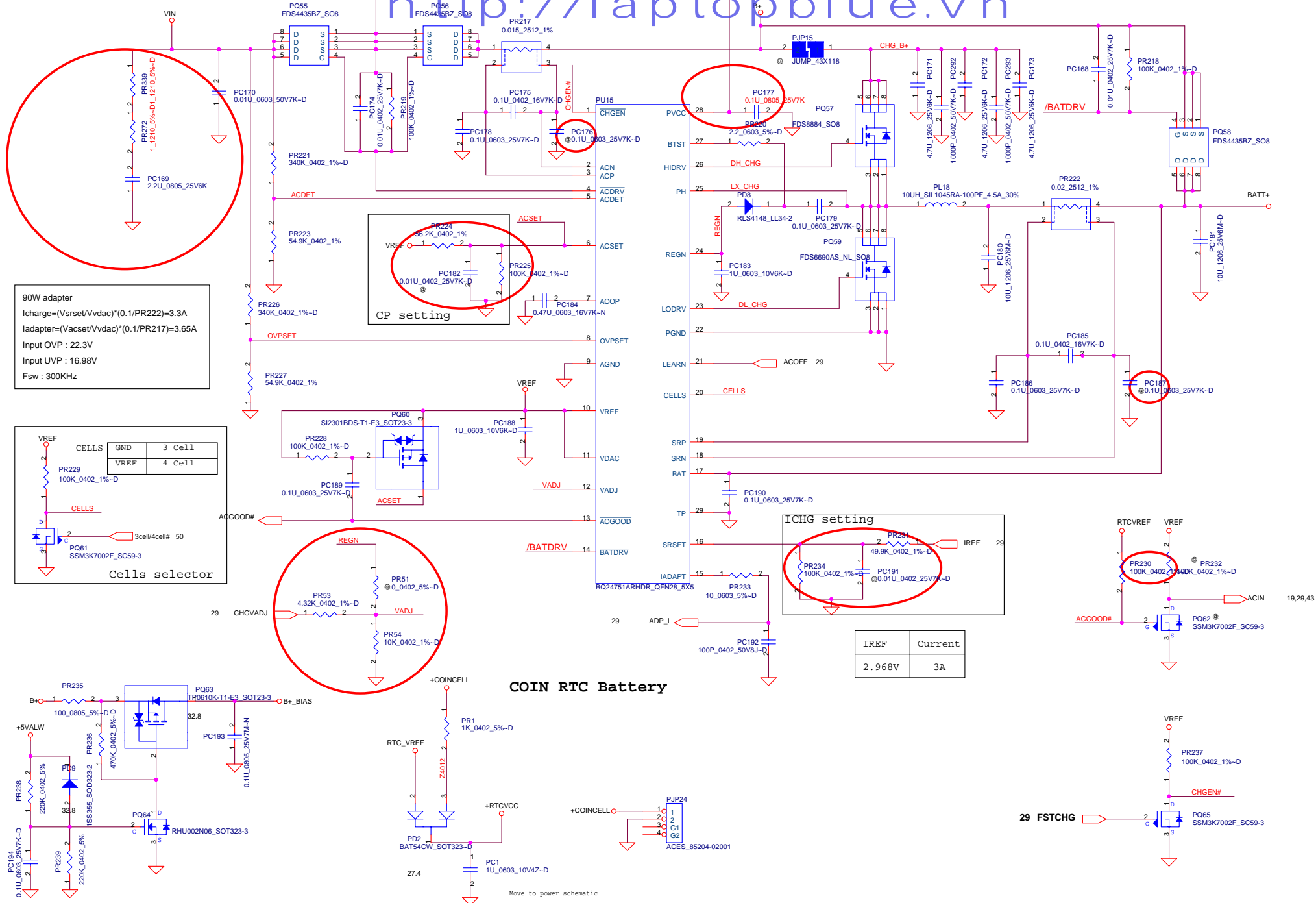


Security Classification	Compal Secret Data			Title	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Screws	
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				LA-4231P	0.1
				Date: Thursday, January 10, 2008	Sheet 42 of 49



	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813

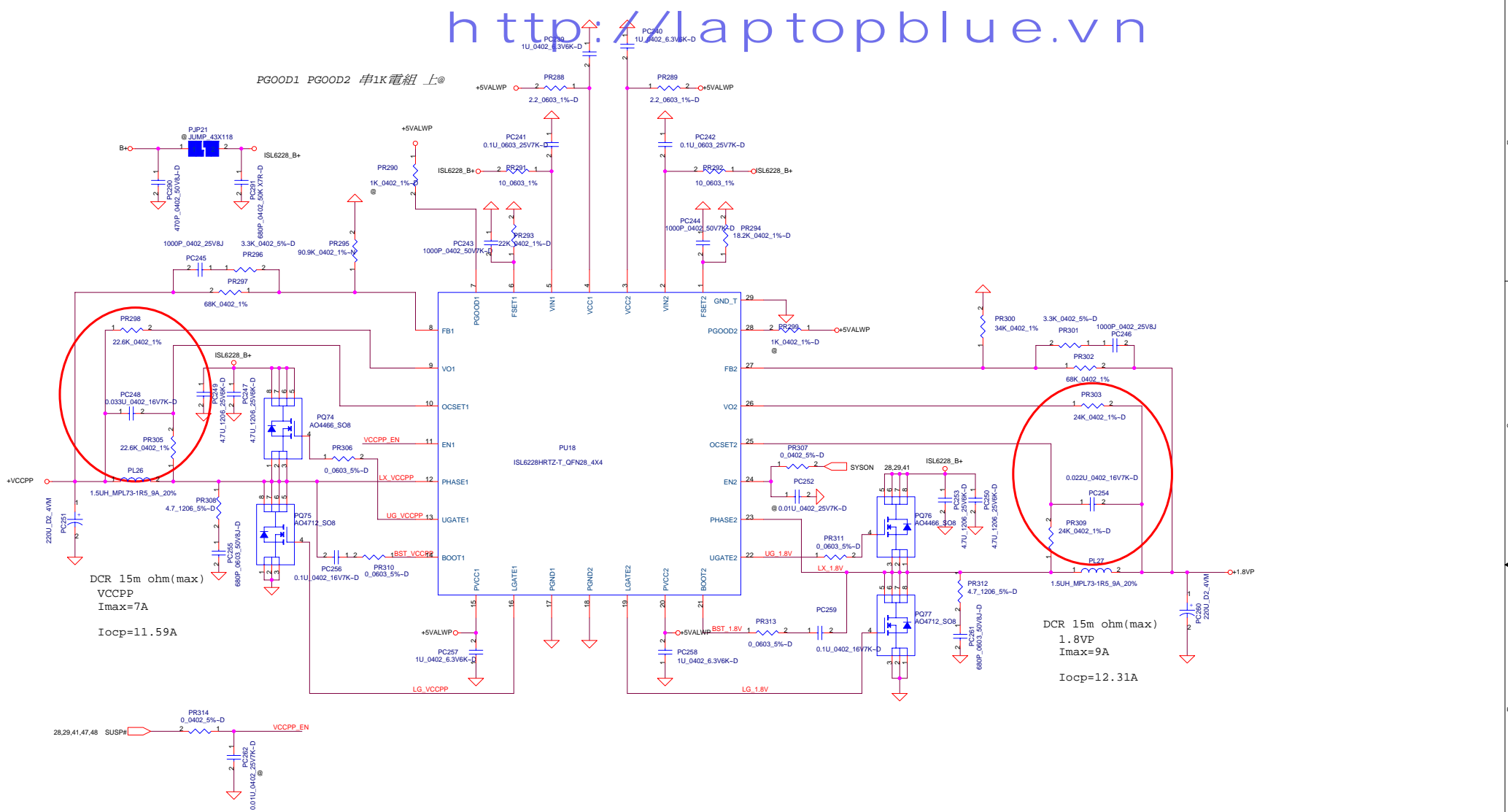




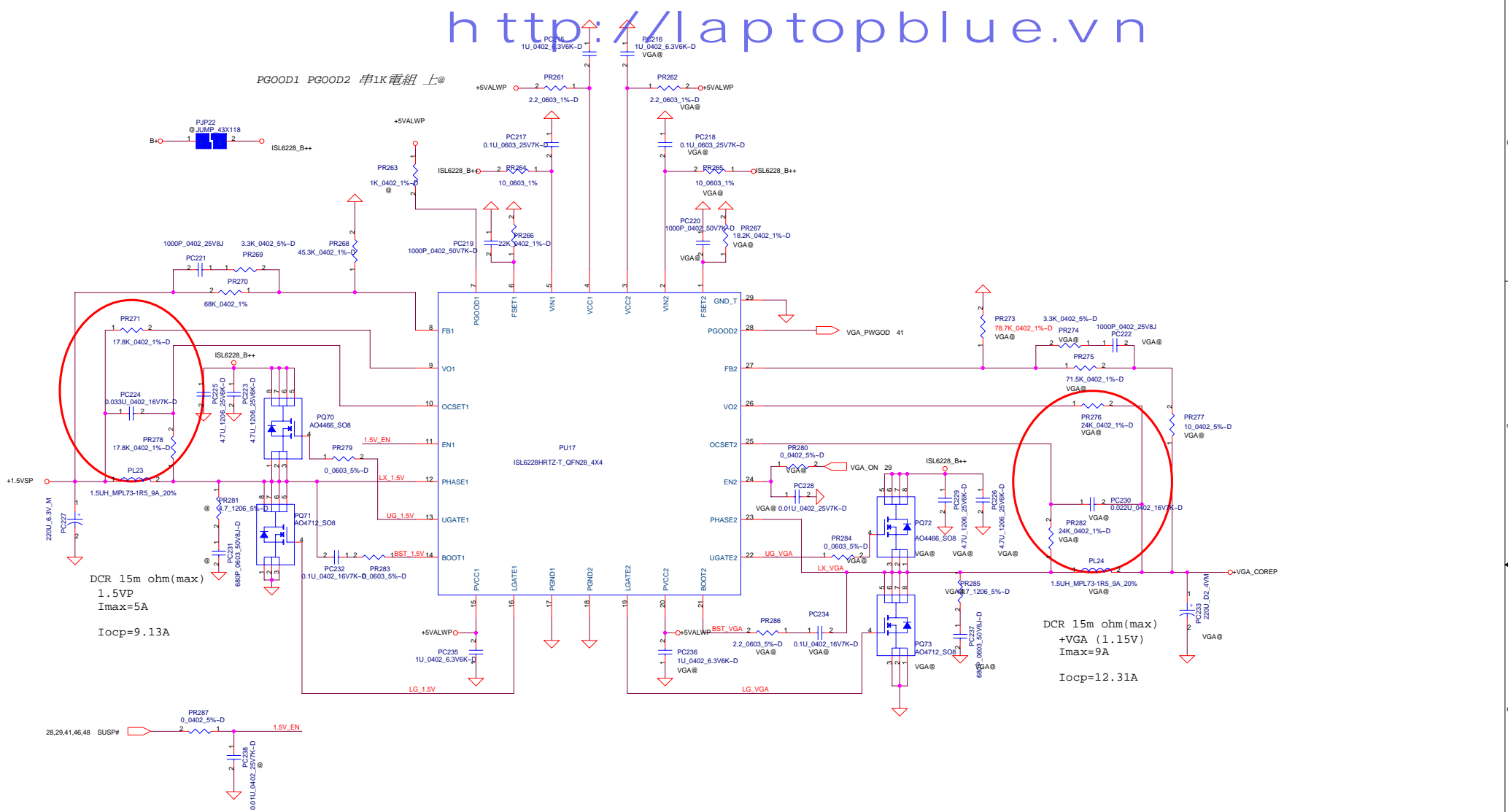
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2006/10/1	Deciphered Date	2007/5/01	Charger			
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				JAL80			

Date: Thursday, January 10, 2008				Sheet 44 of 9			

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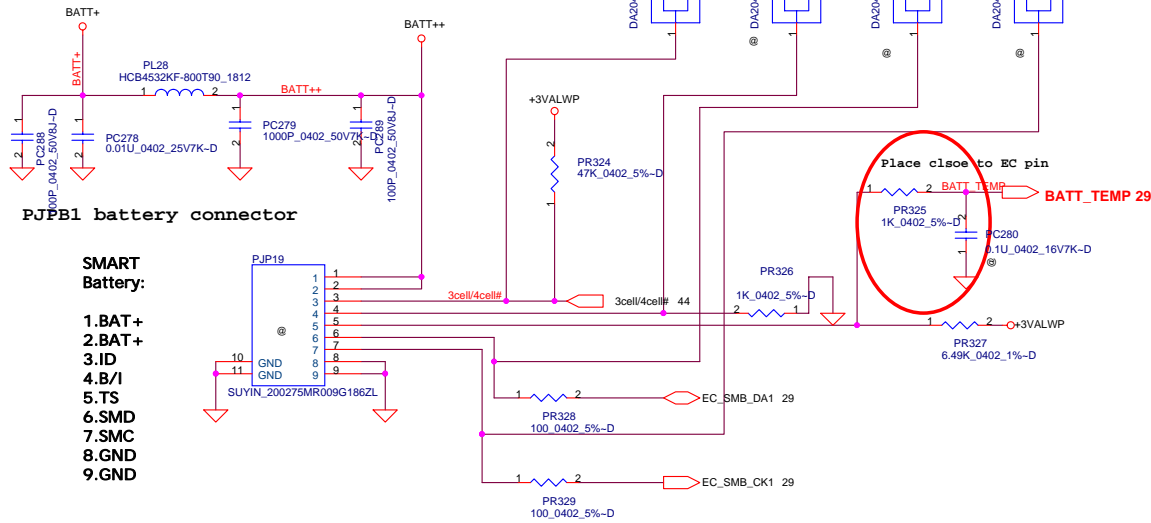


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Security Classification	Compal Secret Data			
Issued Date	2006/10/1	Deciphered Date	2007/5/01	Title
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				JAL80
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Date: Thursday, January 10, 2008		Sheet 47 of 9		

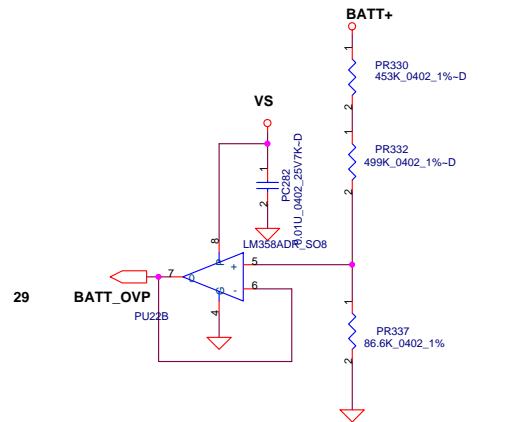
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Issued Date		2005/10/1		Deciphered Date		2007/05/30	
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				+1.25VSP / +0.9VSP/ +1.2VSP			
				Document Number		Rev	
				JAL80		0.2	
				Date:		Thursday, January 10, 2008	
				Sheet		48 of 9	



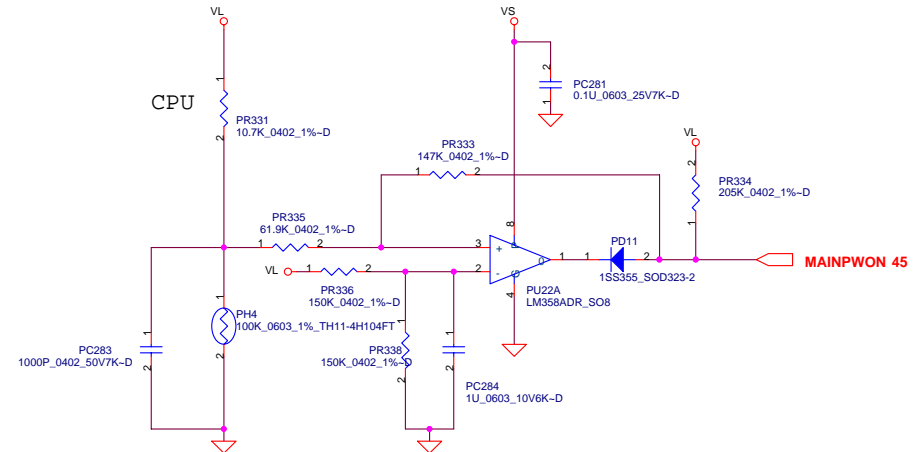
Battery Connect/OTP

CPU

PH1 under CPU bottom side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C



LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.111*BATT+



Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	board rev update to 0.2	R231 change to 15K & R232 pop	0.2
2	40	P40-O2129_Card Reader/1394	07/10/30	compal	CardBus vendor change	CardBus R5C833 change to O2129	0.2
3	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Change pull up resistance	Change EC pin17,18 pull up to 4.7Kohm	0.2
4	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Need pull up	NET MIC_DIAG pull up R to 10Kohm 3VS	0.2
5	13,14	DDR2 SODIMM-I,II Socket	07/10/30	compal	Change Capacitance	Change C84,C189 to SGA00002680 330U	0.2
6	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	EC update rev	EC change to 926C	0.2
7	28	P28-Express card	07/10/30	compal	Express card can't detect	POWER IC(U11) ADD PIN10 CPUSB# PIN9 EXPR_CPUSB#S	0.2
8	32	P32-USB/ BlueTooth/ FP/ Felica	07/10/30	compal	Bluetooth can't detect	BLUETOOTH CONN USB+- change	0.2
9	42	P42-Screws	07/10/30	compal	FIDUCAL no enough	ADD FIDUCAL*4	0.2
10	41	P41-DC/DC Interface	07/10/30	compal	Need pull down	SYSON pull down 10K ohm	0.2
11	41	P41-DC/DC Interface	07/11/12	compal	USB can't detect	SUSP change to 5VALW(Q32)	0.2
12	06	P06-Merom(3/3)-GND/Bypass	07/11/12	compal	Change CPU High Freqeunce Decoupling Capacitance	C195 change to C1150-C1181	0.2
13	41	P41-DC/DC Interface	07/11/13	compal	+1.8VS Discharge error	+1.8VS Discharge circuit Q65 net change to VGA_PWGOD#	0.2
14	41	P41-DC/DC Interface	07/11/16	compal	Delete	Remove SIM card connector	0.2
15	42	P42-Screws	07/11/16	compal	Change Holea size	Change Holea size 2.5 to 2.8, change 3.5 to 3.8	0.2
16	31	P31-PWR_OK/ BTN/ KB / TouchPad	07/11/21	compal	Change Touch PAD/B connector	Touch PAD/B connector change net	0.2
17	15	P15-CRT Conn.& LCD Conn.	07/11/21	compal	Add LCD control pin	Add LCD control pin LCD_CBL_DET# & LCD_TST & LCD_VCC_TEST_EN	0.2
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	+3VALWP/+5VALWP	07/11/19	COMPAL	When in the DC-mode , shut down the system ,5valwp output not turn off	ADD PQ79 to turn off 5VALWP wehn shut down the system in the DC-mode	
2	44	Charge	07/12/26	COMPAL	change charge voltage can to adjust	Change PR53 from 15K to 4.3K	
3	49	CPU_CORE	07/12/26	COMPAL	Increase Resistor 0ohm on CPU_CORE high side gate for EMI request	ADD PR163 PR184	
4	45	+3VALWP/+5VALWP	07/12/26	COMPAL	The schematic location is wrong	DEL PL19	
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