

COMPAL CONFIDENTIAL

MODEL NAME : *BDW00*

COMPAL P/N : *DA8DW00L110/DA8DW00L410*

PCB NO : *LA-1452*

Revision : *1C*

DATE :

Abacus/TangII Schematics Document

uFCBGA/uFCPGA Northwood

2003-02-24

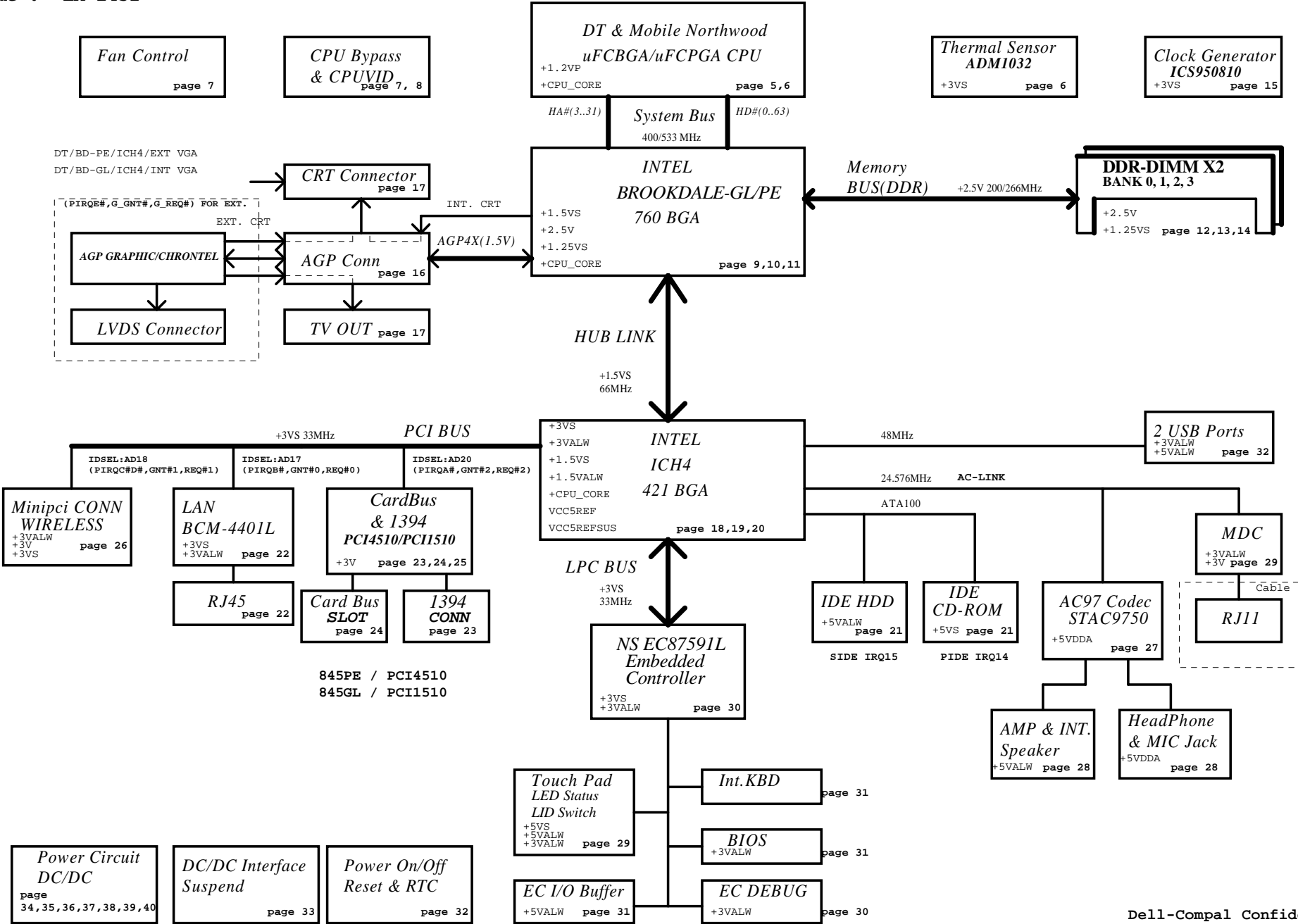
REV: 1C

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Revision List

	Schematics Rev	PCB Rev	CHIPS Rev
SST-Build	0.1	0.1	
PT-Build	0.2	0.2	845PE Rev B0 845GL Rev B1 ICH4 Rev B0
ST-Build			
QT-Build			

Ceramic Capacitor Spec Guide:

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7
CODE	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R

8	9	A	B	C	D	E	F	G
NP0	C0G		BJ	CH	CJ	CK	SH	SJ

H	I	J	
UJ	UK	SL	

Tolerance:

Symbol	A	B	C	D	F	G	H	J
CODE	+/-0.05PF	+/-0.1PF	+/-0.25PF	+/-0.5PF	+/-1PF	+/-2%	+/-3%	+/-5%

K	M	N	P	Q	V	X	Z	
+/-10%	+/-20%	+/-30%	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) (U57)	THERMAL SENSOR (U25/U23)	SODIMM	CLK CHIP	MINI PCI
SMB_EC_CK1 SMB_EC_DA1	NS 87591	✓	✓	✓ (1010)	✗	✗	✗	✗	✗
SMB_EC_CK2 SMB_EC_DA2	NS 87591	✗	✗	✗	✓	✓	✗	✗	✗
SMB_CLK SMB_DATA	ICH4	✗	✗	✗	✗	✗	✓	✓	✓

Power Managment table

Signal State	+3VALW +5VALW +12VALW	+3V +5V +2.5V	+3VS +5VS +1.5VS +1.2VP +CPU_CORE +1.25VS
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

NOTE1:

@XX : Depop component

1@XX : Pop for INT, Depop for EXT

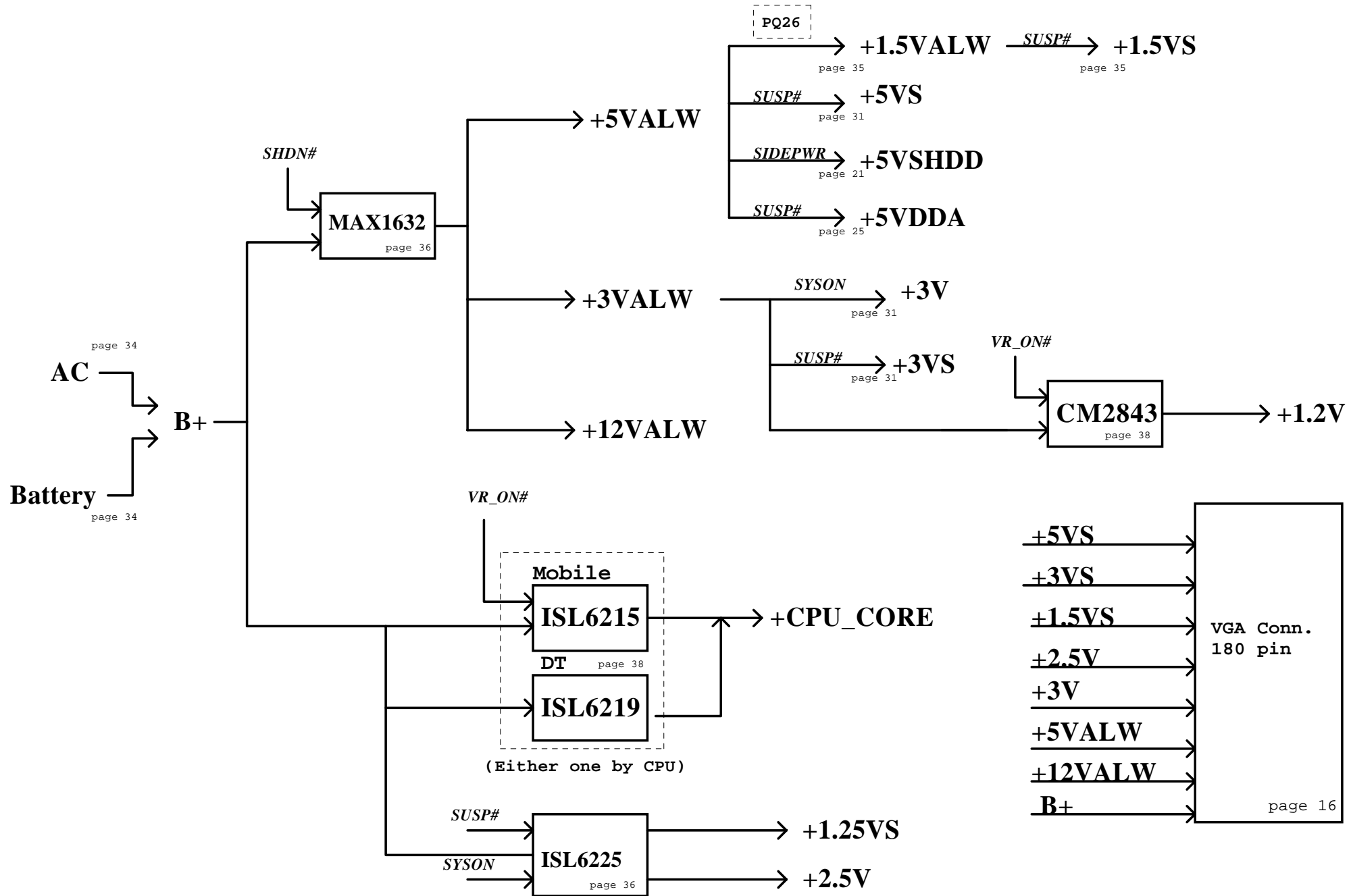
2@XX : Pop for EXT, Depop for INT

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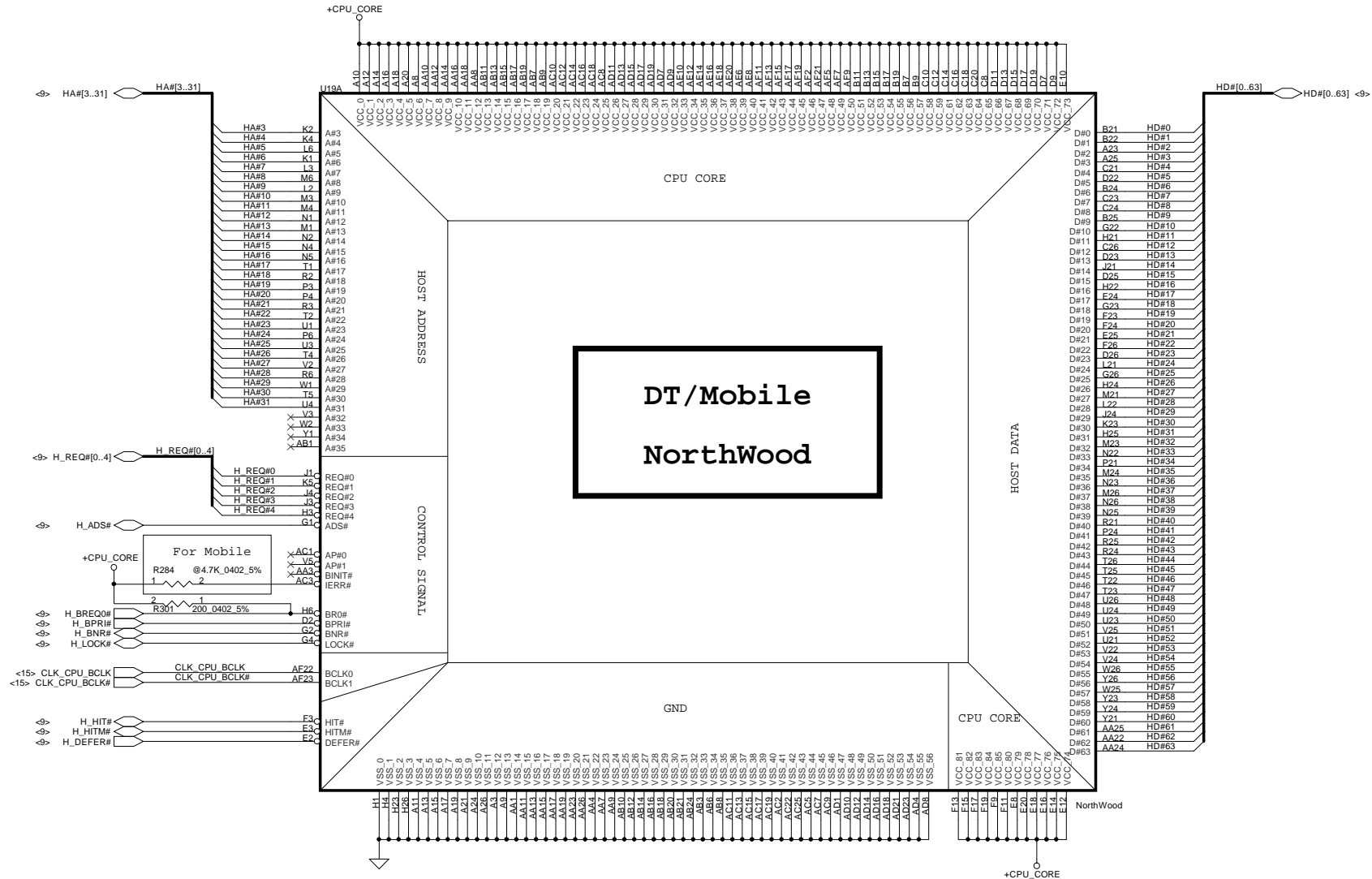


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Place close to CPU, Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

Three circuit diagrams are shown, each representing a different configuration for connecting a CPU_CORE to ground through a series of capacitors. Each diagram consists of a horizontal line representing the signal path, with a vertical line representing the ground connection. The capacitors are connected in series between the signal path and ground.

- Top Diagram:** The signal path is labeled **+CPU_CORE**. It shows a series of five capacitors: C388, C408, C400, C258, and C293. Each capacitor is labeled with its value: 10U_1206_6.3V7K. The ground connection is indicated by a triangle symbol.
- Middle Diagram:** The signal path is labeled **+CPU_CORE**. It shows a series of five capacitors: C411, C410, C257, C402, and C401. Each capacitor is labeled with its value: 10U_1206_6.3V7K. The ground connection is indicated by a triangle symbol.
- Bottom Diagram:** The signal path is labeled **+CPU_CORE**. It shows a series of four capacitors: C403, C405, C291, and C99. Each capacitor is labeled with its value: 10U_1206_6.3V7K. The ground connection is indicated by a triangle symbol.

The image displays three schematic diagrams of power distribution networks for a CPU_CORE. Each diagram shows a series of capacitors connected in parallel between a power rail and ground.

- Top Diagram:** Shows a power rail connected to ground through capacitors C122, C121, C356, C62, and C404. The capacitors are labeled with their values: C122 (10U_1206_6.3V7K), C121 (10U_1206_6.3V7K), C356 (10U_1206_6.3V7K), C62 (10U_1206_6.3V7K), and C404 (10U_1206_6.3V7K).
- Middle Diagram:** Shows a power rail connected to ground through capacitors C351, C292, C368, C100, and C296. The capacitors are labeled with their values: C351 (10U_1206_6.3V7K), C292 (10U_1206_6.3V7K), C368 (10U_1206_6.3V7K), C100 (10U_1206_6.3V7K), and C296 (10U_1206_6.3V7K).
- Bottom Diagram:** Shows a power rail connected to ground through capacitors C409, C64, C68, and C66. The capacitors are labeled with their values: C409 (10U_1206_6.3V7K), C64 (10U_1206_6.3V7K), C68 (10U_1206_6.3V7K), and C66 (10U_1206_6.3V7K).

Place close to CPU power and ground pin as possible (<1inch)

For Mobile's CPU:
ESR total=1.875m ohm
C_{total}=2580uF

For Mobile's CPU:
ESR total=1.875m ohm
C_{total}=2580uF

For DT

+CPU_CORE

C390 4700U_D4_2.5VM

C371 4700U_D4_2.5VM

C261 4700U_D4_2.5VM

C147 4700U_D4_2.5VM

C263 4700U_D4_2.5VM

+CPU_CORE

C352 4700U_D4_2.5VM

C259 4700U_D4_2.5VM

C148 @4700U_D4_2.5VM

C149 4700U_D4_2.5VM

C150 @4700U_D4_2.5VM

+CPU_CORE

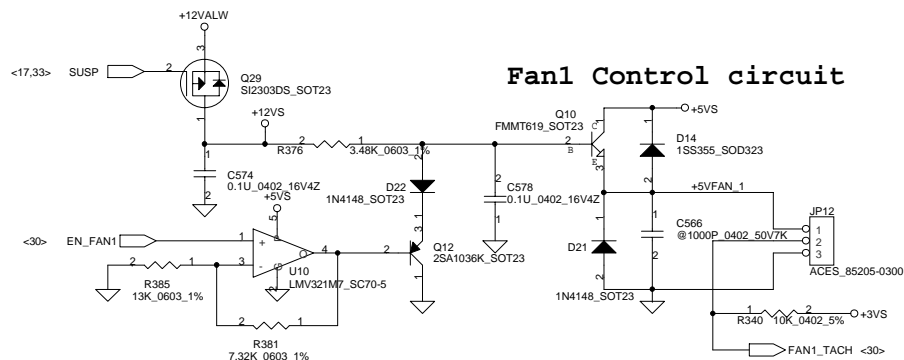
C151 330U_D_2.5VM

C152 @330U_D2E_2.5VM

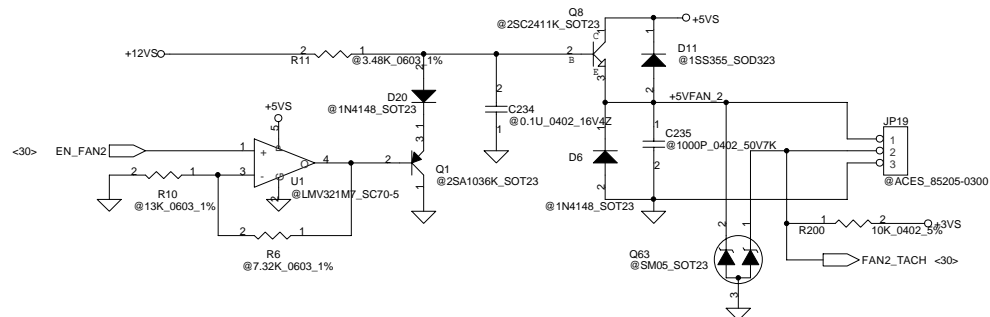
C265 330U_D_2.5VM

C262 330U_D_2.5VM

C266 330U_D_2.5VM



Fan2 Control circuit

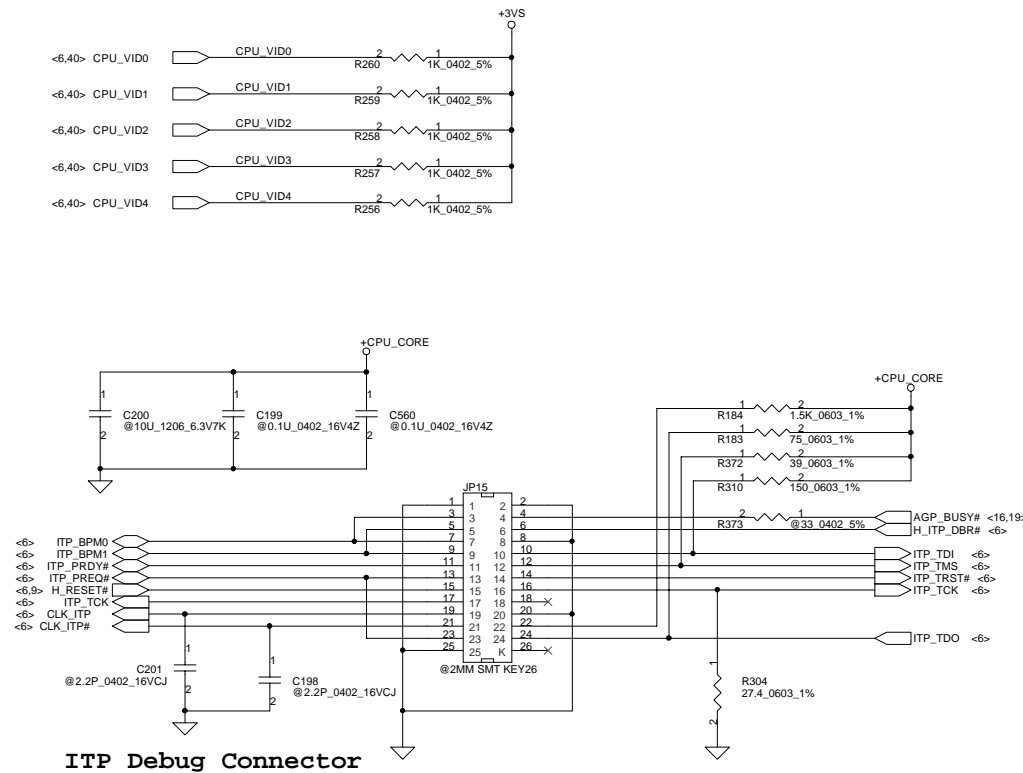


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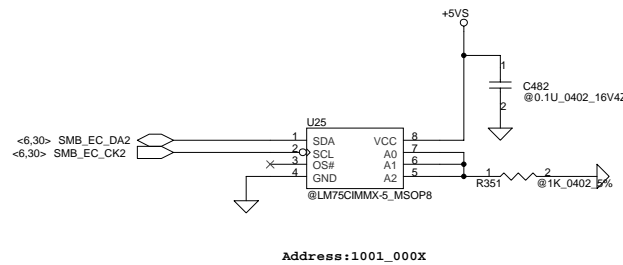
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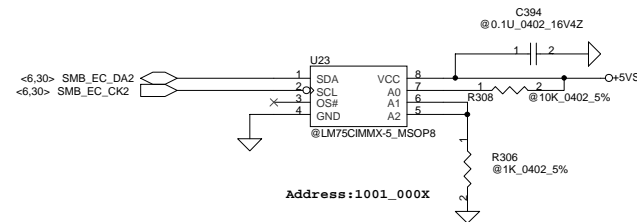
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ITP Debug Connector



Address:1001_000X



Address:1001_000X

MO/DT_CPU	Mobile CPU					Desktop CPU				
	1					0				
VID	4	3	2	1	0	4	3	2	1	0
VCC										
1.750V	0	0	0	0	0	0	0	1	0	0
1.700V	0	0	0	0	1	0	0	1	1	0
1.650V	0	0	0	1	0	0	1	0	0	0
1.600V	0	0	0	1	1	0	1	0	1	0
1.550V	0	0	1	0	0	0	1	1	0	0
1.500V	0	0	1	0	1	0	1	1	1	0
1.450V	0	0	1	1	0	1	0	0	0	0
1.400V	0	0	1	1	1	1	0	0	1	0
1.350V	0	1	0	0	0	1	0	1	0	0
1.300V	0	1	0	0	1	1	0	1	1	0
1.250V	0	1	0	1	0	1	1	0	0	0
1.200V	0	1	0	1	1	1	1	0	1	0
1.150V	0	1	1	0	0	1	1	1	0	0
1.100V	0	1	1	0	1	1	1	1	1	0
1.050V	0	1	1	1	0	X	X	X	X	X
1.000V	0	1	1	1	1	X	X	X	X	X
0.975V	1	0	0	0	0	X	X	X	X	X
0.950V	1	0	0	0	1	X	X	X	X	X
0.925V	1	0	0	1	0	X	X	X	X	X
0.900V	1	0	0	1	1	X	X	X	X	X
0.875V	1	0	1	0	0	X	X	X	X	X
0.850V	1	0	1	0	1	X	X	X	X	X
0.825V	1	0	1	1	0	X	X	X	X	X
0.800V	1	0	1	1	1	X	X	X	X	X
0.775V	1	1	0	0	0	X	X	X	X	X
0.750V	1	1	0	0	1	X	X	X	X	X
0.725V	1	1	0	1	0	X	X	X	X	X
0.700V	1	1	0	1	1	X	X	X	X	X
0.675V	1	1	1	0	0	X	X	X	X	X
0.650V	1	1	1	0	1	X	X	X	X	X
0.625V	1	1	1	1	0	X	X	X	X	X
0.600V	1	1	1	1	1	X	X	X	X	X
VRM output off						1	1	1	1	1

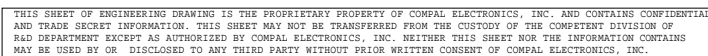
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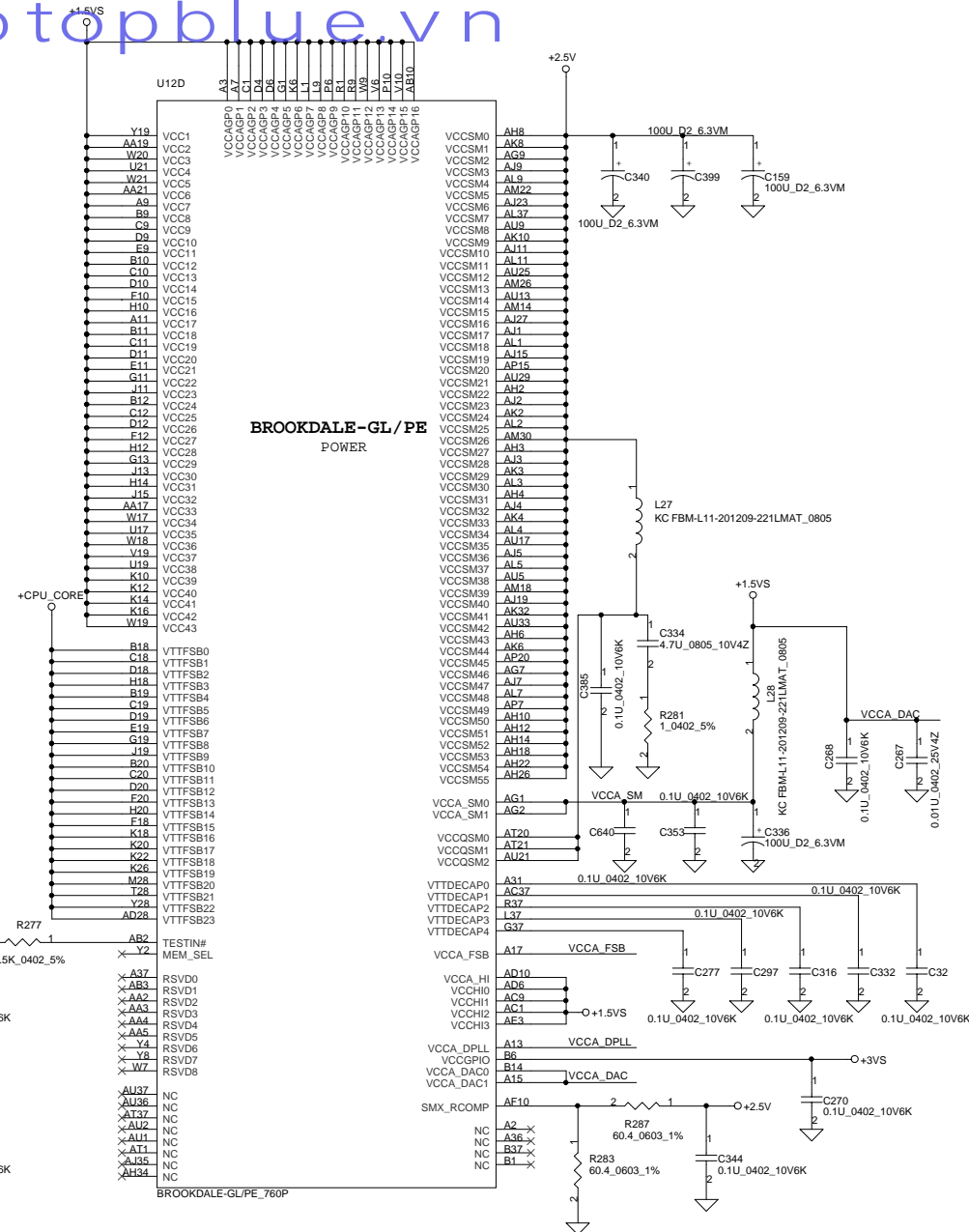
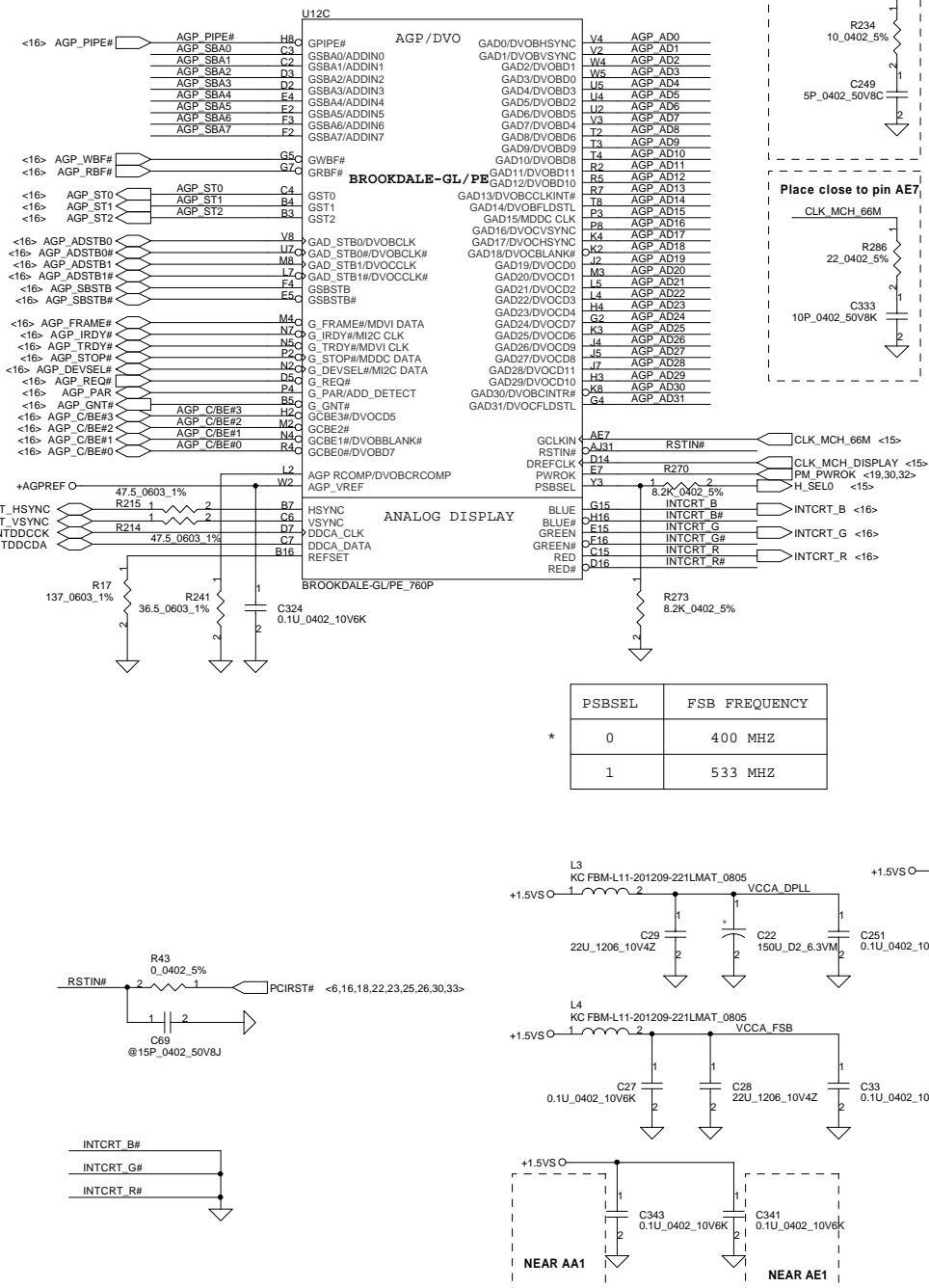
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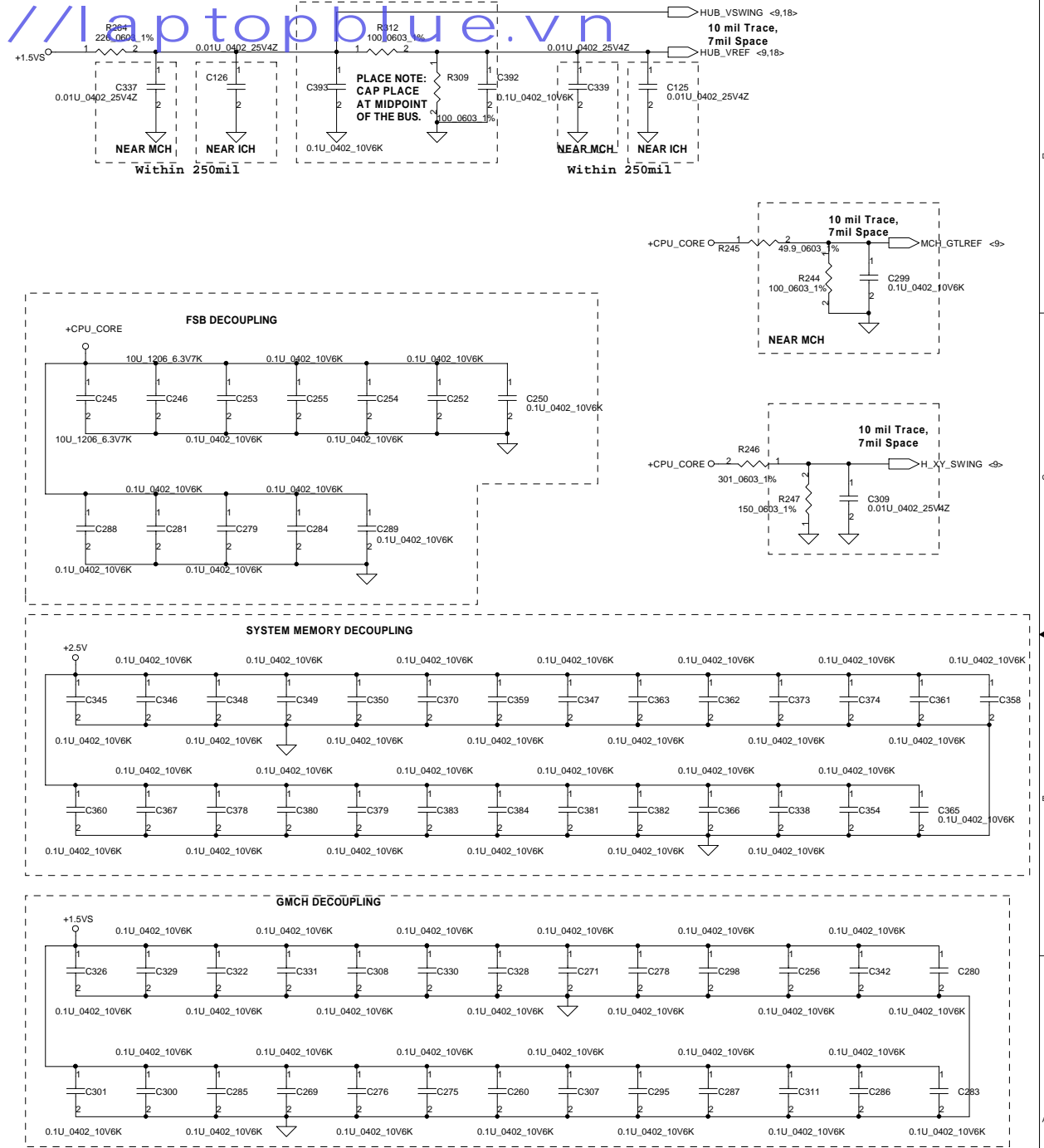
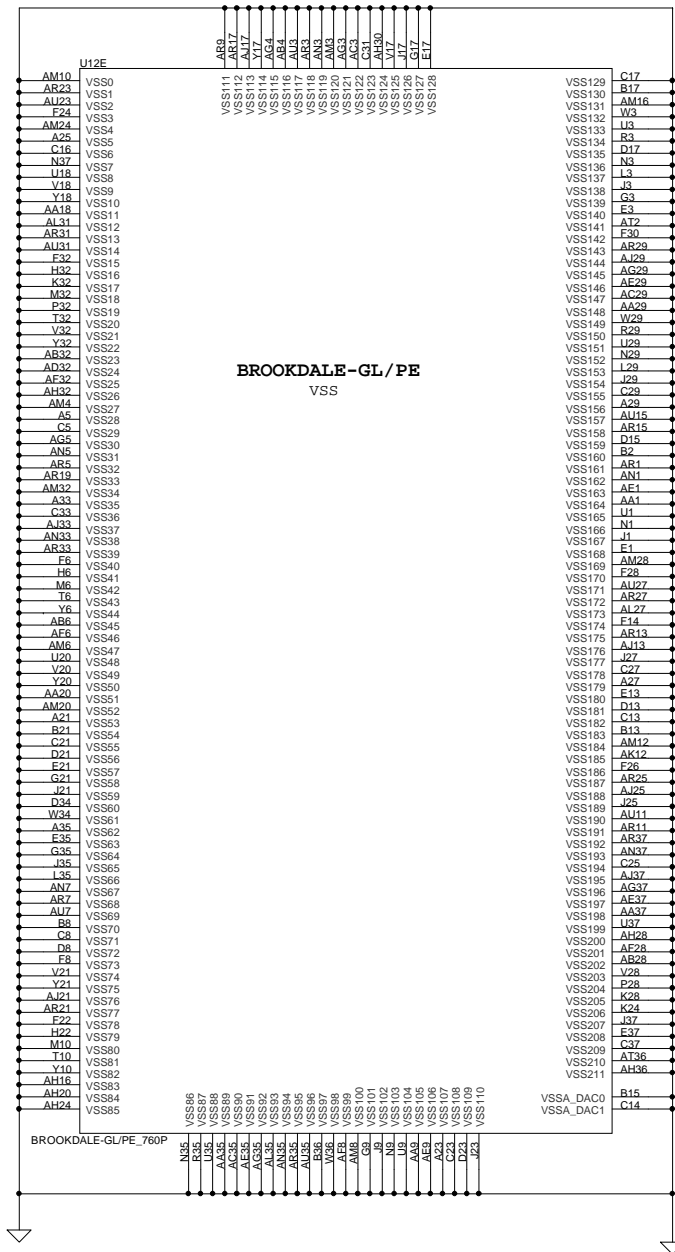
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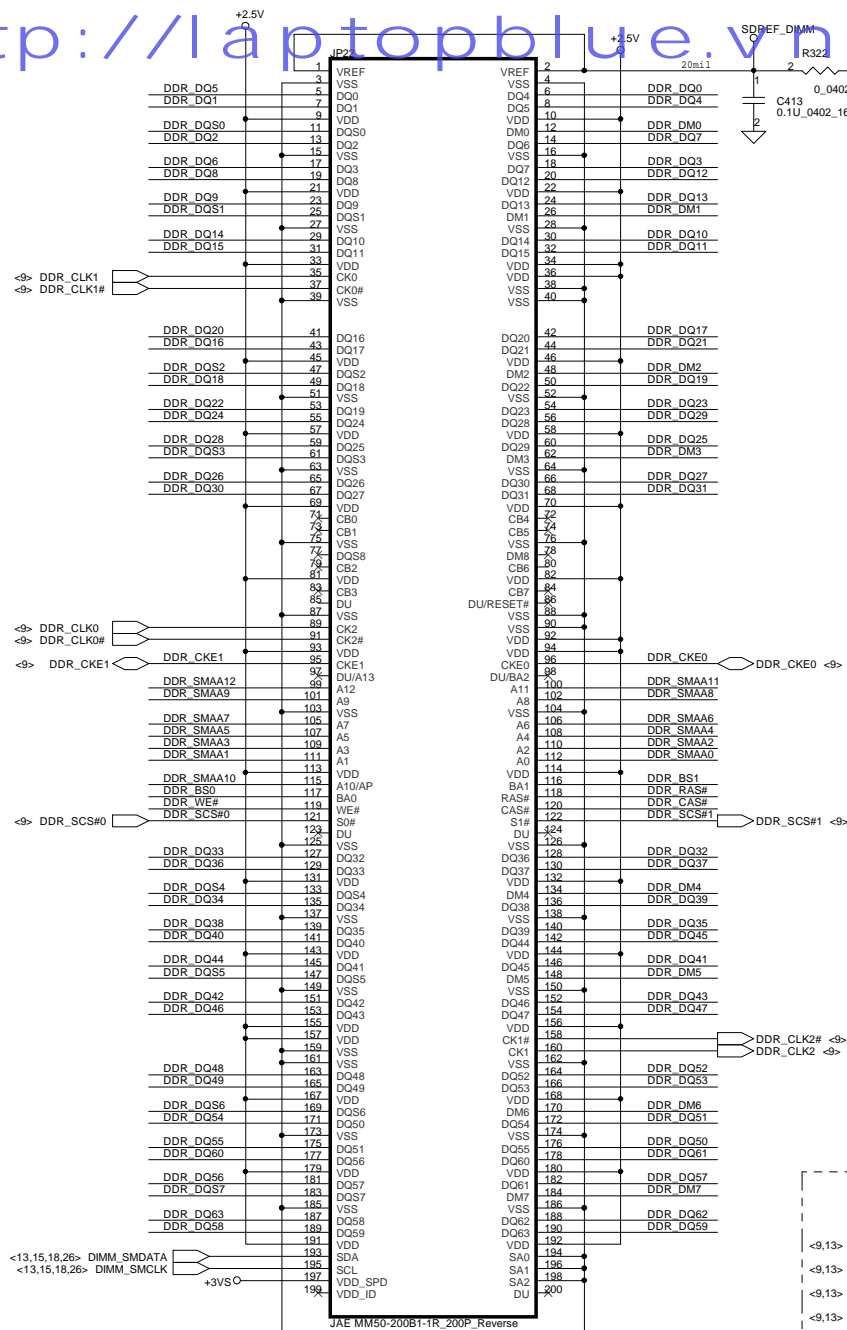
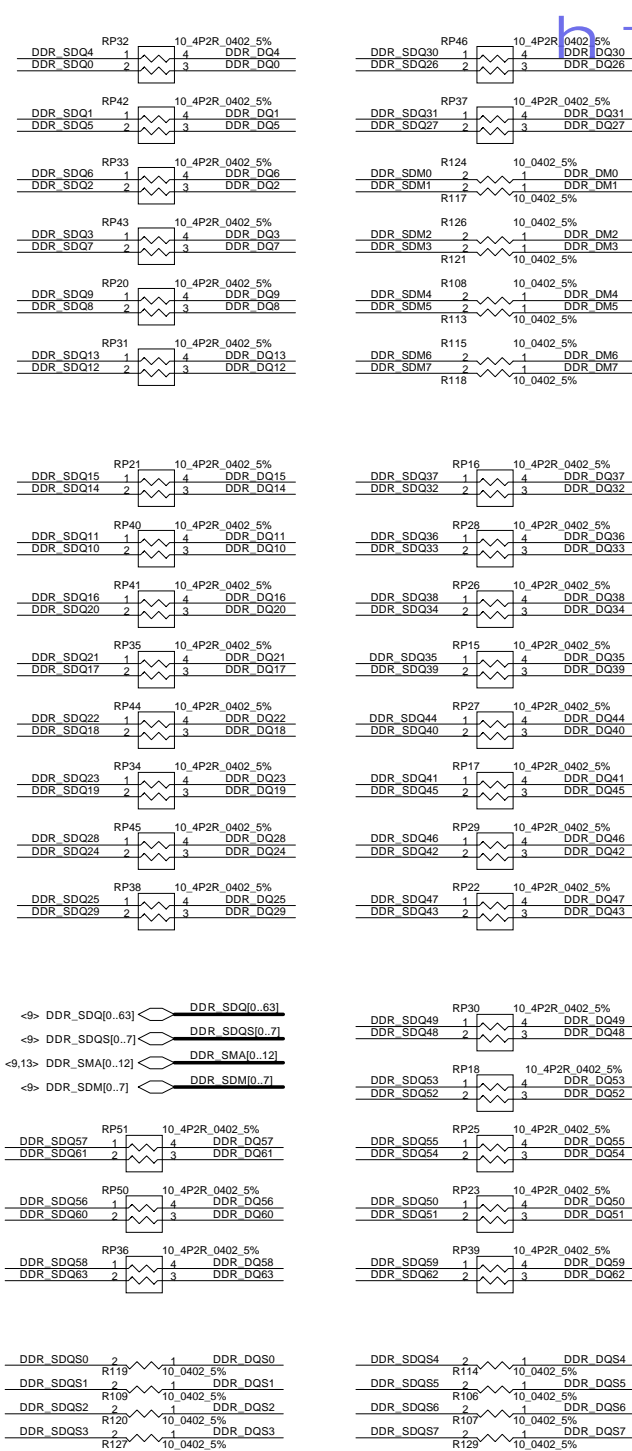
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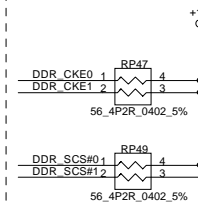
Layout note
Place these resistors
close to DIMM0,
all trace length<500 mil

DDR_DQ[0..63] <13>
DDR_DQS[0..7] <13>
DDR_DM[0..7] <13>
DDR_SMAA[0..12]

DDR_SMA0 2 1 DDR_SMAA0
DDR_SMA1 2 1 DDR_SMAA1
DDR_SMA2 2 1 DDR_SMAA2
DDR_SMA3 2 1 DDR_SMAA3
DDR_SMA4 2 1 DDR_SMAA4
DDR_SMA5 2 1 DDR_SMAA5
DDR_SMA6 2 1 DDR_SMAA6
DDR_SMA7 2 1 DDR_SMAA7
DDR_SMA8 2 1 DDR_SMAA8
DDR_SMA9 2 1 DDR_SMAA9
DDR_SMA10 2 1 DDR_SMAA10
DDR_SMA11 2 1 DDR_SMAA11
DDR_SMA12 2 1 DDR_SMAA12

Note:
Place Close to DIMM0

Layout note
Place these resistor
close by DIMM0,
all trace length
Max=1.4"



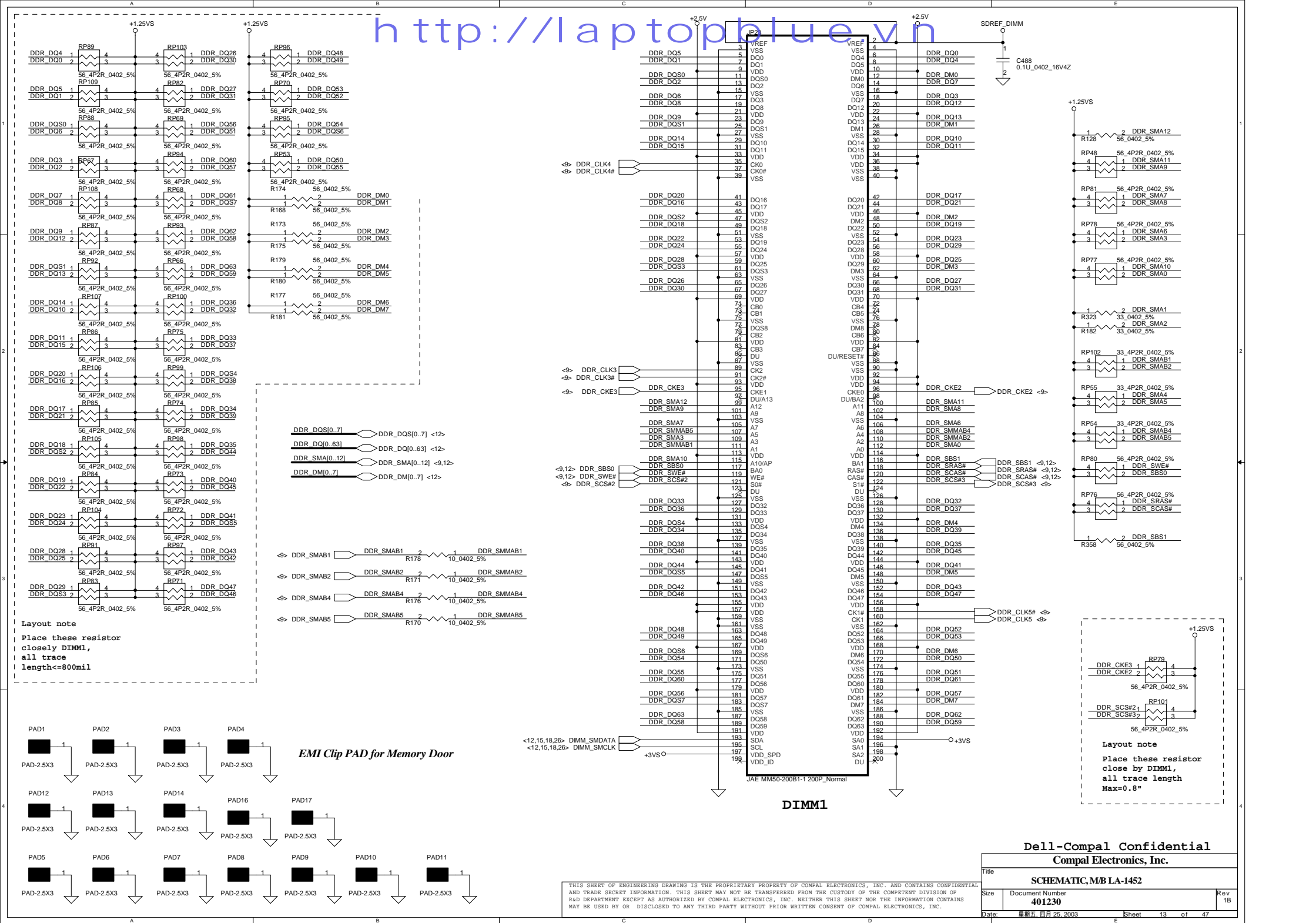
Note:
Place Close to DIMM0

<9.13> DDR_SB0 R139 10.0402 5% DDR_BS0
<9.13> DDR_SBS1 R133 10.0402 5% DDR_BS1
<9.13> DDR_SRAS# R141 10.0402 5% DDR_RAS#
<9.13> DDR_SCAS# R131 10.0402 5% DDR_CAS#
<9.13> DDR_SWE# R138 10.0402 5% DDR_WE#

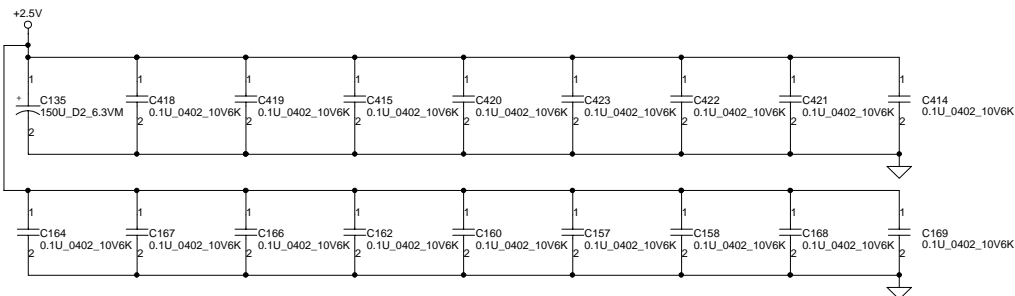
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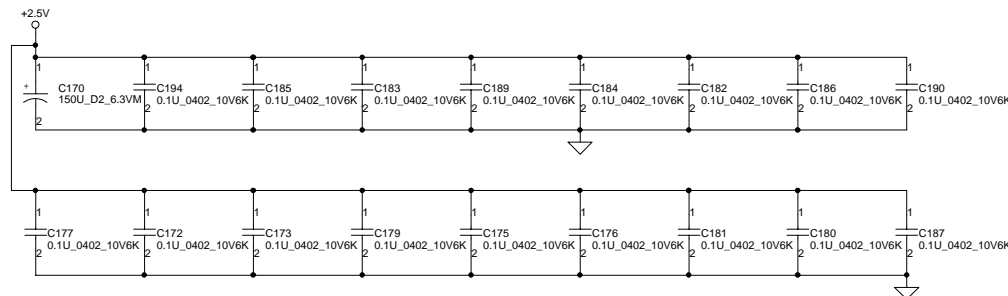
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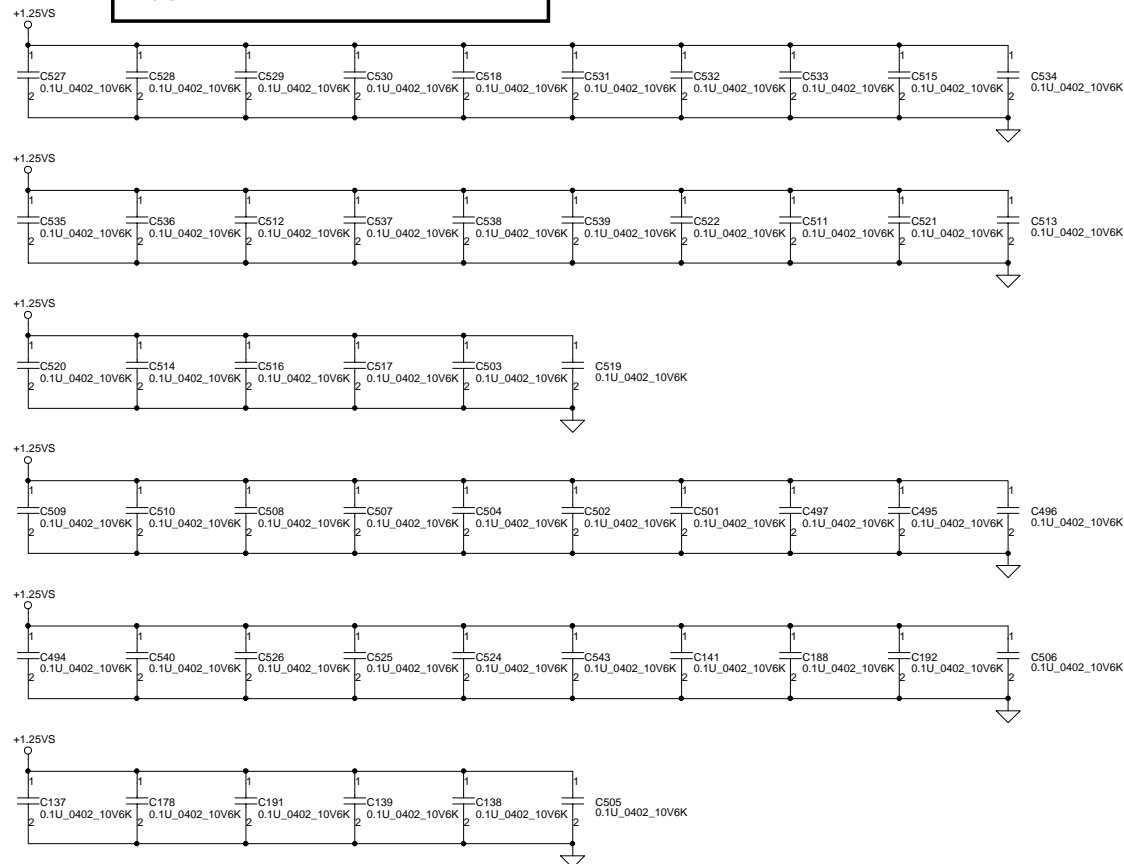
Layout note :
Distribute as close as possible
to DDR-SODIMM0.



Layout note :
Distribute as close as possible
to DDR-SODIMM1.



Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25VS

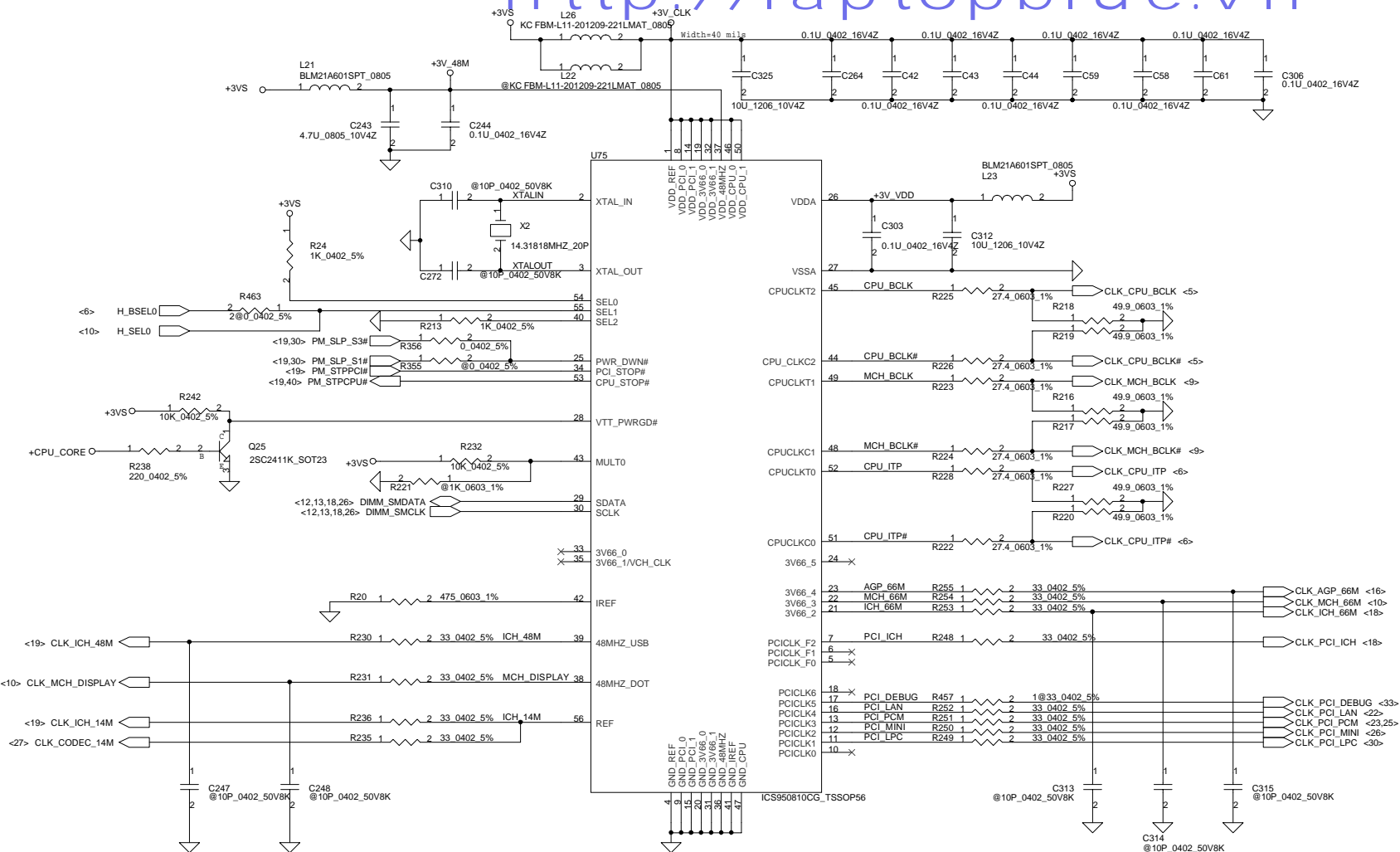


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CPU Frequency Select Table

SEL[2:0]	CK-408 Speed
001	100 MHZ
011	133 MHZ

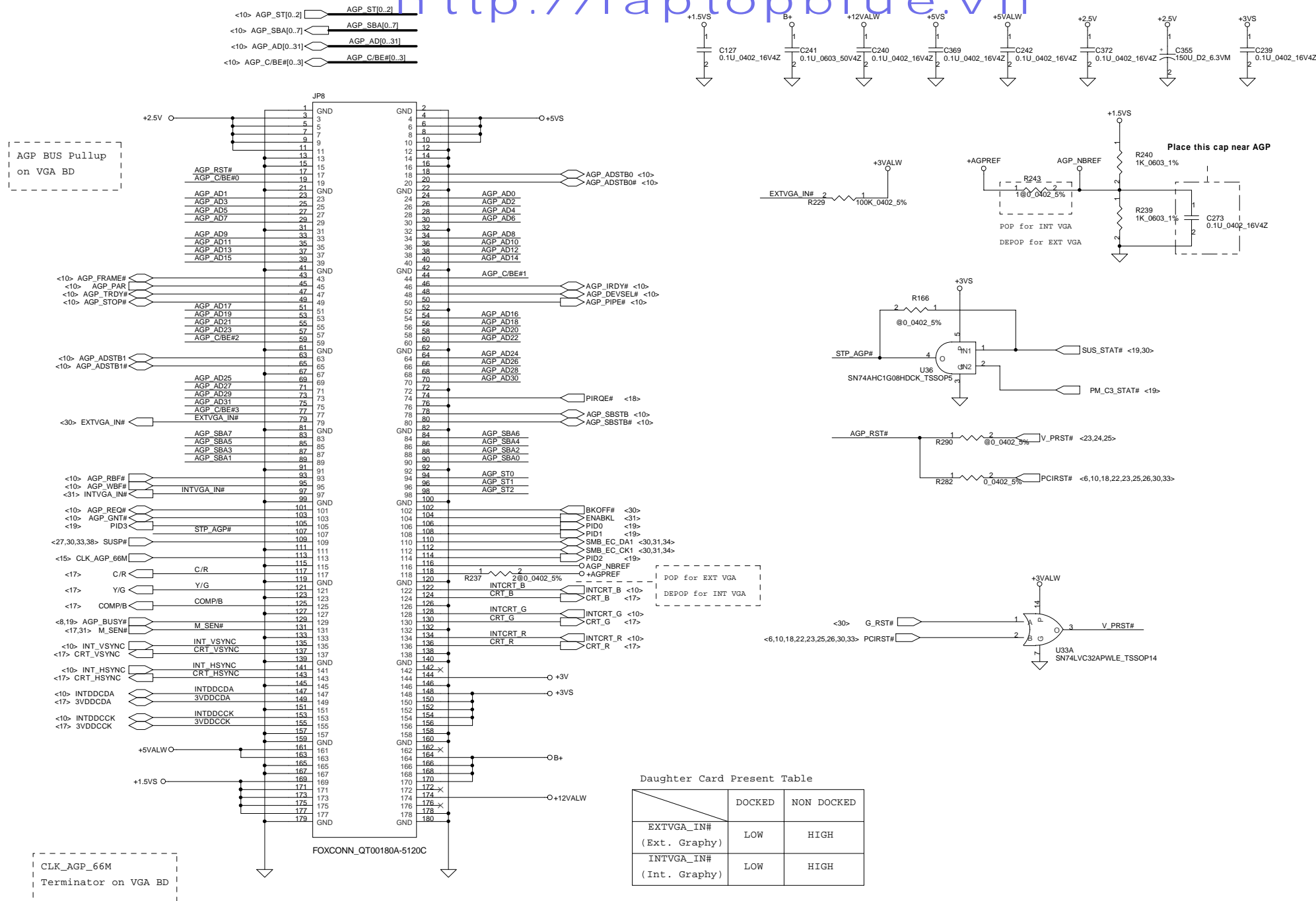
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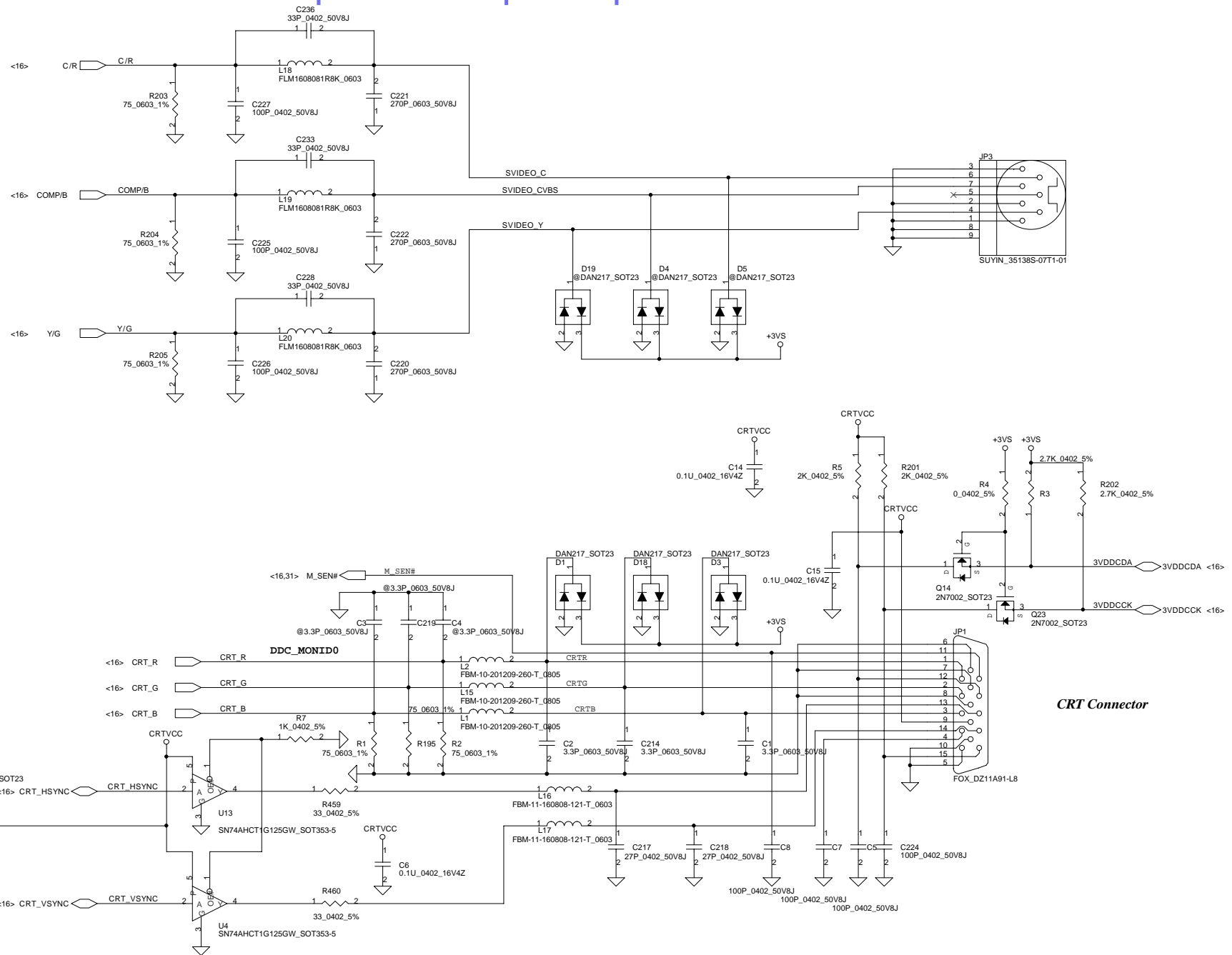
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CRT Connector

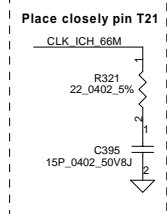
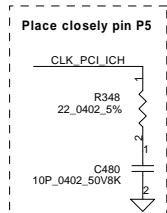
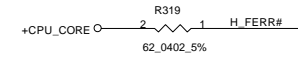
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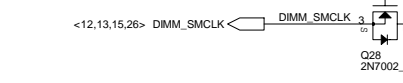
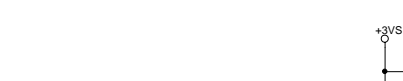
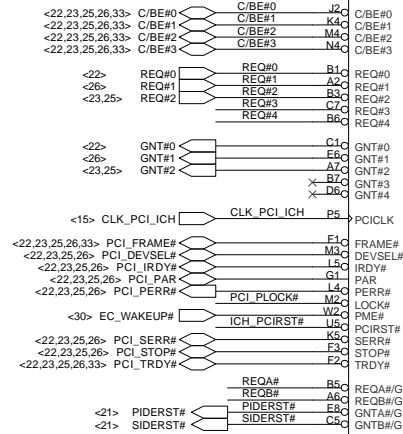
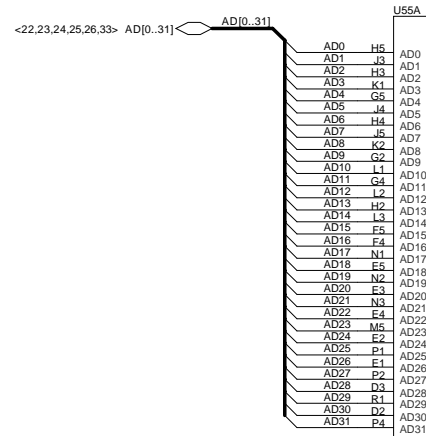
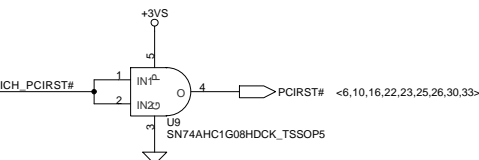
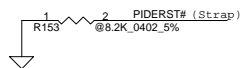
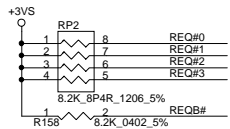
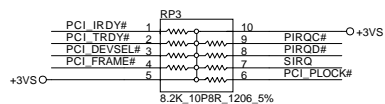
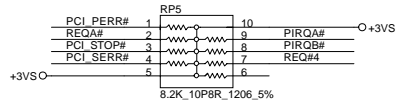
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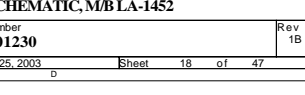
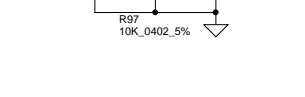
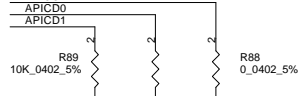
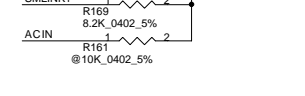
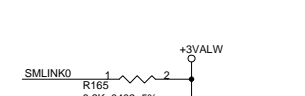
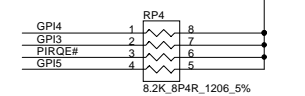
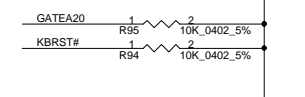
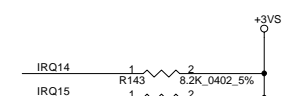
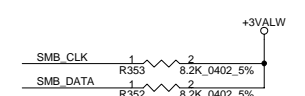
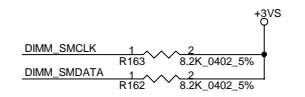
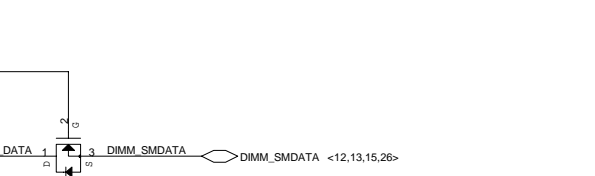
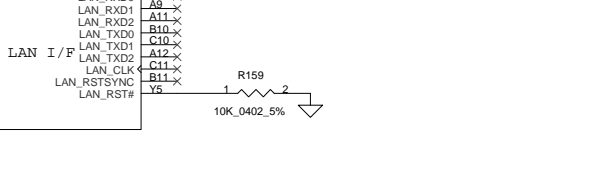
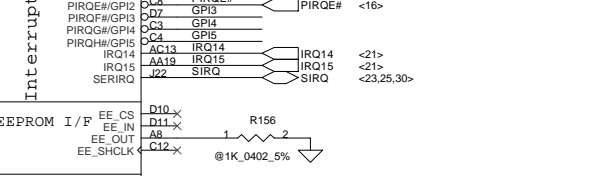
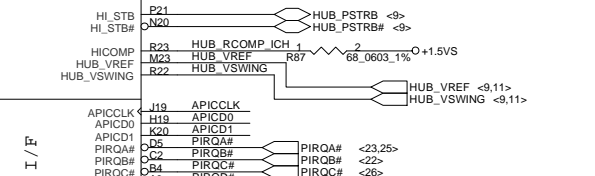
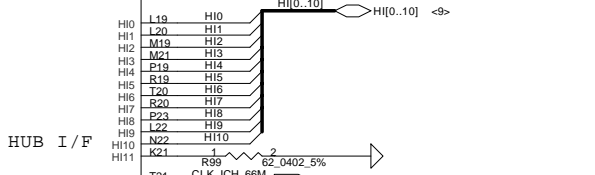
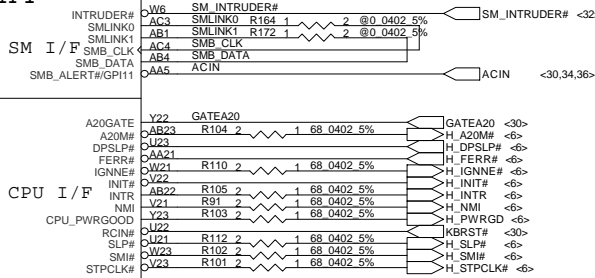
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PCI Pullups



ICH4



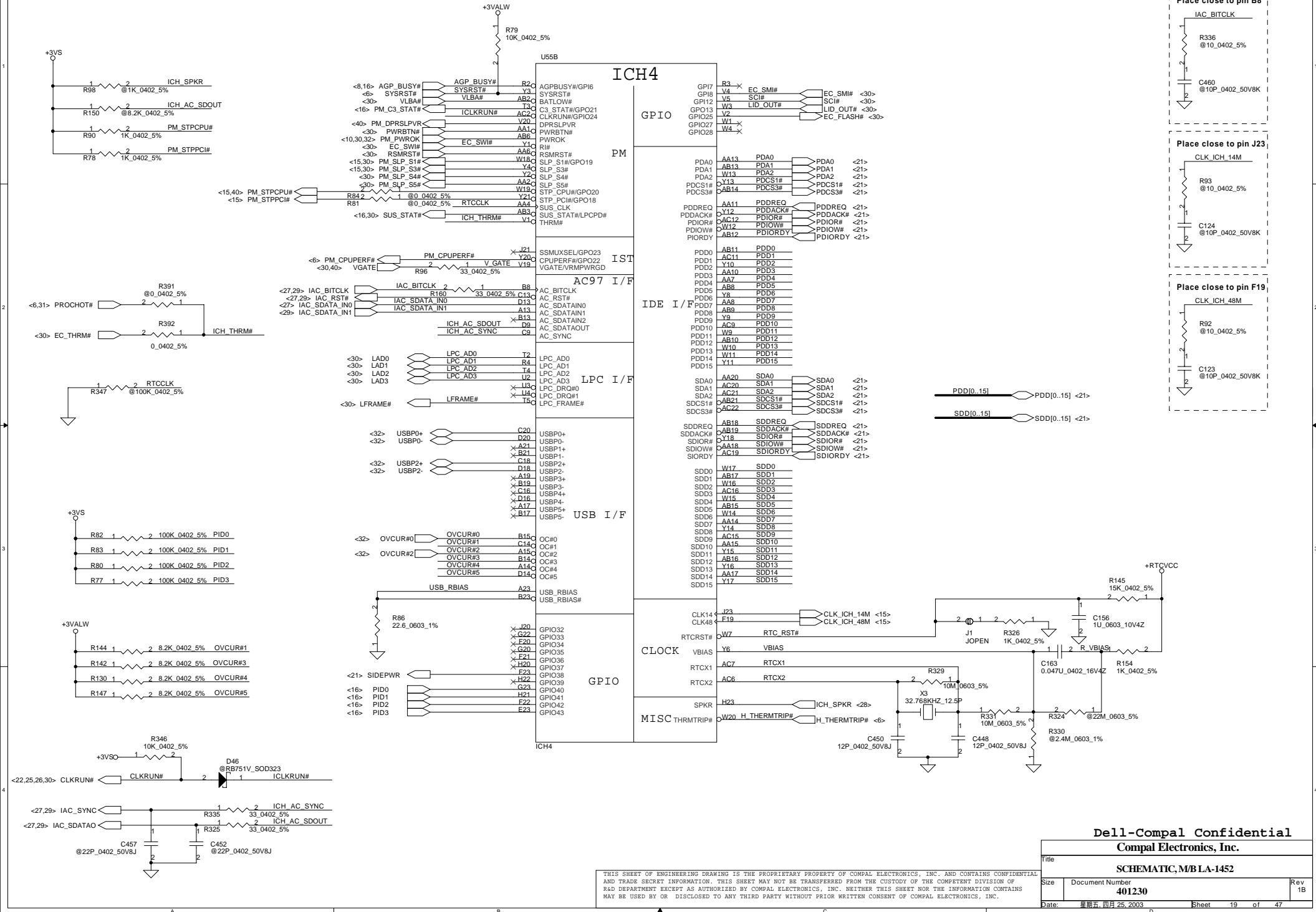
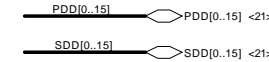
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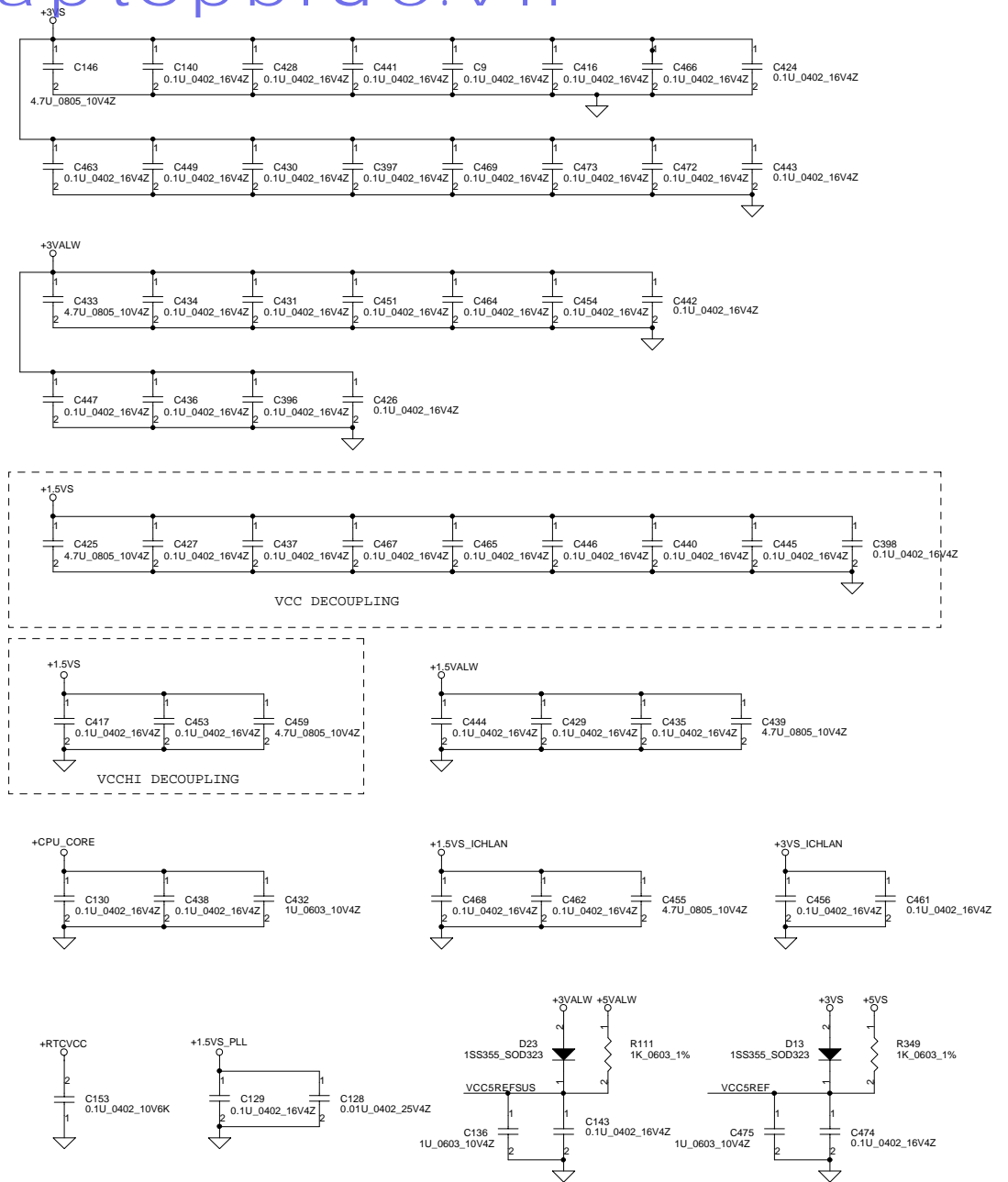
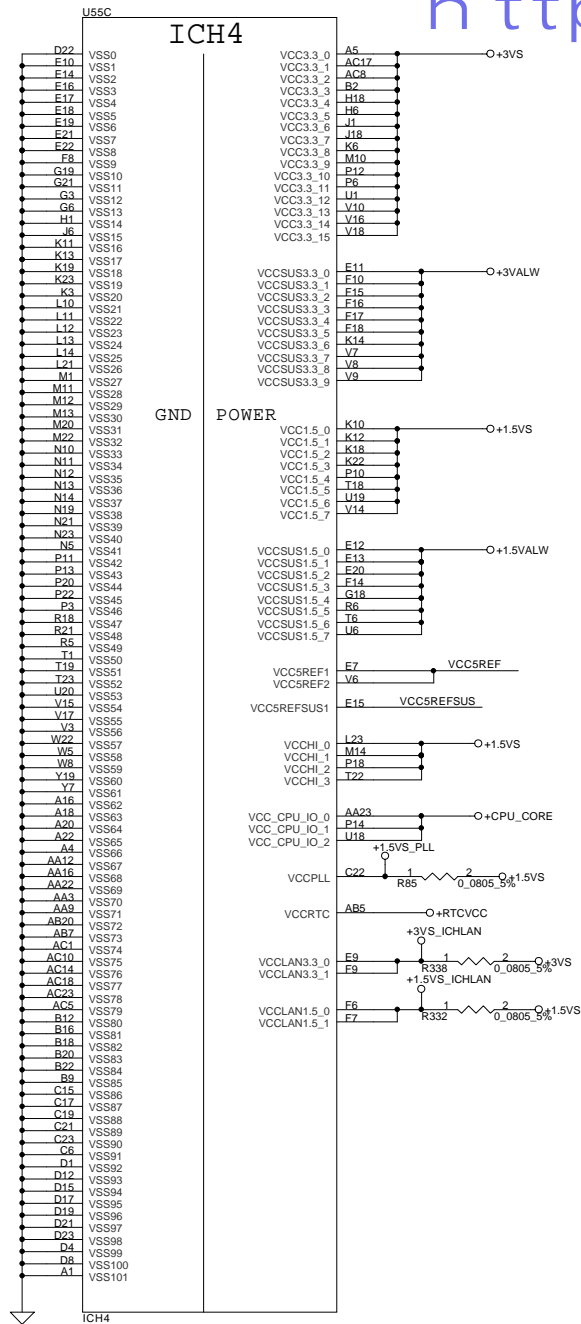
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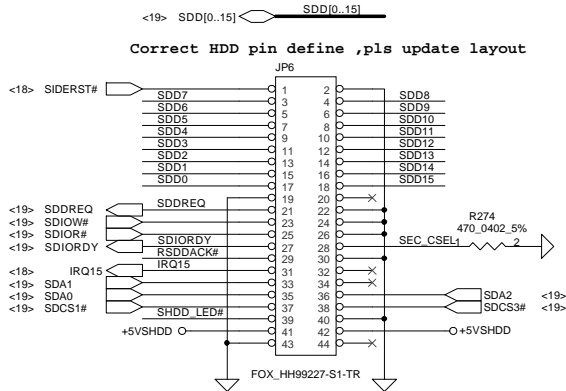
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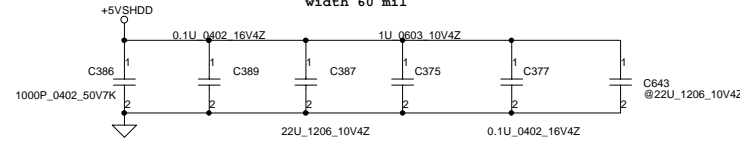
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HDD Connector



Placea caps. near HDD
CONN.

Layout Note: +5VSHDD trace
width 60 mil

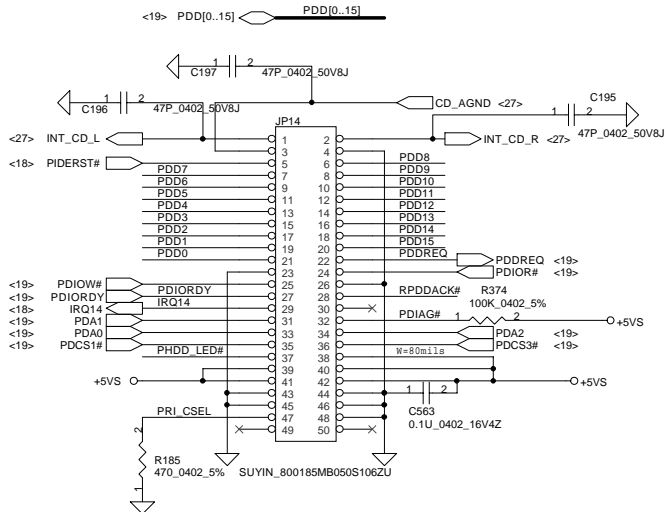


SI2301DS: P CHANNEL
VGS: -4.5V, RDS: 130 mOHM
VGS: -2.5V, RDS: 190mOHM
Id(MAX): 2.3A
VGS(MAX): +8V

1 D



CD-ROM Connector

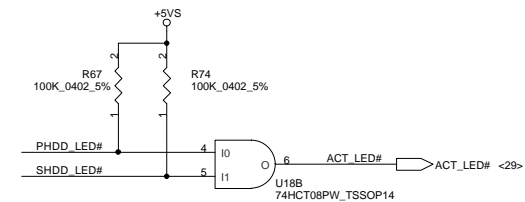
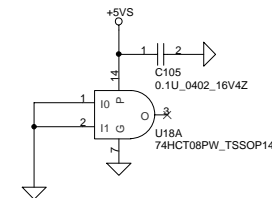
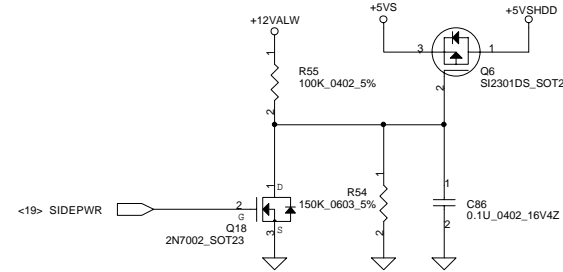
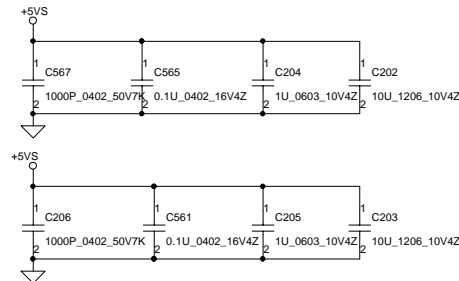


+3VS O R370 4.7K_0402_5%

<19> PDDACK# R371 22_0402_5%

PDDREQ C559 33P_0402_50V8J

Placea caps. near CDROM
CONN.



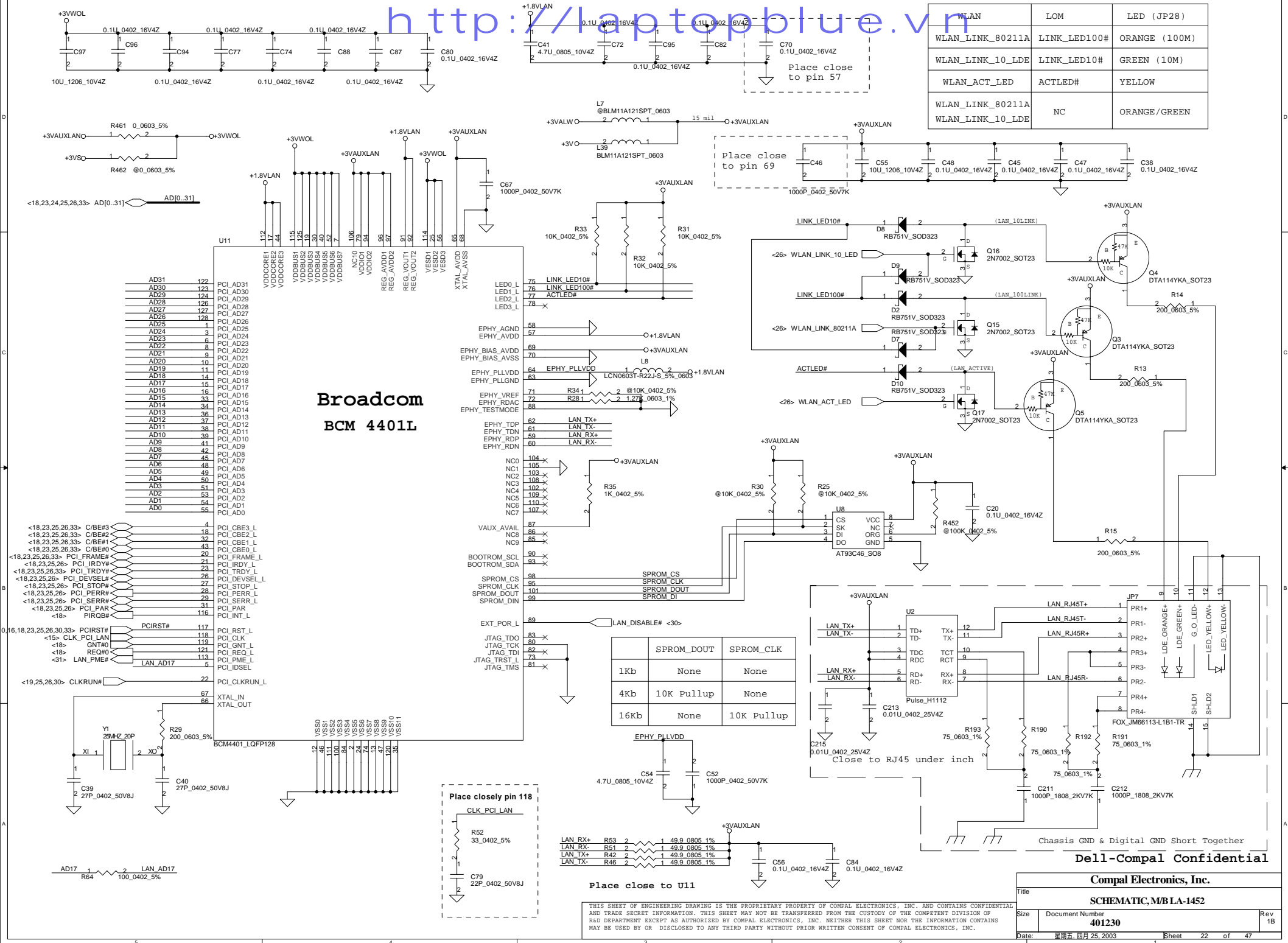
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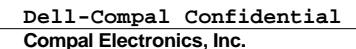
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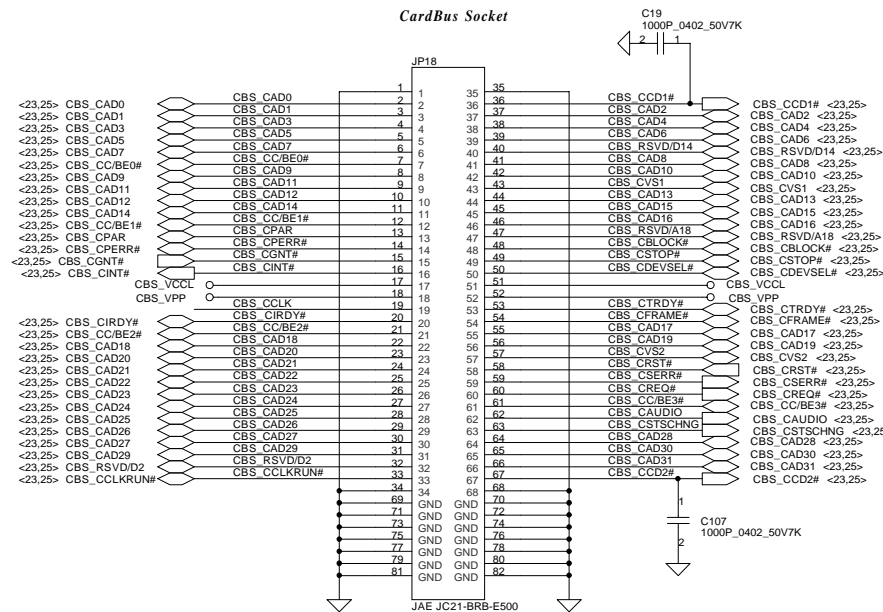
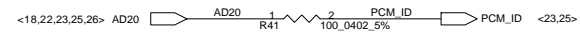
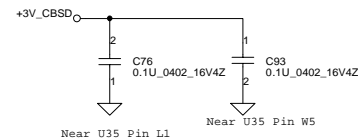
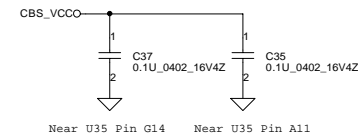
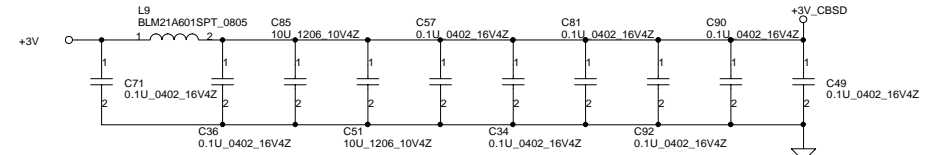
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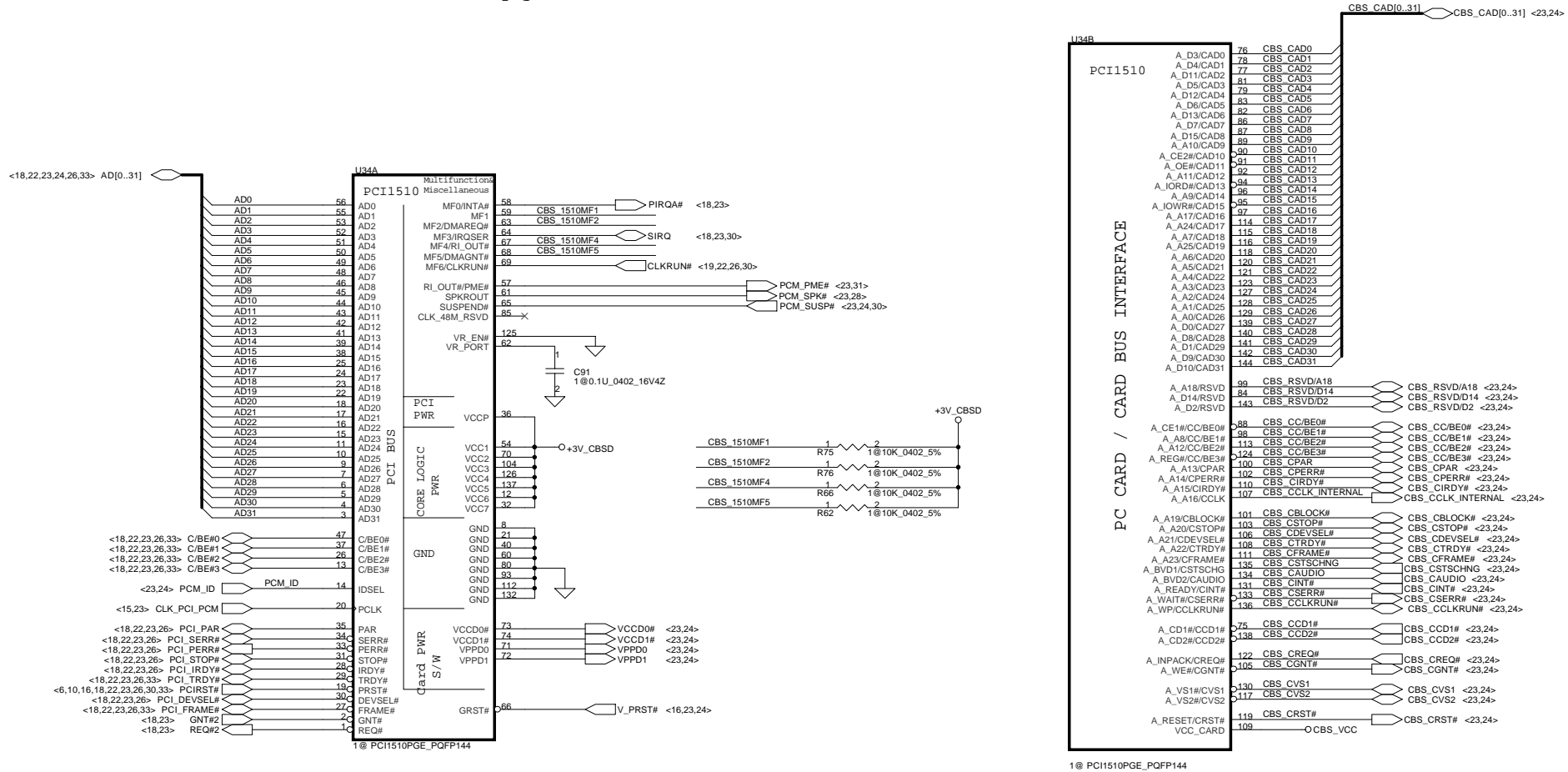




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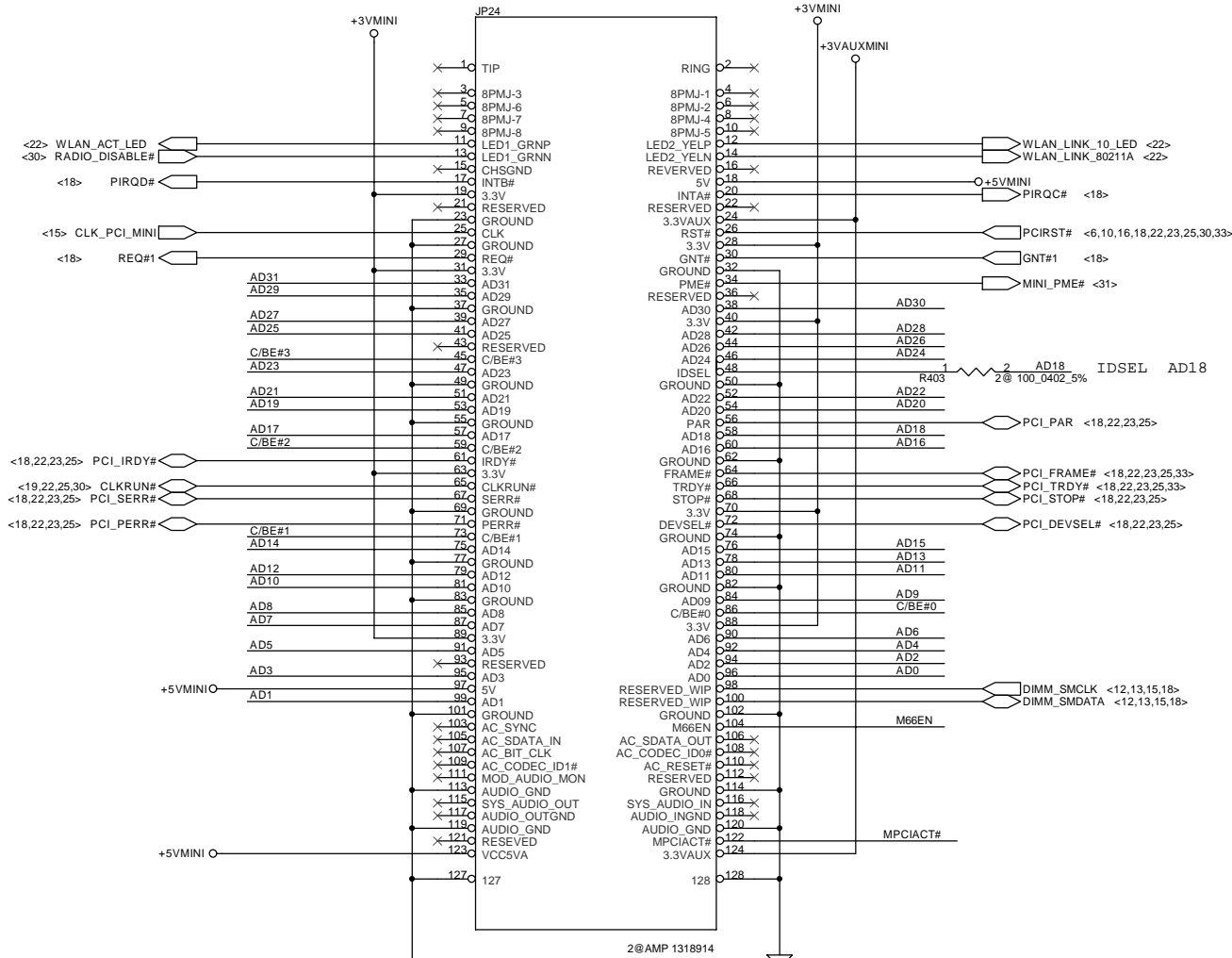
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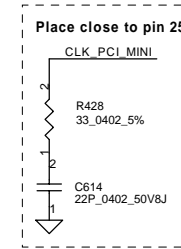
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MINI PCI TYPE III

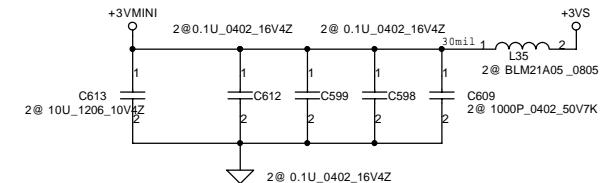
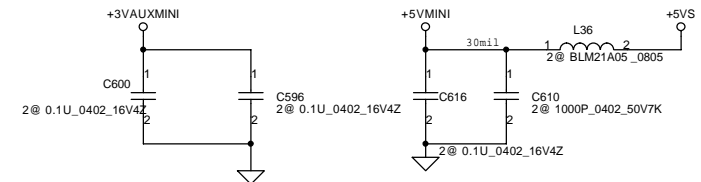
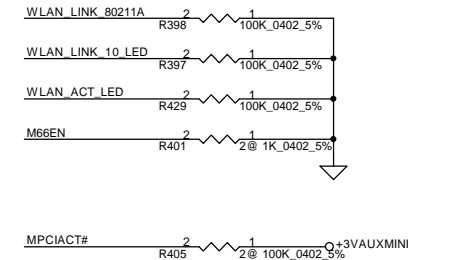
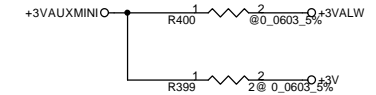


WIRELESS SUPPORT ONLY



<18,22,23,24,25,33> AD[0..31]

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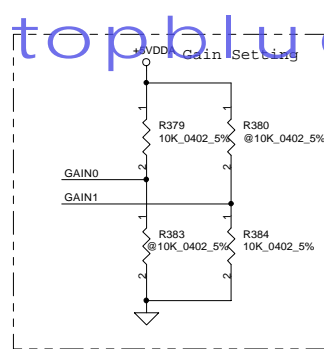
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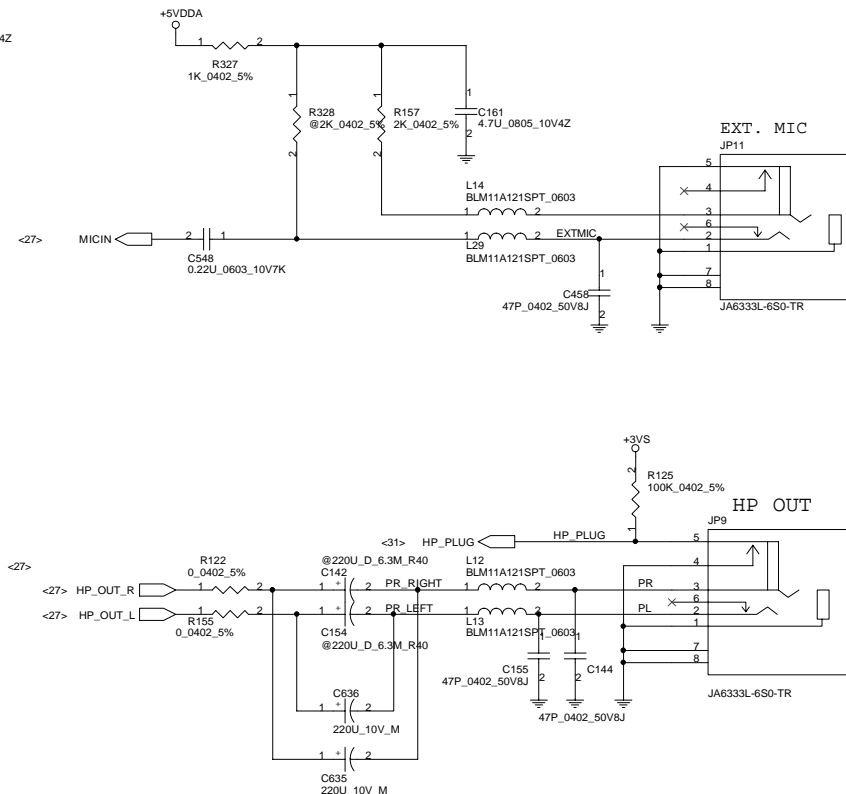
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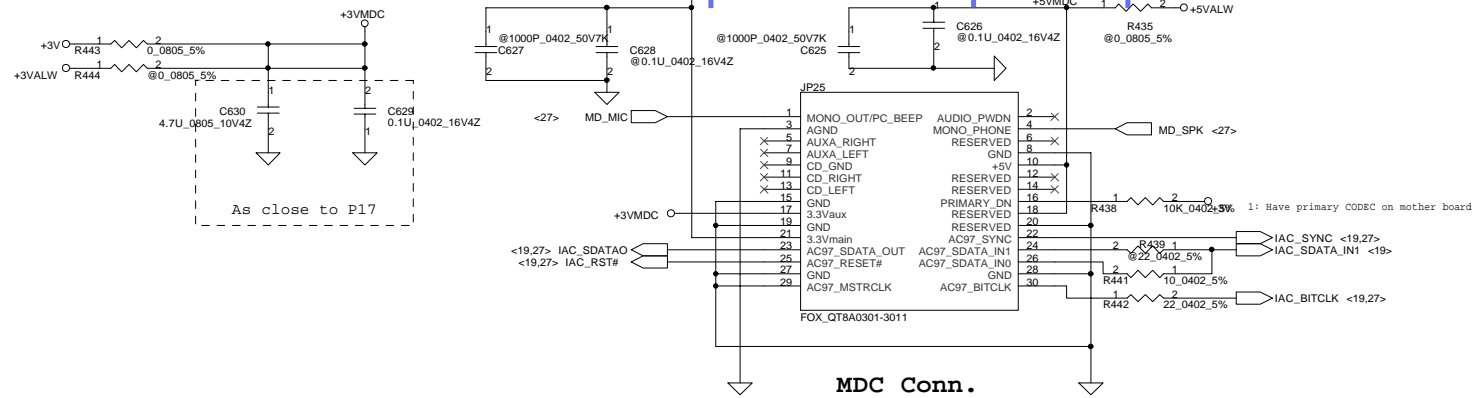




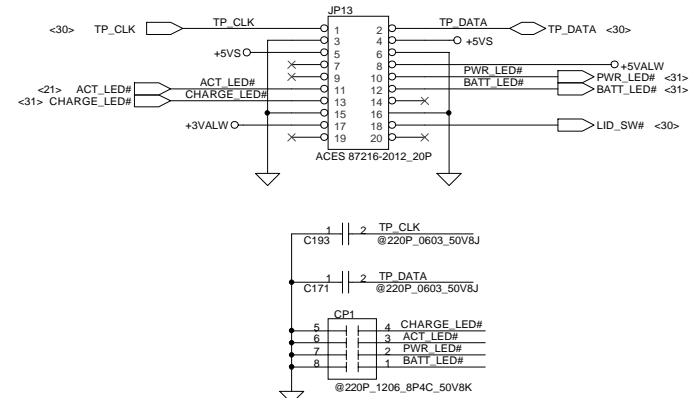
Speaker Connector



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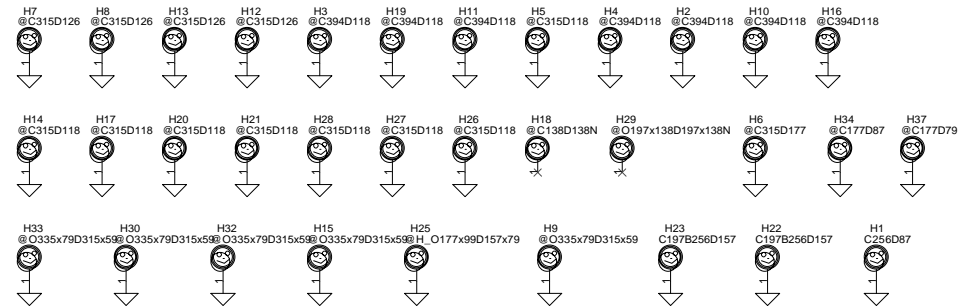
Touch Pad & Status LED Conn.



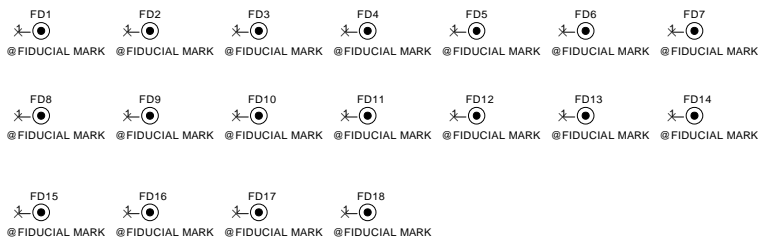
MDC Note

Pin 1 is NC for Pctel and connexant MDC modem
Pin 2 is NC for Pctel and connexant MDC modem

Screw Hole



Fiducial Mark

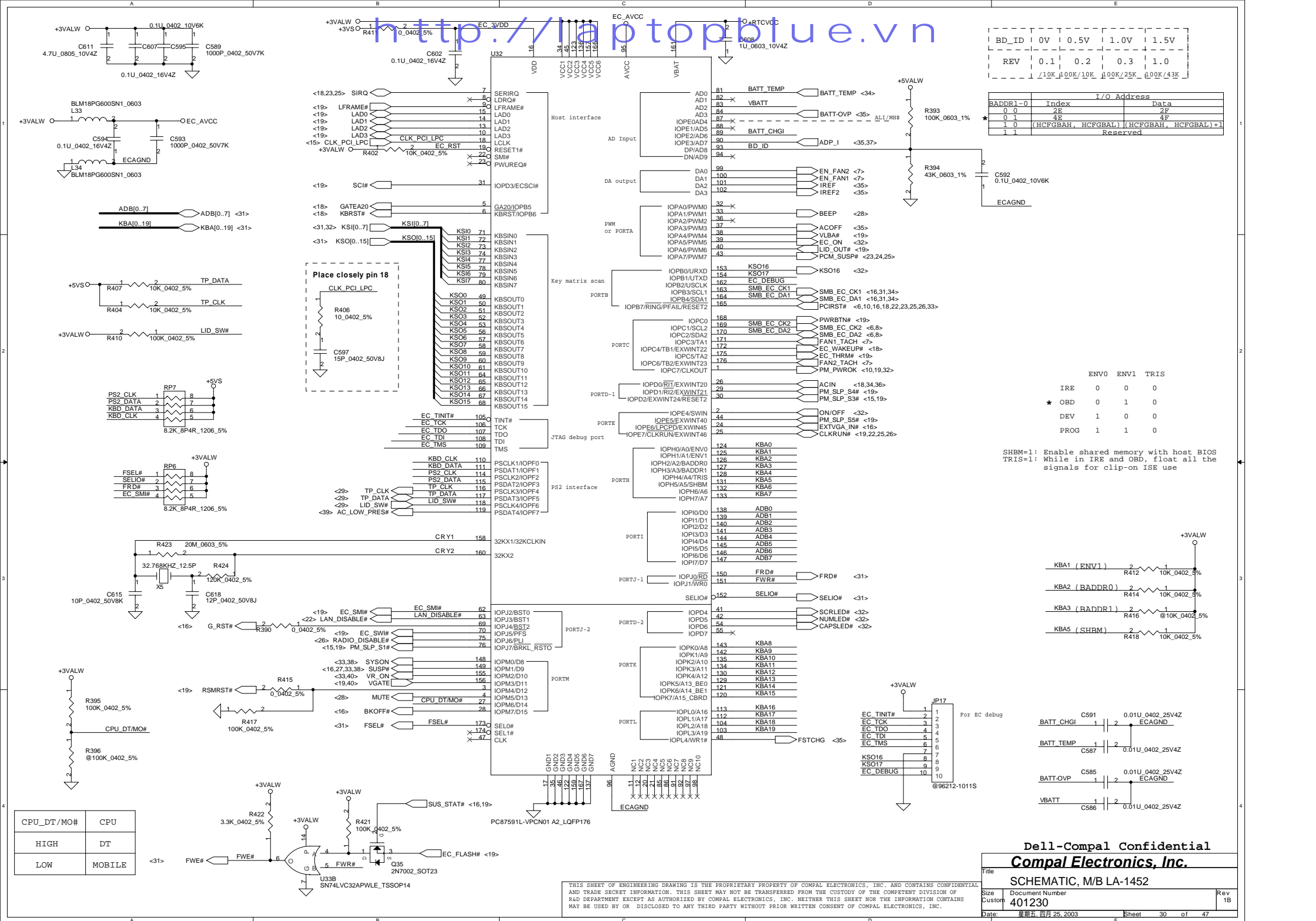


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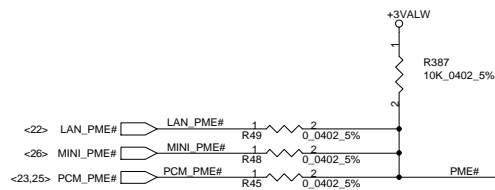
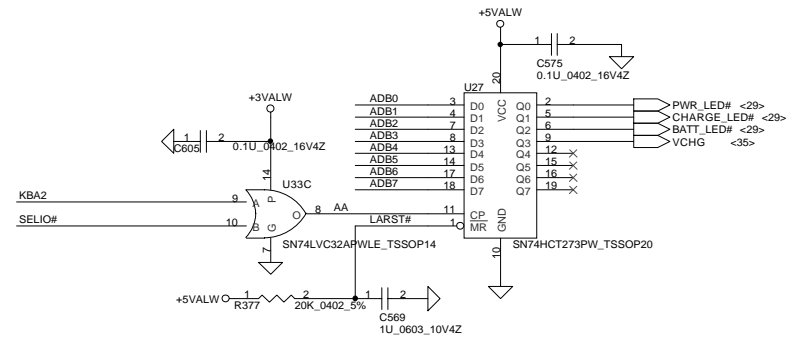
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<http://laptopblue.vn>

Output Port



SST39VF080-70_TSP40

U16

31 VCC0

30 VCC1

25 ADB0

26 ADB1

27 ADB2

28 ADB3

32 ADB4

33 ADB5

34 ADB6

35 ADB7

10 RP#

11 NC

12 READY/BUSY#

25 NC

38 NC

39 GND1

23 GND0

22 CE#

24 OE#

9 WE#

21 KBA0

20 KBA1

19 KBA2

18 KBA3

17 KBA4

16 KBA5

15 KBA6

14 KBA7

13 KBA8

12 KBA9

11 KBA10

10 KBA11

9 KBA12

8 KBA13

7 KBA14

6 KBA15

5 KBA16

4 KBA17

3 KBA18

2 KBA19

33VALW

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0.1U_0402_16V4Z

100K_0402_5%

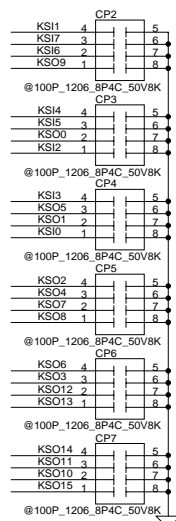
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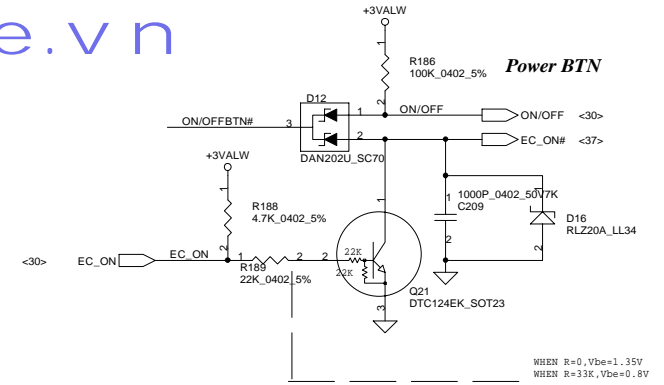
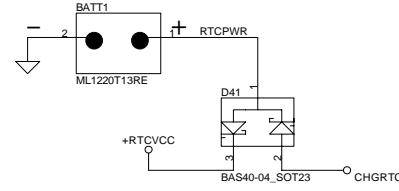
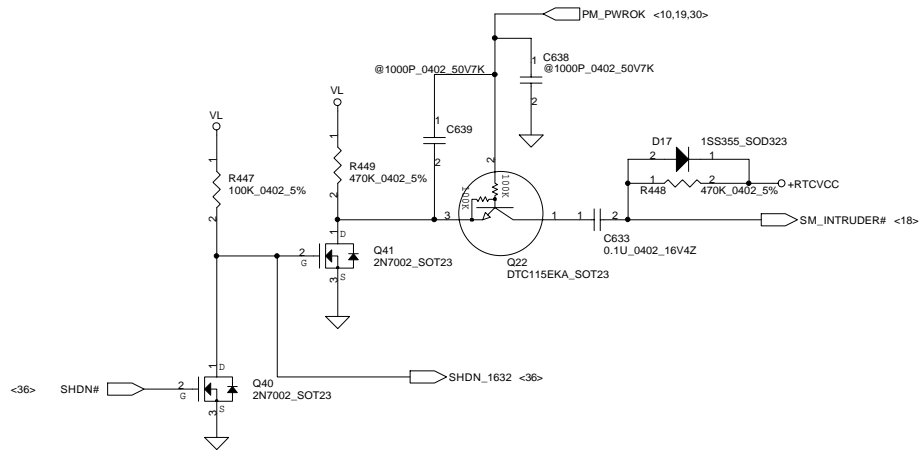
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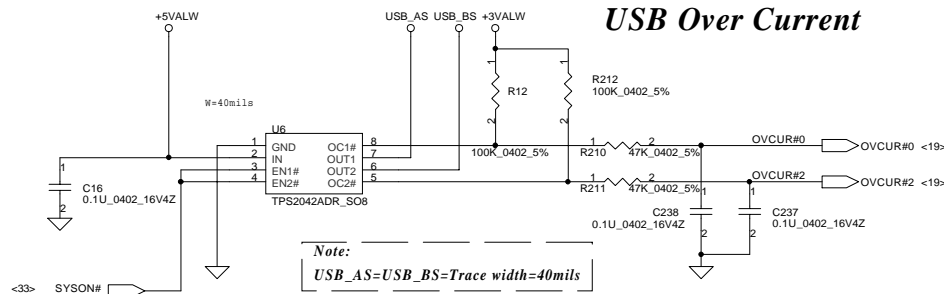
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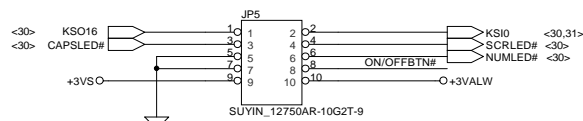
RTC Battery



USB Over Current

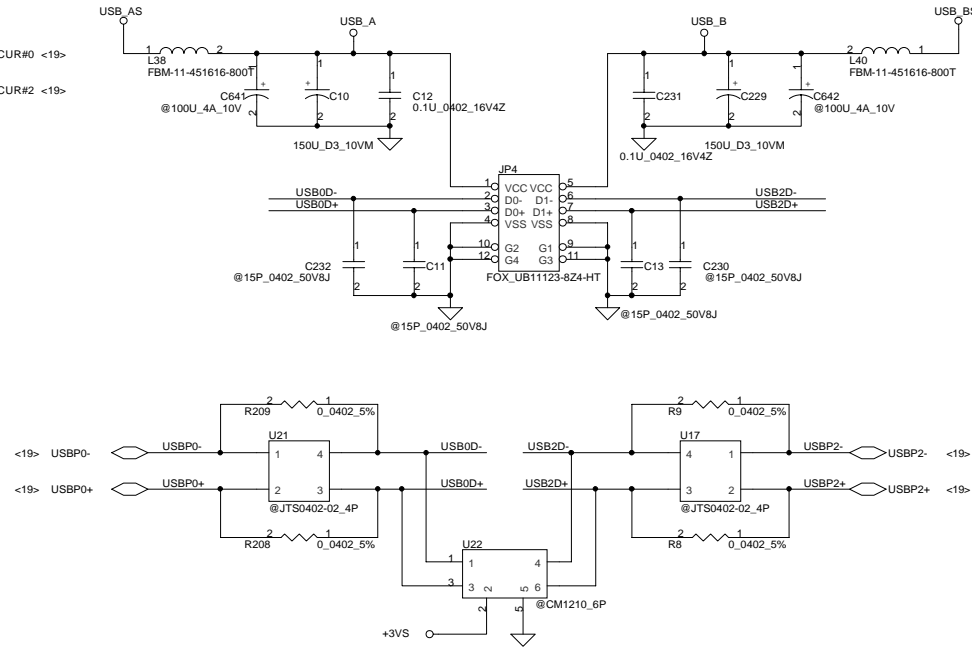


Note:
USB_AS=USB_BS=Trace width=40mils



Power SW Function Button

USB PORT



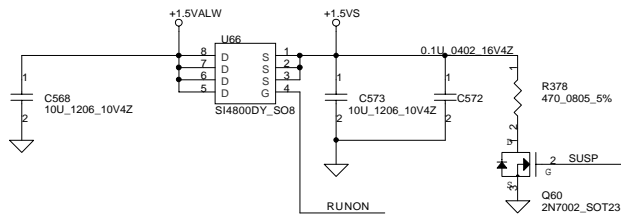
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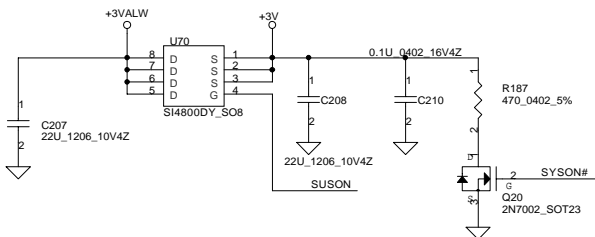
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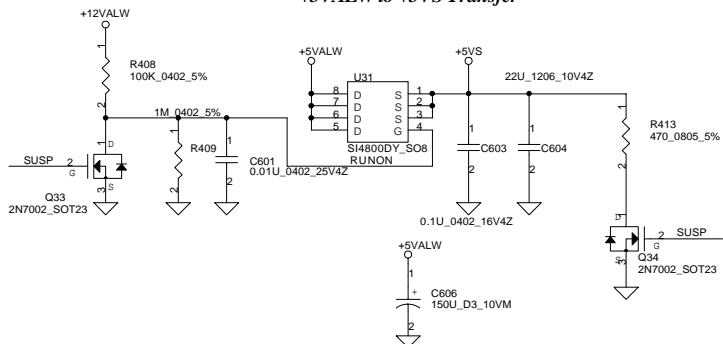
+1.5VALW to +1.5VS Transfer



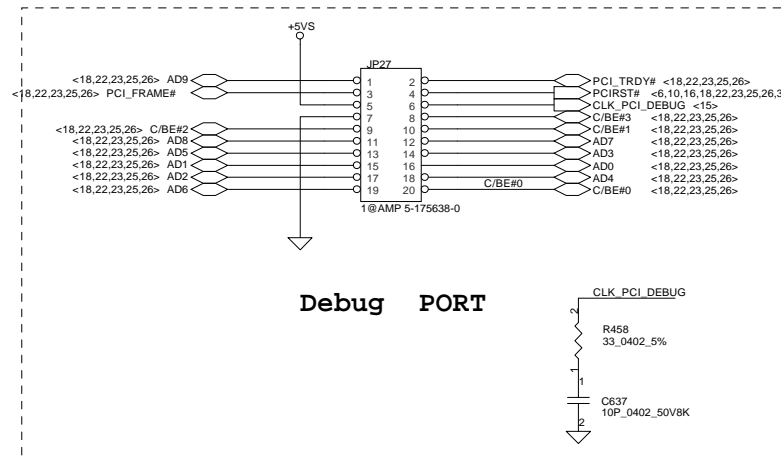
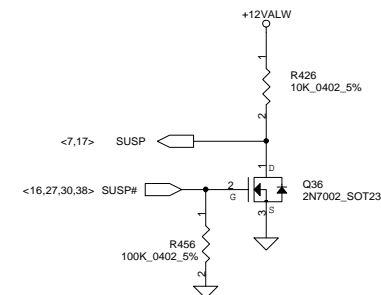
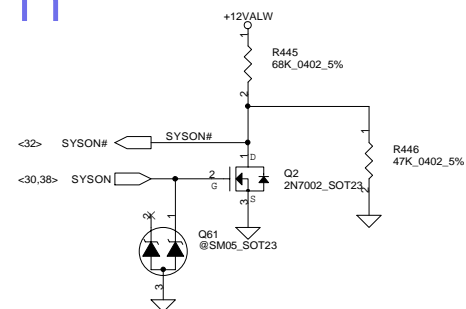
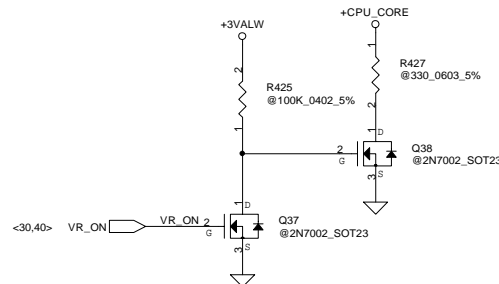
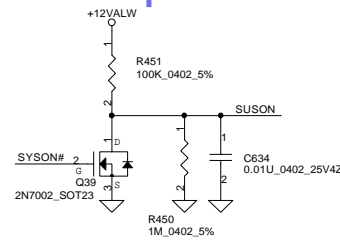
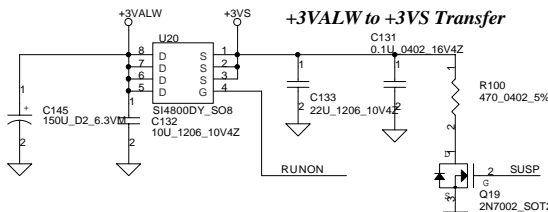
+3VALW to +3V Transfer



+5VALW to +5VS Transfer



+3VALW to +3VS Transfer



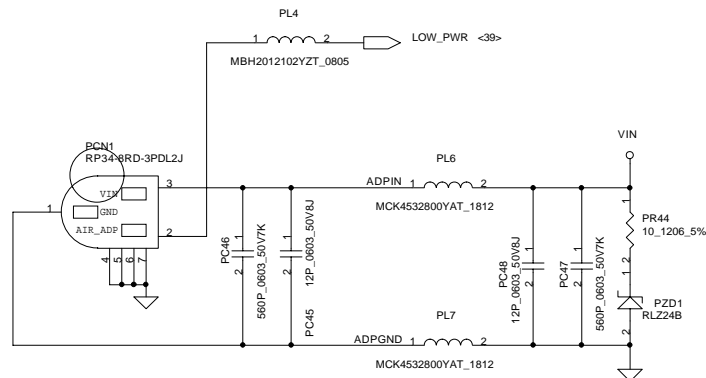
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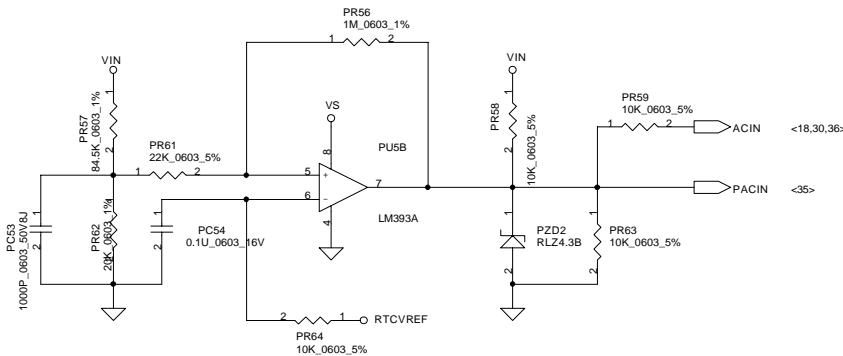


PCN2 battery connector pin assignment

SMART Battery:

- 1.BATT+
- 2.BATT+
- 3.9C/12C#/8C#
- 4.B/I
- 5.TS
- 6.SMB_EC_DA1
- 7.SMB_EC_CK1
- 8.GND
- 9.GND

Vin Detector
17.90V/17.24V



Precharge detector
15.97V/14.84V FOR
ADAPTOR

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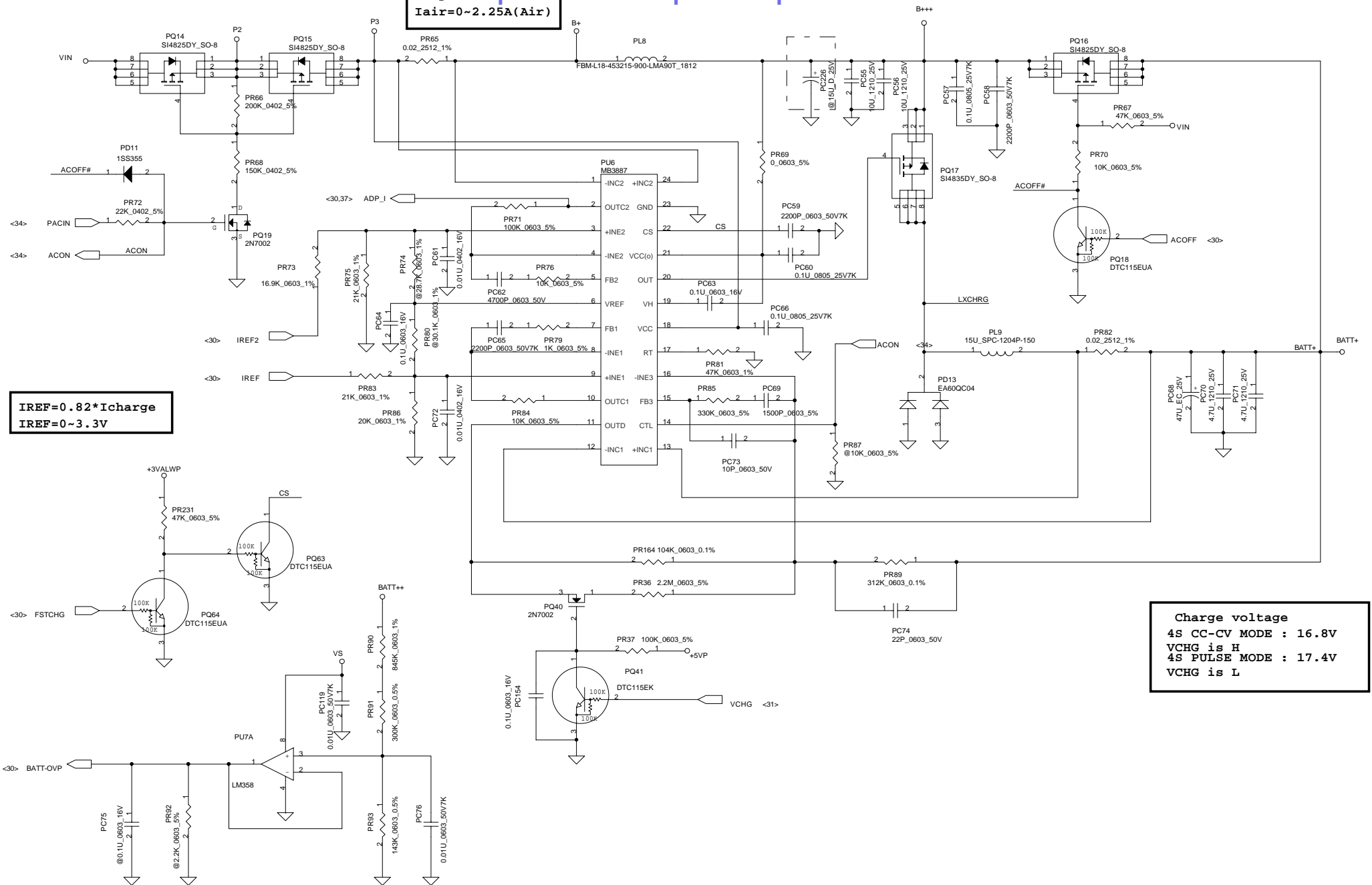
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laptopblue.vn

$I_{adp}=0\sim 4.10A(90W)$
 $I_{adp}=0\sim 3.20A(70W)$
 $I_{air}=0\sim 2.25A(Air)$



$I_{REF}=0.82 \cdot I_{charge}$
 $I_{REF}=0\sim 3.3V$

Charge voltage
 4S CC-CV MODE : 16.8V
 VCHG is H
 4S PULSE MODE : 17.4V
 VCHG is L

OVP voltage :

LI-4S :18.0V----BATT-OVP=2.00V
 LI-3S :13.5V----BATT-OVP=1.50V
 $BATT-OVP=0.2206 \cdot BATT++$

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+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

CPU thermal protection at 90 degree C
Recovery at 45 degree C

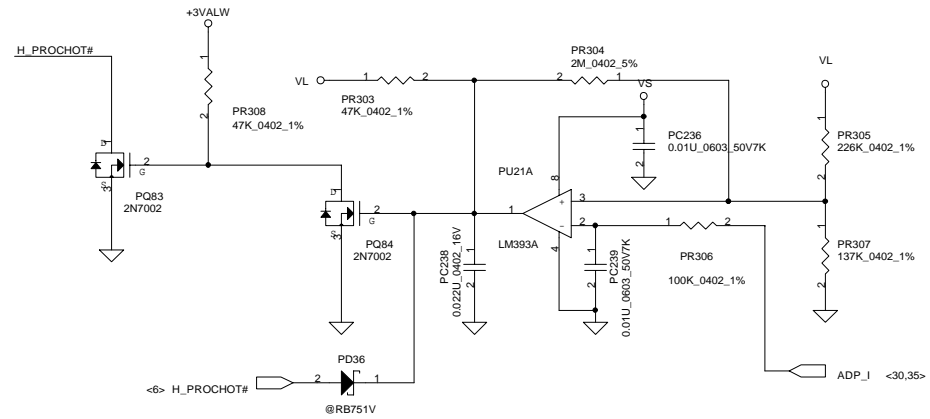
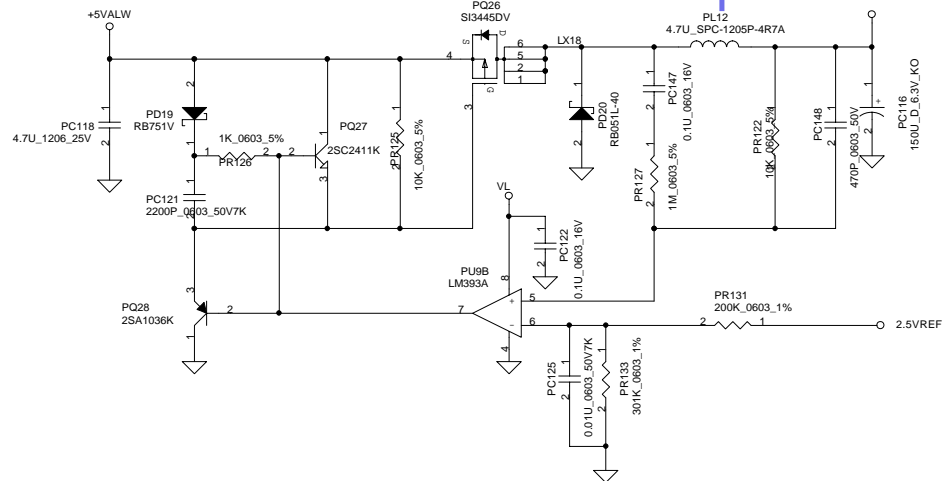
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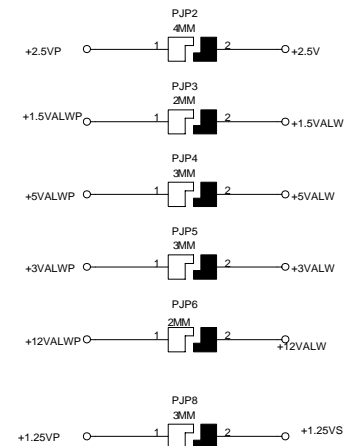
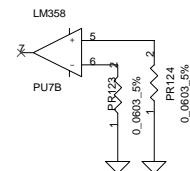
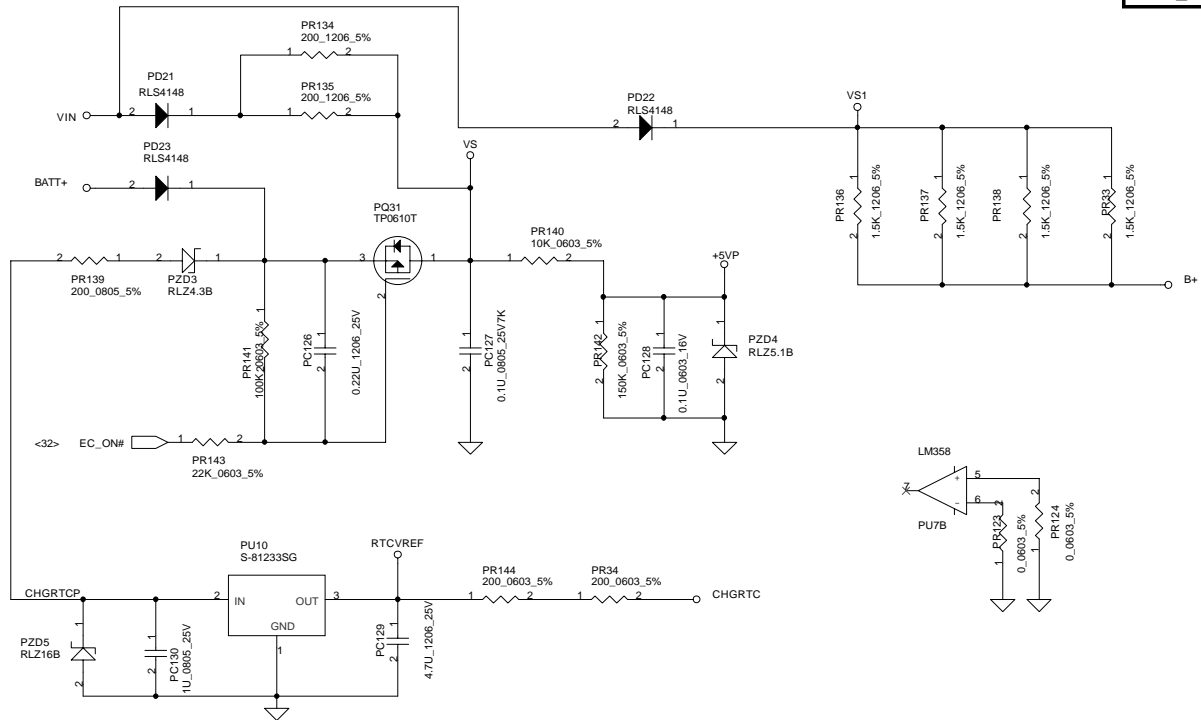
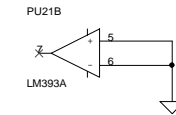
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Adaptor Current Detector
 ADP_I : 2.01V.... clock throttle(lin=5.025A)
 ADP_I : 1.81V....No clock throttle(lin=4.525A)



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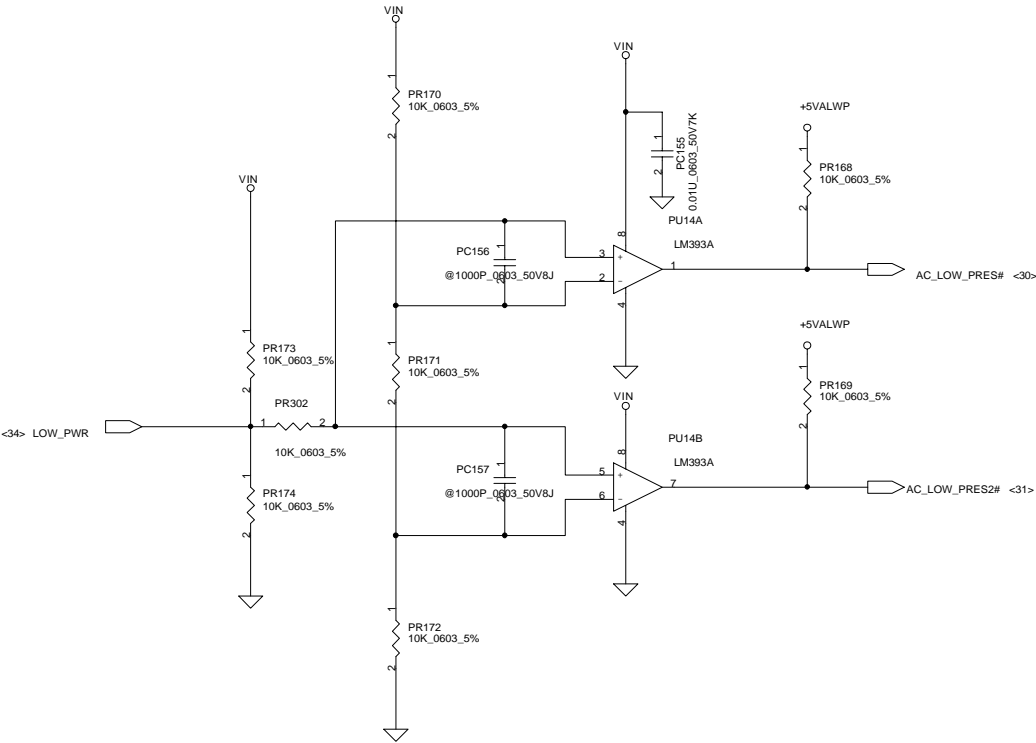
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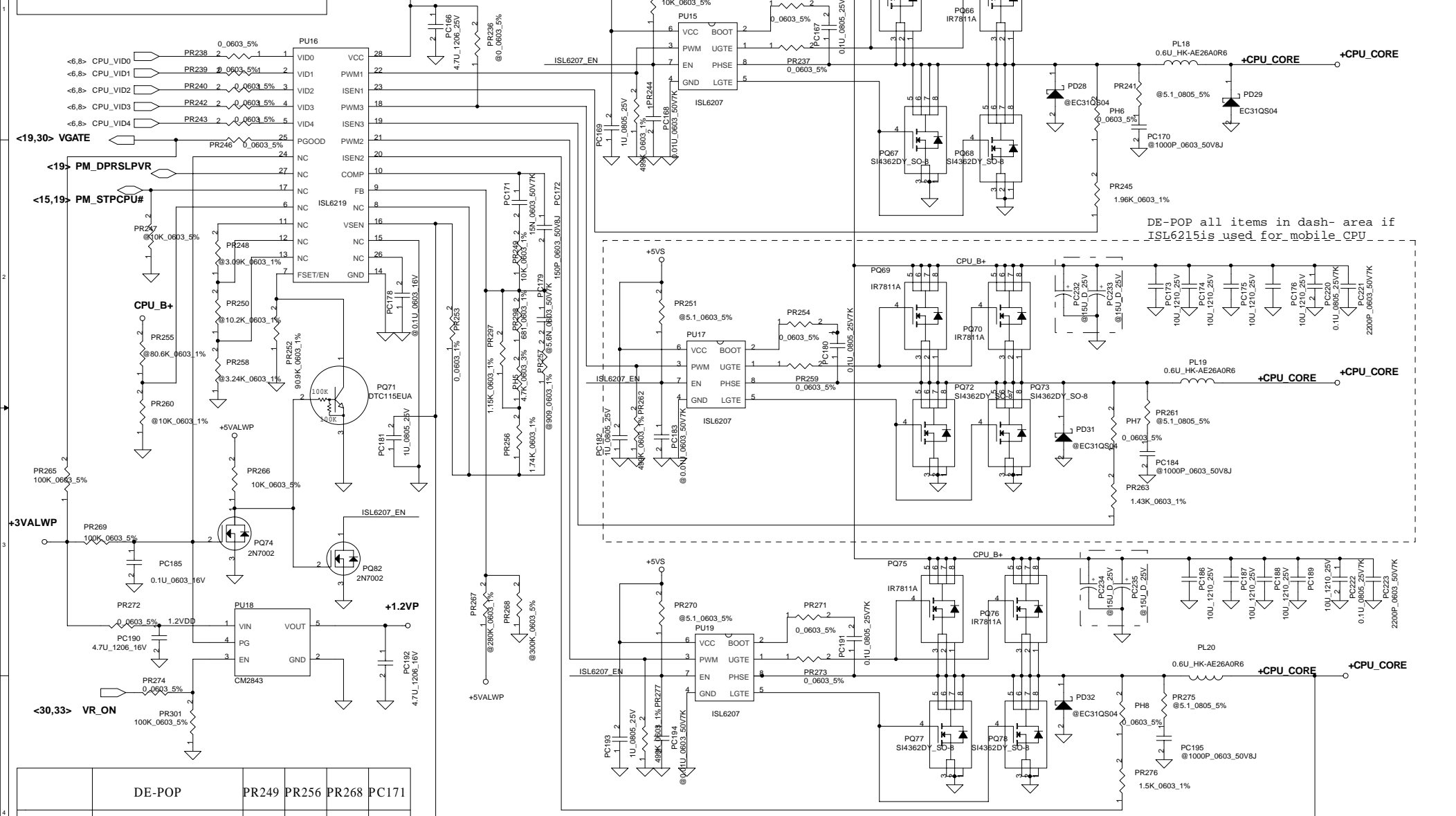
AC Adapter Detector



AC Adapter	LOW_PWR	AC_LOW_PRES#	AC_LOW_PRES2#	IREF2
90W	0V	0	0	2.96V
70W	Float	0	1	2.31V
AIRLINE	20V	1	1	1.62V

Different Pin Definition for ISL6215 in PU16

#6	RAMPS	#12	ALTV	#17	NODV
#8	VMON	#13	OFFSET	#24	EN
#11	OCSET	#15	VRTN	#27	ALTEN
#26	SOFT				



DE-POP all items in dash- area if ISL6215 is used for mobile CPU

	DE-POP	PR249	PR256	PR268	PC171
ISL6219 for desk-top	PR247, PR255, PR260 PR248, PR250, PR258, PC178, PC172, PR236	7.5K	1.74K	unpop	5.6nF
ISL6215 for mobile	PR266, PQ74, PQ71 PR253, PC179, PR257	6.04K	1.5K	130K	4.7nF

PTC solution	1. PH6, PH7, PH8 pop thermal resistor 2. Non-pop PR298 and PH5 3. PR297 0 ohm
NTC solution	1. PH6, PH7, PH8 pop 0 ohm resistor 2. Pop PR298 681_0603_18, PR297 1.15K_0603_18 3. Pop PH5 4.7K thermal resistor

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	Fireware issue	The ICH4 GNTA# strap pull up for EC BIOS	0.1A	18	Depop R153, GNTA# have internal pull up	0.1	SST
2	Leakage current issue	Reduce Broadcom 4401L leakage current	0.1A	22	Depop L39 and pop L7, connecetor power source from +3VALW to +3V, R31, R32, R33 pull up to +3VAUXLAN, Q3,Q4,Q5 pin3 connect to +3VAUXLAN	0.1	SST
3	Fix schematics part value	L21, L22, L23, L26 part value different with BOM	0.1B	15	Change L21, L22, L23, L26 part value from CHB2012U121 to BLM21A601SPT on schematics	0.1	SST
4	BOM issue	R445 include wrong part number	0.1B	33	Change R445 part number from SD028470200 to SD028680200. PN indicate value from 47K_0402_5% to 68K_0402_5%	0.1	SST
5	HDD leakage current issue	When AC in +5VSHDD will go up to 5V	0.1C	21	Q6 change to SI2302DS as schematics, SIDEPPWR active low when HDD power on	0.1	SST
6	Capture library package issue	2N7002 Drain is pin1, Source is pin3	0.1C	28	Fixed Q30, Q31, Q32 Capture libaray, pin1 fixed to pin3, pin3 fixed to pin1	0.1	SST
7	BOM issue	Fixed R196-R199 from 56.2K ohm to 56.2 ohm	0.1C	23	Change R196-R199 PN from SD014562207 to SD014562A00 on schematics	0.1	SST
8	Fix LOM EEPROM issue	U8 (AT93C46) is used X16 organization	0.1C	22	NC or pop R452 to pull up U8 pin6 for X16 organization select	0.1	SST
9	Fix CLKRUN# leakage issue	ICH4 not implement CLKRUN#, GPIO24 is resume power well.	0.1D	19	Add a diode D46 to isolate GPIO24 from ICH4 to PCI devices, and depop D46.	0.2	PT
10	LOM EEPROM issue	U8 (AT93C46) is used X16 organization. U8 pin6 pull up or NC for X16 organization select, pull down for X8 organization select.	0.1D	22	U8 pin6 pull up +3VAUXLAN via R452, and depop R452.	0.2	PT
11	SW BD LED keep turn on	SW BD LED control transistor Emitter connct to +5VALW be keep LED always turn on	0.1D	32	Change JF5 pin9 from +5VS to +3VS	0.2	PT
12	Fix VCCA_SM voltage drop issue	Add current rating for VCCA_SM, VCCA_DPLL, VCCA_FSB (1.5VS)	0.1E	10	Change L3, L4, L27, L28 from MLF2012DR68XT to FBM-L11-201209-121LMA05	0.2	PT
13	Change address and control signals layout topology	Change ddr address and control signal layout topology	0.1E	12,13	DDR address and control signals layout topology same the ddr data layout topology	0.2	PT
14	Fix EE issue item 89	Signal COMP/B and Y/G connect error	0.1E	17	Swap COMP/B and Y/G to correct connection	0.2	PT
15	Fix EE issue item 91	BEEP# from EC should be high active	0.1E	28	Change net name BEEP# to BEEF	0.2	PT
16	Fix EE issue item 92	Fix FSB 400MHz when 845GL pop	0.1E	15	Add R455 (8.2K_5%) pull down for H_BSEL0	0.2	PT
17	Fix EE issue item 95	When AC insertion SUSP# may be floating before the KBC can programit.	0.1E	33	Add R456 (100K_5%) pull down SUSP#	0.2	PT
18	Fix EE issue item 47	Provide enough current rating	0.1F	15	L22 and L26 change frome BLM21A601SPT (300mA) to FBM-L11-201209-121LMA05 (500mA) and depop L22	0.2	PT
19	Card Bus power bead current rating not enough	Provide enough current rating	0.1F	24	L5 and L6 change frome FBM-L11-160808-800LMT_0603 (300mA) to FBM-L11-201209-121LMA05 (500mA)	0.2	PT
20	Fix EE issue item 102	Fix Intel CPU FSB frequency issue	0.1F	10,15	H_SEL0 connect to R270 pin1 from CLK generator, HBSEL0 connector to R270 pin2 from CPU. Depop R270 on GL board.	0.2	PT
21	Battery charge issue	ACIN pull up +3VALW can't change power supplier to Battery when AC exit	0.1F	18	Depop R161	0.2	PT
22	NO	Change PCMCIA connector	0.1F	24	Change PCMCIA connecetor from AMP_0-1376275-1 to JAE_JC21-BRB	0.2	PT
23	Fix INTRUDER issue	ESD protect for Q22	0.1F	32	Add C638, C639 for Q22 protection	0.2	PT
24	Remove PS2 connector	No necessary	0.1G	29	Remove RF7, JF26	0.2	PT
25	Add debug port	GL board have not pop minipci connector, we need a port 80 debug tool	0.1G	33	Add R458, C637 and JF27	0.2	PT
27	For cost save	For cost save	0.1G	32	Depop C10, C229 (150U Poly Cap), add C641, C642 (100U Petit Cap)	0.2	PT
28	It no need	Use R19 pop and depop to control H_SEL0 high or low	0.1G	15	Remove R455	0.2	PT
29	Fix EE issue item 134	Change ddr address and control signal layout topology	0.1H	12,13	Change DDR address and control signal to go back SST topology	0.2	PT
30	Fix EE issue item 149	Pop Petit Cap after EA test	0.1H	32	Depop C641, C642 and pop C10, C229	0.2	PT
31	Fix EMI issue	EMI team's recommendation	0.1I	10	Pop R52, C79 for CLK_CLK_PCI_LAN; R428, C614 for CLK_PCI_MINI; R406, C597 for CLK_PCI_LPC; R321, C395 for CLK_ICH_66M	0.2	PT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
32	No	Connect MiniPci connector metal door to short to GND	0.1I	26	Add JP24 pin 127, 128 on schematics short to GND, JP24 footprint pin 127, 128 (metal lock door) be short to GND	0.2	PT
33	No	Some text mode use wire, change to line	0.1I	10,30,40	Some text mode use wire, change to line	0.2	PT
34	Fix power on issue	Use PCIRST# to set the SHDN_1632# work after PCIRST# high when power on	0.1I	6	Add Q62 gate connect to PCIRST#, source connect to SHDN_1632#	0.2	PT
35	No	Change to use approve part	0.1I	31	RP18 (8.2K +-5% 4P2R) change to R453, R454 (8.2K_0402_5%)	0.2	PT
36	No	Hard Disk source power change to +5VS	0.1I	21	Q6 change back to SI2301DS (PMOS) pin3 connect to +5VS	0.2	PT
37	Fix EE issue item 134	Change DDR address and control signal topology back to REV0.1	0.1I	12,13	Change DDR address and control signal topology back to REV0.1	0.2	PT
38	Fix EE issue item 171	For CRT Hsync and Vsync to allow tuning	0.1I	17	Add series resistors R459, R460 for Hsync and Vsync	0.2	PT
39	No	Schematic version change for PT build	0.2	ALL	Change revision from 0.1I to 0.2	0.2	PT
40	Fix issue item 20	Slow rising and falling time	0.2A	10	Pop R234, C249 for CLK_MCH_DISPLAY; R286, C333 for CLK_MCH_66M	0.2	PT
41	Fix CRT rising and falling time issue	Fast rising and falling time	0.2A	17	Pop L1, L2, L15 Change form FCM-2012C-800 to FBM-10-201209-260T for PE board	0.2	PT
42	No	Change Board ID output level	0.2A	30	Pop R393 100K_0603_1% for Board ID	0.2	PT
43	No	Add off-page reference	0.2A	24	Add off-page on pg24 FCMCIA connector	0.2	PT
44	No	Net in for Rev 0.2A Gerber	0.2B	ALL	Modify Text	0.2A	PT-2
45	Fix DFX issue	C387 effect DIMM door lock	0.2C	21	Add C643 22u_I206 replace C387's layout location and C387 leave DIMM area.	0.2A	PT-2
46	No	Add JPL8 PCMCIA connector GND pads	0.2C	24	JPL8 pin75,76,77,78,79,80,81,82 connect to GND	0.2A	PT-2
47	No	PM_GMUXSEL for mobil platform to support SpeedStep, desktop platform just GPIO fuction	0.2C	19	Remove PM_GMUXSEL signal net	0.2A	PT-2
48	Fix PIR2 issue	PIR not match schemaitcs	0.2F	22	Pop L39 and depop L7	0.2A	PT-2
49	Fix PIR19 issue	PIR not match schemaitcs	0.2F	24	L5, L6 change to FBM-L11-201209-221LMAT (3A). And Depop L5	0.2A	PT-2
50	Fix PIR23 issue	PIR not match schemaitcs	0.2F	32	Depop C638	0.2A	PT-2
51	Fix PIR24 issue	PIR not match schemaitcs	0.2F	30	RP7 pop for pull up PS2 signal	0.2A	PT-2
52	Fix PIR25 issue	PIR not match schemaitcs	0.2F	33	JP27 pop on GL board for debug and depop on PE board	0.2A	PT-2
53	Fix EE issue item 62	Schematics component's PN not match BOM	0.2G	29	JP13 (TP CONN) PN change to "SP020010910" in schematics to match BOM	0.2A	PT-2
54	Fix EE issue item 63	Schematics component's PN not match BOM	0.2G	29	JP25 (MDC CONN) PN change to "SP02F00410L" in schematics to match BOM	0.2A	PT-2
55	Fix EE issue item 64	Schematics component's PN not match BOM	0.2G	32	JP4 (USB CONN) PN change to "DC233I0241L" in schematics to match BOM	0.2A	PT-2
56	3VDDCDA, 3VDDCK rising time issue	3VDDCDA, 3VDDCK rising slow on SMBus EA measurement	0.2G	17	R5, R201 change from 10K_0402_5% to 2K_0402_5%	0.3	ST
57	EE issue list item 91	CLK_PCI_ICH timing out of spec	0.2H	18	Pop R349 (22_0402_5%), C480 (10F_0402_50V8K) for CLK_PCI_ICH AC termination	0.3	ST
58	EE issue list item 103	Depop sub thermal sensors for cost save	0.2H	8	Depop U25, U23, C394, C482, R308, R351 and R306	0.3	ST
59	Fix Boardcom 4401L wake up from S3 issue	Fix Boardcom 4401L wake up from S3 issue	0.2H	22	Add R461, R462 and depop R462. Option VESD and VDDBUS power source from +3VS to +3VAUXLAN. C97, C96, C77, C74, C88, C87, C80 bypass +3VWOL	0.3	ST
60	EE issue list item 103	H_BSEL0 of 845PE should get 1.5V at input and CLK chip should be seeing 3.3V with 533MHz CPU	0.2H	15	Add R463 (0_0402_5%) Pop on PE board. R19 move to CPU side and power source +3VS.	0.3	ST

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
61	ESD protection on 2nd FAN	ESD protection on 2nd FAN	0.2I	7	Reserve Q63 (SM05) for 2nd FAN ESD protection	0.3	ST
62	Fix EE issue item 105	H_BSEL0 circuit not correct	0.2I	10, 15	Serie resistor R270 for CPU and MCH	0.3	ST
63	No	Change Board ID for ST build	0.2I	30	R394 change from 10K_0603_1% to 24.9K_0603_1%	0.3	ST
64	No	Change for ITP test on PCBA	0.2I	6, 8	Depop R313, R305 and pop R310, R372, R183, R184, R304	0.3	ST
65	Fix EE issue item 126	Using larger cap for high-pot margin	0.2J	22	C211, C212 change package from 1206 size to 1808.	0.3	ST
66	RJ11 ISN failed	EMI team recommend to resolve RJ11 ISN test failed	0.2J	29	Cut a seperated GND for MDC and connect to system GND via a schottky diode. Reserve a jump for connect system and MDC GND.	0.3	ST
67	Fix EE issue item 140	Connect 9C/12C#/8C# to EC GPIO for future 9Cell support if required	0.2K	31, 34	Connect 9C/12C#/8C# from PR162 to U30 pin17 and remove R388	0.3	ST
68	TI TPS793475DBVR damage issue	When power on, there are 1.5A sink current when TPS793475DBVR started	0.2K	29	For power solution, C558 change package size from 0402 to 0603 for value tolerance	0.3	ST
69	Fix EE issue item 136	Add hardware circuit to sense Adapter current and automatically generate PROCHOT to the CPU to generate automatic throttling	0.2K	6	R311 change to 4.7K_0402_5%, H_PROCHOT# connect to PD36	0.3	ST
70	Fix ThermTrip function	When thermal protective resistor PH1 work, SHDN_1632# can't tie to low	0.2K	6	R320 connect to Q59 base, R316 connect to Q59 collector and VL power source. Add Q64 between Q59 and Q62. Q62 change pin1 Drain to connect SHDN_1632#	0.3	ST
71	RJ11 ISN failed	Change solution for ISN failed	0.3	29	Remove PJP9-13 and D47	0.3	ST
72	Fix EE issue item 136	Follow Intel desing guide recommend pull up resistor value	0.3	6	R311 change back to 62_0402_5%	0.3	ST
73	Fix EE issue item 141	Prevent noise issue	0.3	28	Depop R328 for noise prevention	0.3	ST
74	No	For cost save	0.3	7	Depop C148, C150 (470U_D4_2.5VM) and C152 (330U_D2E_2.5VM)	0.3	ST
75	Fix PROTO3 EE issue item 44	Minipci connector pop for PE board only	0.3B	26	Add 2@ symbol for JP24 for PE board pop only	0.3	ST
76	No	Vendor schematics review recommendation	0.3B	22	R35 change from 10K_0402_5% to 1K_0402_5%	0.3	ST
77	Fix PROTO3 EE issue item 45	Remove minipci suport component for GL board cost save	0.3B	26	Remove R405, R399, C600, C596, C613, C612, C599, C598, C609, L35, C616, C610, L36, R401, R403 on GL board	0.3	ST
78	No	Modify material value	0.3C	23, 26, 27, 28	Change value L11, L30, L31, L35, L36 from BDM21A05_0805 to BLM21A05_0805	0.3	ST
79	No	Modify material part number	0.3C	27	U24 STAC9750 change from (SA097500000) to (SA097500010) for both BOM	0.3	ST
80	No	Depop Fan2 Control circuit	0.3C	7	Delete R11, D11, D20, U1, R10, R6, Q1, C234, Q8, JP19	0.3	ST
79	No	EMI require	1.0	17	Pop D1, D3, D18 for EMI requirement	1.0	QT
80	No	Modify Fiduiial Mark & Screw Hole value for non pop	1.0	29	Fiduiial Mark & Screw Hole value add @ symbol	1.0	QT
81	No	BD_ID change for QT build	1A	30	R394 change from 24.9K_0603_1% to 43K_0603_1%	1.0	QT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
82	INTRUDER# issue	Sometimes when normal shutdown, INTRUDER# record a event	1A	32	Q22 change from 2N7002 to BJT DTC115EKA	1.0	QT
83	No	Because Q22 change to DTC115EKA, C639 is no necessary	1B	32	Depop C639 (1000P_0402_50V7K)	1.0	QT
84	Fix Qual issue item 35	Improve IAC_SDATA_IN1 singnal quaility	1B	29	The serie resistor R441 change from 22_0402_5% to 10_0402_5%	1.0	Pilot
85	Fix audio not switching to headphones or ext speakers immediately	For audio switching to headphones or ext speakers immediately	1C	28	Depop C580 and change C588 from 4.7uf to 0.47uf	1.0	RTS

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	CPU_CORE can't power up	Pin7 of PU16 can't be used as on/off control pin	0.1B	40	1. Change VCC power source of PU16 from +5VALWP to +5VS	0.1	SST
2	current limited is not up to 60A	Current limited is about 37A while PH6,PH7,PH8 is 1.5K that is not enough for design target.Because we don't use PTC resistor on PCB now, the value must be tuned later.	0.1B	40	1. Change PH6,PH7,PH8 from 1.5K_0603_5% to 3K_0603_1%	0.1	SST
3	Turn on voltage of PQ19 is not enough	Vgs of PQ19 is 2V while PR72 is 47K. That is not enough. While PR72 is 22K, the Vgs can be improved to 2.5V.	0.1B	35	1. Change PR72 from 47K_0402_5% to 22K_0402_5%	0.1	SST
4	current rating is not enough.	FBM-L11-322513-151LMAT is 5A that is not enough.So FBM-L18-453215-900LMA90T1812 is 9A that is better.	0.1B	35	1. Change PL8 from FBM-L11-322513-151LMAT to FBM-L18-453215-900LMA90T1812.	0.2	PT
5	Fix noise issue	On SST PCB, we can sound some noise due to PC77, the cernamic capacitor has sounded noise with thinner type.	0.1C	36	1. Change PC77 from 2.2U_1206_25V to 4.7U_1210_25V	0.2	PT
6	Fix CPU_CORE Transient Response fail	The transient response is too slow. We must to tune feedback resistor and capacitor to fix it.	0.1E	40	1. Change PR249 from 3.48K_0603_1% to 5.76K_0603_1%. 2. Change PR257 from 49.9_0603_1% to 1.1K_0603_1% 3. Populate PC172 68PF_0603_50V.	0.2	PT
7	SDREF output voltage is over spec.	Add bypass capacitor pallel pin18 of ISL6225	0.1E	38	Populate PC218 470P_0603_50V7K	0.2	PT
8	PG of CM28423 has a glitch while VCC is ready and VR_ON is float	Add pulldown resistor tie to GND while VR_ON is float that can be made sure the logic is low.	0.1E	40	Add PR301 100K_0603_1%	0.2	PT
9	Change VCC power source of PU15, PU17, PU19 from +5VALWP to +5VS	Negative voltage was observed on +5VALWP when system powered off	0.1E	40	1. Change VCC power source of PU15, PU17, PU19 from +5VALWP to +5VS	0.2	PT
10	Prevent abnormal function OVP caused by ISL6219 while system powerwd off ; bouble pulses was observed at output PW1, PW2, PWM3 of ISL6219	ISL6219 caused OVP when on/off pin changed from high to low level	0.1E	40	1. Add FQ82 2N7002 2. Change PR232 from 5.1_0603_5% to 10K_0603_5% 3. Change PC168 from 1U_0805_25V to 0.01U_0603_50V. 4. Depop PR251, PR270, PC183, PC194 5. Tie the EN pin of PU15, PU17, PU19 to Pin1 of PQ82	0.2	PT
11	Fine-tune current sharing of CPU VR phasel,2,3 to have thermal balance	uneven current sharing found	0.1E	40	1. Change PH6, PH7, PH8 form 3K_0603_1% to 0_0603_5% 2. Change PR245 from 0_0603_5% to 1.96K_0603_1% 3. Change PR263 from 0_0603_5% to 1.43K_0603_1%. 4. Change PR276 from 0_0603_5% to 1.5K_0603_1%	0.2	PT
12	Fine-tune CPU load-line with NTC	Fine-tune CPU load-line with NTC	0.1E	40	1. Keep PR268 nonpop 2. Change PR256 from 2K_0603_1% to 1.74K_0603_1% 3. Change PR297 from 0_0603_5% to 1.15K_0603_1%. 4. Change PH5from depop to 4.7K_0603_1% 5. Change PR298 from depop to 681_0603_1% 6. Change PR257 from 49.9_0603_1% to 909_0603_1% 7. Change PC179 from 3900P_0603_50V to 5.6N_0603_50V 8. Change PR249 from 3.48K_0603_5% to 7.5K_0603_1% 7. Change PC171 from 6800P_0603_50V to 5.6N_0603_50V 8. Change PC172 from depop to 47P_0603_50V	0.2	PT
13	Audio noise found	Still find root cause	0.1E	35, 36, 38, 40	1. reserve 15U_D_25V capacitors on PC226-PC235,	0.2	PT
14	PC212 location space change	requested by ME to put a connector around	0.1E	38	1. change the size of PC212 from D size to 0805 and pop 4.7U_0805_10V	0.2	PT
15	Remove PD5	no possibilty to have a reverse voltage at Vin when adapter plug-in because of the DC-jack orientation structure	0.2C	34	1.delete PD5 from schematics	0.2A	PT-2
16	Prevent PU14 from burn out	When pin1 (GND pin) of DC-jack PCN1 disconnected from B/M (damaged by force from outside), there is a large current going through PU14 resulted in PU14 damaged	0.2C	39	Add PR302 10K_0603_5%	0.2A	PT-2

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
17	100MHz EMI broad-band over spec.	Improve 100MHz EMI broad-band	0.2E	34	Add a FBM-L18-453215-900-LMA90T_1812 bead on PL7	0.2A	PT-2
18	100MHz EMI broad-band over spec.	Improve 100MHz EMI broad-band	0.2H	34	1. Change PL6,PL7 from FBM-L18-453215-900-LMA90T_1812 to MCK4532800YAT_1812 2. Add PL4 MBH2012102YZT_0805 3. Change PC45 from 100P to 560P, PC46 from 1000P to 12P,PC47 from 100P to 12P and PC48 from 1000P to 560P	0.3	ST
19	Precharge function has some bug, while AC Adapter plug in first time	Precharge can reduce surge current from AC adapter,while Adapter plugged in	0.2H	34	1. Change PR51 from 1M to 2.2M,PR55 from 215K to 191K. 2. Change PR54 from 10K to 34K,add PR32 66.5K. 3. Change PC51 from 0.1U_16V to 1000P_50V. 4. Change PC50 from 1000P_50V to 0.1U_16V. 5. Change net +5VP and RTCVREF to VL. 6. Change PR113 from 47K_0402_5% to 0.0402_5%. 7. De-pop PC111 and change PC158 from 0.1U_16V to 0.47U_16V.	0.3	ST
20	Power rating of 0.02_2010 is not enough.	rating power of 0.02_2010 is 0.5W that is very poor for 90W adpater	0.2H	35	1. Change PR65 from 0.02_2010_1% to 0.02_2512_1%.	0.3	ST
21	Power open issue	Change size of thermal resistor and cost down	0.2H	36	Change PH1 from 10K_0805_1% to 10K_0603_1%.	0.3	ST
22	Power good giltch issue in ISL6225	The giltch occurs while secondary PWM is enabled that effects system boots up	0.2H	38	1. Add PR31 1K_0402_5%.. 2. De-pop PR294	0.3	ST
23	Fix open issue #137	DELL don't approve item22 solution, prefer using new version ISL6225	0.2J	38	1. De-pop PR31 1K_0402_5%. 2. De-pop PR294 0_0402_5%. 3. Add PR30 0_0402_5%.	0.3	ST
24	Fix open issue #124	Fix open issue #124 and using ISL6219A	0.2J	40	1. Change PR232 from 10K_0603_5% to 5.1_0603_5%. 2. Populate PR251 and PR270 5.1_0603_5%. 3. Populate PC183 and PC194 0.01U_0603_50V. 4. De-pop PQ82,PD31,PD,32	0.3	ST
25	Fix ISN fail issue	Fix ISN fail with 200KHz	0.2J	35	1. Change PR81 from 66.5K_0603_1% to 47K_0603_1% 2. Change PC55 and PC56 from 4.7U_1210_25V to 10U_1210_25V 3. Change PL9 from 15UH to 22UH	0.3	ST
26	Fix open issue #123	Rds(on) of SI4835DY is too high,change PQ14,15,16 to SI4825DY for power stress	0.2J	35	Change PQ14,PQ15,and PQ16 from SI4835DY to SI4825DY	0.3	ST
27	Adapter shut down while running P4MaxPower 100%	Adapter current over 5.5A 4 sec while running P4MaxPower 100%	0.3	37	1. add PR303, PR306 47K_0402_1%. 2. add PR304 1M_0402_1%. 3. add PR305 226K_0402_1% 4. add PR307 147K_0402_1% 5. add PR308 100K_0402_1% 6. add PC236 0.01U_0603_50V 7. add PC239 0.1U_0603_16V 8. add PC238 1000P_0402_50V 9. add PQ83, PQ84 2N7002 10. add PU21 LM393A	0.3	ST
28	Modify thermal protect temp. from 95C to 87C	Based on thermal team requirement	0.3A	36	1. ChangePR119 from 21K_0603_1% to 17.8K_0603_1% 2. Change PR117 from 1.74K_0603_1% to 2.05K_0603_1%	0.3	ST

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
29	modify compension for reduce output capacitor	modify compension for reduce output capacitor	0.3A	40	1. De-pop PR257 and PC179. 2. Change PC171 from 5.6N_0603_50V to 15N_0603_50V 3. Change PC172 form 47P_0603_50V to 150P_0603_50V 4. Change PR249 from 7.5K_0603_1% to 10K_0603_1%	0.3	ST
30	Fix item25 about ISN test without changing inductor	Fix item25 about ISN test without changing inductor	0.3A	35	1. Change PL9 from 22UH_SPC-1205P-220A to 15UH_SPC-1204P-150	0.3	ST
31	Capacitor DFX issues	Component layout pad overlap (reservated for noise issue) causes some components shifting when pass the re-flow	0.3D	35 36 38 40	remove PC226, PC227, PC228, PC229, PC230, PC231, PC232, PC233, PC234, PC235	1.0	QT
32	Noise issue in B+ power	Add reservated caps. back for noise issue	0.3E	35 36 38 40	reserve PC226, PC227, PC228, PC229, PC230, PC231, PC232, PC233, PC234, PC235	1.0	QT
33	Change OTP from 87C to 90C	Change OTP from 87C to 90C	1.0B	36	1. Change PR117 from 2.05K_0603_1% to 1.96K_0603_1% 2. Change PR119 from 17.8K_0603_1% to 19.1K_0603_1%	1.0	QT
34	Fine tune adaptor detector	Fine tune adaptor detector	1.0B	37	1. Change PC238 from 1000P_0603_50V% to 0.022U_0402_16V 2. Change PC239 from 0.1U_0603_16V to 0.01U_0603_50V 3. Change PR304 from 1M_0402_1% to 2M_0402_5% 4. Change PR307 from 147K_0402_1% to 137K_0402_1%	1.0	QT
35	Use new version ISL6225	Use new version ISL6225	1.0B	38	1. Change PU20 from ISL6225CA to ISL6225BCA	1.0	QT
36	Fix surge voltage in +CPU_CORE while power up	Fix surge voltage in +CPU_CORE while power up	1.0B	40	1. Add PR244,PR262,PR277 499K_0603_1% 2. No populate PR251,PR270,PC183 and PC194. 3. Change PR232 from 5.1_0603_5% to 10K_0603_5%. 4. Add PQ82 2N7002	1.0	QT

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