

MODEL NAME : *KML50*

PCB NO : *LA-4596P (DA60000B710)*

BOM P/N : *11*

Half Penny Bridge 15.4

Compal Confidential

Schematic Document

Cantiga + ICH9

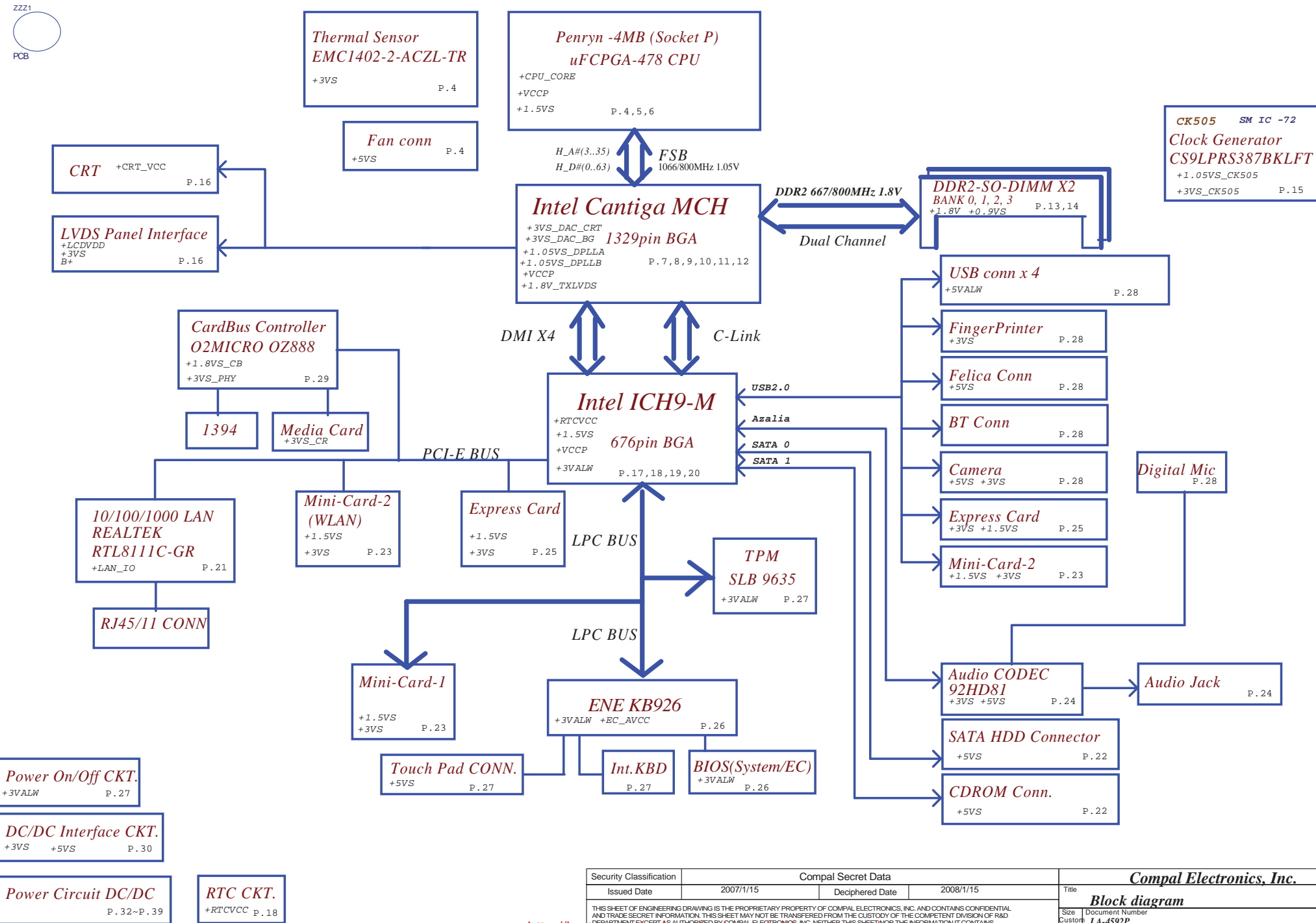
2009 / 01 / 14 Rev:1.0(A00)

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File Name : LA-4596P

Half Penny Bridge 15.4



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power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

ICH9-M	USB PORT#	DESTINATION
	0	JUSBP1
	1	CAMERA
	2	JUSBP3 Top
	3	Felica
	4	Blue Tooth
	5	Finger Printer
	6	JMINI2-WLAN
	7	Express card
	8	JUSBP3 Bottom
	9	JMINI1-WWAN
	10	JUSBP4
	11	NA

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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Symbol Note :



: means Digital Ground



: means Analog Ground

@ : means just reserve , no build

CONN@ : means ME CONN compont.

TPM@:TPM compont

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	GLAN RTL8111DL
Lane 3	MINI CARD-2 WLAN
Lane 4	EXPRESS CARD
Lane 5	CARD READER OZ888
Lane 6	NA

SATA	DESTINATION
Lane 0	HDD
Lane 1	ODD
Lane 4	NA
Lane 5	NA

SMBUS Control Table

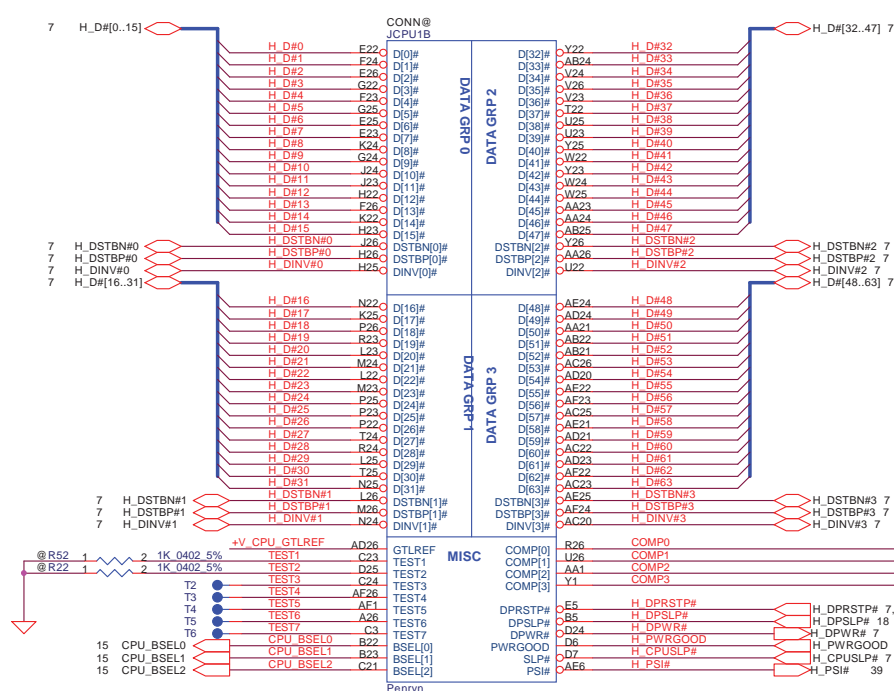
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

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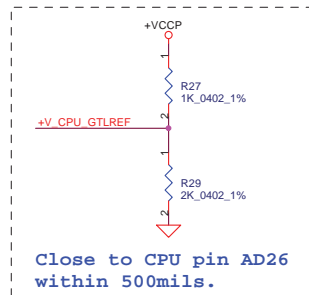


<http://laptop-motherboard-schematic.blogspot.com>



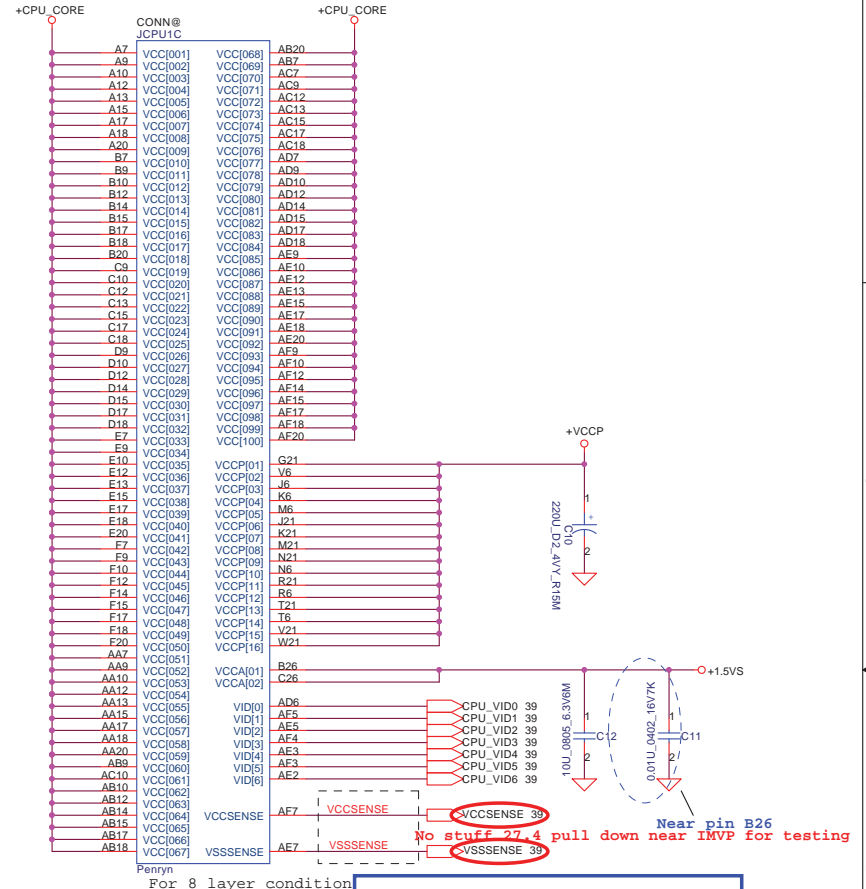
layout note: Rout H_DPRSTP# from ICH9 to IMPV6 then to GMCH & CPU
 layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

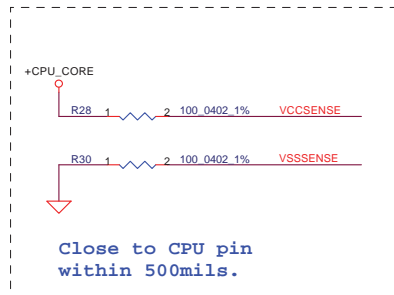


Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4

For 6 layer
 $Z=27.4 \text{ ohm}$
 VCCSENSE, VSSSENSE/ 14mils (MS),
 16mils (SL) width, 7mils space, 25mils
 space to other signals Mismatch = 25mils.

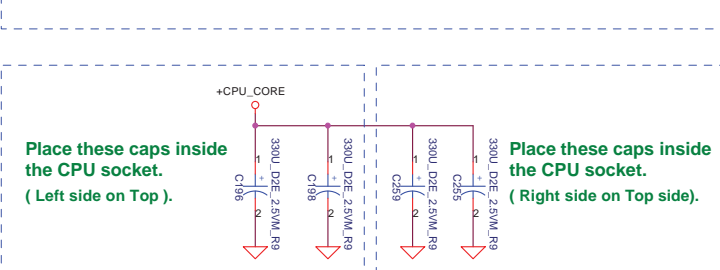
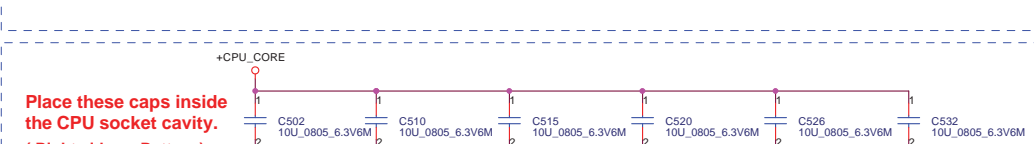
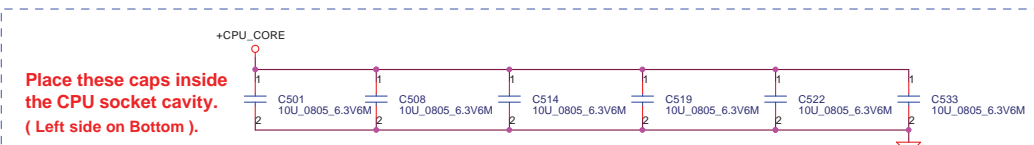
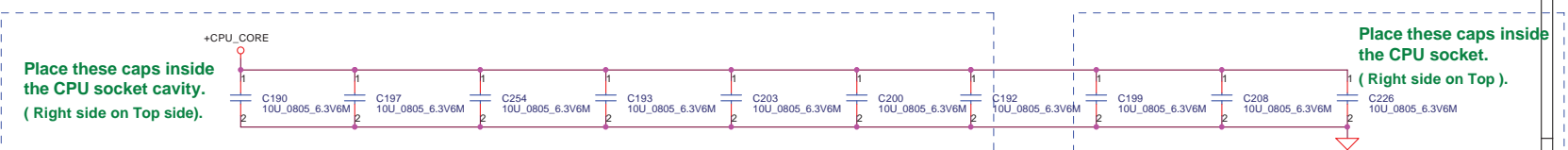
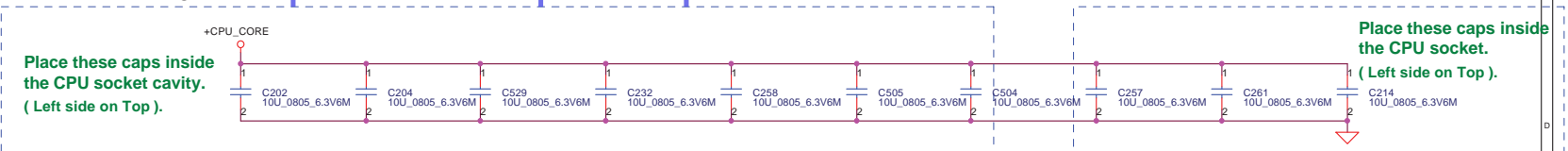


Length match within 25 mils.
 The trace width/space/other is 20/7/25.

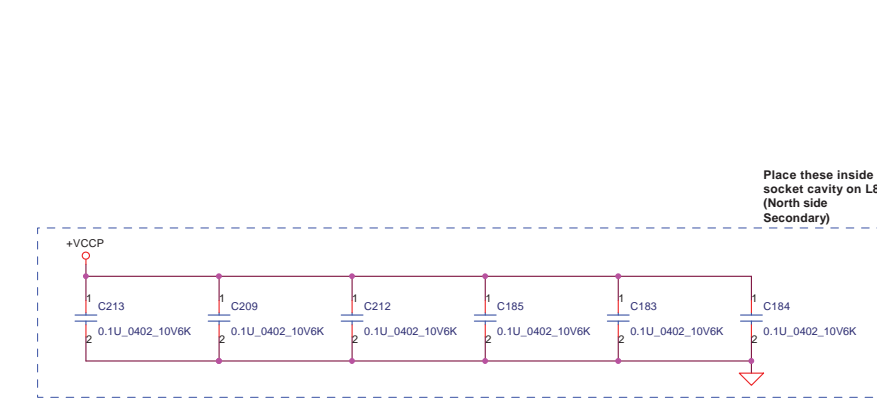


High Frequency Decoupling

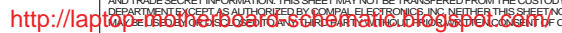
10uF 0805 X5R -> 85 degree.

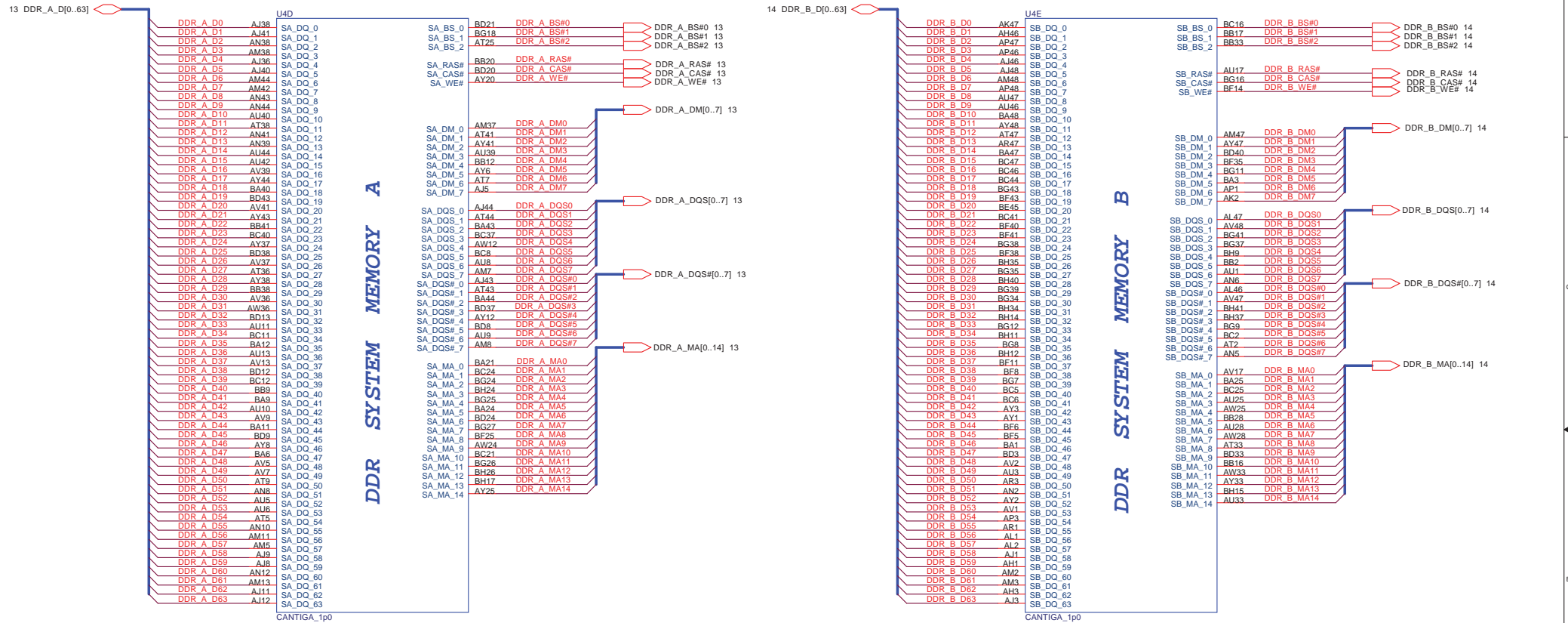


ESR <= 1.5m ohm
Capacitor > 880 uF



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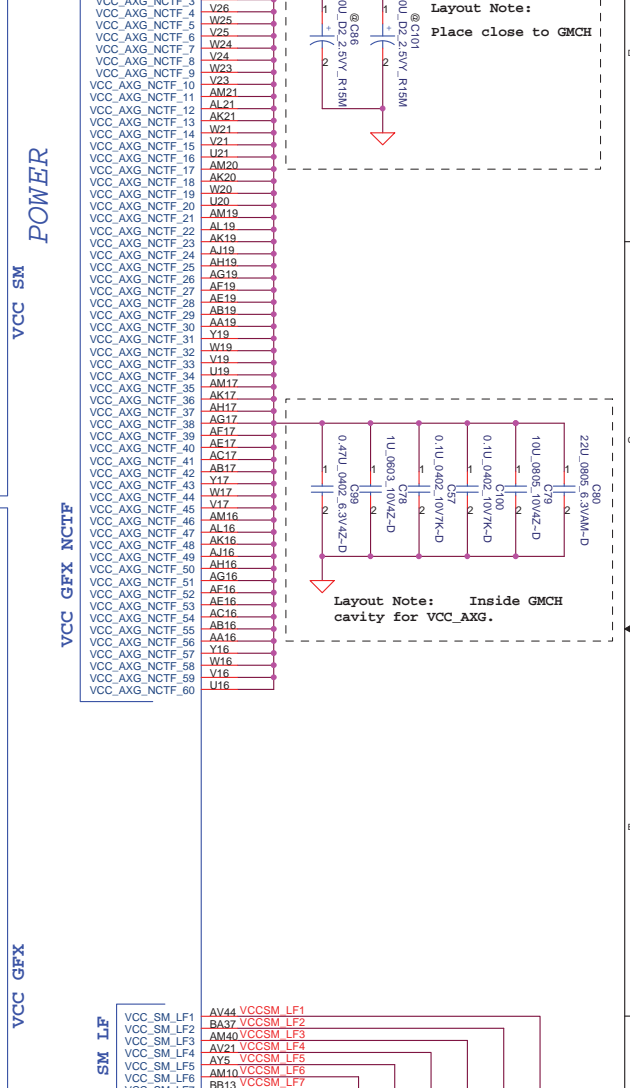
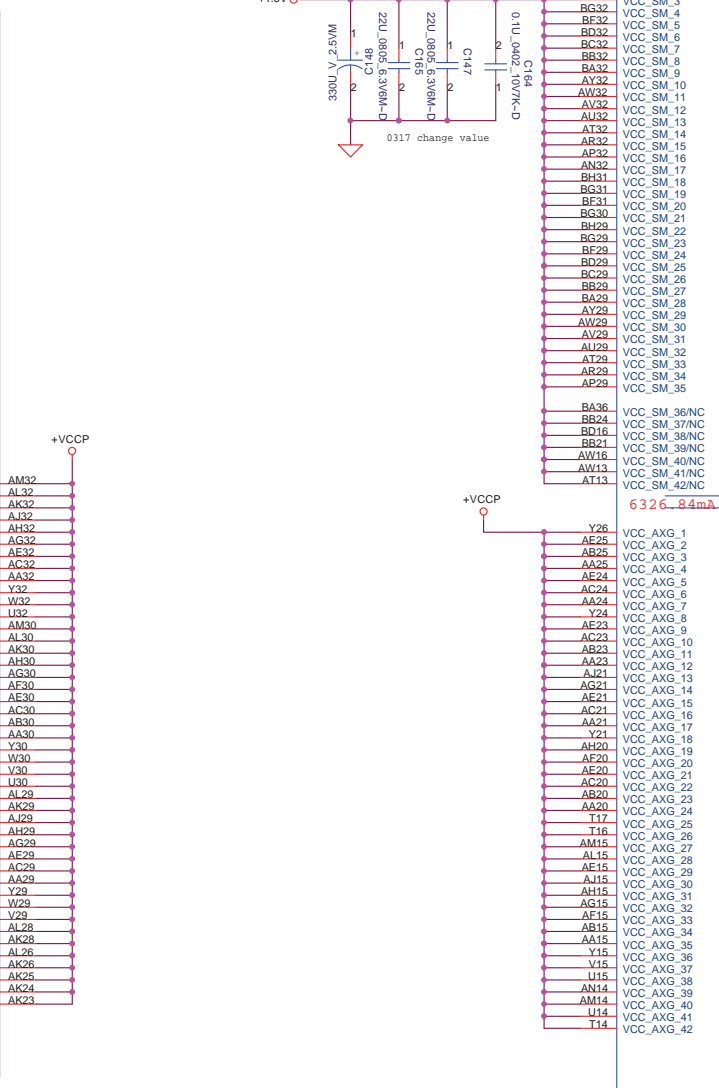
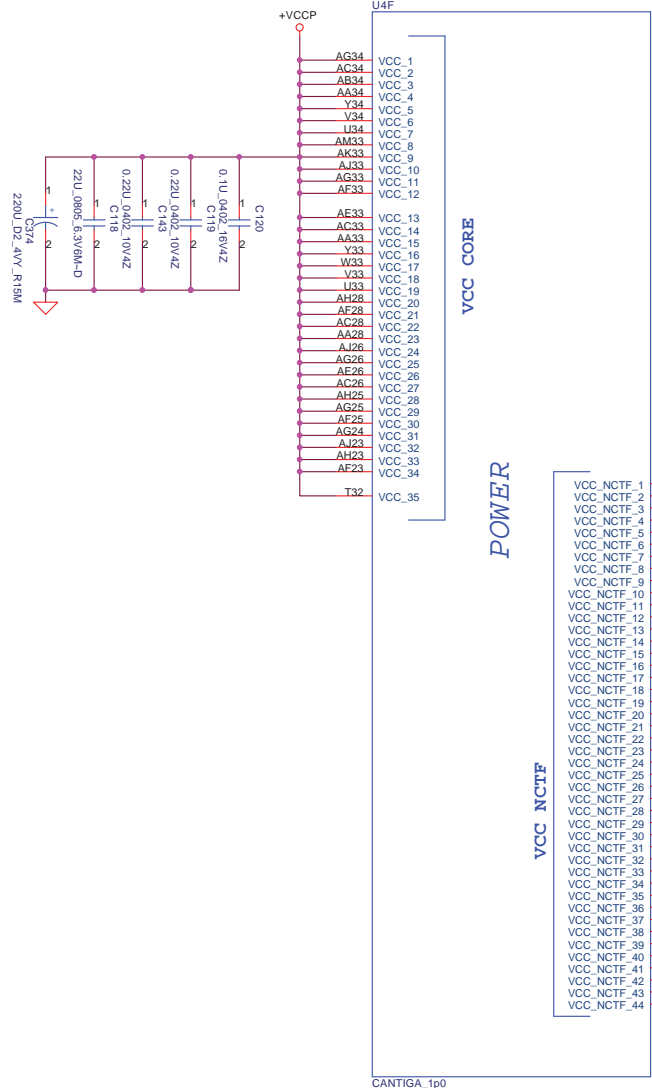
The diagram illustrates two circuit configurations for microcontroller pins:

- CFG5[16] have internal pullup:** This section shows five pins (CFG5, CFG6, CFG7, CFG9, CFG16) each with an internal pullup resistor connected to +3VS. The pins are labeled with their respective resistor values and configurations:
 - CFG5: @ R66, 1, 2, 2.21K, 0402, 1%-D
 - CFG6: @ R58, 1, 2, 2.21K, 0402, 1%-D
 - CFG7: @ R59, 1, 2, 2.21K, 0402, 1%-D
 - CFG9: @ R55, 1, 2, 2.21K, 0402, 1%-D
 - CFG16: @ R70, 1, 2, 2.21K, 0402, 1%-D
- CFG19[20] have internal pulldown:** This section shows two pins (CFG19, CFG20) each with an internal pulldown resistor connected to +3VS. The pins are labeled with their respective resistor values and configurations:
 - CFG19: @ R72, 1, 2, 4.02K, 0402, 1%-D
 - CFG20: @ R73, 1, 2, 4.02K, 0402, 1%-D

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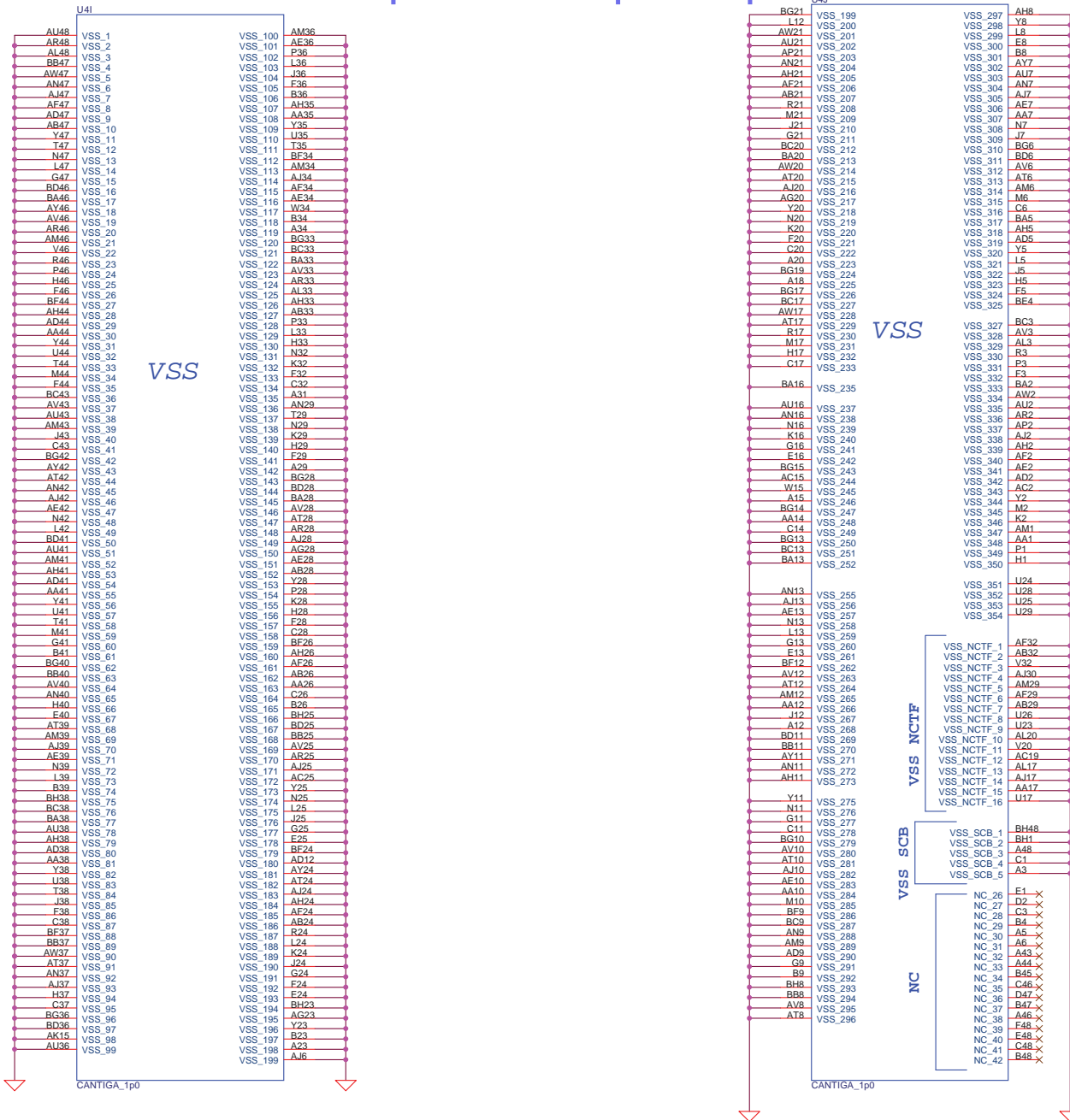


Extenal Graphic: 1210.34mA
integrated Graphic: 1930.4mA



Layout Note:
Place close to GMCH

Layout Note:
Inside GMCH cavity for VCC_AXG.

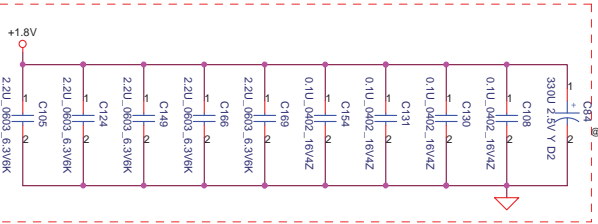


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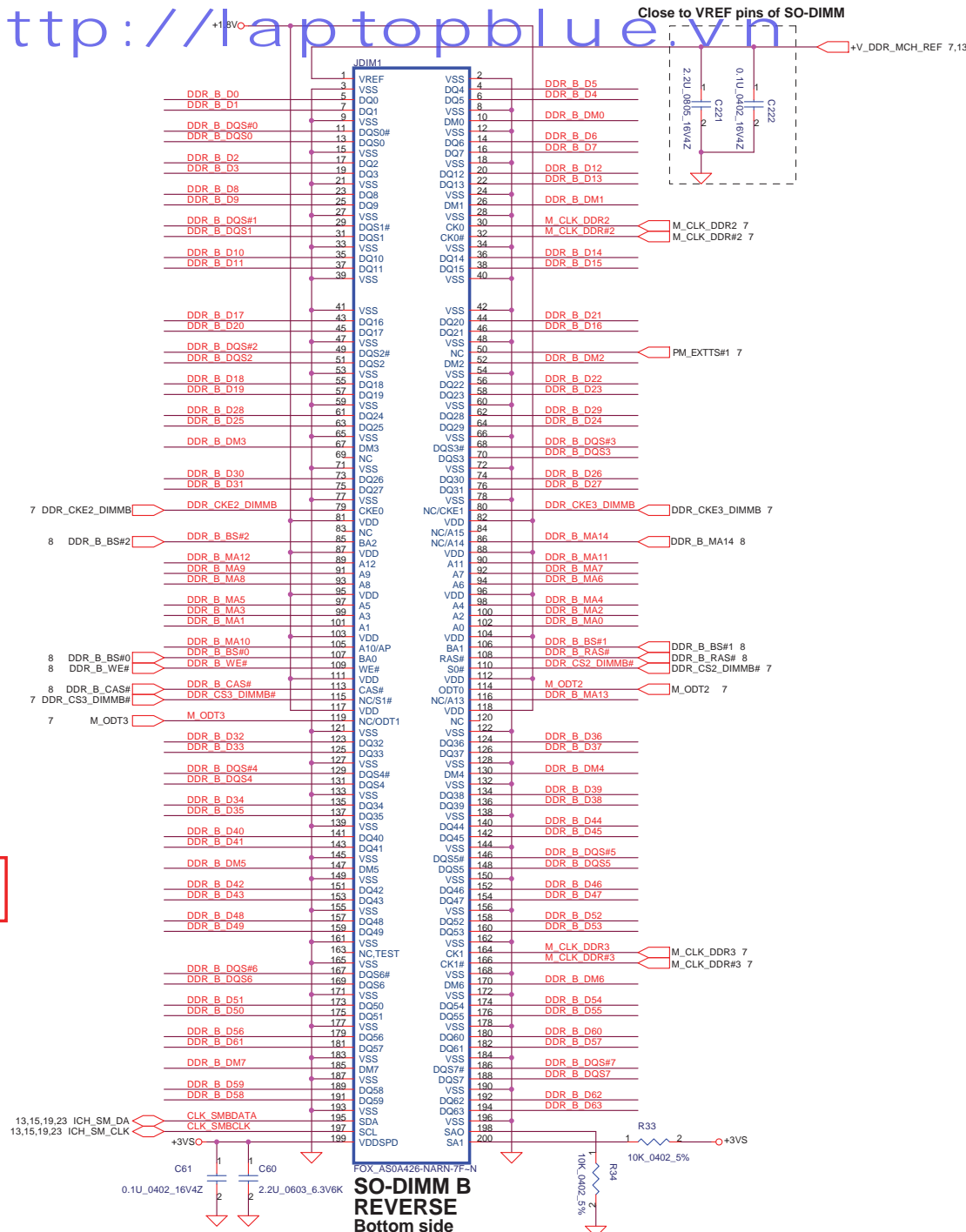


Layout Note:
Place near JDIM1



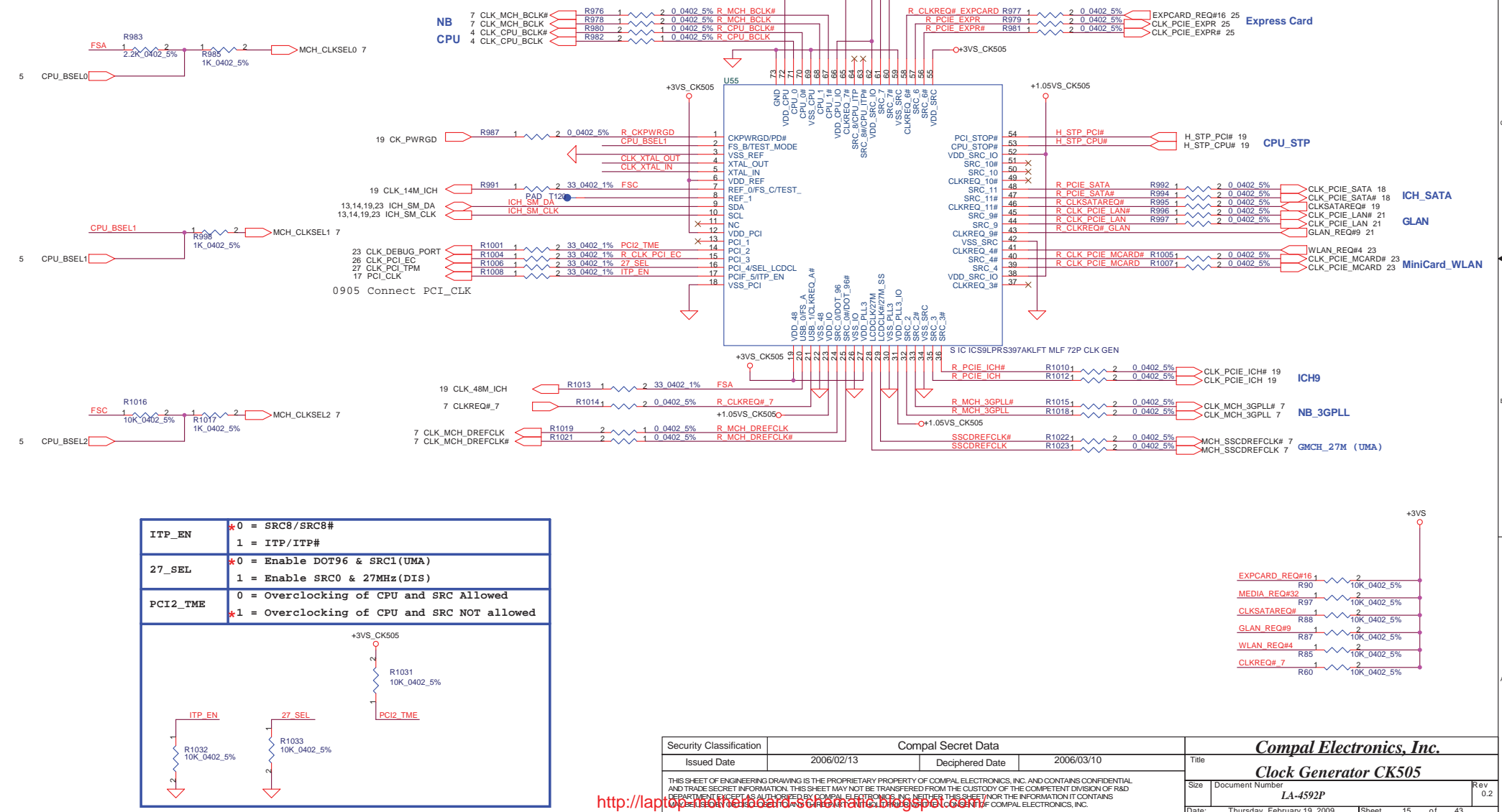
Layout Note:
Place these resistor
closely JP42,all
trace length Max=1.5"

h t t p : / / l a p t o p b l u e . y n



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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



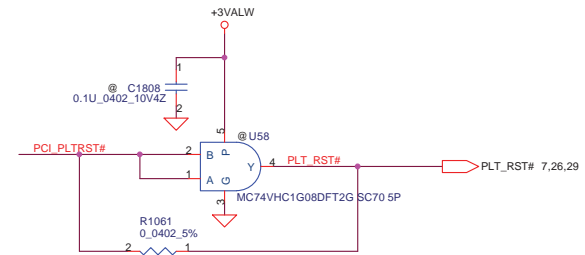
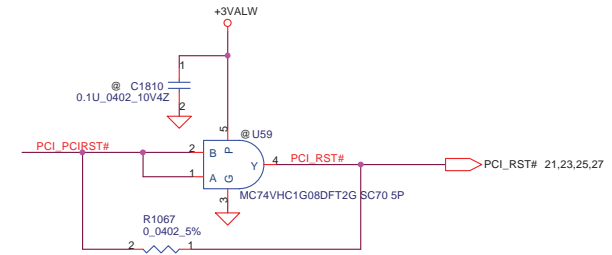
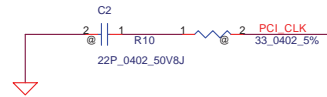
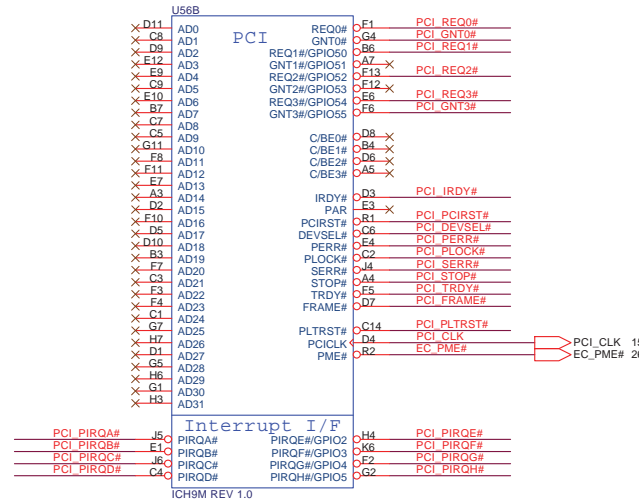
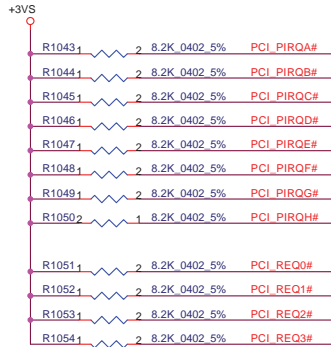
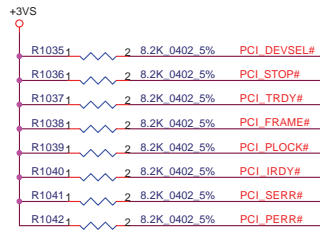
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W=60mils



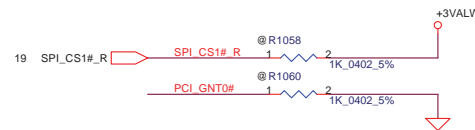
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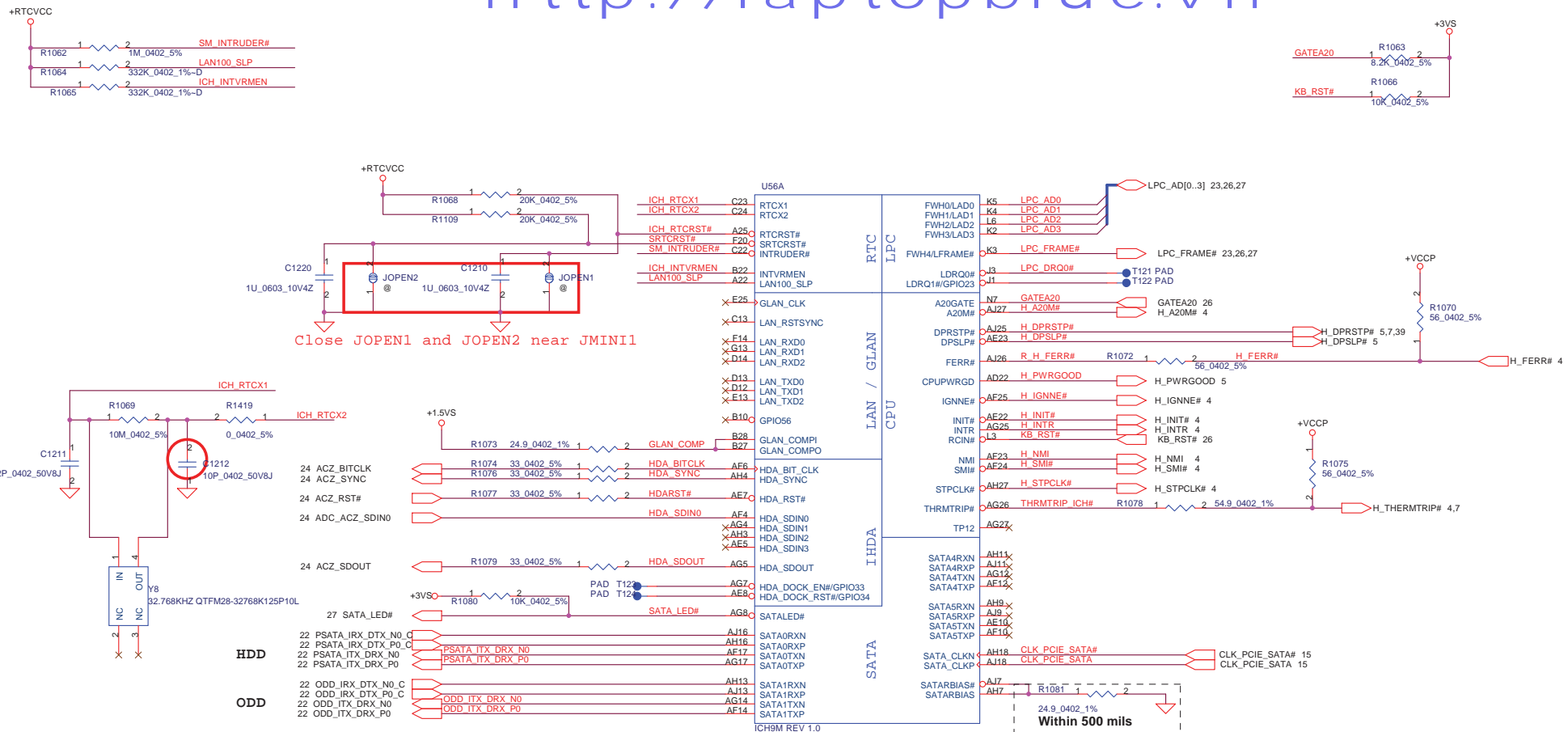
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



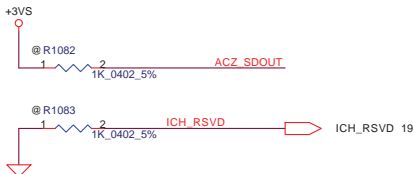
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



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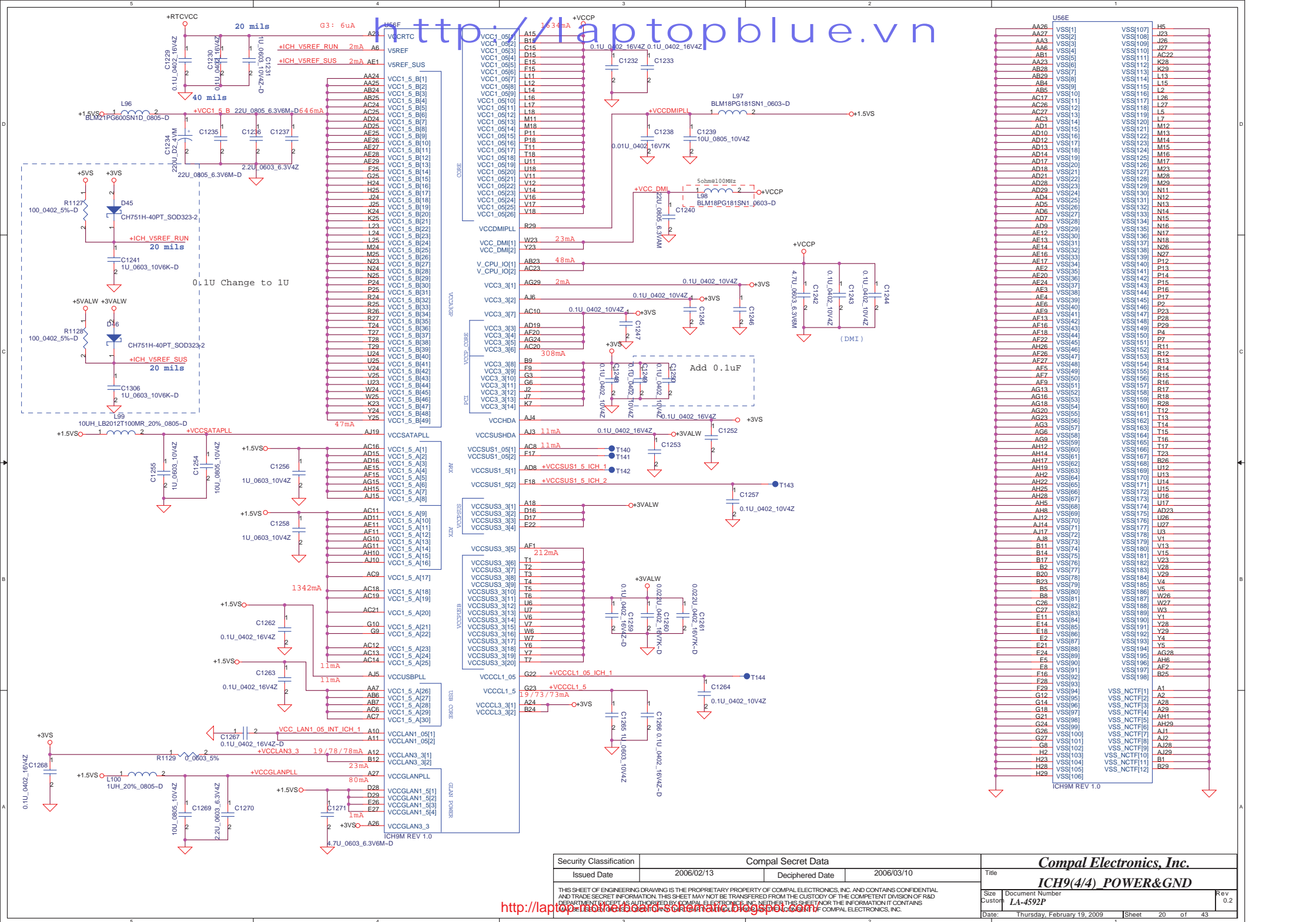


XOR CHAIN ENTRANCE STRAP:RSVD



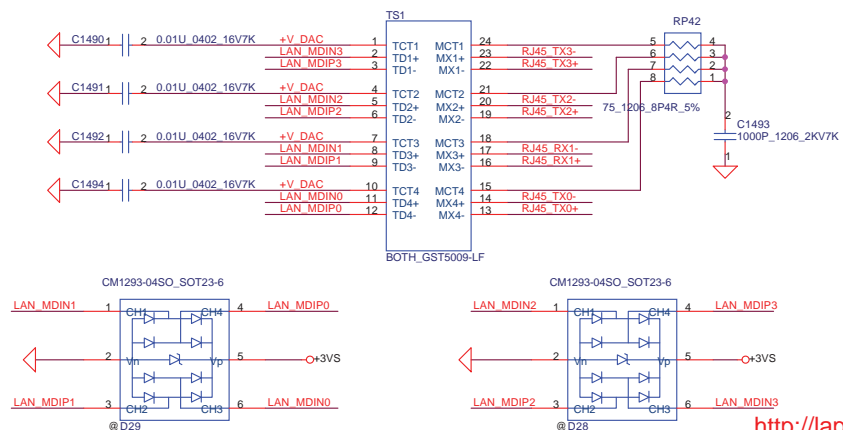
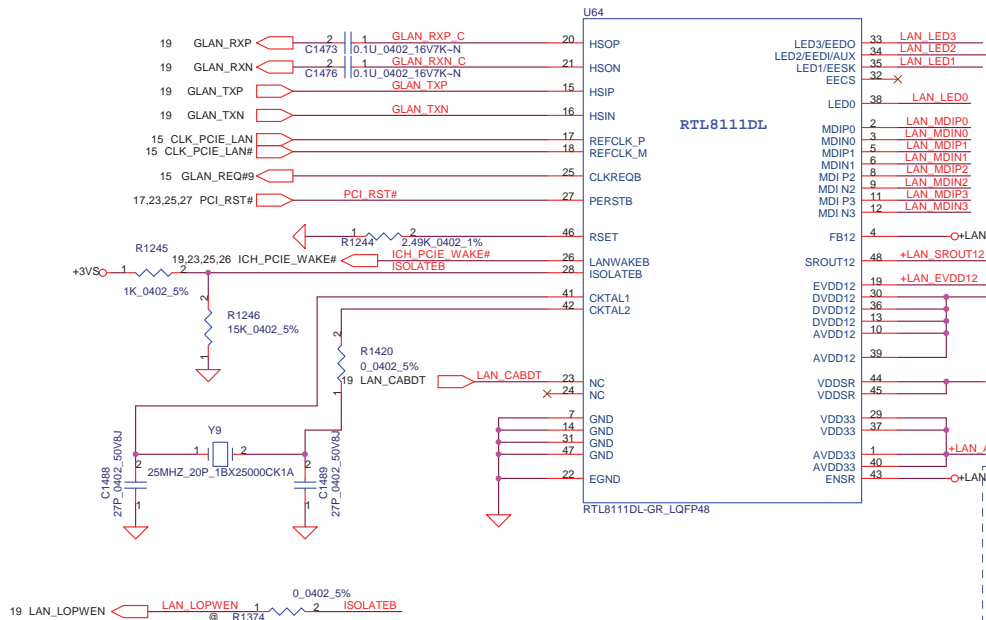
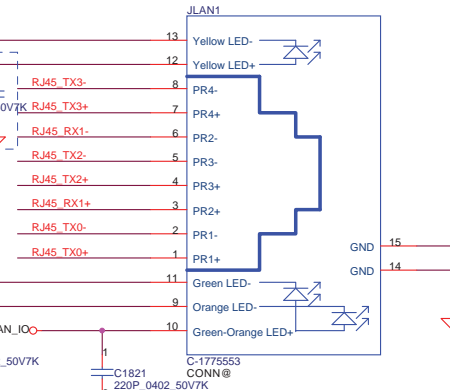
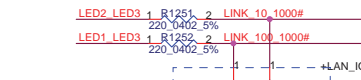
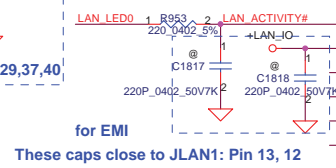
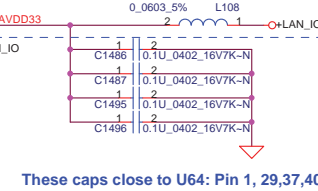
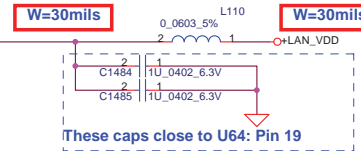
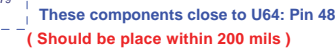
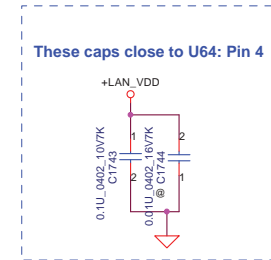
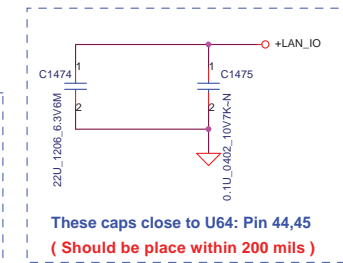
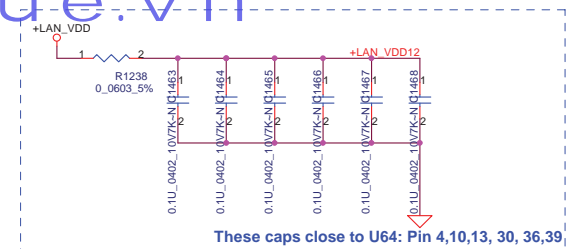
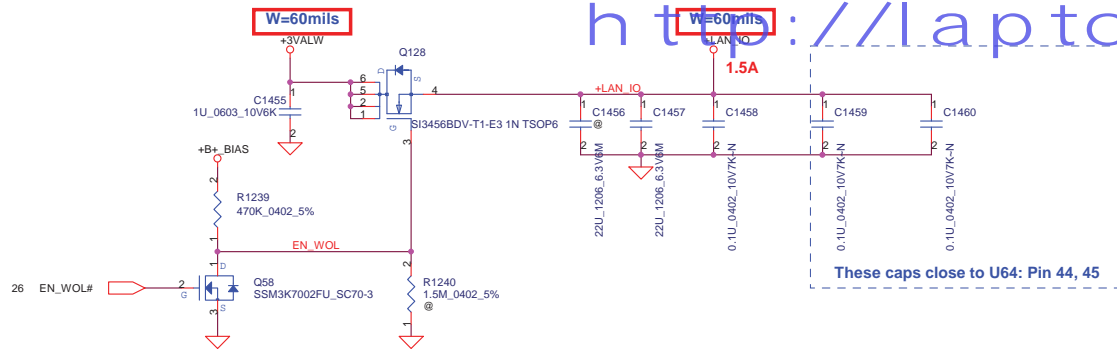
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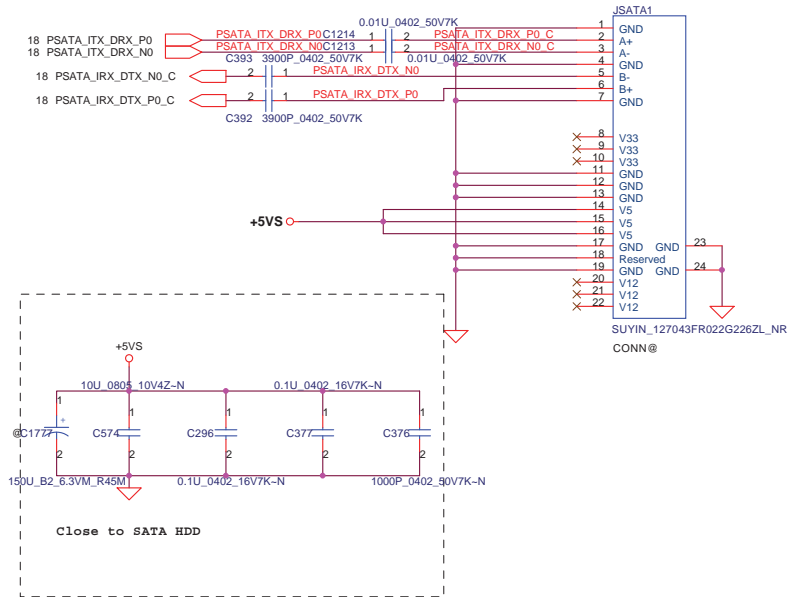
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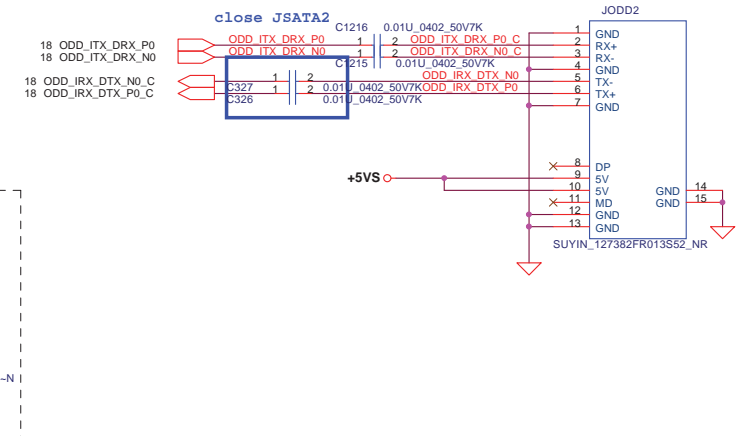


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SATA HDD CONN

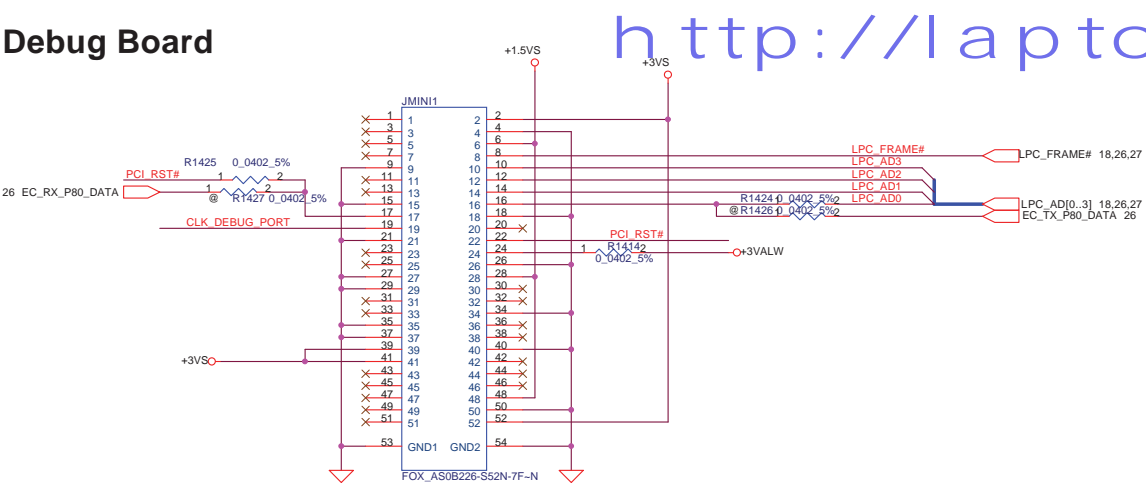


SATA ODD CONN

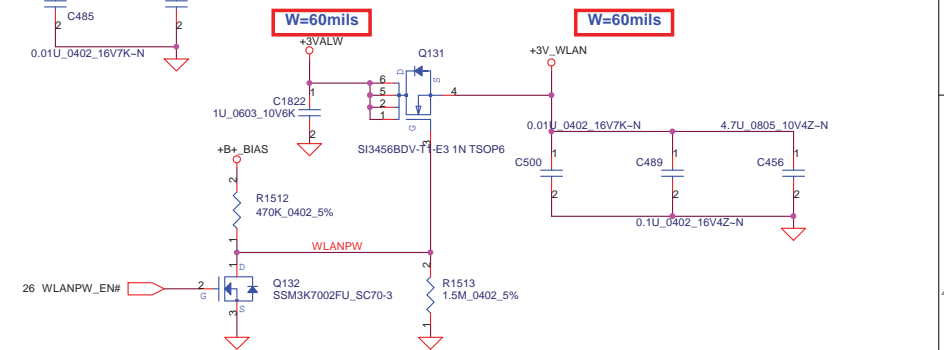
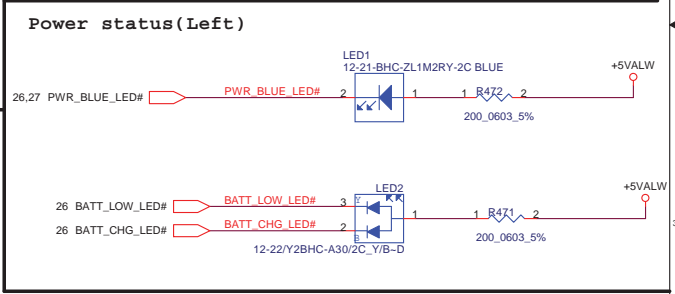
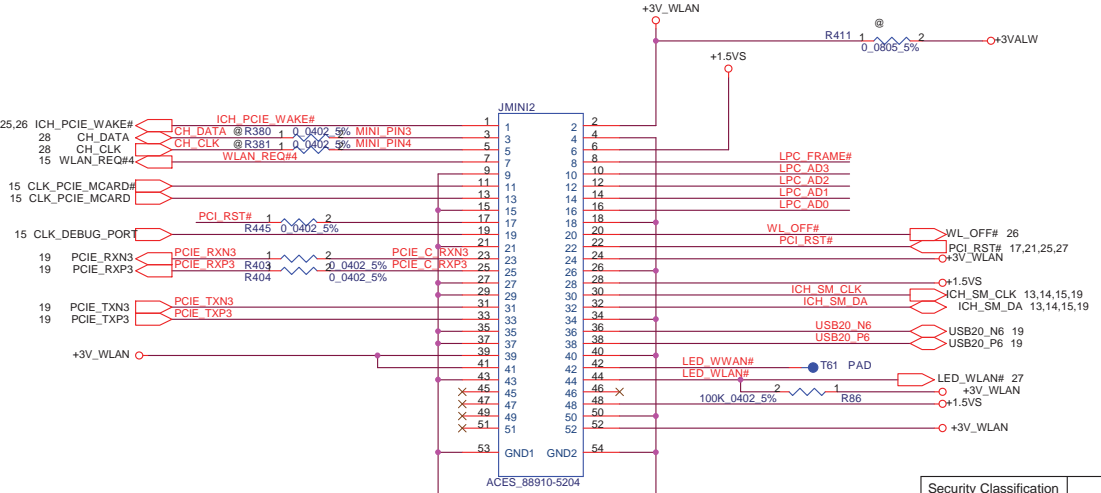


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				Customer	LA-4592P
				Date	Thursday, February 19, 2009
				Sheet	22 of 43
				Rev	0.2

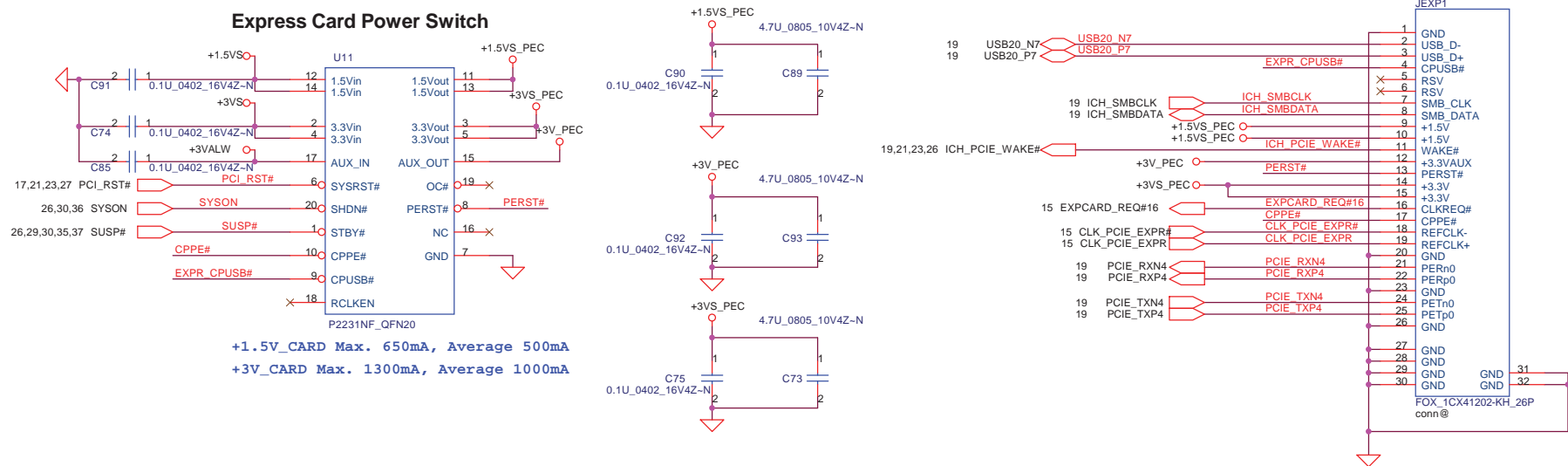
Debug Board



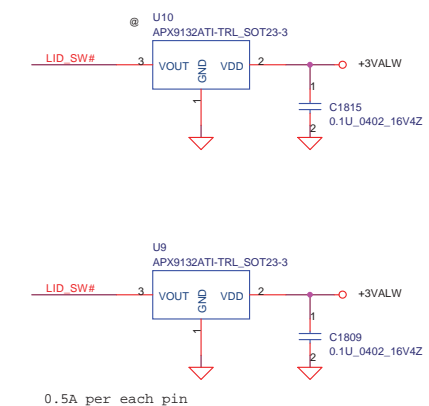
Mini-Express Card---WLAN



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INT. KBD. CONN.



INT. KBD. CONN.



INT. KBD. CONN.



INT. KBD. CONN.



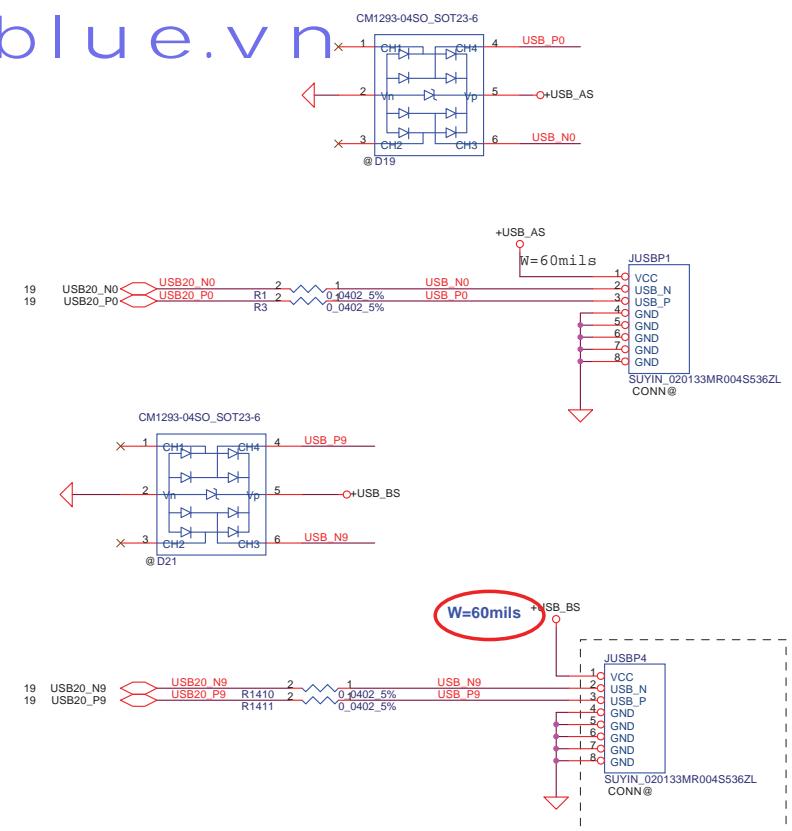
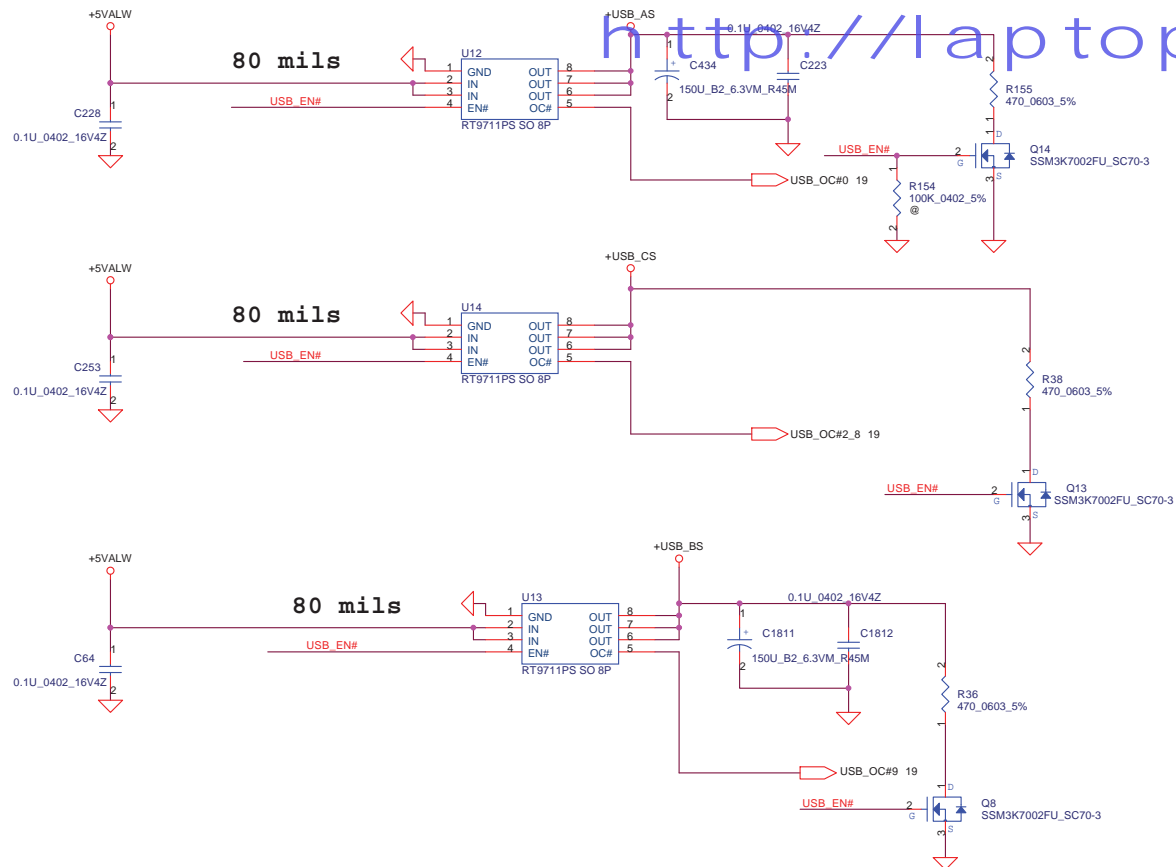
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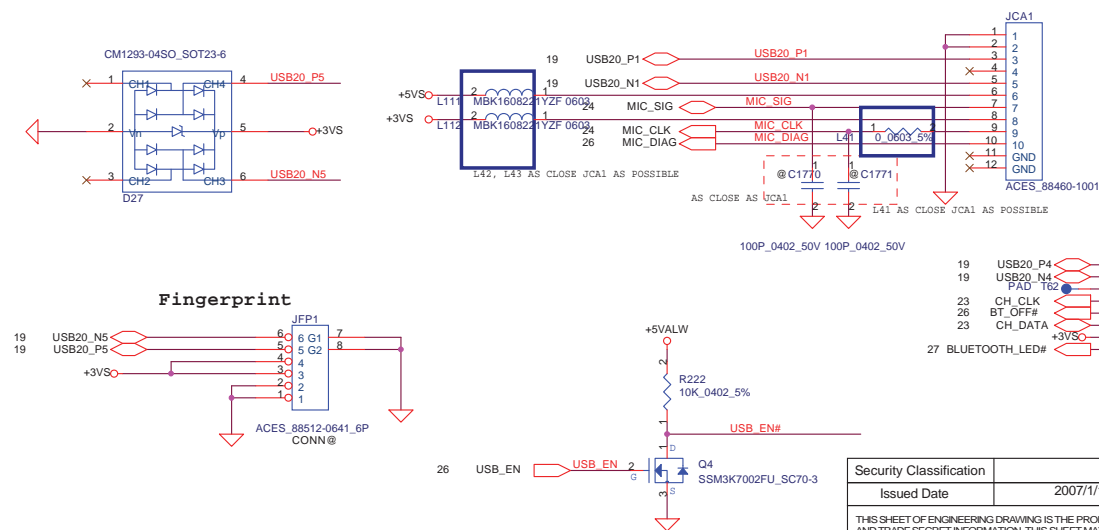
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INT. KBD. CONN.

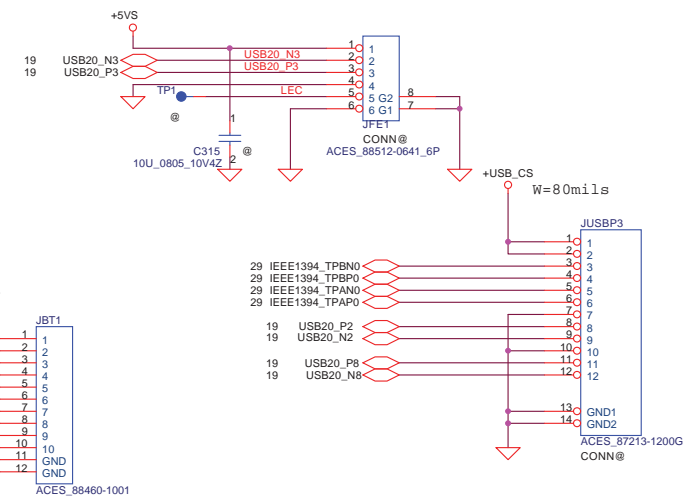


Check Module pin define Camera Conn



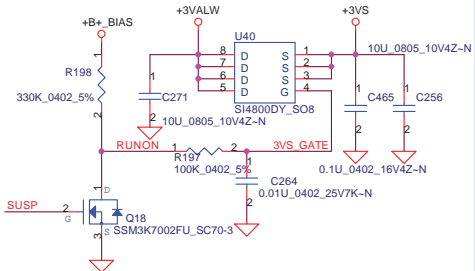
Bluetooth

Felica Conn

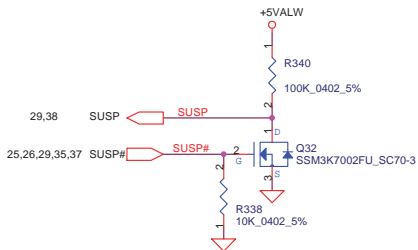
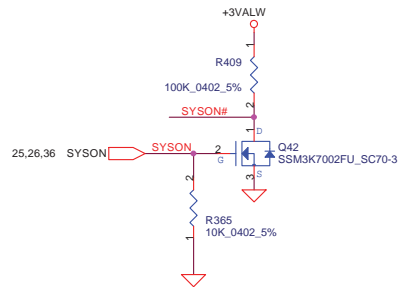
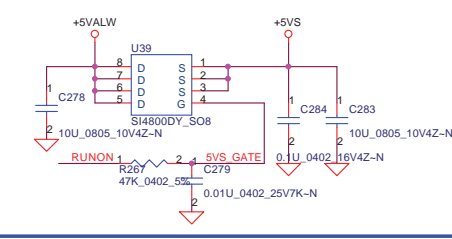


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								USB/BlueTooth/FP/Felcia	
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+3VALW to +3VS Transfer

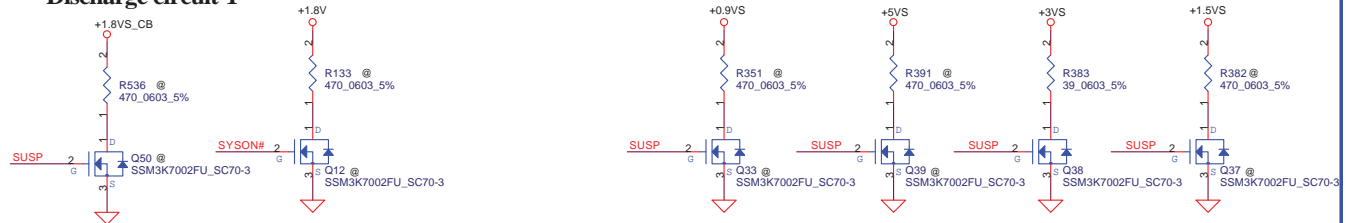


+5VALW to +5VS Transfer



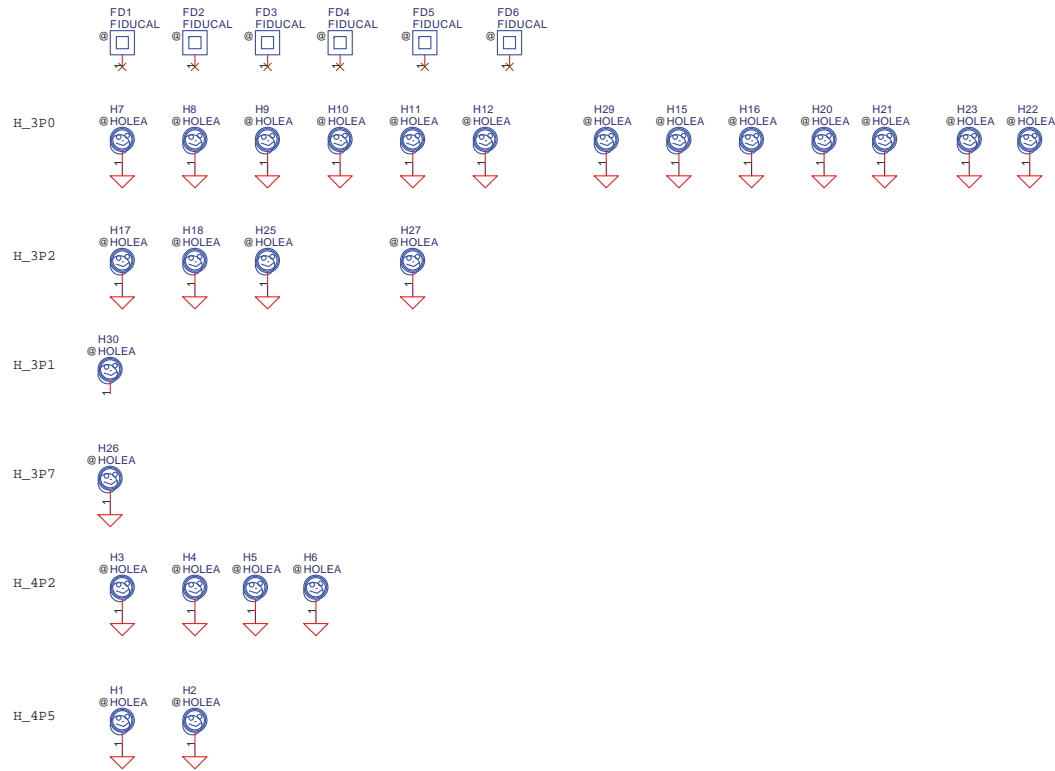
VGA Discharge circuit

Discharge circuit-1

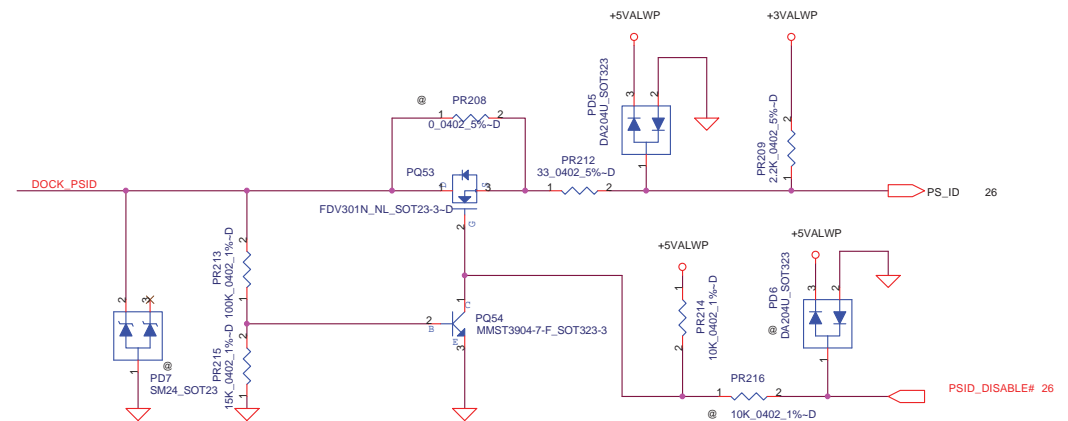
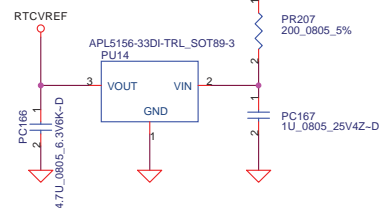
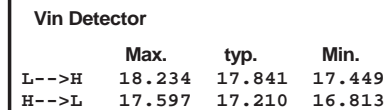
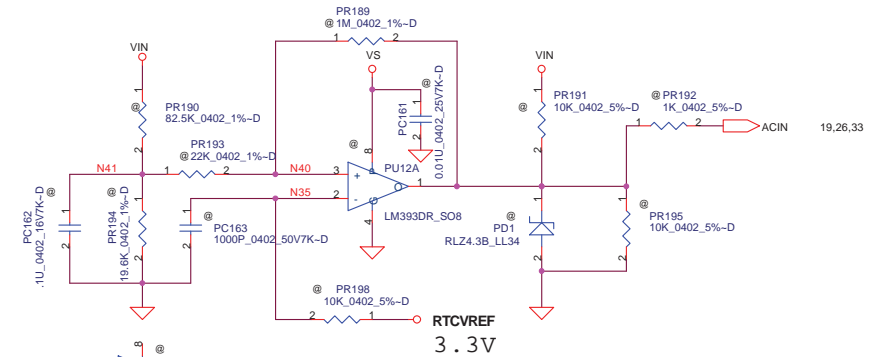


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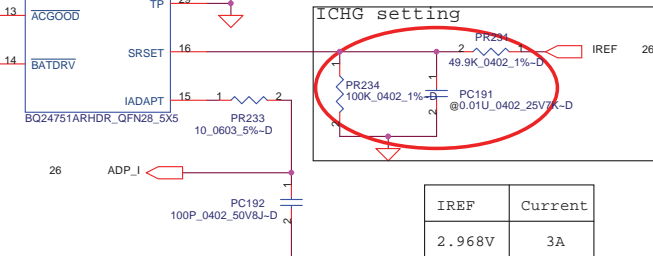
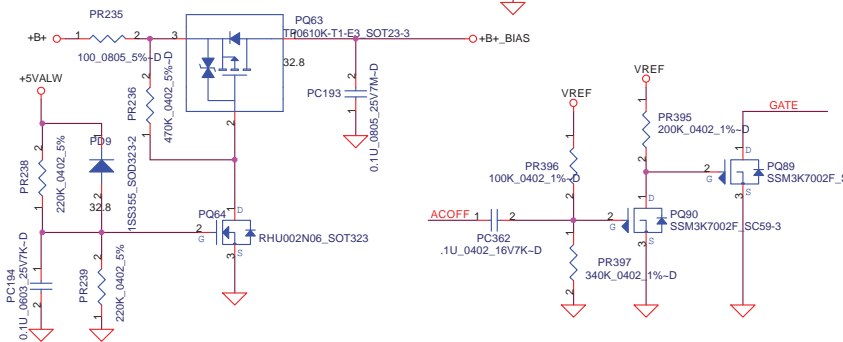
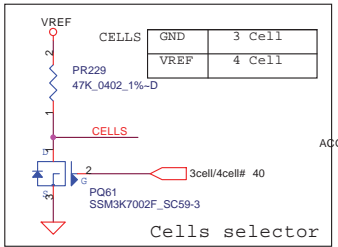


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				Sheet	31 of 43

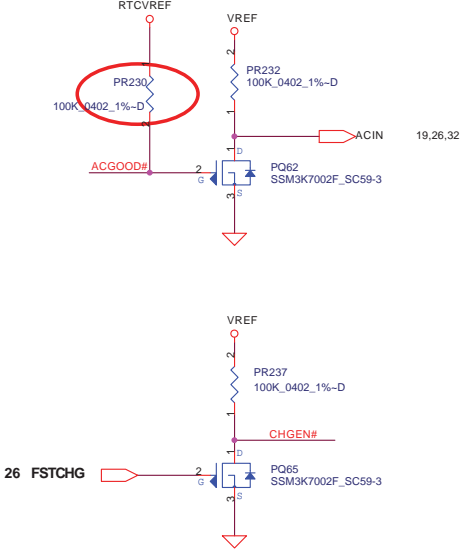
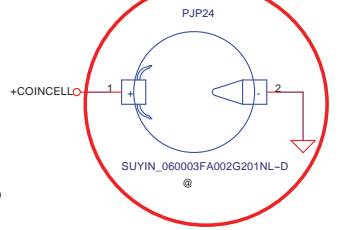


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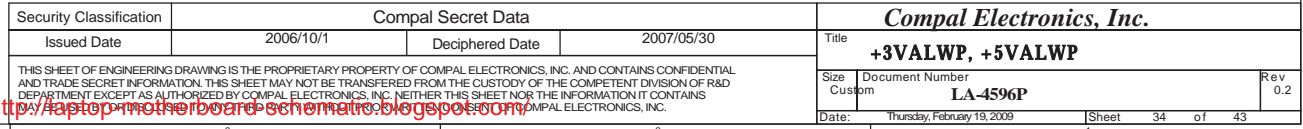
90W adapter
 $I_{charge} = (V_{srset}/V_{vdac}) * (0.1/PR34) = 3.34A$
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR17) = 3.1A$
 Input OVP : 22.3V
 Input UVP : 16.98V
 Fsw : 300KHz

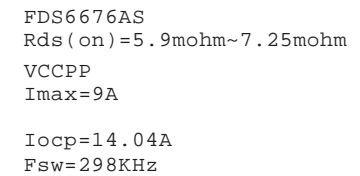


COIN RTC Battery

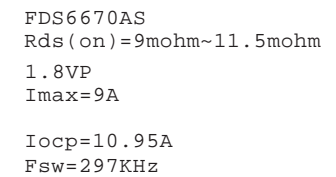


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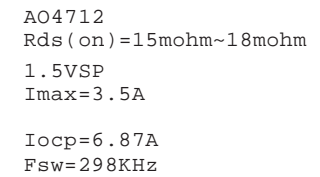




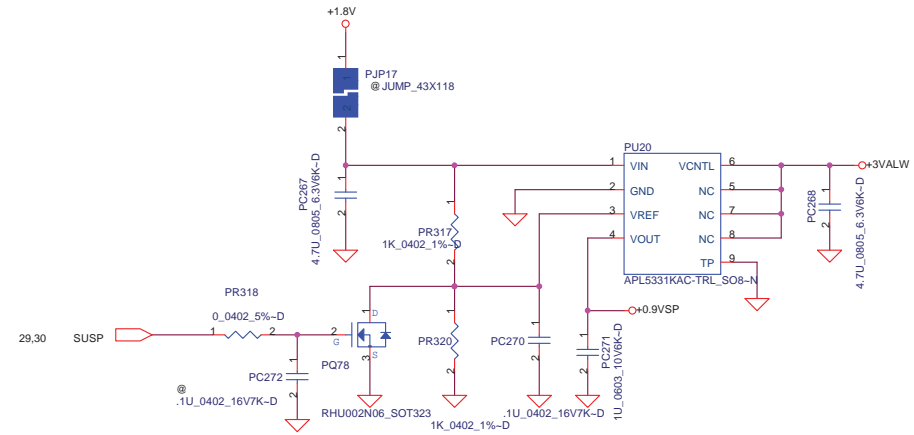
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Battery Connect/OTP

PJPB1 battery connector

SMART Battery:

- 1.BAT+
- 2.BAT+
- 3.ID
- 4.B/I
- 5.TS
- 6.SMD
- 7.SMC
- 8.GND
- 9.GND

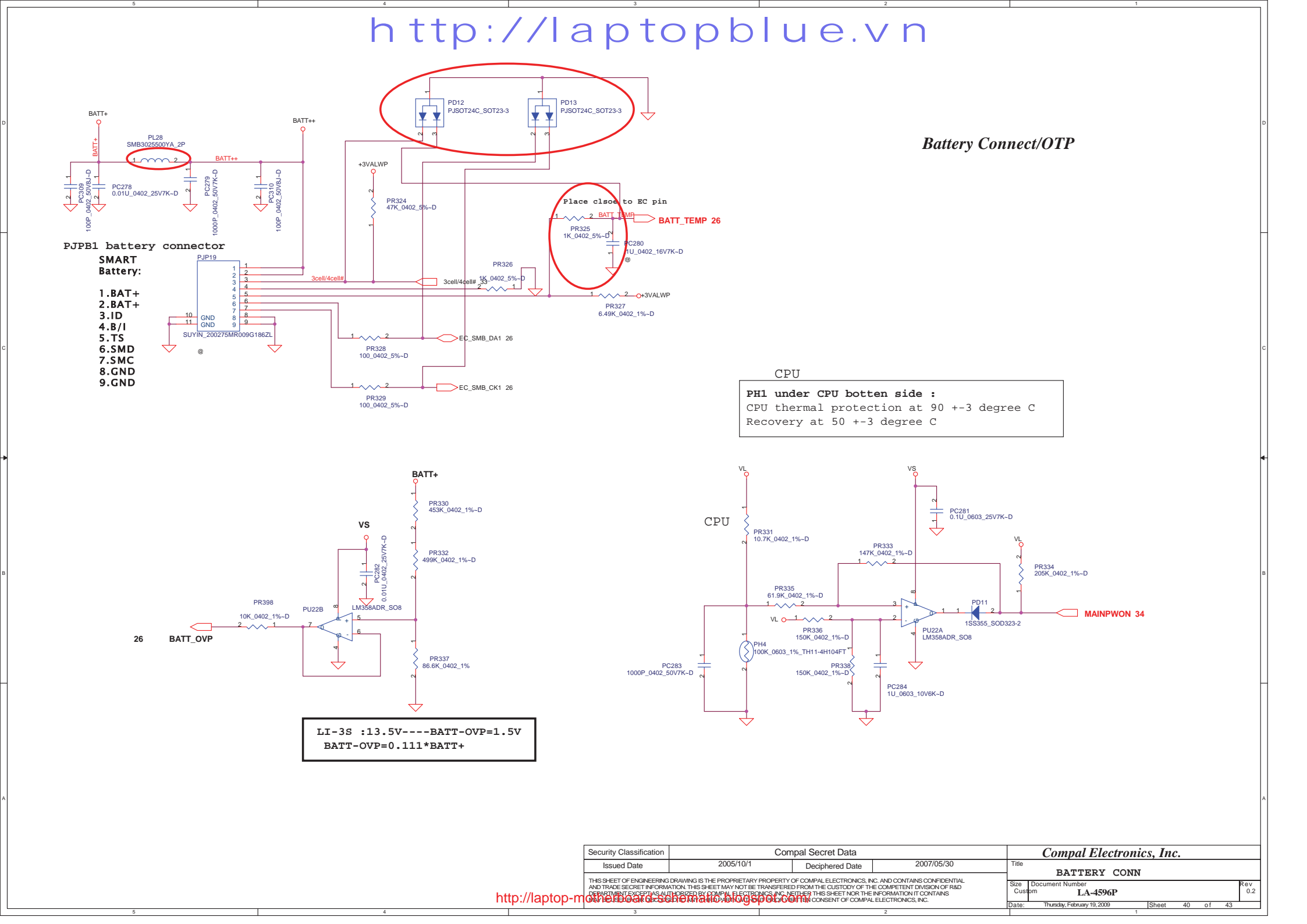
LI-3S :13.5V---BATT-OVP=1.5V
BATT-OVP=0.111*BATT+

CPU

PH1 under CPU bottom side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C

MAINPWON 34

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Battery Connect/OTP

PJPB1 battery connector

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MAINPWON 34

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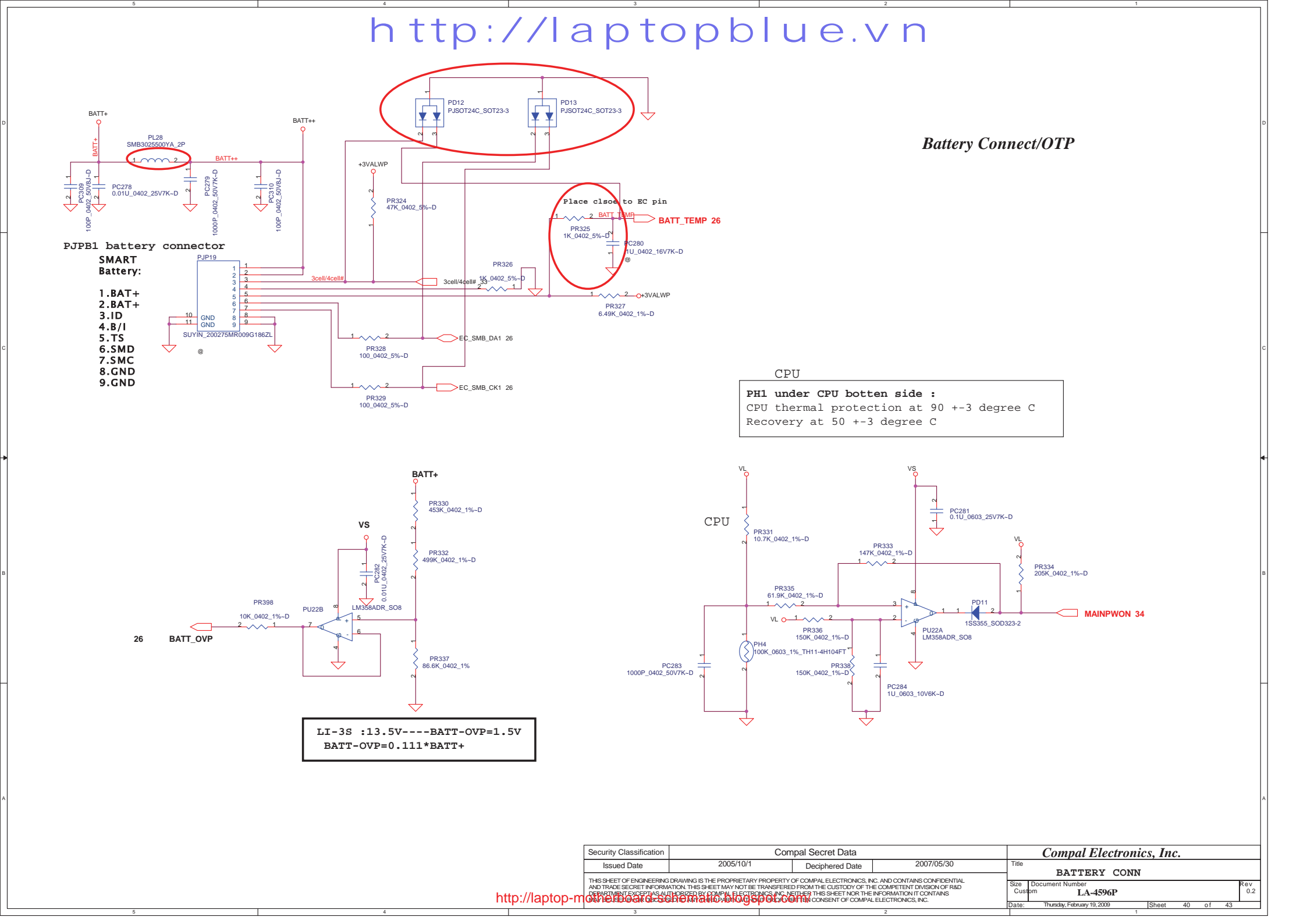
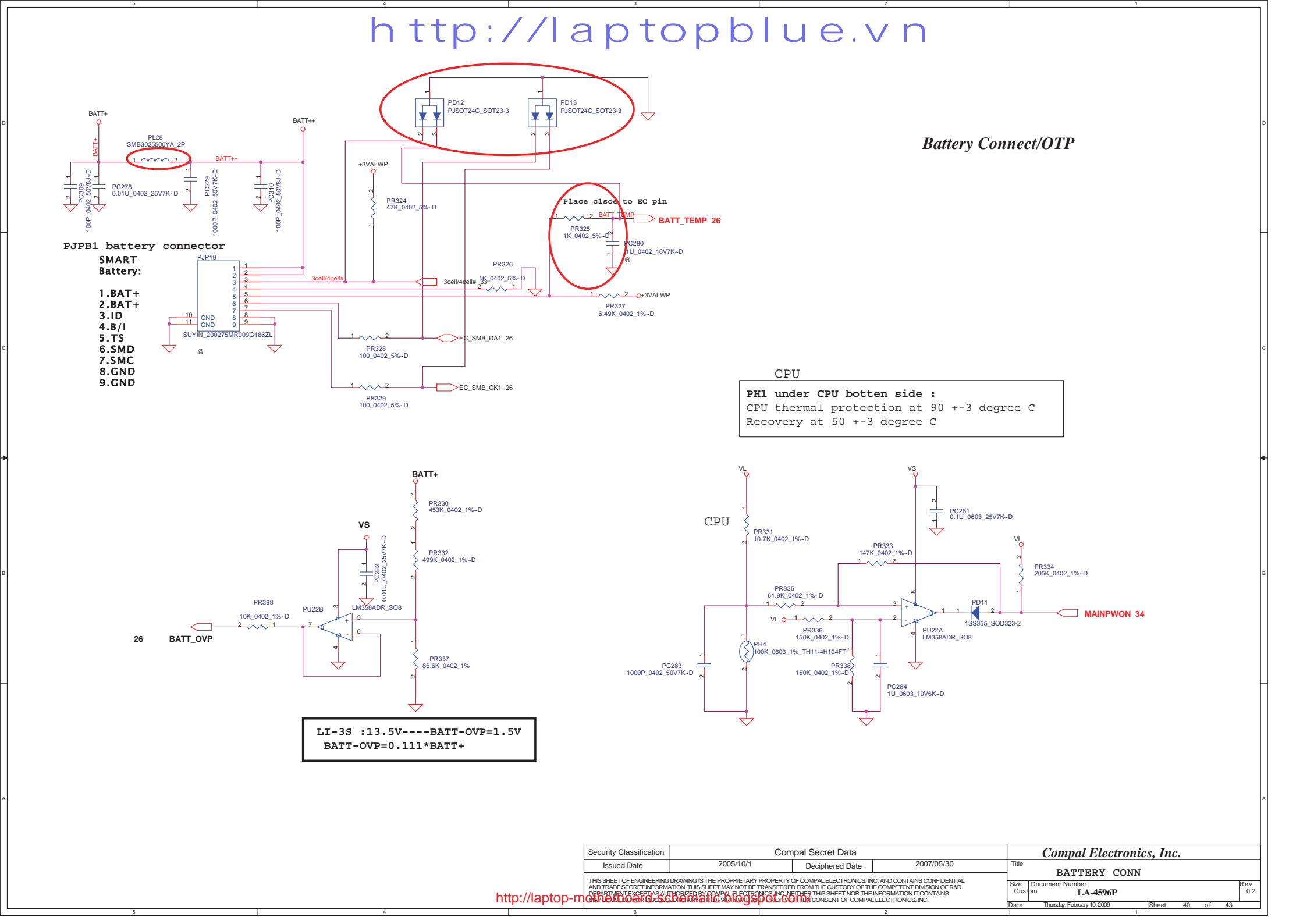
LI-3S :13.5V---BATT-OVP=1.5V
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MAINPWON 34

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BATT-OVP=0.111*BATT+

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Recovery at 50 +-3 degree C

MAINPWON 34

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	32	DCIN /Vin Detector	08/12/08	COMPAL	common circuit design modify	change PR203 from 33 to 68 and add PR204 to 68	0.3
2			08/12/08	COMPAL	design modify	change PL17 from SM010018880 to SM010008E10	0.3
3	33	Charger	08/12/08	COMPAL	vendor FAE suggest	change PR272 PR339 from 1 to 3.3	0.3
4	40	BATTERY CONN	08/12/08	COMPAL	design modify	change PL28 from SM010018210 to SM010008E10	0.3
5	32	DCIN /Vin Detector	08/12/12	COMPAL	increase capacitor for EMI request	add PC313 at 0.01uf and PC314 at 0.1uf	0.3
6	35	VCCPP	08/12/12	COMPAL	change resister for EMI request	change PR342 from 0 to 2.2	0.3
7	36	1.8VP	08/12/12	COMPAL	change resister for EMI request	change PR352 from 0 to 2.2	0.3
8	37	1.5VSP	08/12/12	COMPAL	change resister for EMI request	change PR362 from 0 to 2.2	0.3
9	35	VCCPP	08/12/18	COMPAL	add resister and capacitor for EMI request	add PR346 at 4.7and pc323 at 680p	0.3
10	36	1.8VP	08/12/18	COMPAL	add resister and capacitor for EMI request	add PR356 at 4.7and pc334 at 680p	0.3
11	37	1.5VSP	08/12/18	COMPAL	add resister and capacitor for EMI request	add PR367 at 4.7and pc344 at 680p	0.3
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		Date:		Thursday, February 19, 2009	
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	28	USB/BT/ FP/ Felica/Camera	2008/12/02	Compal_HW	Small USB board no function	Modify Pin definition of JUSBP3	0.2
2	24	HDA-IDT_92HD81	2008/12/02	Compal_HW	R voice and L voice fail	Modify Pin definition of JSPK1	0.2
3	27	PWR_OK/ BTN/ KB / TP/TPM1.2	2008/12/02	Compal_HW	Switch function fail	Modify Pin definition of SW1	0.2
4	21	LAN-8111D	2008/12/16	Compal_HW	EMI LAN test fail	Add C1817-C1820 for LAN connector	0.2
5	23	Mini-Card/WWAN/Roboson	2008/12/16	Compal_HW	S5 wake on Wirlesslan fail	Add U89 to control wirless lan voltage	0.2
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