

Model Name: KML50 DIS  
PCB NO: LA-4595PR04  
BOM P/N: DA80000DR00

http://laptopblue.vn

# Half Penny Bridge 15.4

# Compal Confidential

## Schematic Document

## Cantiga + ICH9

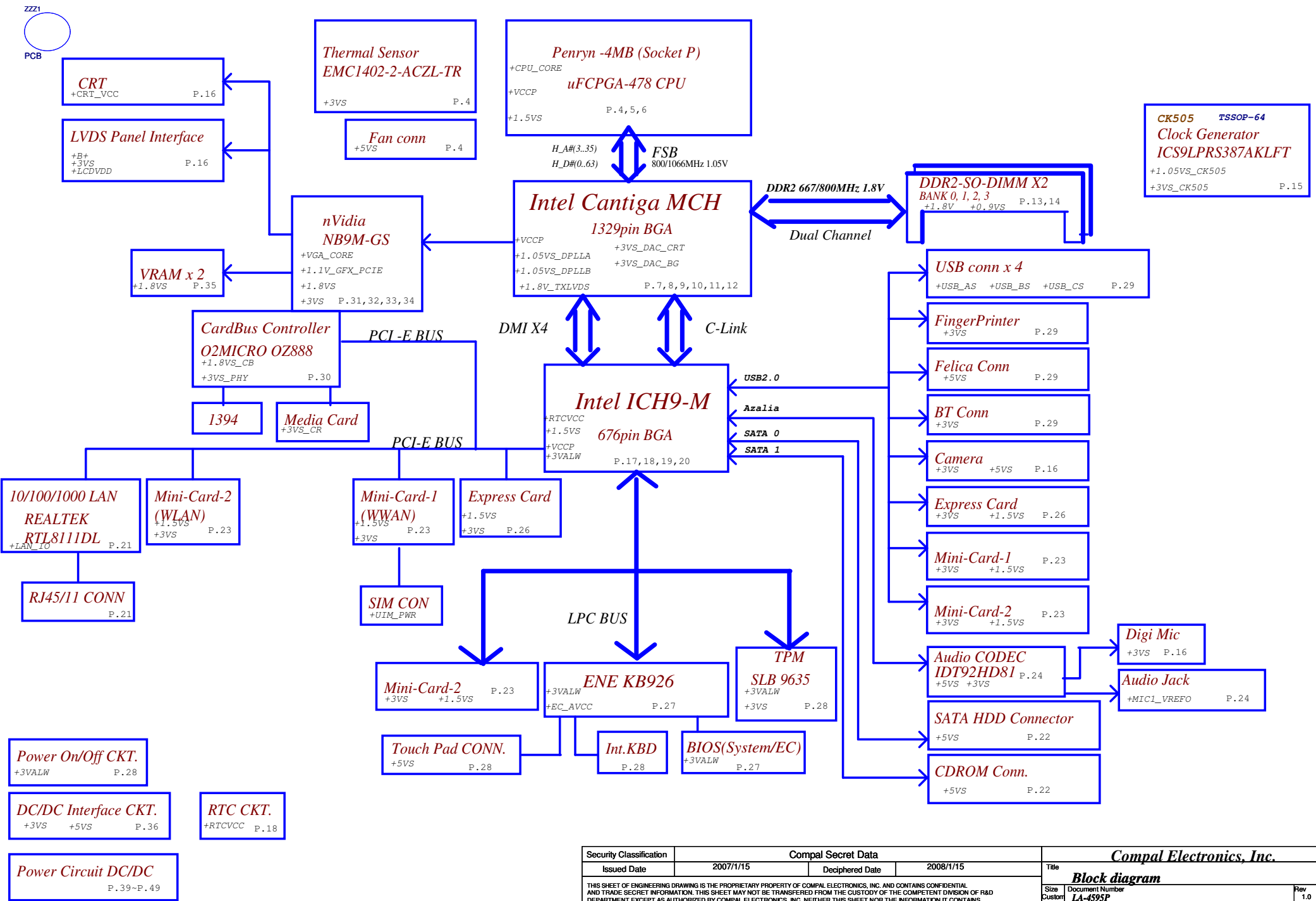
2009 / 02 / 17 Rev:1.0 (A00)

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File Name : LA-4595P

# Half Penny Bridge 15.4 DIS



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# Voltage Rails

O MEANS ON X MEANS OFF

power plane				
State				
				+5VS +3VS +1.5VS +0.9VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +1.1V_GFX_PCIEP
	+B	+5VALW +3VALW	+1.8V	
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

ICH9-M	USB PORT#	DESTINATION
	0	JUSBP1
	1	CAMERA
	2	JUSBP3 TOP
	3	Felica
	4	Blue Tooth
	5	Finger Printer
	6	JMINI2-WLAN
	7	Express card
	8	JUSBP3 BOT
	9	JMINI1-WWAN
	10	JUSBP4
	11	NA

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Symbol Note :



: means Digital Ground



: means Analog Ground

@ : means just reserve , no build

CON@ : means ME connectors

TPM@ : means TPM function

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	GLAN RTL8111DL
Lane 3	MINI CARD-2 WLAN
Lane 4	EXPRESS CARD
Lane 5	CARD READER OZ888
Lane 6	NA

SATA	DESTINATION
Lane 0	HDD
Lane 1	ODD
Lane 4	NA
Lane 5	NA

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	X	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

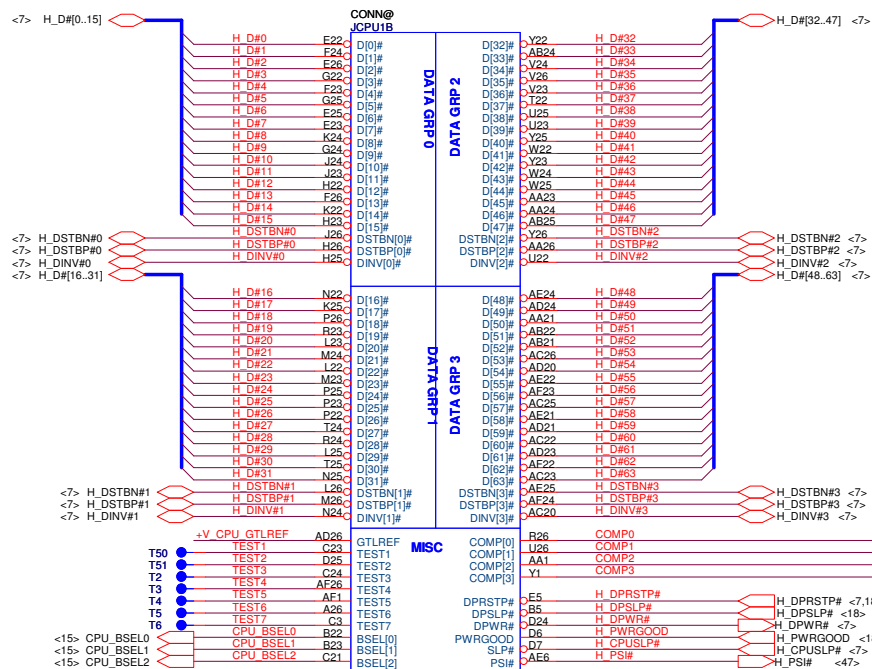
## I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010
LED panel	58	01011000

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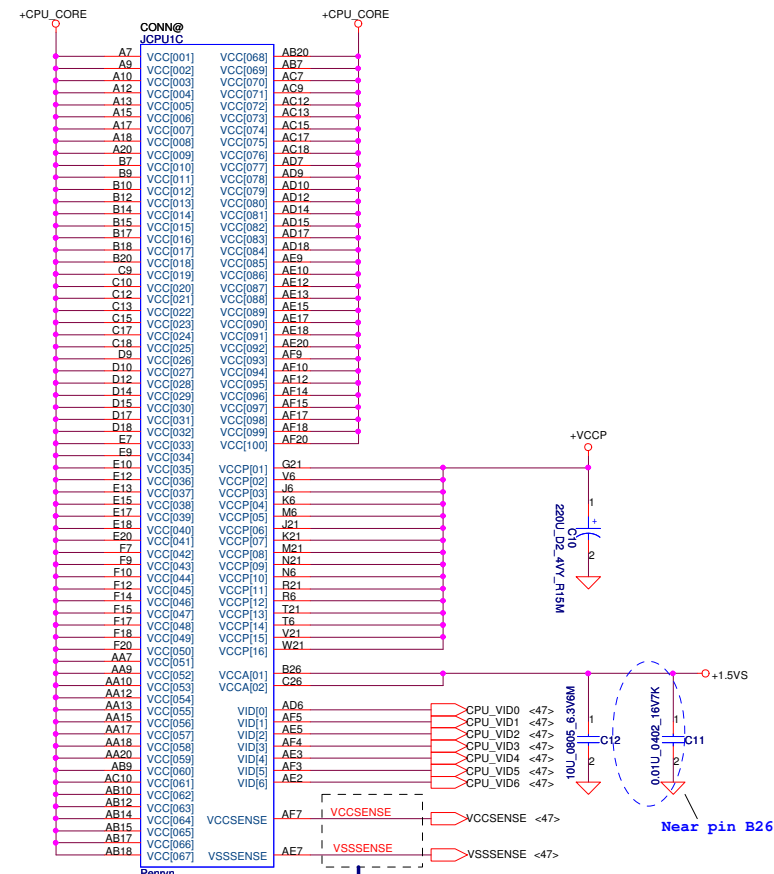
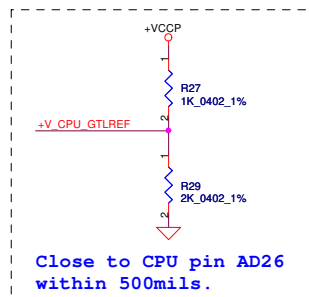
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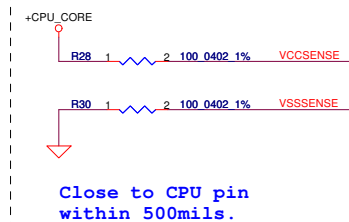
layout note: Rout H\_DPRSTP# from ICH9 to IMVP6 then to GMCH & CPU  
 layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPS

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within  
0.5" of CPU pin. Trace  
should be at least 25  
mils away from any other  
toggling signal.  
COMP[0,2] trace width is  
18 mils. COMP[1,3] trace  
width is 4



For 8 layer condition  
Length match within 25 mils.  $Z_0=27.4$  ohm  
The trace width/space/other is 20/7/25.

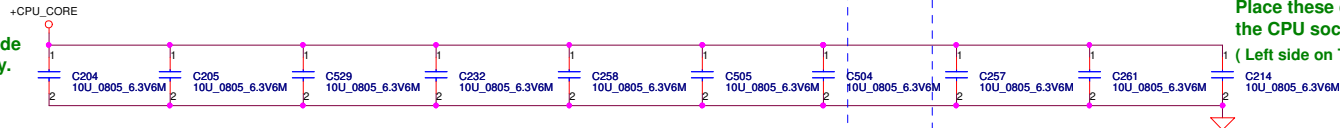


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# High Frequency Decoupling

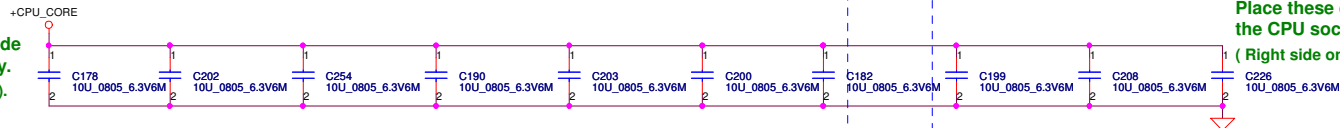
10uF 0805 X5R -> 85 degree.

Place these caps inside the CPU socket cavity. ( Left side on Top ).



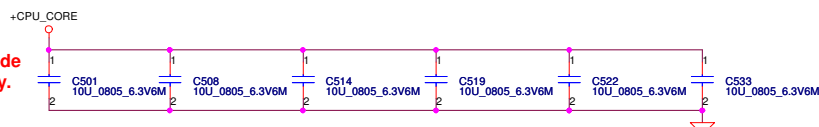
Place these caps inside the CPU socket. ( Left side on Top ).

Place these caps inside the CPU socket cavity. ( Right side on Top side ).

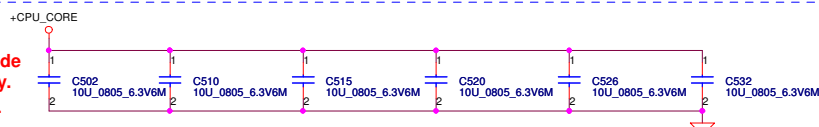


Place these caps inside the CPU socket. ( Right side on Top ).

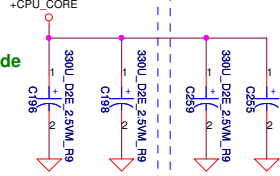
Place these caps inside the CPU socket cavity. ( Left side on Bottom ).



Place these caps inside the CPU socket cavity. ( Right side on Bottom ).

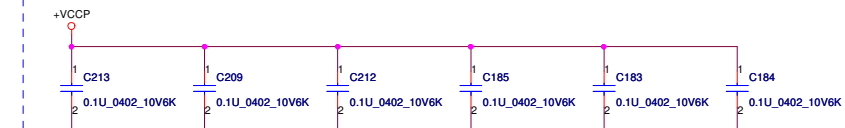


Place these caps inside the CPU socket. ( Left side on Top ).



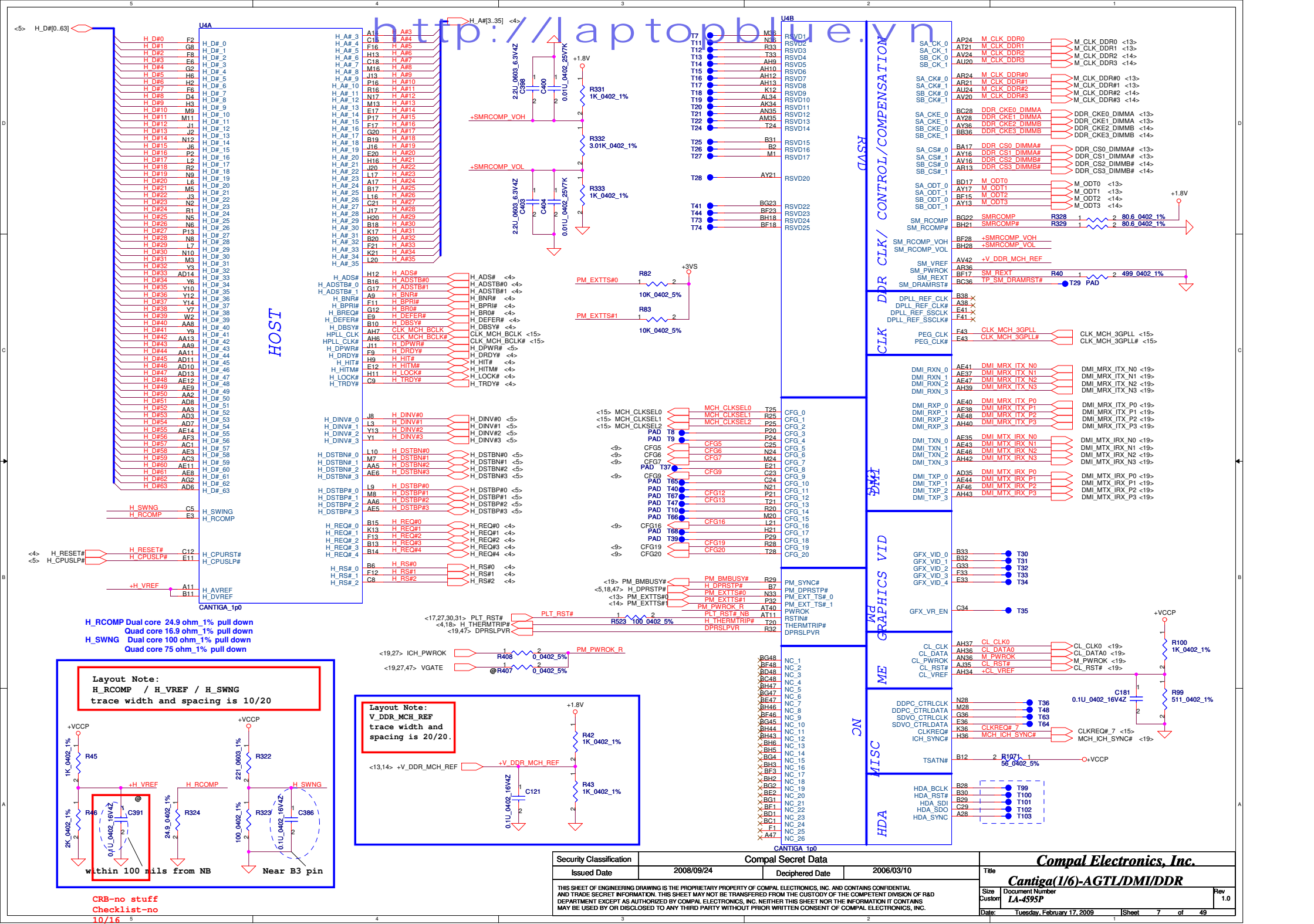
Place these caps inside the CPU socket. ( Right side on Top side ).

ESR <= 1.5m ohm  
Capacitor > 880 uF

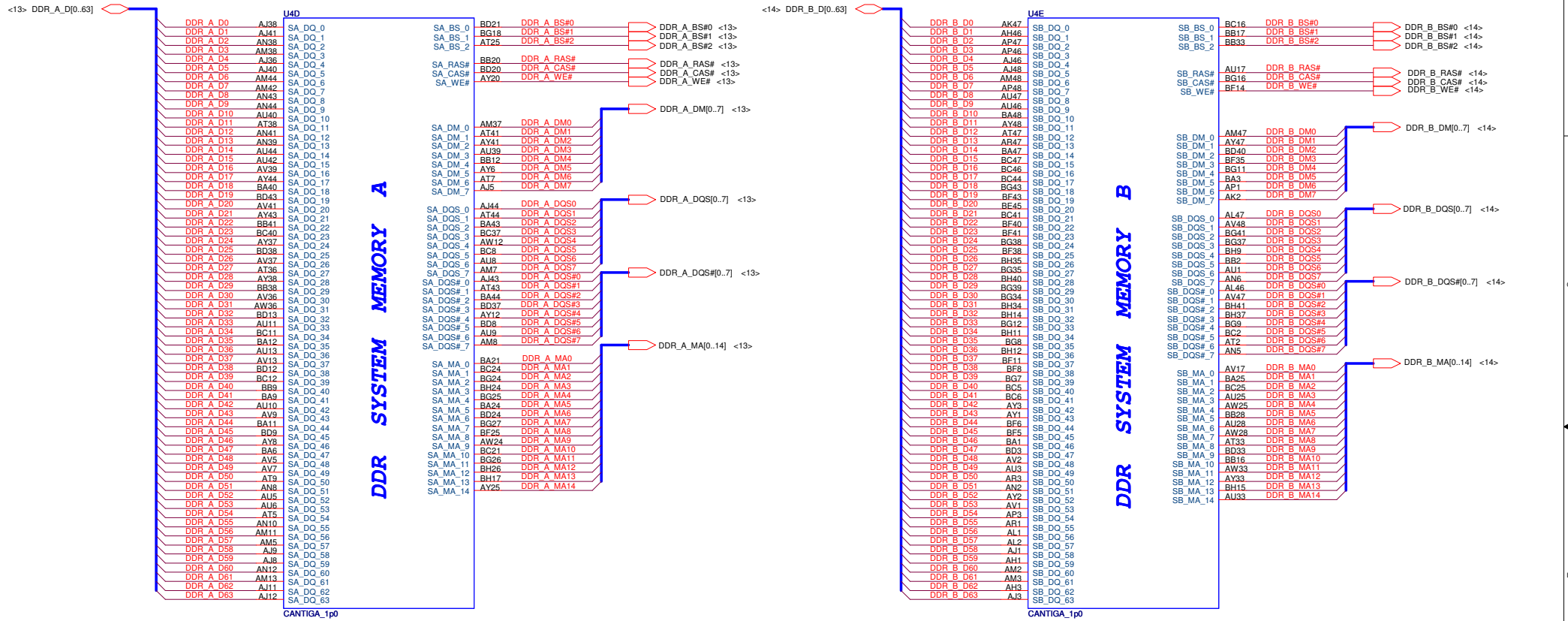


Place these inside socket cavity on L8 (North side Secondary)

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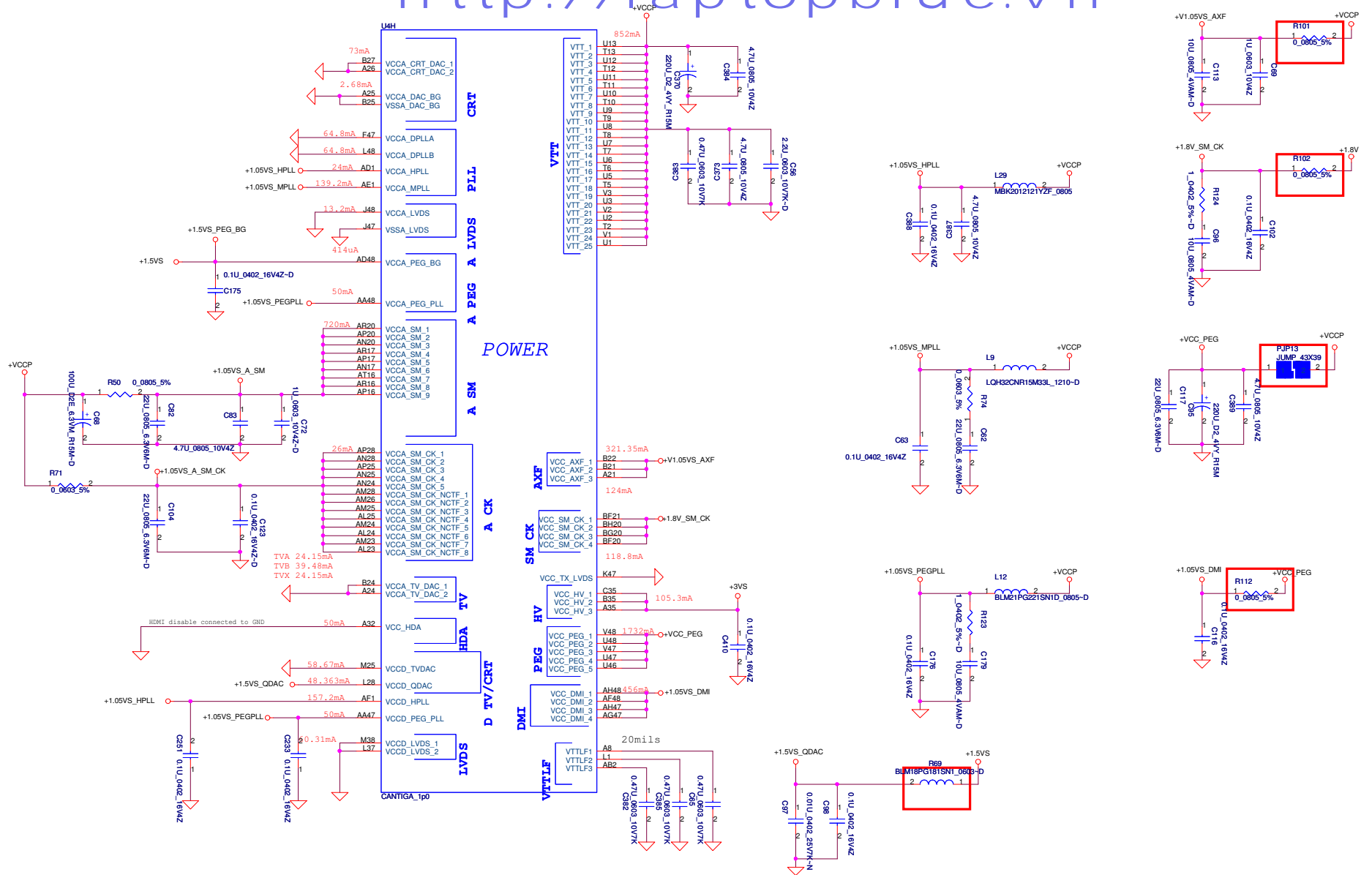




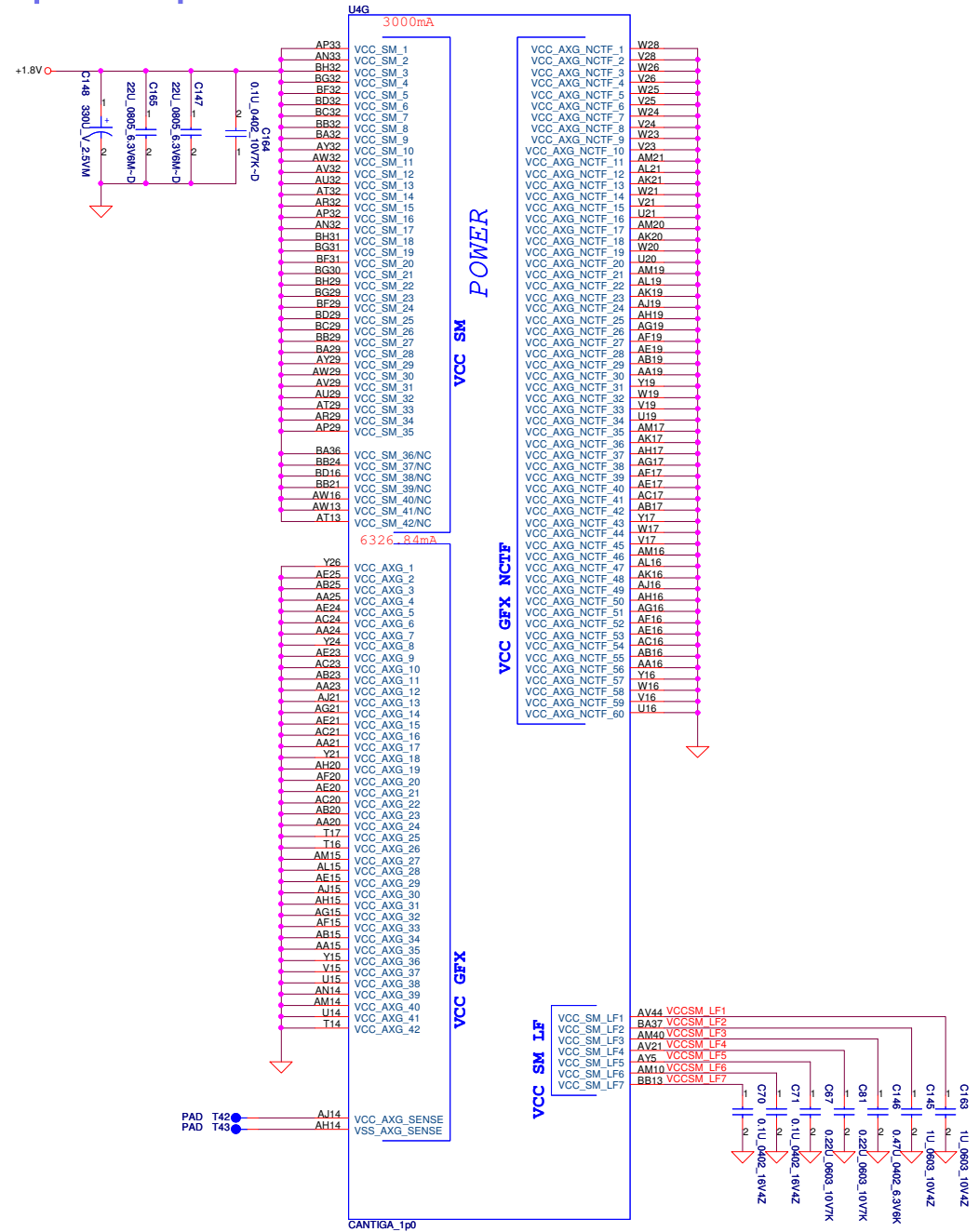
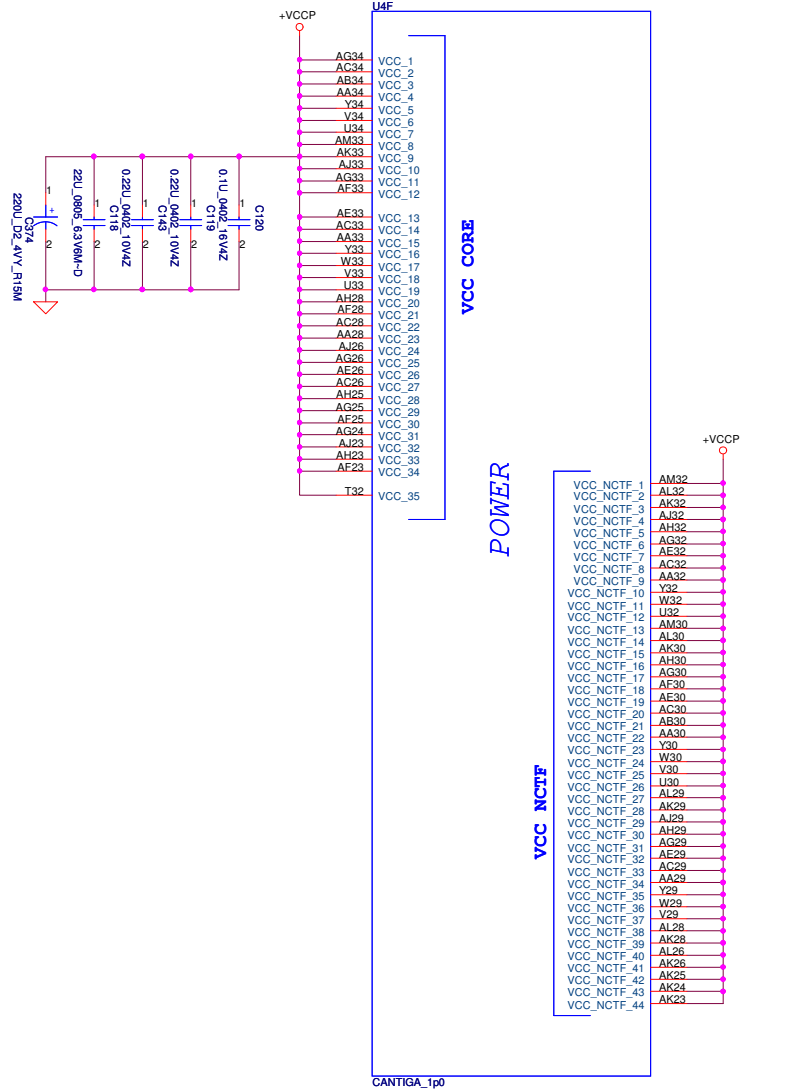




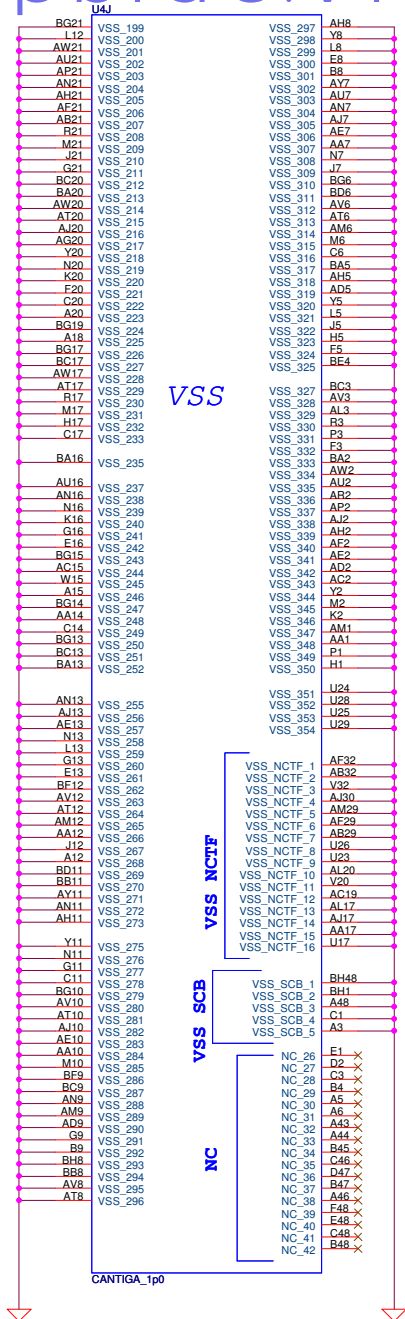
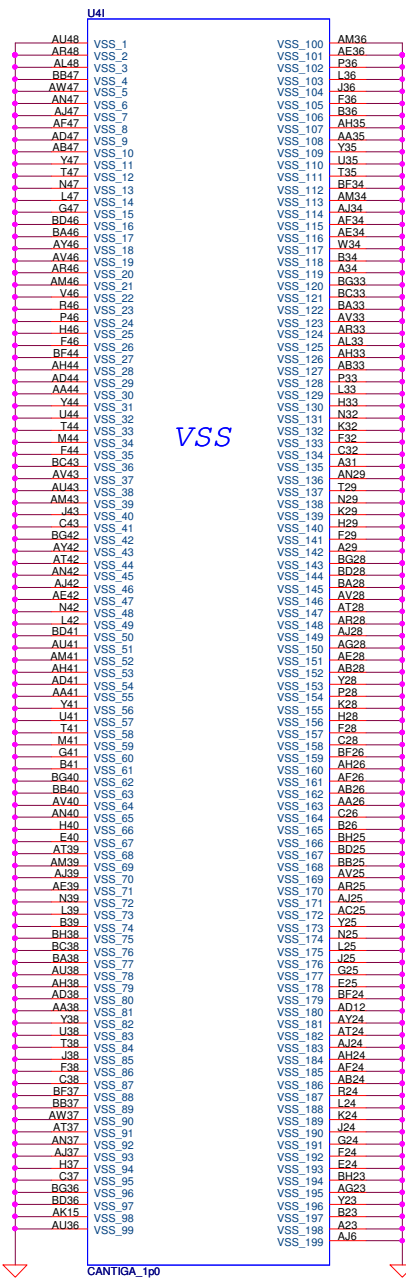




Extl Graphic: 1210.34mA  
integrated Graphic: 1930.4mA



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VSS

VSS NCTF

VSS SCB

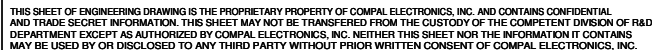
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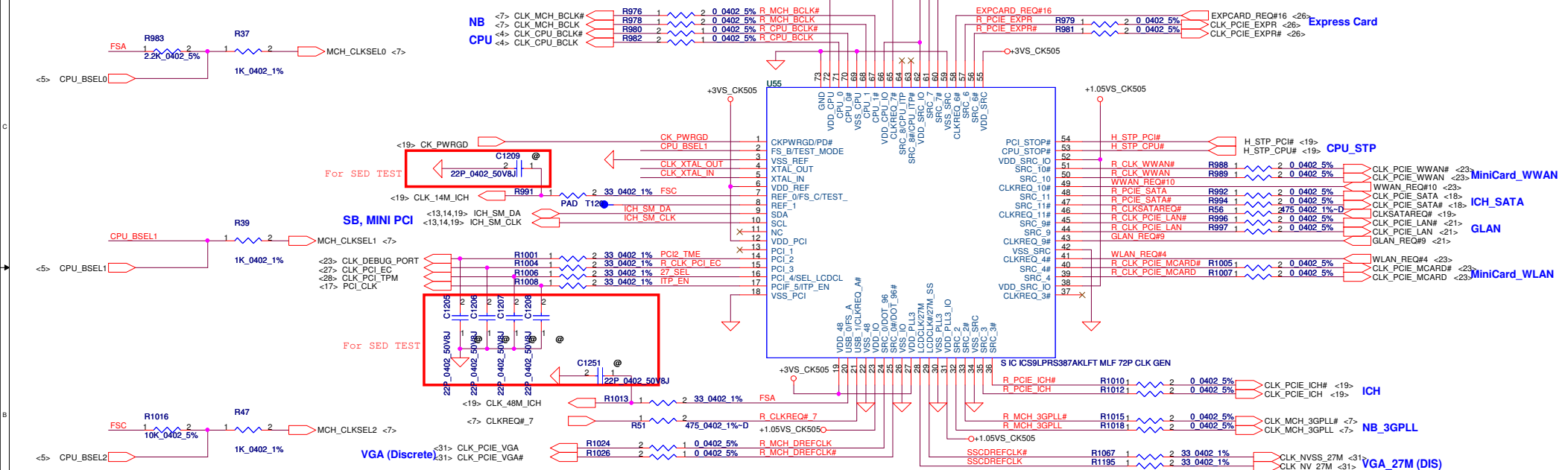
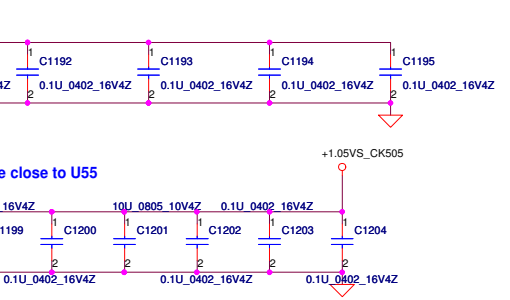
+1.8V

 +V\_DDR\_MCH\_REF <7,14>

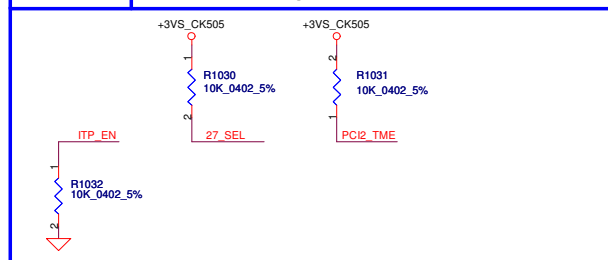
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ITP_EN	*0 = SRC8/SRC9# 1 = ITP/ITP#
27_SEL	0 = Enable DOT96 & SRC1 (UMA) *1 = Enable SRC0 & 27MHz (DIS)
PCI2_TME	0 = Overclocking of CPU and SRC Allowed *1 = Overclocking of CPU and SRC NOT allowed



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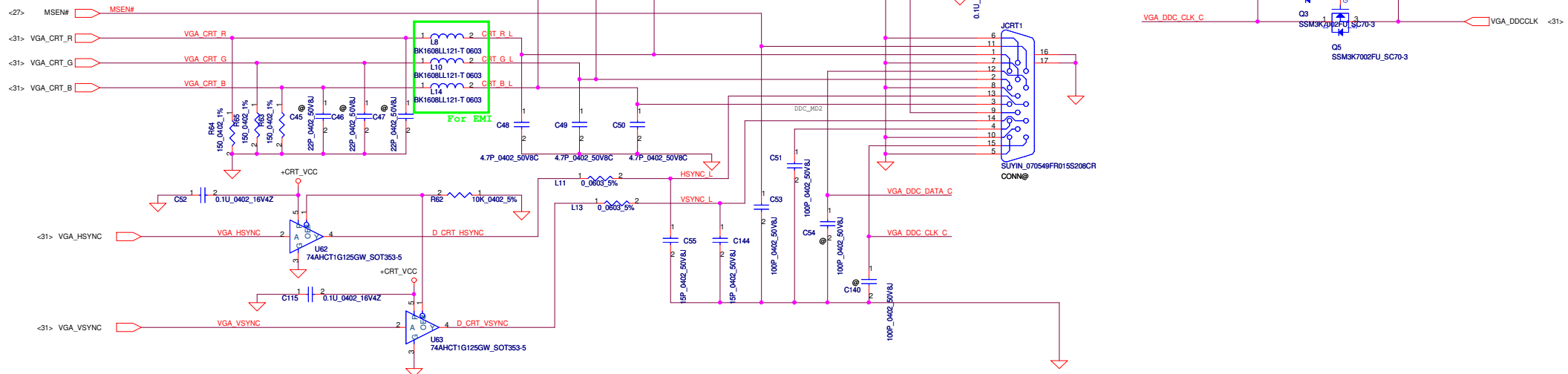


# CRT

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For Nvidia

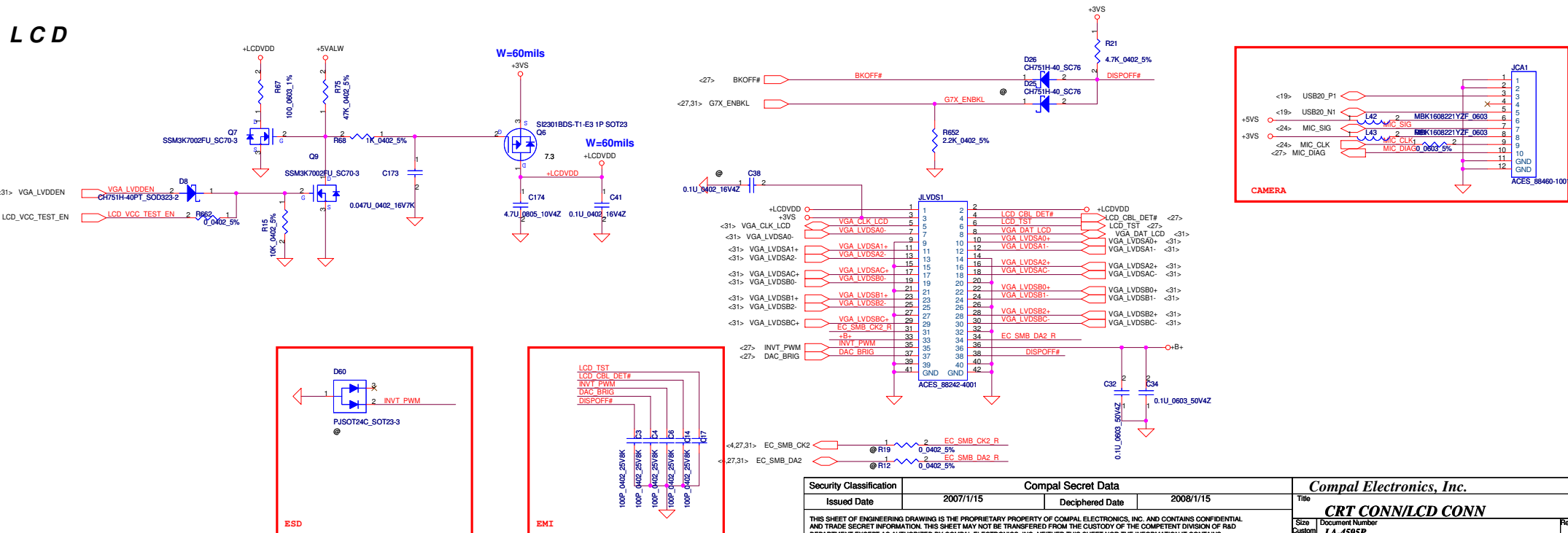
W=40mils



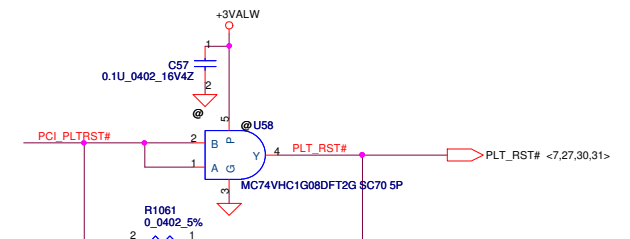
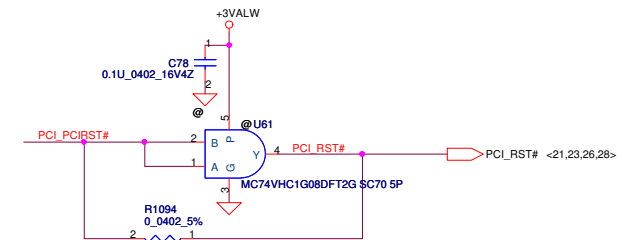
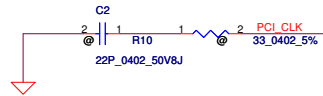
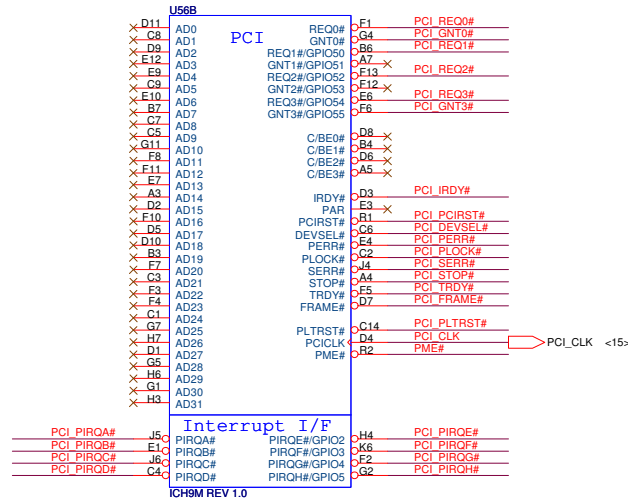
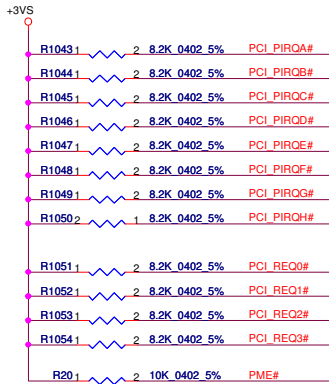
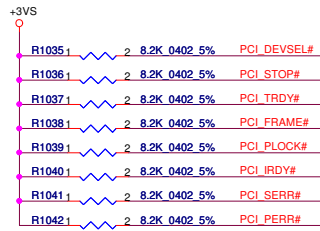
# LCD

W=60mils

W=60mils

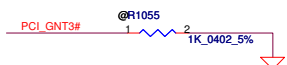


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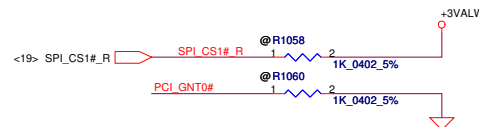
### A16 swap override Strap

Low= A16 swap override Enable  
High= Default \*

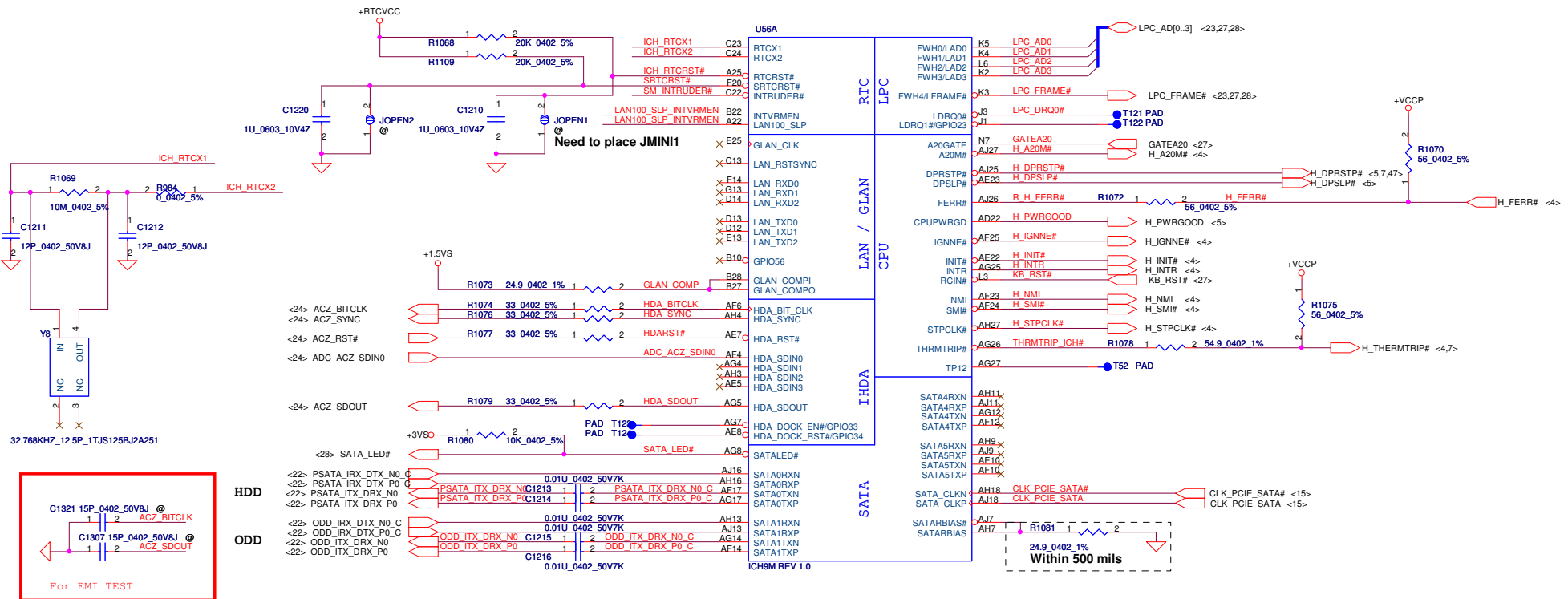
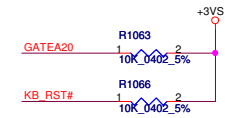


### Boot BIOS Strap

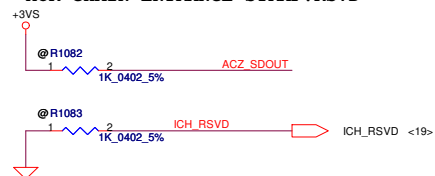
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



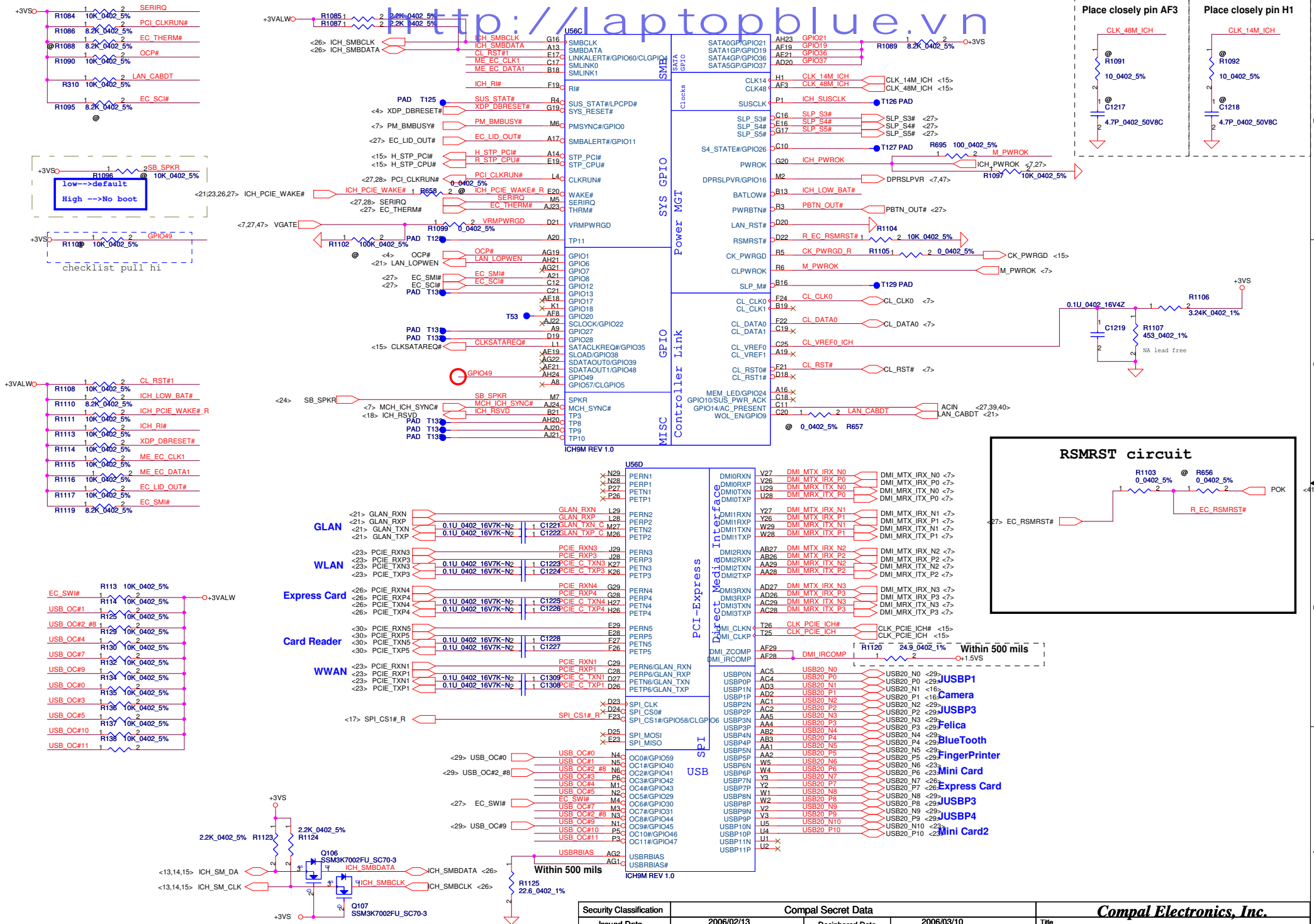
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XOR CHAIN ENTRANCE STRAP:RSVD

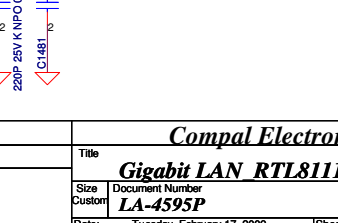
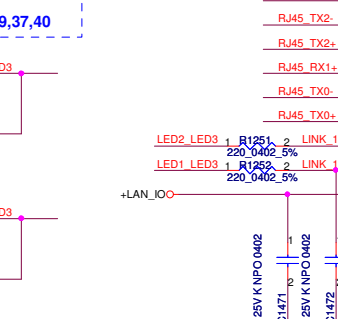
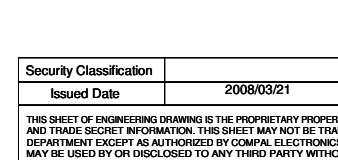
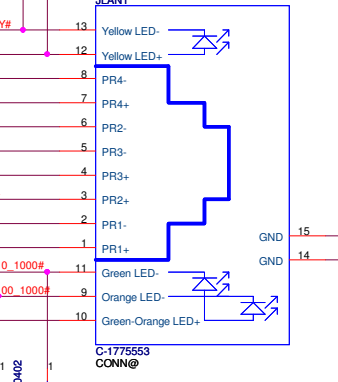
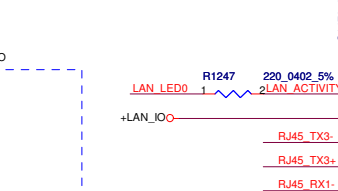
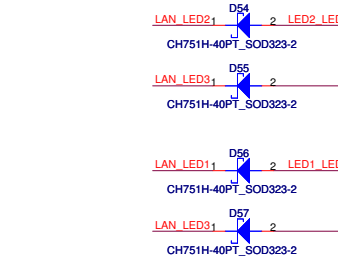
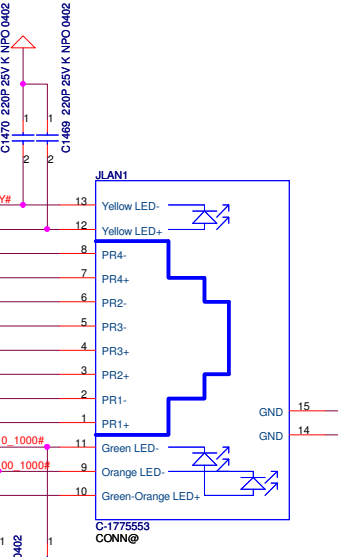
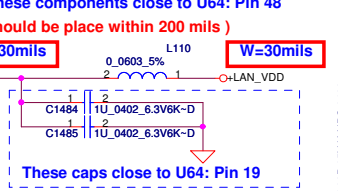
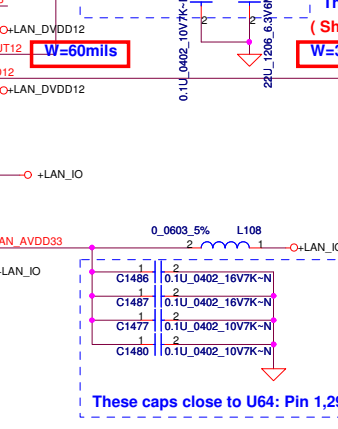
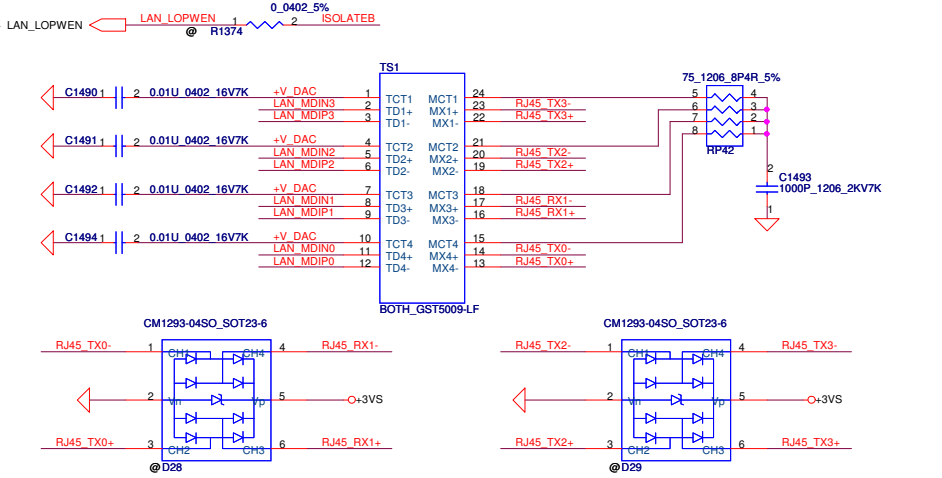
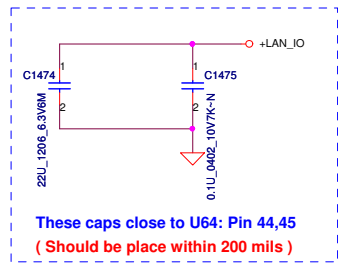
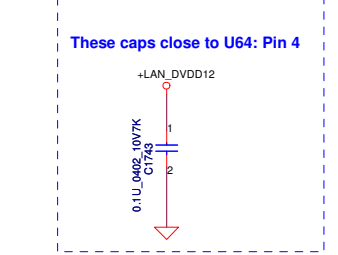
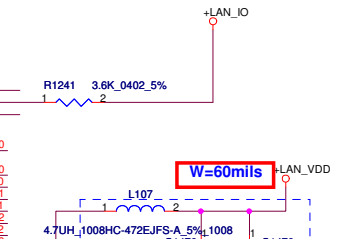
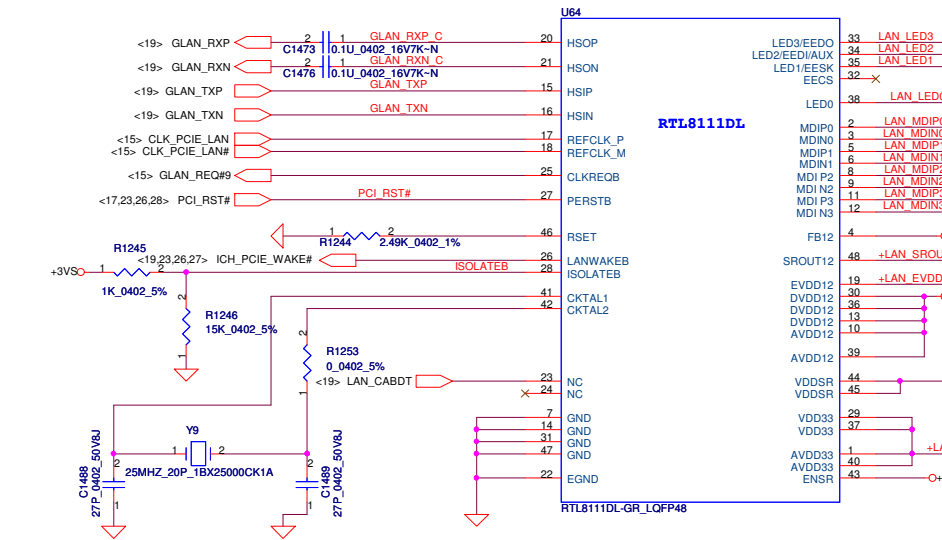
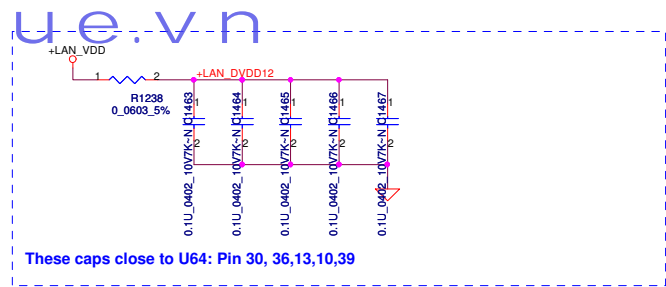
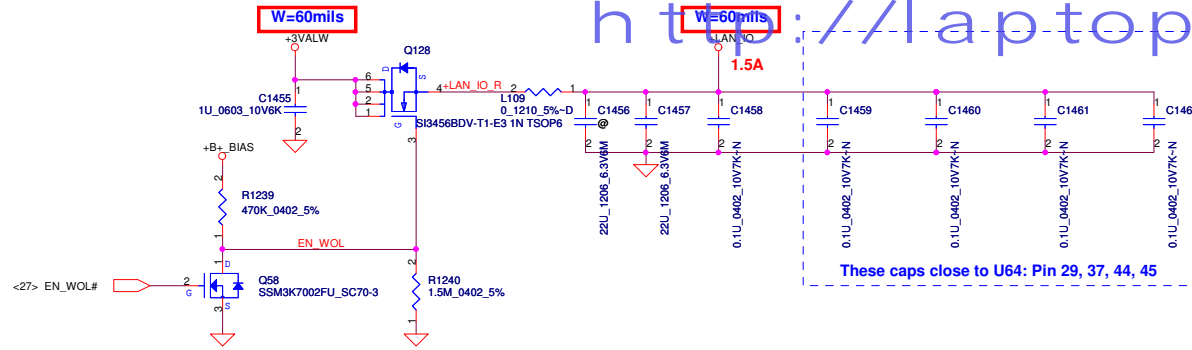


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				Custom	1.0
Date: Tuesday, February 17, 2009		Sheet 18 of 49			

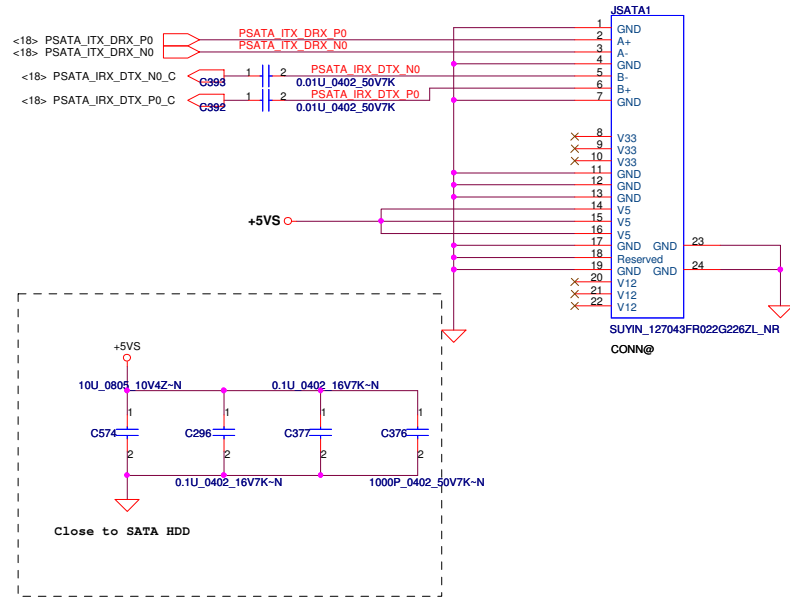


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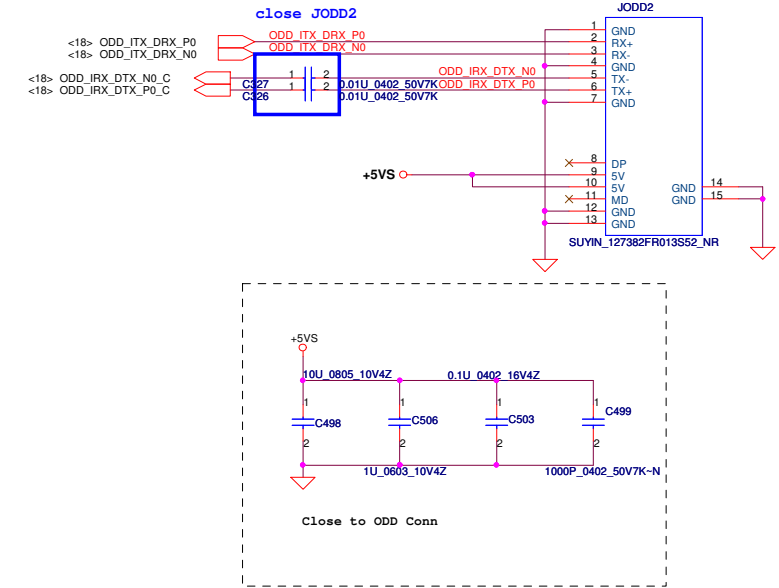
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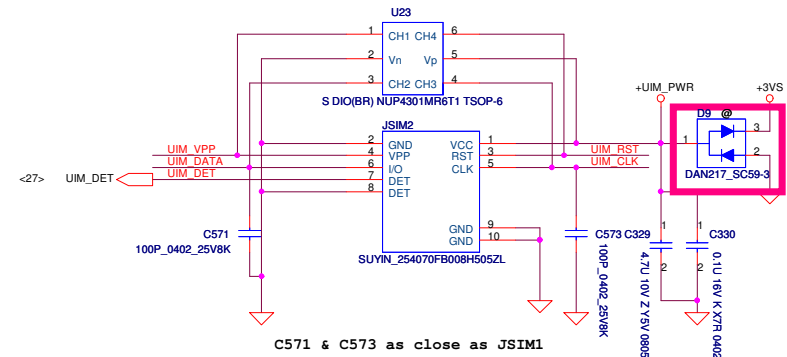
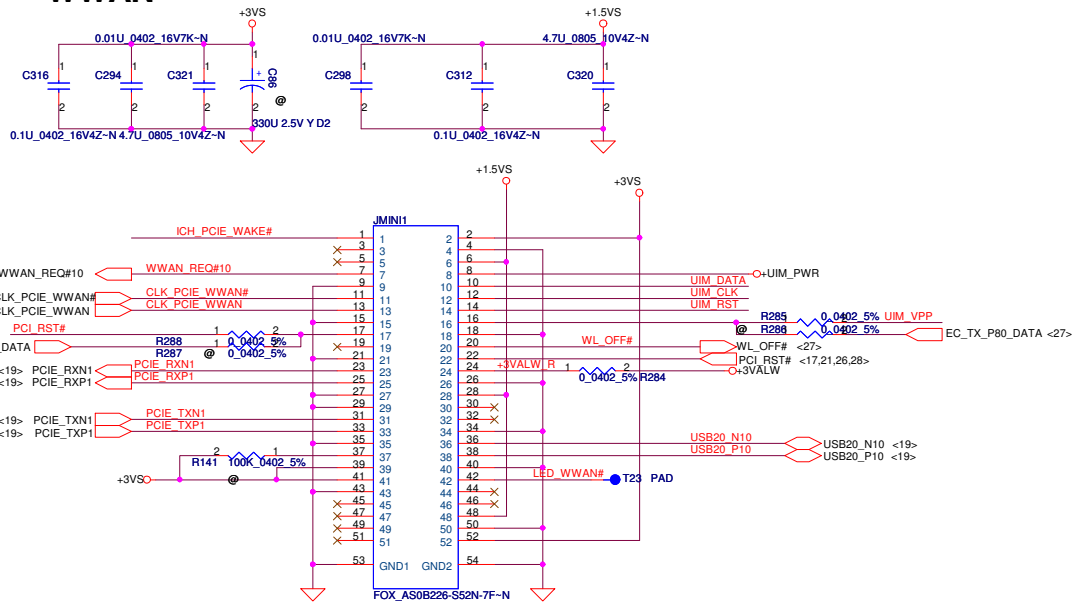


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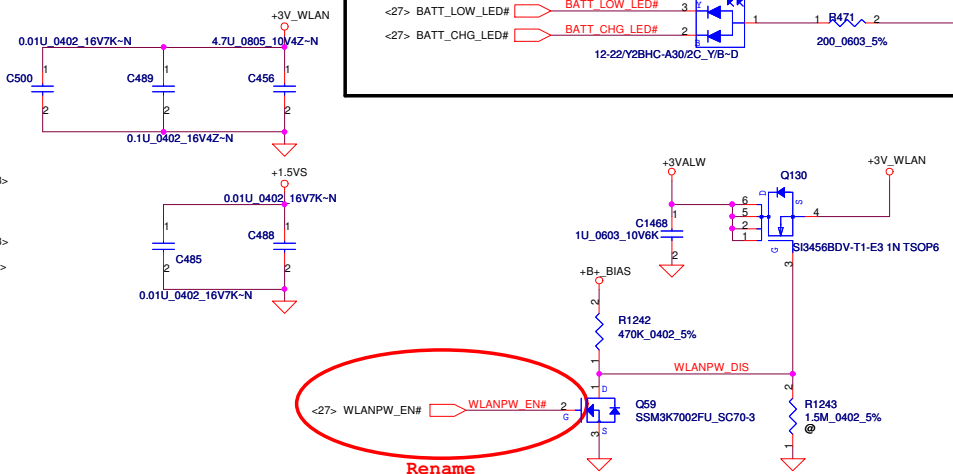
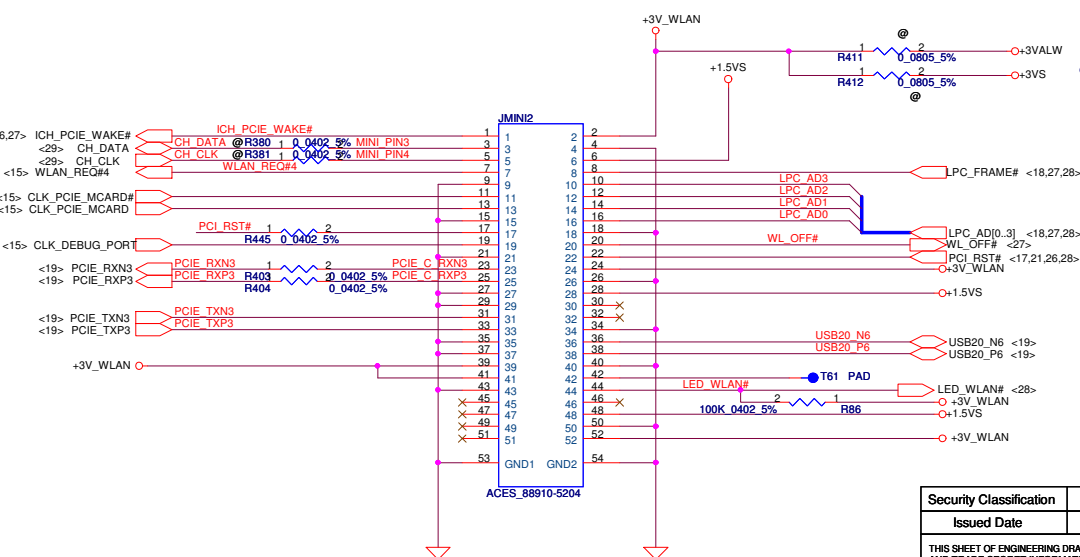
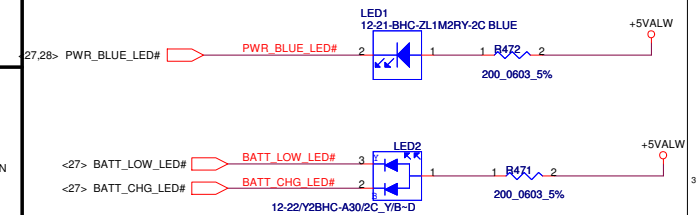


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				Date	Tuesday, February 17, 2009
				Sheet	22 of 49
				Rev	1.0

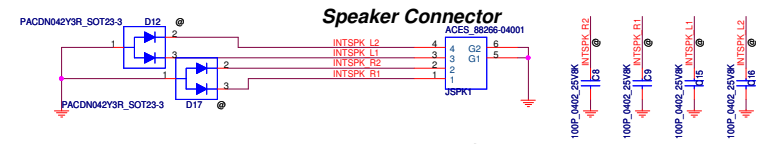


**WWAN**

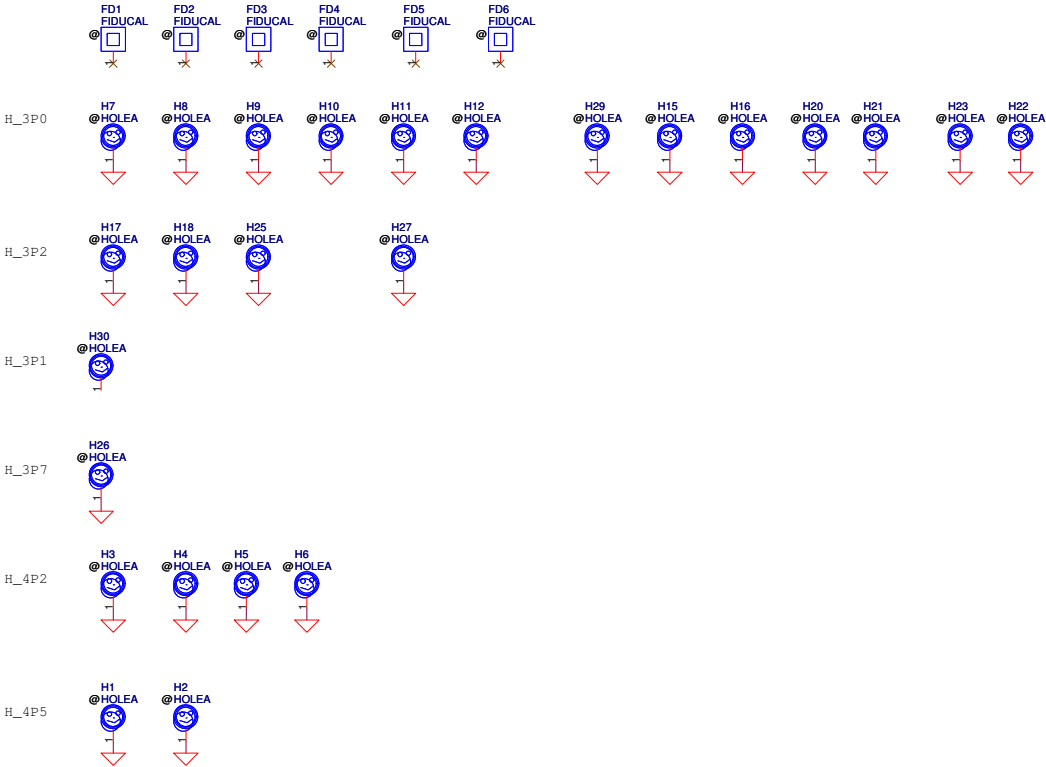
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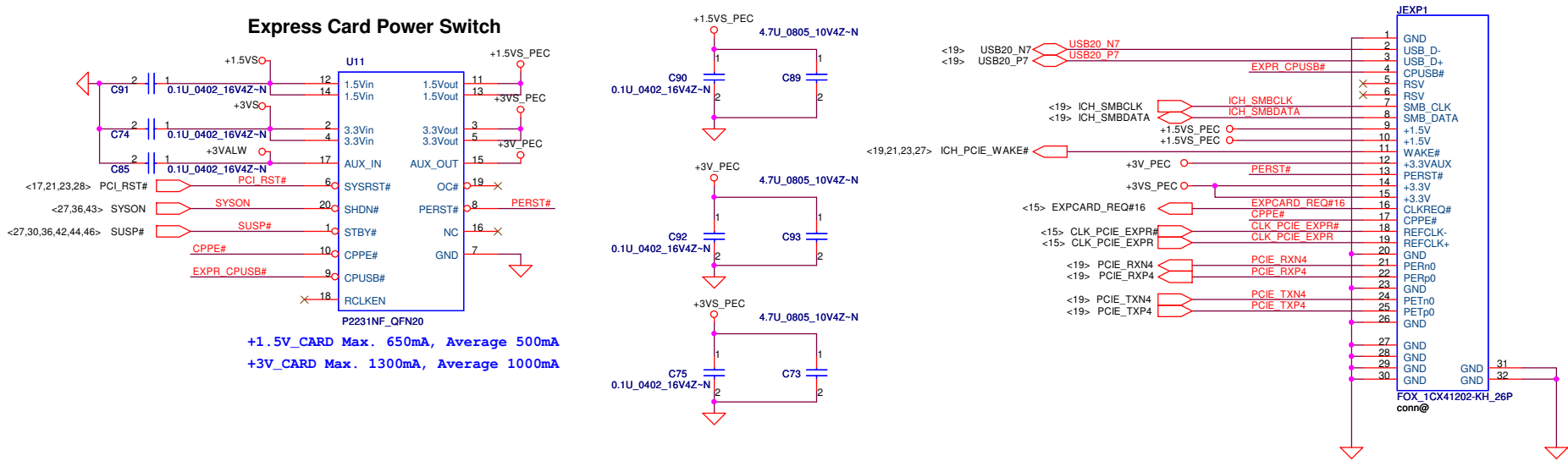


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Date:		Tuesday, February 17, 2009		Sheet	23 of 49

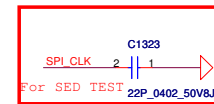


GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



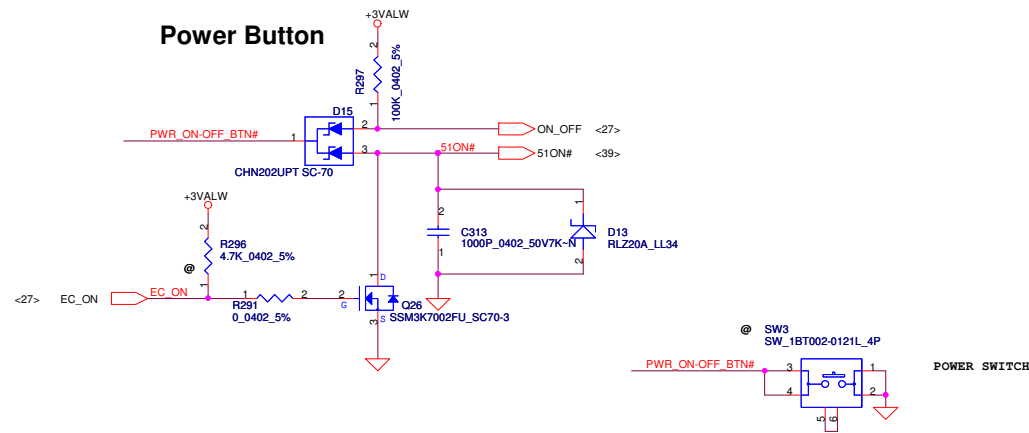
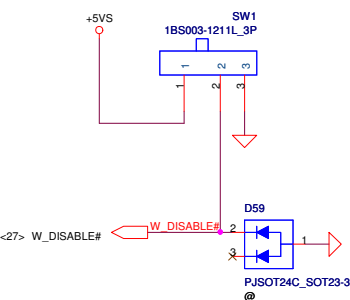


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				Date: Tuesday, February 17, 2009	Rev 1.0
				Sheet 26 of 49	

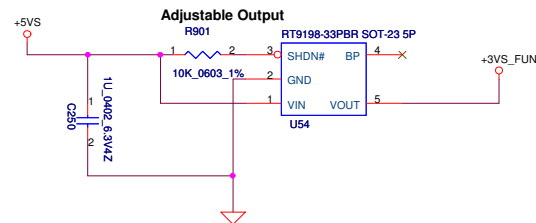


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						<b>BIOS &amp; EC I/O Port</b>		
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							LA-4595P	1.0
Date:				Tuesday, February 17, 2009	Sheet	27 of 49		

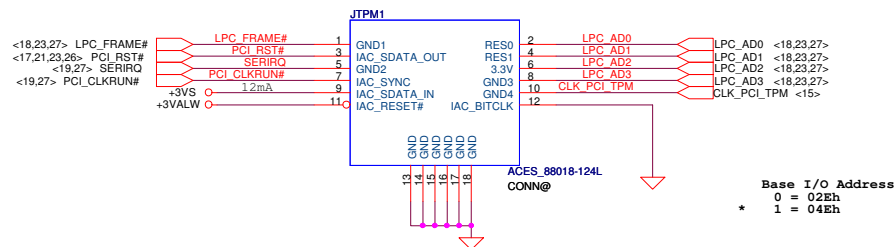
## Power Button

**Wireless\_BTN**

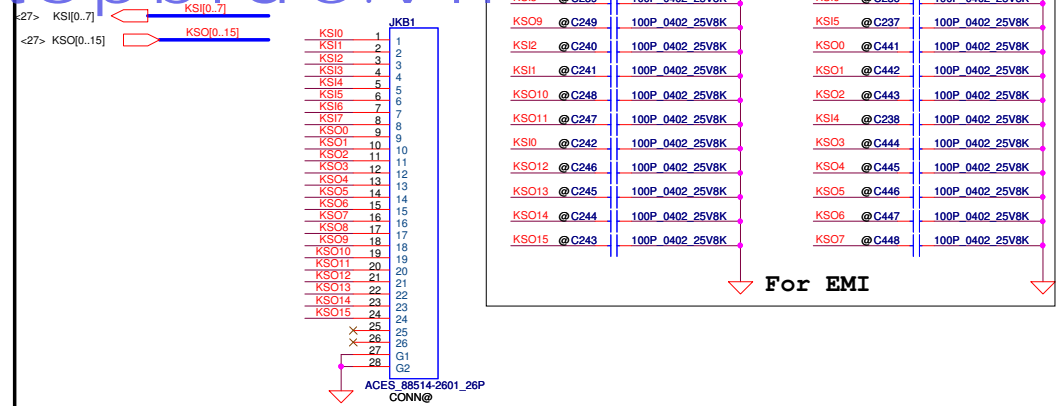
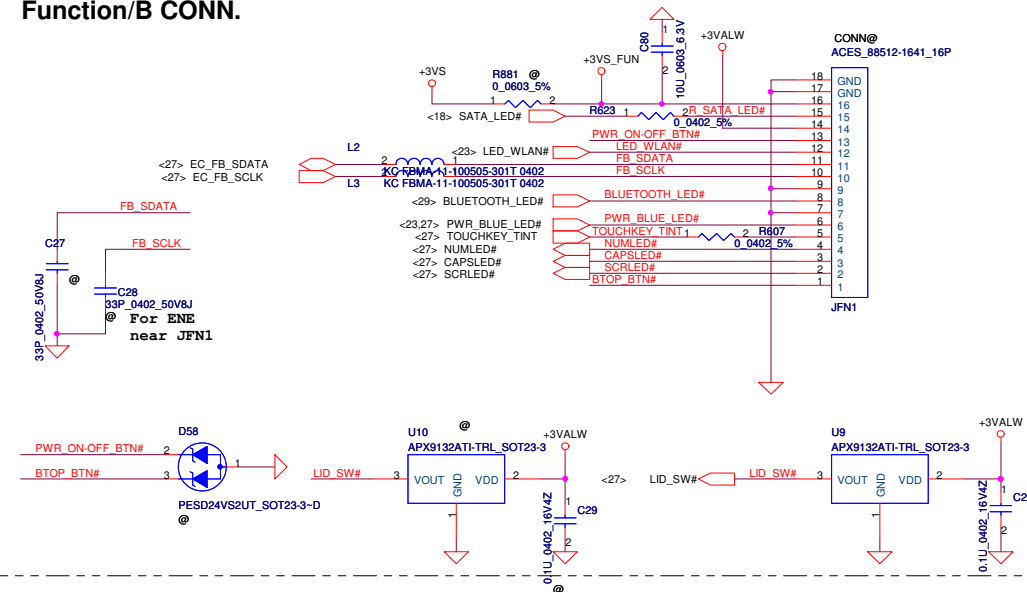
### Regulator for ENE sensor



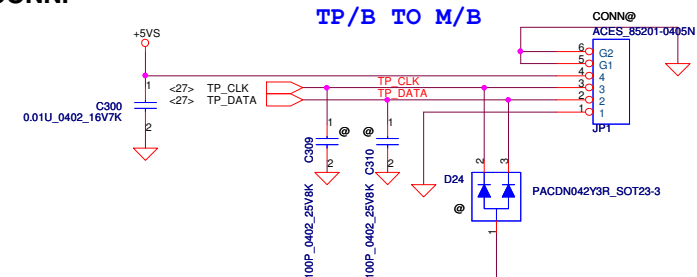
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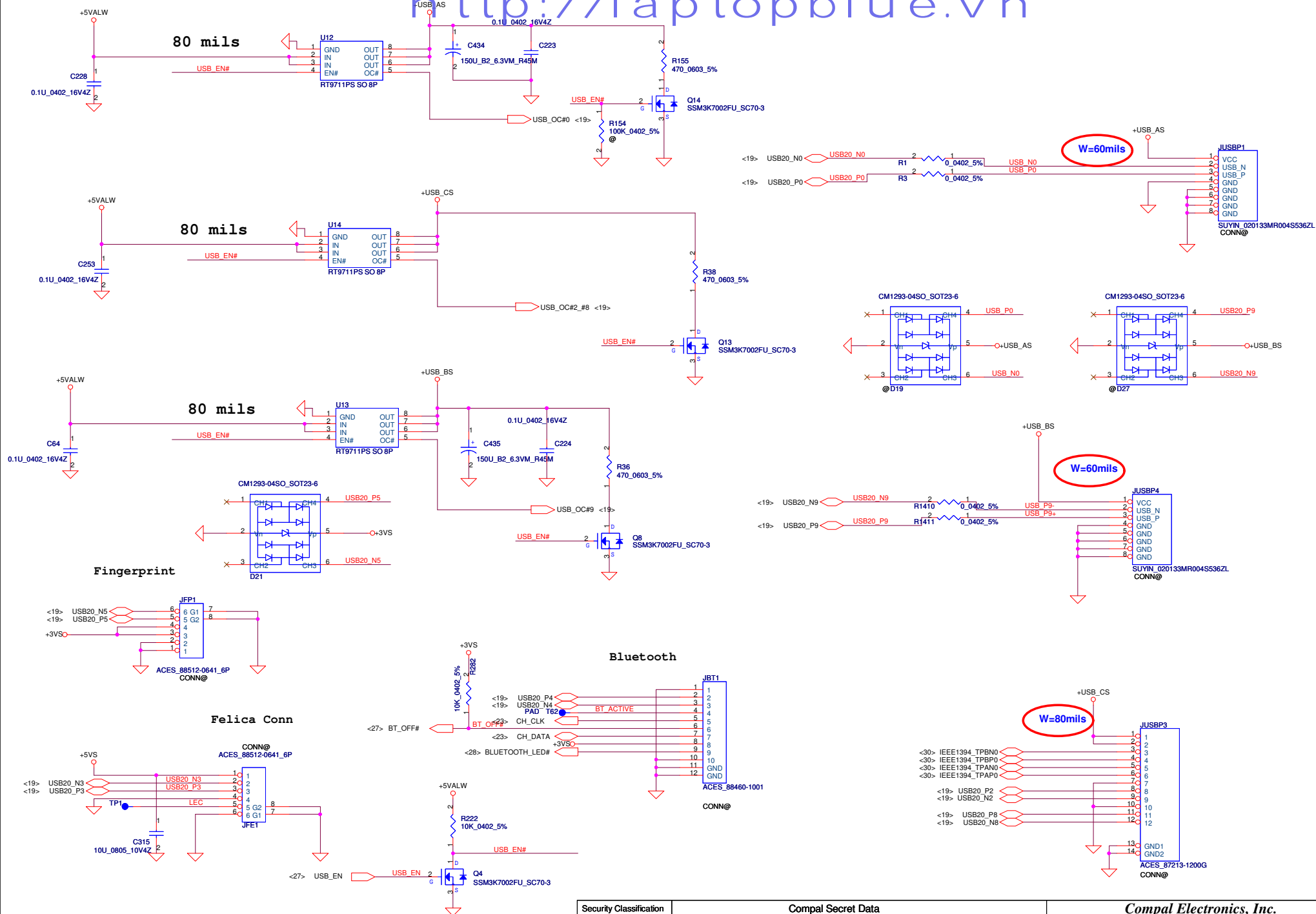
## INT\_KBD\_CONN.

**Function/B CONN.**

**Touch PAD/B CONN.**



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				Custom	LA-495P	1.0
				Date:	Tuesday, February 17, 2009	Sheet 28 of 49



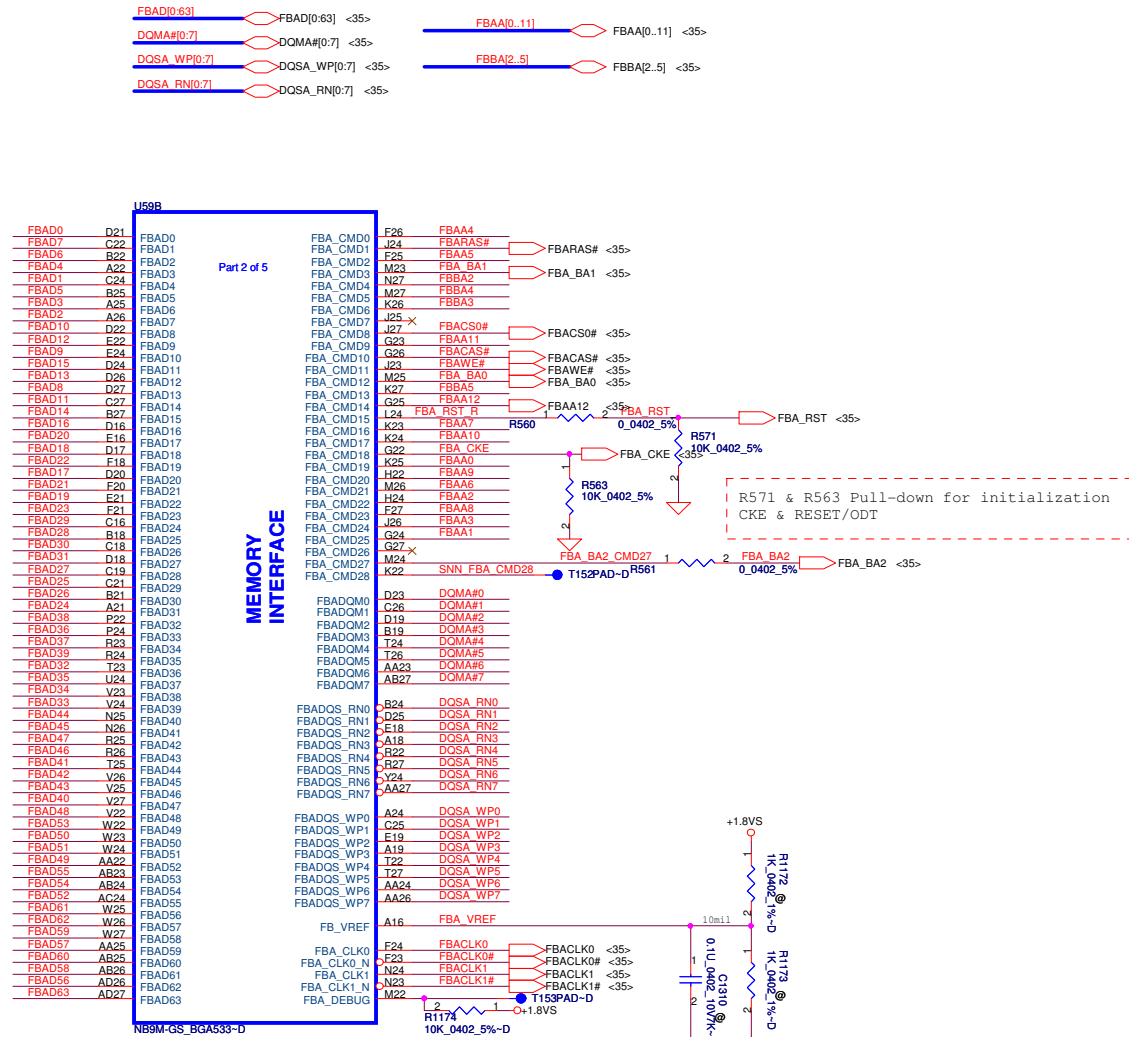
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Security Classification	Compal Secret Data			<div> <div>Title</div> <div>OZ888G\$0L1N Media Card/1394</div> </div>		
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					LA-4595P	1.0
				Date:	Tuesday, February 17, 2009	Sheet 30 of 49





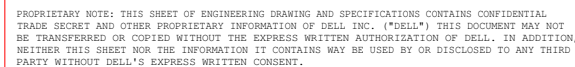
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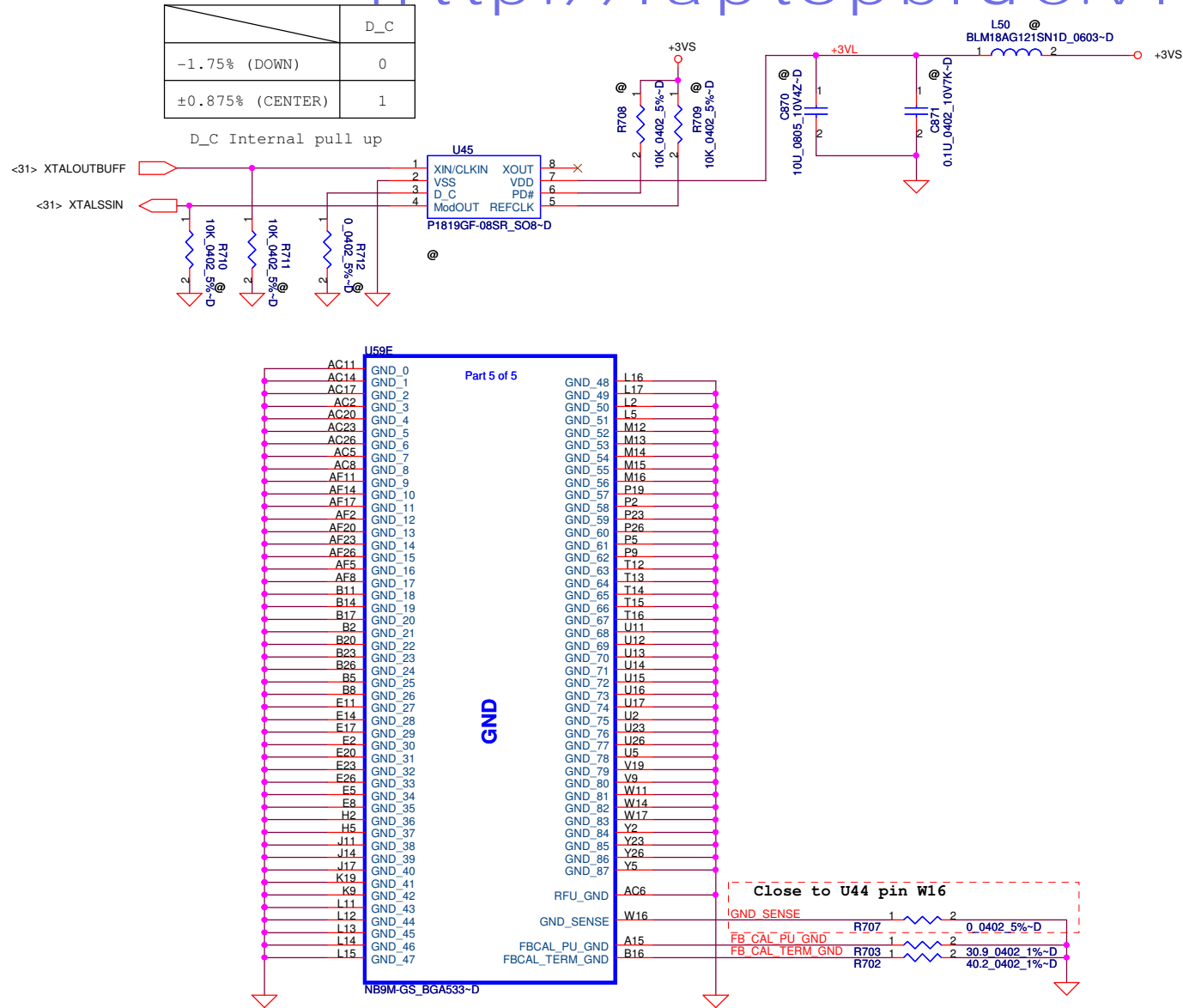


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Title		NVG98 Memory Interface	
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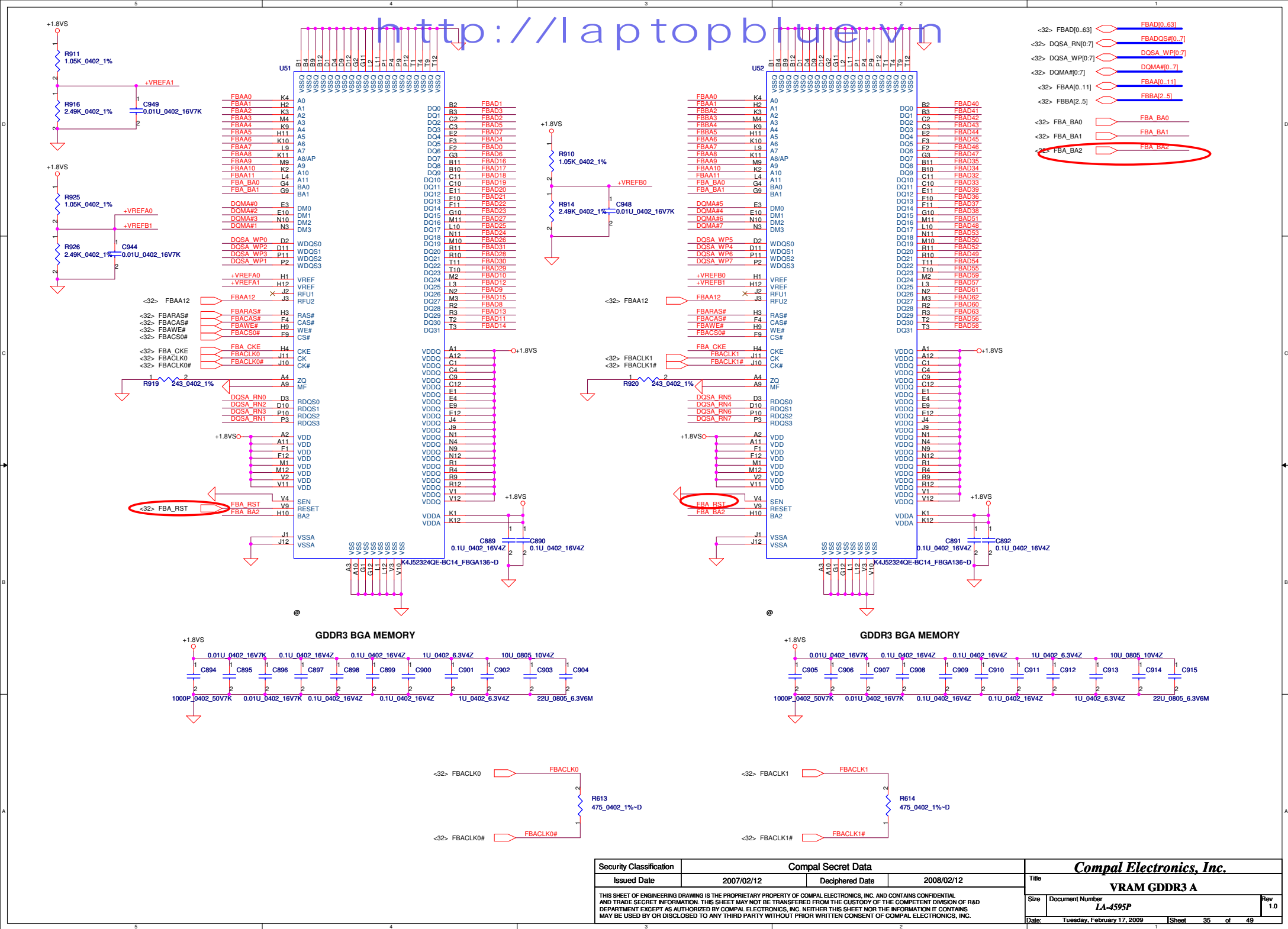
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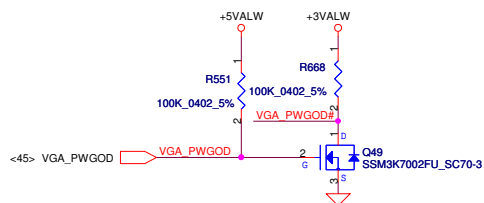
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Size	Document Number		Rev
	LA-4595P		1.0
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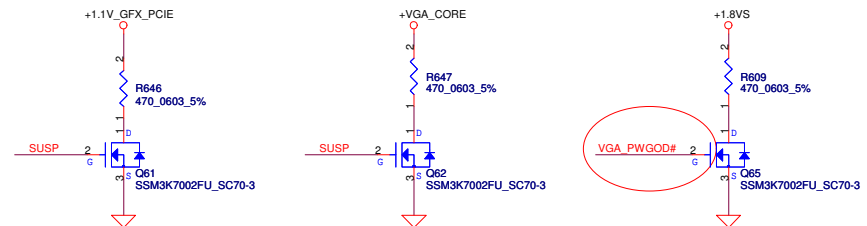
# +5VALW to -5V/S Transfer

The diagram illustrates a circuit for transferring the +5VALW signal to the -5V/S output. A MOSFET (U39, SI4800DY\_S08) is used as a switch. The gate is driven by a +5V\_GATE signal through a 47K resistor (R207) and a 0.01uF capacitor (C279). The drain is connected to the +5VALW input through a 10uF capacitor (C278). The source is connected to the -5V/S output through a 10uF capacitor (C284) and a 0.01uF capacitor (C283). The MOSFET's body is connected to ground. The output is labeled -5V/S.

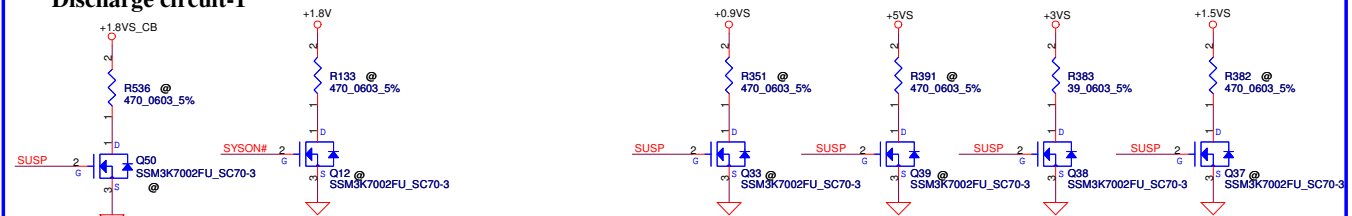
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SYSON -&gt; SUSP# -&gt; VGA\_ON-&gt;VGA\_PWGOD

### VGA Discharge circuit



### Discharge circuit-1

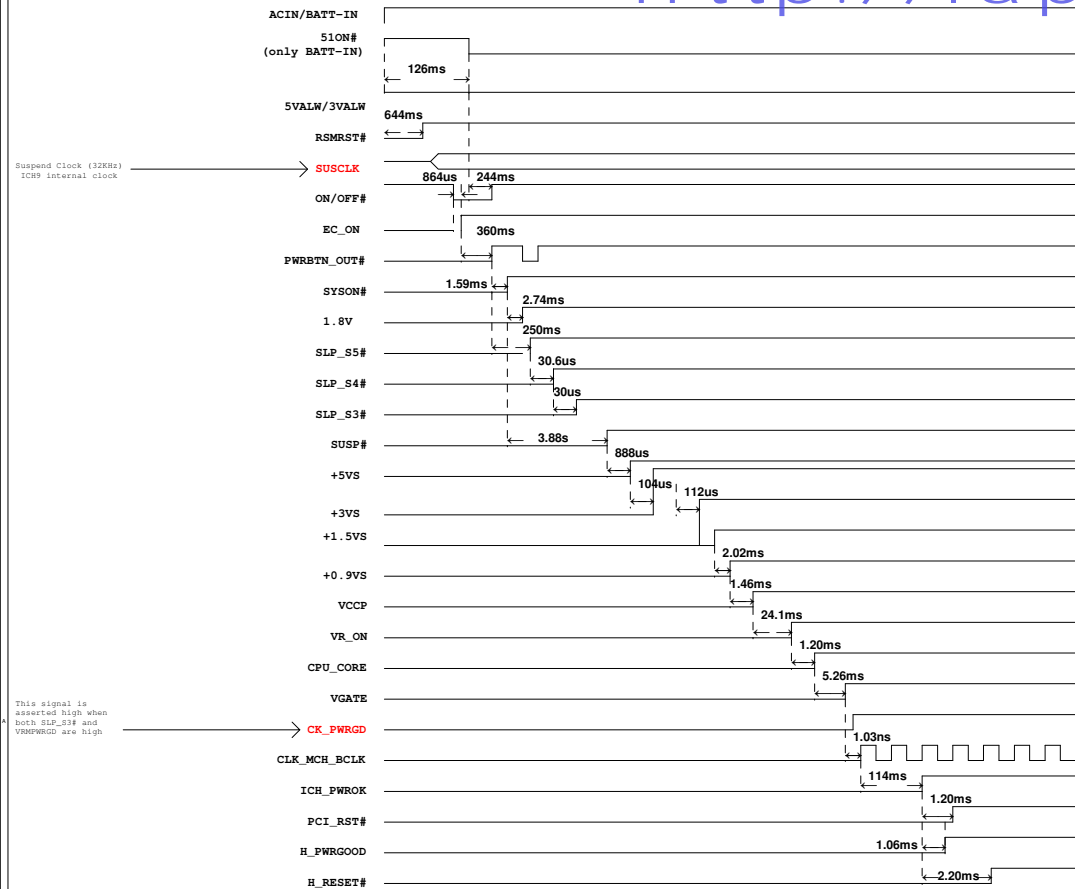


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						Size Custom	Document Number LA-4595P	Rev 1.0
						Date: Tuesday, February 17, 2009		Sheet 36 of 49



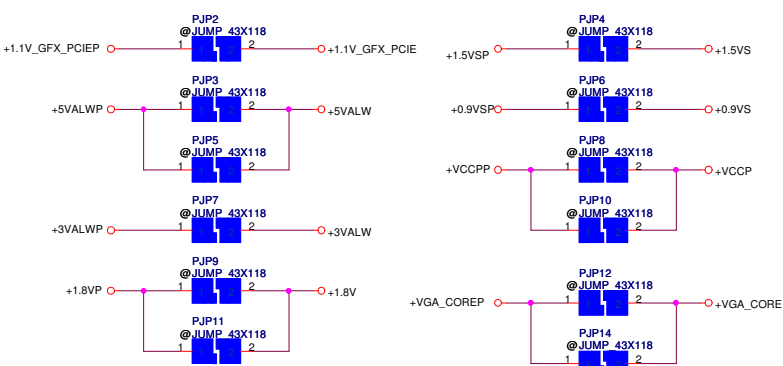
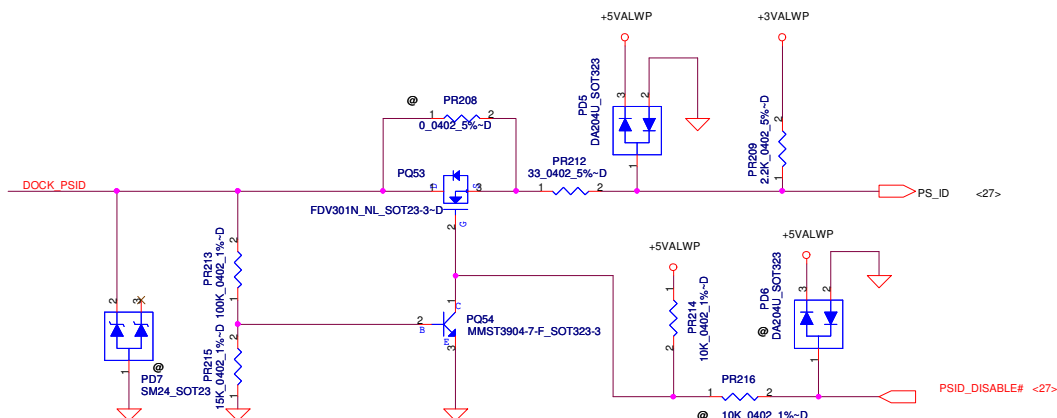
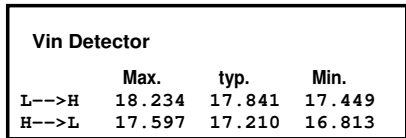
# KAL80 POWER UP SEQUENCE

http://laptopblue.vn

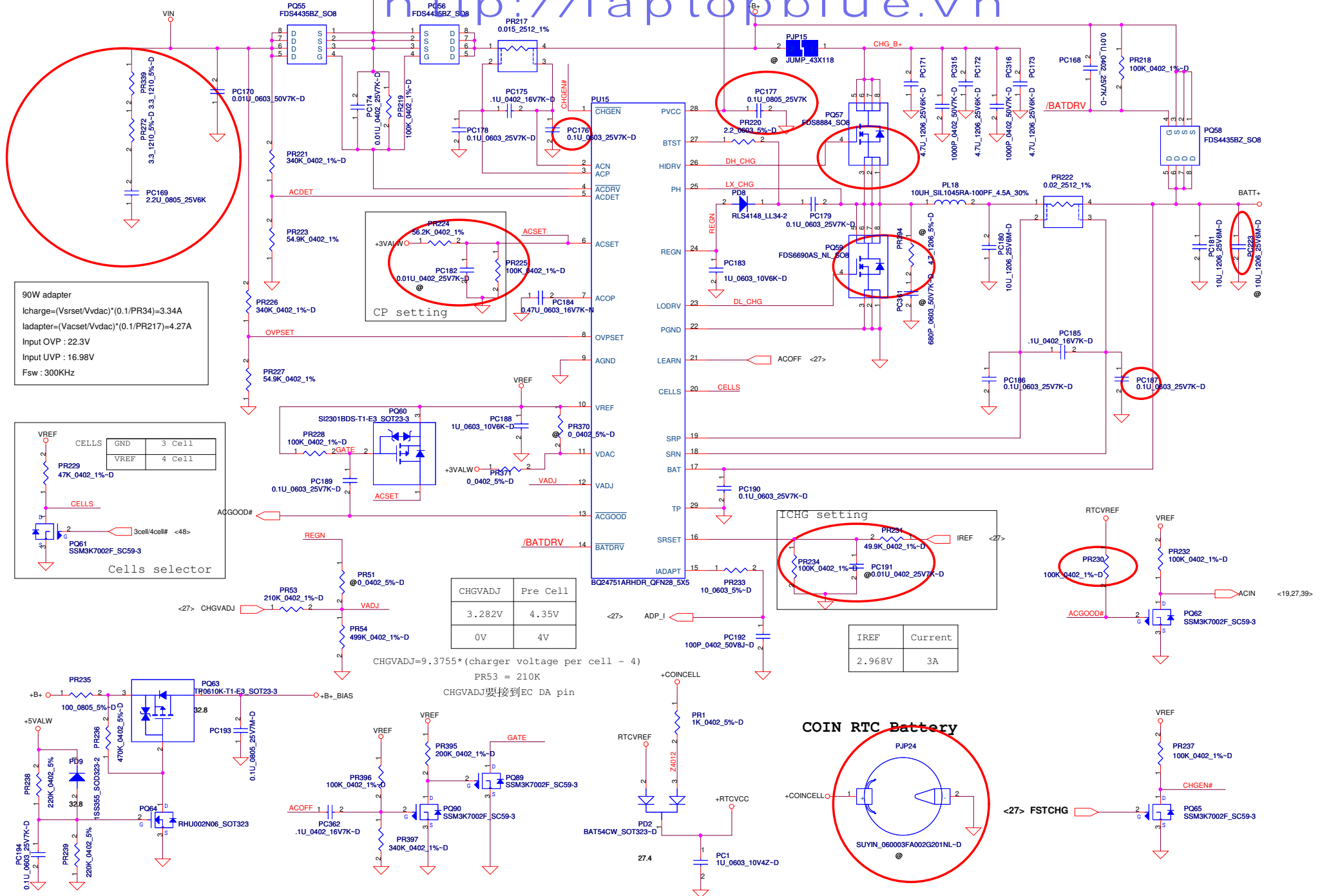


Version Change List ( P. I. R. List ) <span>Page 1/1</span>						
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description <span>Rev.</span>
1		Swap SW1	12/02	EE		
2		Update JUSBP3 pin define	12/02	EE		
3		R405 POP	12/02	EE		
4		U50 unPOP & R1190 POP	12/02	EE		
5		WWAN move to PORT6	12/02	BIOS		
6		Add C1391 & C1392	12/02	NVidia	LVDS single channel issue	Short U59.V2 & U59.V3. Add C1391 C1392 for IFPB_IOVDD
7		Swap JSPK1 Pin	12/02	EE		
8		R101	12/04	EE	Change to 0805	
9		TPM Con	12/04	EE	Modify to Con	
10		R76 & R78 UnPOP	12/09	EE	EC update to Rev:C1	
11		Q7 & Q9	12/09	EE	Update Q7 & 9 footprint	
12		R658 & R281	12/11	EE	R685 UnPOP & R281 UnPOP for wake on LAN	
13		U89 & WLANPW_DIS#	12/11	EE	Add U89 for wake on LAN. Add WLANPW_DIS# of EC	
14		C1484 & C1485	12/11	EE	C1484 & C1485 modify to 1U form LAN vendor	
15		Update PW schematic	12/12	PW		
16		C260 & C252	12/15	EE	IDT ask UnPop	
17		Add D29 D28	12/15	ESD	ESD for LAN	
18		U9 Pop & U10 UnPop	12/15	ME		
19		Wake On WLAN	12/16	EE	Modify WLANPW_DIS# circuit	
20		Add T49 & T53	12/16	Layout		
21		C696	12/16	EE	Update PN	
22		WLANPW_DIS#	12/17	EE	Move WLANPW_DIS# to EC-GPIO40 and Del BTOP_ON	
23		L42 & L43	12/17	EMI	L42 & L43 update to Bead from 0 ohm	
24		C3 C4 C6 C14 C17	12/17	EMI	POP 100 P	
25		R69	12/17	EE	Update to Bead drom 100 ohm	
26		Cap	12/17	EMI	Add C1469 C1470 C1471 C1472 C1481 R81	
27		D21 D12 D17	12/17	ESD	ESD ask POP	
28		Update PW schematic	12/17	PW		
29		Update Q128 Q130 PN	12/18	EE		
30		Update Board ID	12/18	EE	R231	
31		Add U16 for OZ888	12/18	EE		
32		C1323 POP	12/18	EE	For Kepar	
33		R1421 UnPOP	12/22	EE		
34		C292 C297	12/22	EE	Modify to 22P form 18P (Crystal Vendor)	
35		C1745 C1749	12/22	EE	Modify to 18P form 10P(C1749) and 15P from 10P(C1745) (Crystal Vendor)	
36		C1211	12/22	EE	Modify to 12P form 15P (Crystal Vendor)	
37		R1423 & R1422	01/07	EE	Add for O2	
38		L6 & R1190	01/10	EE	Change to 0805	
39		Modify LDO to +5VS	01/12	EE		
40		Add C80 & D59 & D60	01/12	EE		
41		Add components of JHP1	01/13	EE	For vendor	
42		R360 & R361	01/19	EE	Update R360 & R361 to 56 ohm	
43		U37	01/19	EE	Update U37 to SA00001KN10	
44		R231	01/19	EE	Update Board ID	

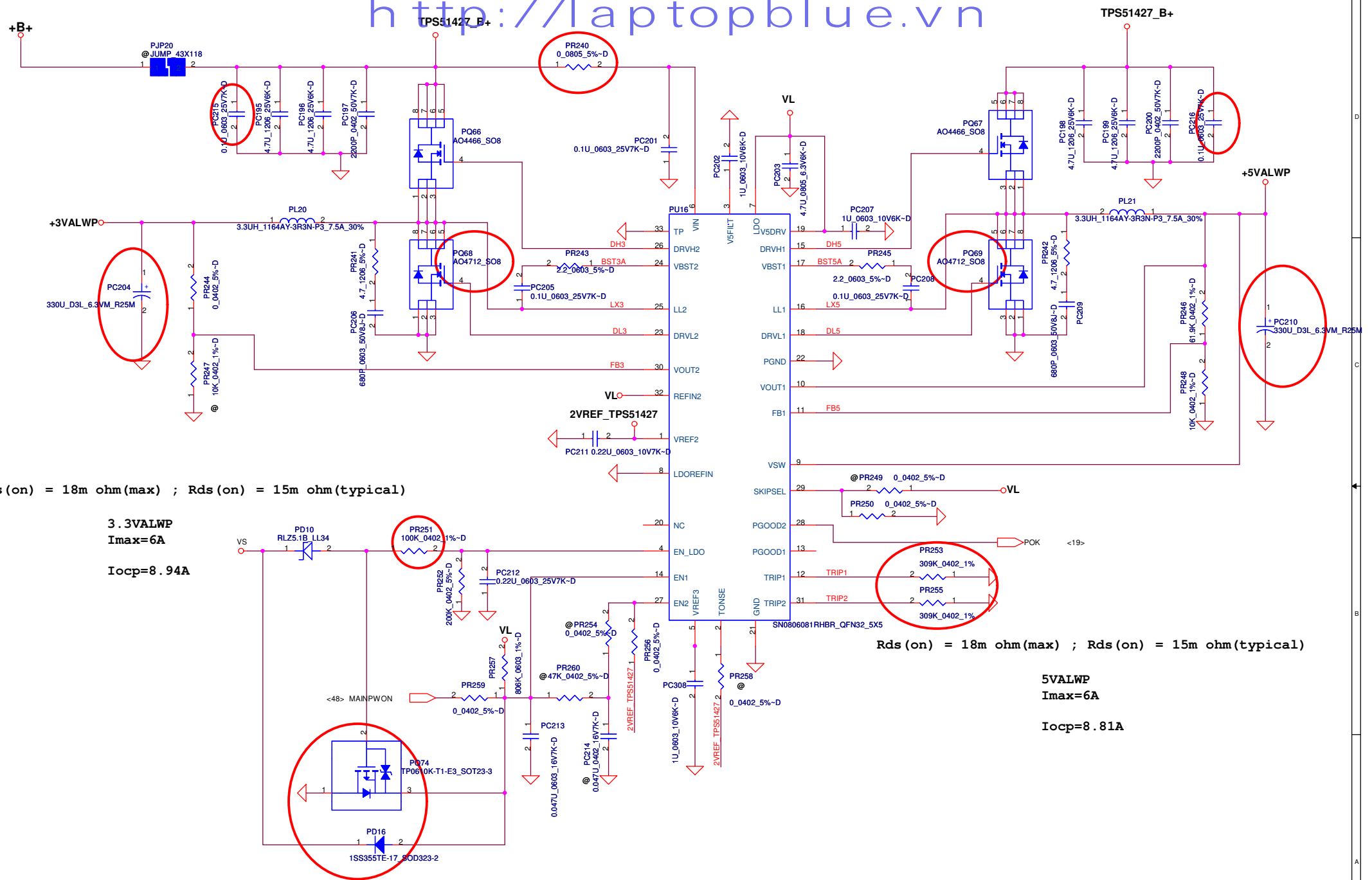
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				Size Custom	Document Number LA-4595P	Rev 1.0
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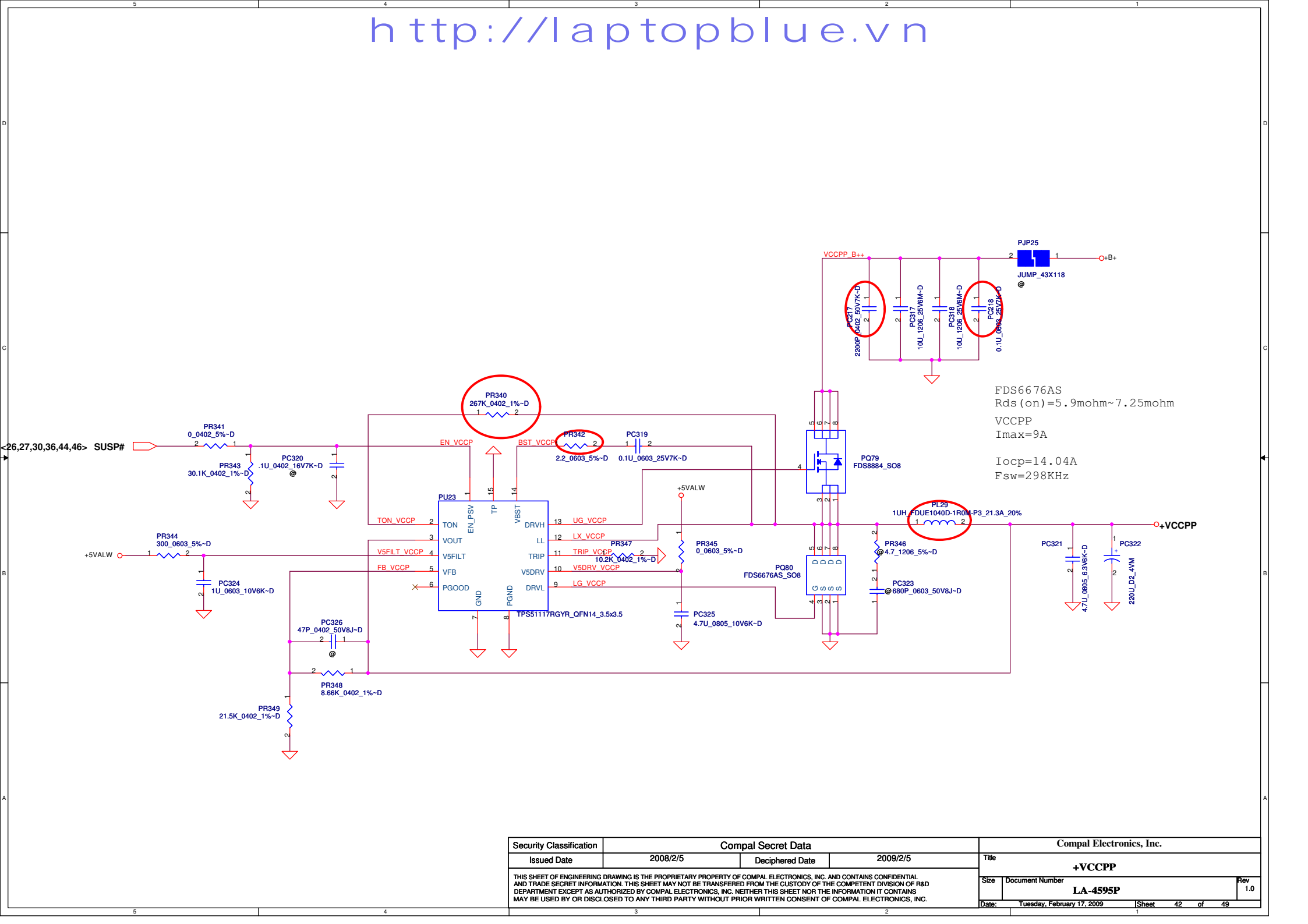
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				Size B	Document Number	Rev	
					KML50	1.0	
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Issued Date	2006/10/1	Deciphered Date	2007/05/30	Size Custom	Document Number <b>LA-4595P</b>
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http://laptopblue.vn

26,27,30,36,44,46> SUSP#

PR341 0.0402\_5%-D

PR343 30.1K\_0402\_1%-D

PC320 .1U\_0402\_16V7K-D

PR344 300.0603\_5%-D

PC324 1U\_0603\_10V6K-D

PC326 47P\_0402\_50V8J-D

PR348 8.66K\_0402\_1%-D

PR349 21.5K\_0402\_1%-D

PR340 267K\_0402\_1%-D

PR342 2.2\_0603\_5%-D

PC319 0.1U\_0603\_25V7K-D

PR345 0.0603\_5%-D

PC325 4.7U\_0805\_10V6K-D

PR347 10.2K\_0402\_1%-D

PR346 4.7\_1206\_5%-D

PC323 680P\_0603\_50V8J-D

PC321 4.7U\_0805\_53V6K-D

PC322 220U\_D2\_4VM

PL29 1UH\_FDUE1040D-1R0M-P3\_21.3A\_20%

VCCPP B++

PJP25 JUMP\_43X118 @

PQ79 FDS8884\_SO8

PQ80 FDS6676AS\_SO8

TPSS1117RGYR\_QFN14\_3.5x3.5

TON\_VCCP

V5FILT\_VCCP

FB\_VCCP

EN\_VCCP

BST\_VCCP

UG\_VCCP

LX\_VCCP

TRIP\_VCCP

V5DRV\_VCCP

LG\_VCCP

Rds(on)=5.9mohm~7.25mohm

VCCPP

Imax=9A

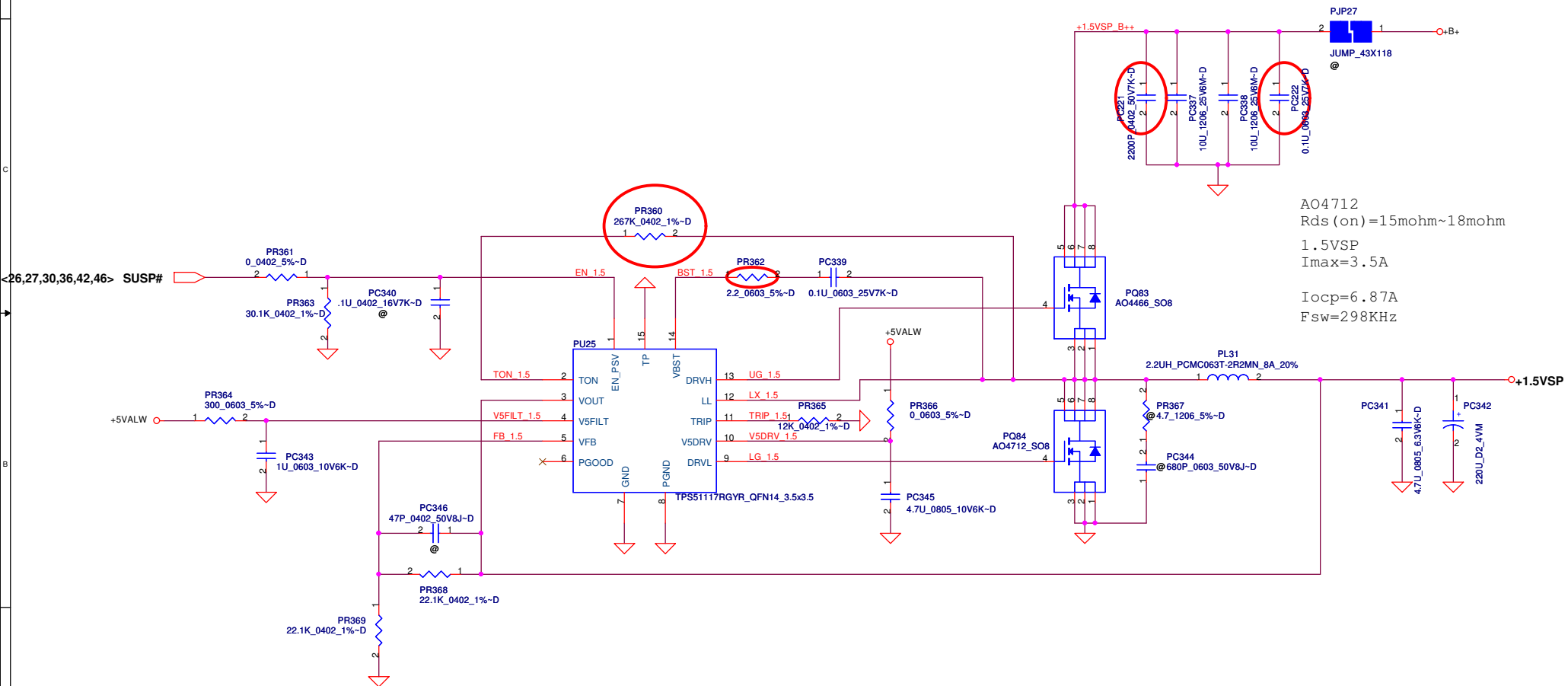
Iocp=14.04A

Fsw=298KHz

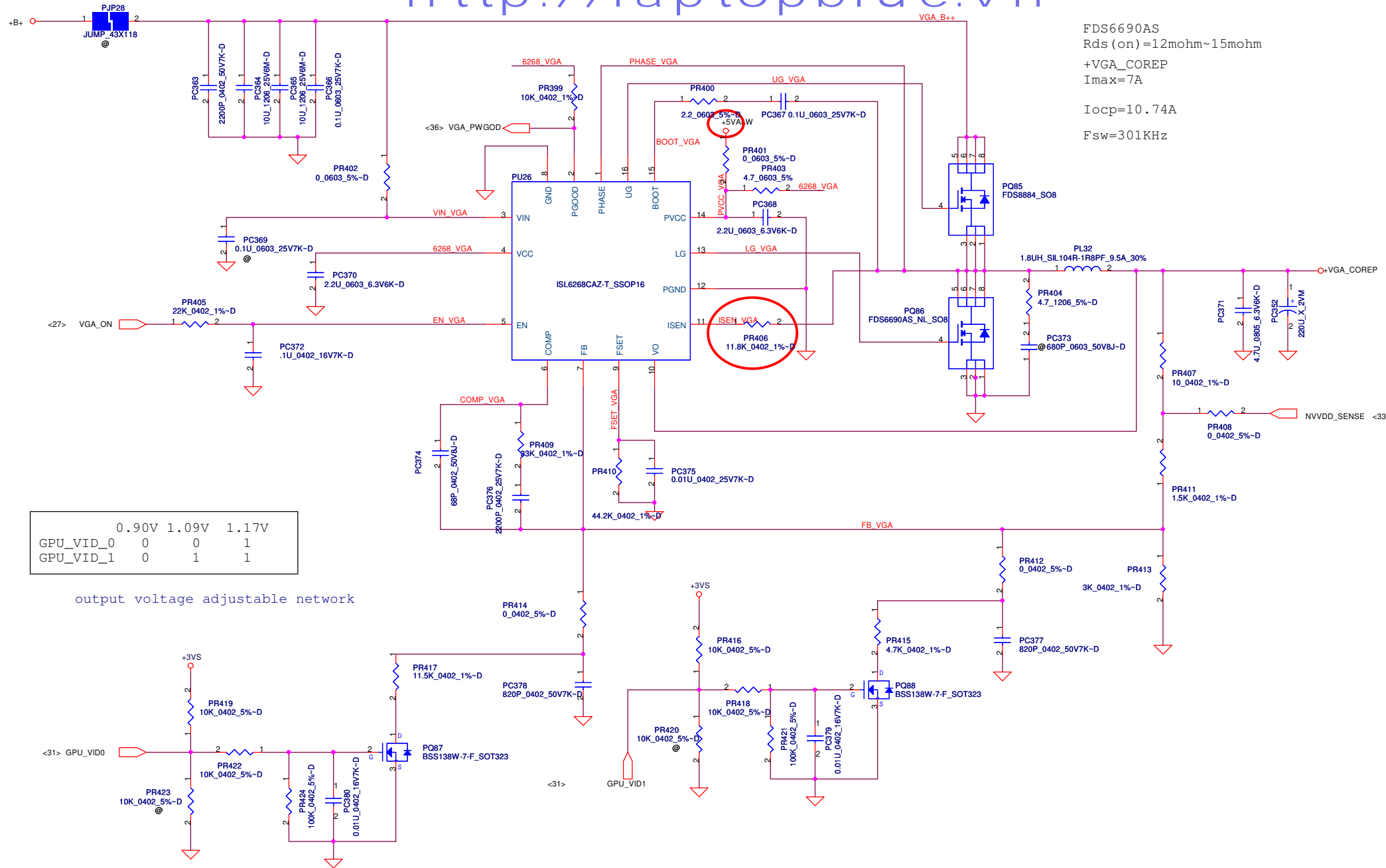
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				Size	Document Number
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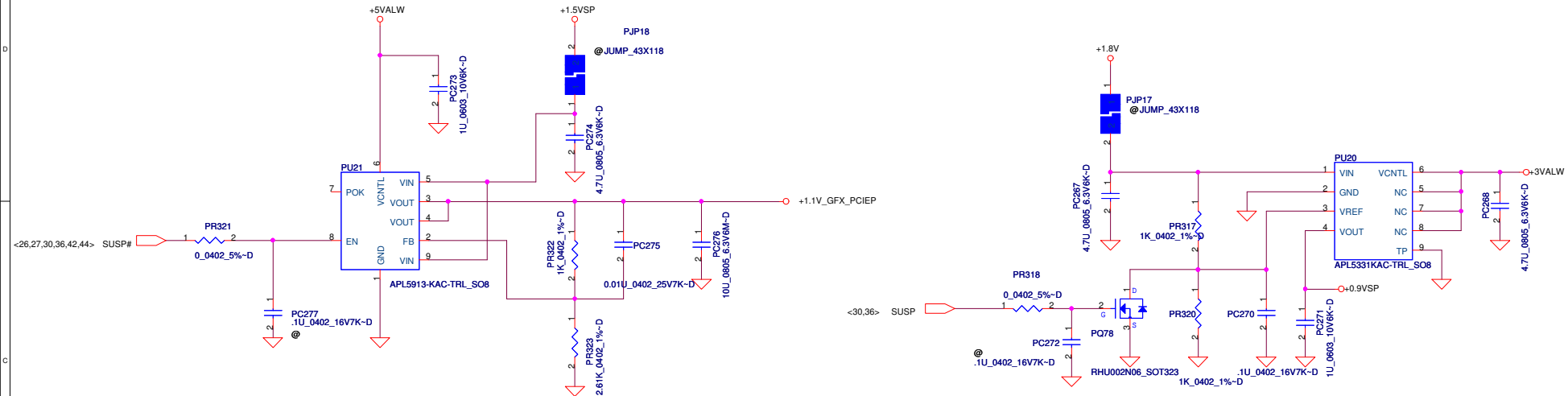


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				Rev	1.0

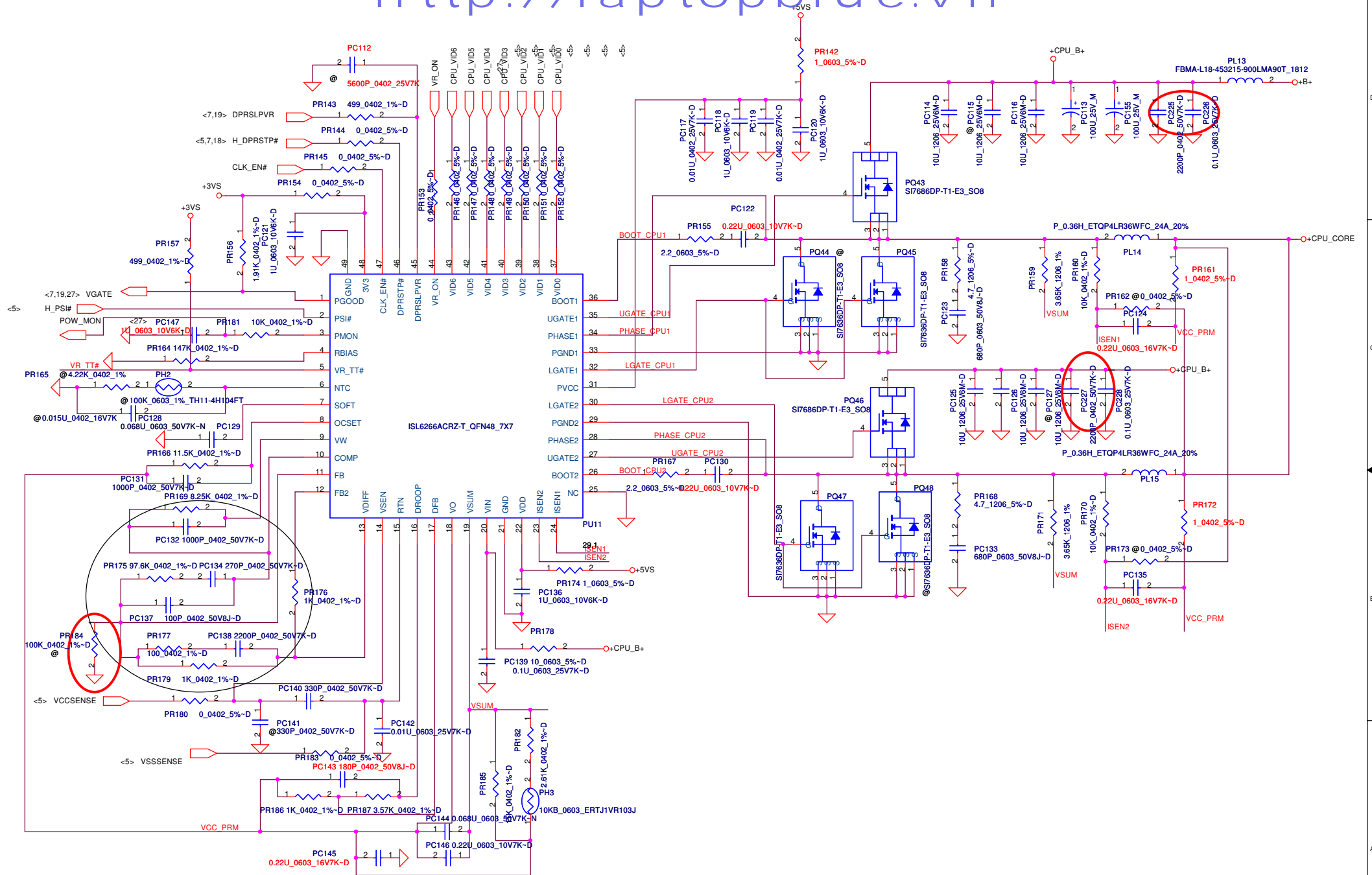


FDS6690AS  
 $R_{ds(on)} = 12\text{mohm} \sim 15\text{mohm}$   
 +VGA\_COREP  
 $I_{max} = 7A$   
 $I_{ocp} = 10.74A$   
 $F_{sw} = 301KHz$

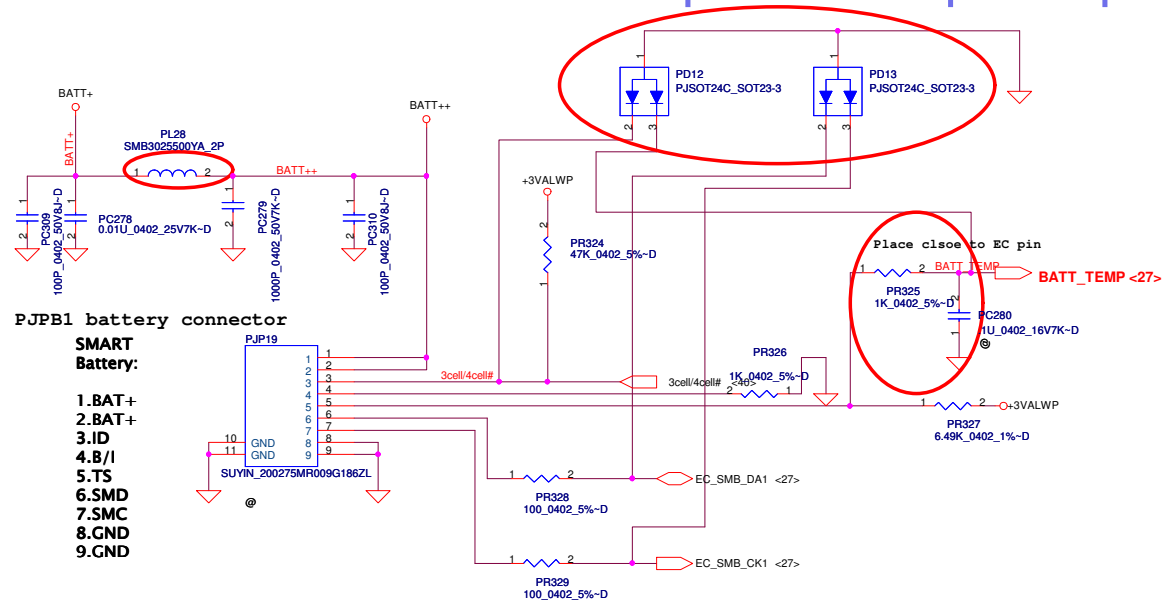
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				+0.9VSP/+1.1V_GFX_PCIEP				
				Size	Document Number			Rev
				Custom	LA-4595P			1.0
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Size	Custom	Document Number	LA-4595P	Rev	
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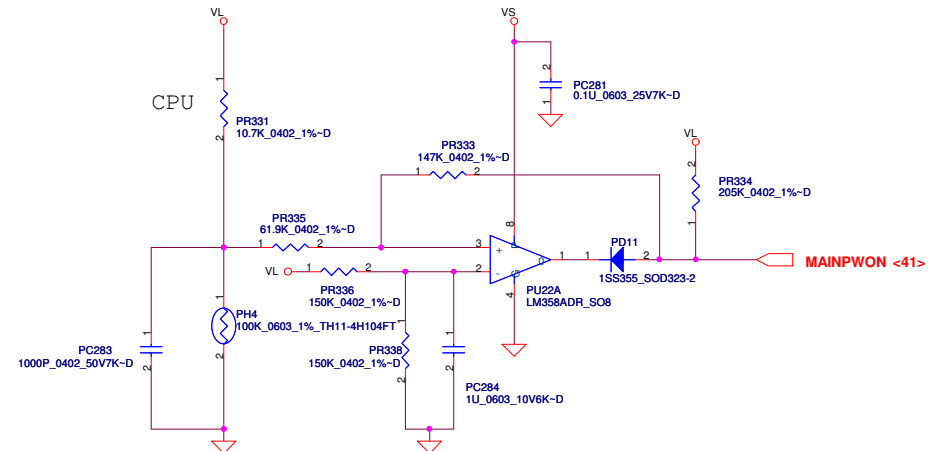
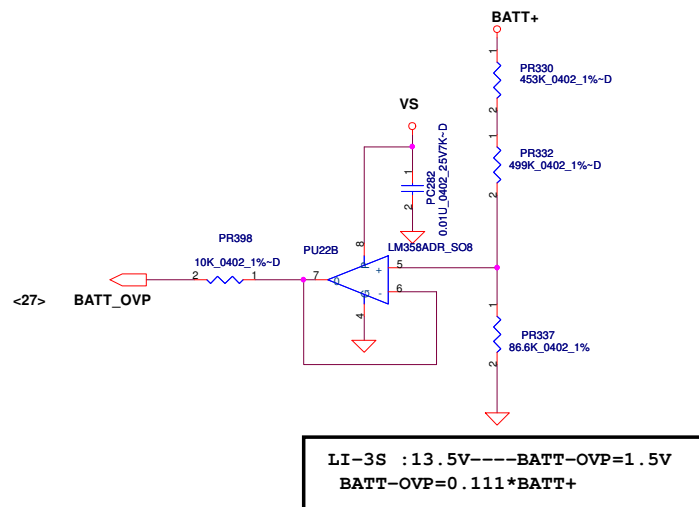


## Battery Connect/OTP

### CPU

**PH1 under CPU bottom side :**

CPU thermal protection at 90 +3 degree C  
Recovery at 50 +3 degree C



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2005/10/1				Deciphered Date			
2007/05/30				Title				BATTERY CONN			
Size				Document Number				Rev			
Custom				LA-4595P				1.0			
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	39	DCIN /Vin Detector	08/12/08	COMPAL	common circuit design modify	change PR203 from 33 to 68 and add PR204 to 68	0.3
2			08/12/08	COMPAL	design modify	change PL17 from SM010018880 to SM010008E10	0.3
3	40	Charger	08/12/08	COMPAL	vendor FAE suggest	change PR272 PR339 from 1 to 3.3	0.3
4	48	BATTERY CONN	08/12/08	COMPAL	design modify	change PL28 from SM010018210 to SM010008E10	0.3
5	39	DCIN /Vin Detector	08/12/12	COMPAL	increase capacitor for EMI request	add PC313 at 0.01uf and PC314 at 0.1uf	0.3
6	42	VCCPP	08/12/12	COMPAL	change resister for EMI request	change PR342 from 0 to 2.2	0.3
7	43	1.8VP	08/12/12	COMPAL	change resister for EMI request	change PR352 from 0 to 2.2	0.3
8	44	1.5VSP	08/12/12	COMPAL	change resister for EMI request	change PR362 from 0 to 2.2	0.3
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