

Compal Model Name: KML60

PCB NO: LA-4671P R03(X02)

BOM P/N: 46161631L01 (DIS)

46161631L02 (UMA)

Function Field: @ unpop
UMA@ UMA component
VGA@ discrete component
CONN@ ME connector
TPM@ TPM component

<http://laptopblue.vn>

Half Penny Bridge 17"

Compal Confidential

Schematic Document

Cantiga + ICH9

2009 / 2 / 19 Rev:1.0 (A00)

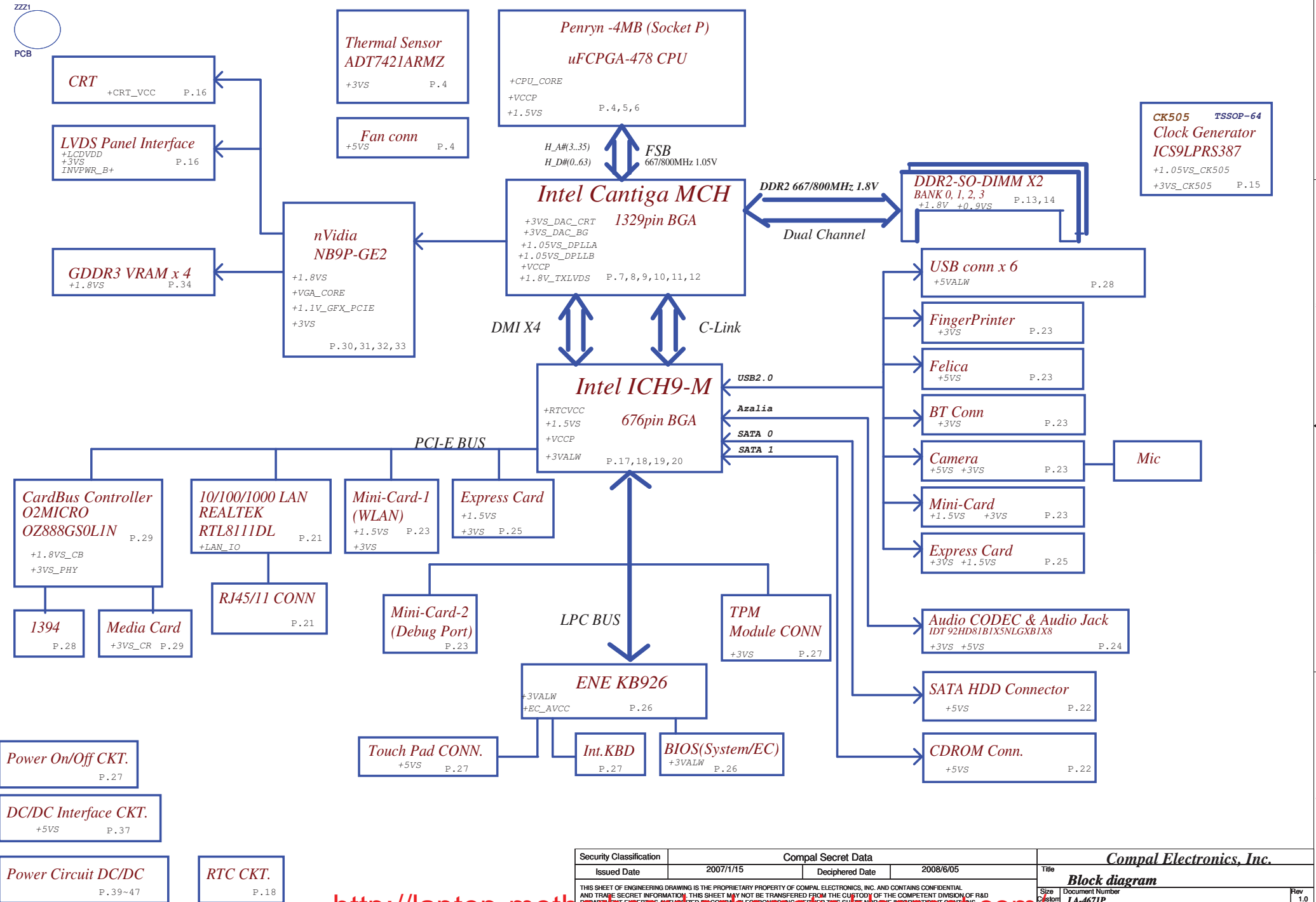
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Half Penny Bridge 17

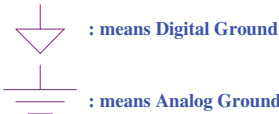


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power plane	+B	+5VALW	+1.8V	+5VS
				+3VS
State		+3VALW		+1.5VS
				+0.9V
				+VCCP
				+CPU_CORE
				+VGA_CORE
				+2.5VS
				+1.8VS
				+1.2VS
				+0.9VGA
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

ICH9-M	USB PORT#	DESTINATION
	0	JUSBP1
	1	CAMERA
	2	JUSBP3
	3	Felica
	4	Blue Tooth
	5	Finger Printer
	6	JMINI2-WLAN
	7	Express card
	8	JUSBP3
	9	JMINI1-WWAN
	10	JUSBP4
	11	NA

Symbol Note :



@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	115K +/-1%	1.6613 V	1.7651 V	1.8706 V
1	154K +/-1%	1.8857 V	2.0008 V	2.1173 V
2	215K +/-1%	2.1261 V	2.2524 V	2.38 V
3	316K +/-1%	2.3948 V	2.5067 V	2.6447 V
4	560K +/-1%	2.6519 V	2.8 V	2.9488 V
5	NC			
6	NC			
7	NC			

PCI EXPRESS	DESTINATION
Lane 1	NA
Lane 2	GLAN RTL8111DL
Lane 3	MINI CARD WLAN
Lane 4	EXPRESS CARD
Lane 5	CARD READER OZ886
Lane 6	NA

SATA	DESTINATION
Lane 0	HDD
Lane 1	ODD
Lane 4	NA
Lane 5	NA

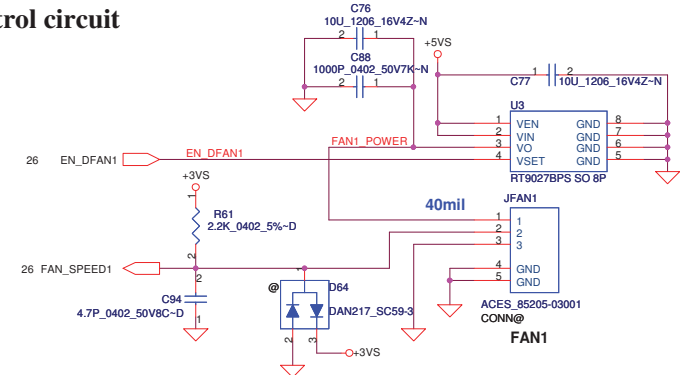
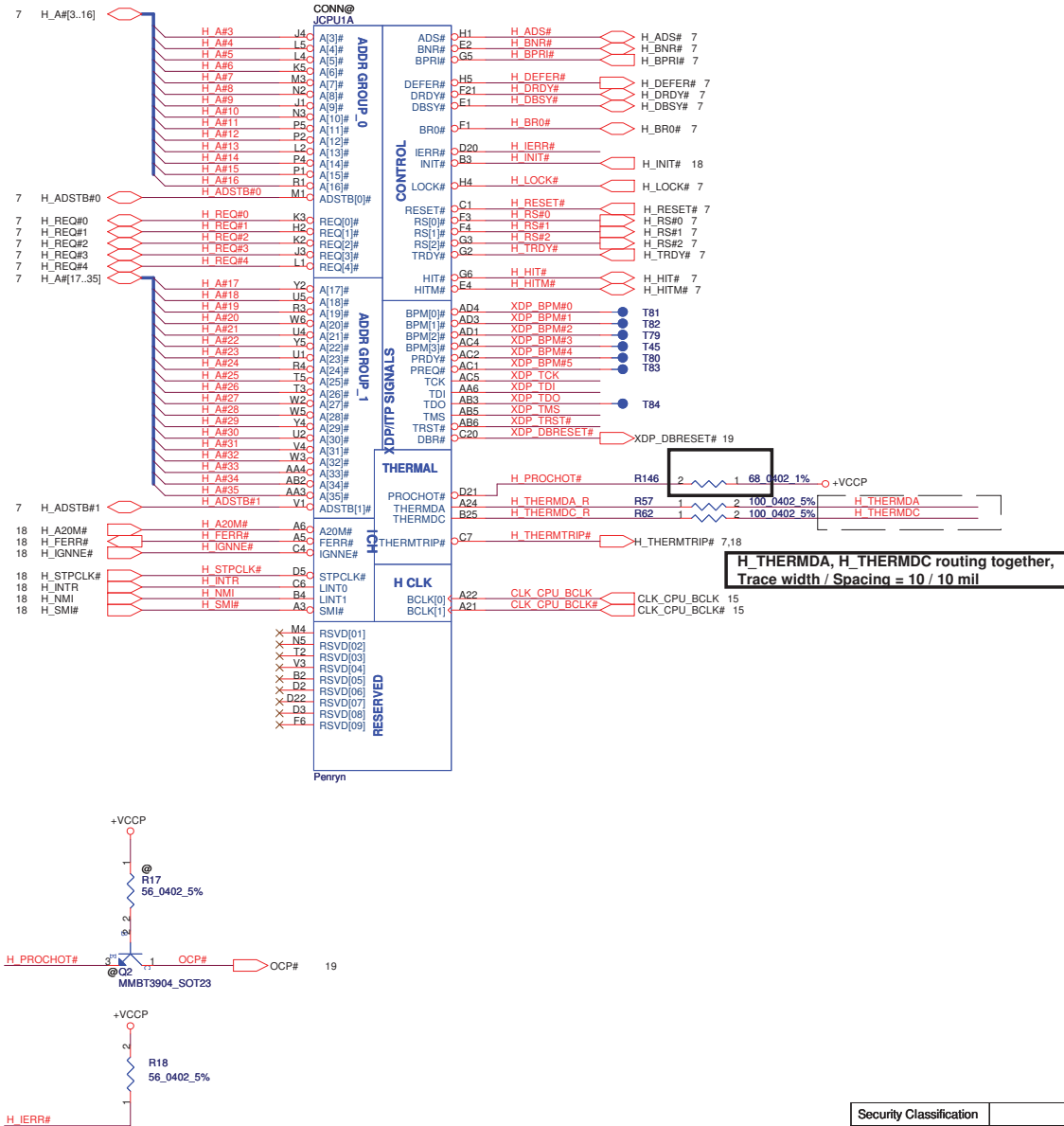
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

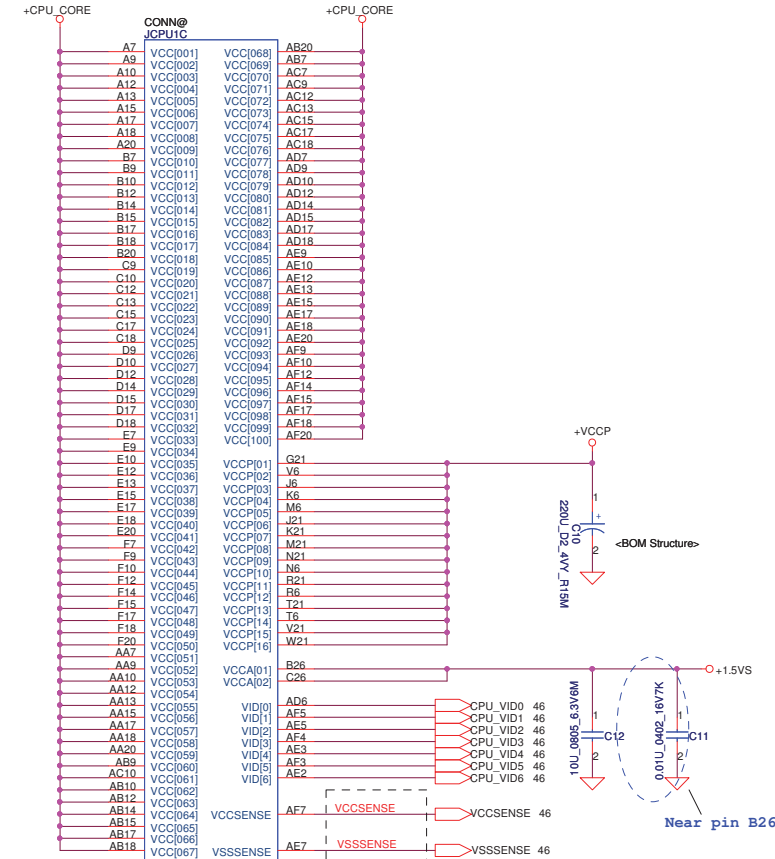
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

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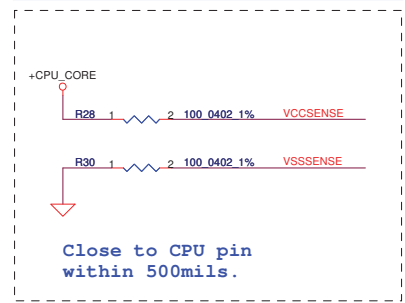


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Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4

Length match within 25 mils.
The trace width/space/other is
20/7/25.



Close to CPU pin
within 500mils.

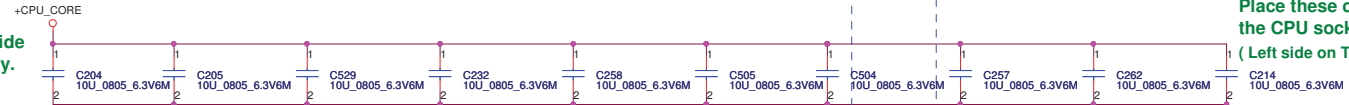
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High Frequency Decoupling

10uF 0805 X5R -> 85 degree.

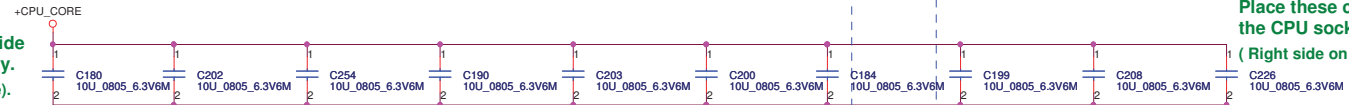
CONN#	ICPUID				
A4	VSS[001]	VSS[082]	P6		
A8	VSS[002]	VSS[083]	P21		
A11	VSS[003]	VSS[084]	P24		
A14	VSS[004]	VSS[085]	R5		
A16	VSS[005]	VSS[086]	R22		
A19	VSS[006]	VSS[087]	R25		
A23	VSS[007]	VSS[088]	T1		
AF2	VSS[008]	VSS[089]	T4		
B6	VSS[009]	VSS[090]	T23		
B8	VSS[010]	VSS[091]	T26		
B11	VSS[011]	VSS[092]	U3		
B13	VSS[012]	VSS[093]	U6		
B16	VSS[013]	VSS[094]	U21		
B19	VSS[014]	VSS[095]	U24		
B21	VSS[015]	VSS[096]	V2		
B24	VSS[016]	VSS[097]	V5		
C5	VSS[017]	VSS[098]	V22		
C8	VSS[018]	VSS[099]	V25		
C11	VSS[019]	VSS[100]	W1		
C14	VSS[020]	VSS[101]	W4		
C16	VSS[021]	VSS[102]	W23		
C19	VSS[022]	VSS[103]	W26		
C2	VSS[023]	VSS[104]	Y3		
C22	VSS[024]	VSS[105]	Y6		
C25	VSS[025]	VSS[106]	Y21		
D1	VSS[026]	VSS[107]	Y24		
D4	VSS[027]	VSS[108]	AA2		
D8	VSS[028]	VSS[109]	AA5		
D11	VSS[029]	VSS[110]	AA8		
D16	VSS[030]	VSS[111]	AA11		
D19	VSS[031]	VSS[112]	AA14		
D23	VSS[032]	VSS[113]	AA16		
D26	VSS[033]	VSS[114]	AA19		
E3	VSS[034]	VSS[115]	AA22		
E6	VSS[035]	VSS[116]	AA25		
E8	VSS[036]	VSS[117]	AB1		
E11	VSS[037]	VSS[118]	AB4		
E14	VSS[038]	VSS[119]	AB8		
E16	VSS[039]	VSS[120]	AB11		
E19	VSS[040]	VSS[121]	AB13		
E21	VSS[041]	VSS[122]	AB16		
E24	VSS[042]	VSS[123]	AB19		
F5	VSS[043]	VSS[124]	AB23		
F8	VSS[044]	VSS[125]	AB26		
F11	VSS[045]	VSS[126]	AC3		
F13	VSS[046]	VSS[127]	AC6		
F16	VSS[047]	VSS[128]	AC8		
F19	VSS[048]	VSS[129]	AC11		
F2	VSS[049]	VSS[130]	AC14		
F22	VSS[050]	VSS[131]	AC16		
F25	VSS[051]	VSS[132]	AC19		
G4	VSS[052]	VSS[133]	AC21		
G11	VSS[053]	VSS[134]	AC24		
G23	VSS[054]	VSS[135]	AD2		
G26	VSS[055]	VSS[136]	AD5		
H3	VSS[056]	VSS[137]	AD8		
H6	VSS[057]	VSS[138]	AD11		
H21	VSS[058]	VSS[139]	AD13		
H24	VSS[059]	VSS[140]	AD16		
J2	VSS[060]	VSS[141]	AD19		
J5	VSS[061]	VSS[142]	AD22		
J22	VSS[062]	VSS[143]	AD25		
J25	VSS[063]	VSS[144]	AE1		
K1	VSS[064]	VSS[145]	AE4		
K4	VSS[065]	VSS[146]	AE8		
K23	VSS[066]	VSS[147]	AE11		
K26	VSS[067]	VSS[148]	AE14		
L3	VSS[068]	VSS[149]	AE16		
L6	VSS[069]	VSS[150]	AE19		
L21	VSS[070]	VSS[151]	AE23		
L24	VSS[071]	VSS[152]	AE26		
M2	VSS[072]	VSS[153]	A2		
M5	VSS[073]	VSS[154]	AF6		
M22	VSS[074]	VSS[155]	AF8		
M25	VSS[075]	VSS[156]	AF11		
N1	VSS[076]	VSS[157]	AF13		
N4	VSS[077]	VSS[158]	AF16		
N23	VSS[078]	VSS[159]	AF19		
N26	VSS[079]	VSS[160]	AF21		
P3	VSS[080]	VSS[161]	A25		
	VSS[081]	VSS[162]	AF25		
		VSS[163]			

Place these caps inside the CPU socket cavity. (Left side on Top).



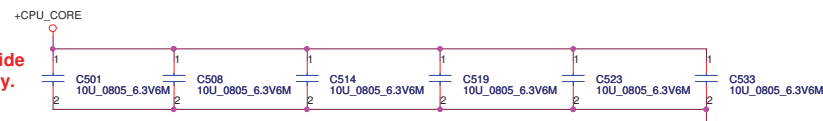
Place these caps inside the CPU socket. (Left side on Top).

Place these caps inside the CPU socket cavity. (Right side on Top side).

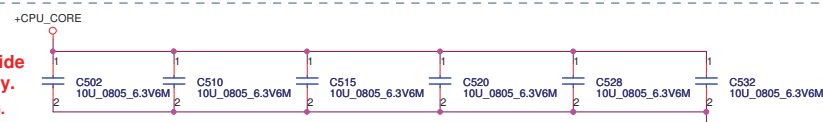


Place these caps inside the CPU socket. (Right side on Top).

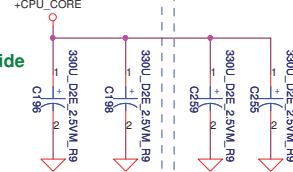
Place these caps inside the CPU socket cavity. (Left side on Bottom).



Place these caps inside the CPU socket cavity. (Right side on Bottom).



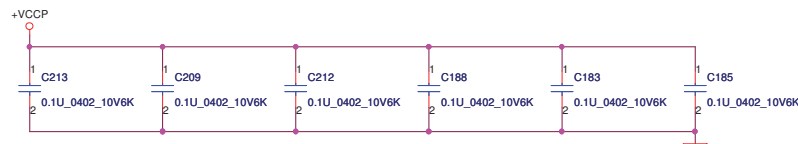
Place these caps inside the CPU socket. (Left side on Top).



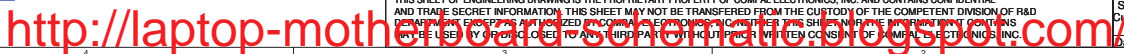
Place these caps inside the CPU socket. (Right side on Top side).

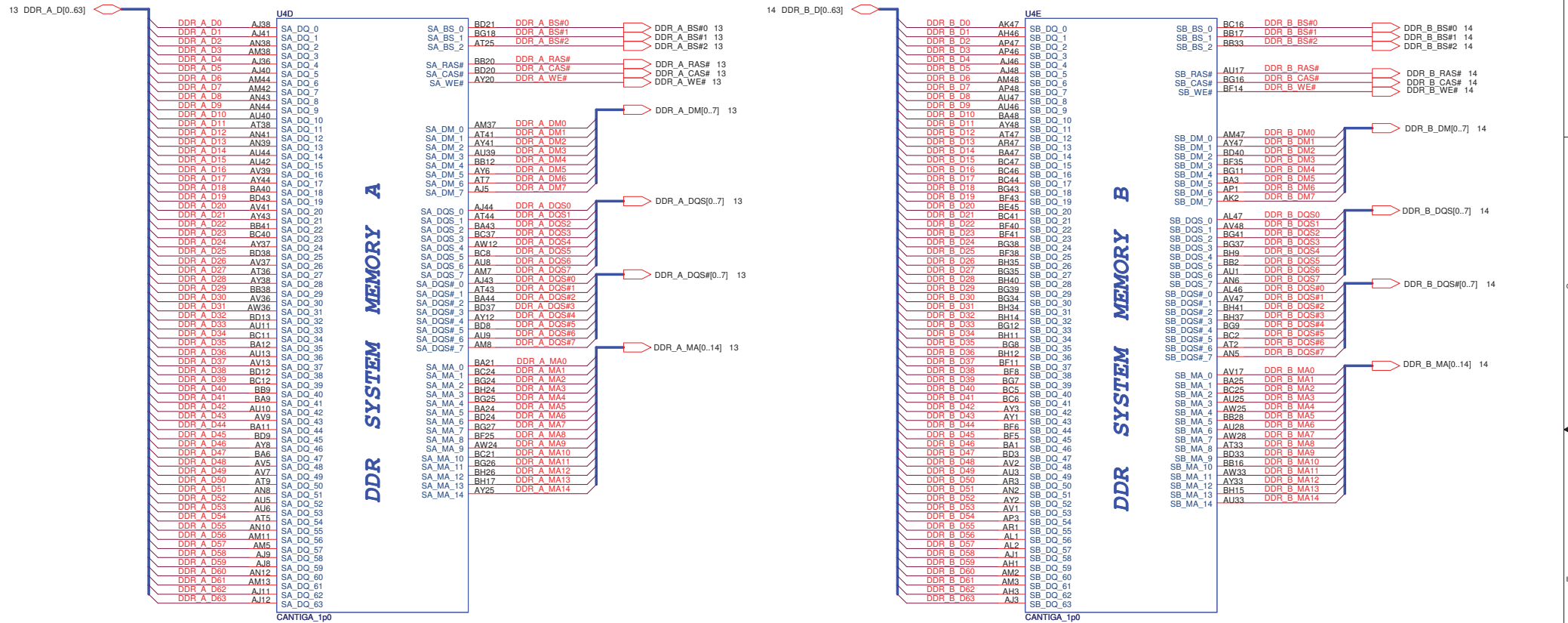
ESR <= 1.5m ohm
Capacitor > 880 uF

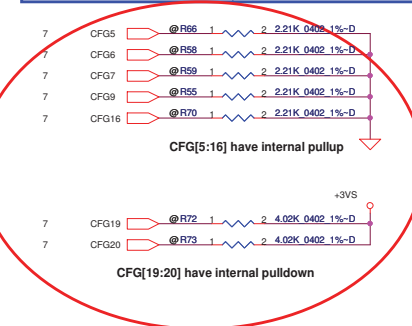
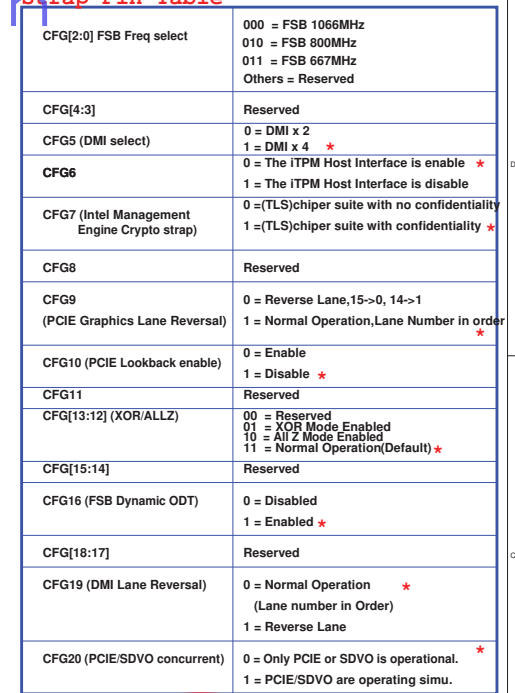
Place these inside socket cavity on L8 (North side Secondary)



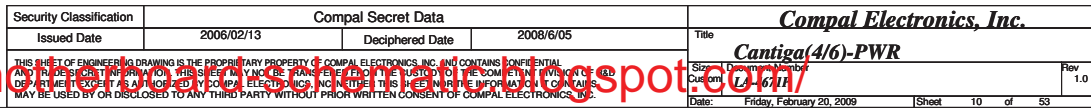
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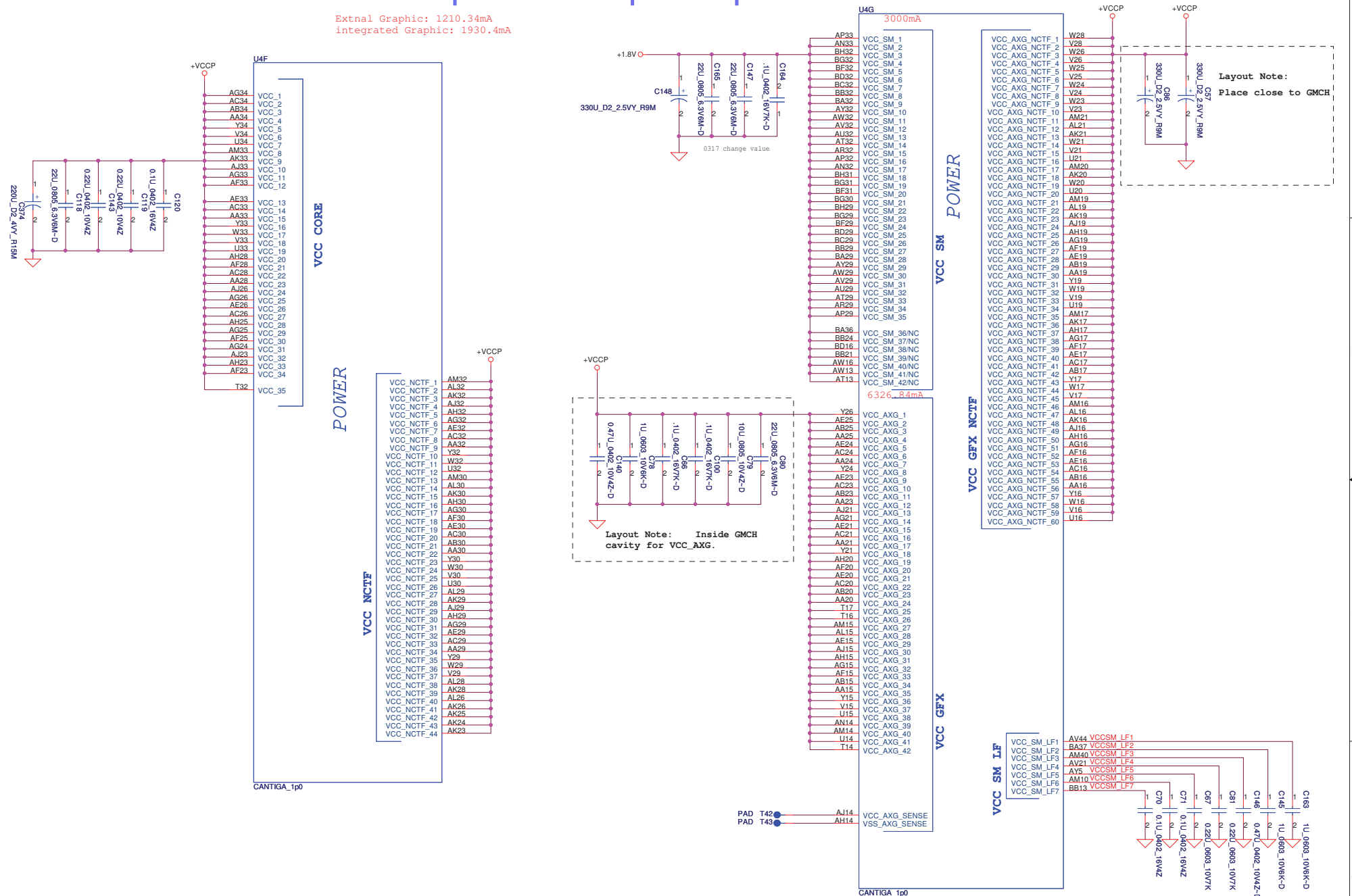




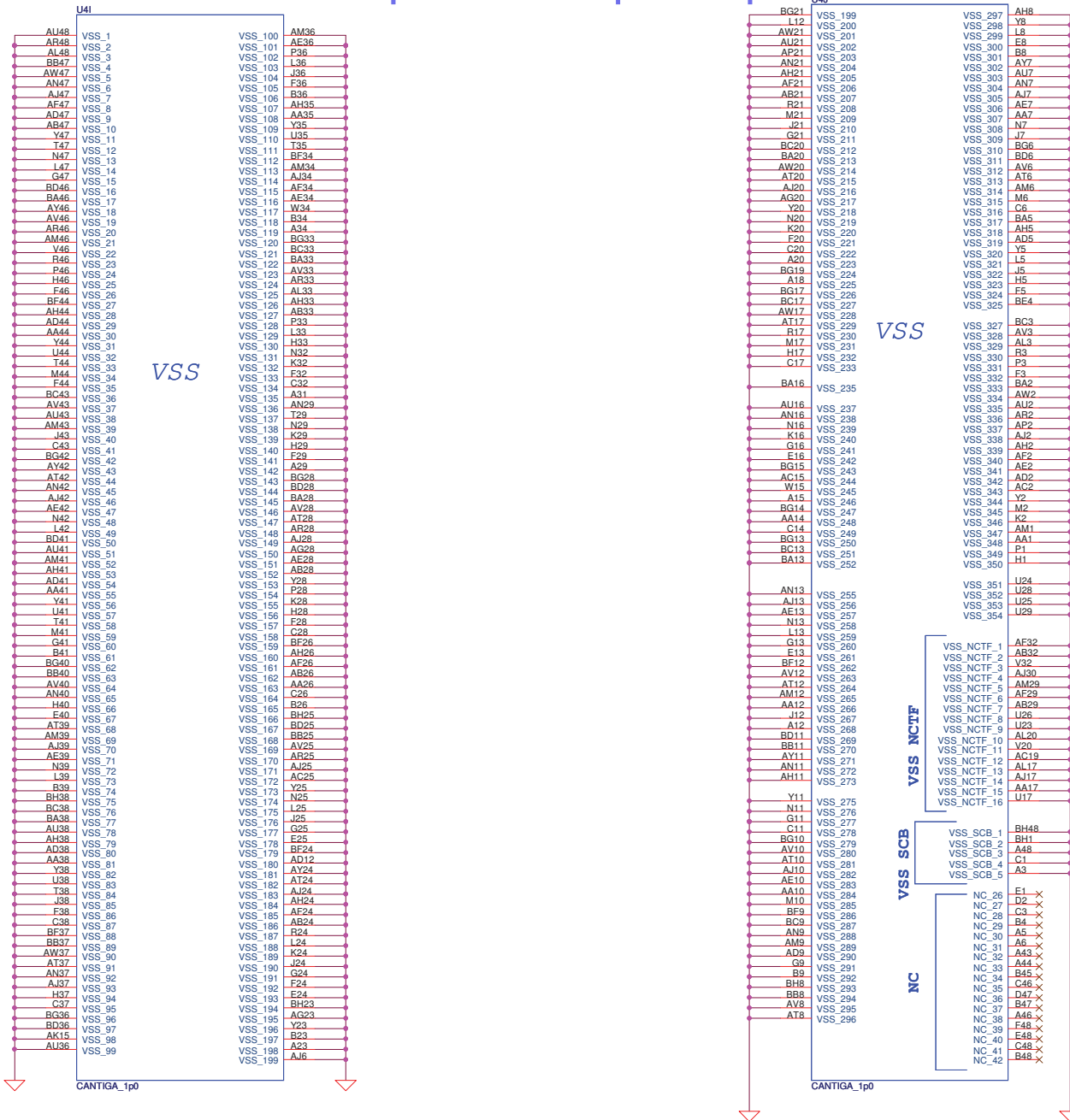


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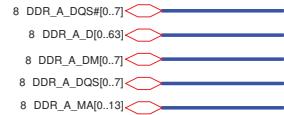




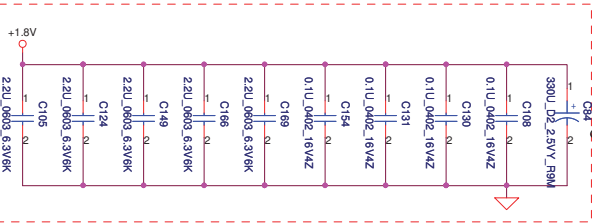
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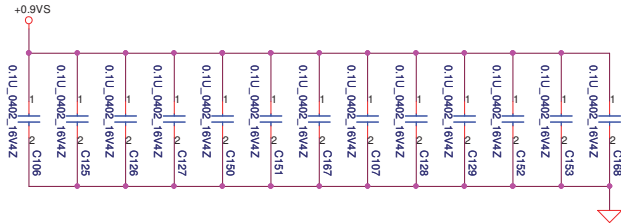
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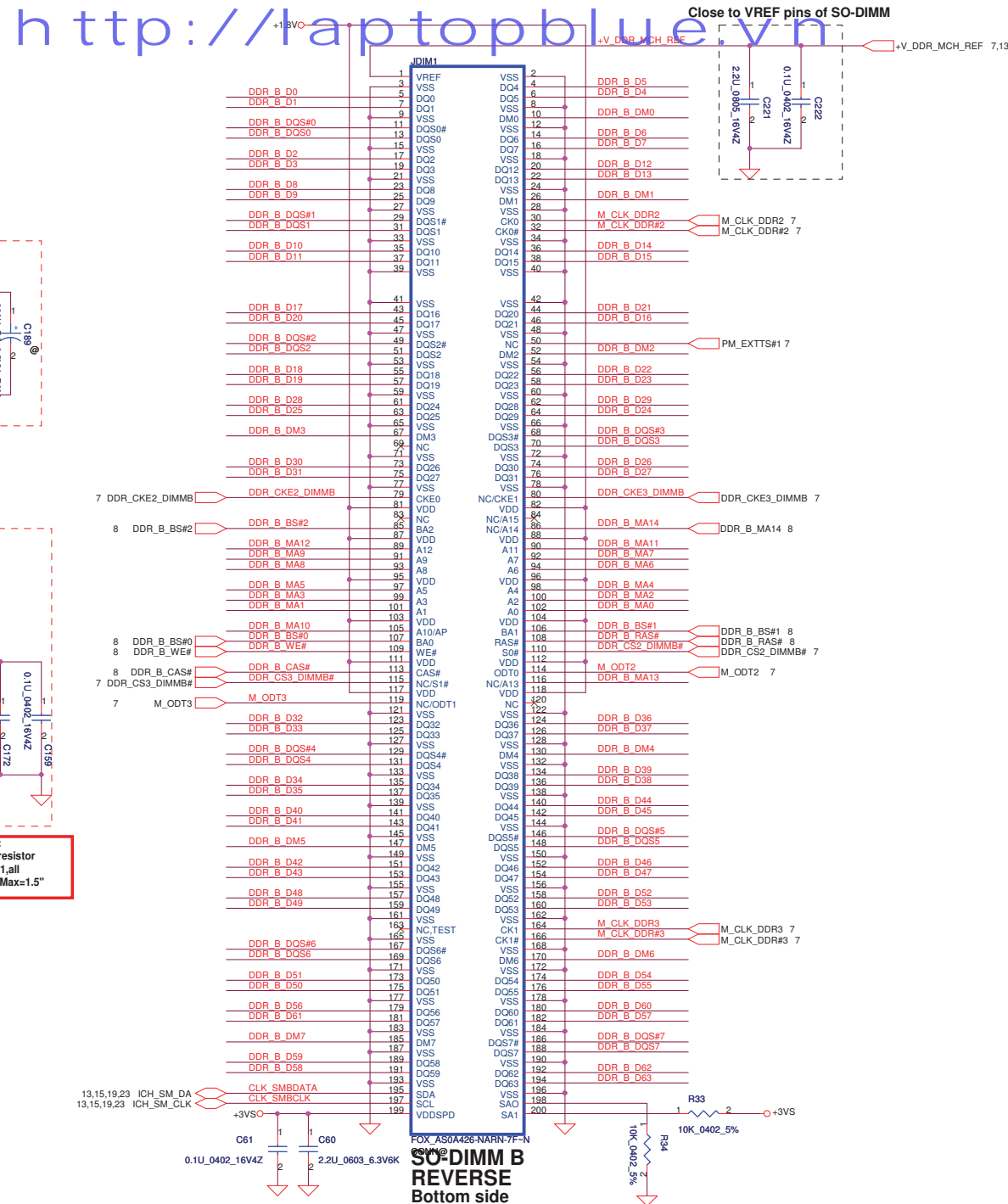
Layout Note:
Place near JDM2



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V

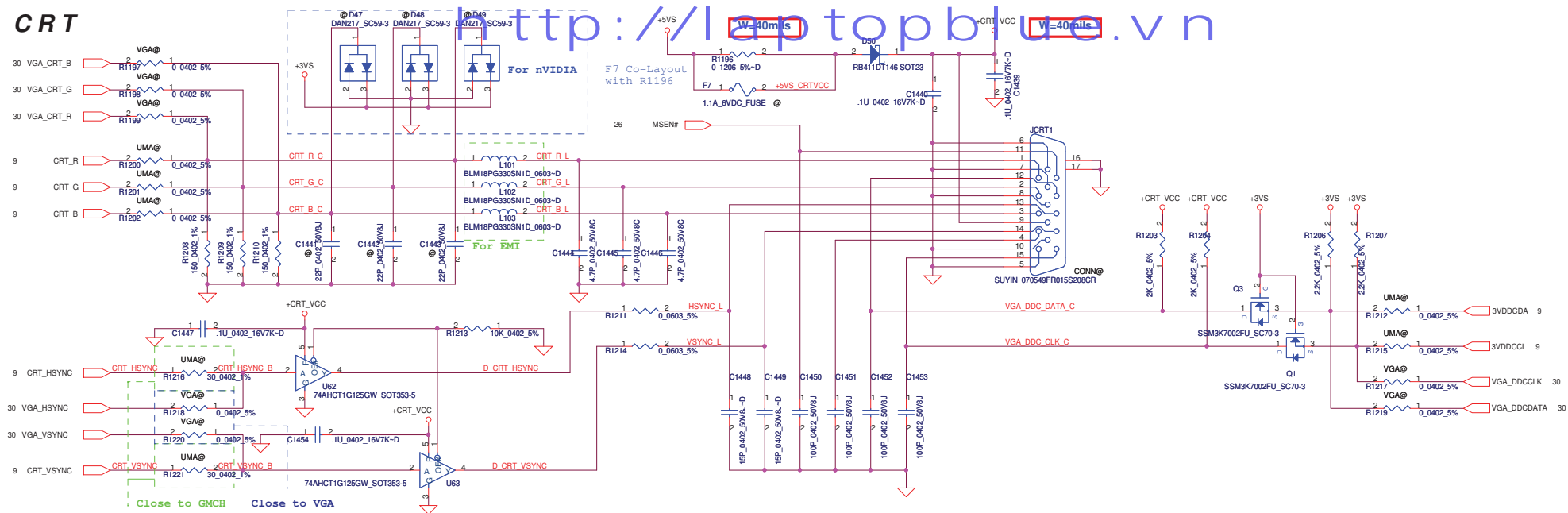


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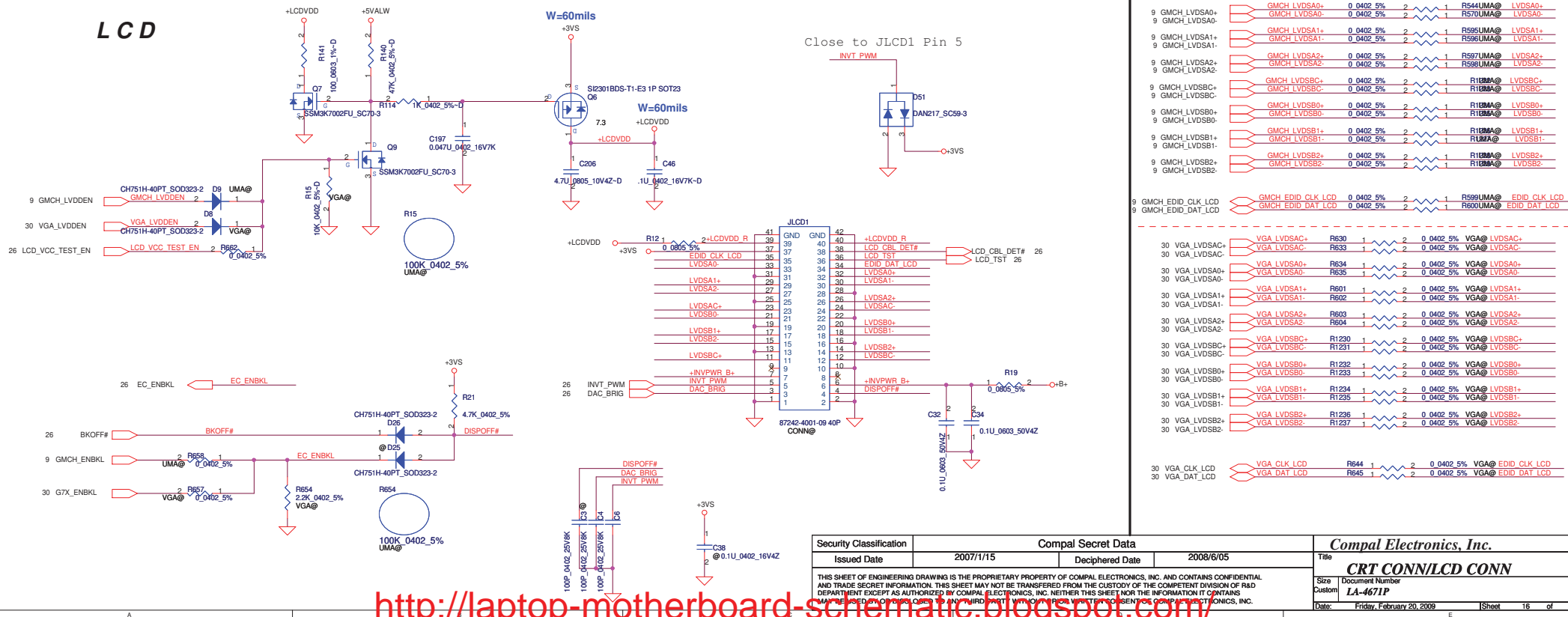


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				Checked by	14010101	
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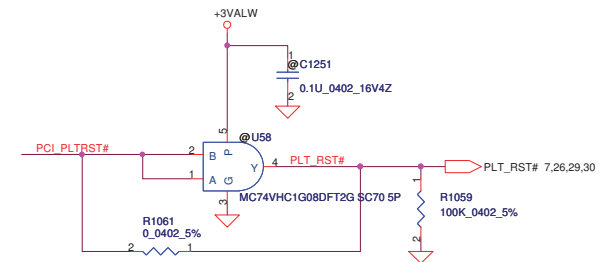
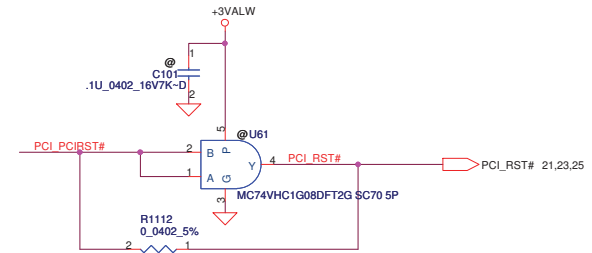
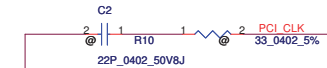
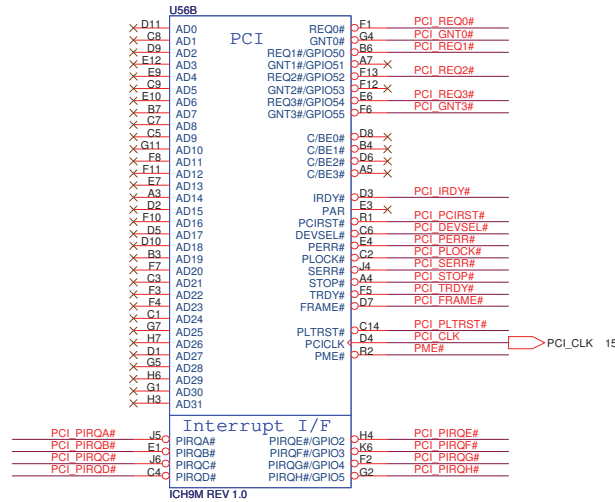
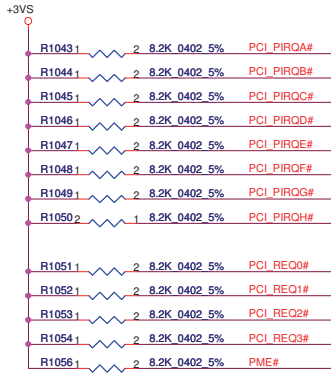
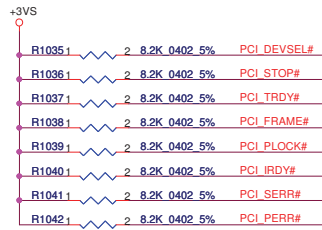
CRT



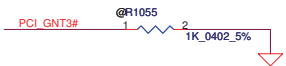
LCD



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				Custom	LA-467IP	1.0
Date: Friday, February 20, 2009				Sheet	16	of 53



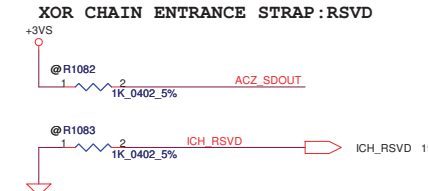
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*



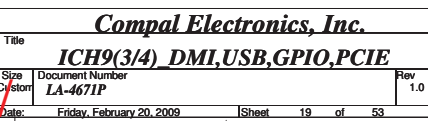
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

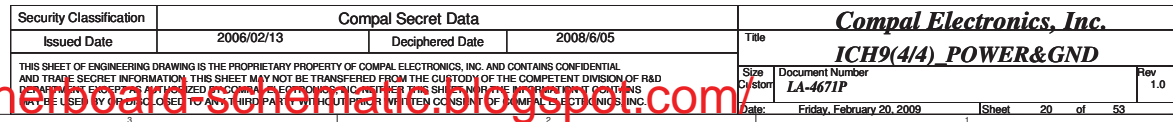


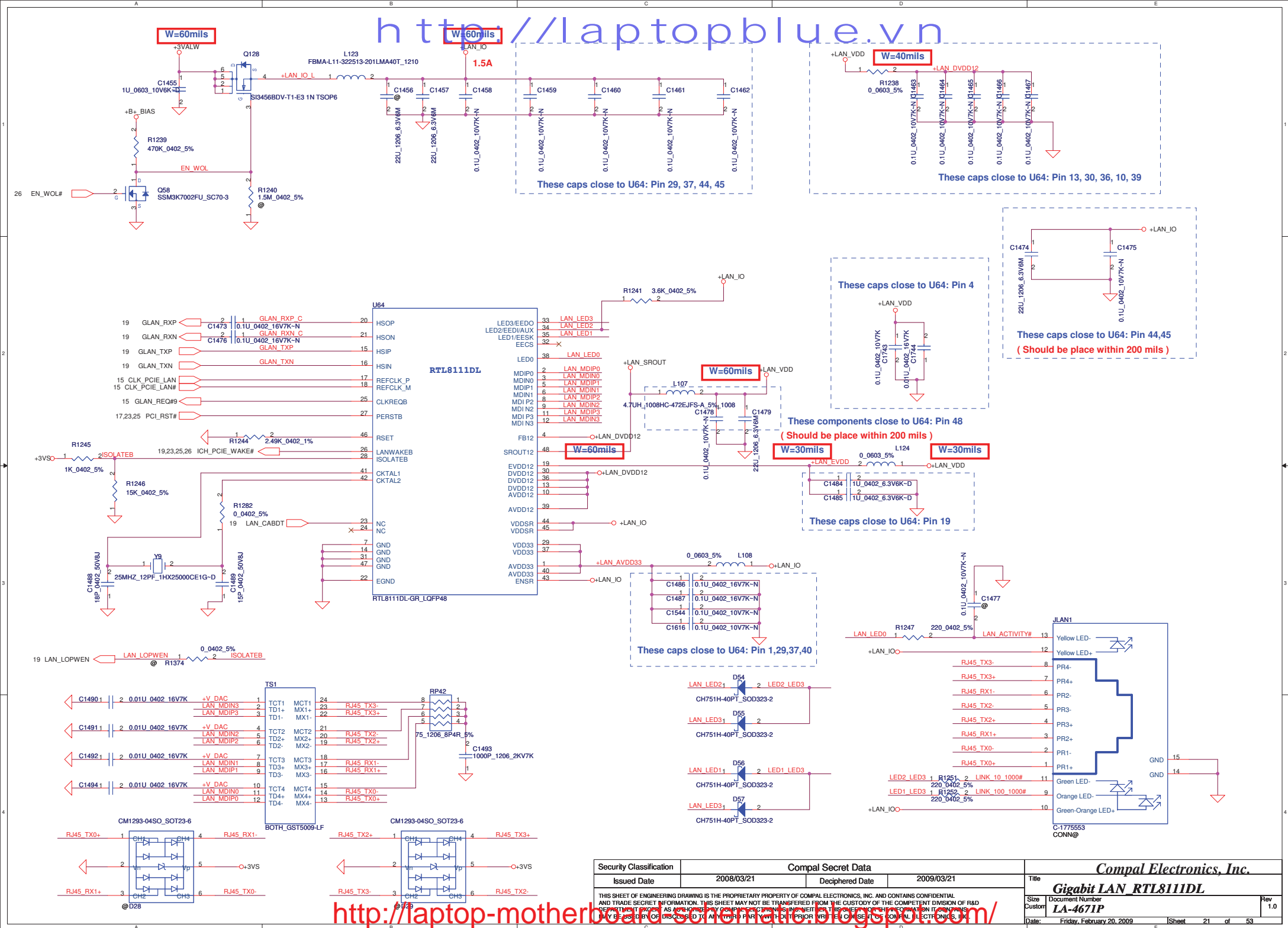
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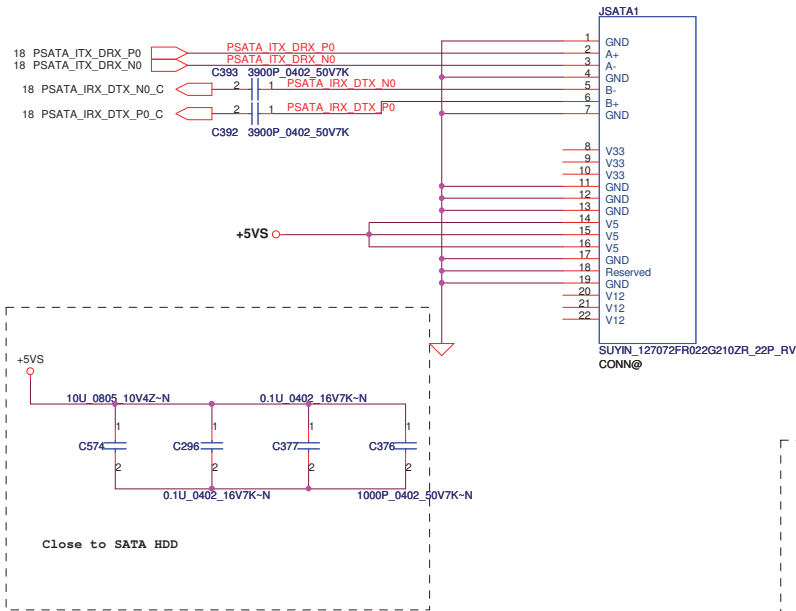
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Issued Date	2006/02/13	Deciphered Date	2008/6/05	Title	
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				Date:	Friday, February 20, 2009
				Sheet	18 of 53



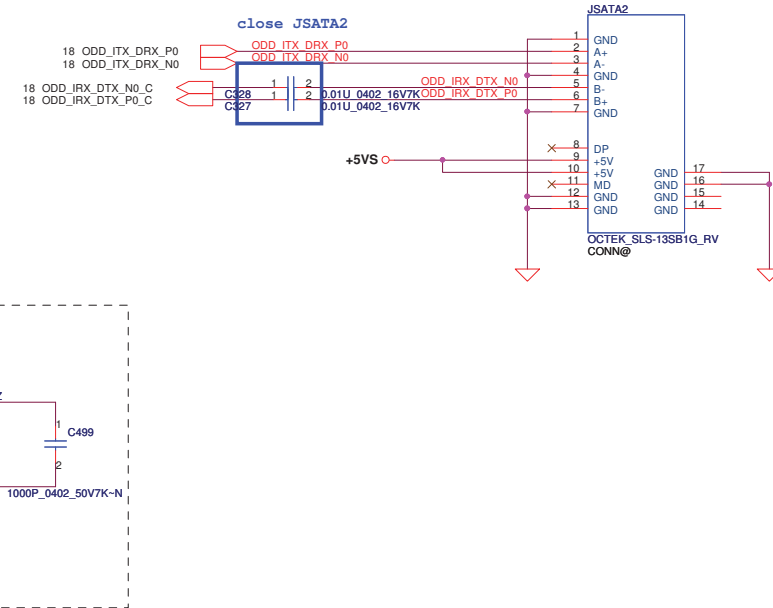




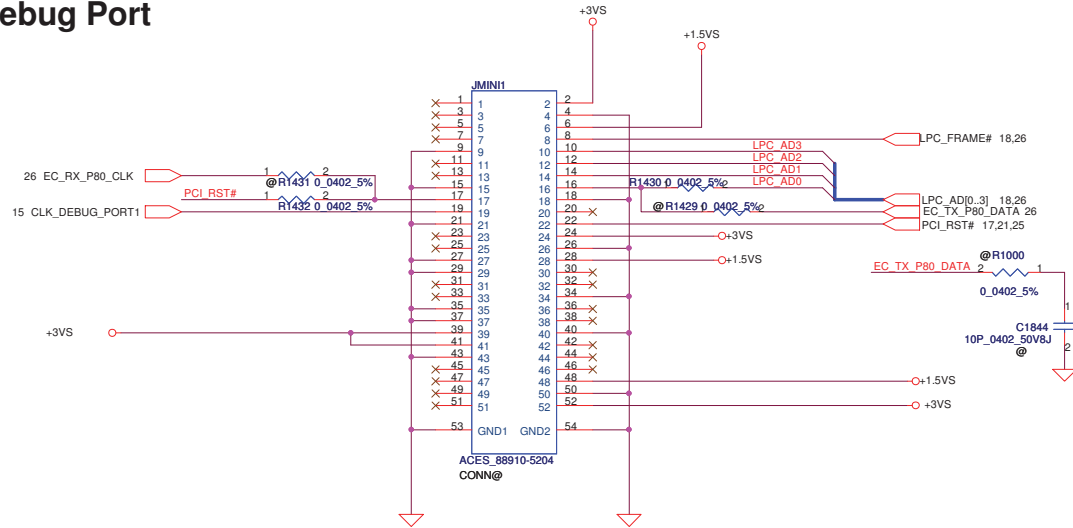
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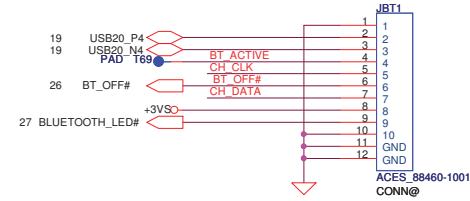
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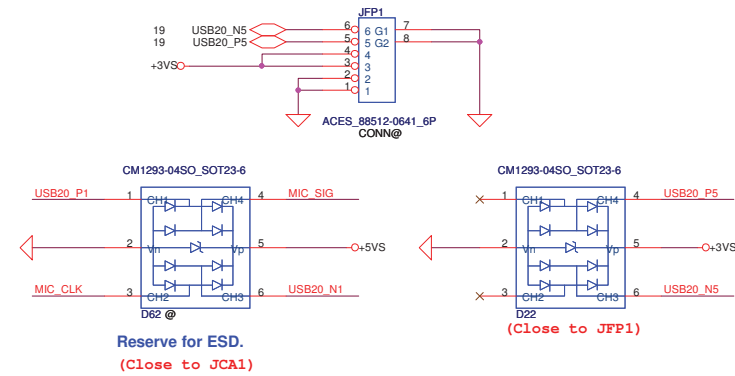
Debug Port



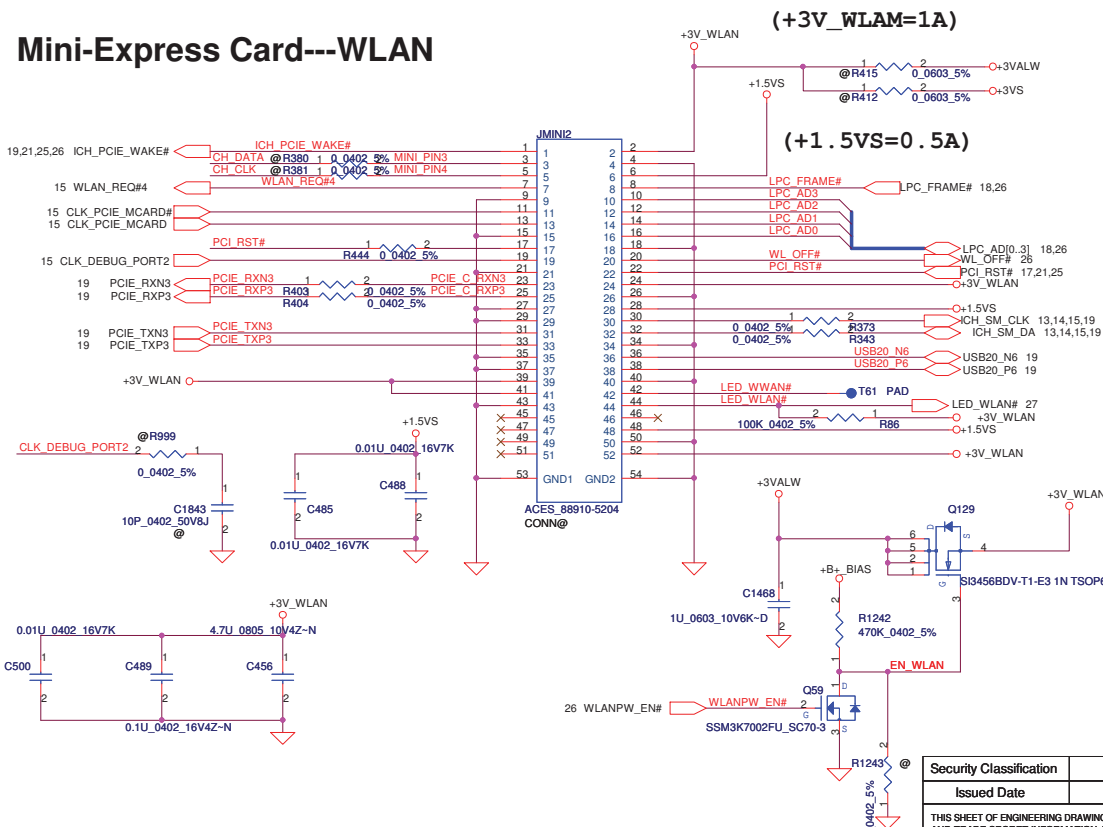
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Fingerprint

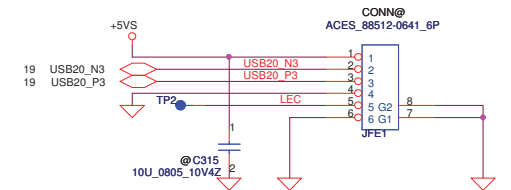


Mini-Express Card---WLAN

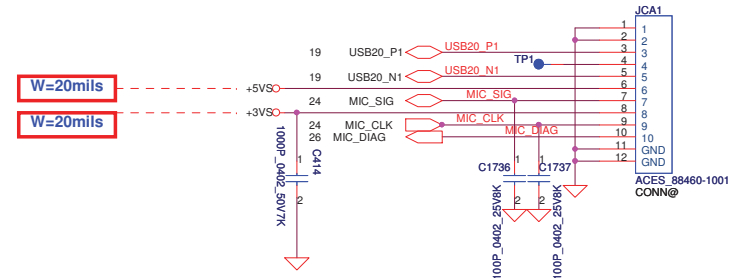


Felica

Felica Conn

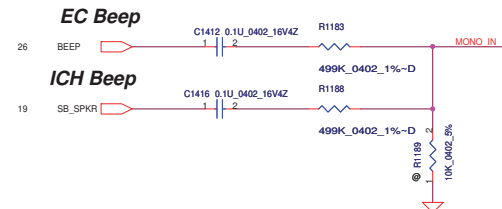


Camera Conn



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				Date	Friday, February 20, 2009
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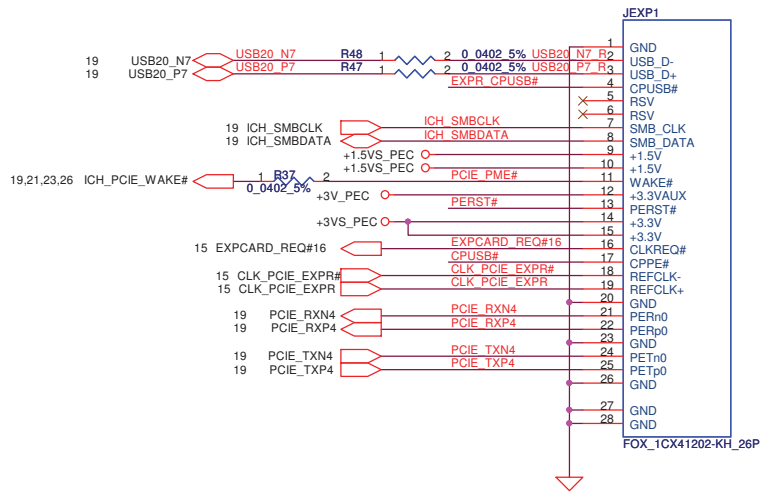
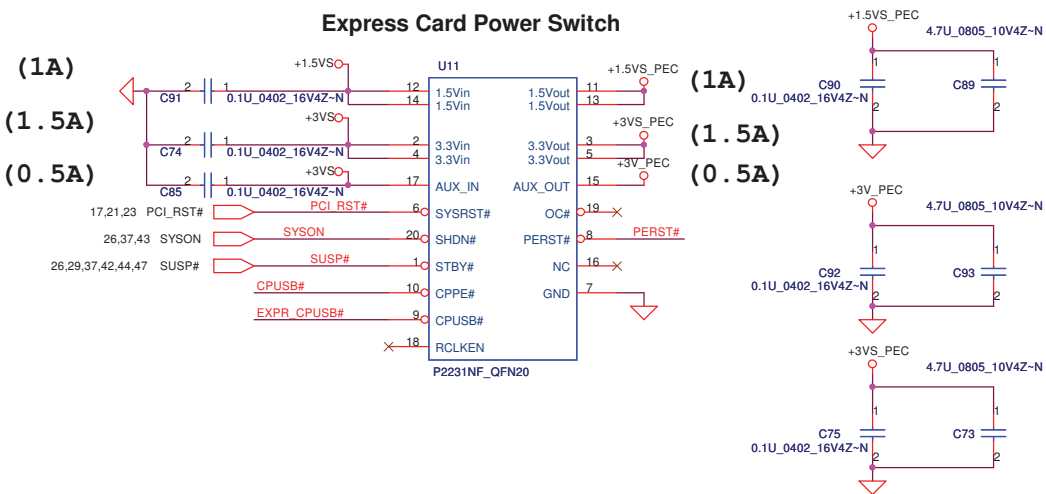
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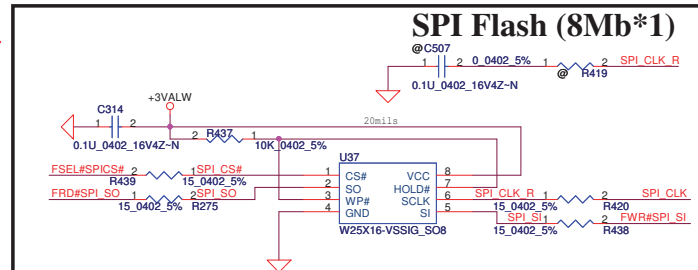
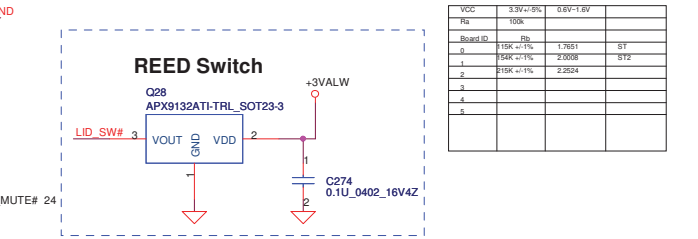
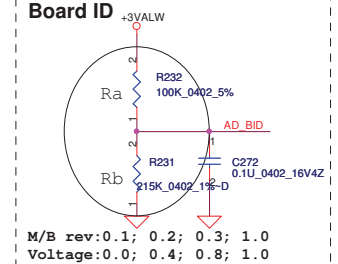
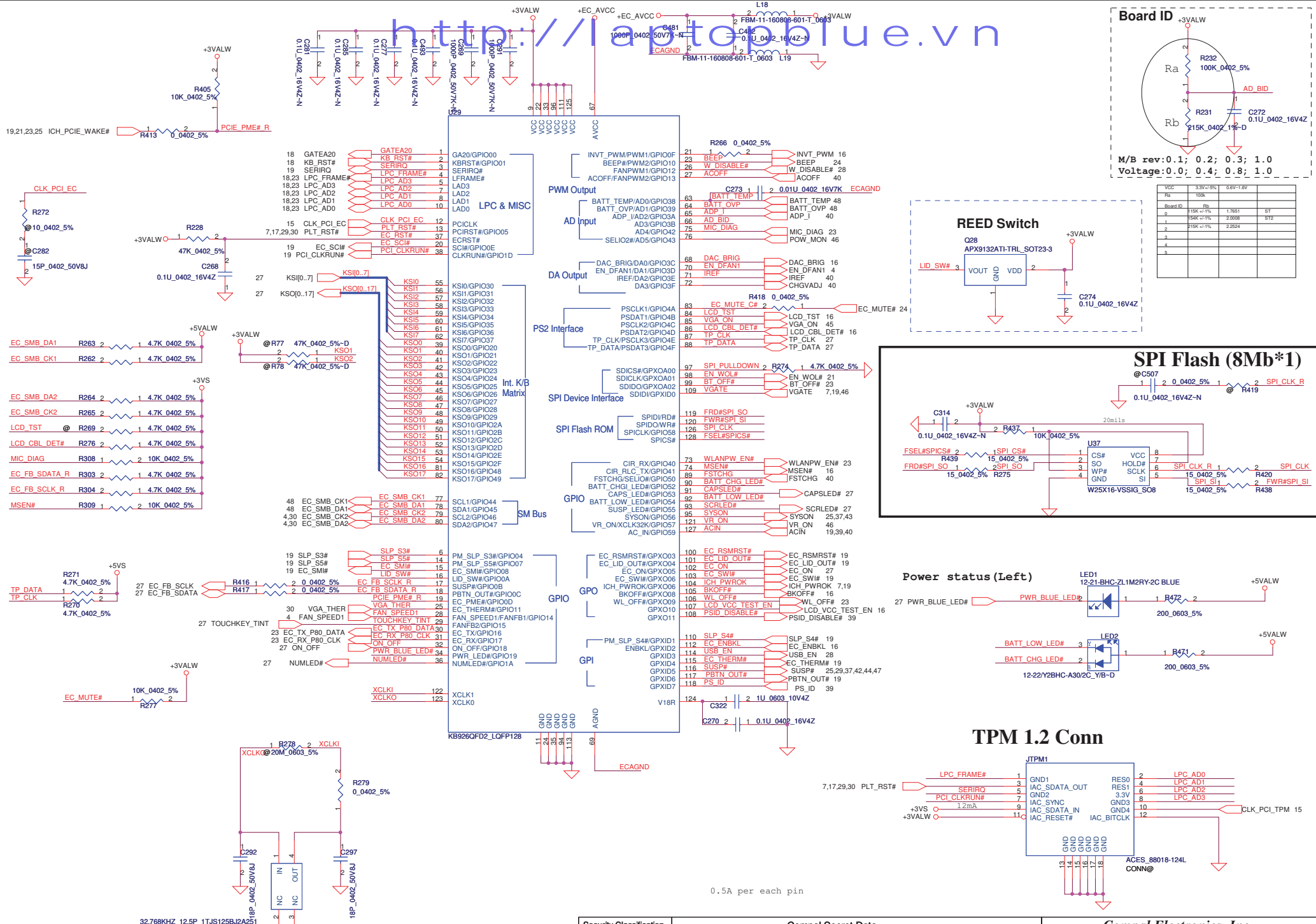


Q141~Q144 Co-Layout with Q146~Q149

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				Date:	Friday, February 20, 2009
				Sheet	24 of 53

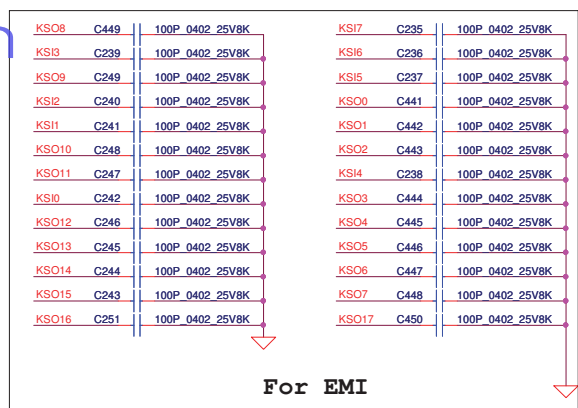
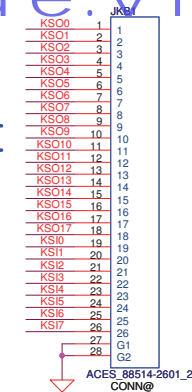
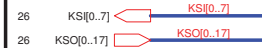
<http://laptop-motherboard.com/>



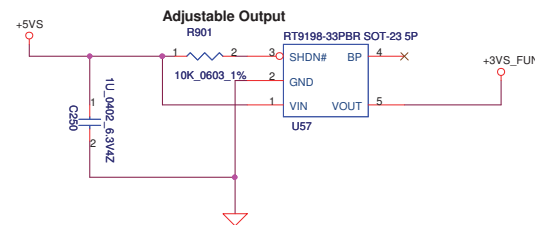
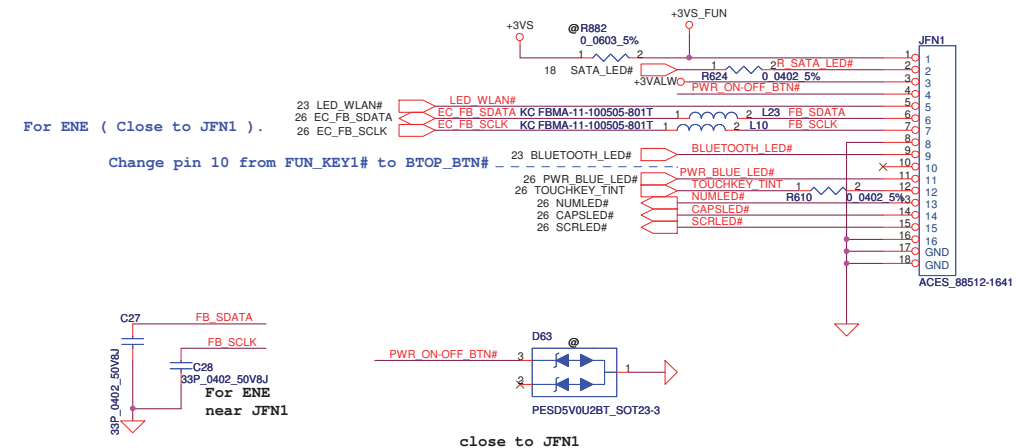


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				Custom	LA-4671P
				Date	Friday, February 20, 2009
				Sheet	26 of 53

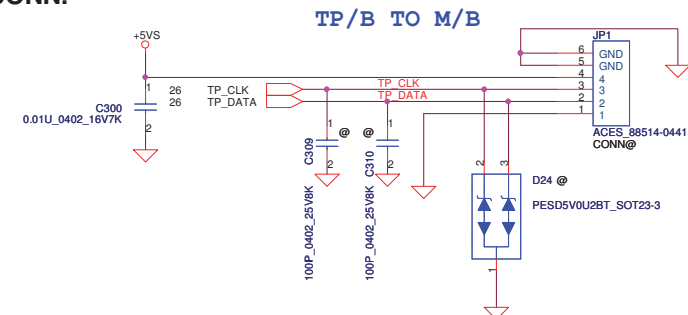
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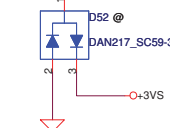
Regulator for ENE sensor

**Function/B CONN.**

Touch PAD/B CONN.



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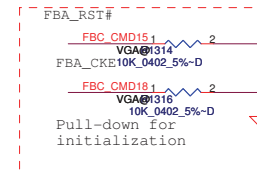
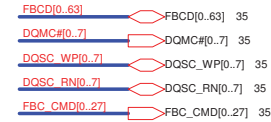


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USBC VGA@

Part 3 of 6

MEMORY
INTERFACE 2

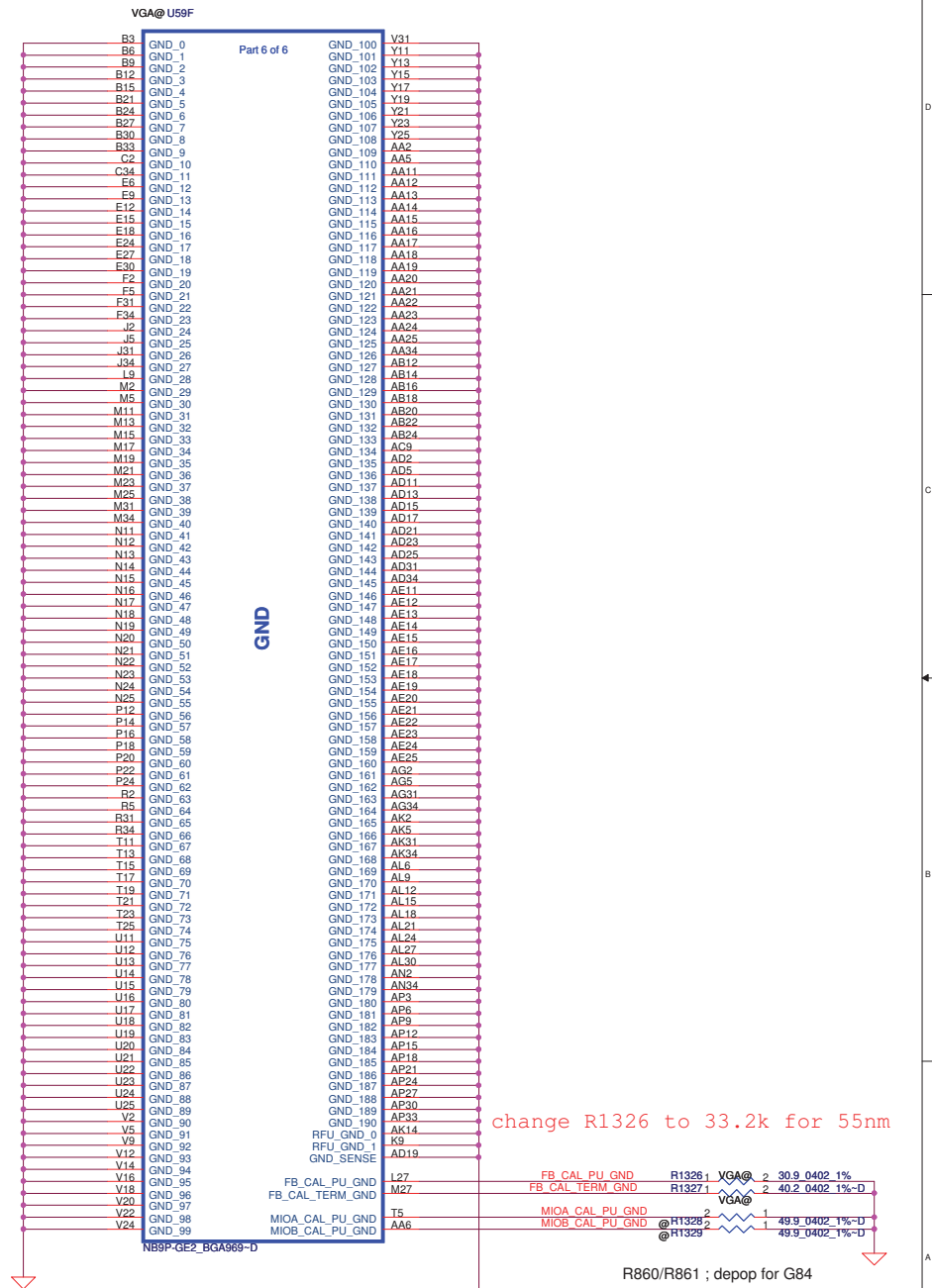
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FBCD132	F106	FBCD132	F106	FBCD132	F106	FBCD132	F106
FBCD133	F107	FBCD133	F107	FBCD133	F107	FBCD133	F107
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FBCD138	F112	FBCD138	F112	FBCD138	F112	FBCD138	F112
FBCD139	F113	FBCD139	F113	FBCD139	F113	FBCD139	F113
FBCD140	F114	FBCD140	F114	FBCD140	F114	FBCD140	F114
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FBCD172	F146	FBCD172	F146	FBCD172	F146	FBCD172	F146
FBCD173	F147	FBCD173	F147	FBCD173	F147	FBCD173	F147
FBCD17							

Date: Friday, February 20, 2009 Sheet 31 of 53

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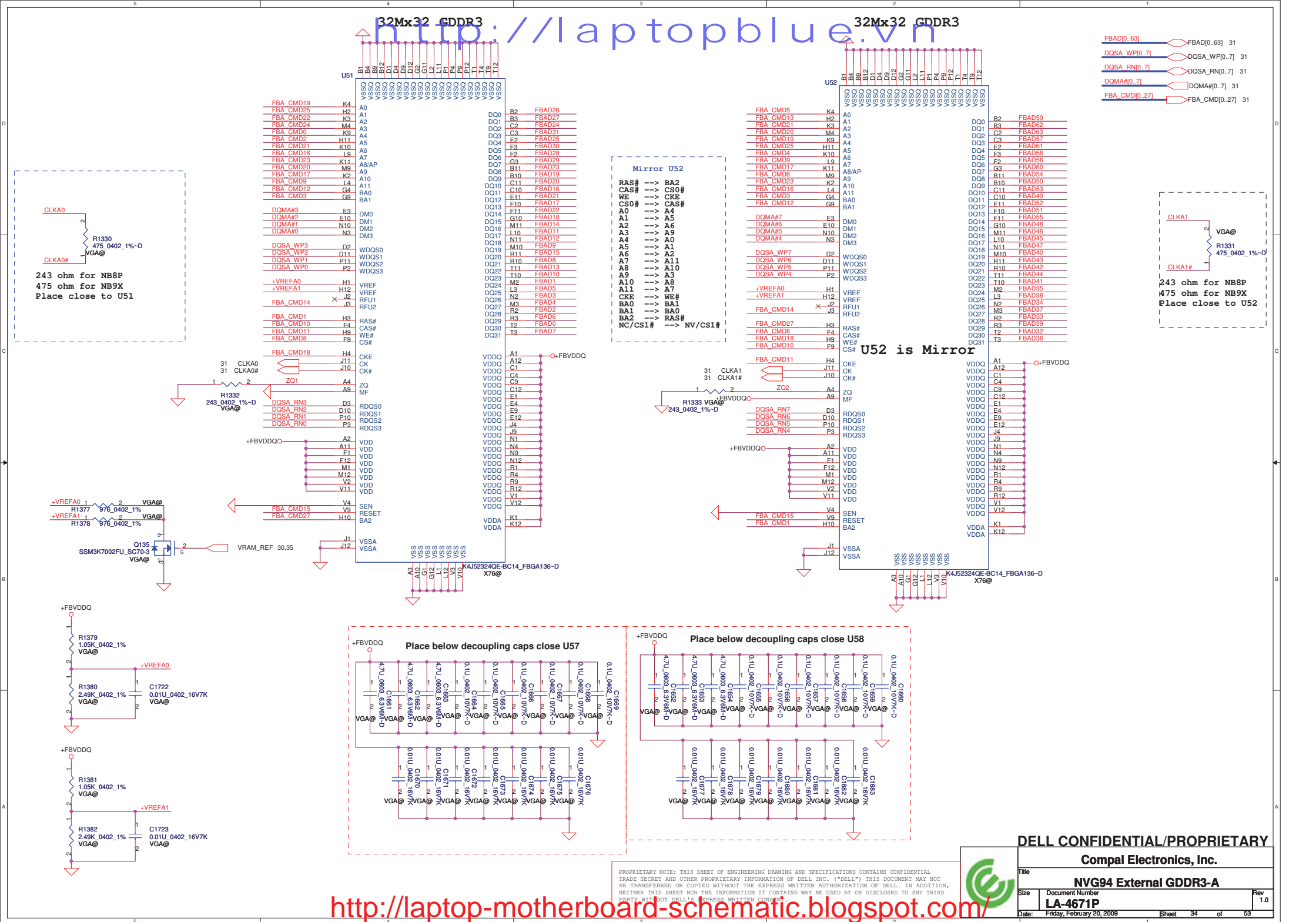
<http://laptop-motherboard-schematic.blogspot.com/>



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Size	Document Number	Rev
	IA 1671D	1.0

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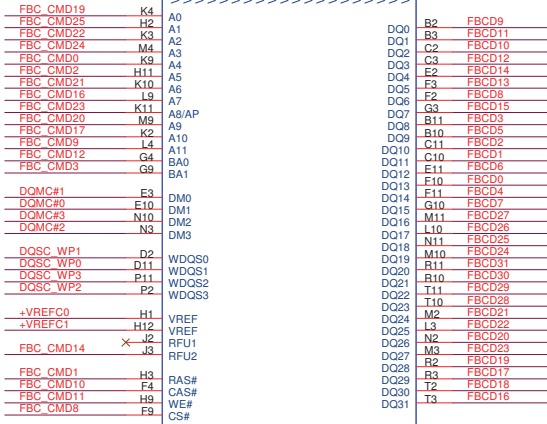


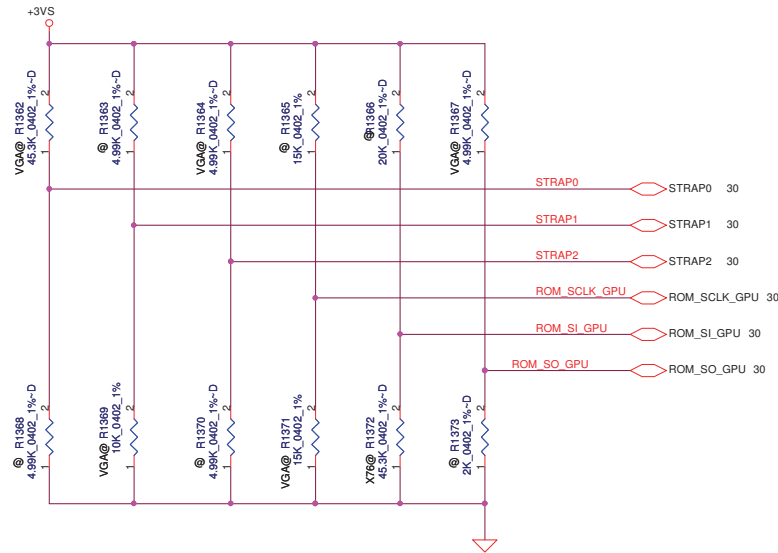
32Mx32 GDDR3

32Mx32 GDDR3

U53

U54





STRAP0	Pull up 45K
STRAP1	Pull down 10K
STRAP2	Pull up 5K
ROM_SCLK_GPU	Pull down 15K
ROM_SI_GPU	
ROM_SO_GPU	Pull up 5K

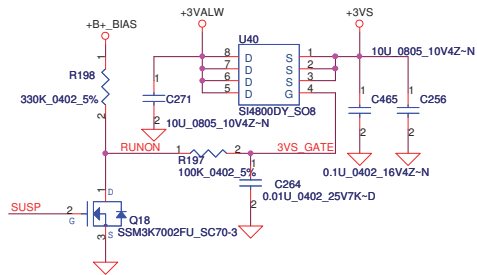
All GDDR3

ROM_SI_GPU	Pull down
Q:16x32	10K_1%
H:16x32	15K_1%
S:16x32	20K_1%
Q:32x32	30K_1%
H:32x32	35K_1%
S:32x32	45.3K_1%

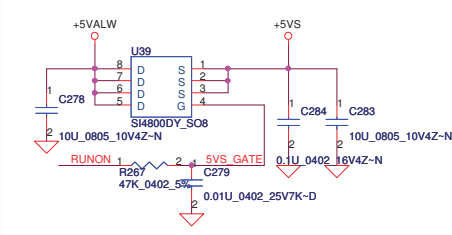
	R1364	R1365	
17"	24.9K	15K	NB9P-???



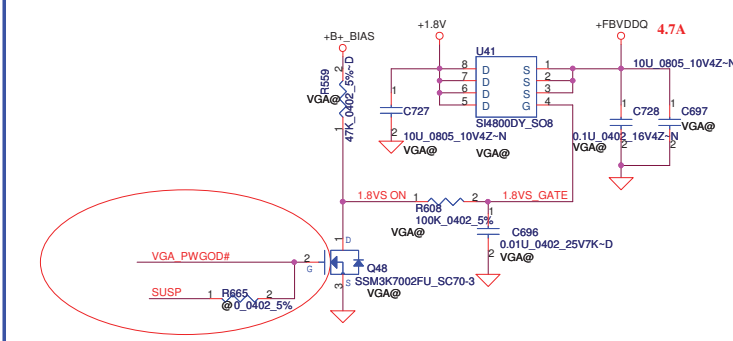
+3VALW to +3VS Transfer



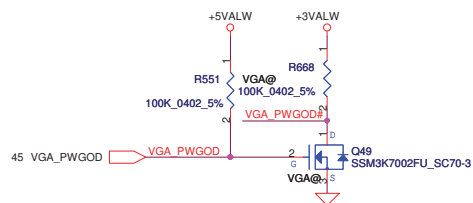
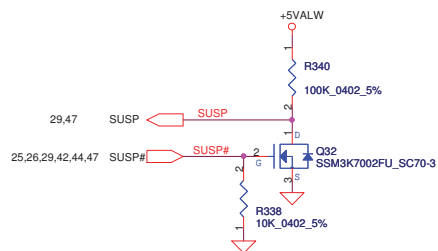
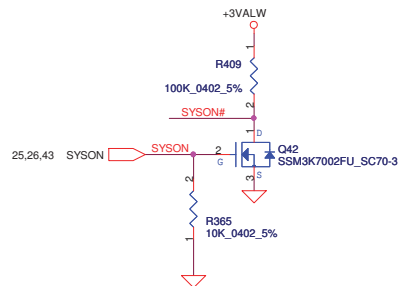
+5VALW to +5VS Transfer



+1.8V to +1.8VS Transfer

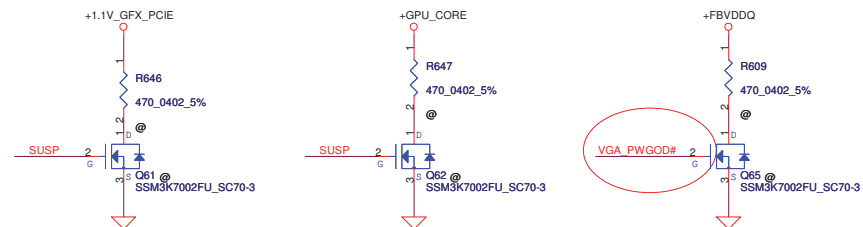


+CPU_CORE @ C211 1 2 0.1U_0402_16V4Z-N VCCP

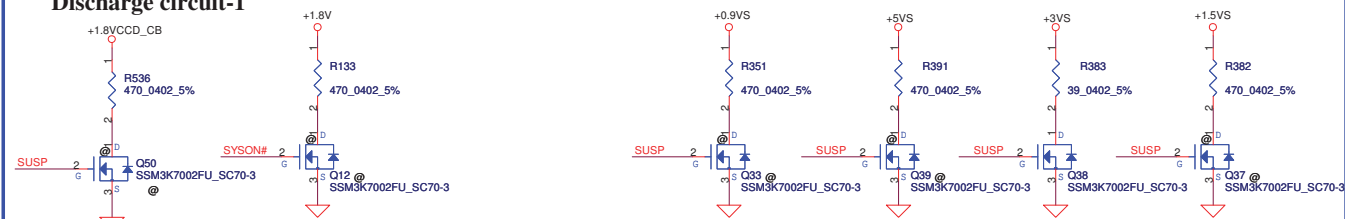


SYSON -> SUSP# -> VGA_ON->VGA_PWGOD

VGA Discharge circuit

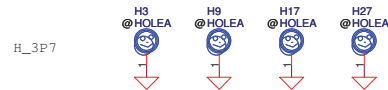
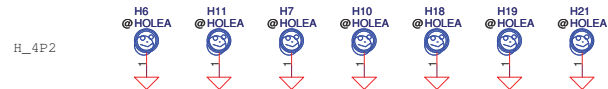
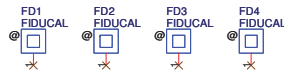


Discharge circuit-1

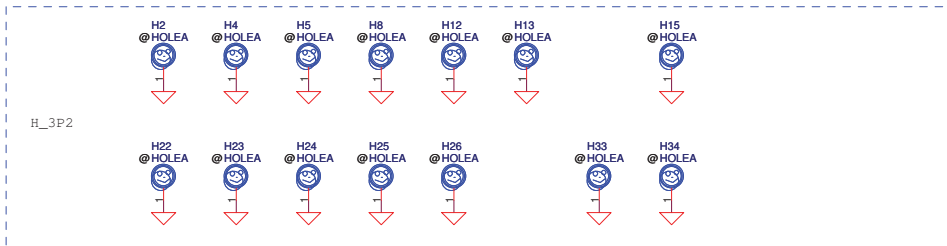


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				DC/DC Circuits			
Size		Document Number		LA-4671P		Rev	
Custm						1.0	
Date:				Friday, February 20, 2009		Sheet 37 of 53	

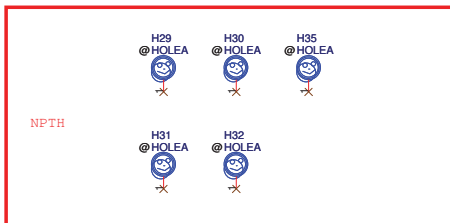
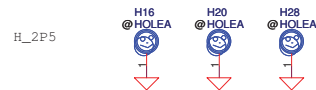
<http://laptop-motherboard.schematic.blogspot.com/>



Change Location H5 (3P2), H17 (3P7)
Add H27 (3P2)
(2008-10-31 update)

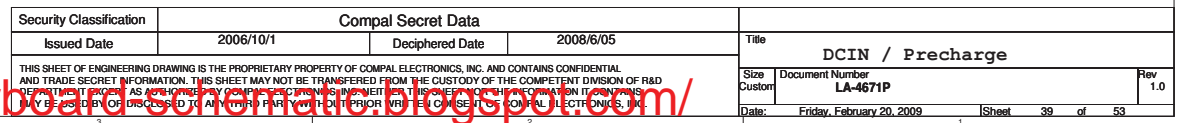


Add H34 (3P2)
(2008-11-11 update)



NPTH

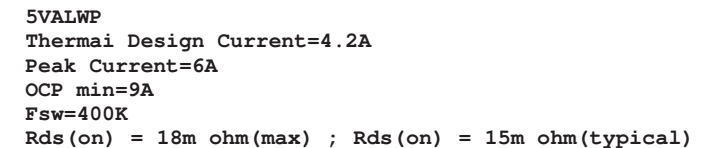
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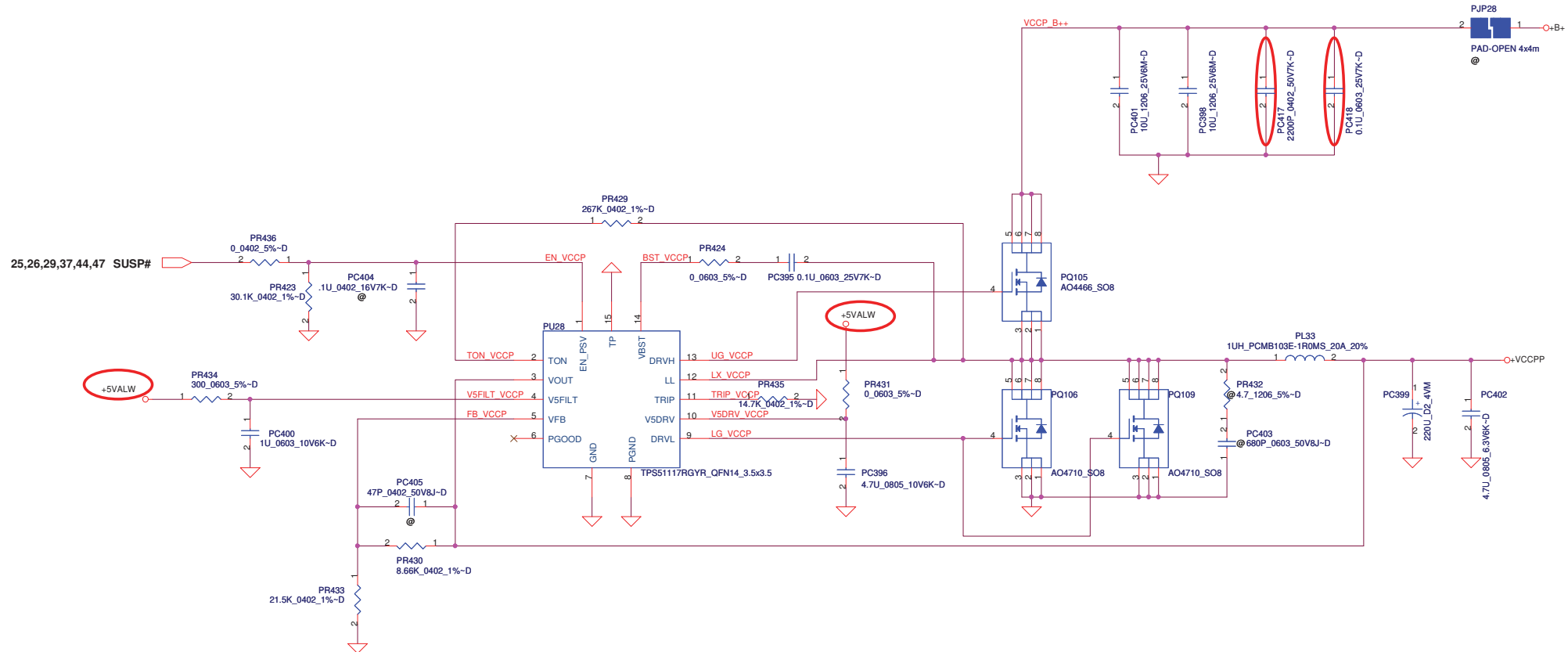


IREF	Current
2.968V	3A

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Date: Friday, February 20, 2009				Sheet	40 of 53	

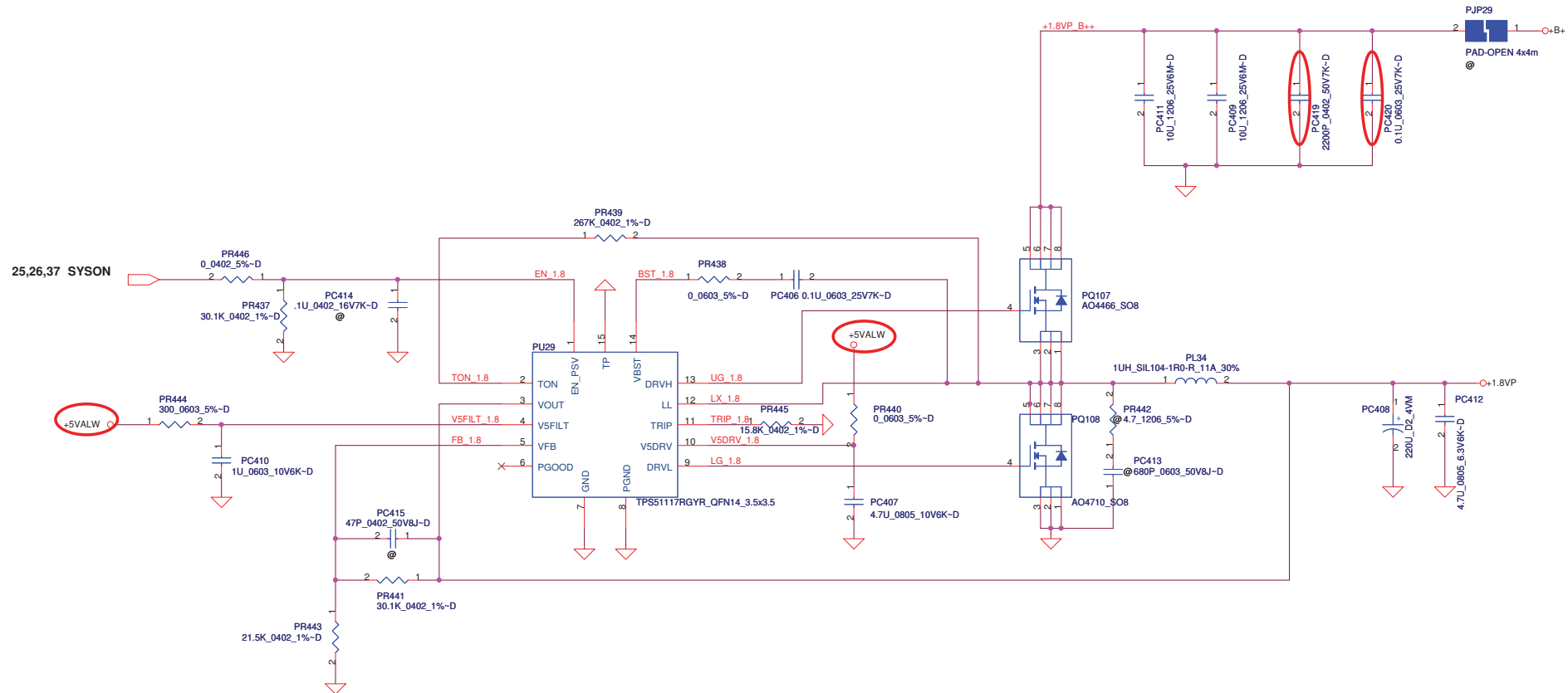


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				Customer	1.0	
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				53		



VCCP
 Thermal Desig Current=11.6A
 Peak Current=14A
 OCP min=17A
 Fsw=298KHz
 <Vo=1.05V> VFB=0.75V
 Vo=VFB*(1+PR430/PR433)=0.75*(1+8.66K/21.5K)=1.052V

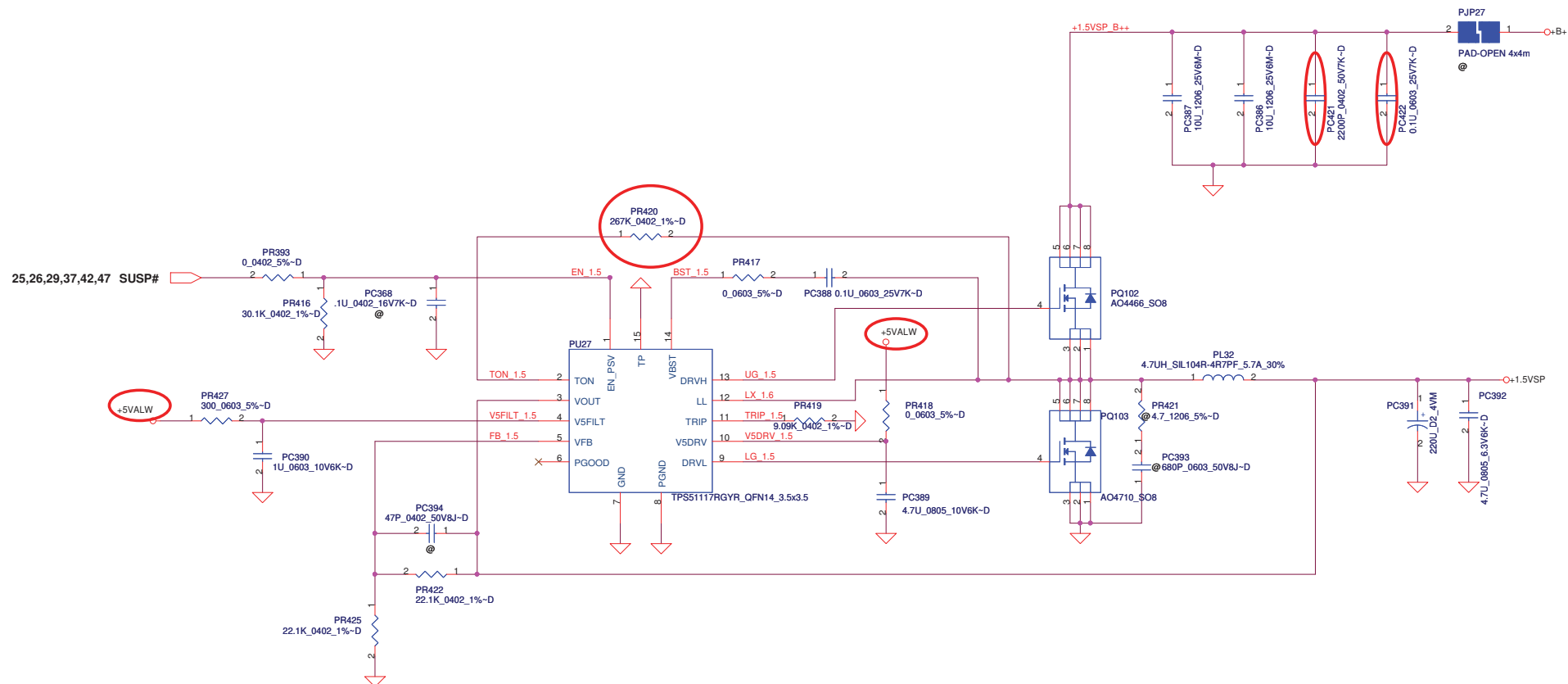
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1.8V
Thermal Design Current=6.3A
Peak Current=9A
OCP_min=12A
Fsw=297KHz

<Vo=1.8V> VFB=0.75V
 $V_o = V_{FB} * (1 + \frac{PR441}{PR443}) = 0.75 * (1 + \frac{30.1K}{21.5K}) = 1.8V$
Fsw=297KHz

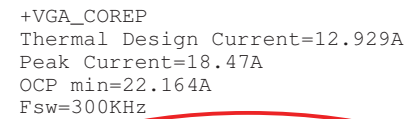
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Size		Document Number				Rev	1.0
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1.5V
Thermal Design Current=2.45A
Peak Current=3.5A
OCP min=5.25A
Fsw=298KHz

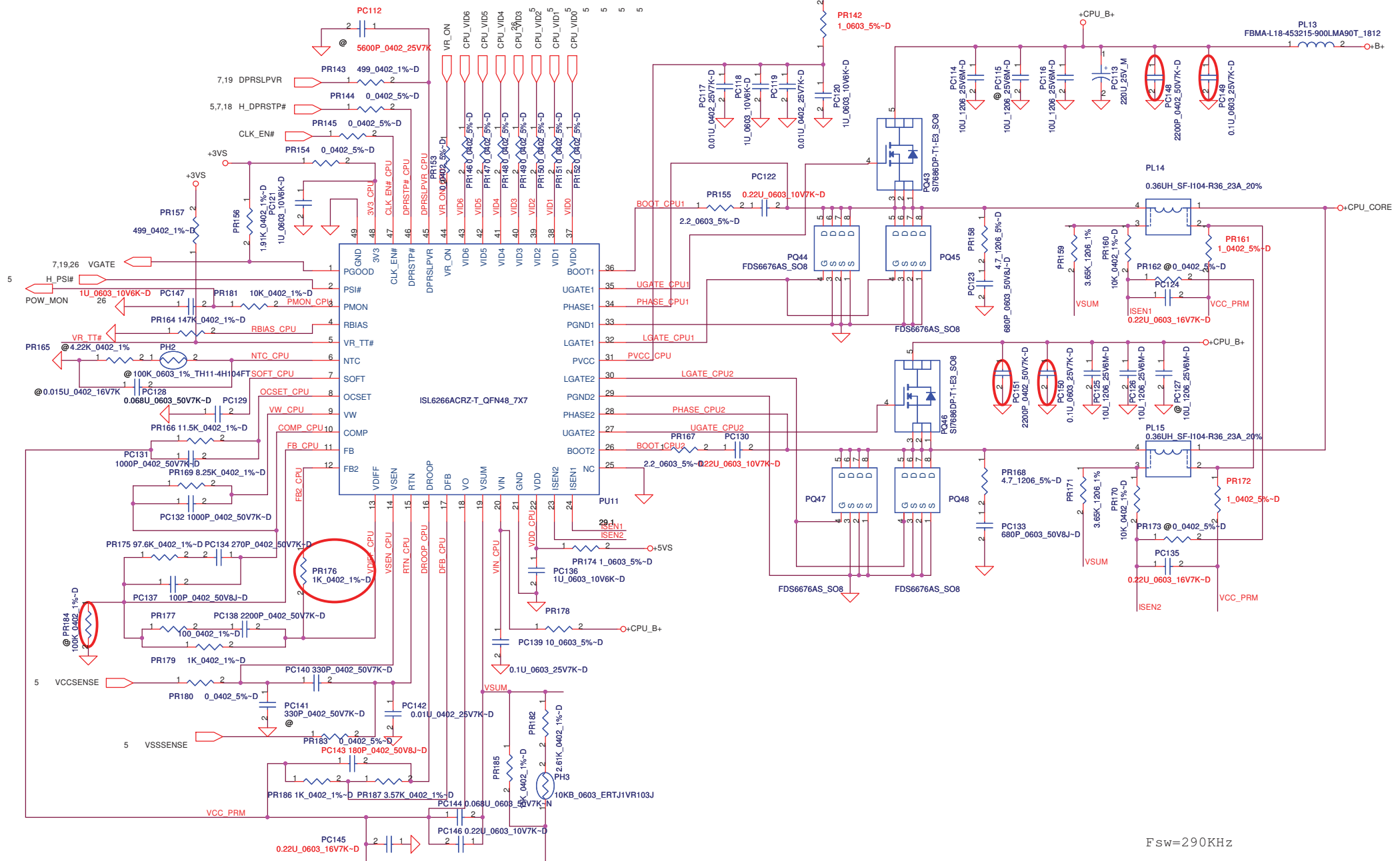
<Vo=1.5V> VFB=0.75V
 $V_o = V_{FB} * (1 + PR422 / PR425) = 0.75 * (1 + 22.1K / 22.1K) = 1.5V$

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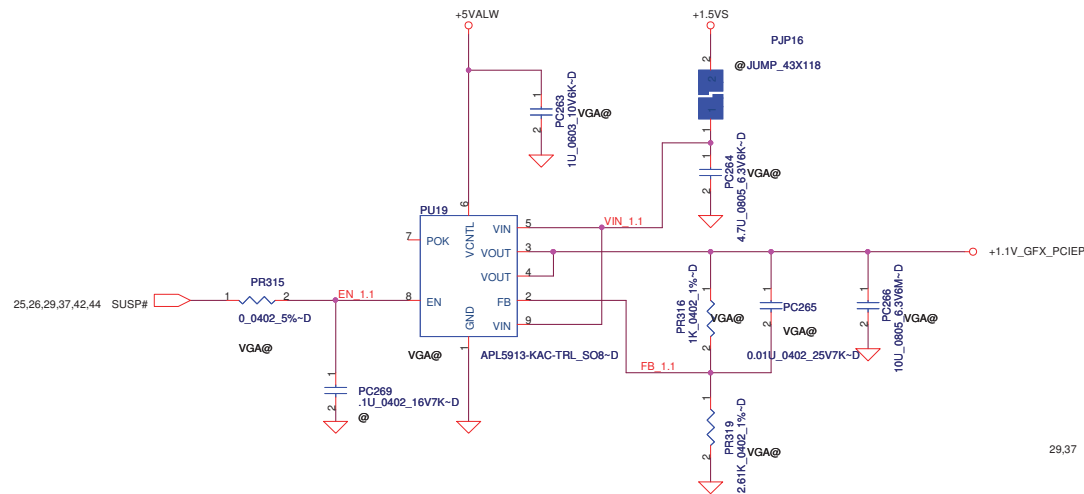
GPU_VID_0	0.89V	1.00V
	0	1

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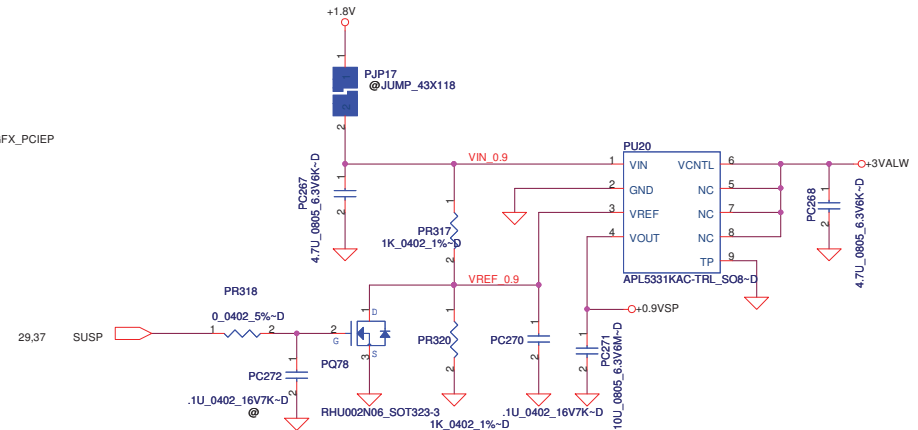


Fsw=290KHz

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				Date	Friday, February 20, 2009
				Sheet	46 of 53

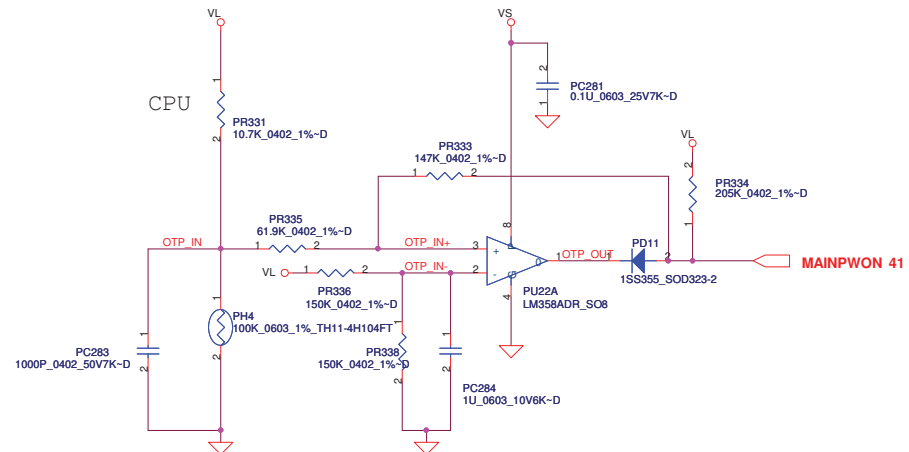
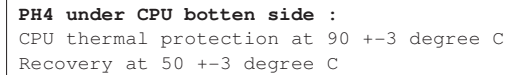



1.1V GFX_PCIEP
Thermal Design Current=1.61A
Peak Currnet=2.3A
OCP min=2.76A



0.9VSP
Thermal Design Current=0.7A
Peak Currnet=1A
OCP min=1.2A

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				+0.9VSP/ +1.1V GFX_PCIEP			
Size		Document Number		Rev		1.0	
Customer		LA-4671P					
Date:		Friday, February 20, 2009		Sheet		47 of 53	



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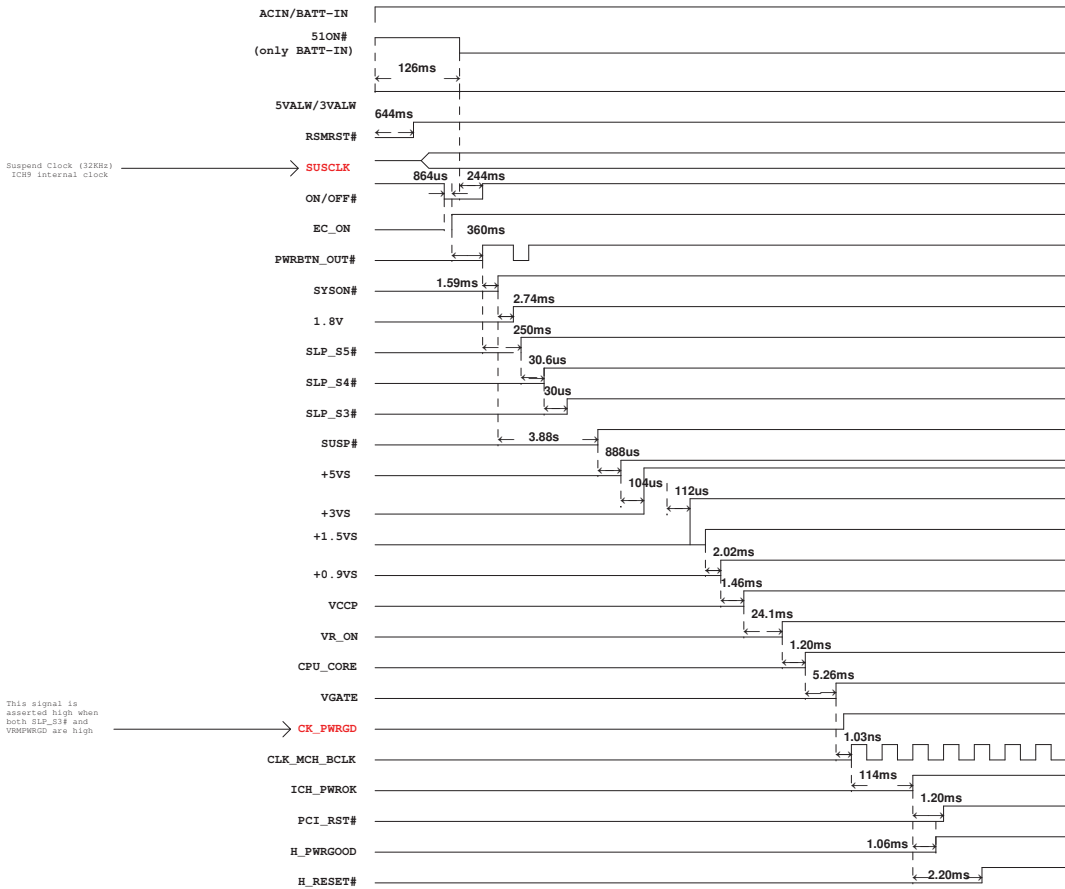
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	40	DCIN/Precharge	08/12/17	COMPAL	Common circuit design modify	add PC290,PC291 between ADPIN and GND	
2			08/12/17	COMPAL	Common circuit design modify	add PR204 between VS and PD3.1	
3	41	Charger	08/12/17	COMPAL	Common circuit design modify	add PR262 between +3VALW and PU15.11	
4			08/12/17	COMPAL	Common circuit design modify	reserve PR261 between PU15.10 and PU15.11	
5			08/12/17	COMPAL	Common circuit design modify	change PR224.1 POWER source from VREF into +3VALW	
6	42	+3VALWP,+5VALWP	08/12/17	COMPAL	Common circuit design modify	add PC216,PC217 between TP951427+B+ and GND	
7			08/12/17	COMPAL	Wrong net name issue	change PU16.1 net name from 2VREF_ISL6237 to 2VREF_TP951427	
8	44	+1.8VP	08/12/17	COMPAL	+1.8V no power issue in S3 mode	change PR440.1,PR444.1 POWER source from +5VS to +5VALW	
9			08/12/17	COMPAL	Common circuit design modify	add PC419,PC420 between +1.8VP_B++ and GND	
10	46	+VGA_COREP	08/12/17	COMPAL	Common circuit design modify	add PC423,PC424 between VGA_B++ and GND	
11			08/12/17	COMPAL	Change VID require	change PR410 to 5.62K ohm	
12			08/12/17	COMPAL	Change VID require	reserve PQ100,PR406,PC382,PR408,PC384,PR413,PR411,PR409	
13			08/12/17	COMPAL	Common circuit design modify	change PR409.2,PR412.2 POWER source from +5VS to +3VS	
14			08/12/17	COMPAL	Common circuit design modify	change 396.1 POWER source from +5VS to +5ALW	
15	43	+VCCP	08/12/17	COMPAL	Common circuit design modify	add PC417,PC418 between VCCP_B++ and GND	
16			08/12/17	COMPAL	Common circuit design modify	change PR434.1,PR431.1 POWER source from +5VS to +5ALW	
17	45	+1.5VSP	08/12/17	COMPAL	Common circuit design modify	add PC421,PC422 between +1.5VSP_B++ and GND	
18			08/12/17	COMPAL	Common circuit design modify	change PR427.1,PR418.1 POWER source from +5VS to +5ALW	
19	47	+CPU_CORE	08/12/17	COMPAL	Common circuit design modify	add PC148,PC149,PC150,PC151 between +CPU_B+ and GND	
20			08/12/17	COMPAL	Common circuit design modify	add PR176 between PU11.12 and PU11.13	
21			08/12/17	COMPAL	Common circuit design modify	reserve PR184 between PU11.11 and GND	
22	48	+VGA_COREP	08/12/22	COMPAL	Change VID require	change PR410 to 8.45K ohm	
23			08/12/22	COMPAL	Relink data base	Relink data base for PQ98	
24							
25							

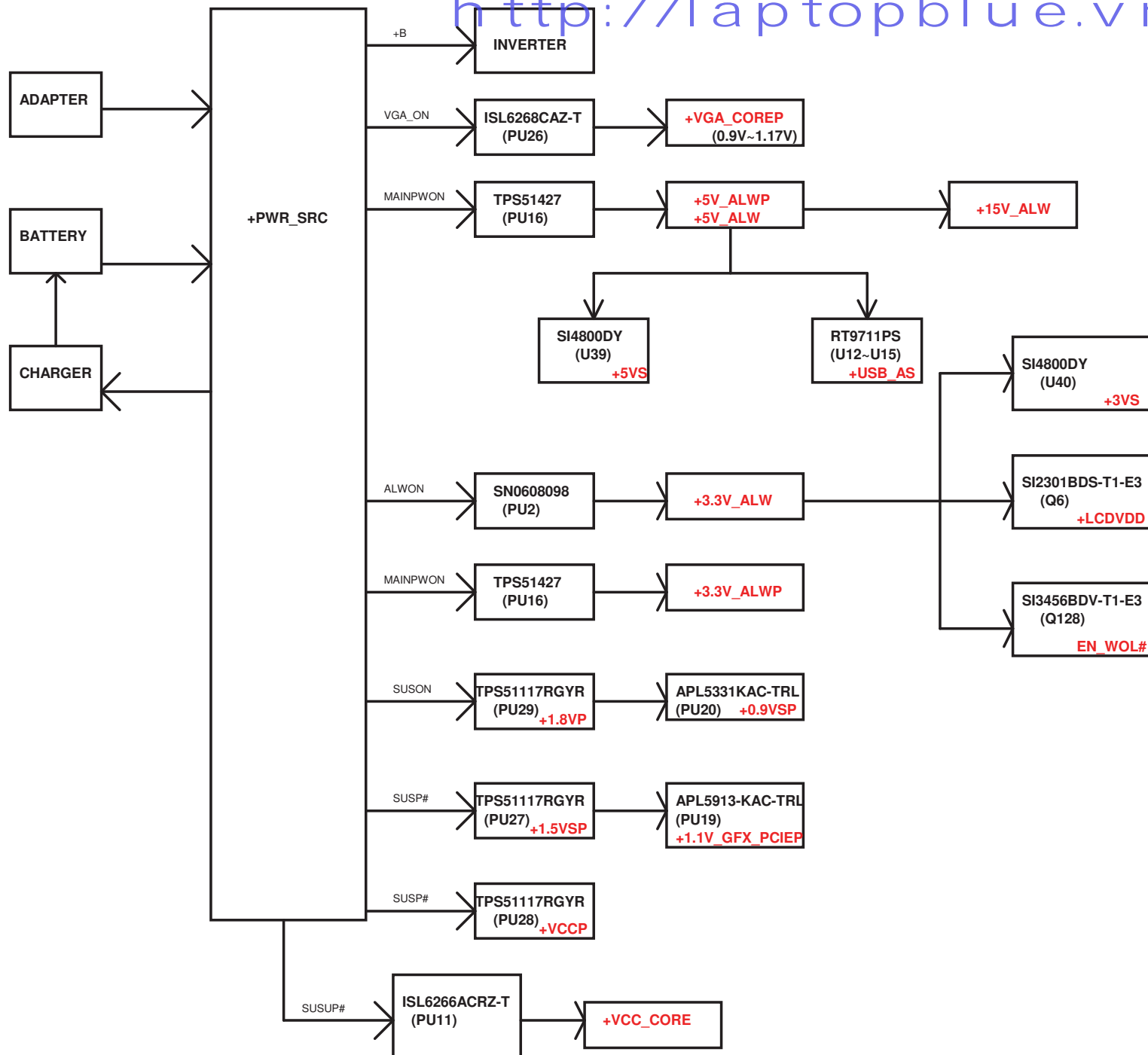
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P10	Cantiga(4/6)-PWR	12/15/2008	EE	DIS can not boot issue	a. change L13 L14 BOM structure from "UMA#" to "g" b. change R1400 R1401 BOM structure to "UMA#"	X02
2	P17	ICH9(1/4)-PCI/INT	12/15/2008	EE	PCI reset and PLT reset connect error	change R1112 pin 1 net name from PLT_RST# to PCI_RST#	X02
3	P24	Codec 92HD81B	12/15/2008	EE	Internal MIC no function issue	add a 2.49K ohm pull high resistor (R315) to +5VS at SENSE_A	X02
4	P27	PWR_OK/BTN/TP	12/15/2008	EE	CAP sensor no function issue	SWAP JFN1 pin 6 and pin 7 signals	X02
5	P27	PWR_OK/BTN/TP	12/15/2008	EE	Battery only can not boot issue	The breakdown voltage of D63 is too low now. Change D63 back to old part.	X02
6	P19	ICH9(3/4)_DMI,USB,GPIO,PCIE	12/15/2008	EE	part change to consistent with 13" and 15"	Change Q106 to SSM3K7002FU_SC70-3 and add Q107	X02
7	P26	BIOS & EC I/O Port	12/15/2008	EE	Add wake on LAN feature	change PCIE wake up signal connection to support wake up on LAN/WLAN feature.	X02
8	P23	WLAN/BT/FP	12/16/2008	EE	WLAN card S3/S4 resume fail issue and add wake on LAN function	Add Q129 and net WLANPW_DIS# to switch +3V_WLAN power from +3VALW unpop R412, R415	X02
9	P10	Cantiga(4/6)-PWR	12/16/2008	EE	follow 13"/15" design	change R101 from 0603 to 0805 size	X02
10	P26	BIOS & EC I/O Port	12/16/2008	EE	follow 13"/15" design	unpop R77 R78	X02
11	P21	Gigabit LAN_RTL8111DL	12/16/2008	EE	follow 13"/15" design	Change C1484, C1485 from 0.1uF to 1uF	X02
12	P10	Cantiga(4/6)-PWR	12/16/2008	EE		change R69 to L15	X02
13	P24	Codec 92HD81B	12/16/2008	EE	vendor (IDT) request	unpop C260 C262	X02
14	P22	HDD/CDROM	12/17/2008	ME	For ODD CONN SMT issue	Change part of JSATA2	X02
15	P34 P35	NVG94 External GDDR3	12/17/2008	EE		Change Q135 Q136 to SSM3K7002FU_SC70-3	X02
16	P29	OZ129_Card Reader / 1394	12/19/2008	EE	For Card Reader / 1394 issue	add a LDO (U65) for +1.8VS_CB	X02
17	P16	CRT CONN/LCD CONN	12/19/2008	EE	U29 pin 21 (INVT_PWM) broken issue	add a ESD diode(D51) to INVT_PWM close to JLCD1	X02
18	P29	OZ129_Card Reader / 1394	12/19/2008	EE	crystal vendor suggestion	change X3 bypass CAP. C1781 C1785 from 15pF to 18pF	X02
19	P21	Gigabit LAN_RTL8111DL	12/19/2008	EE	crystal vendor suggestion	change Y9 from CL=20pF to CL=12pF change C1488=18pF, C1489=15pF	X02
20	P7	Cantiga(1/6)-AGTL/DMI/DDR	12/22/2008	EE	13"/15" system hang with some special CPUs issue	Reserve 0.1uF Cap. C141 at H_DPRSTP# close to MCH	X02
21	P38	Screws	12/22/2008	ME	ME change ODD connector and change screw holes	remove H14	X02
22	P07~P12	GMCH	12/22/2008	EE	GMCH revision change	change GMCH from A1 version to B3	X02
23	P18	ICH9(2/4)_LAN,HD,IDE,LPC	12/23/2008	EE	crystal vendor suggestion	change C1211 from 15pF to 12pF	X02
24	P23	WLAN/BT/FP	12/23/2008	EE	ESD team request	change D22, D62 to SC300000000	X02
25	P24	Codec 92HD81B	12/23/2008	EE	ESD team request	change D19, D20, D21, D27 to SCA00000T00	X02
26	P27	PWR_OK/BTN/TP	12/23/2008	EE	ESD team request	change D63 D24 to SC3000000000	X02
27	P28	USB/ESATA/1394 CONN	12/23/2008	EE	ESD team request	change D58 D59 D60 to SC3000000000	X02
28	P27	PWR_OK/BTN/TP	12/23/2008	EE	ESD team request	change L10, L23 from 301T to 801T pop C27, C28	X02
29	P23	WLAN/BT/FP	12/23/2008	EE	ESD team request	add a 1000pF cap C414 at +3VS close to JCA1	X02
30	P28	USB/ESATA/1394 CONN	12/24/2008	EE	follow 13"/15" schematic	change R155 R1257 R1262 R1267 from 30K to 470 ohm un-pop R1255 R1260 R1264 R1269	X02
31	P29	OZ129_Card Reader / 1394	01/05/2009	EE	customer suggestion	change LDO output to 1.95V	X02
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KAL60 POWER UP SEQUENCE





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