Winery CALPELLA N11M-GE Schematics

Mobile Arrandale

Intel Ibex Peak-M

2010-01-18

REV : X-build

DY : Nopop Component

UMA : Pop when schematic is UMA
DIS : Pop when schematic is DIS

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Cover Page***	
Size: Custom	Document Number: ***Vostro Calpella***	Rev: ***X01***
Date: Monday, January 18, 2010	Sheet 1 of 91	

Winery CALPELLA Block Diagram

Project code : 91.4ES01.001
Part Number : 48.4ES11.0SB
PCB P/N : 09297
Revision : SA

PCB LAYER

L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

Clock Generator
SLG8SP585 7

Intel CPU
Arrandale
8,9,10,11,12,13,14

DDRIII 1066 Channel A
800/1066MHz
DDRIII 1066 Slot 0 18

DDR III 1066 Channel B
800/1066MHz
DDRIII 1066 Slot 1 19

VRAM(gDDR3)
64Mbx16x4 (512MB) 84,85

VRAM

Nvidia
N11M-GE(40nm)
80,81,82,83

100MHz/
2.5Gbps
PCIe x 16
Bandwidth
:8GB

Power SW
TPS2231R

New Card
(On daughter board)

PCIE x 1 & USB 2.0 x 1

HDMI 57
CRT 55
LCD 54

HDMI
LVDS
RGB CRT

Switchable 74
Switchable 74

10/100/1000LOM
RTL8111DL 35
(On daughter board)

RJ45 CONN 61

PCIE x 1

DMIx4
2.5 GT/s

FDI(UMA)
2.7 GT/s

Mini-Card
802.11a/b/g/n 65

Mini-Card
WWAN/ WiMAX 64

USB 2.0 x 1
PCIE x 1

Intel
PCH

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
20,21,22,23,24,25,26,27,28

PCIE
100MHz
2.5Gbps
USB 2.0
480Mbps

Touch Panel
(only for 15") 76

Left Side:
USB x 2
76

Right Side:
USB x 1
63

CAMERA 73

Bluetooth 73

Biometric 78

USB 2.0 x 1
USB 2.0 x 2

CardReader
Realtek
RTS5138

(8 in 1)SD/MMC
MS/MS Pro/xD

USB 2.0
480Mbps

(On daughter board)

SM Bus
400KHz

Free fall sensor 40

LPC Bus
33MHz

TPM
(only for 15") 76
(On daughter board)

Digital Mic Array

MIC IN
HP OUT
(On daughter board)

Azalia
CODEC
OP AMP
IDT
92HD81 30

AZALIA
24MHz

KBC
NUVOTON
NPCE781BA0DX 37

SPI
SM Bus

SATA,USB
SATA 3Gbps
SPI

Flash ROM
256kB 62

Touch PAD 68

Int. KB 68

Thermal & Fan
EMC2102 39,58

Capacity Board
(On daughter board)

2CH SPEAKER
60

USB,ESATA
Multi-Port x1
63

ODD
HDD 59

Flash ROM
4MB 62

CPU DC/DC
ISL62883 47,48

INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC
TPS51125 46

INPUTS	OUTPUTS
+PWR_SRC	+15V_ALW +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC
TPS51116 50

INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_MCH_REF

SYSTEM DC/DC
ADP3211 53

INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFXCORE

SYSTEM DC/DC
TPS51218 86

INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE

CHARGER
BQ24745

INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC
TPS51218 49

INPUTS	OUTPUTS
+PWR_SRC	VTT_CORE

LDO
APL5930 51

INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN

LDO
RT9025 87

INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN_GPU

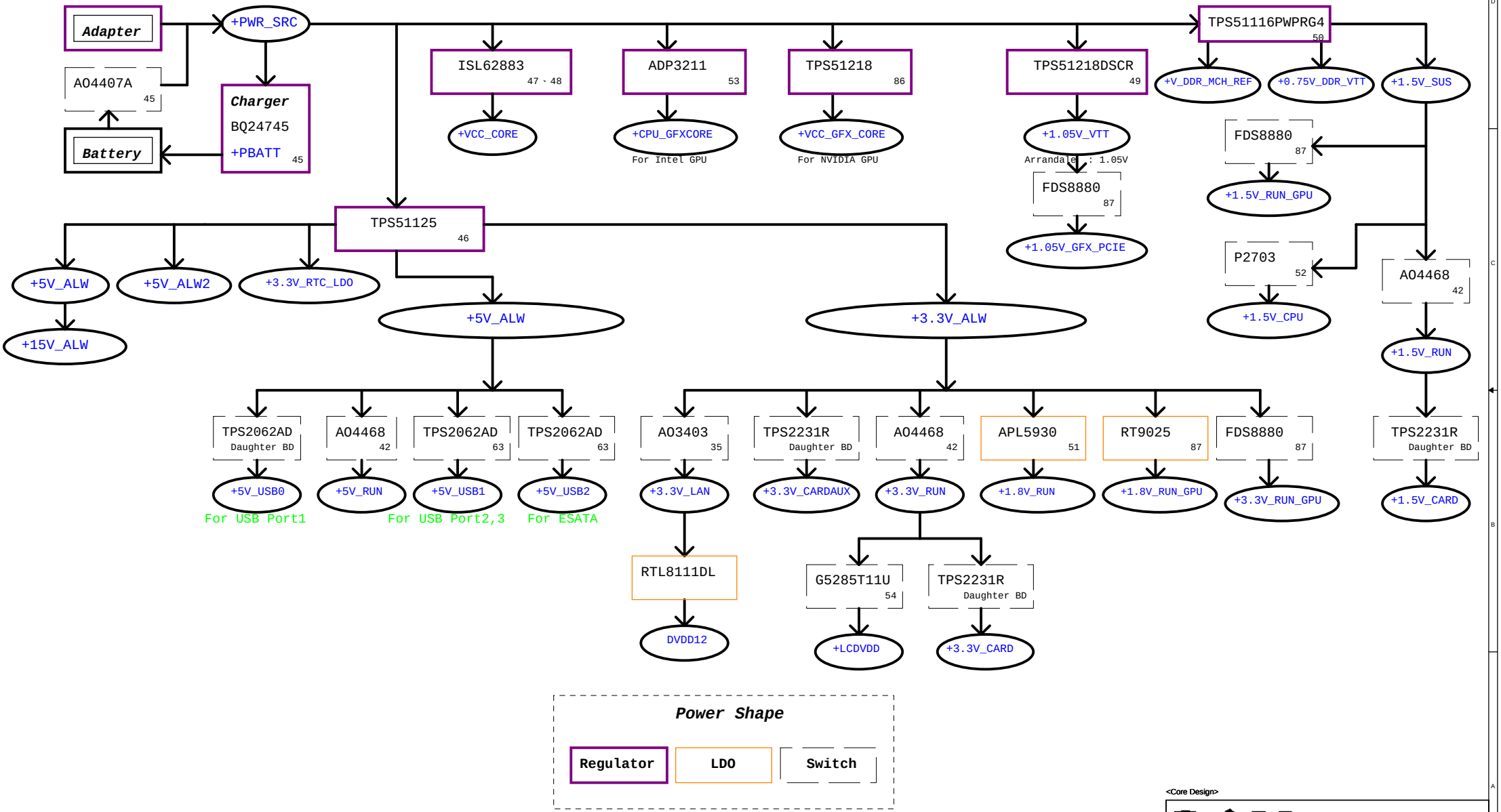
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 2 of 91



<Core Design>

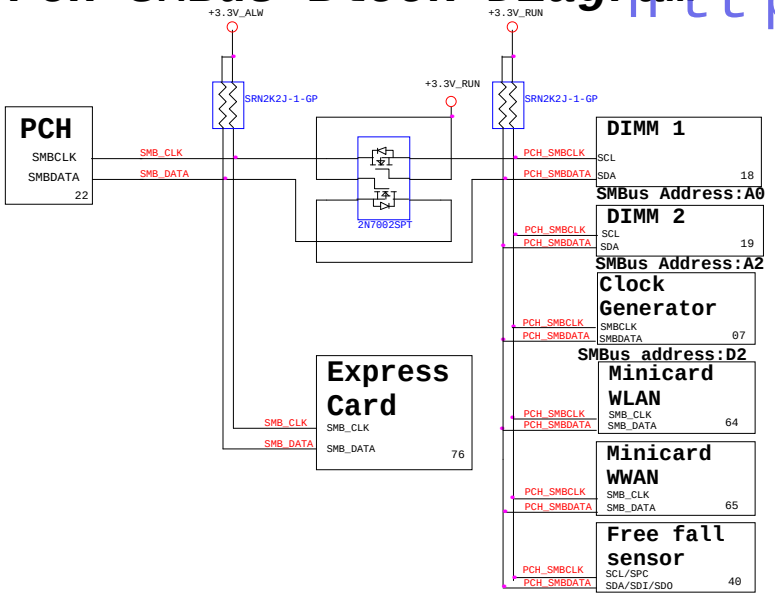
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

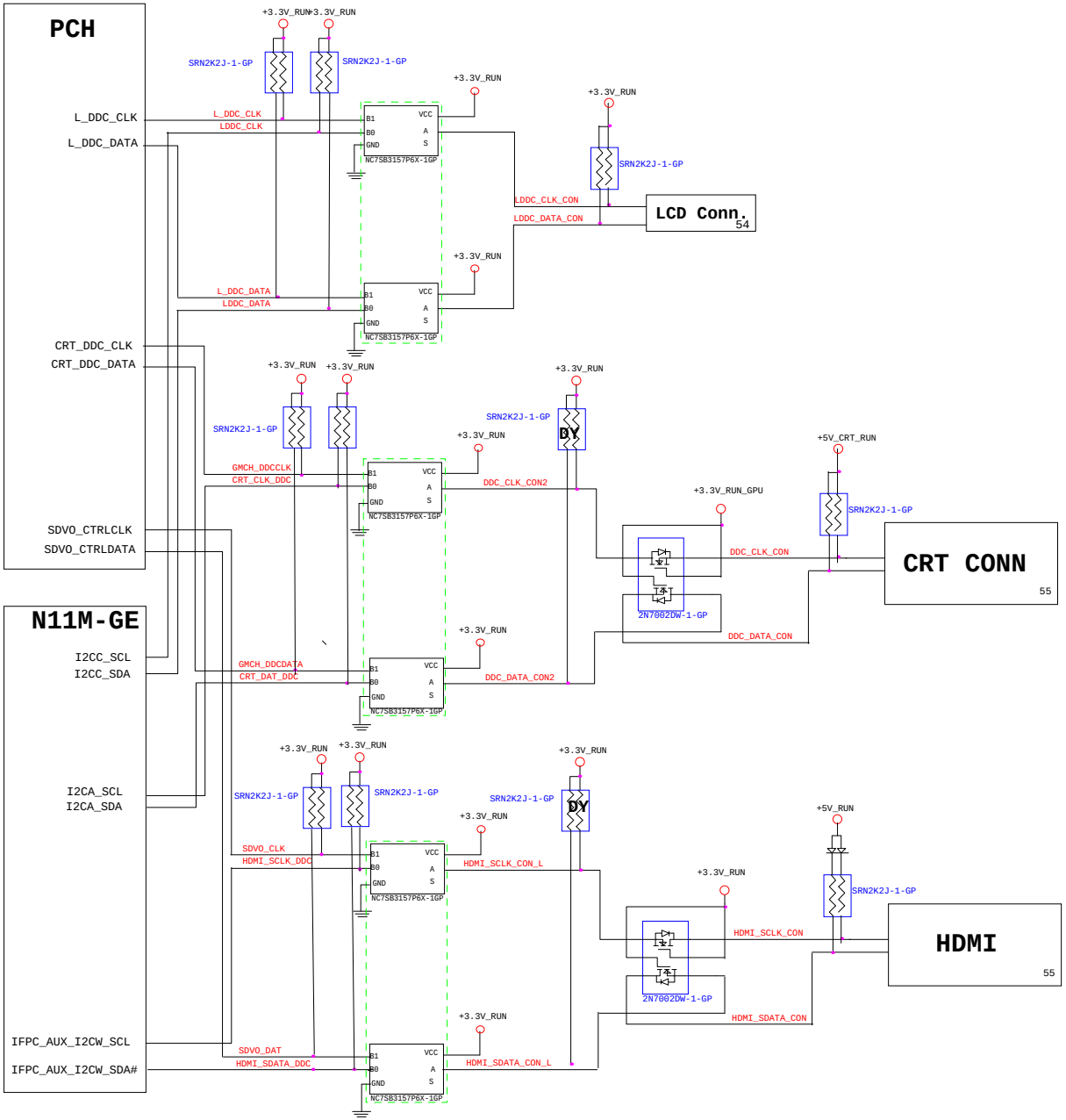
Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 3 of 91

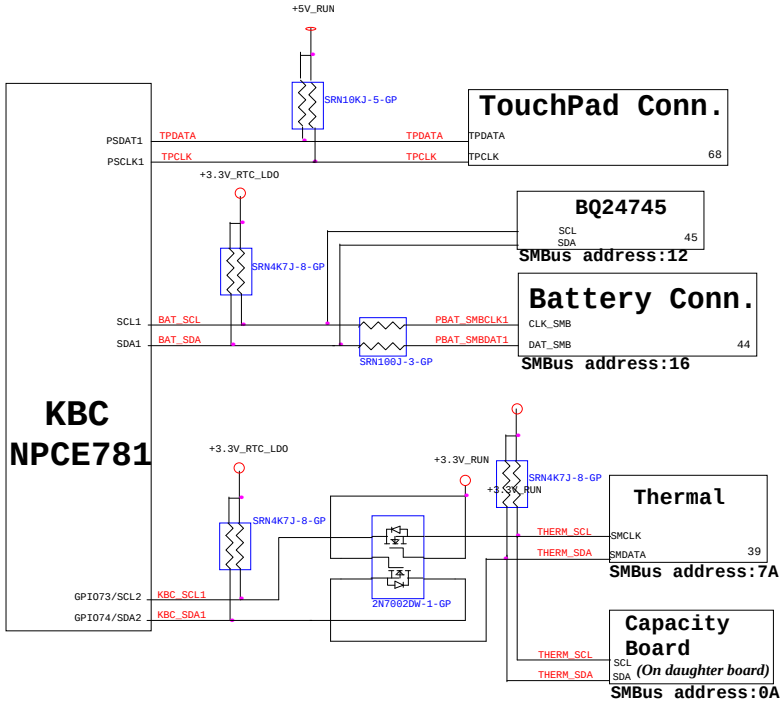
PCH SMBus Block Diagram



Switchable Graphic SMBus Block Diagram



KBC SMBus Block Diagram

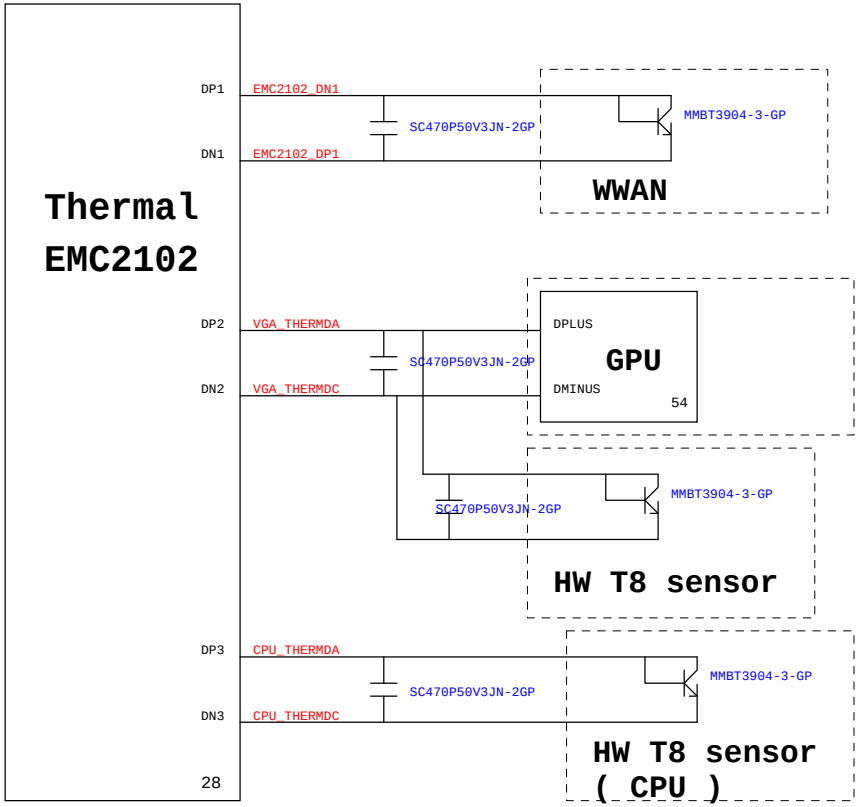


<Core Design>

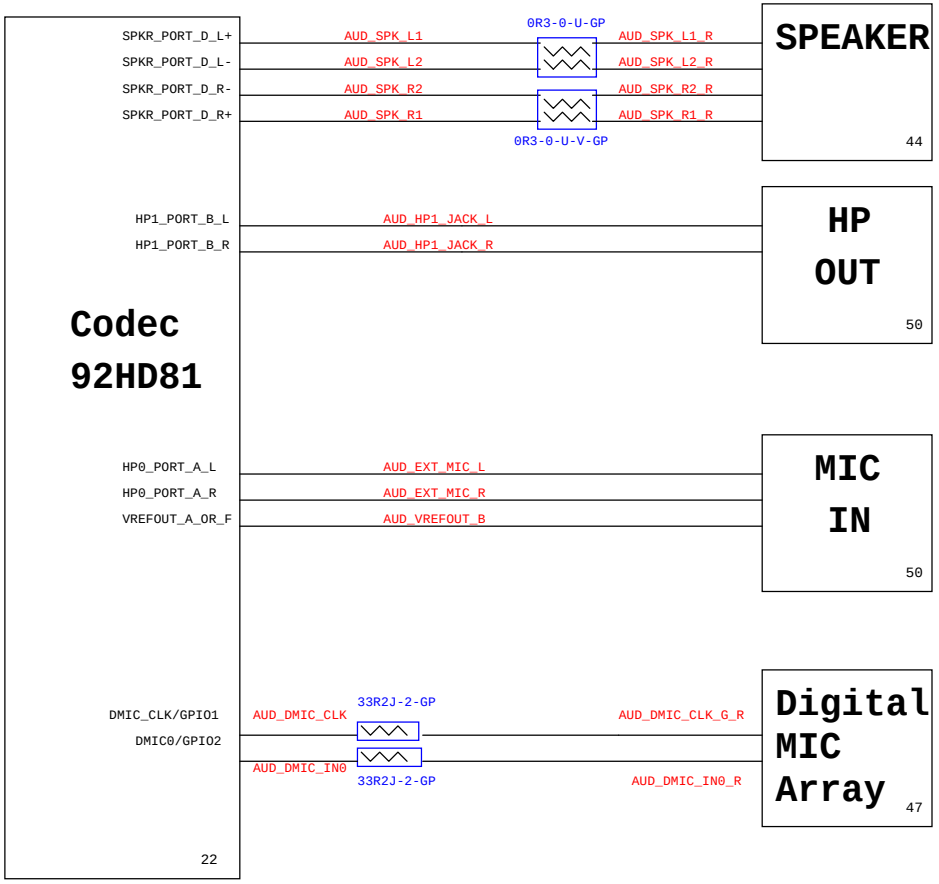
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram
Size: C
Document Number: Vostro Calpella
Rev: X01
Date: Monday, January 18, 2010
Sheet 4 of 91

Thermal Block Diagram



Audio Block Diagram



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
Custom	Vostro Calpella	X01

Date: Monday, January 18, 2010 Sheet 5 of 91

PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode**Note: Connect to ground with 4.7-k? weak pull-down resistor. CRB uses a 1 k do not stuff resistor
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#/GPIO51	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE1	Card reader
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	MiniCard WWAN
LANE5	New Card

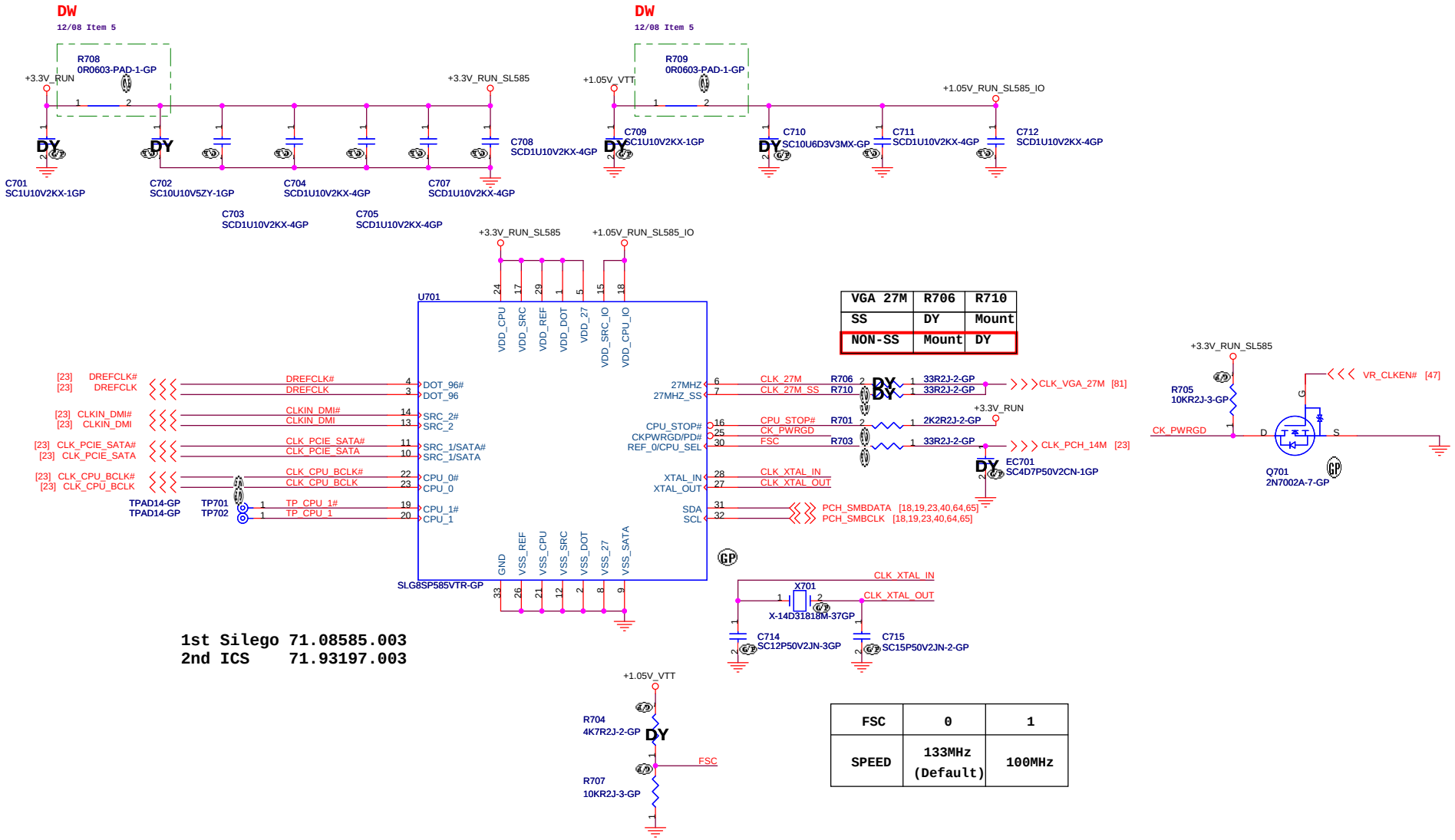
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Table of Content

Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 6 of 91



VGA 27M	R706	R710
SS	DY	Mount
NON-SS	Mount	DY

FSC	0	1
SPEED	133MHz (Default)	100MHz

1st Silego 71.08585.003
2nd ICS 71.93197.003

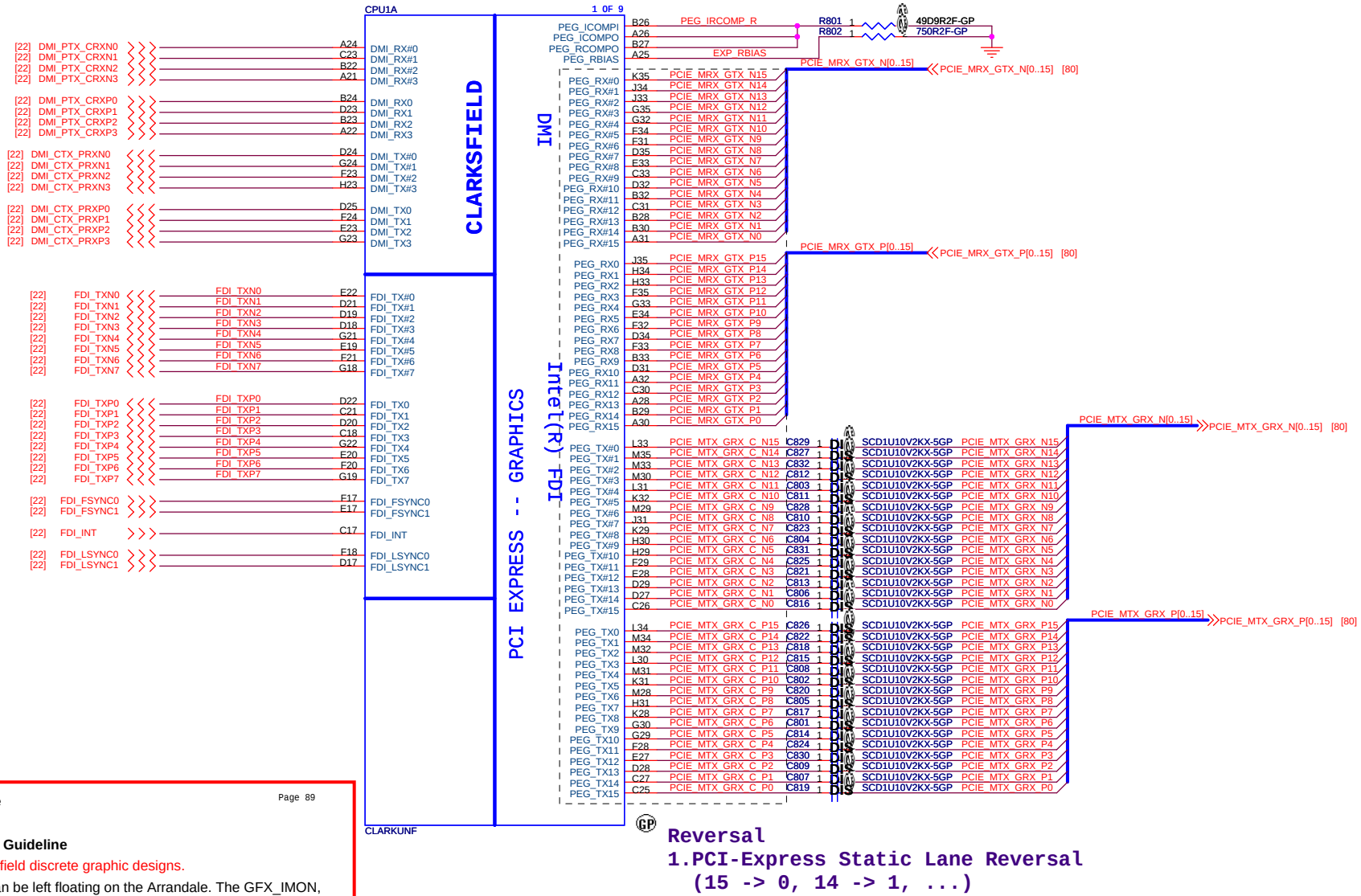
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator SLG8SP585

Size | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 7 of 91



Reversal
1.PCI-Express Static Lane Reversal
(15 -> 0, 14 -> 1, ...)

Calpella Platform Design Guide
Revision 1.6

Page 89

2.4 Arrandale Graphics Disable Guideline

It applies to Arrandale and Clarksfield discrete graphic designs.

FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

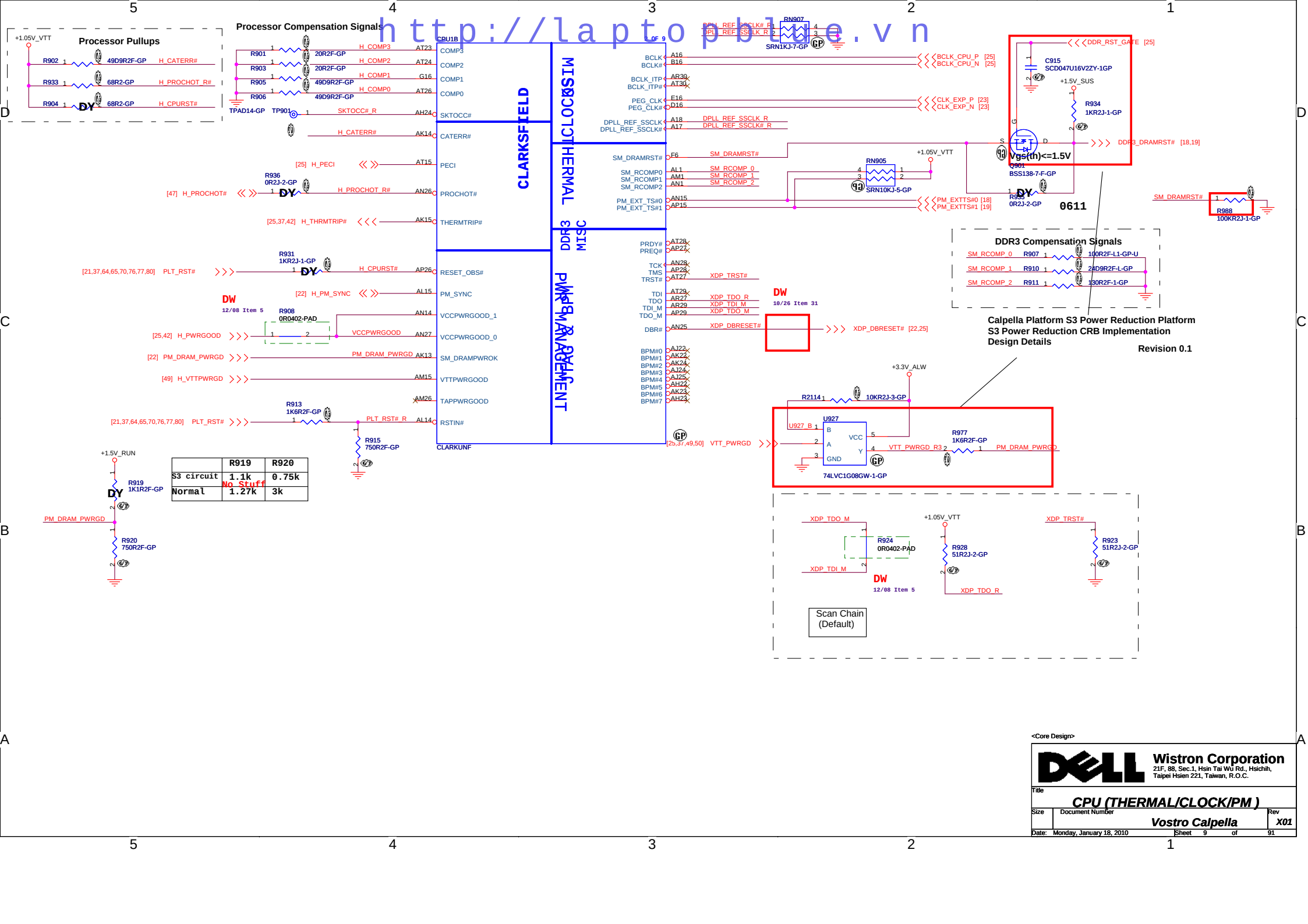
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/DMI/FDI)

Size	Document Number	Rev
	Vostro Calpella	X01

Date: Monday, January 18, 2010 Sheet 8 of 91



	R919	R920
S3 circuit	1.1k	0.75k
Normal	1.27k	3k

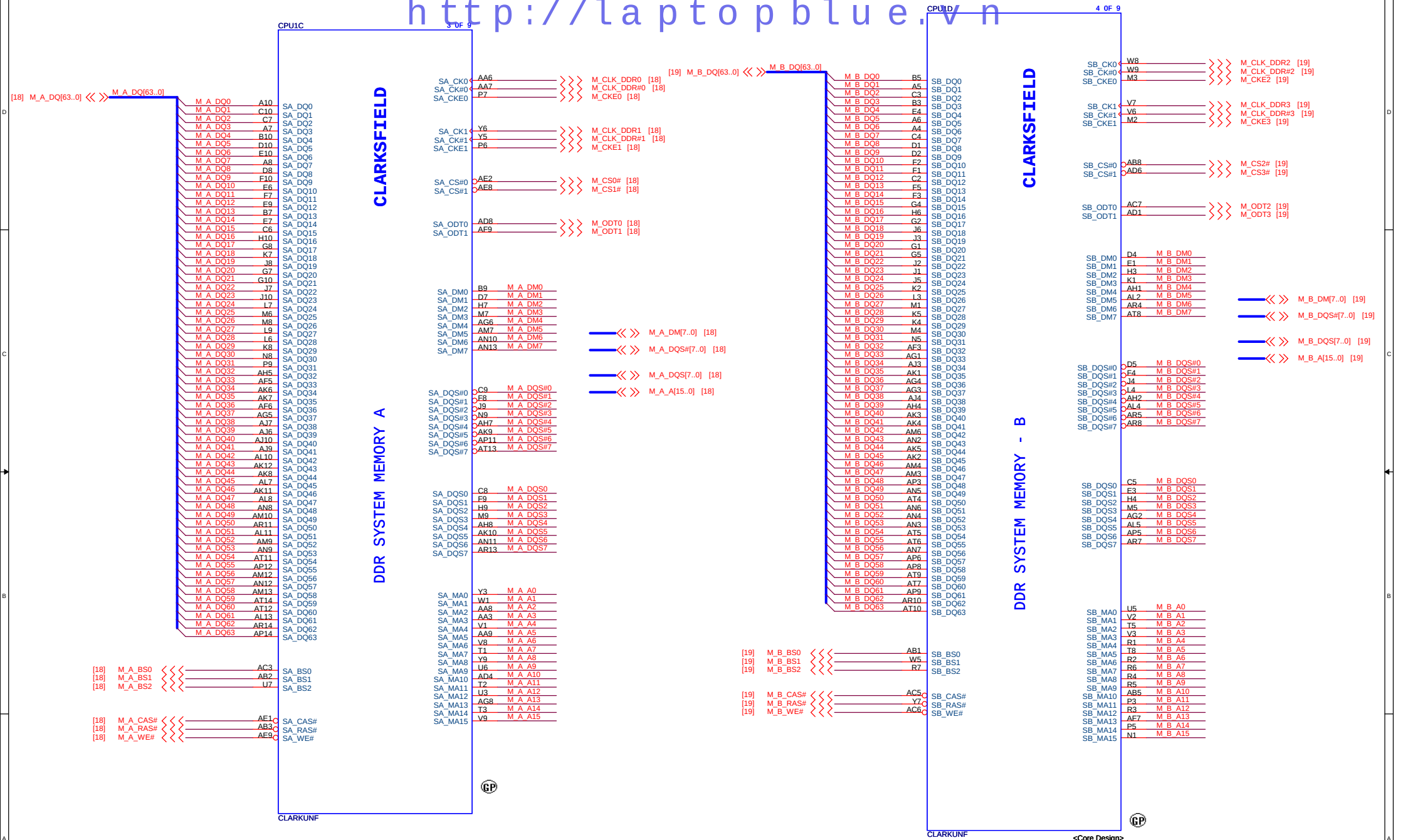
No Stuff

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
	Vostro Calpella	X01

Date: Monday, January 18, 2010 Sheet 9 of 91



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDR)

Size | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 10 of 91

<Core Design>

CFG0

R1101
3KR2F-GP
DY

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

DIS改5%

CFG3

R1102
3KR2F-GP

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4

R1103
3KR2F-GP
DY

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

Calpella Platform Design Guide
Revision 1.6

4.8.3.1 LVDS Switching

Switchable GFX, just like integrated GFX only, to enable LVDS it is required that the OEM set the LDVS (L_DDC_DATA) strap to present (pulled up) and the eDP strap (CFG[4]) to disabled (not pulled down).

4.8.3.2 eDP Switching

eDP for Switchable GFX can only be driven out of Port D of PCH. To configure Port D for embedded DP it is required to set the DDPD_CTRLDATA strap high to 3.3V Core rail through 2.2 kΩ ±5% resistor, LVDS (L_DDC_DATA) strap as no connect and the eDP strap CFG[4] as no connect.

Page 482, 486

CFG7

TP1118
TPAD14-GP

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

CPU1E — 5 OF 9 — CLARKSFIELD / RESERVED

TP1116 SA_DIMM_VREF#
TP1117 SB_DIMM_VREF#

AP25 RSVD#AP25
AL25 RSVD#AL25
AL24 RSVD#AL24
AL22 RSVD#AL22
AJ33 RSVD#AJ33
AG9 RSVD#AG9
M27 RSVD#M27
L28 RSVD#L28
J17 SA_DIMM_VREF
H17 SB_DIMM_VREF
G25 RSVD#G25
G17 RSVD#G17
E31 RSVD#E31
E30 RSVD#E30

RSVD#AJ13 AJ13
RSVD#AJ12 AJ12
RSVD#AH25 AH25
RSVD#AK26 AK26
RSVD#AL26 AL26
RSVD_NCTF_37 AR2
RSVD#AJ26 AJ26
RSVD#AJ27 AJ27

CFG0 AM30 CFG0
AM28 CFG1
AP31 CFG2
CFG3 AL32 CFG3
CFG4 AL30 CFG4
AM31 CFG5
AN29 CFG6
CFG7 AM32 CFG7
AK32 CFG8
AK31 CFG9
AK28 CFG10
AJ28 CFG11
AN30 CFG12
AN32 CFG13
AJ32 CFG14
AJ29 CFG15
AJ30 CFG16
AK30 CFG17
H16 RSVD_TP_86

RSVD#AL28 AL28
RSVD#AL29 AL29
RSVD#AP30 AP30
RSVD#AP32 AP32
RSVD#AL27 AL27
RSVD#AT31 AT31
RSVD#AT32 AT32
RSVD#AP33 AP33
RSVD#AR33 AR33
RSVD#AR32 AR32
RSVD_TP#E15 E15
RSVD_TP#F15 F15
KEY A2
RSVD#D15 D15
RSVD#C15 C15
RSVD#AJ15 AJ15
RSVD#AH15 AH15

B19 RSVD#B19
A19 RSVD#A19
A20 RSVD#A20
B20 RSVD#B20
U9 RSVD#U9
T9 RSVD#T9
AC9 RSVD#AC9
AB9 RSVD#AB9
J29 RSVD#J29
J28 RSVD#J28

SA_CK2 AA5
SA_CK#2 AA4
SA_CKE2 R8
SA_CS#2 AD3
SA_ODT2 AD2
SA_CK3 AA2
SA_CK#3 AA1
SA_CKE3 R9
SA_CS#3 AG7
SA_ODT3 AE3

SB_CK2 V4
SB_CK#2 V5
SB_CKE2 N2
SB_CS#2 AD5
SB_ODT2 AD7
SB_CK3 W3
SB_CK#3 W2
SB_CKE3 N3
SB_CS#3 AE5
SB_ODT3 AD9

VSS AP34

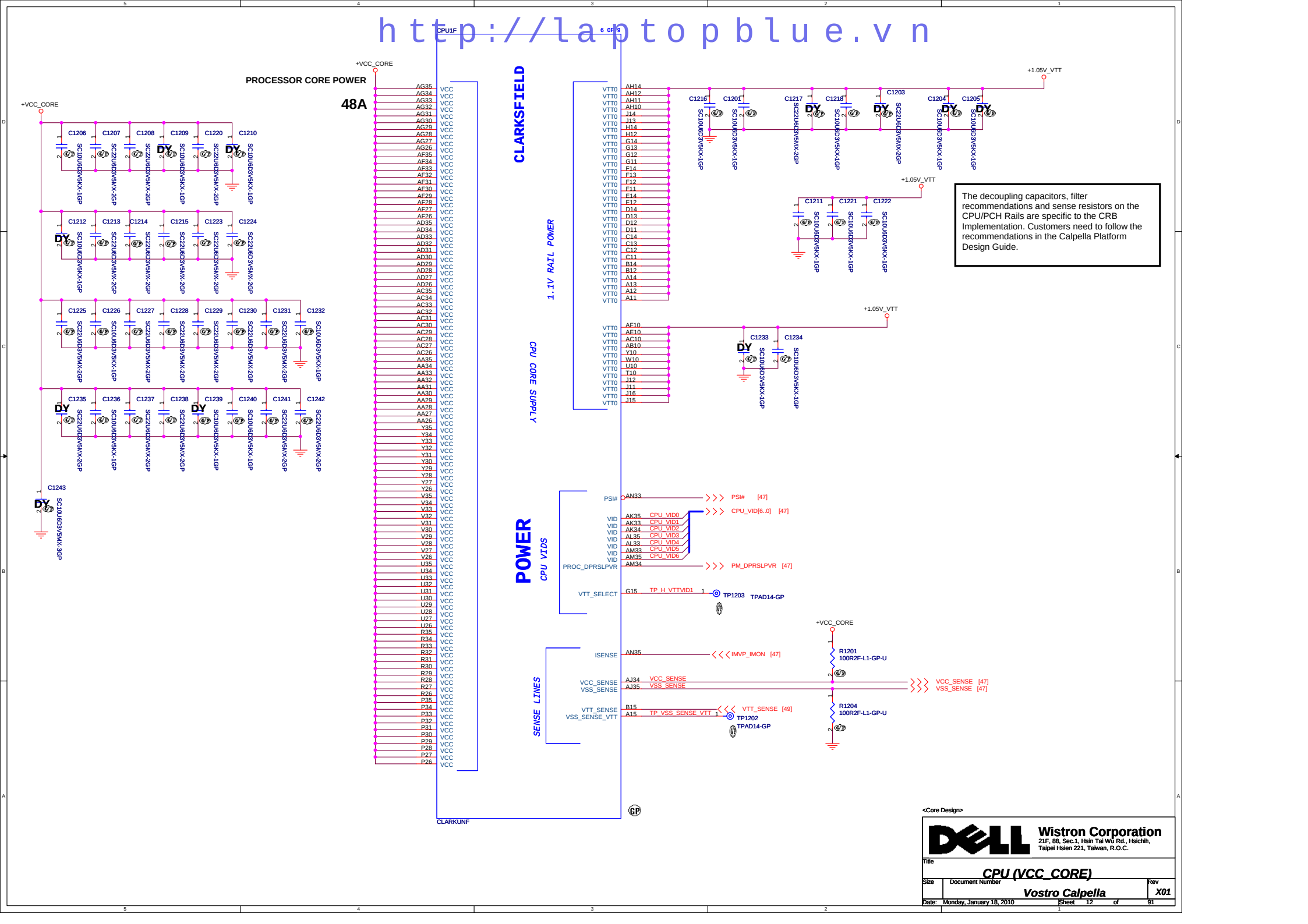
CLARKUNF

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RESERVED)
Size: | Document Number: Vostro Calpella | Rev: X01
Date: Monday, January 18, 2010 | Sheet 11 of 91



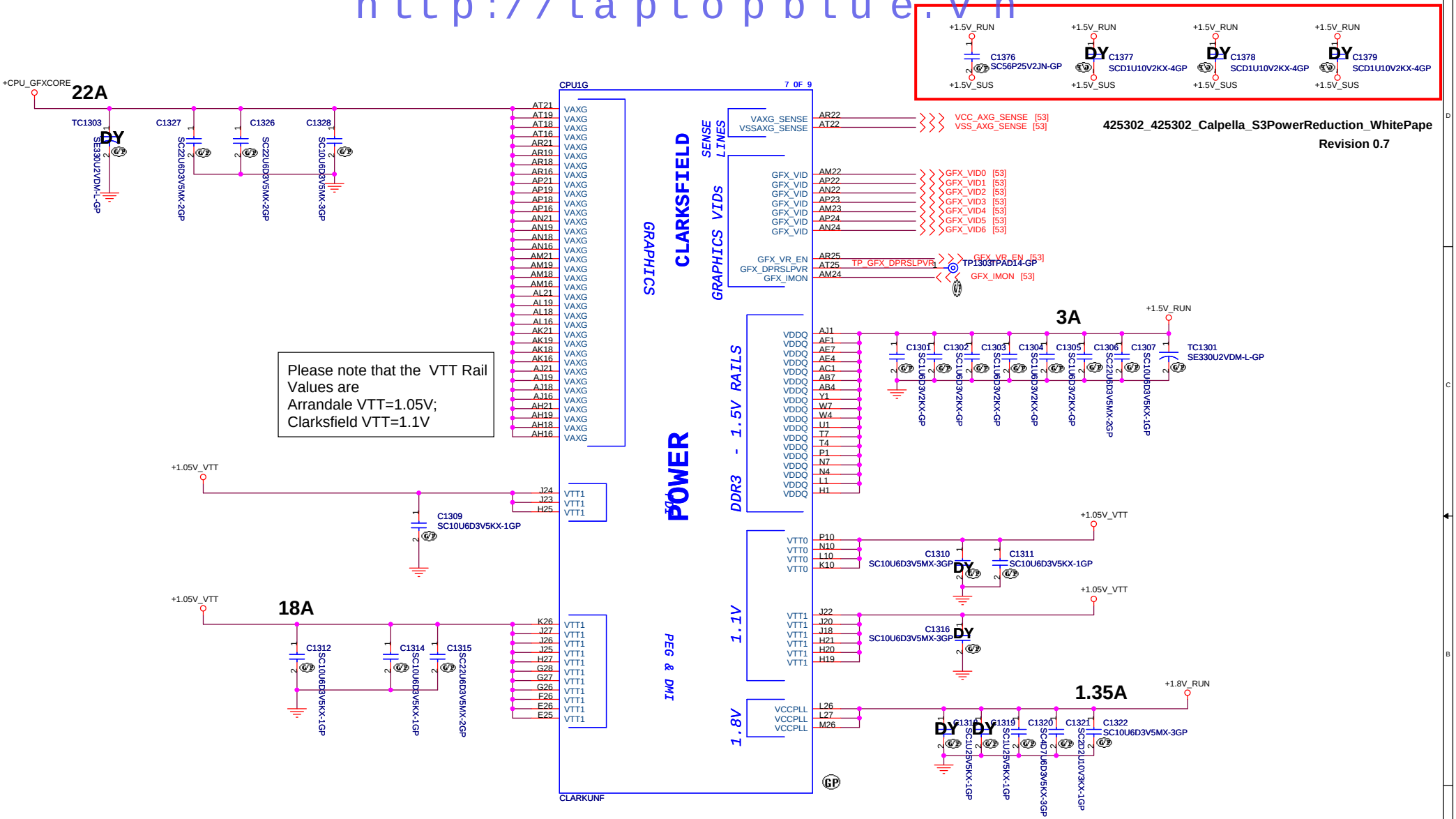
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Core Design>

Title: CPU (VCC_CORE)

Size | Document Number: Vostro Calpella | Rev: X01

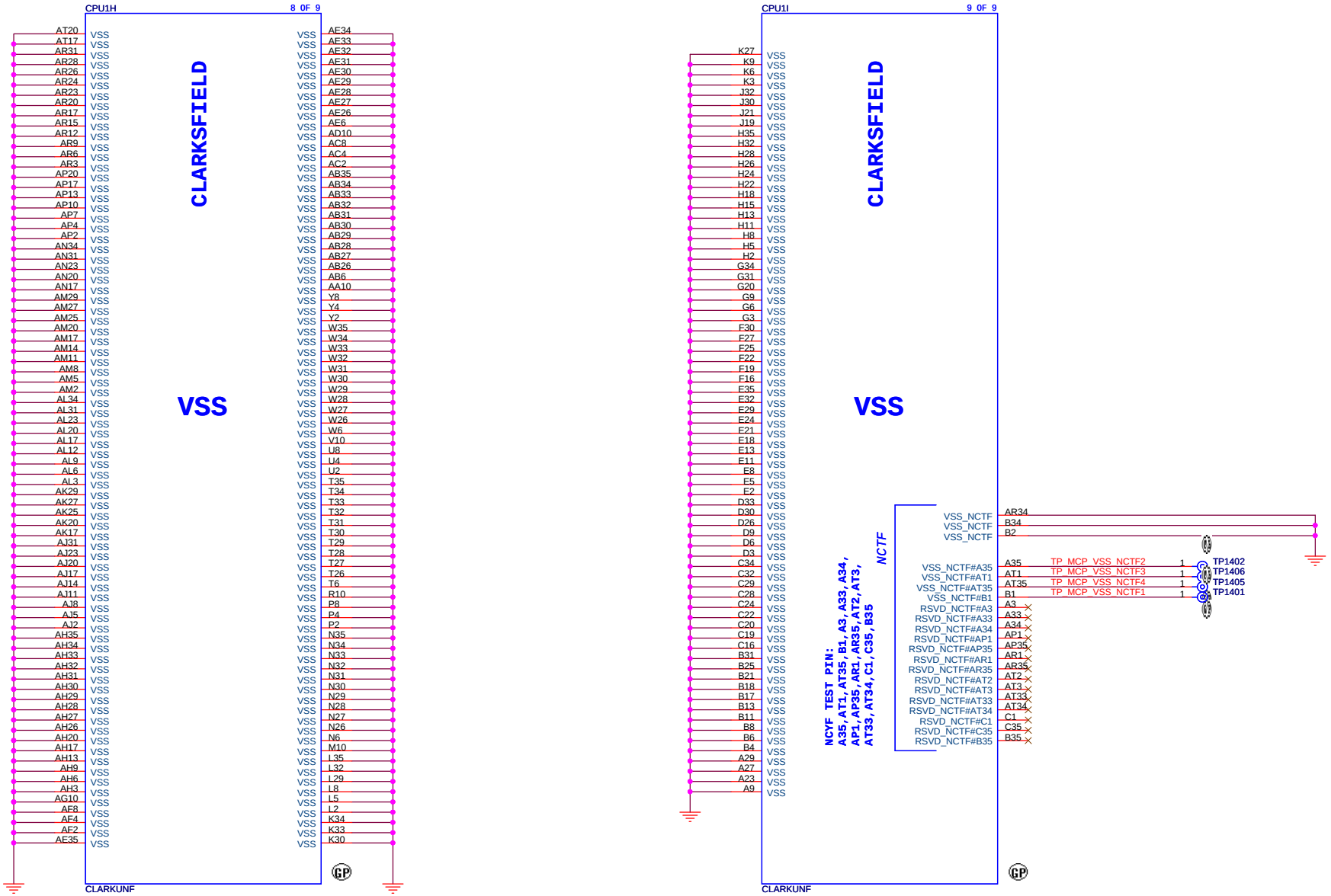
Date: Monday, January 18, 2010 | Sheet 12 of 91



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (VCC_GFXCORE)	
Size	Document Number: Vostro Calpella	Rev: X01
Date: Monday, January 18, 2010	Sheet 13 of 91	



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 14 of 91

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Vostro Calpella*	*X01*

Date: Monday, January 18, 2010 Sheet 15 of 91

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Vostro Calpella* | Rev: *X01*

Date: Monday, January 18, 2010 | Sheet 16 of 91

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserve)*

Size	Document Number	Rev
Custom	*Vostro Calpella*	*X01*

Date: Monday, January 18, 2010 Sheet 17 of 91

SSID = MEMORY

[10] M_A_DQS#[7..0]
[10] M_A_DQ[63..0]
[10] M_A_DM[7..0]
[10] M_A_DQS[7..0]
[10] M_A_A[15..0]

DM1

M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15
M_A_BS2 79 A16/BA2

[10] M_A_BS2
[10] M_A_BS0
[10] M_A_BS1

M_A_BS0 109 BA0
M_A_BS1 108 BA1

M_A_DQ0 5 DQ0
M_A_DQ1 7 DQ1
M_A_DQ2 15 DQ2
M_A_DQ3 17 DQ3
M_A_DQ4 4 DQ4
M_A_DQ5 6 DQ5
M_A_DQ6 16 DQ6
M_A_DQ7 18 DQ7
M_A_DQ8 21 DQ8
M_A_DQ9 23 DQ9
M_A_DQ10 33 DQ10
M_A_DQ11 35 DQ11
M_A_DQ12 22 DQ12
M_A_DQ13 24 DQ13
M_A_DQ14 34 DQ14
M_A_DQ15 36 DQ15
M_A_DQ16 39 DQ16
M_A_DQ17 41 DQ17
M_A_DQ18 51 DQ18
M_A_DQ19 53 DQ19
M_A_DQ20 40 DQ20
M_A_DQ21 42 DQ21
M_A_DQ22 50 DQ22
M_A_DQ23 52 DQ23
M_A_DQ24 57 DQ24
M_A_DQ25 59 DQ25
M_A_DQ26 67 DQ26
M_A_DQ27 69 DQ27
M_A_DQ28 56 DQ28
M_A_DQ29 58 DQ29
M_A_DQ30 68 DQ30
M_A_DQ31 70 DQ31
M_A_DQ32 129 DQ32
M_A_DQ33 131 DQ33
M_A_DQ34 141 DQ34
M_A_DQ35 143 DQ35
M_A_DQ36 130 DQ36
M_A_DQ37 132 DQ37
M_A_DQ38 140 DQ38
M_A_DQ39 142 DQ39
M_A_DQ40 147 DQ40
M_A_DQ41 149 DQ41
M_A_DQ42 157 DQ42
M_A_DQ43 159 DQ43
M_A_DQ44 146 DQ44
M_A_DQ45 148 DQ45
M_A_DQ46 158 DQ46
M_A_DQ47 160 DQ47
M_A_DQ48 163 DQ48
M_A_DQ49 165 DQ49
M_A_DQ50 175 DQ50
M_A_DQ51 177 DQ51
M_A_DQ52 164 DQ52
M_A_DQ53 166 DQ53
M_A_DQ54 174 DQ54
M_A_DQ55 176 DQ55
M_A_DQ56 181 DQ56
M_A_DQ57 183 DQ57
M_A_DQ58 191 DQ58
M_A_DQ59 193 DQ59
M_A_DQ60 180 DQ60
M_A_DQ61 182 DQ61
M_A_DQ62 192 DQ62
M_A_DQ63 194 DQ63

M_A_DQS#0 10 DQS0#
M_A_DQS#1 27 DQS1#
M_A_DQS#2 45 DQS2#
M_A_DQS#3 62 DQS3#
M_A_DQS#4 135 DQS4#
M_A_DQS#5 152 DQS5#
M_A_DQS#6 169 DQS6#
M_A_DQS#7 186 DQS7#

M_A_DQS0 12 DQS0
M_A_DQS1 29 DQS1
M_A_DQS2 47 DQS2
M_A_DQS3 64 DQS3
M_A_DQS4 137 DQS4
M_A_DQS5 154 DQS5
M_A_DQS6 171 DQS6
M_A_DQS7 188 DQS7

[10] M_ODT0
[10] M_ODT1

M_ODT0 116 ODT0
M_ODT1 120 ODT1

126 VREF_CA
1 VREF_DQ

[9,19] DDR3_DRAMRST# 30 RESET#

203 VTT1
204 VTT2

NP1 NP2

RAS# 110 M_A_RAS# [10]
WE# 113 M_A_WE# [10]
CAS# 115 M_A_CAS# [10]

CS0# 114 M_CS0# [10]
CS1# 121 M_CS1# [10]

CKE0 73 M_CKE0 [10]
CKE1 74 M_CKE1 [10]

CK0 101 M_CLK_DDR0 M_CLK_DDR0 [10]
CK0# 103 M_CLK_DDR#0 M_CLK_DDR#0 [10]

CK1 102 M_CLK_DDR1 M_CLK_DDR1 [10]
CK1# 104 M_CLK_DDR#1 M_CLK_DDR#1 [10]

DM0 11 M_A_DM0
DM1 28 M_A_DM1
DM2 46 M_A_DM2
DM3 63 M_A_DM3
DM4 136 M_A_DM4
DM5 153 M_A_DM5
DM6 170 M_A_DM6
DM7 187 M_A_DM7

SDA 200 PCH_SMBDATA PCH_SMBDATA [7,19,23,40,64,65]
SCL 202 PCH_SMBCLK PCH_SMBCLK [7,19,23,40,64,65]

EVENT# 198 PM_EXTTS#0 [9]

VDDSPD 199

SA0 197 SA0_DM1
SA1 201 SA1_DM1

NC#1 77
NC#2 122
NC#/TEST 125

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

VSS 2
VSS 3
VSS 8
VSS 9
VSS 13
VSS 14
VSS 19
VSS 20
VSS 25
VSS 26
VSS 31
VSS 32
VSS 37
VSS 38
VSS 43
VSS 44
VSS 48
VSS 49
VSS 54
VSS 55
VSS 60
VSS 61
VSS 65
VSS 66
VSS 71
VSS 72
VSS 127
VSS 128
VSS 133
VSS 134
VSS 138
VSS 139
VSS 144
VSS 145
VSS 150
VSS 151
VSS 155
VSS 156
VSS 161
VSS 162
VSS 167
VSS 168
VSS 172
VSS 173
VSS 178
VSS 179
VSS 184
VSS 185
VSS 189
VSS 190
VSS 195
VSS 196
VSS 205
VSS 206

Height 5.2mm

DDR3-204P-47-GP

SA0_DM1
SA1_DM1

RN1802
SRN10KJ-5-GP

SMBUS address:A0

+3.3V_RUN

C1806 SCD1U16V2KX-3GP
C1807 SC2D2U10V3KX-1GP

+1.5V_SUS

Layout Note:
Place near DM1

C1803 SC10U6D3V5MX-3GP
C1812 SC10U6D3V5MX-3GP
C1811 SC10U6D3V5MX-3GP
C1804 SC10U6D3V5MX-3GP
C1802 SC10U6D3V5MX-3GP
C1816 SC10U6D3V5MX-3GP
TC1803 ST330U2D5VBM-1-GP

Layout Note:
Put close to VTT1,VTT2.

+0.75V_DDR_VTT

C1823 SC10U6D3V5MX-3GP
C1813 SC1U10V2KX-1GP
C1801 SC1U10V2KX-1GP
C1814 SC1U10V2KX-1GP
C1815 SC1U10V2KX-1GP

+1.5V_SUS

C1872 SCD1U10V2KX-4GP
C1873 SCD1U10V2KX-4GP
C1874 SCD1U10V2KX-4GP
C1875 SCD1U10V2KX-4GP

425302_425302_Calpella_S3PowerReduction_WhitePape
Revision 0.7

+V_DDR_REF

C1810 SCD1U16V2KX-3GP
C1809 SC2D2U10V3KX-1GP

+V_DDR_REF

C1817 SCD1U16V2KX-3GP
C1805 SC2D2U10V3KX-1GP

62.10017.P31

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII-SODIMM SLOT1

Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 18 of 91

SSID = MEMORY

[10] M_B_DQS#[7..0]
[10] M_B_DQ[63..0]
[10] M_B_DM[7..0]
[10] M_B_DQS[7..0]
[10] M_B_A[15..0]

Layout Note:
Place near DM2

+1.5V_SUS

DY C1919 SC10U6D3V5MX-3GP
C1911 SC10U6D3V5MX-3GP
C1913 SC10U6D3V5MX-3GP
C1905 SC10U6D3V5MX-3GP
C1916 SC10U6D3V5MX-3GP
C1920 SC10U6D3V5MX-3GP
DY TC1903 ST330U2D5VBM-1-GP

Layout Note:
Put close to VTT1,VTT2.

+0.75V_DDR_VTT

C1908 SC1U10V2KX-1GP
C1909 SC1U10V2KX-1GP
C1917 SC1U10V2KX-1GP
C1918 SC1U10V2KX-1GP

+1.5V_SUS

C1976 SCD1U10V2KX-4GP
DY C1977 SCD1U10V2KX-4GP
C1978 SCD1U10V2KX-4GP
C1979 SCD1U10V2KX-4GP

425302_425302_Calpella_S3PowerReduction_WhitePape
Revision 0.7

+V_DDR_REF

C1907 SCD1U16V2KX-3GP
DY C1914 SC2D2U10V3KX-1GP

+V_DDR_REF

C1910 SCD1U16V2KX-3GP
DY C1912 SC2D2U10V3KX-1GP

DM2

M_B_A0	98	A0
M_B_A1	97	A1
M_B_A2	96	A2
M_B_A3	95	A3
M_B_A4	92	A4
M_B_A5	91	A5
M_B_A6	90	A6
M_B_A7	86	A7
M_B_A8	89	A8
M_B_A9	85	A9
M_B_A10	107	A10/AP
M_B_A11	84	A11
M_B_A12	83	A12
M_B_A13	119	A13
M_B_A14	80	A14
M_B_A15	78	A15
[10] M_B_BS2	79	A16/BA2
M_B_BS0	109	BA0
[10] M_B_BS0 [10] M_B_BS1	108	BA1
M_B_DQ0	5	DQ0
M_B_DQ1	7	DQ1
M_B_DQ2	15	DQ2
M_B_DQ3	17	DQ3
M_B_DQ4	4	DQ4
M_B_DQ5	6	DQ5
M_B_DQ6	16	DQ6
M_B_DQ7	18	DQ7
M_B_DQ8	21	DQ8
M_B_DQ9	23	DQ9
M_B_DQ10	33	DQ10
M_B_DQ11	35	DQ11
M_B_DQ12	22	DQ12
M_B_DQ13	24	DQ13
M_B_DQ14	34	DQ14
M_B_DQ15	36	DQ15
M_B_DQ16	39	DQ16
M_B_DQ17	41	DQ17
M_B_DQ18	51	DQ18
M_B_DQ19	53	DQ19
M_B_DQ20	40	DQ20
M_B_DQ21	42	DQ21
M_B_DQ22	50	DQ22
M_B_DQ23	52	DQ23
M_B_DQ24	57	DQ24
M_B_DQ25	59	DQ25
M_B_DQ26	67	DQ26
M_B_DQ27	69	DQ27
M_B_DQ28	56	DQ28
M_B_DQ29	58	DQ29
M_B_DQ30	68	DQ30
M_B_DQ31	70	DQ31
M_B_DQ32	129	DQ32
M_B_DQ33	131	DQ33
M_B_DQ34	141	DQ34
M_B_DQ35	143	DQ35
M_B_DQ36	130	DQ36
M_B_DQ37	132	DQ37
M_B_DQ38	140	DQ38
M_B_DQ39	142	DQ39
M_B_DQ40	147	DQ40
M_B_DQ41	149	DQ41
M_B_DQ42	157	DQ42
M_B_DQ43	159	DQ43
M_B_DQ44	146	DQ44
M_B_DQ45	148	DQ45
M_B_DQ46	158	DQ46
M_B_DQ47	160	DQ47
M_B_DQ48	163	DQ48
M_B_DQ49	165	DQ49
M_B_DQ50	175	DQ50
M_B_DQ51	177	DQ51
M_B_DQ52	164	DQ52
M_B_DQ53	166	DQ53
M_B_DQ54	174	DQ54
M_B_DQ55	176	DQ55
M_B_DQ56	181	DQ56
M_B_DQ57	183	DQ57
M_B_DQ58	191	DQ58
M_B_DQ59	193	DQ59
M_B_DQ60	180	DQ60
M_B_DQ61	182	DQ61
M_B_DQ62	192	DQ62
M_B_DQ63	194	DQ63
M_B_DQS#0	10	DQS0#
M_B_DQS#1	27	DQS1#
M_B_DQS#2	45	DQS2#
M_B_DQS#3	62	DQS3#
M_B_DQS#4	135	DQS4#
M_B_DQS#5	152	DQS5#
M_B_DQS#6	169	DQS6#
M_B_DQS#7	186	DQS7#
M_B_DQS0	12	DQS0
M_B_DQS1	29	DQS1
M_B_DQS2	47	DQS2
M_B_DQS3	64	DQS3
M_B_DQS4	137	DQS4
M_B_DQS5	154	DQS5
M_B_DQS6	171	DQS6
M_B_DQS7	188	DQS7
M_ODT2	116	ODT0
M_ODT3	120	ODT1
	126	VREF_CA
	1	VREF_DQ
[9,18] DDR3_DRAMRST#	30	RESET#
+0.75V_DDR_VTT	203	VTT1
	204	VTT2

NP1 NP2

RAS#	110	M_B_RAS# [10]
WE#	113	M_B_WE# [10]
CAS#	115	M_B_CAS# [10]
CS0#	114	M_CS2# [10]
CS1#	121	M_CS3# [10]
CKE0	73	M_CKE2 [10]
CKE1	74	M_CKE3 [10]
CK0	101	M_CLK_DDR2 M_CLK_DDR2 [10]
CK0#	103	M_CLK_DDR#2 M_CLK_DDR#2 [10]
CK1	102	M_CLK_DDR3 M_CLK_DDR3 [10]
CK1#	104	M_CLK_DDR#3 M_CLK_DDR#3 [10]
DM0	11	M_B_DM0
DM1	28	M_B_DM1
DM2	46	M_B_DM2
DM3	63	M_B_DM3
DM4	136	M_B_DM4
DM5	153	M_B_DM5
DM6	170	M_B_DM6
DM7	187	M_B_DM7
SDA	200	PCH_SMBDATA PCH_SMBDATA [7,18,23,40,64,65]
SCL	202	PCH_SMBCLK PCH_SMBCLK [7,18,23,40,64,65]
EVENT#	198	PM_EXTTS#1 [9]
VDDSPD	199	
SA0	197	SA0_DM2
SA1	201	SA1_DM2
NC#1	77	
NC#2	122	
NC#/TEST	125	

VDD1	75	
VDD2	76	
VDD3	81	
VDD4	82	
VDD5	87	
VDD6	88	
VDD7	93	
VDD8	94	
VDD9	99	
VDD10	100	
VDD11	105	
VDD12	106	
VDD13	111	
VDD14	112	
VDD15	117	
VDD16	118	
VDD17	123	
VDD18	124	

VSS	2
VSS	3
VSS	8
VSS	9
VSS	13
VSS	14
VSS	19
VSS	20
VSS	25
VSS	26
VSS	31
VSS	32
VSS	37
VSS	38
VSS	43
VSS	44
VSS	48
VSS	49
VSS	54
VSS	55
VSS	60
VSS	61
VSS	65
VSS	66
VSS	71
VSS	72
VSS	127
VSS	128
VSS	133
VSS	134
VSS	138
VSS	139
VSS	144
VSS	145
VSS	150
VSS	151
VSS	155
VSS	156
VSS	161
VSS	162
VSS	167
VSS	168
VSS	172
VSS	173
VSS	178
VSS	179
VSS	184
VSS	185
VSS	189
VSS	190
VSS	195
VSS	196
VSS	205
VSS	206

Height 9.2mm

DDR3-204P-55-GP

+3.3V_RUN

RN1903 SRN10KJ-5-GP

SA0_DM2
SA1_DM2

SMBUS address:A4

+3.3V_RUN

DY C1906 SCD1U16V2KX-3GP
C1921 SC2D2U10V3KX-1GP

+1.5V_SUS

Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
If SA0_DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4

[10] M_ODT2
[10] M_ODT3

+0.75V_DDR_VTT

62.10017.Q31

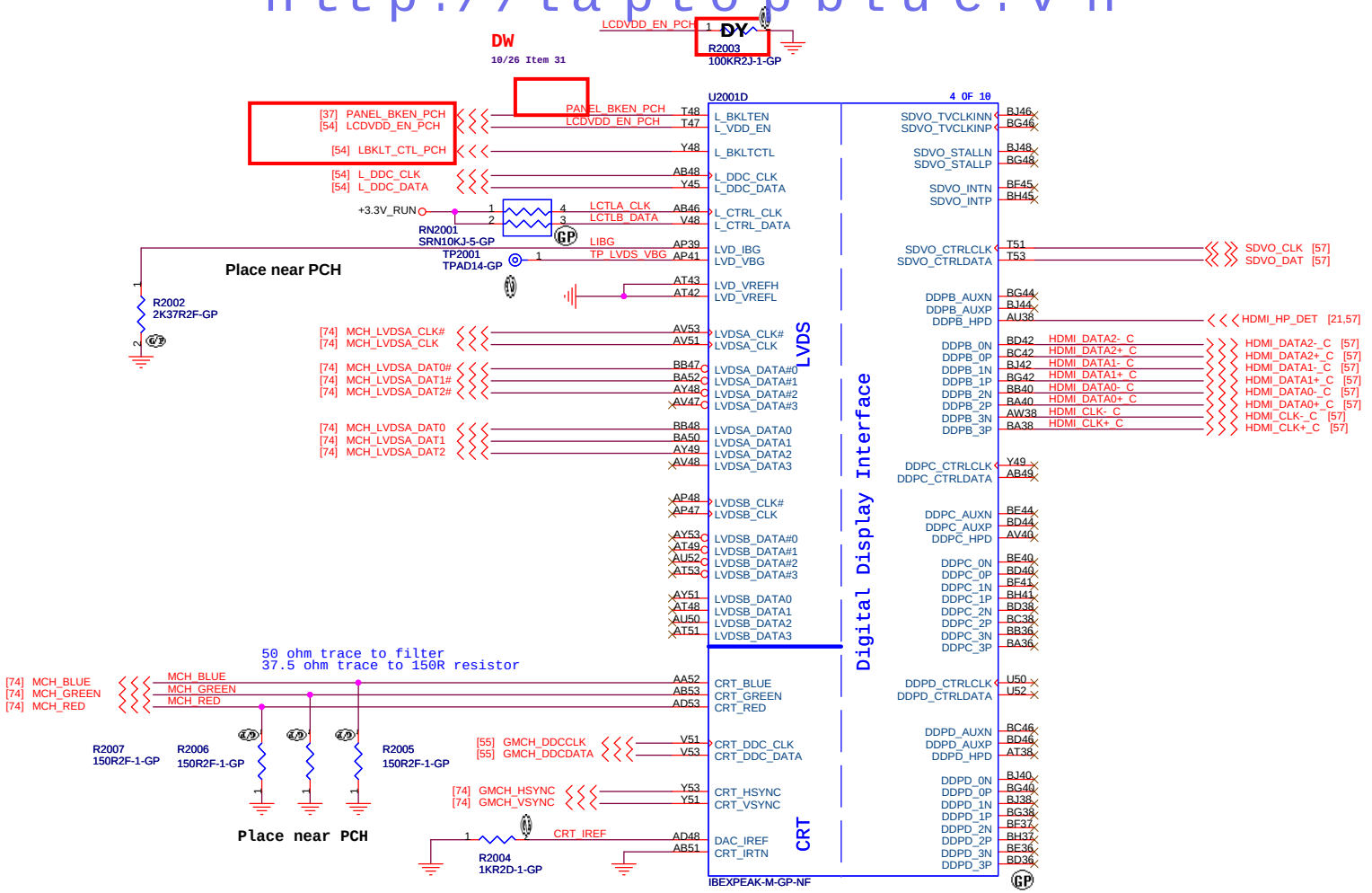
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDRIII-SODIMM SLOT2**

Size: Custom | Document Number: **Vostro Calpella** | Rev: X01

Date: Monday, January 18, 2010 | Sheet 19 of 91



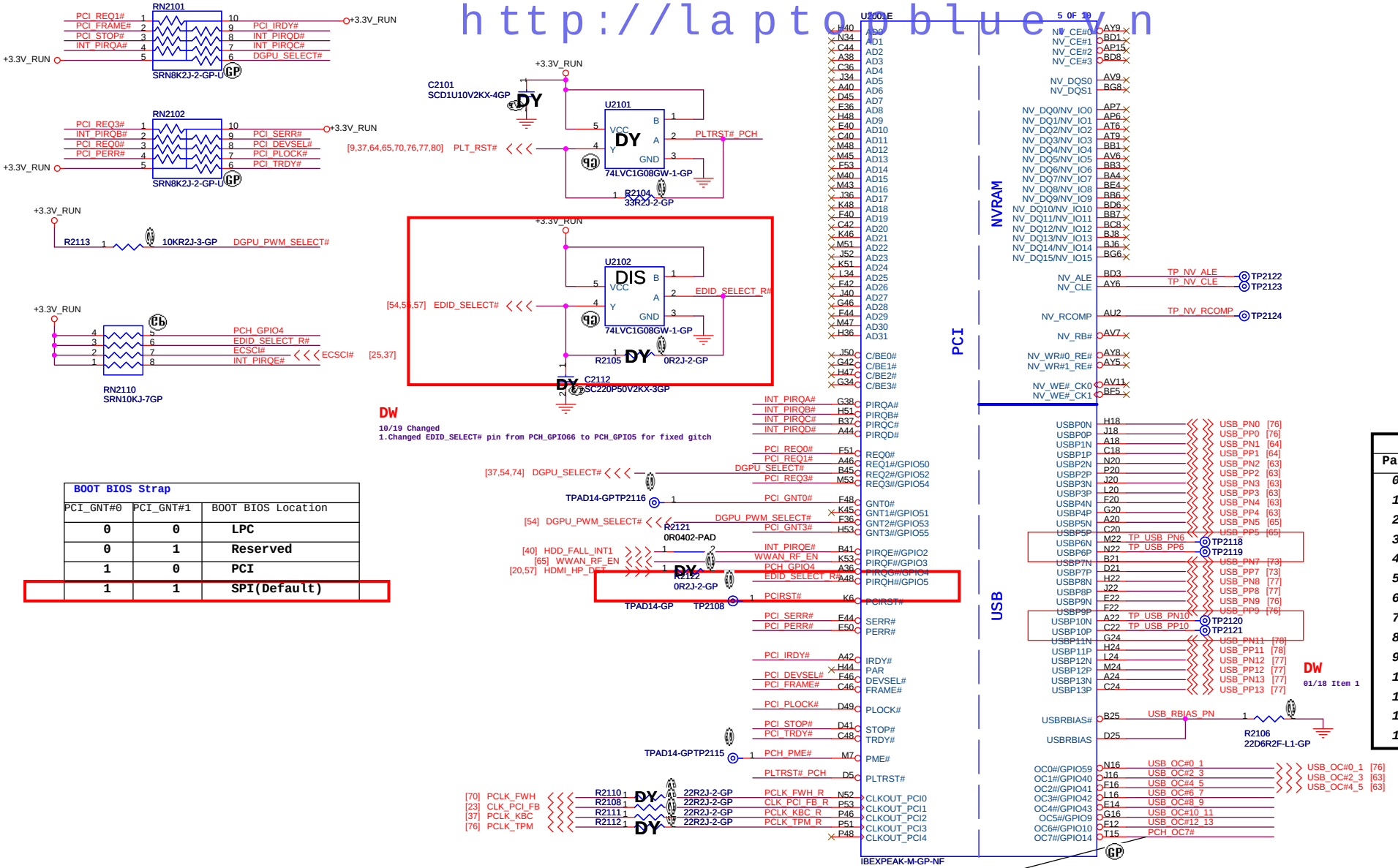
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 20 of 91



DW
10/19 Changed
1.Changed EDID_SELECT# pin from PCH_GPIO66 to PCH_GPIO5 for fixed gitch

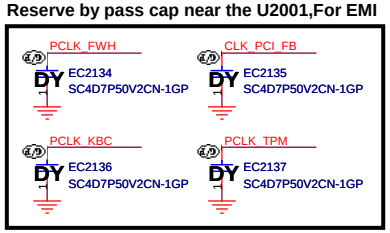
DW
01/18 Item 1

BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)

USB	
Pair	Device
0	USB1
1	WLAN
2	USB2
3	USB3
4	USB for ESATA
5	WWAN
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BLUETOOTH
9	Touch Panel
10	CAMERA
11	Biometric
12	New Card
13	CardReader

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Reserve by pass cap near the U2001,For EMI



Calpella Platform Design Guide
Revision 1.6

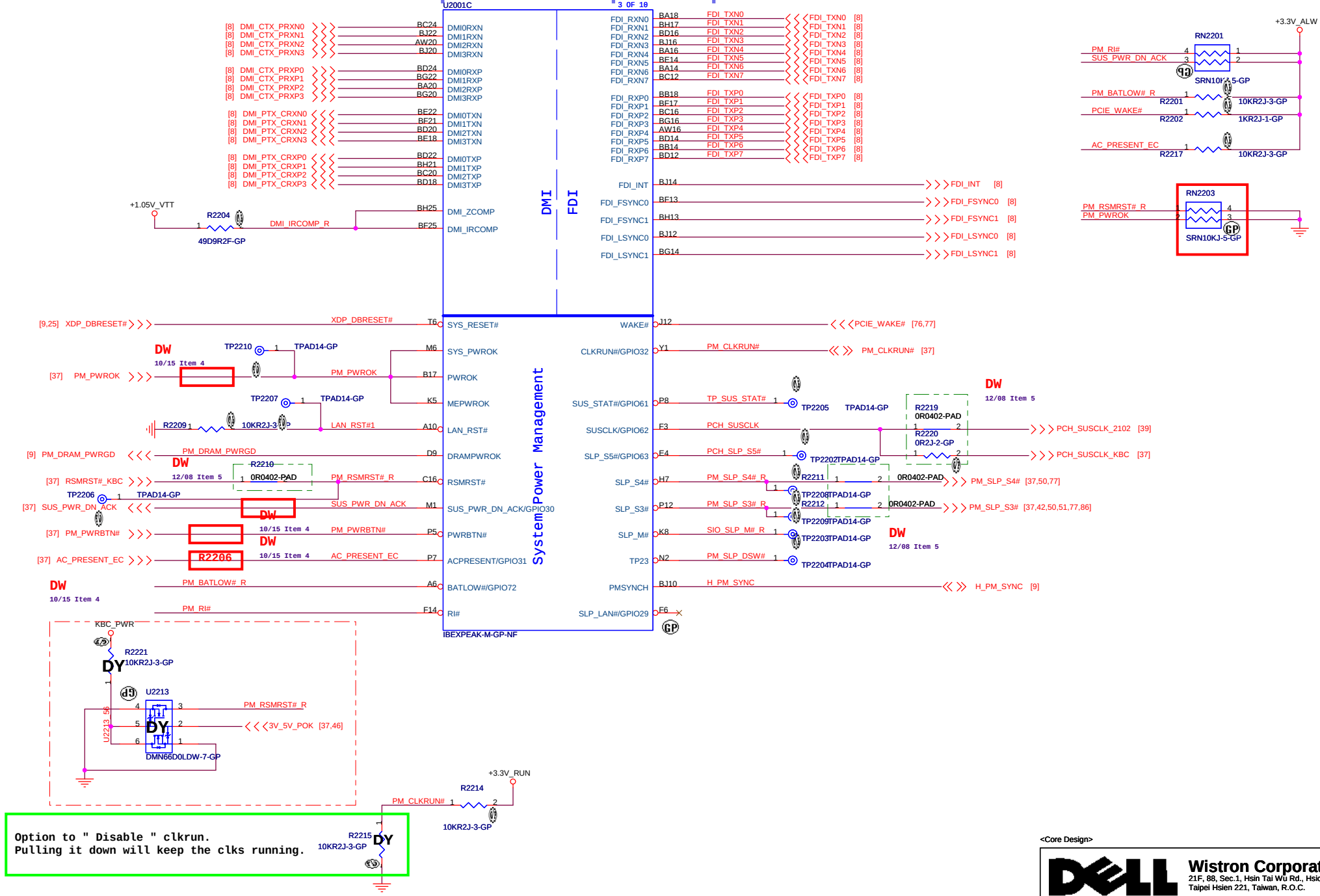
Table 111. Overcurrent Pin Example Configuration

These OC7# pins are not used for USB overcurrent protection and should be configured as GPIOs. The unused USB ports can be left as no connect.

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Core Design>

Title: PCH (PCI/USB/NVRAM)
Size: Document Number: Vostro Calpella Rev: X01
Date: Monday, January 18, 2010 Sheet 21 of 91



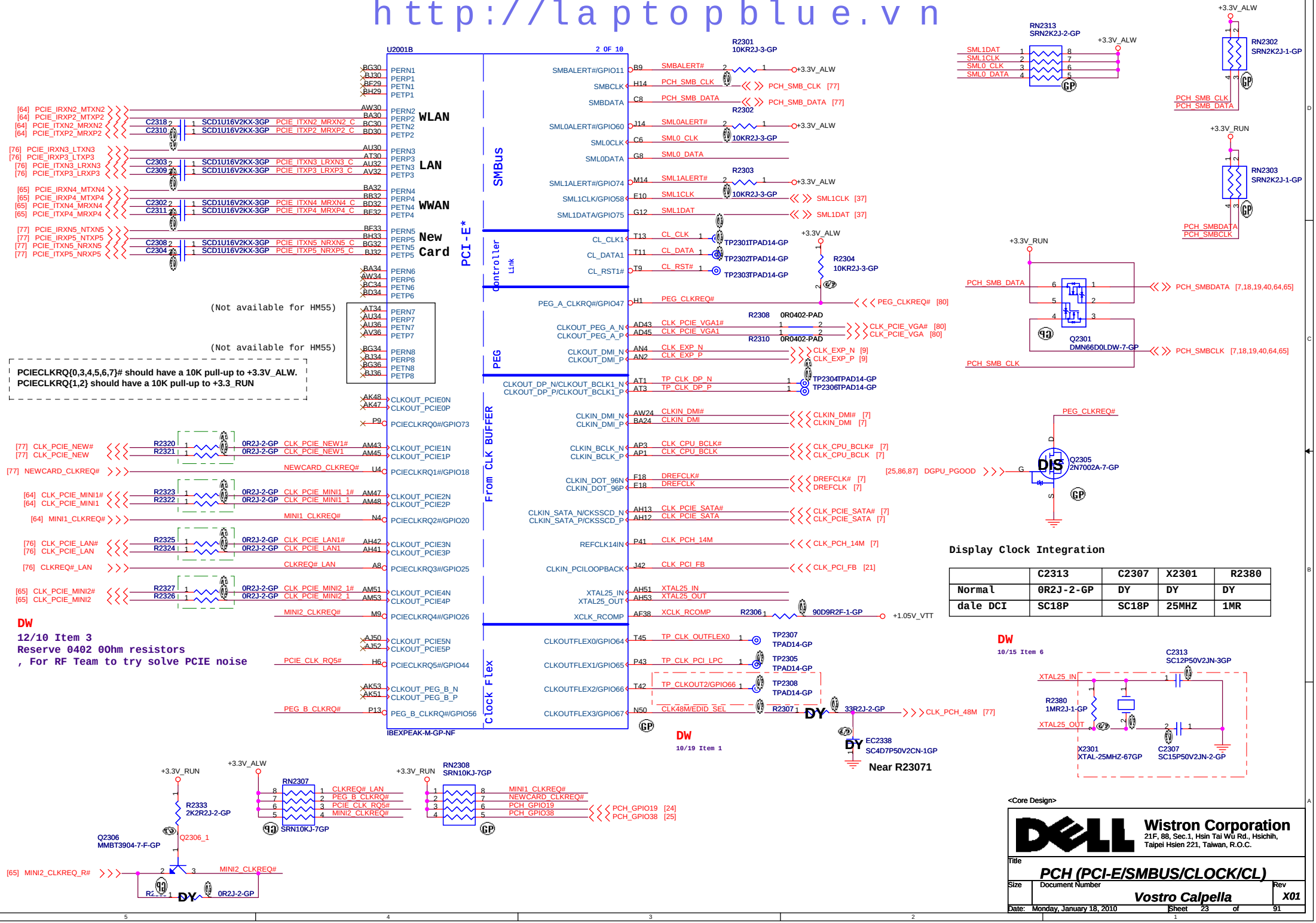
<Core Design>

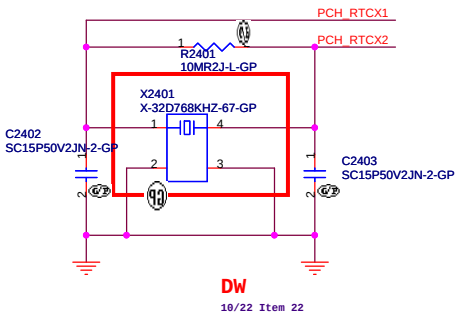
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

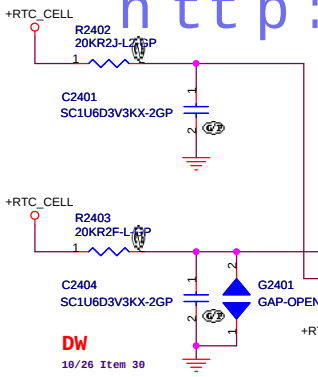
Title: PCH (DM I/FDI/PM)

Size | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 22 of 91

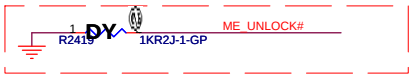


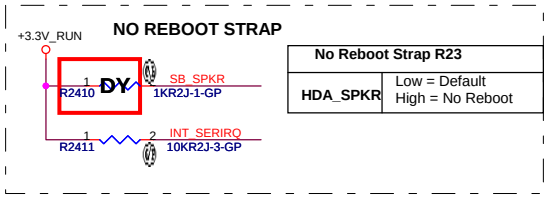




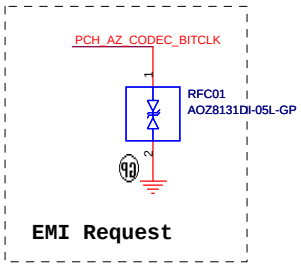
INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

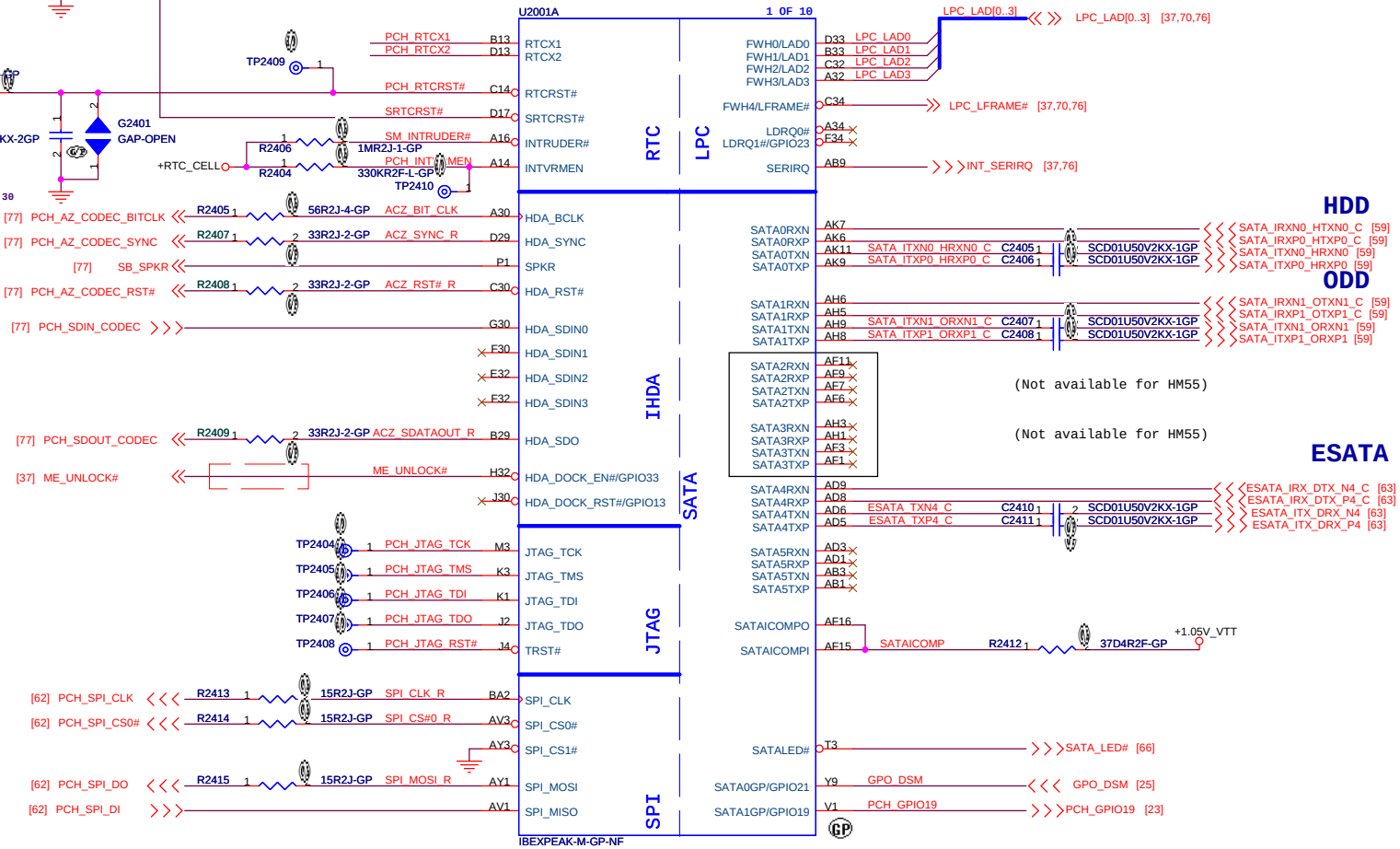
Flash Descriptor Security Override/ ME Debug Mode	
ME_UNLOCK#	This strap should only be asserted low via external pull down in manufacturing/debug environments ONLY.

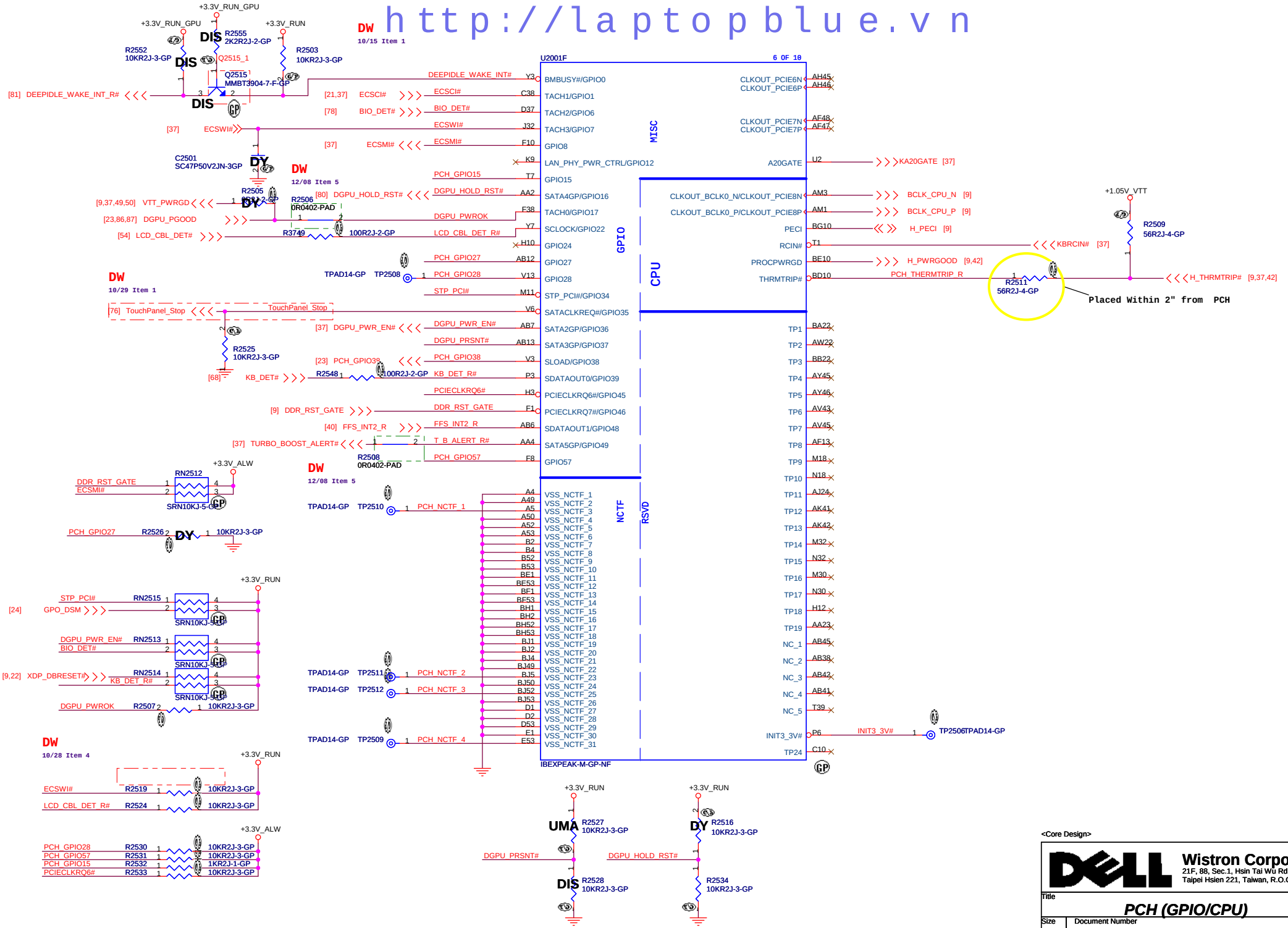


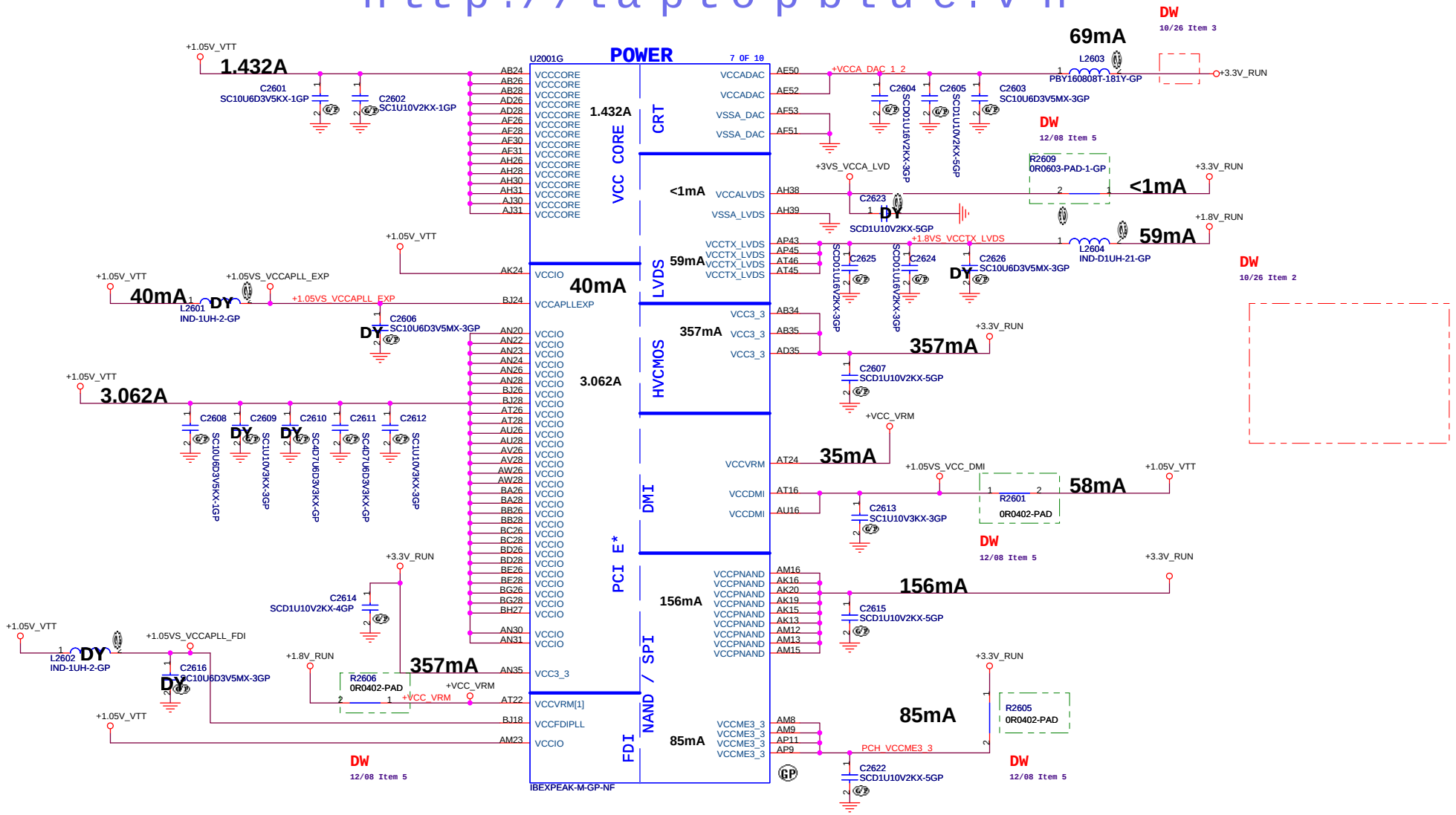


No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot





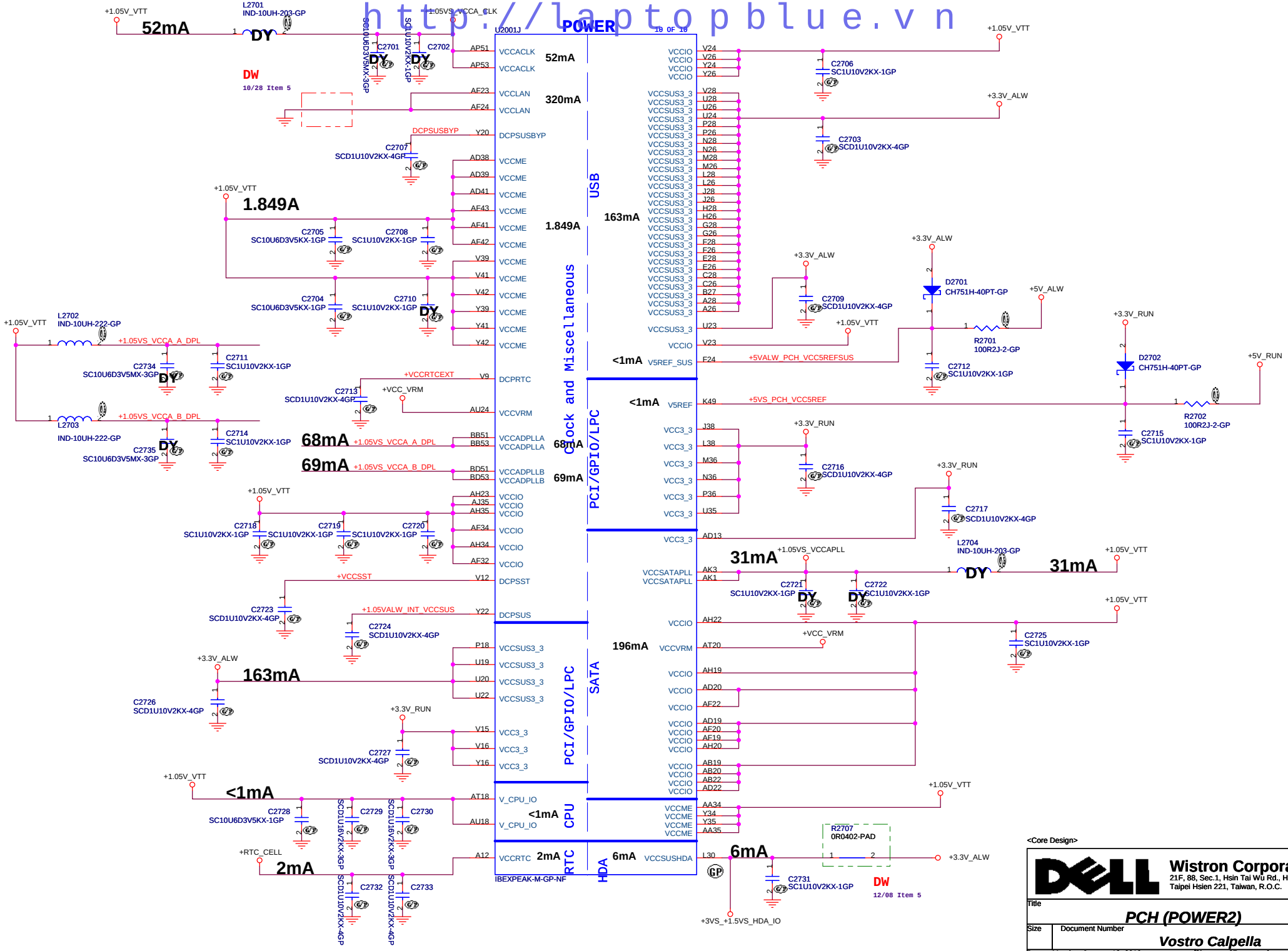




<Core Design>

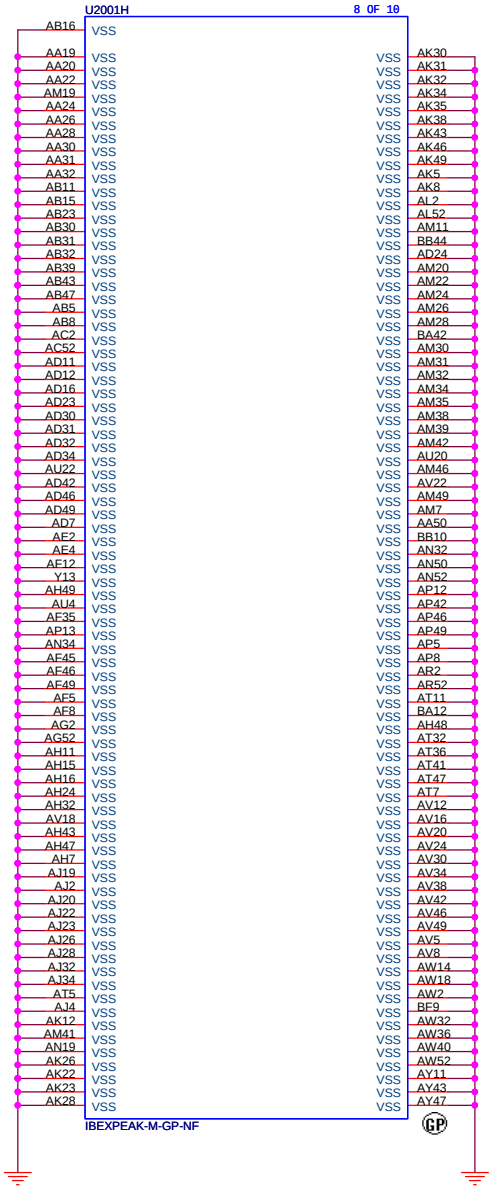
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

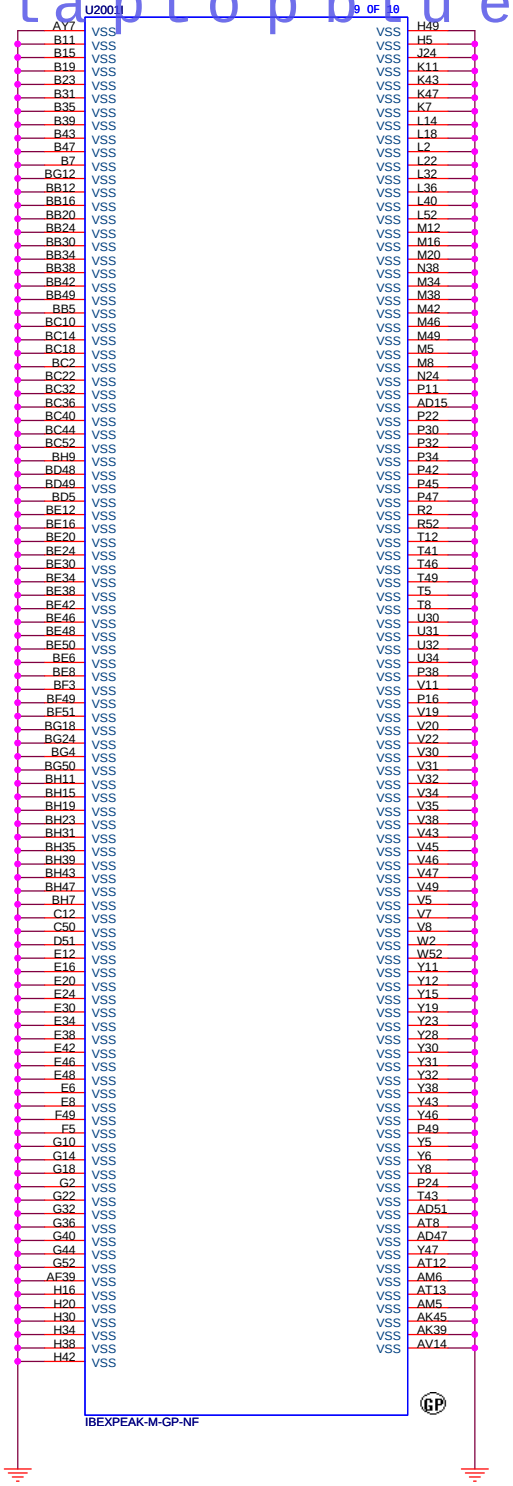
Title	PCH (POWER1)	
Size	Document Number: Vostro Calpella	Rev: X01
Date: Monday, January 18, 2010	Sheet 26 of 91	



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (POWER2)	
Size	Document Number: Vostro Calpella	Rev: X01
Date: Monday, January 18, 2010	Sheet 27 of 91	





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (VSS)**

Size | Document Number: **Vostro Calpella** | Rev: **X01**

Date: Monday, January 18, 2010 | Sheet 28 of 91

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*X01*

Date: Monday, January 18, 2010 Sheet 29 of 91

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*X01*

Date: Monday, January 18, 2010 Sheet 30 of 91

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*X01*

Date: Monday, January 18, 2010 Sheet 31 of 91

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserve*

Size: A3 | Document Number: *Vostro Calpella* | Rev: *X01*

Date: Monday, January 18, 2010 | Sheet 32 of 91

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*X01*

Date: Monday, January 18, 2010 Sheet 33 of 91

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*X01*

Date: Monday, January 18, 2010 Sheet 34 of 91

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserve)

Size	Document Number	Rev
A3	*Vostro Calpella*	*X01*

Date: Monday, January 18, 2010 Sheet 35 of 91

(Blank)

<Core Design>

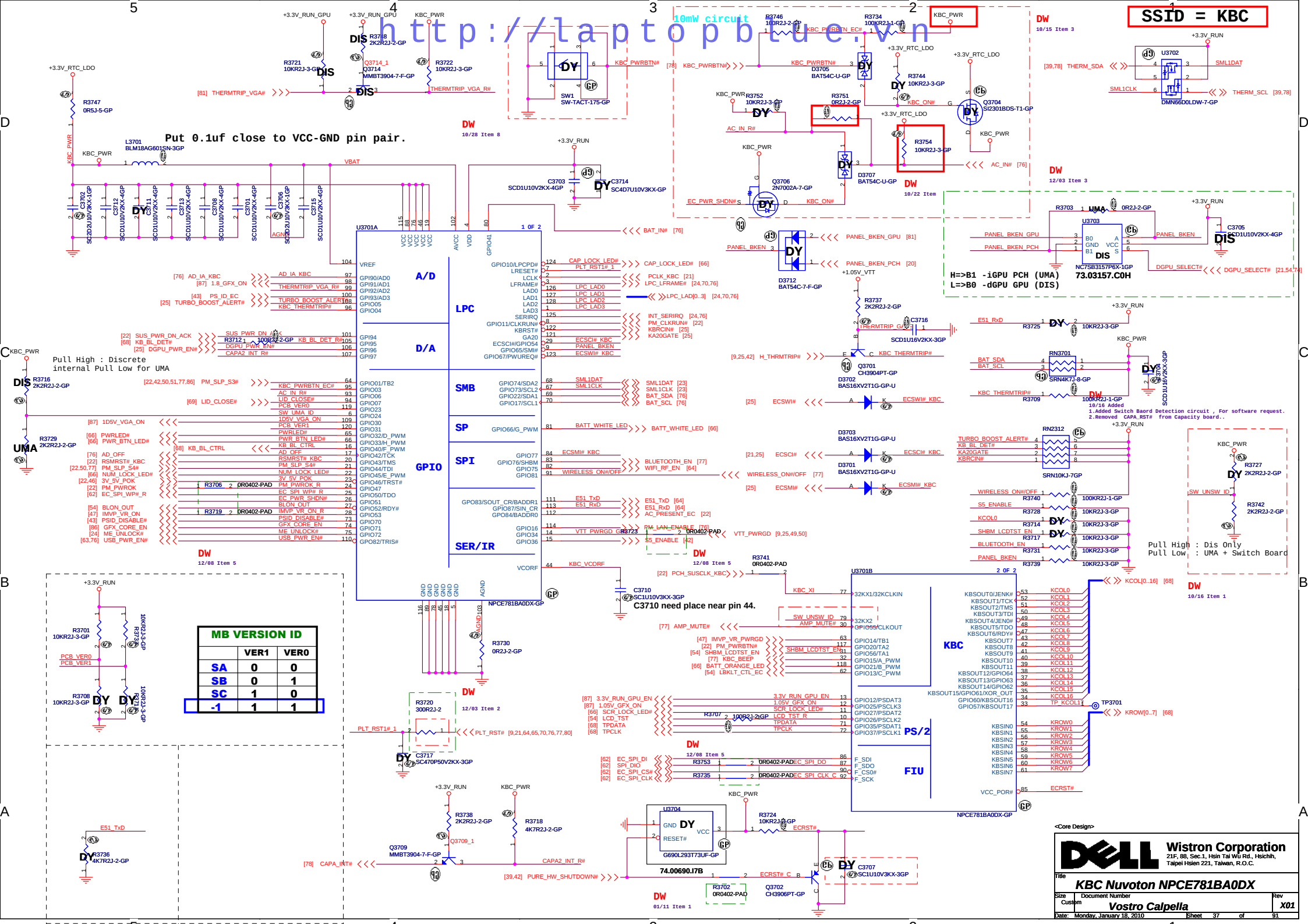
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
A3	*Vostro Calpella*	*X01*

Date: Monday, January 18, 2010 Sheet 36 of 91



(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*X01*

Date: Monday, January 18, 2010 Sheet 38 of 91

SSID = Thermal

25mil

C3910 SC4D7U6D3V5KX-3GP
C3909 SCD1U16V2KX-3GP
R3907 10KR2J-3-GP
R3912 0R2J-2-GP
D3901 B0530WS-7-F-GP
R3901 10KR2J-3-GP
EMC2102_FAN_TACH
EMC2102_FAN_TACH_1
EMC2102_FAN_TACH_1 [58]
EMC2102_FAN_DRIVE
EMC2102_FAN_DRIVE [58]
25mil
RN3901 SRN4K7J-8-GP
THERM_SCL [37,78]
THERM_SDA [37,78]

1. WWAN

Q3905 must be near WWAN
C3912 must be near Q3905
Q3905 CH3904PT-GP
C3912 SC470P50V2JN-GP
C3914 SC470P50V2JN-GP
C3914 must be near EMC2102

Layout notice:
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

2. GPU Sensor

RN3906 SRN0J-6-GP
[81] VGA_THERMDC
[81] VGA_THERMDA
C3906 SC470P50V2JN-GP
C3906 must be near EMC2102
CH2_TDC
CH2_TDA
RN3907 SRN0J-6-GP
Q3904 MMBT3904-3-GP
C3913 SC470P50V3JN-2GP
C3913 must be near Q3904

2. CPU Sensor

Layout notice :
Both VGA_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing.

C3901 must be near Q3901
Q3901 CH3904PT-GP
C3901 SC470P50V2JN-GP
C3903 SC470P50V2JN-GP
C3903 must be near EMC2102

3.HW T8 sensor (CPU)

Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

+3.3V_RUN
R3908 49D9R2F-GP
EMC2102_VDD_3D3
C3905 SCD1U16V2KX-3GP

U3901 EMC2102

29 GND			
28 TACH			
27 VDD_5Va			
26 FANa			
25 FANb			
24 VDD_5Vb			
23 SMCLK			
22 SMDATA			
1 VDD_3V		21 NC#21	
2 DN1	EMC2102_DN1	20 GND	
3 DP1	EMC2102_DP1	19 ALERT#	TP_ALERT# → TP3903 TPAD14-GP
4 DN2	CH2_THERMDC	18 CLK_IN	CLK_32K
5 DP2	CH2_THERMDA	17 CLK_SEL	EMC2102_CLK_SEL → R3906 10KR2J-3-GP → +3.3V_RUN
6 DN3	T8_THERMDC	16 RESET#	TP_EM2102_RESET# → TP3904 TPAD14-GP
7 DP3	T8_THERMDA	15 NC#15	
8 NC#8		14 POWER_OK#	
9 SHDN_SEL		13 THERMTRIP#	EMC2102_THERMTRIP#
10 FAN_MODE		12 SYS_SHDN#	
11 TRIP_SET			

EMC2102-DZK-GP

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

R3903 10KR2J-3-GP — EMC2102_SHDN
R3916 0R2J-2-GP — EMC2102_FAN_mode
R3914 10KR2J-3-GP

RN3902 SRN10KJ-5-GP
EMC2102_PWROK
EMC2102_THERMTRIP#

KBC_PWR
R3910 10KR2J-3-GP
R3917 10KR2J-3-GP
SYS_SHDN#
SHDN
Q3903 2N7002A-7-GP
PURE_HW_SHUTDOWN# [37,42]
V_DEGREE

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

C3902 SCD1U16V2KX-3GP
R3902 10KR2F-2-GP
C3904 SCD1U16V2KX-3GP
R3904 2K37R2F-GP

TRIP_SET Pin Voltage
V_DEGREE=(((Degree-75)/21)
T8 shutdown is set 86 deg-C.

32K suspend clock output

[22] PCH_SUSCLK_2102
Q3902 2N7002A-7-GP
CLK_32K_R
R3913 10R2J-2-GP
CLK_32K
C3911 SC4D7P50V2CN-1GP
RUN_POWER_ON [42]

<Core Design>

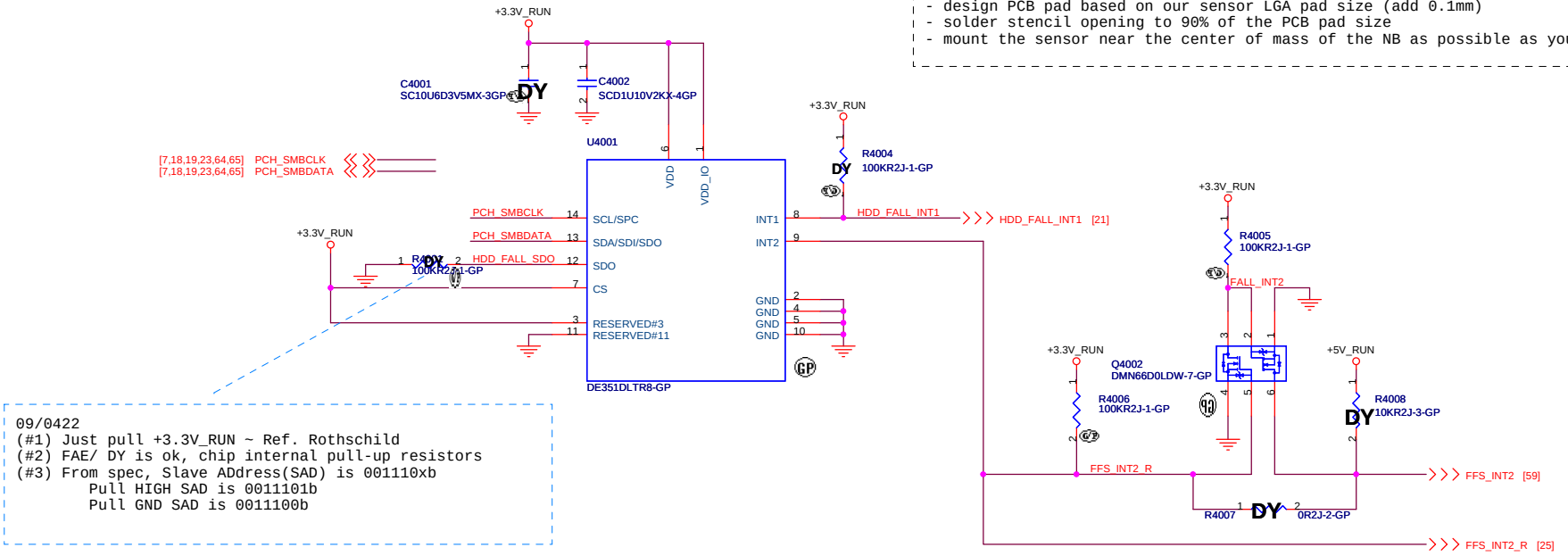
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102
Size: Custom | Document Number: Vostro Calpella | Rev: X01
Date: Monday, January 18, 2010 | Sheet 39 of 91

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



09/0422
(#1) Just pull +3.3V_RUN ~ Ref. Rothschild
(#2) FAE/ DY is ok, chip internal pull-up resistors
(#3) From spec, Slave ADdress(SAD) is 001110xb
Pull HIGH SAD is 0011101b
Pull GND SAD is 0011100b

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Free Fall Sensor

Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 40 of 91

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*X01*

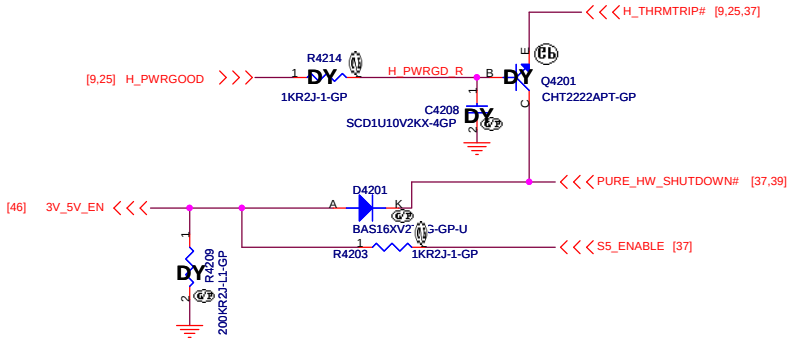
Date: Monday, January 18, 2010 Sheet 41 of 91

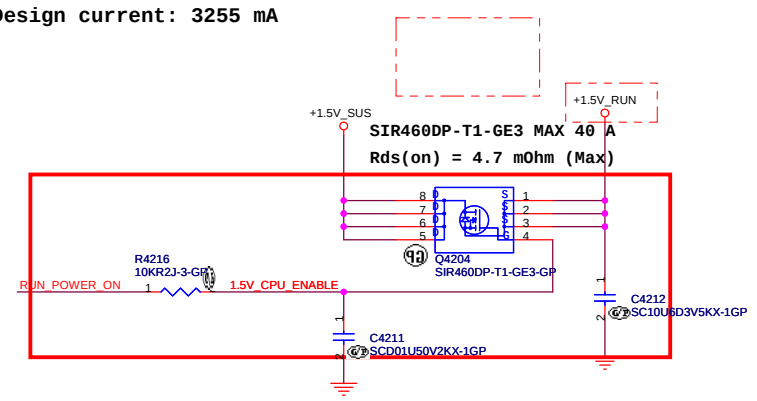
SSID = Reset.Suspend

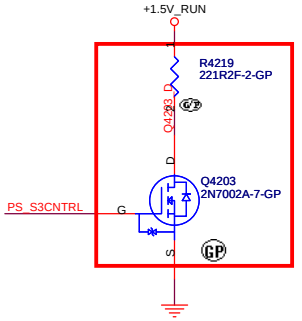
+1.5V_RUN:

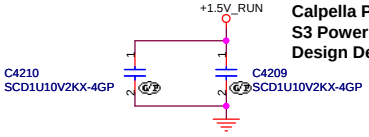
Peak current: 4650 mA
Design current: 3255 mA

DW
10/26 Item 3







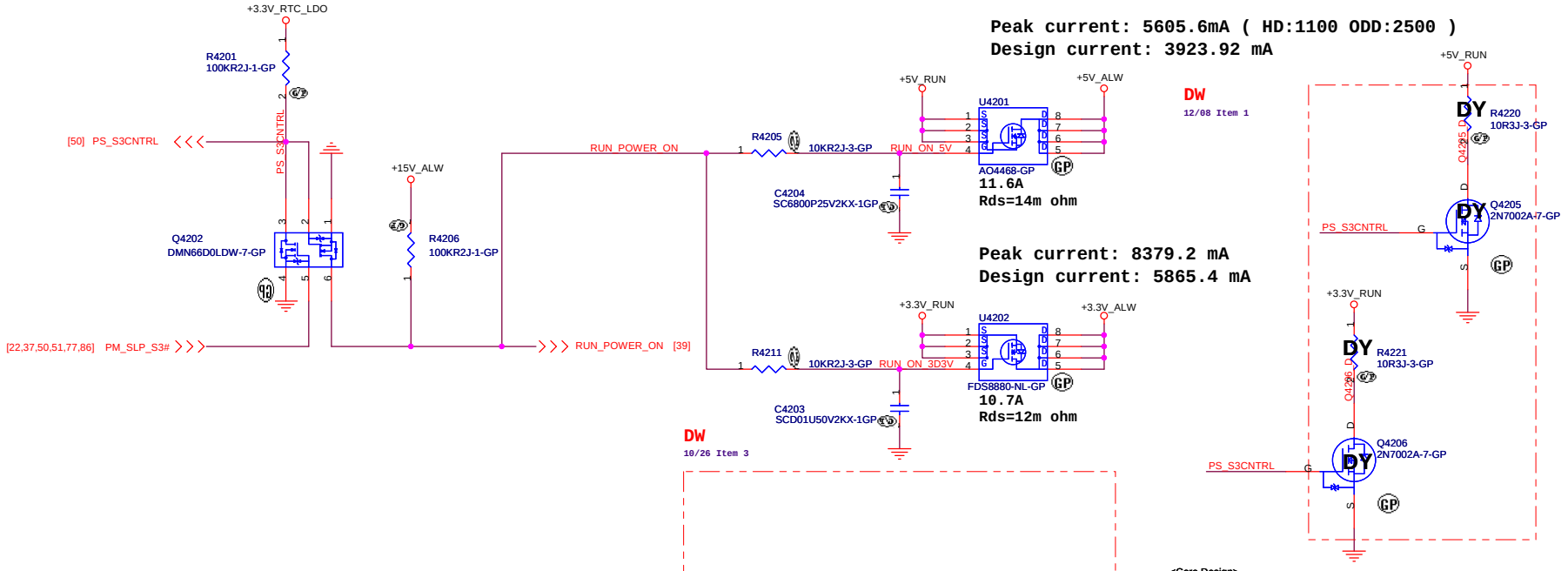


Calpella Platform S3 Power Reduction Platform
S3 Power Reduction CRB Implementation
Design Details

Revision 0.1

Peak current: 5605.6mA (HD:1100 ODD:2500)
Design current: 3923.92 mA

DW
12/08 Item 1



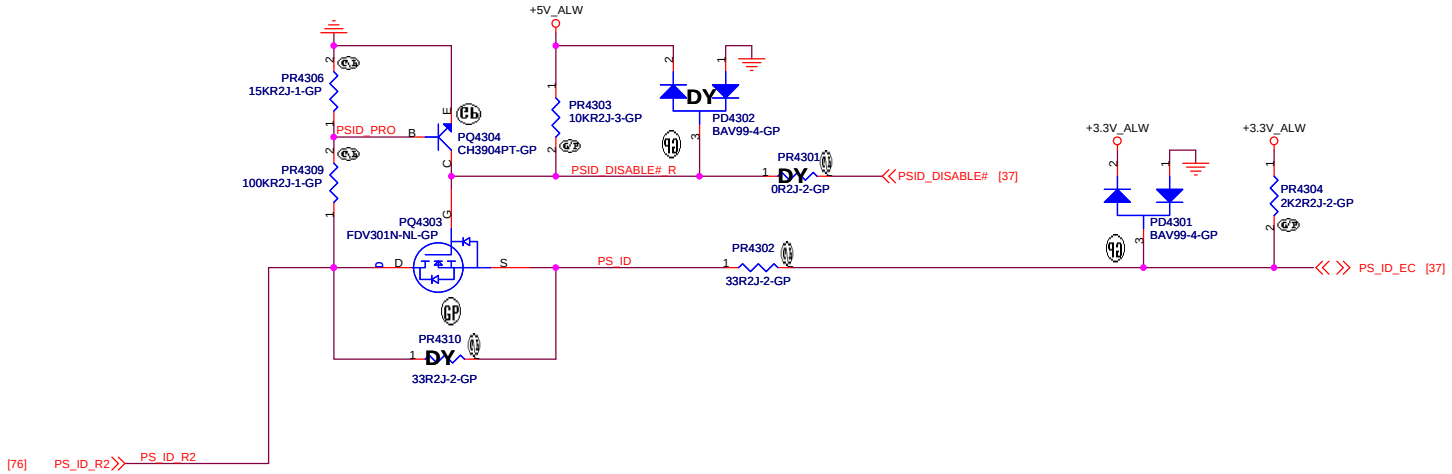
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Plane Enable***

Size: Custom | Document Number: ***Vostro Calpella*** | Rev: ***X01***

Date: Monday, January 18, 2010 | Sheet 42 of 91



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC IN

Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 43 of 91

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserve)*

Size: A3 | Document Number: *Vostro Calpella* | Rev: *X01*

Date: Monday, January 18, 2010 | Sheet 44 of 91

(Blank)

<Core Design>

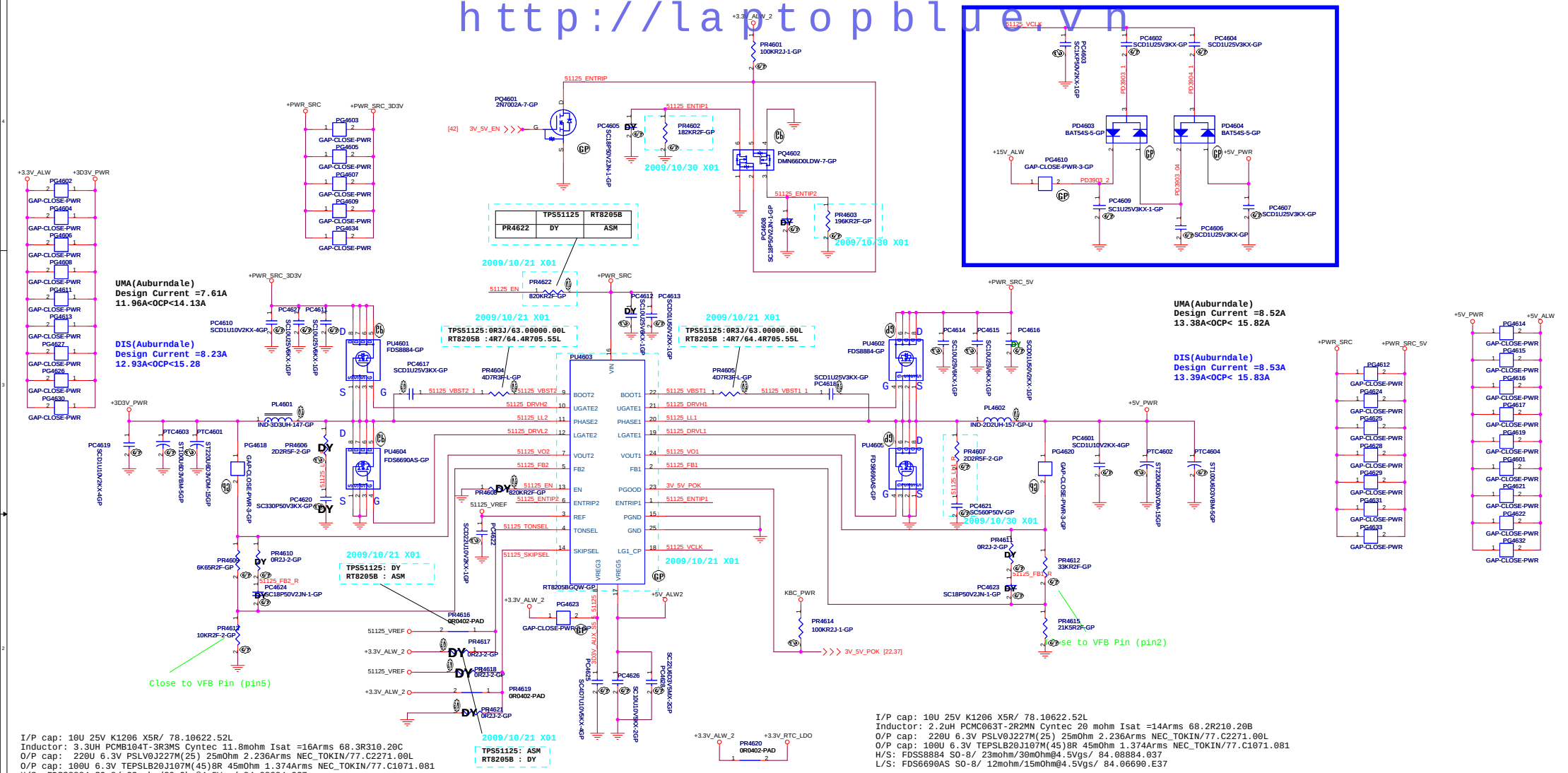
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*X01*

Date: Monday, January 18, 2010 Sheet 45 of 91



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMB104T-3R3MS Cyntec 11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 20 mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

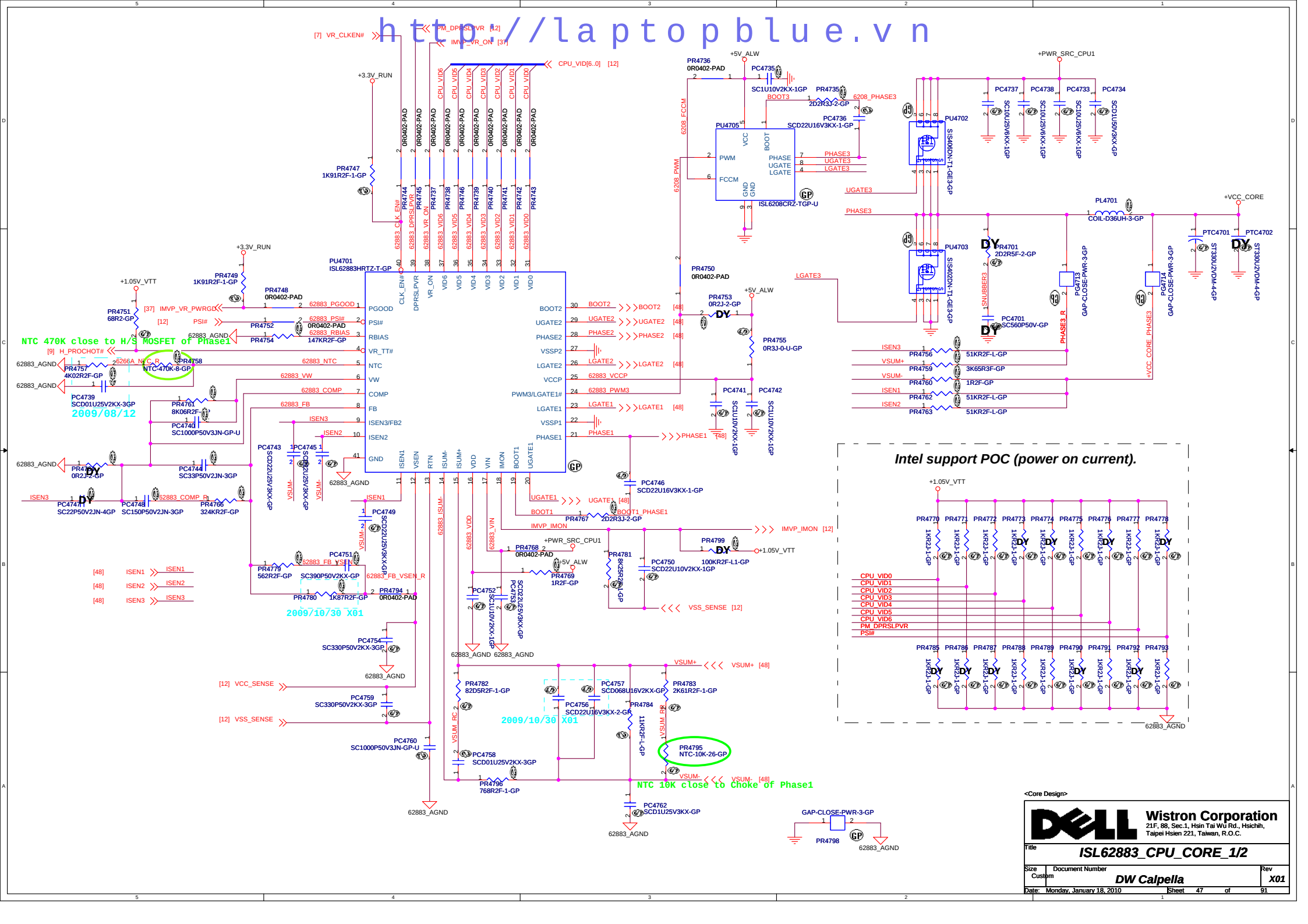
<Core Design>

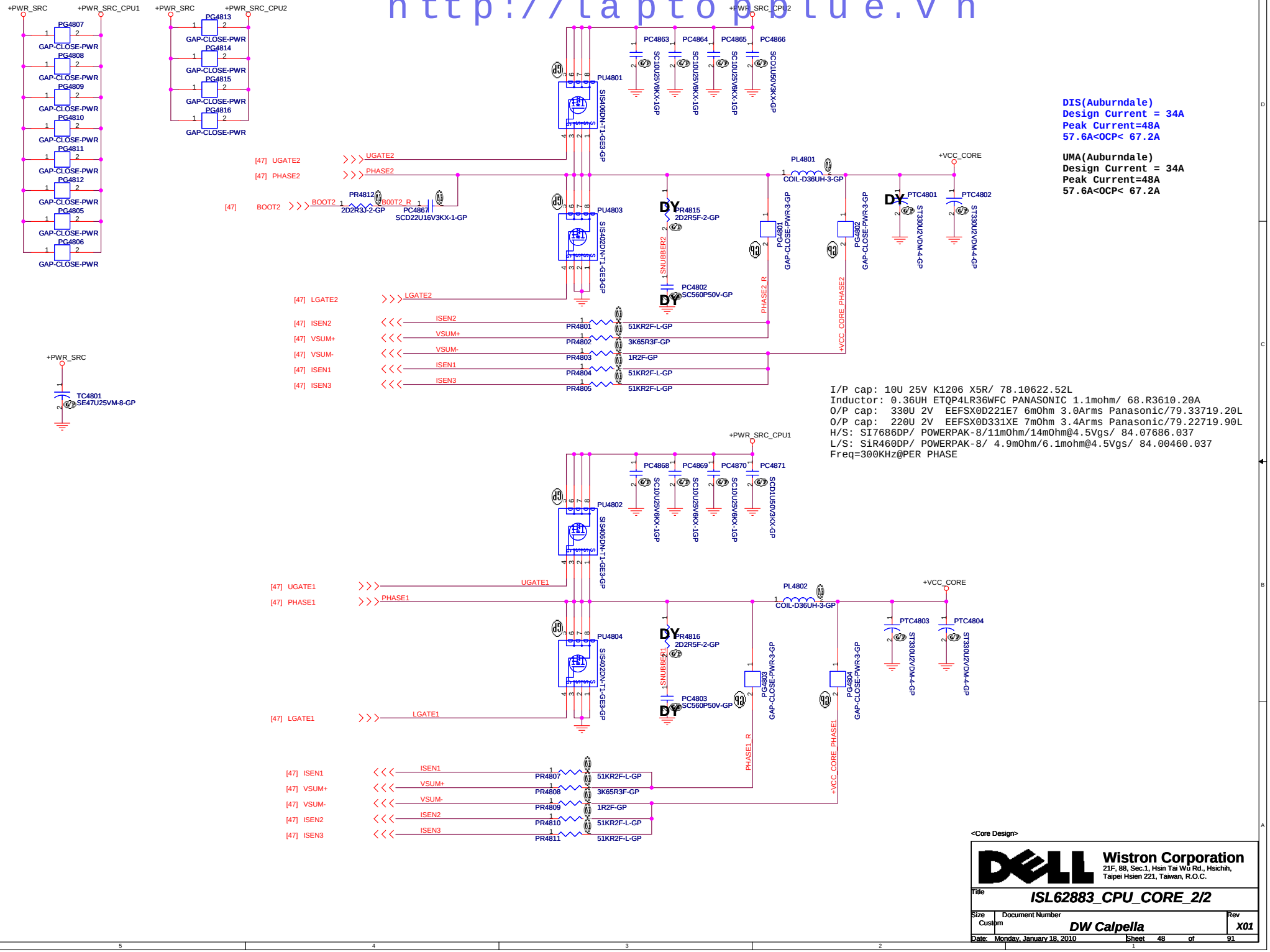
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8205B_5V/3D3V

Size: Custom | Document Number: DW Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 46 of 91





DIS(Auburndale)
Design Current = 34A
Peak Current=48A
57.6A<OCP< 67.2A

UMA(Auburndale)
Design Current = 34A
Peak Current=48A
57.6A<OCP< 67.2A

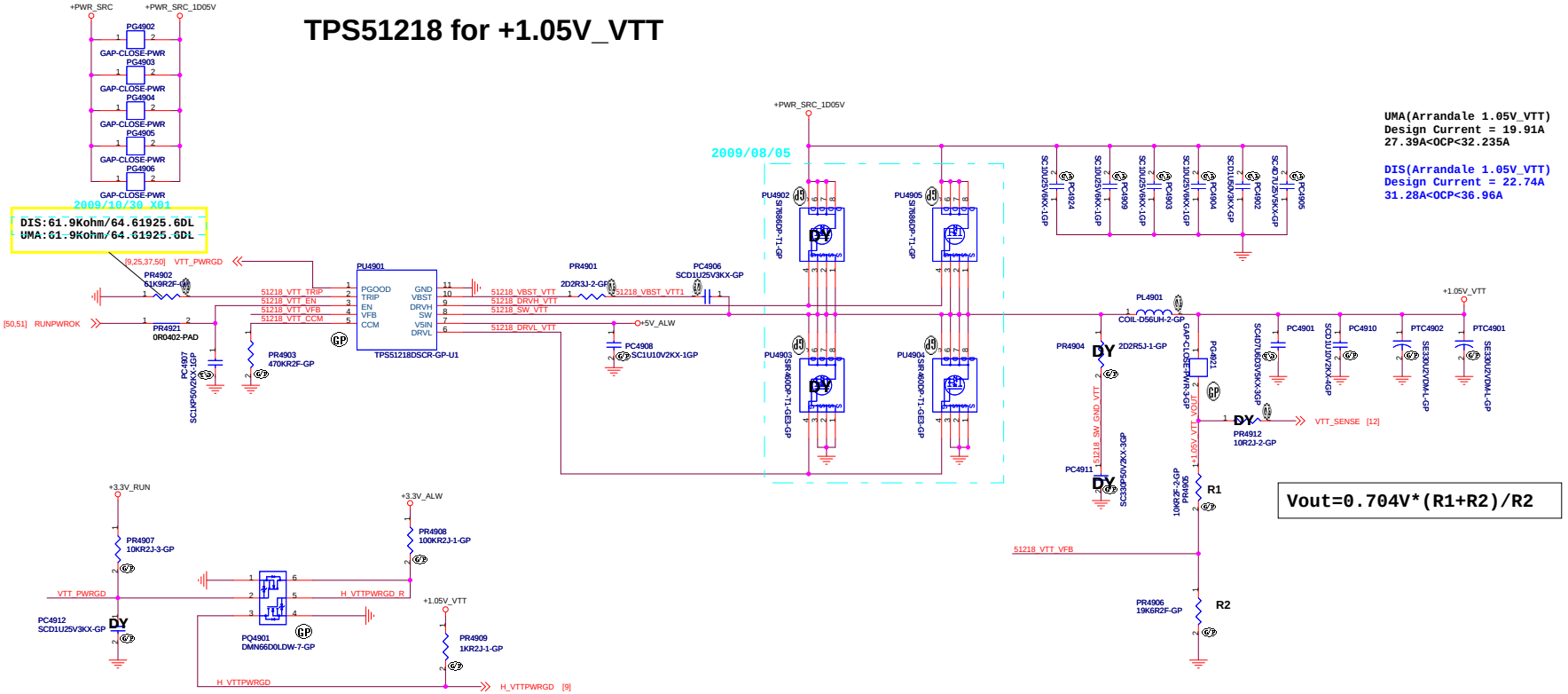
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L
O/P cap: 220U 2V EEFSX0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Freq=300KHz@PER PHASE

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ISL62883_CPU_CORE_2/2	
Size: Custom	Document Number: DW Calpella	Rev: X01
Date: Monday, January 18, 2010	Sheet 48 of 91	

TPS51218 for +1.05V_VTT



UMA(Arrandale 1.05V_VTT)
Design Current = 19.91A
27.39A<OCP<32.235A

DIS(Arrandale 1.05V_VTT)
Design Current = 22.74A
31.28A<OCP<36.96A

Vout=0.704V*(R1+R2)/R2

Frequency setting
470K -->290KHz
200K -->340KHz
100K -->380KHz
39K -->430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SIR474DP-T1-GE3/10mohm/ 12mOhm@4.5Vgs/ 84.00474.037
L/S: SI7170DP-T1-GE3/3.6mOhm/4.3mohm@4.5Vgs/ 84.07170.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218 +1.05V_VTT

Size	Document Number	Rev
Custom	DW Calpella	X01

Date: Monday, January 18, 2010 Sheet 49 of 91

SSID = PWR.Plane.Regulator_1p5v0p75v

2009/10/30 X01

DIS:12.4Kohm/64.12425.6DL
UMA:7.5Kohm/64.75015.6DL

TPS51116RGER-GP-U

Design Current = 0.7A

DW
10/29 Item 1

DIS(Auburndale)
Design Current = 11.82A
18.57A<OCP<21.95A

UMA(Auburndale)
Design Current = 8.86A
13.92A<OCP<16.45A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: FDS8880 SO-8/ 9.6mOhm/12mOhm @4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq-->400KHz

425302_425302_Calpella_S3PowerReduction_WhitePape
Revision 0.7

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

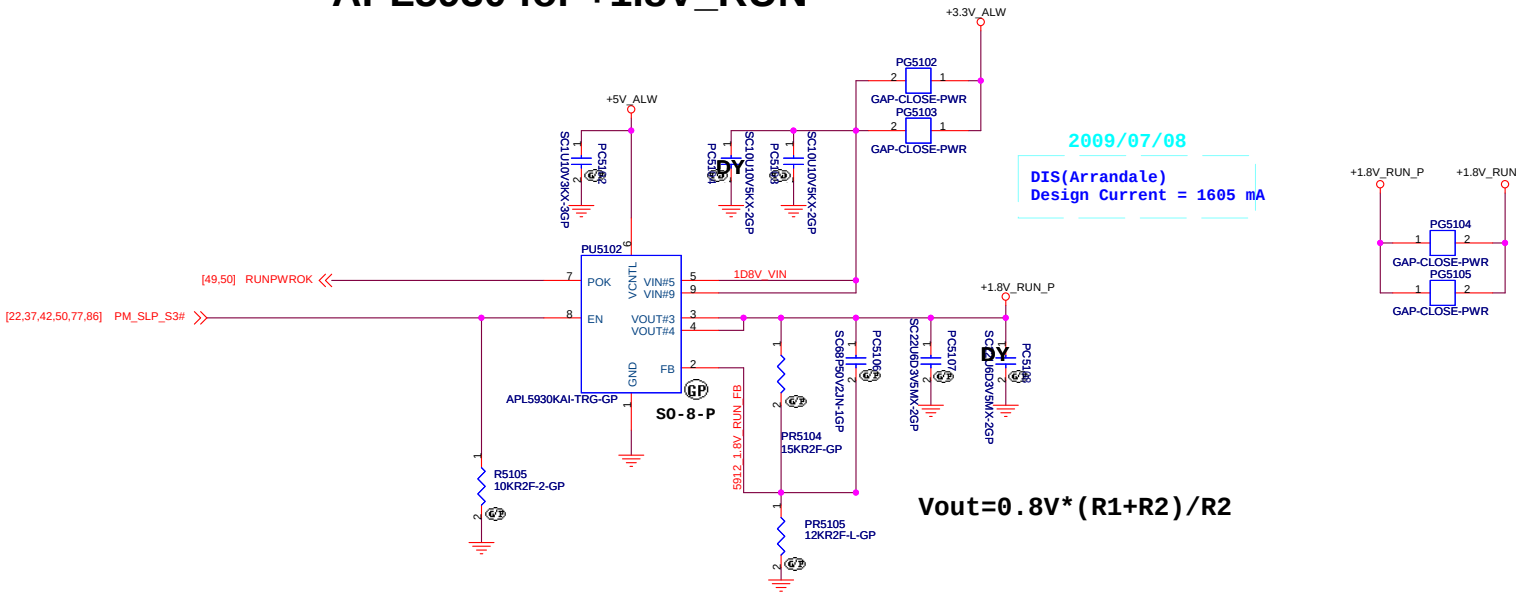
Title: TPS51116_+1.5V_SUS

Size: Custom | Document Number: DW Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 50 of 91

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



Vout=0.8V*(R1+R2)/R2

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APL5930 +1.8V_RUN

Size: Custom | Document Number: DW Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 51 of 91

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

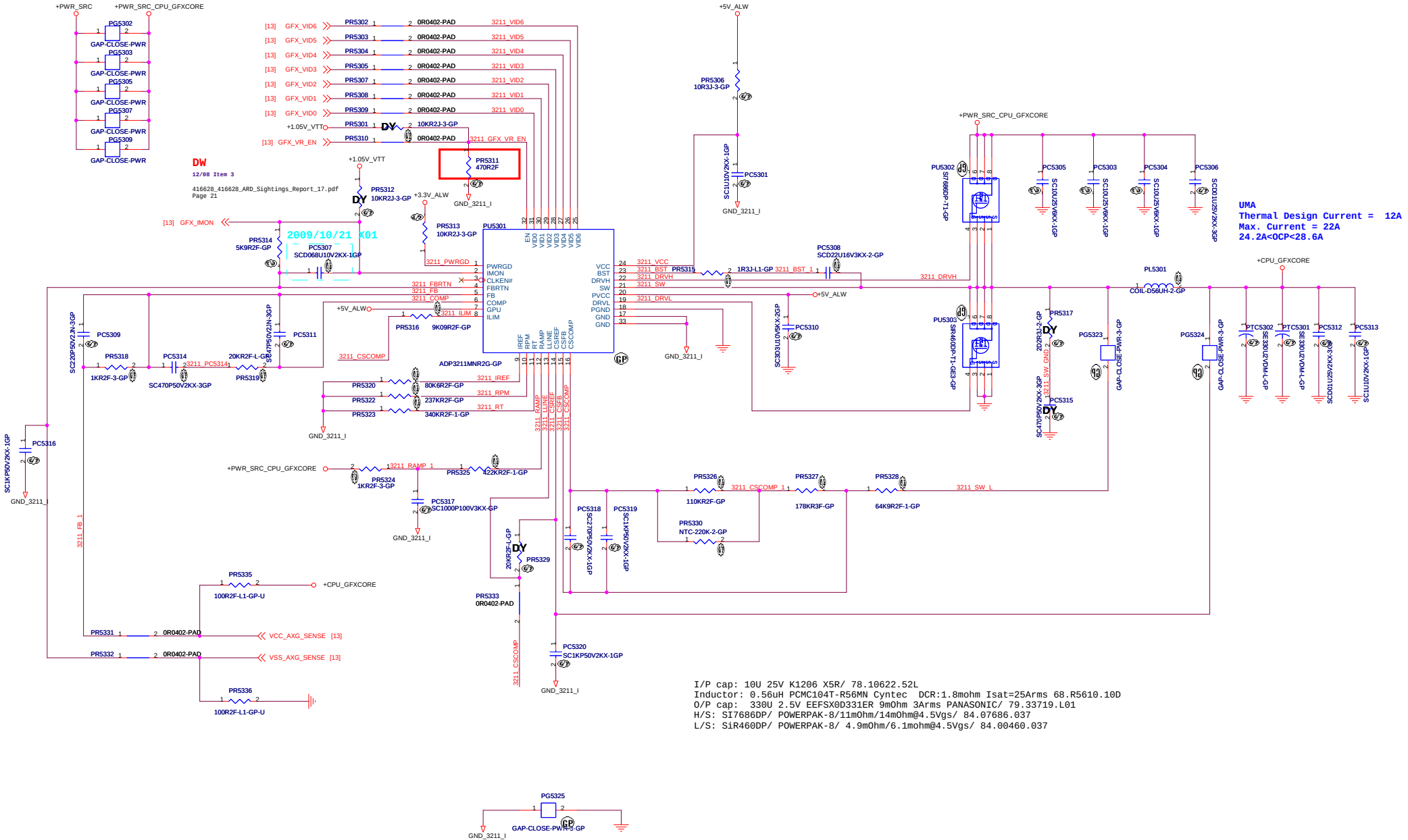
Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*X01*

Date: Monday, January 18, 2010 Sheet 52 of 91

SSID = CPU.GFX.Regulator



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

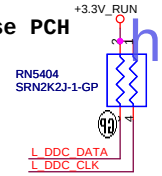
Title: ADP3211 CPU GFXCORE

Size: Custom | Document Number: DW Calpella UMA | Rev: X01

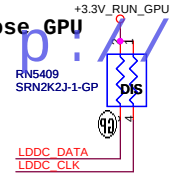
Date: Monday, January 18, 2010 | Sheet 53 of 91

SSID = VIDEO

Close PCH

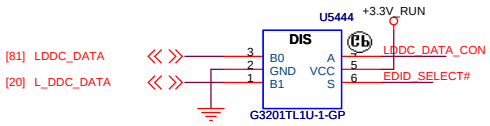


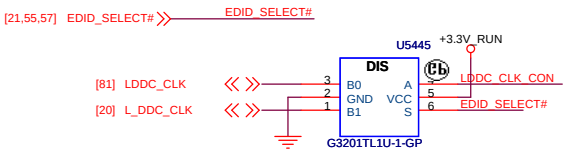
Close GPU

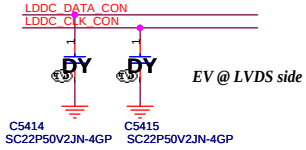


UMA/DIS LVDS DDC CLK/DAT select circuit

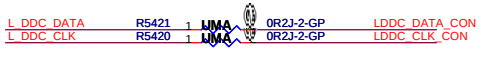
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

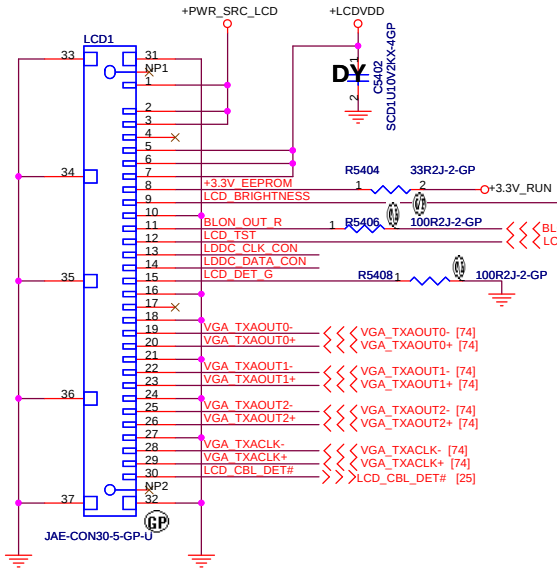






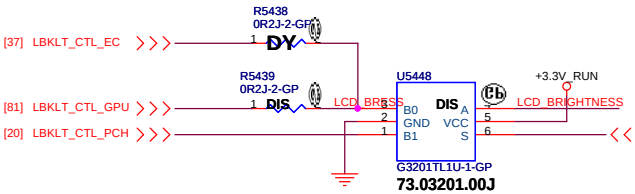
LVDS CONNECTOR



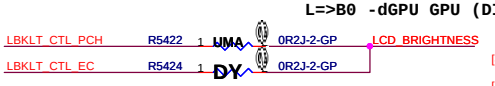


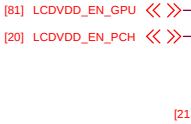
20.F1555.030

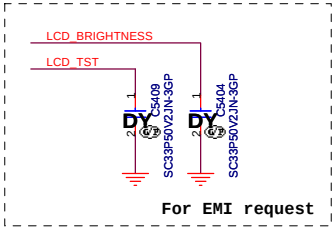
UMA/DIS LVDS PWM select circuit

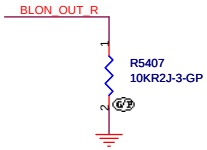


H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)



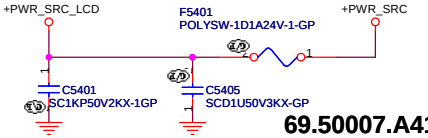






SSID = Inverter

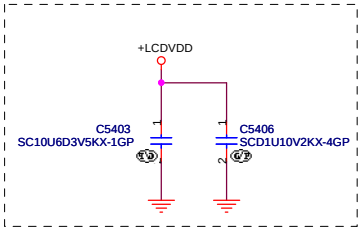
INVERTER POWER

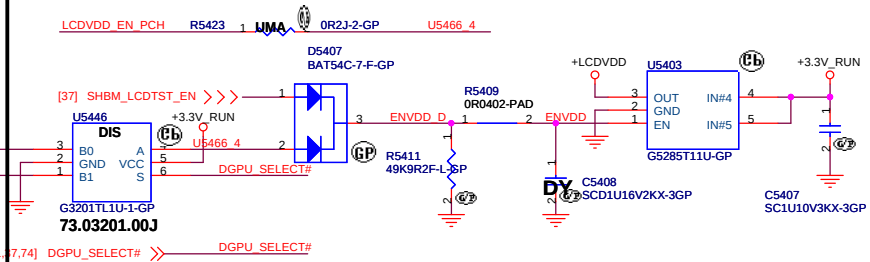


69.50007.A41
2ND : 69.50007.A31

SSID = VIDEO

LCD POWER





H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

<Core Design>

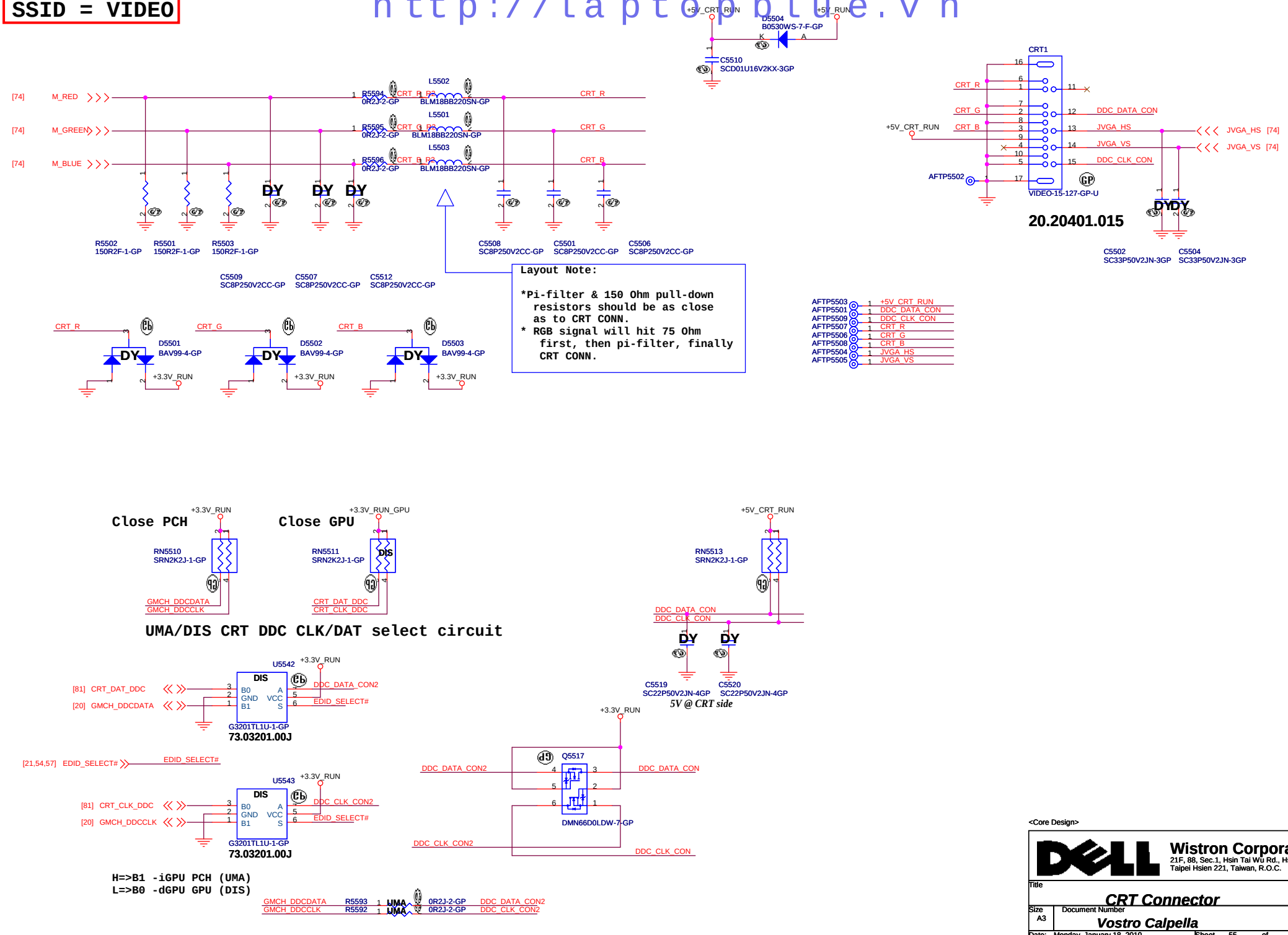
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 54 of 91

SSID = VIDEO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size	Document Number	Rev
A3	Vostro Calpella	X01

Date: Monday, January 18, 2010 Sheet 55 of 91

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

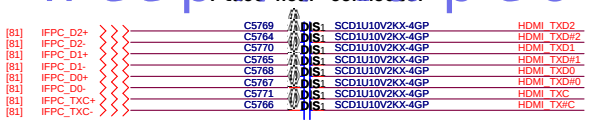
(Reserve)

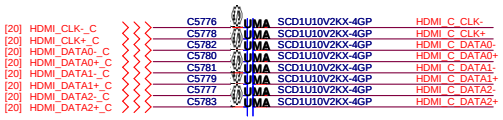
Size	Document Number	Rev
Custom	*Vostro Calpella*	*X01*

Date: Monday, January 18, 2010 Sheet 56 of 91

UMA/DIS HDMI signal select circuit

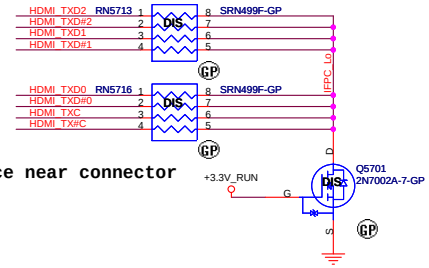
Place near connector

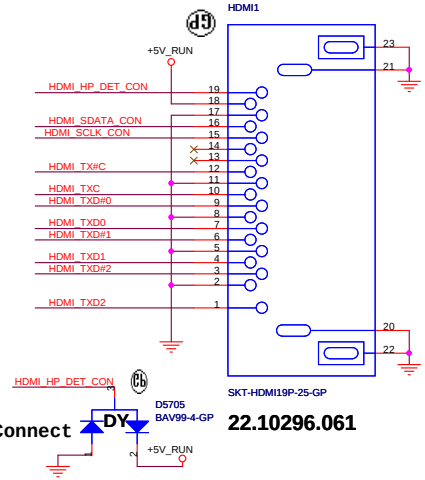




Close to PCH

Place near connector





Close HDMI Connect

22.10296.061

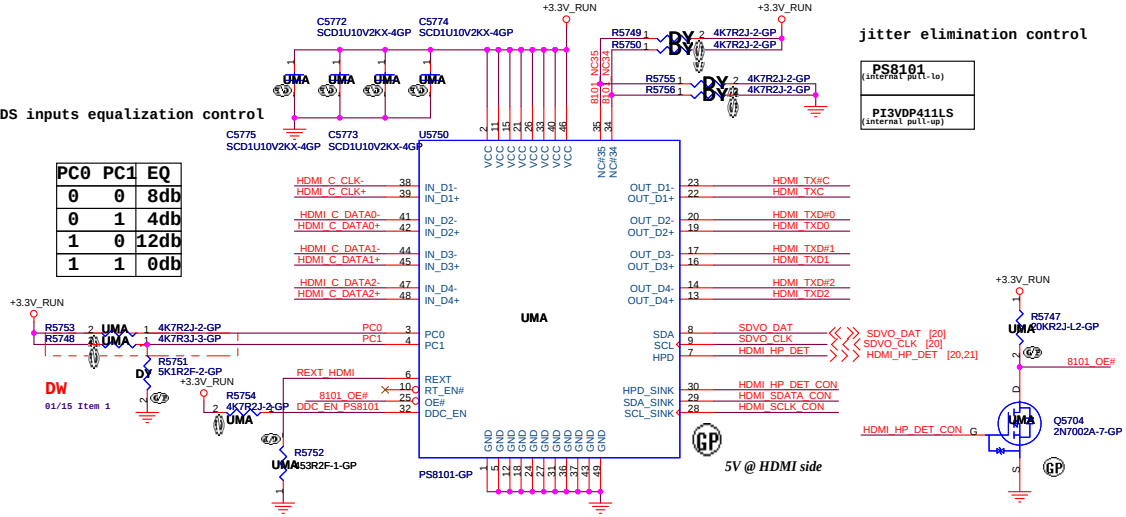
UMA HDMI level shift circuit

PS8101 TMDS inputs equalization control

PC0	PC1	EQ
0	0	8db
0	1	4db
1	0	12db
1	1	0db

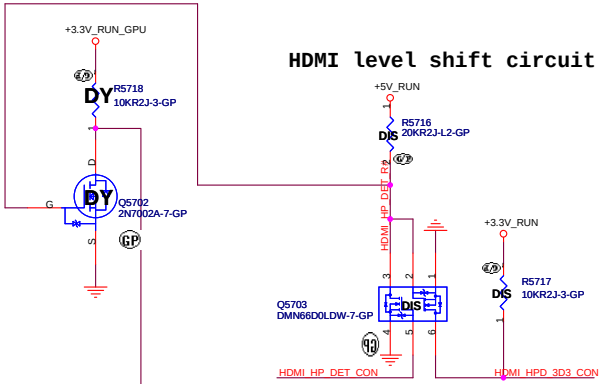
jitter elimination control

PS8101 (internal pull-lo)
PI3VDP411LS (internal pull-up)

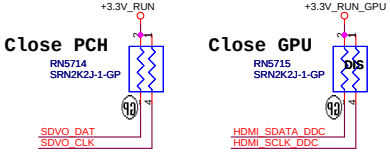


5V @ HDMI side

71.P8101.003 (PARADE)
2ND = 71.03360.A0K (NXP)



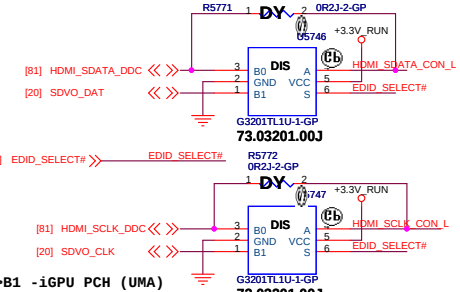
HDMI level shift circuit



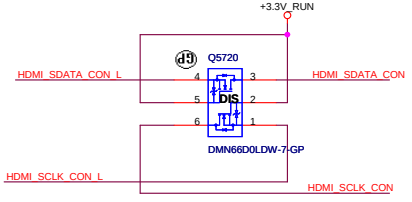
Close PCH

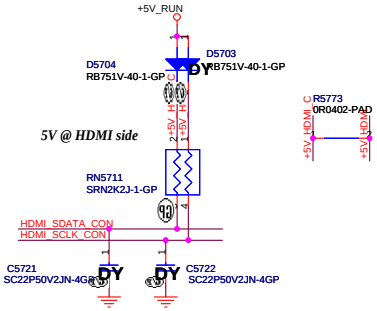
Close GPU

UMA/DIS HDMI DDC CLK/DAT select circuit



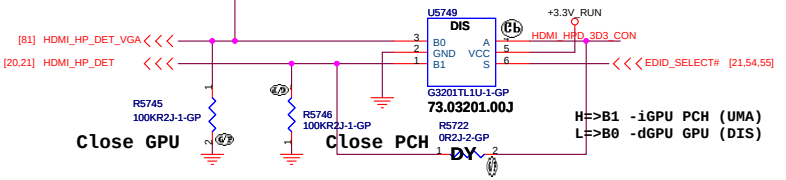
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)





R5773 0R0402-PAD

UMA/DIS HDMI Detection select circuit



Close GPU

Close PCH

H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

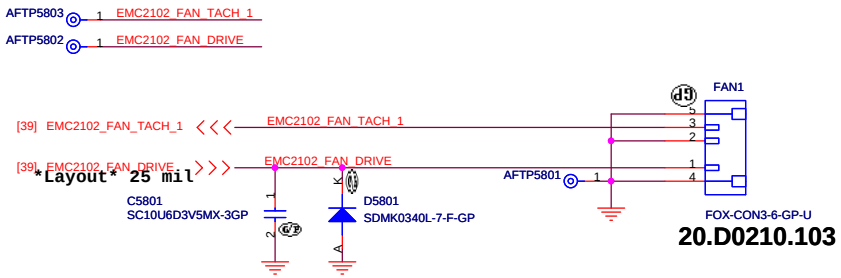
Title: HDMI Connector

Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 57 of 91

SSID = Thermal

Fan Connector



<Core Design>

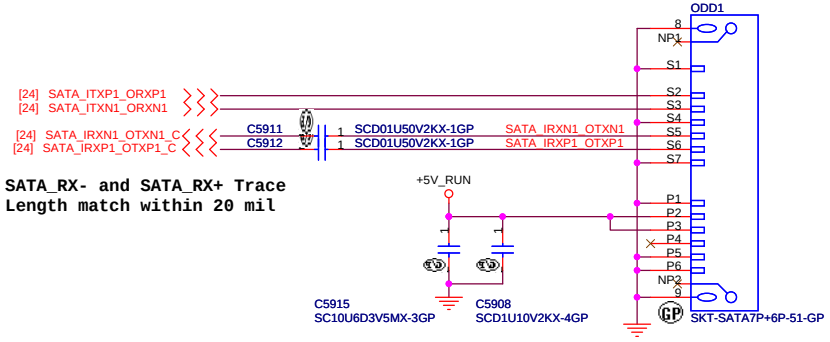
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FAN		
Size: A3	Document Number: Vostro Calpella	Rev: X01
Date: Monday, January 18, 2010	Sheet 58 of 91	

SSID = SATA

SSID = SATA

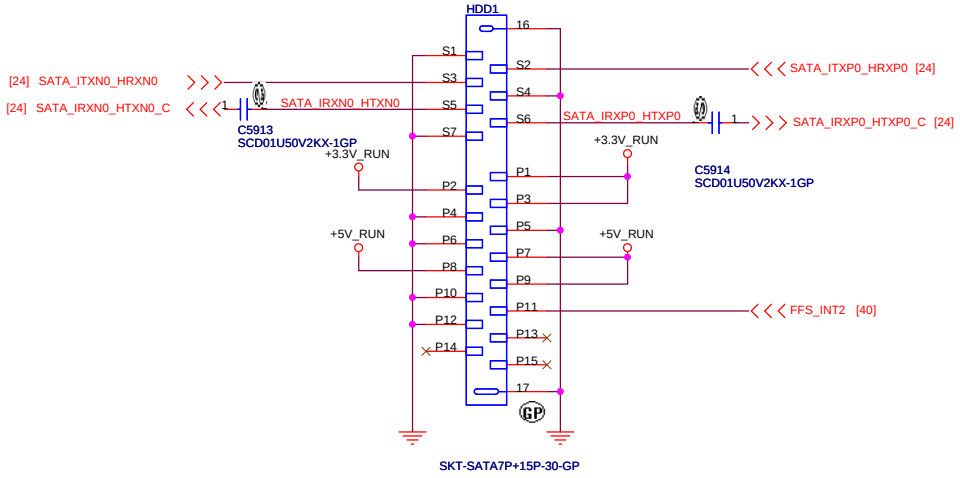
ODD Connector



SATA_RX- and SATA_RX+ Trace Length match within 20 mil

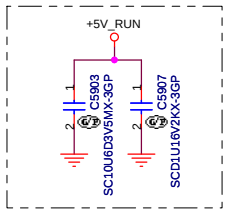
62.10065.671

SATA HDD Connector

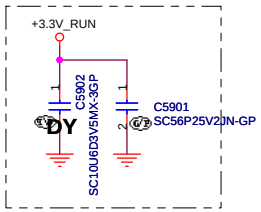


62.10065.911

Close to CONN 5V power pin



Close to CONN 3.3V power pin



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD Connector		
Size: A3	Document Number: Vostro Calpella	Rev: X01
Date: Monday, January 18, 2010	Sheet 59 of 91	

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*X01*

Date: Monday, January 18, 2010 Sheet 60 of 91

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

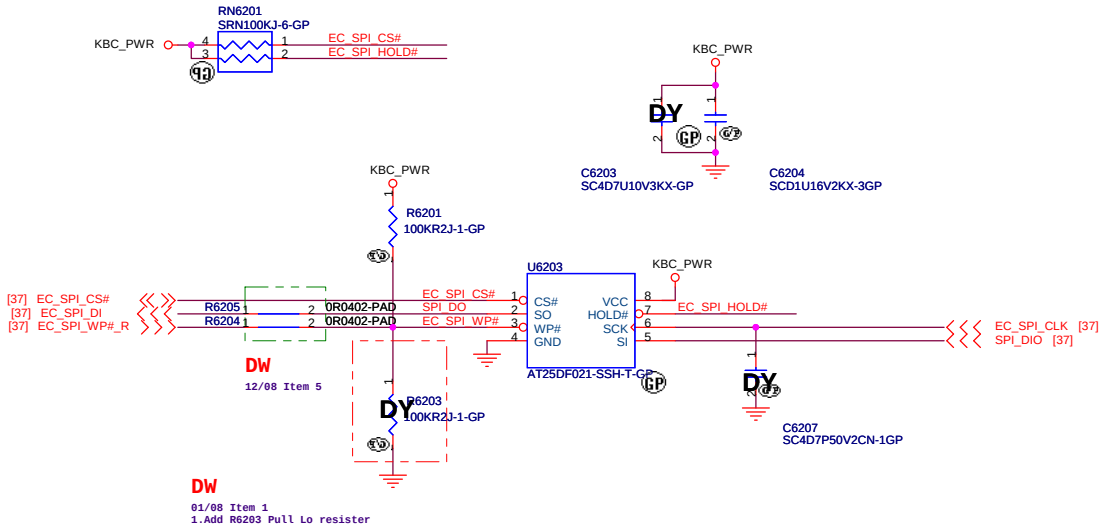
(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*X01*

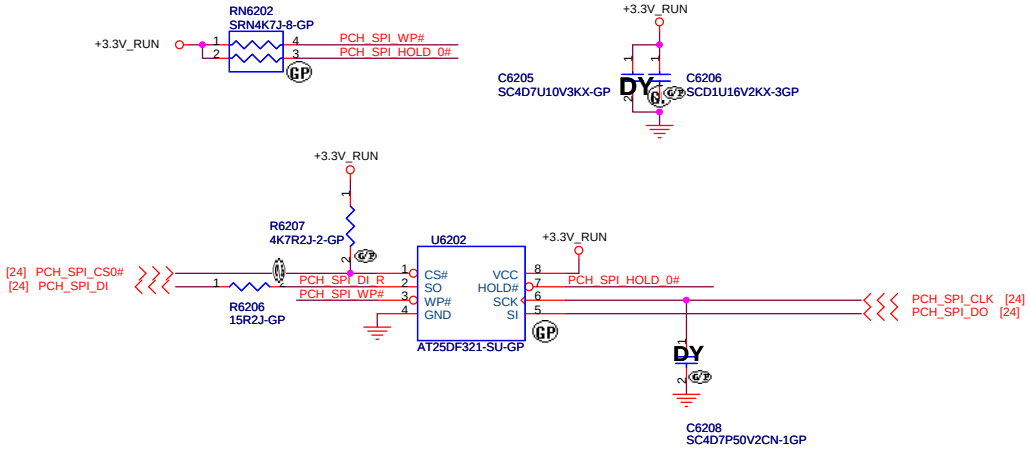
Date: Monday, January 18, 2010 Sheet 61 of 91

SSID = Flash.ROM

SPI FLASH ROM (256K bytes) for KBC

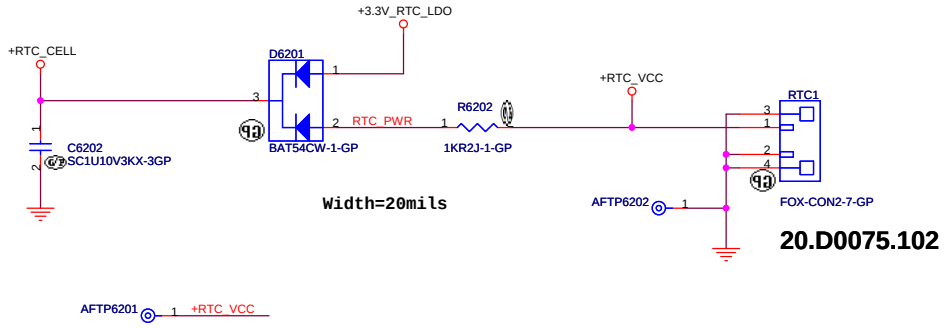


SPI FLASH ROM (4M bytes) for PCH



SSID = RBATT

RTC Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

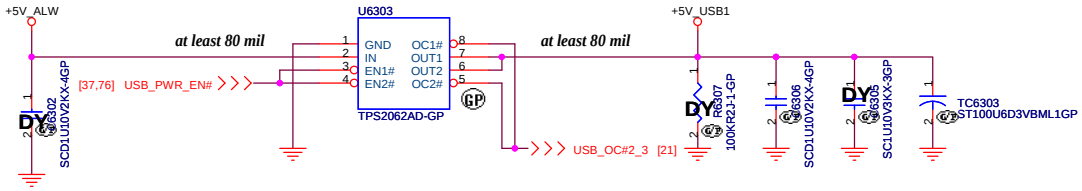
Title: EEPROM/RTC Connector

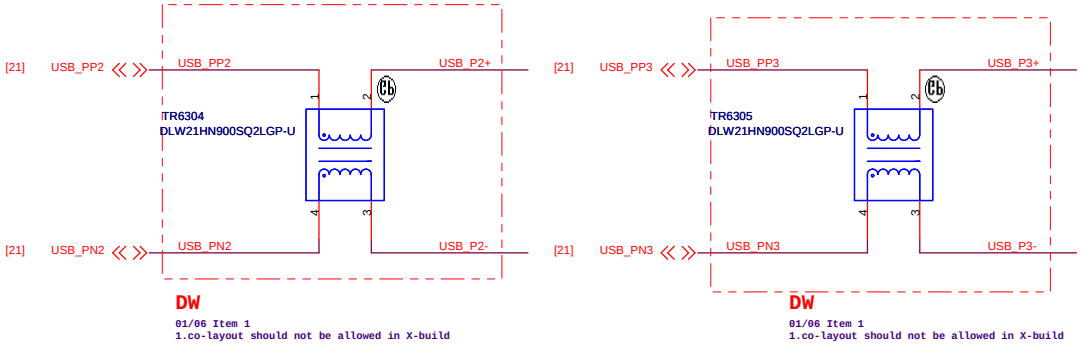
Size	Document Number	Rev
A3	Vostro Calpella	X01

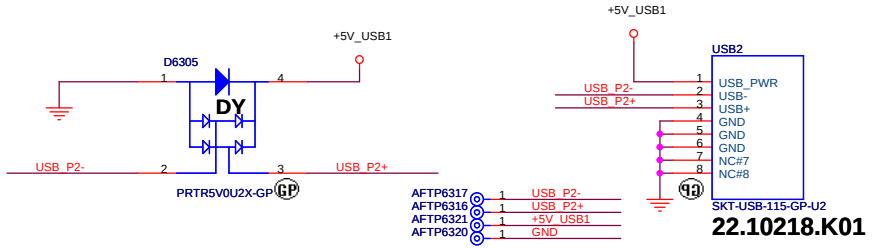
Date: Monday, January 18, 2010 Sheet 62 of 91

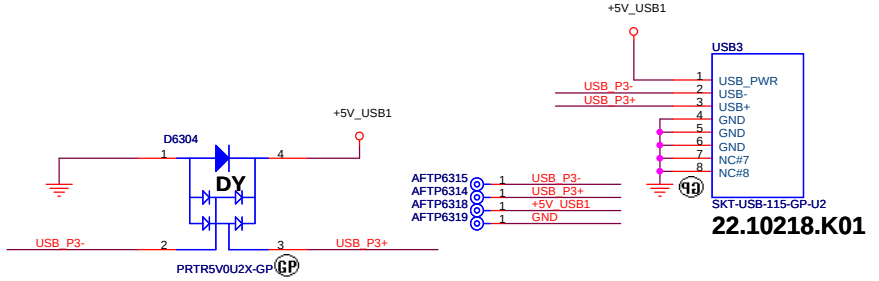
SSID = USB

USB Power

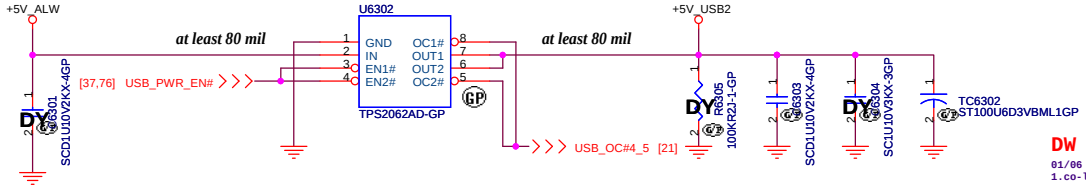


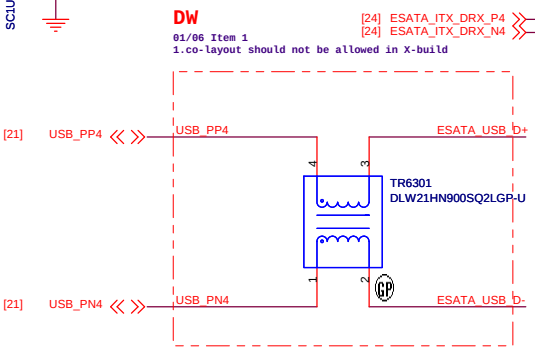


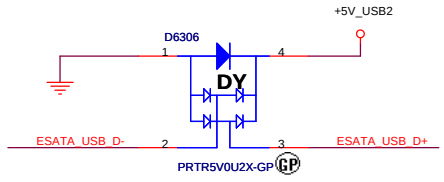


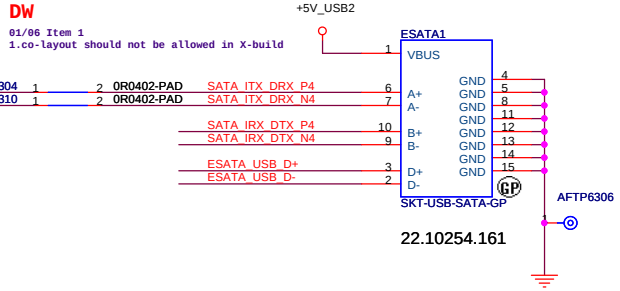


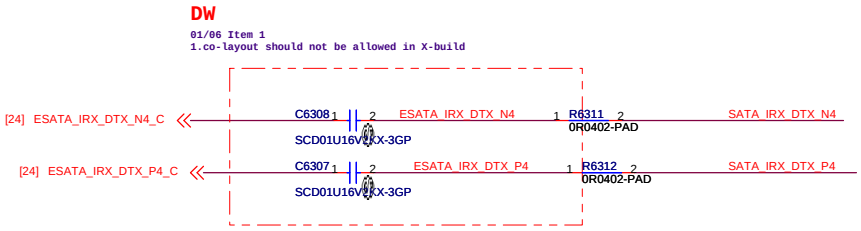
ESATA Power

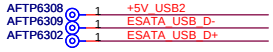












<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

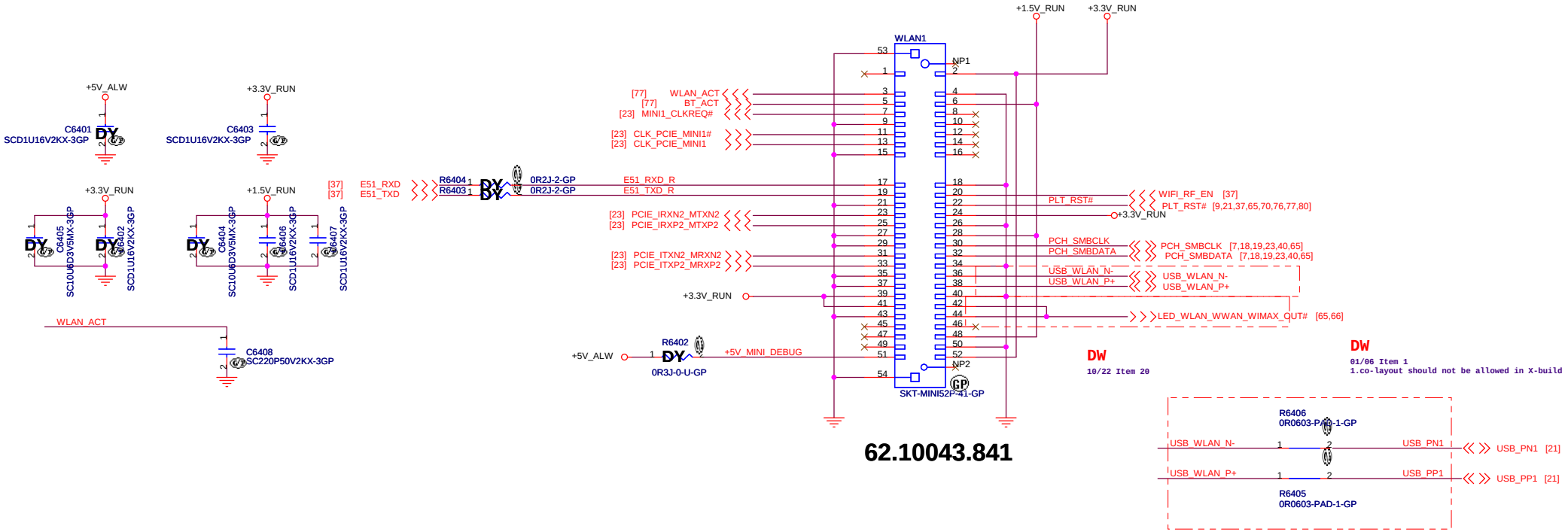
Title: USB /ESATA Port

Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 63 of 91

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



DW
10/22 Item 20

DW
01/06 Item 1
1.co-layout should not be allowed in X-build

62.10043.841

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

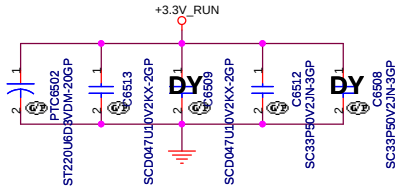
Size	Document Number	Rev
A3	Vostro Calpella	X01

Date: Monday, January 18, 2010 Sheet 64 of 91

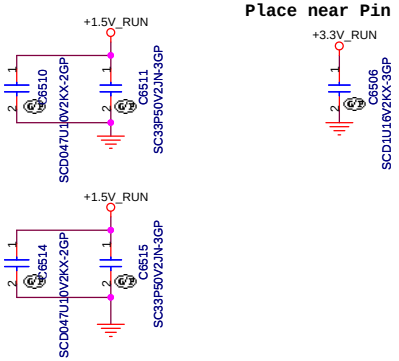
SSID = Wireless

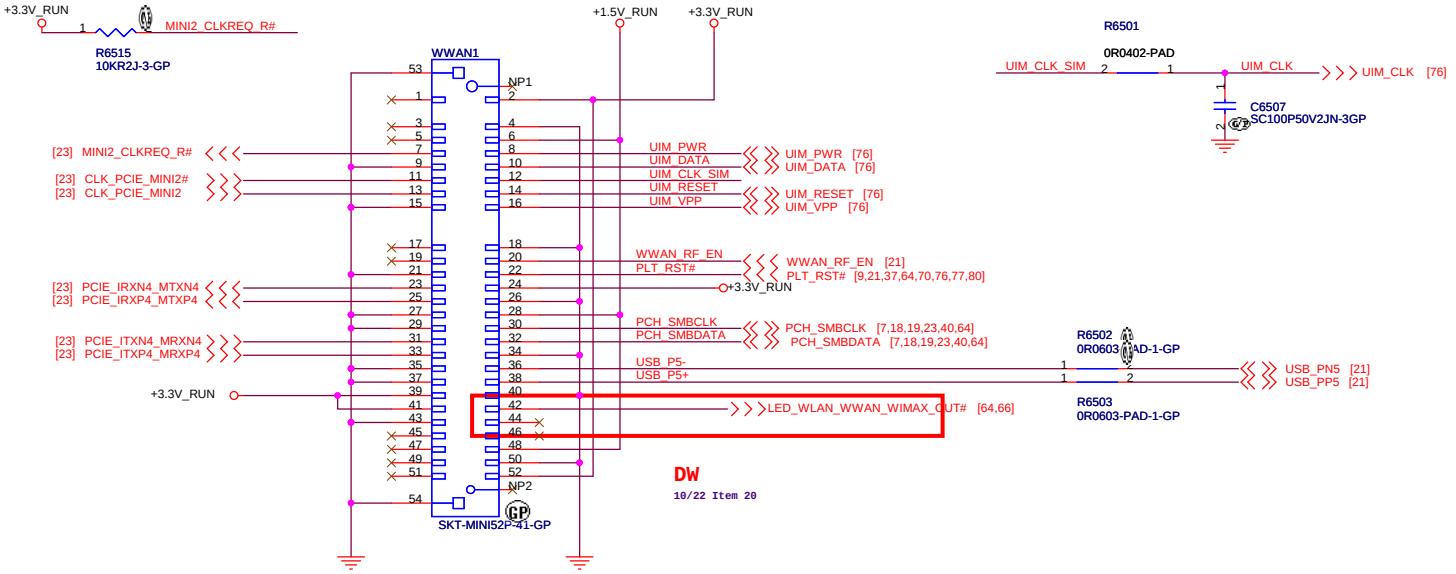
Mini Card Connector(WWAN)

Place near MINI Card CONN



Place near Pin 24





62.10043.841

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	WWAN Connector	
Size: A3	Document Number: Vostro Calpella	Rev: X01
Date: Monday, January 18, 2010	Sheet 65 of 91	

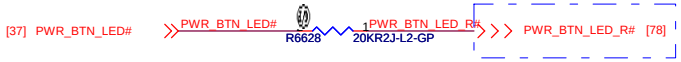
For LED & Capacity board:

LED Type	Color	Power rail
SCRL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WLAN WWAN WIMAX LED	White	RUN

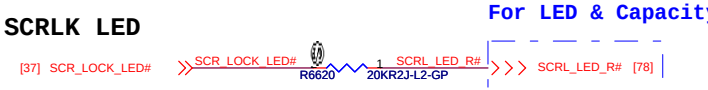
For IO board

LED Type	Color	Power rail
PWR LED2	White(Multi-color)	ALW
BATTERY LED2	Amber(Multi-color)	ALW
	White(Multi-color)	ALW

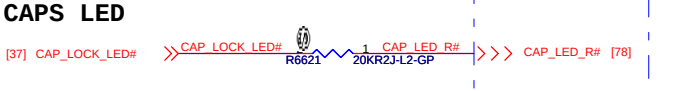
PWR BTN LED



SCRLK LED



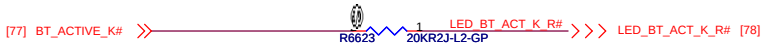
CAPS LED



NUM LED

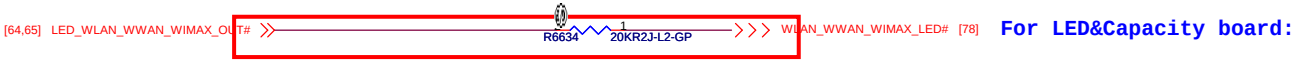
Remove BJT to daughetr board

Bluetooth LED

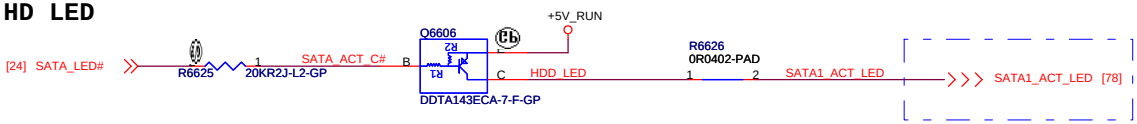


WLAN WWAN WIMAX LED

DW
10/22 Item 20

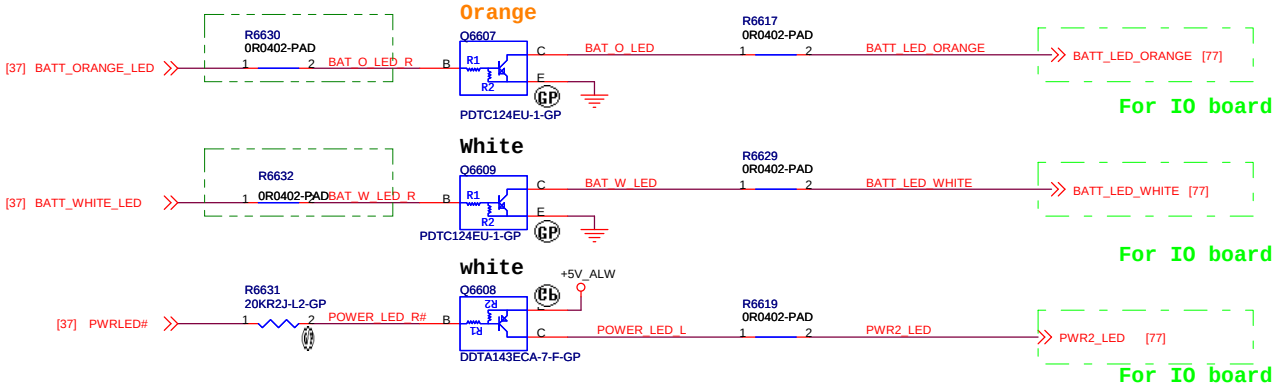


HD LED



Battery & Power LED

DW
12/08 Item 5



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED

Size	Document Number	Rev
A3	Vostro Calpella	X01

Date: Monday, January 18, 2010 Sheet 66 of 91

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

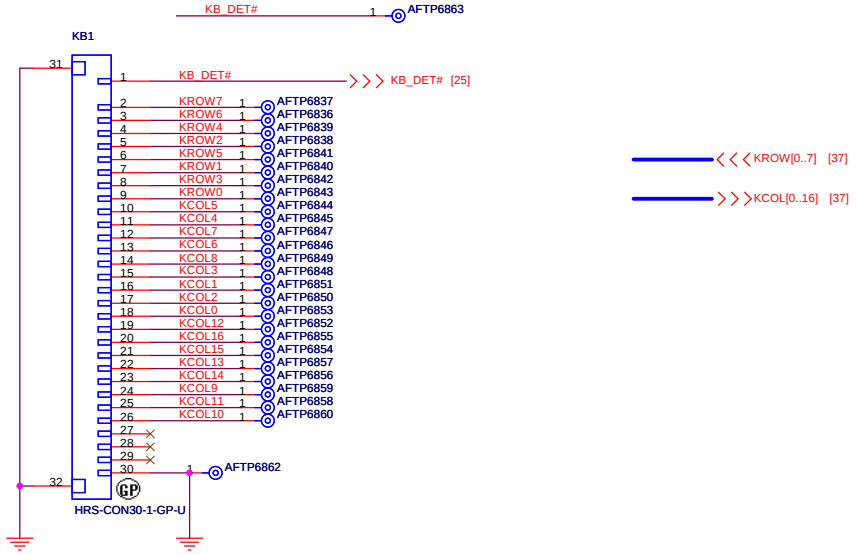
(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*X01*

Date: Monday, January 18, 2010 Sheet 67 of 91

SSID = KBC

Internal KeyBoard Connector

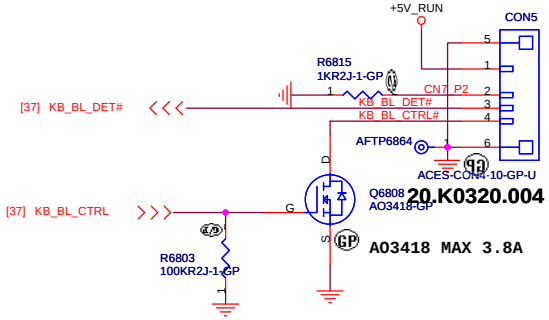


KROW[0..7] [37]

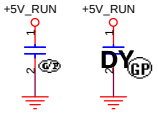
KCOL[0..16] [37]

20.K0259.030

KB Backlight CONN



AFTP6833 1 +5V_RUN
AFTP6832 1 CN7_P2
AFTP6834 1 KB_BL_DET#
AFTP6861 1 KB_BL_CTRL#



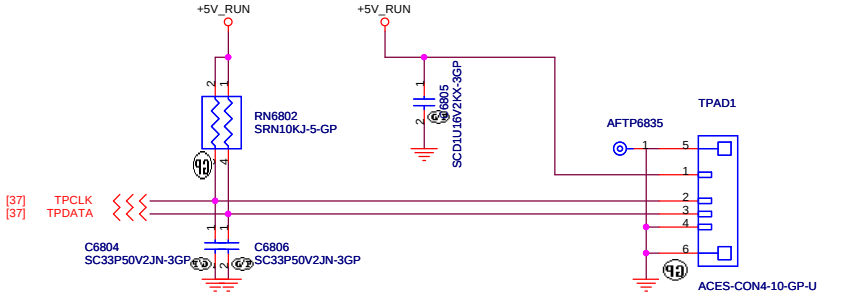
C6812 SCD1U25V2ZY-1GP

C6895 SC4D7U10V5KX-1GP

Place near CON5

SSID = Touch.Pad

TouchPad Connector



20.K0320.004

AFTP6815 1 +5V_RUN
AFTP6816 1 TPCLK
AFTP6817 1 TPDATA

<Core Design>

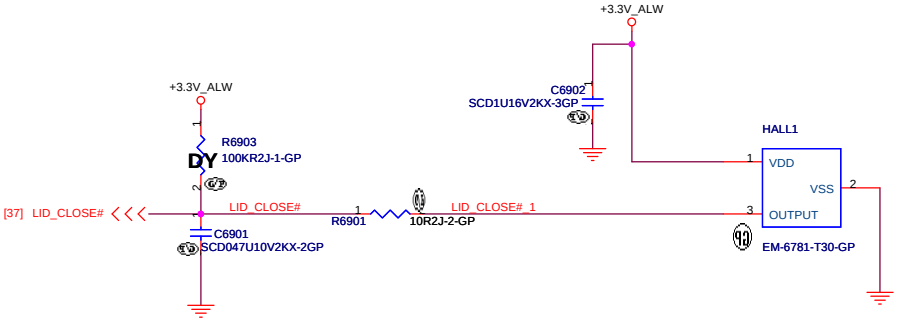
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Keyboard/Touch Pad

Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 68 of 91

Hall Sensor Connector



<Core Design>

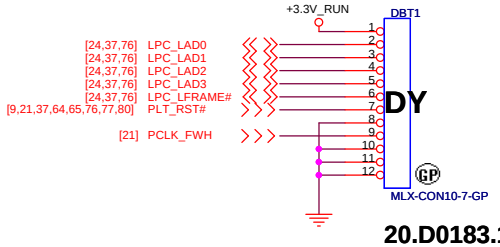
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Hall sensor

Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 69 of 91

GOLDEN FINGER FOR DEBUG BOARD



20.D0183.110

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Debug port***	
Size: Custom	Document Number: ***Vostro Calpella***	Rev: ***X01***
Date: Monday, January 18, 2010	Sheet 70 of 91	

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*X01*

Date: Monday, January 18, 2010 Sheet 71 of 91

(Blank)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

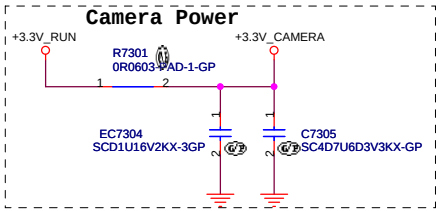
Title: *(Reserve)*

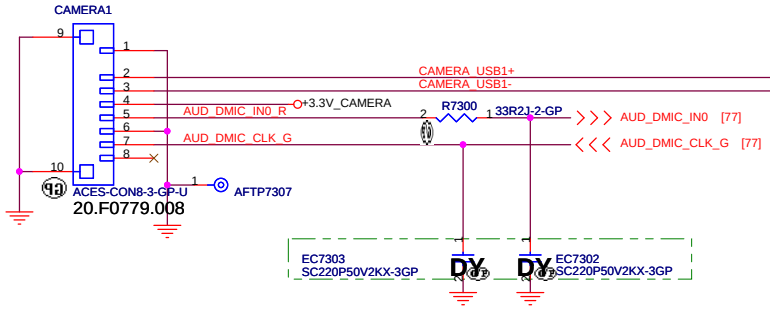
Size: Custom | Document Number: *Vostro Calpella* | Rev: *X01*

Date: Monday, January 18, 2010 | Sheet 72 of 91

SSID = User.Interface

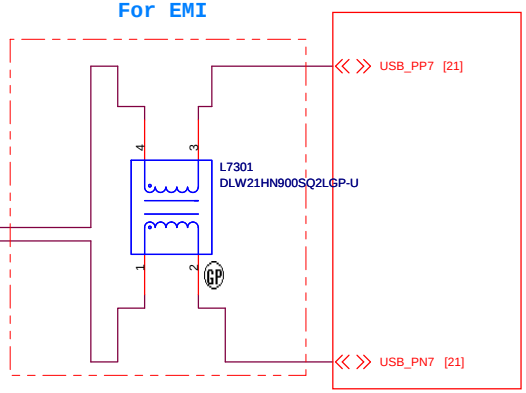
Camera Connector





DW
12/08 Item 5

For EMI



DW
01/18 Item 1

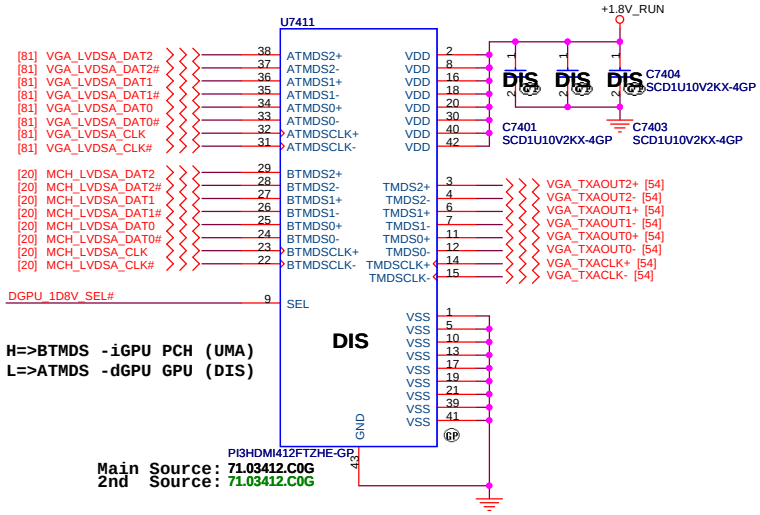
DW
01/06 Item 1
1.co-layout should not be allowed in X-build

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Camera CONN		
Size: A3	Document Number: Vostro Montevina Discrete	Rev: X01
Date: Monday, January 18, 2010	Sheet 73 of 91	

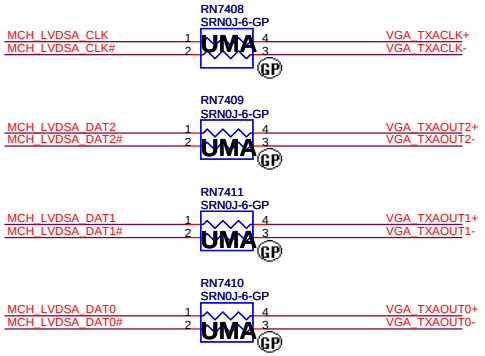
UMA/DIS LVDS signal select circuit



H=>BTMDS -iGPU PCH (UMA)
L=>ATMDS -dGPU GPU (DIS)

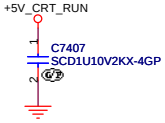
Main Source: 71.03412.C0G
2nd Source: 71.03412.C0G

UMA LVDS signal circuit



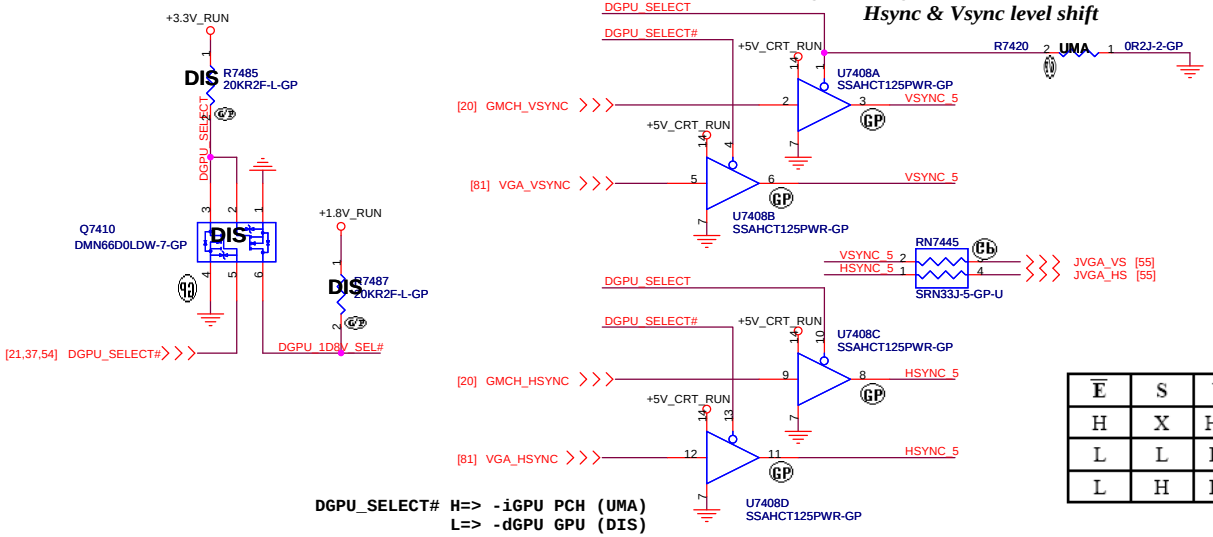
FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-



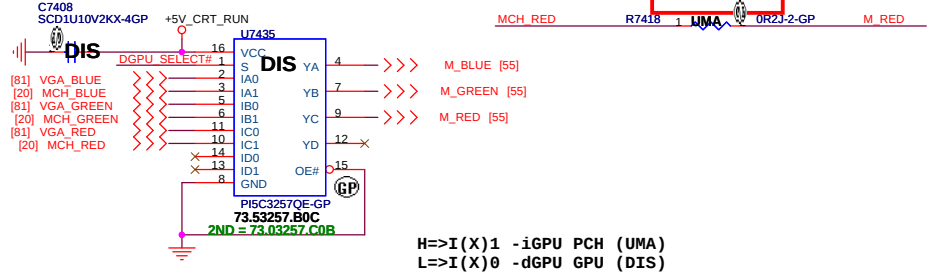
UMA/DIS CRT Hsync/Vsync select circuit

Hsync & Vsync level shift



DGPU_SELECT# H=> -iGPU PCH (UMA)
L=> -dGPU GPU (DIS)

UMA/DIS CRT signal select circuit



DW
10/23 Item 25

H=>I(X)1 -iGPU PCH (UMA)
L=>I(X)0 -dGPU GPU (DIS)

$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Swith-1

Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 74 of 91

(Blank)

<Core Design>

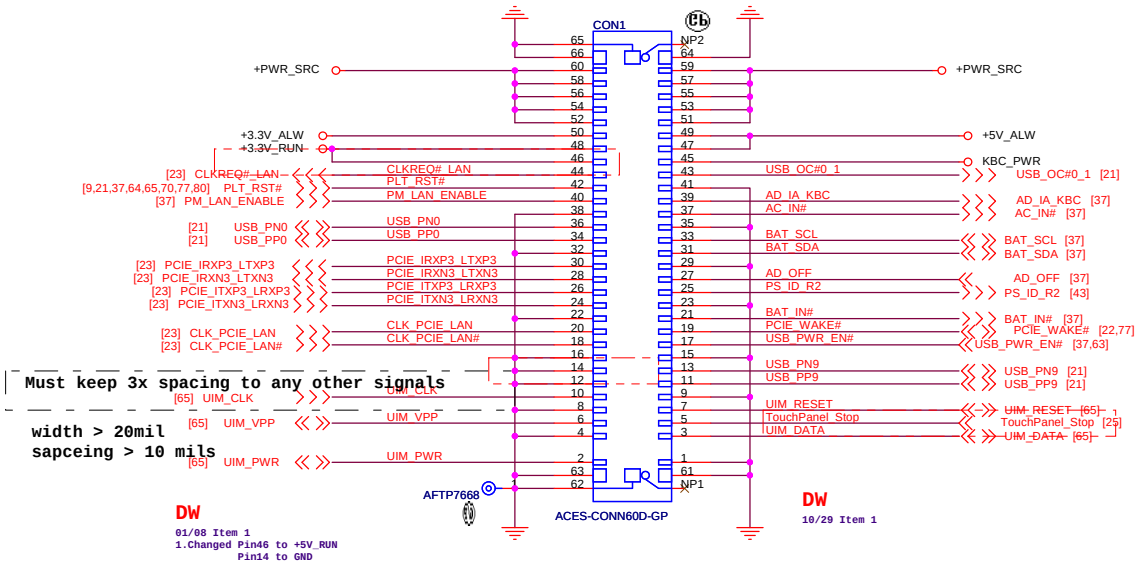
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserve*

Size: A3 | Document Number: *Vostro Calpella* | Rev: *X01*

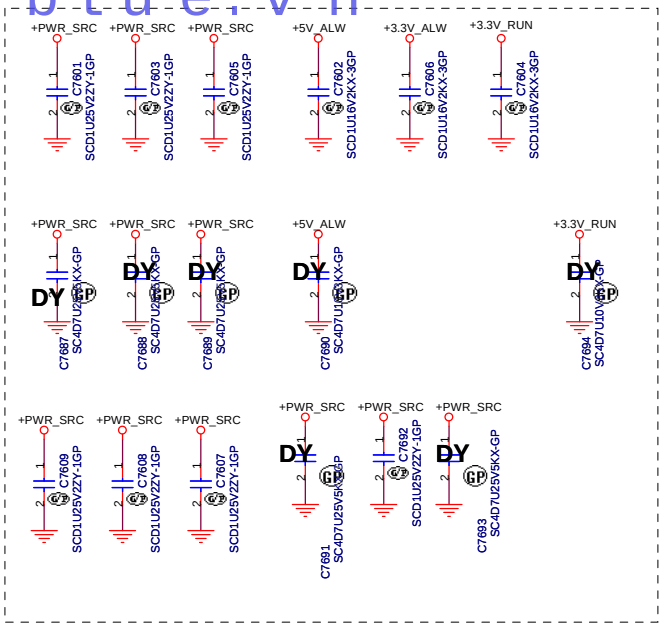
Date: Monday, January 18, 2010 | Sheet 75 of 91

DC_IN board CON



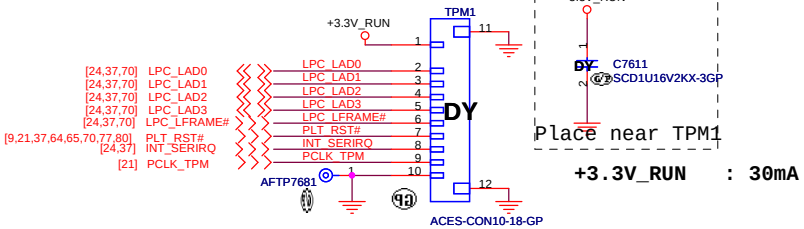
20.F1009.060

Place near CON1



+5V_ALW : 2000mA
+3.3V_ALW : 347mA
+3.3V_RUN/+5V_RUN:80mA (Touch Panel)
KBC_PWR : < 1mA
+PWR_SRC : Estimated by using battery 11.1V,85W

TPM board CON



20.K0315.010

+3.3V_RUN : 30mA

DW
01/08 Item 1
1.Remove DC-IN Board AFTP

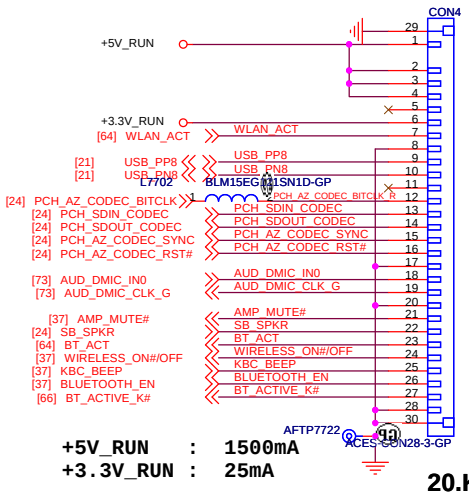
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC_IN/TPM board CON	
Size: Custom	Document Number: Vostro Calpella	Rev: X01
Date: Monday, January 18, 2010	Sheet 76 of 91	

SSID = User.Interface

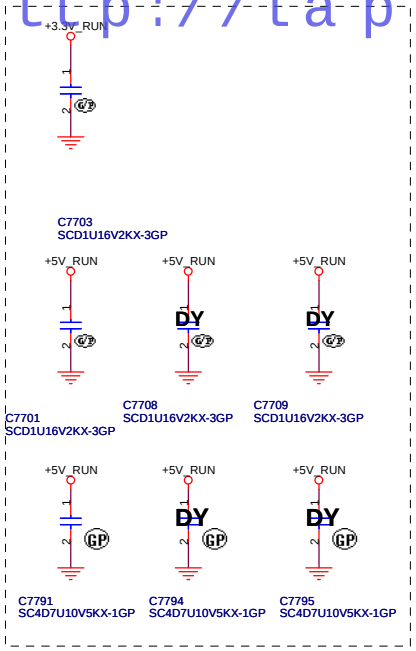
Audio board CON

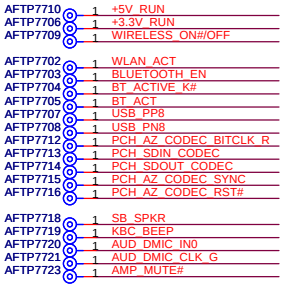


+5V_RUN : 1500mA
+3.3V_RUN : 25mA

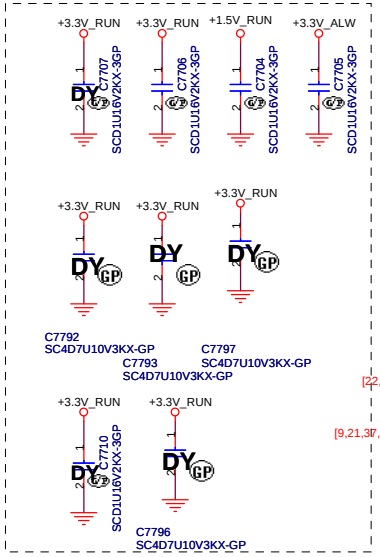
20.K0315.028

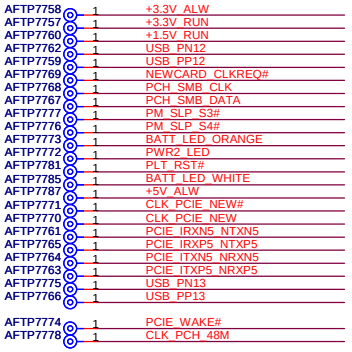
Place near CON4



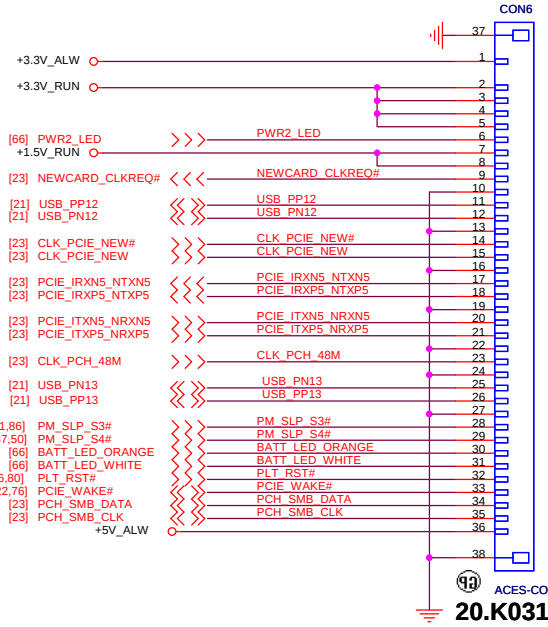


Place near CON6



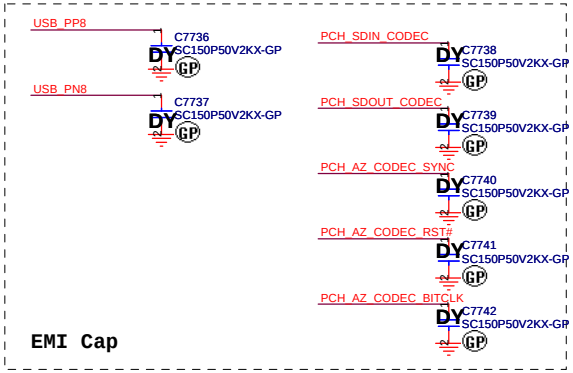


IO board CON



20.K0315.036

+1.5V_RUN : 650mA
+3.3V_RUN : 1775mA
+3.3V_ALW : 275mA
+5V_ALW: 60mA



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

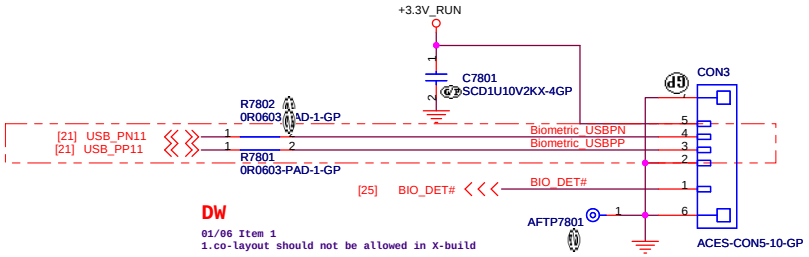
Title: Audio BD/IO BD CONN

Size: Custom | Document Number: Vostro Montevina Discrete | Rev: X01

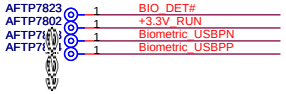
Date: Monday, January 18, 2010 | Sheet 77 of 91

+3.3V_RUN : 3.5mA
+5V_RUN : 240mA
+5V_ALW : 80mA

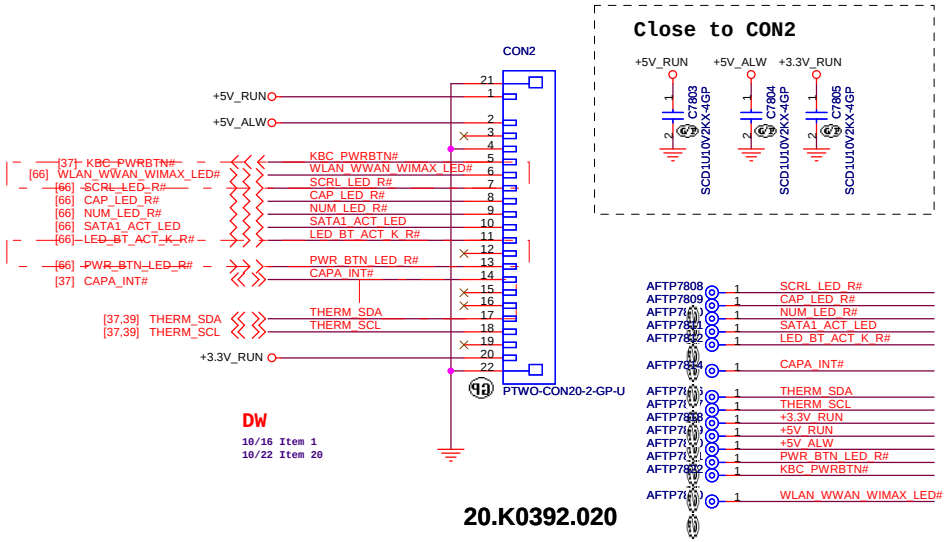
Finger Printer Connector



20.K0315.005



LED&Capacity board CONN



20.K0392.020

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Finger Printer/Capacity

Size	Document Number	Rev
Custom	Vostro Calpella	X01

Date: Monday, January 18, 2010 Sheet 78 of 91

SSID = Mechanical

BOSS:

Thermal

DW 10/15 Item 7

BOSS1 STF237R136H91-GP — 34.4ES32.001 On Bottom

BOSS2 STF256R89H178-GP — 34.4B417.001 On Bottom

BOSS3 STF256R89H178-GP — 34.4B417.001 On Bottom

BOSS4 STF256R50H172-GP — 34.4CQ02.101 On ??

H13 HOLE198R182 — ZZ.ZZZZZ.ZZZ

For DMI

+1.05V_VTT: C7936 SCD1U25V2ZY-1GP, C7937 SCD1U25V2ZY-1GP, C7938 SCD1U25V2ZY-1GP

+5V_USB1: RFC27 SCD1U25V2ZY-1GP; RFC26 SC56P25V2JN-GP

+5V_RUN: RFC29 SC56P25V2JN-GP; RFC28 SC1KP50V2KX-1GP

+5V_ALW: RFC31 SCD1U25V2ZY-1GP; RFC30 SC56P25V2JN-GP

For RF Team

RFC02 SC33P50V2JN-3GP; RFC03 SC1KP50V2KX-1GP; RFC04 SC56P25V2JN-GP

RFC18 SCD1U25V2ZY-1GP; RFC16 SCD1U25V2ZY-1GP

+3.3V_RUN: RFC21 SCD1U25V2ZY-1GP; RFC20 SCD1U25V2ZY-1GP

+3.3V_ALW: RFC23 SCD1U25V2ZY-1GP; RFC24 SCD1U25V2ZY-1GP; RFC25 SCD1U25V2ZY-1GP

RFC22 SC56P25V2JN-GP

RFC33 SC56P25V2JN-GP; RFC34 SCD1U25V2ZY-1GP

RFC07 SCD1U25V2ZY-1GP; RFC08 SCD1U25V2ZY-1GP

RFC19 SCD1U25V2ZY-1GP; RFC17 SC56P25V2JN-GP

RFC35 SCD1U25V2ZY-1GP; RFC32 SCD1U25V2ZY-1GP; RFC37 SCD1U25V2ZY-1GP; RFC36 SCD1U25V2ZY-1GP

RFC09 SCD1U25V2ZY-1GP; RFC10 SCD1U25V2ZY-1GP

RFC13 SCD1U25V2ZY-1GP; RFC14 SCD1U25V2ZY-1GP; RFC15 SCD1U25V2ZY-1GP

RFC38 SCD1U25V2ZY-1GP; RFC39 SCD1U25V2ZY-1GP; RFC40 SCD1U25V2ZY-1GP

RFC11 SCD1U25V2ZY-1GP; RFC12 SC56P25V2JN-GP

RFC43 SCD1U25V2ZY-1GP; RFC41 SCD1U25V2ZY-1GP; RFC42 SCD1U25V2ZY-1GP

EC7950 SCD1U25V2ZY-1GP

DW 12/03 Item 5

HOLE:

H_HD1 SPRING-95-GP; H_HD2 SPRING-95-GP — 34.4ES31.001 34.4ES31.001

HOLE1 HOLE355X355R126-GP; HOLE2 HTE10BE10R32-U-55-GP; HOLE3 HT95X95B95R32-GP — ZZ.00PAD.I71 ZZ.00PAD.K81 ZZ.00PAD.N81

HOLE4 HT95X95B95R32-GP; HOLE5 HT95X95BE95R32-U-475-S-GP; HOLE6 HOLE355X355R126-GP — ZZ.00PAD.N81 ZZ.00PAD.Q41 ZZ.00PAD.I71

HOLE7 HOLE355X355R126-GP; HOLE8 HTE95B85R32-U-475-GP; HOLE9 HOLE256R126-GP — ZZ.00PAD.I71 ZZ.00PAD.N91 ZZ.00PAD.J01

HOLE10 HOLE197R166-GP; HOLE11 HOLE197R166-GP; HOLE12 HOLE197R166-GP — 34.4EM01.001 34.4EM01.001 34.4EM01.001

+PWR_SRC: EC7921 SCD1U25V2ZY-1GP; EC7934 SCD1U25V2ZY-1GP

+1.5V_SUS: EC7935 SCD1U25V2ZY-1GP; EC7936 SCD1U25V2ZY-1GP; EC7937 SCD1U25V2ZY-1GP

+1.5V_SUS: EC7942 SC100P50V3JN-GP; EC7943 SC100P50V3JN-GP; EC7944 SCD1U25V2ZY-1GP; EC7945 SC100P50V3JN-GP

+PWR_SRC: EC7946 SCD1U25V2ZY-1GP; EC7947 SCD1U25V2ZY-1GP

+PWR_SRC: EC7938 SCD1U25V2ZY-1GP; EC7939 SCD1U25V2ZY-1GP; EC7940 SCD1U25V2ZY-1GP; EC7941 SCD1U25V2ZY-1GP

+VCC_CORE: EC7948 SCD1U25V2ZY-1GP; EC7949 SCD1U25V2ZY-1GP

EMI Request

+PWR_SRC: RFC44 SCD1U25V2ZY-1GP

+VCC_CORE: RFC70 SCD1U25V2ZY-1GP

+PWR_SRC: RFC68 SCD1U25V2ZY-1GP

+1.05V_VTT: RFC45 SCD1U25V2ZY-1GP; RFC46 SCD1U25V2ZY-1GP; RFC47 SCD1U25V2ZY-1GP; RFC48 SCD1U25V2ZY-1GP; RFC49 SCD1U25V2ZY-1GP; RFC50 SCD1U25V2ZY-1GP

+1.5V_SUS: RFC52 SCD1U25V2ZY-1GP; RFC51 SCD1U25V2ZY-1GP

+PWR_SRC: RFC57 SCD1U25V2ZY-1GP; RFC53 SCD1U25V2ZY-1GP; RFC54 SCD1U25V2ZY-1GP; RFC55 SCD1U25V2ZY-1GP; RFC56 SCD1U25V2ZY-1GP; RFC58 SCD1U25V2ZY-1GP

+1.8V_RUN: RFC60 SCD1U25V2ZY-1GP; RFC59 SCD1U25V2ZY-1GP

+VCC_GFX_CORE: RFC61 SCD1U25V2ZY-1GP

+5V_ALW: RFC64 SCD1U25V2ZY-1GP; RFC62 SCD1U25V2ZY-1GP; RFC63 SCD1U25V2ZY-1GP

+3.3V_ALW: RFC65 SCD1U25V2ZY-1GP; RFC66 SCD1U25V2ZY-1GP

+5V_RUN: RFC67 SCD1U25V2ZY-1GP

+5V_RUN: RFC69 SC56P25V2JN-GP

+VCC_GFX_CORE: RFC71 SCD1U25V2ZY-1GP; RFC72 SCD1U25V2ZY-1GP; RFC73 SCD1U25V2ZY-1GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Miscellaneous Components

Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 79 of 91

SSID = VIDEO

http://laptopblue.vn

U8001B 2 OF 7

N11M-GE1-S-A2-GP-U

IOVDD + IOVDDQ = 2200mA

PEX_PLLVDD = 120mA

Place under GPU

Place near GPU

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

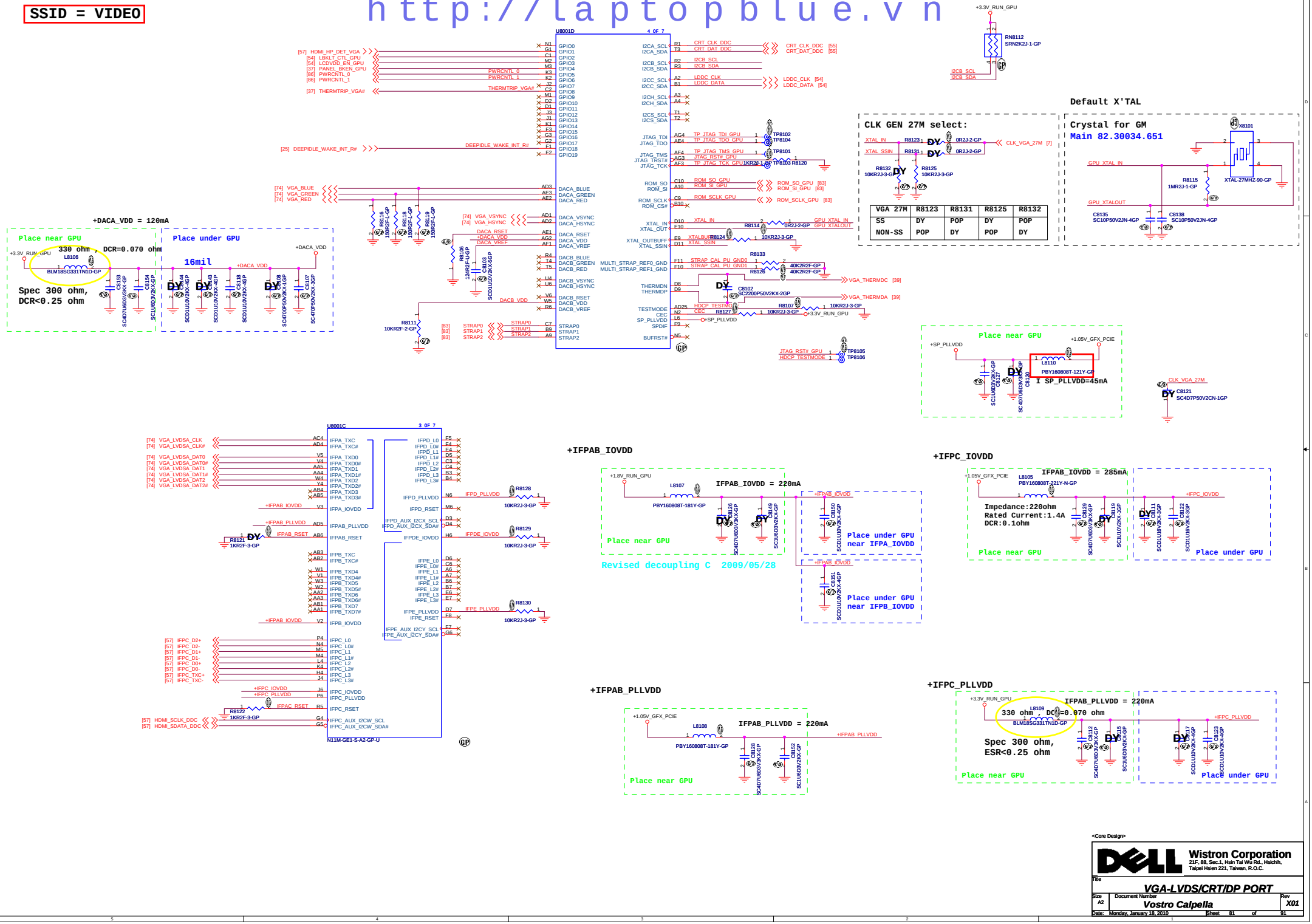
Title: VGA-PCIE/LVDS(1/4)

Size: A3 | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 80 of 91

SSID = VIDEO

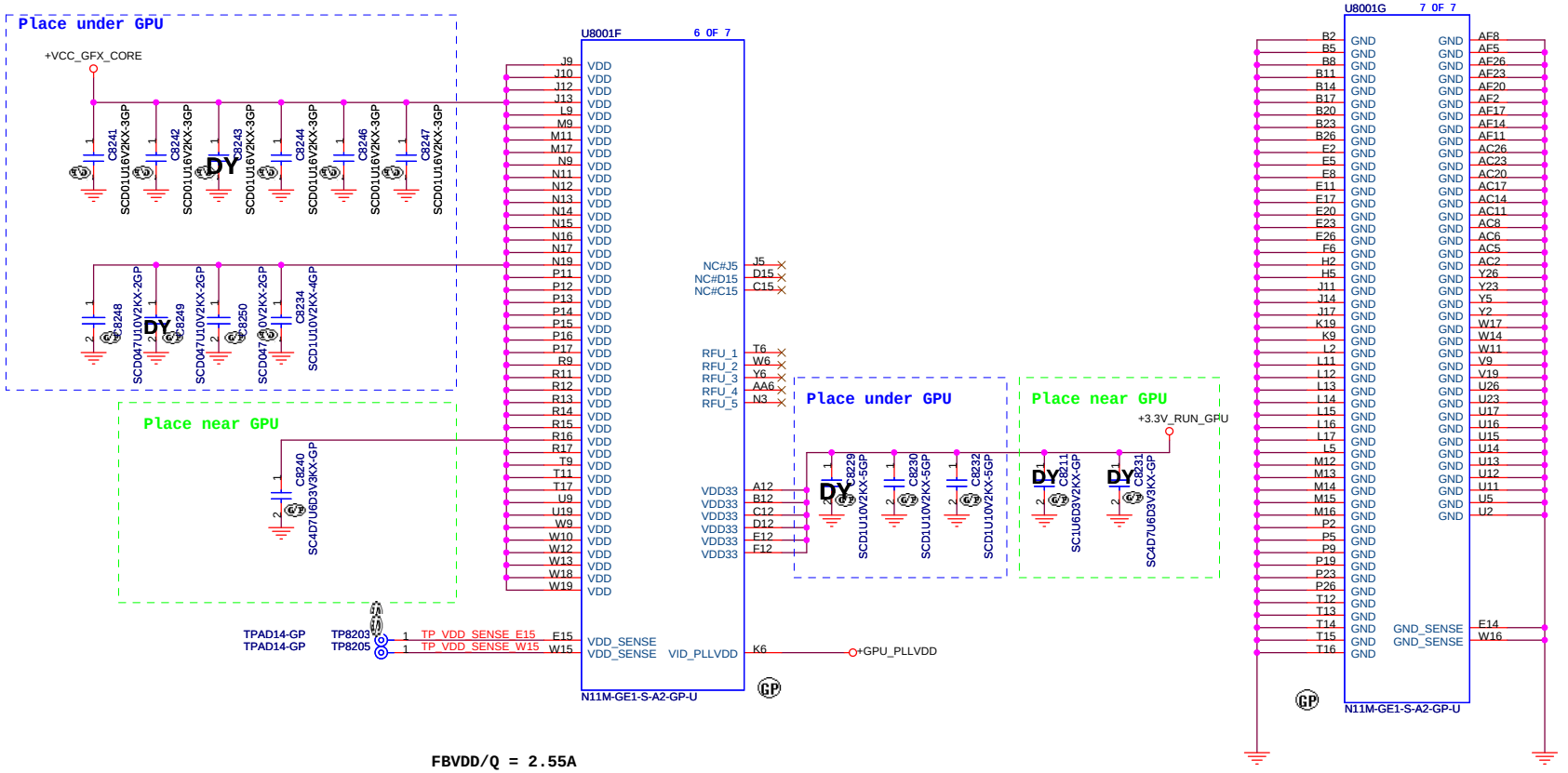
http://laptopblue.vn



<Core Design>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	VGA-LVDS/CRT/DP PORT
Size: A2	Document Number: Vostro Calpella
Rev: X01	
Date: Monday, January 18, 2010	Sheet 81 of 91

SSID = VIDEO



<Core Design>

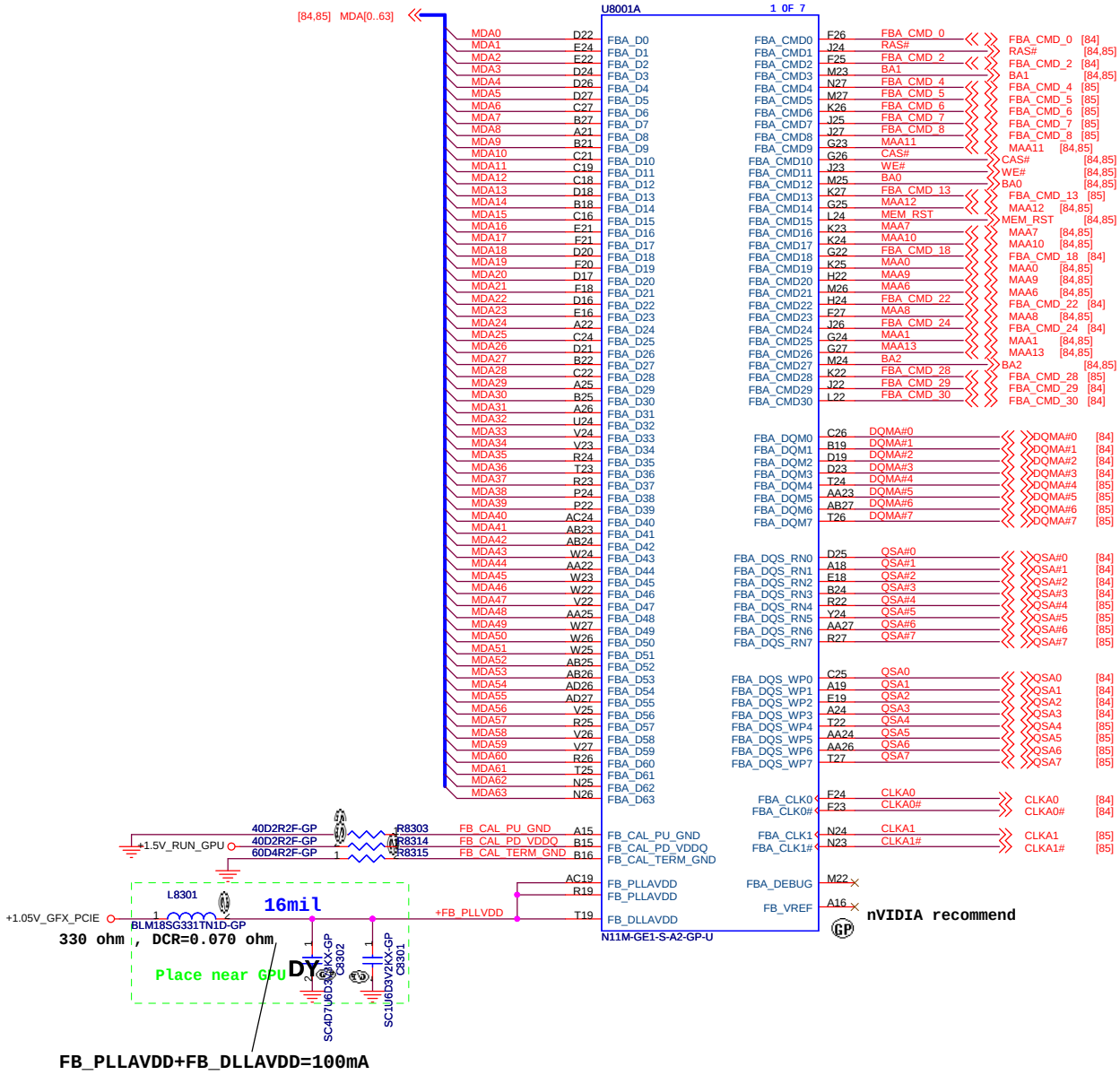
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-POWER/GND(3/4)

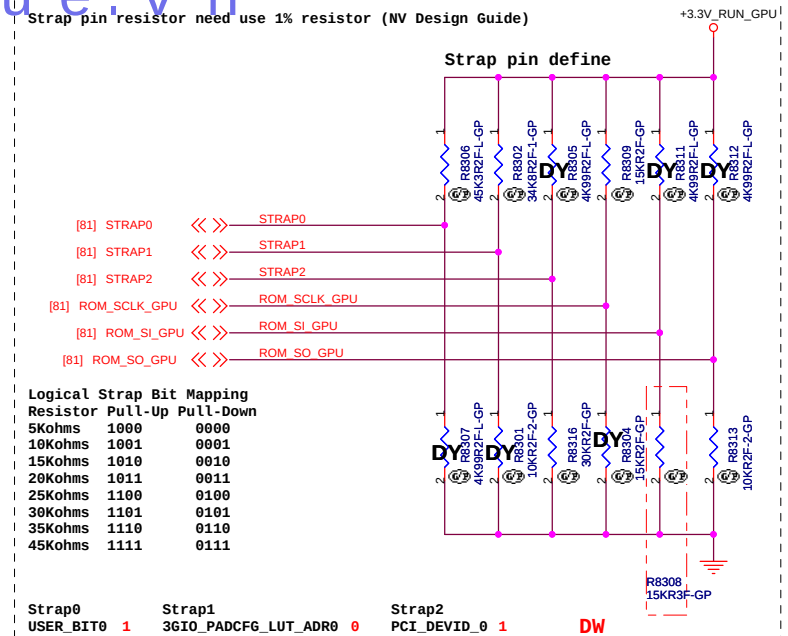
Size: A3 | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 82 of 91

SSID = VIDEO



Strap pin resistor need use 1% resistor (NV Design Guide)



Logical Strap Bit Mapping

Resistor	Pull-Up	Pull-Down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111

Strap0		Strap1		Strap2	
USER_BIT0	1	3GIO_PADCFG_LUT_ADR0	0	PCI_DEVID_0	1
USER_BIT1	1	3GIO_PADCFG_LUT_ADR1	1	PCI_DEVID_1	0
USER_BIT2	1	3GIO_PADCFG_LUT_ADR2	1	PCI_DEVID_2	1
USER_BIT3	1	3GIO_PADCFG_LUT_ADR3	1	PCI_DEVID_3	0
EDID is used		Reserved		N11M-GE1 GPU Device ID=0x0A75	

DW
01/15 Item 1

ROM_SI_GPU		ROM_SO_GPU		ROM_SCLK_GPU	
RAM_CFG0		VGA_DEVICE	1	PEX_PLL_EN_TERM	0
RAM_CFG1		SMB_ALT_ADDR	0	SLOT_CLK_CONFIG	1
RAM_CFG2		FB_0_BAR_SIZE	0	SUB_VENDOR	0
RAM_CFG3		XCLK_417	0	PCI_DEVID_4	1

Default setting: SAMSUNG sDDR3 64Mx16BIT-->20K pull down (0x0011)

RAM_CFG[3:0]	Config	FB_BUS Width	Definitions
0000			
0001			
0010	64MX16	DDR3 64Bit	Hynix
0011	64MX16	DDR3 64Bit	Samsung Default
0100			
0101			
0110			
0111			

If use Hynix sDDR3 64Mx16BIT(0x0010), R8308 change to 15K

SUB_VENDOR	XCLK_417	PEX_PLL_EN_TERM
0 No VBIOS ROM	0 277MHz(POR)	0 Disable (POR)
1 BIOS ROM present	1 Reserved	1 Enable

3GIO_PADCFG	USER[3:0]
0000 Desktop	1111 Use EDID to detect panel settings
1110 Notebook (POR)	

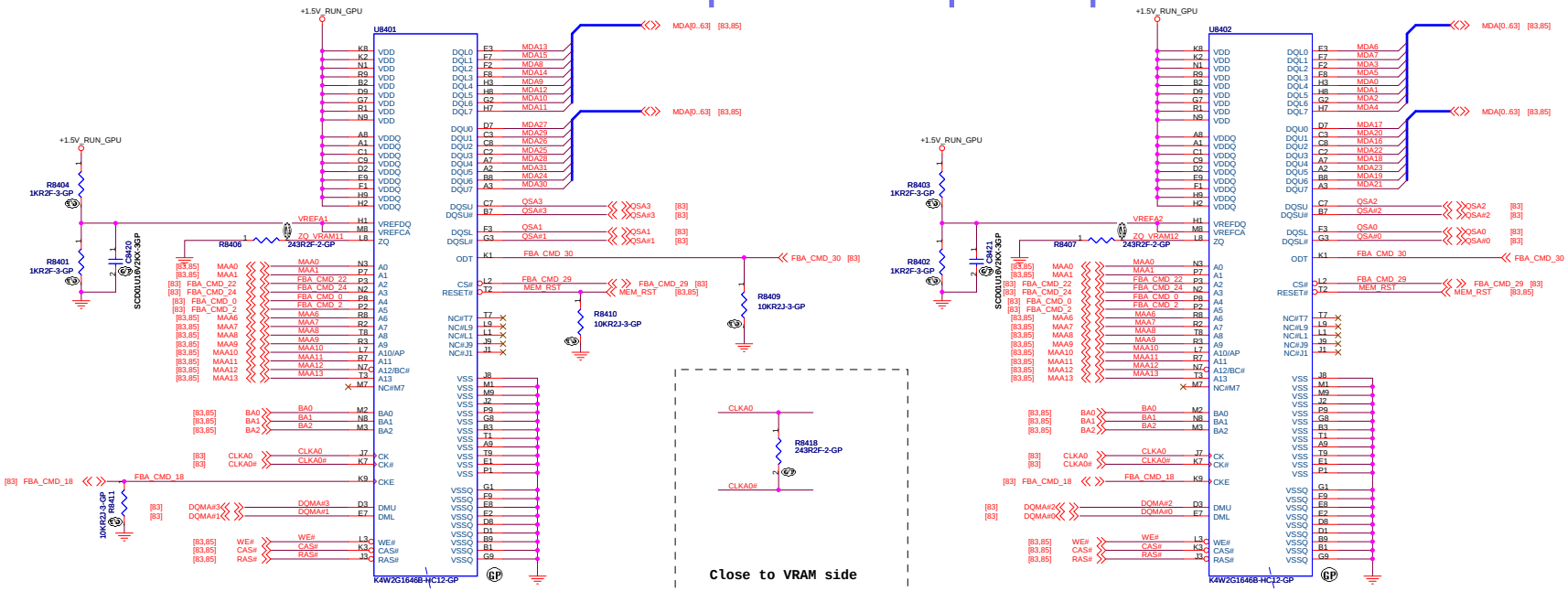
SLOT_CLOCK_CFG
0 GPU and MCH do not share a common reference clock
1 GPU and MCH share a common reference clock (POR)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

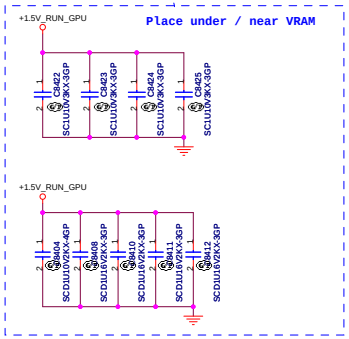
Title: VGA-MEMORY/STRAPS(4/4)
Size: A3 | Document Number: Vostro Calpella | Rev: X01
Date: Monday, January 18, 2010 | Sheet 83 of 91

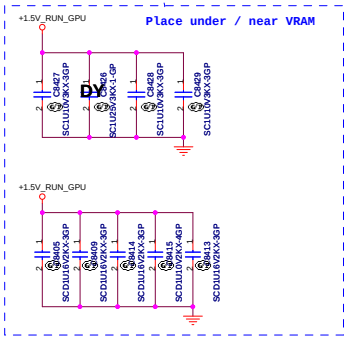
SSID = VIDEO



64X16 SAMSUNG K4W1G1646E-HC12 P/N:72.41164.H0U

64X16 HYNIX H5TQ1G63BFR-12C P/N:72.51G63.C0U





DV

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

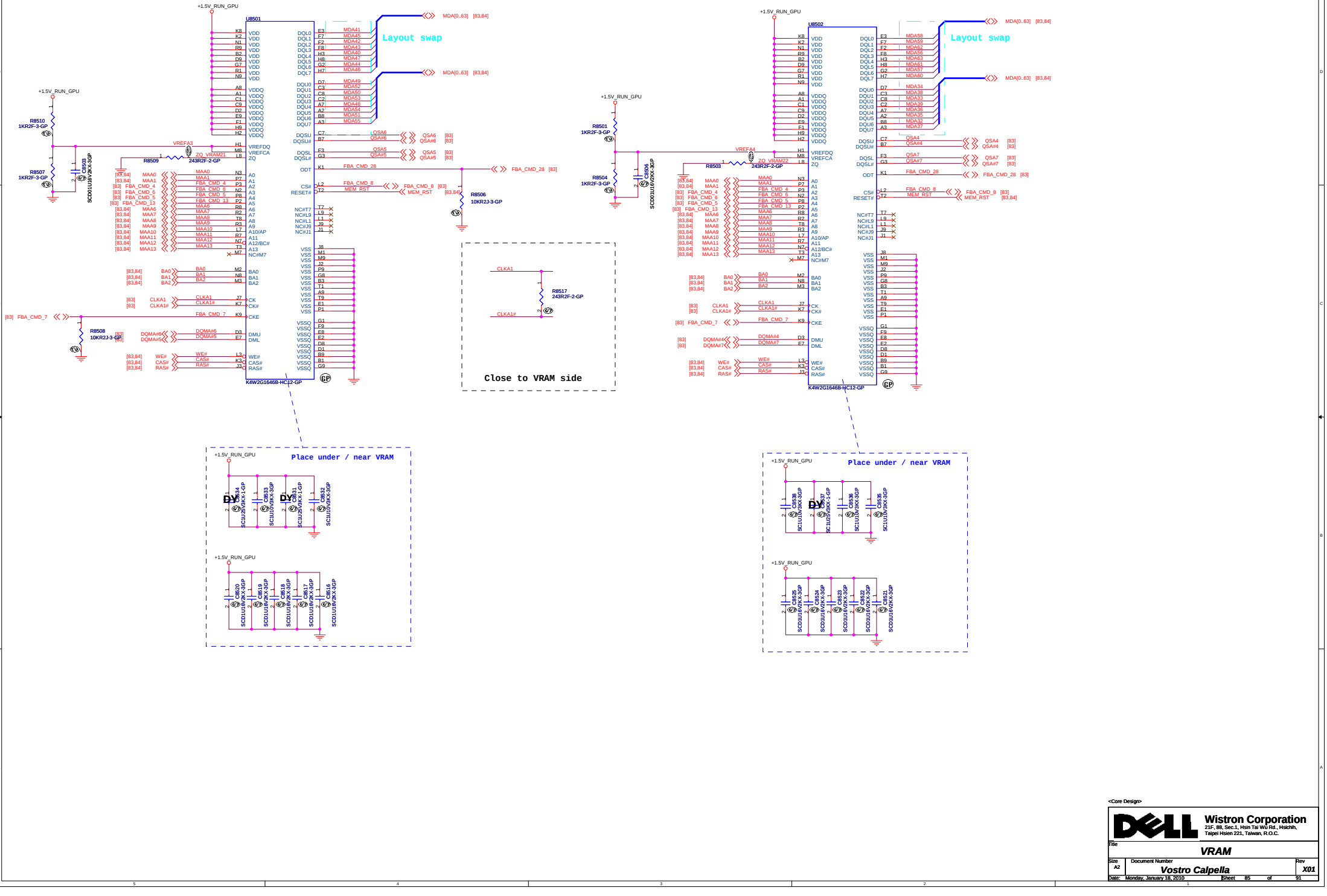
Title: VRAM(1/2)

Size: A2 | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 84 of 91

SSID = VIDEO

http://laptopblue.vn



<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

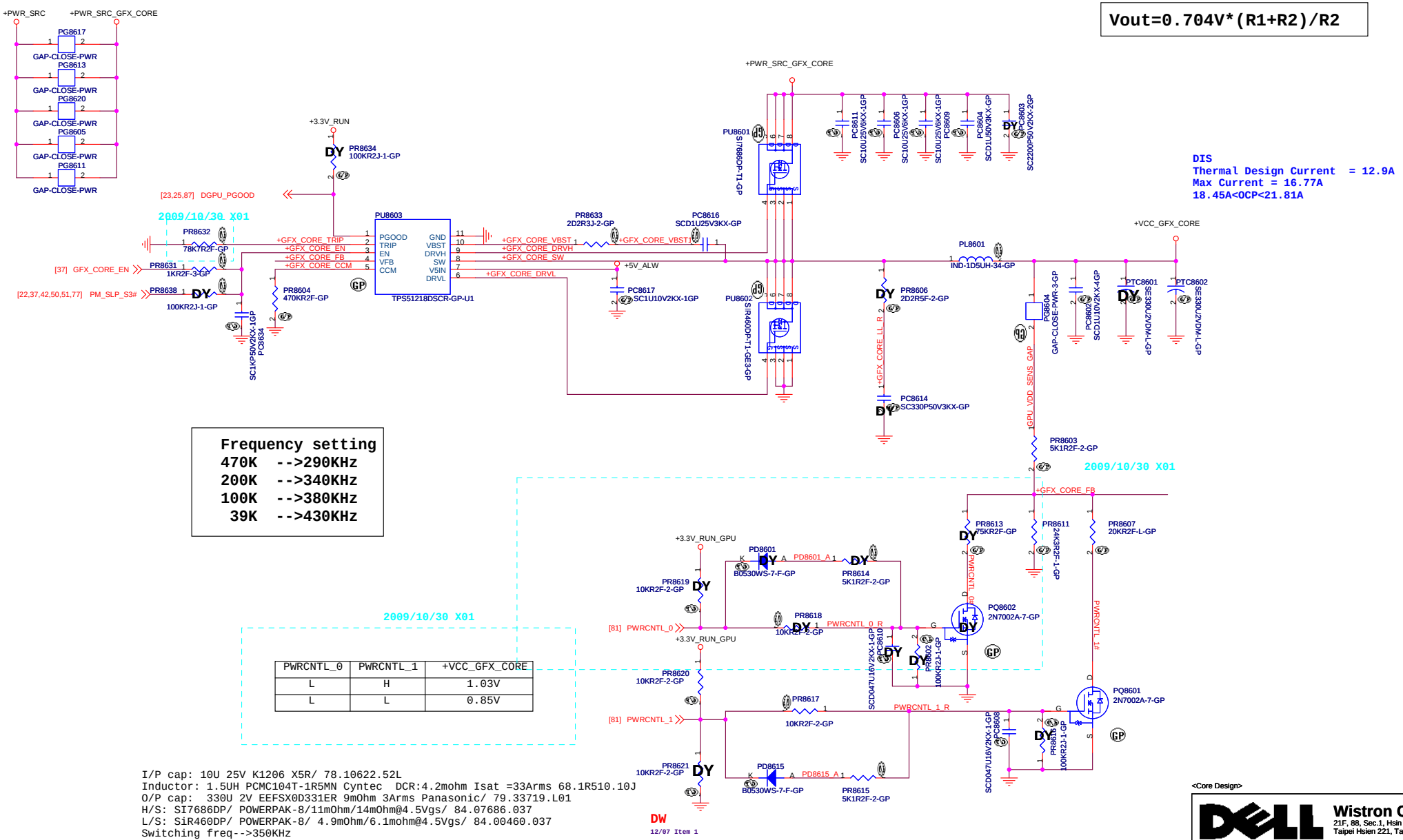
Title: VRAM

Size	Document Number	Rev
A2	Vostro Calpella	X01

Date: Monday, January 18, 2010 Sheet 85 of 91

SSID = PWR.Plane.Regulator_GFX http://laptopblue.vn

Vout=0.704V*(R1+R2)/R2



Frequency setting
470K --->290KHz
200K --->340KHz
100K --->380KHz
39K --->430KHz

2009/10/30 X01

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
L	H	1.03V
L	L	0.85V

DIS
Thermal Design Current = 12.9A
Max Current = 16.77A
18.45A<OCP<21.81A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->350KHz

DW
12/07 Item 1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218 +VCC_GFX_CORE

Size	Document Number	Rev
Custom	Vostro Calpella (Discrete)	X01

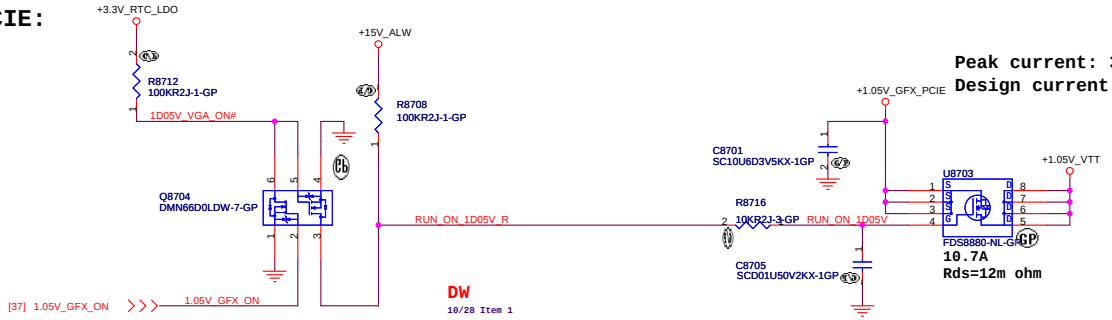
Date: Monday, January 18, 2010 Sheet 86 of 91

+3.3V_RUN_GPU

Peak current: 1140 mA
Design current: 798 mA

AO3434L-GP MAX 4.2A
Rds(on) = 52 mOhm (Max)

+1.05V_GFX_PCIE:

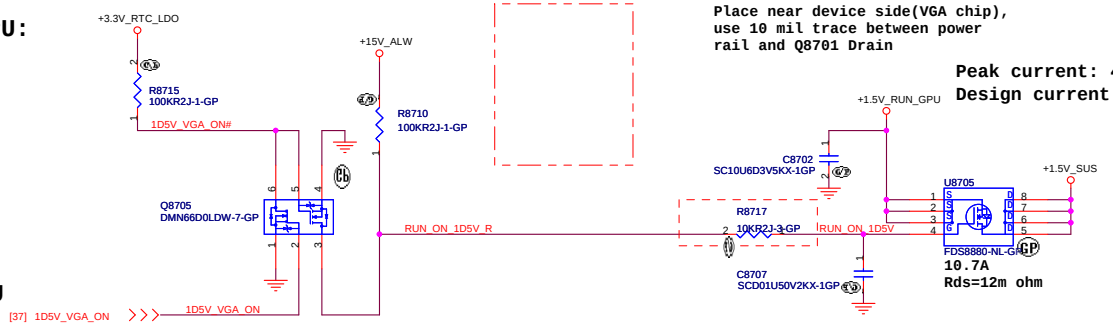


Peak current: 3550 mA
Design current: 2485 mA

10.7A
Rds=12m ohm

DW
10/28 Item 1

+1.5V_RUN_GPU:

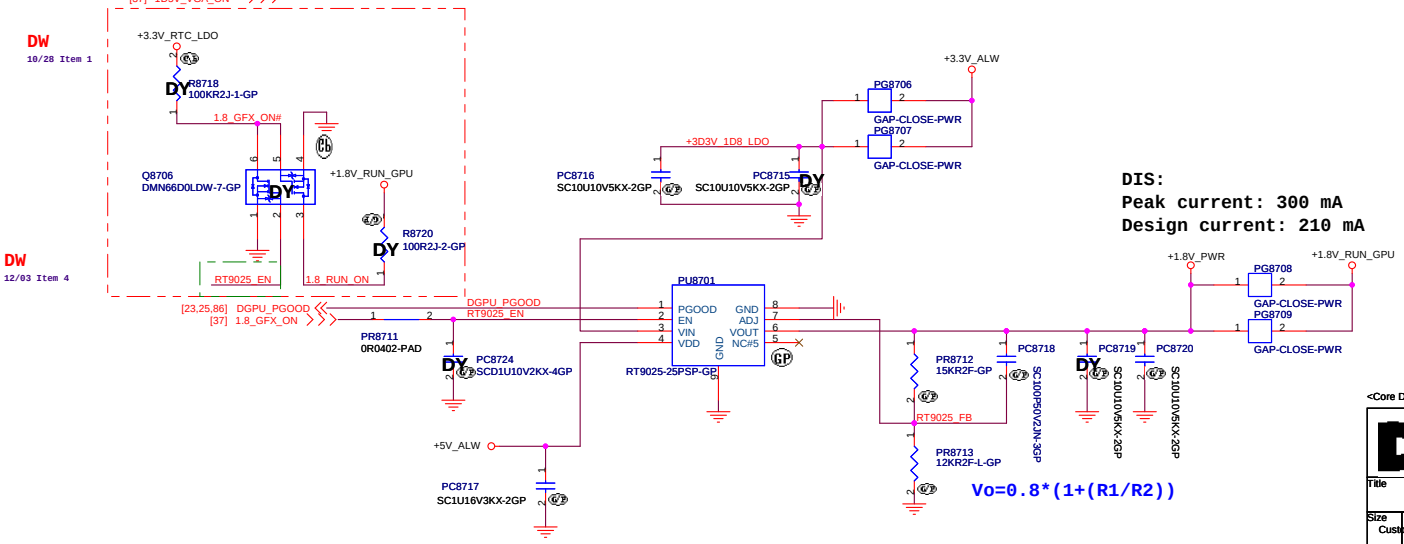


Place near device side(VGA chip), use 10 mil trace between power rail and Q8701 Drain

Peak current: 4230 mA
Design current: 2961 mA

10.7A
Rds=12m ohm

+1.8V_RUN_GPU



DIS:
Peak current: 300 mA
Design current: 210 mA

Vo=0.8*(1+(R1/R2))

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LDO 1.8V

Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 87 of 91

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/10/15	X01	1	25	Swapped Q2515 C,E Pin	For correct.	EE
		2	All	Combine pull-up/down resistors from single to series resistor	For save more part counts	EE
		3	37	Update 10mW circuit.	For DC mode power consumption can be less than 10mW under S5.	EE
		4	22	Add U2213,R2221	Added 3v/5v S5 power good to control resume reset sequence circuit prevent RTC data loss.	EE
		5	51	stuffed PC5105 with 1uF	For power sequencing of +1.8V_RUN , Delay timing	EE
		6	23	Added 25M Crystal	For DCI (DisplayClock_Integration)	EE
		7	79	Added BOSS4	For Steady the thermal module	EE
		9	All	BOSS1 from 34.4W005.001 to 34.4CQ03.101 CON3 from 20.K0315.005 to 20.K0293.006 CON4 from 20.K0315.028 to 20.K0275.028 CON6 from 20.K0315.036 to 20.K0276.036 DM1 from 62.10017.U81 to 62.10017.P31 DM2 from 62.10017.U71 to 62.10017.Q31 HOLE1 from ZZ.00PAD.I71 to ZZ.00PAD.G51 HOLE2 from ZZ.00PAD.K81 to ZZ.00PAD.E11 HOLE3 from ZZ.00PAD.N81 to ZZ.00PAD.D71 HOLE4 from ZZ.00PAD.N81 to ZZ.00PAD.D71 HOLE5 from ZZ.00PAD.K11 to ZZ.00PAD.E11 HOLE6 from ZZ.00PAD.I71 to ZZ.00PAD.G51 HOLE7 from ZZ.00PAD.I71 to ZZ.00PAD.G51 HOLE8 from ZZ.00PAD.N91 to ZZ.00PAD.D31 HOLE9 from ZZ.00PAD.J01 to ZZ.00PAD.D11 LCD1 from 20.F1093.040 to 20.F1555.030 TPAD1 from 20.K0320.004 to 20.K0265.004	For ME request Changed connect PN:	ME
2009/10/16		1	37,87	Removed CAPA_RST# from Capacity board		EE
				Added Switch Baord Detection circuit	For software request.	EE
2009/10/19		1	77	Reversal CON6 Pin 36 <-> 1 ; 35 <-> 2	For new connect pin define.	EE
		2	9,27	Changed RN907,L2701,L2704	For update components	EE
		3	74	Swapped the RN7408,RN7409,RN7410,RN7411	For Layout request.	EE

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change List - EE(1)

Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 88 of 91

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/10/19	X01	1	21,23	Changed EDID_SELECT# pin from PCH_GPIO66 to PCH_GPIO5	For fixed gitch.	EE
2009/10/22		1	All	Swapped resistance	For Layout request.	EE
		2	64,65 66,78	Merge WWAN and WLAN LED	Update SPEC	EE
		3	All	DM1 from 62.10017.U81 to 62.10017.P31 DM2 from 62.10017.U71 to 62.10017.Q31 HOLE5 from ZZ.00PAD.K11 to ZZ.00PAD.K81 TPM1 from 20.K0238.010 to 20.K0315.010 WLAN1 from 20.F1286.052 to 62.10043.841 WWAN1 from 20.F1286.052 to 62.10043.841 Update H13 Footprint	For ME request Changed connect PN	ME
		4	24	X2401 from 82.30001.691 to 82.30001.A81	Update component	EE
		5	9,42 50	Stuff "S3 Power Reduction" circuit reserve component	Update schematic base on test result.	EE
2009/10/27		1	79	Add RFC7907 +5V_ALW to GND 33pF Cap		RF
				Add RFC7908 +5V_ALW to GND 0.1uF Cap		
				Add RFC7909 +3.3V_RUN to GND 0.1uF Cap		
		2	All	Changed power rail netname from +1.5V_CPU to +1.5V_RUN	Merge +1.5V_CPU to +1.5V_RUN ,For CosDown.	EE
			42	Del U4204,R4213,C4206,R4215,R4217,R4218		
2009/10/28		1	87	Del Q8701,R8709	Remove +1.5V_RUN_GPU discharge circuit,base on test result.	EE
				Add Q8706,R8718,R8720	Reserve +1.8V_RUN_GPU discharge circuit,base on test result.	
		2	26	Del U2601,C2629,C2628	Remove reserve circuit +3.3V_CRT_LDO Circuit for LDO Regulators,base on test result.	
		3	26	Del R2602	Remove reserve resistor,For save more part counts	
		4	25	Del R2517	Remove reserve pull-Hi resistors,For not use it	
		5	27	Del R2708	Remove reserve resistor,For save more part counts	
		6	80	Del R8039	Remove reserve resistor,For save more part counts	
		7	57	Add R5773 between +5V_HDMI_C and +5V_HDMI.	dummy D5703 Stuff R5773 ,For save more part counts base on test result.	
		8	37	Add SW1	Add mine switch to control PWR_BTN , Only on Sample stage	
2009/10/29		1	25,76	Assign PCH GPIO35 for TouchPanel_Stop..	Add TouchPanel Stop Pin to control ON/OFF by PCH GPIO35	EE
2009/12/03	SC	1	24,63 79	Rename RFC***, USBESATA1 Part Referse	Rename Part Referse Ex: USBESATA1 to ESATA1 for manufactory request	EE
		2	37	Add R3720 damping resistor.	Add damping resistor for signal improvement	EE
		3	37	Add R3703,U3703,C3705	Co-layout MUX and OR gate for BLON to solve white screen issue while iGPU to dGPU.	EE
		4	87	Changed Net Connect	Changed Q8706.2 from 1.8_GFX_ON to RT9025_EN ,For correct.	EE
		5	79	For ME request Changed below connect PN:	Change P/N of “HOLE5” from ZZ.00PAD.K81 to ZZ.00PAD.Q41.	ME
2009/12/08	SC	1	38	Add PR8621 Pull-Lo resistor.	Reserve for control. +VCC_GFX_CORE power rail default to 0.85.	EE
		2	42	Add Q4205,Q4206,R4220,R4221	Added discharge circuit for +5_RUN,+3_RUN.	EE
2010/01/11	X-Bulid	1	76	Del AFTP7634 ~ 7662; 7664~7667 ;7669;7672;7302	Del AFTP For saved more layout space.	EE
		2	51	PR5102 short ; replacing PC5105 by 10K resistor to GND	prevent PM_SLP_S3# signal rebound	EE
		3	All	Mount EMI CHOKE or Reserve colse Gap for Differential-Pair	Co-layout should not be allowed in X-build.	EE
		4	23	Del RN2327 , Reserve colse Gap	For saved more layout space.	EE
		5	37,62	Reserve threadhold 2.93V reset IC (74.00690.I7B) in PURE_HW_SHUTDOWN# pin Reserve Pull-Lo resistor for SPI_WP#.	Reserve For Flash ROM Damaged Issue.	EE
2010/01/18	X-Bulid	1	21,73	Swap Camera USB Port from Port-10 to Port-7	For Camera USB issue	EE

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change List - EE(2)

Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 89 of 91

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/10/19	X01	2	81	Remove R8149	For EMI team request	EMI
			21	PCLK_FWH、CLK_PCI_FB、PCLK_KBC、PCLK_TPM reserve by pass cap		
			23	CLK_PCH_48M reserve by pass cap		
			23	Romove R2350 and C2324		
			37	Romove R3726 and C3704		
			79	Reserve +PWR_SRC to GND cap		
2009/10/22		3	79	Add EC7934 0.1u in +VCC_CORE	For EMI team request	EMI
				Add EC7911 0.1u +1.5V_SUS to GND cap*1		
				Add EC7935,EC7936 0.1u +1.5V_SUS to GND cap*2		
				Add EC7937 0.1u +1.5V_SUS to GND cap*1		
				Add EC7938 0.1u +PWR_SRC to GND cap*1		
				Update TR6304,TR6305 p/n to 68.00201.141		
2009/10/23		4	73	Move EC7302	For EMI team request	EMI
			79	dummy 0.1u x 2 in green area 6135,195 ----EC7939,EC7940		
				dummy 0.1u cap in red area 1755,4435 -----EC7941		
				dummy 1000p in green area 5225,6950----EC7942		
				dummy 1000p in green area 3780,6180-----EC7943		
				dummy 104p and 1000p in green area 5385,7010--- EC7944,EC7945		
				dummy 0.1u in green area 3400,6300---EC7946		
				dummy 0.1u in green area 1240,4035--EC7947		
			55	add damping 33ohm on R,G,B Singel---R5594,R5595,R5596		
2009/12/08	SC	1	79	mount EC7948,EC7949,EC7934	For RF Team request	RF
2009/12/09	SC	1	73	mount LECM2012H-900QT-GP in L7301	For EMI team request	EMI
		2	24,77	change R2405 from 10 ohm to 56 ohm and mount 120 ohm bead bead p/n:BLM15EG121SN1 L7702		
		3	73	mount 220p cap on EC7302 and EC7303		
		4	79	Add EC7950		

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change List - EMI&RF

Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 90 of 91

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/10/22	X011	1	46	PR4604,PR4605 --> 4.7ohm for RT, 0 ohm for TI	Change PU4603 from TPS51125 to RT8205B	Power Team
				PR4622 --> 820k ohm for RT, DY for TI		
				PR4616 --> ASM for RT, DY for TI		
				PR4617 --> DY for RT, ASM for TI		
			53	PC5307 change to 68nF for Intel spec		
2009/10/29		2	50	Add 4.7uF at +PWR_SRC_1D5V	Improve Jitter issue	Power Team

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change List - Power

Size: Custom | Document Number: Vostro Calpella | Rev: X01

Date: Monday, January 18, 2010 | Sheet 91 of 91