

# Winery CALPELLA N11M-GE Schematics

Mobile Arrandale

Intel Ibex Peak-M

2010-01-18

REV : X-build

*DY : Nopop Component*

*UMA : Pop when schematic is UMA*

*DIS : Pop when schematic is DIS*

# Winery CALPELLA Block Diagram

PCB LAYER

- ```
L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom
```

**Clock Generator**  
**SLG8SP585**

**Nvidia**  
**TM-GE(40nm)**

100MHz/  
2.5Gbps  
PCIe x 16  
Bandwidth  
: 8GB

*Intel CPU*

*Arrandale*

8, 9, 10, 11, 12, 13, 14

FDI (UMA)  
2.7 GT/s

**Intel**  
**PCH**

14 USB 2.0/1.1 ports  
ETHERNET (10/100/1000Mb)  
High Definition Audio  
SATA ports (6)  
PCIe ports (8)  
LPC I/F  
ACPI 1.1  
PCI/PCI BRIDGE

20,21,22,23,24,25,26,27,28

**USB,ESATA  
Multi-Port**

Flash ROM  
**4MB** 62

Flash ROM  
256kB 62

**Touch  
PAD**

*Int.*  
*KB* 68

**Thermal  
& Fan**  
**EMC2102** 39,58

Capacity Board  
(on daughter board)

Project code : 91.4ES01.001  
Part Number : 48.4ES11.0SB  
PCB P/N : 09297  
Revision : SA

CPU DC/DC  
ISL62883 <sup>47,48</sup>

| INPUTS   | OUTPUTS   |
|----------|-----------|
| +PWR_SRC | +VCC_CORE |

SYSTEM DC/DC  
TPS51125 46

| INPUTS   | OUTPUTS                                           |
|----------|---------------------------------------------------|
| +PWR_SRC | +15V_ALW<br>+3.3V_RTC_LDO<br>+5V_ALW<br>+3.3V_ALW |

SYSTEM DC/DC  
TPS51116 50

| INPUTS   | OUTPUTS                                      |
|----------|----------------------------------------------|
| +PWR_SRC | +1.5V_SUS<br>+0.75V_DDR_VTT<br>+V_DDR_MCH_RE |

SYSTEM DC/DC  
ADP3211 53

| INPUTS   | OUTPUTS      |
|----------|--------------|
| +PWR_SRC | +CPU_GFXCORE |

SYSTEM DC/DC  
TPS51218 86

| INPUTS   | OUTPUTS       |
|----------|---------------|
| +PWR_SRC | +VCC_GFX_CORE |

CHARGER  
BQ24745

| INPUTS           | OUTPUTS  |
|------------------|----------|
| +DC IN<br>+PRATE | +PWR_SRC |

SYSTEM DC/DC  
TPS51218 49

| INPUTS   | OUTPUTS  |
|----------|----------|
| +PWR_SRC | VTT_CORE |

LDO  
APL5930

| INPUTS    | OUTPUTS   |
|-----------|-----------|
| +3.3V_ALW | +1.8V_RUN |

LDO  
RT9025

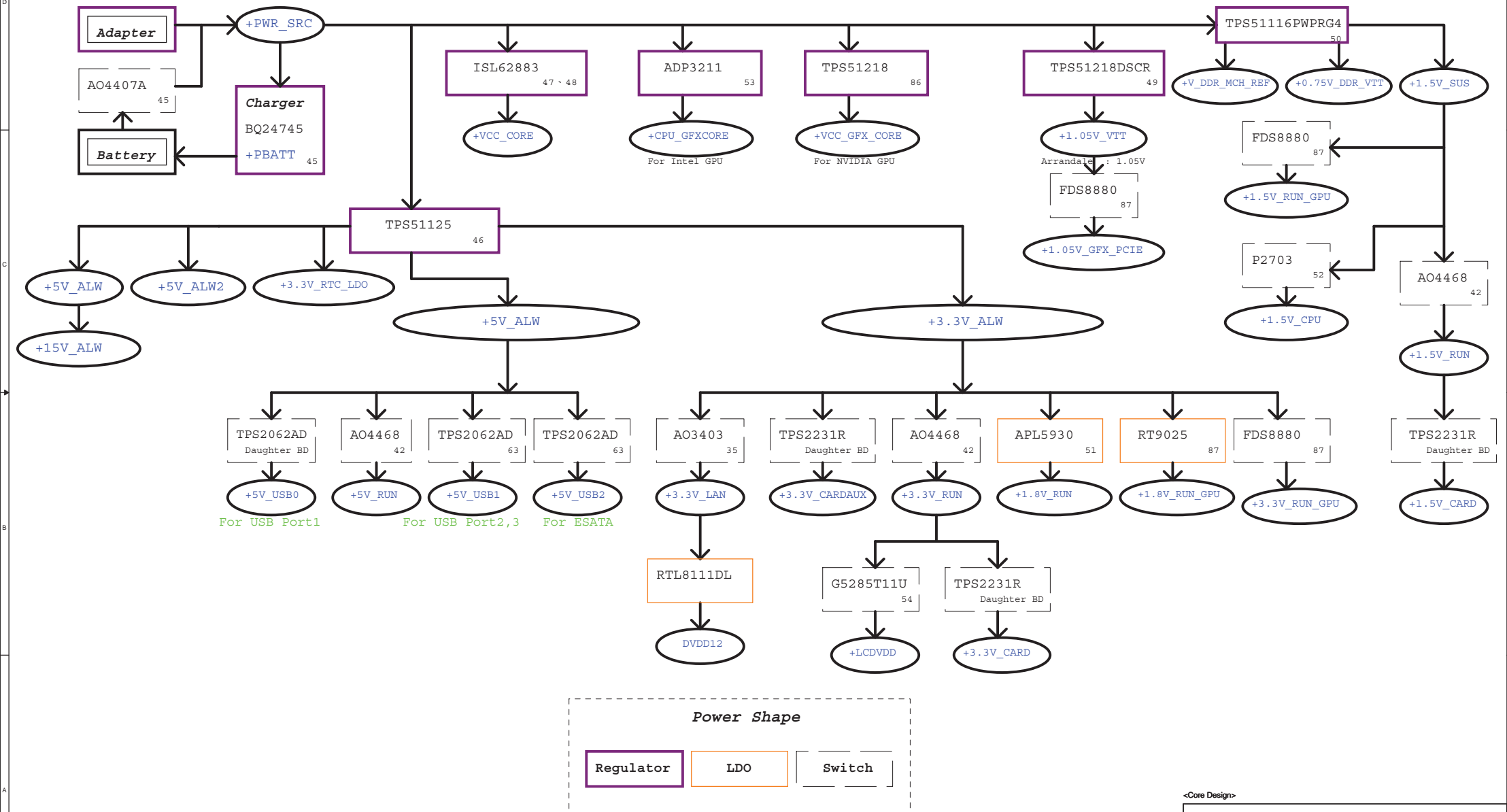
| INPUTS    | OUTPUTS       |
|-----------|---------------|
| +3.3V_ALW | +1.8V_RUN_GPU |

<Core Design>

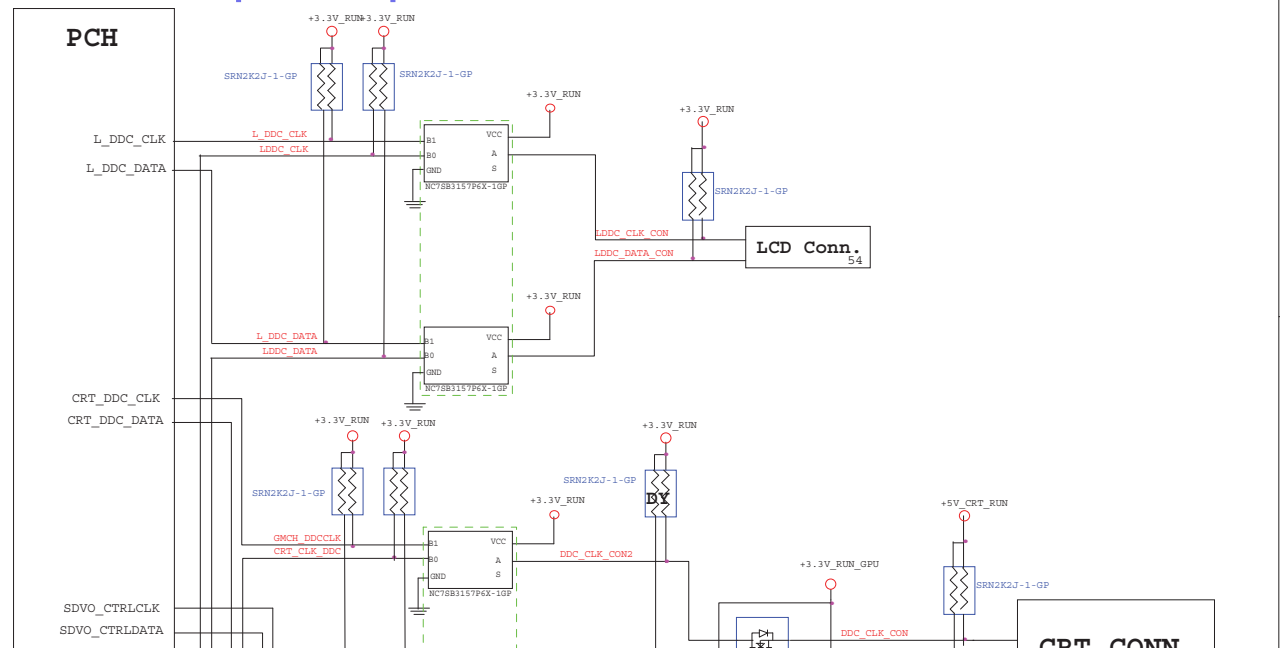
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|                      |                          |            |    |
|----------------------|--------------------------|------------|----|
| Title                |                          |            |    |
| <b>Block Diagram</b> |                          |            |    |
| Size                 | Document Number          | Rev        |    |
| Custom               | <b>Vostro Calpella</b>   | X01        |    |
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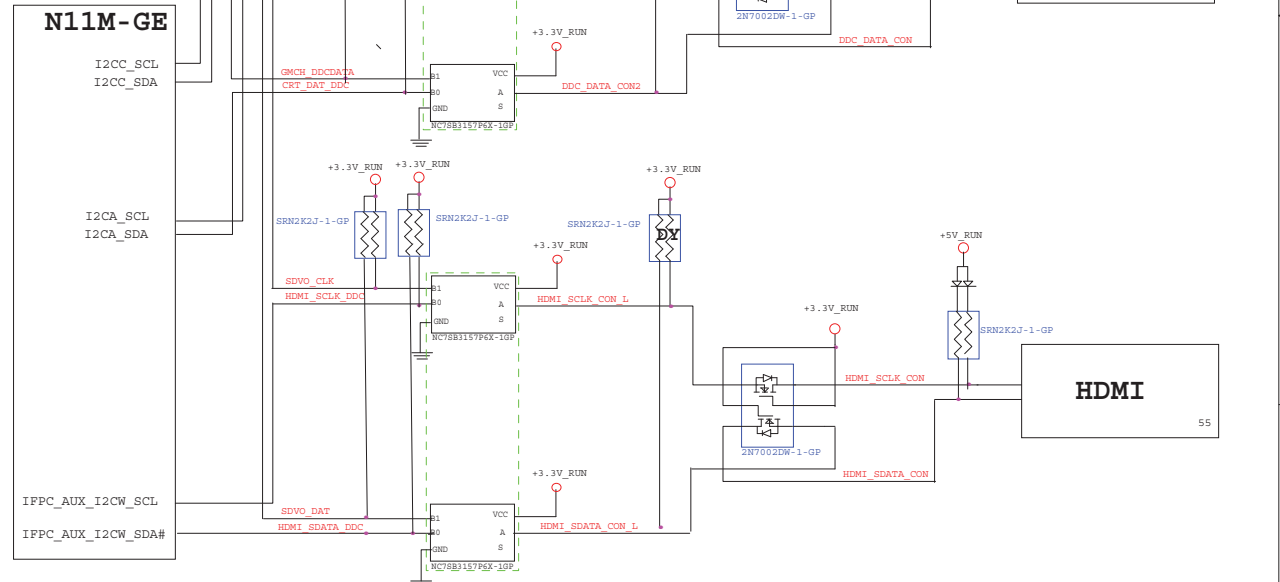
<http://laptop-motherboard-schematic.blogspot.com/>



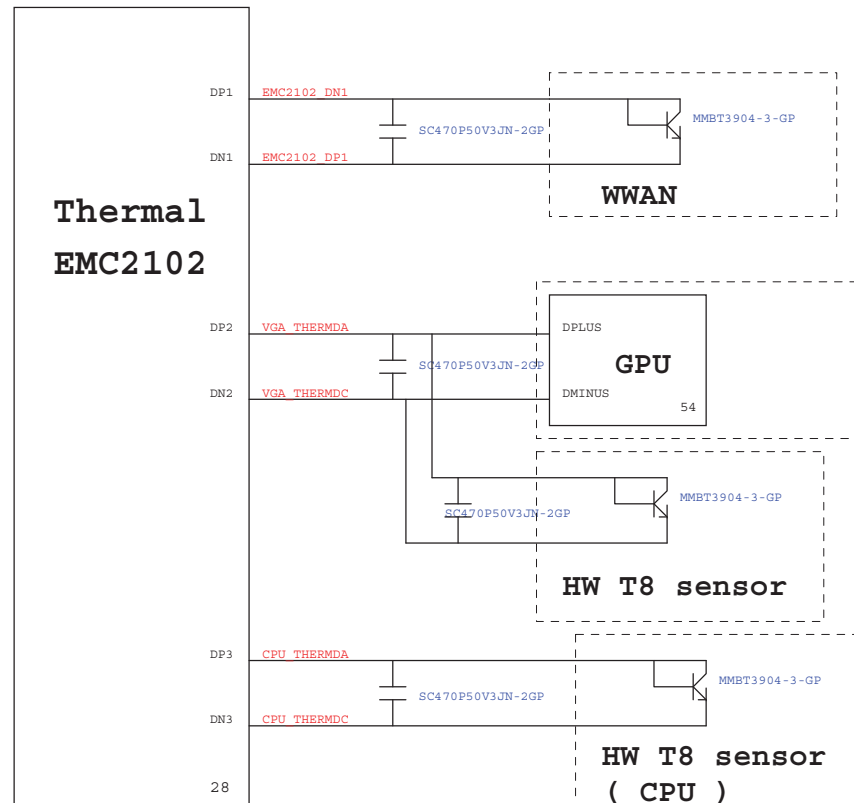
## Switchable Graphic SMBus Block Diagram



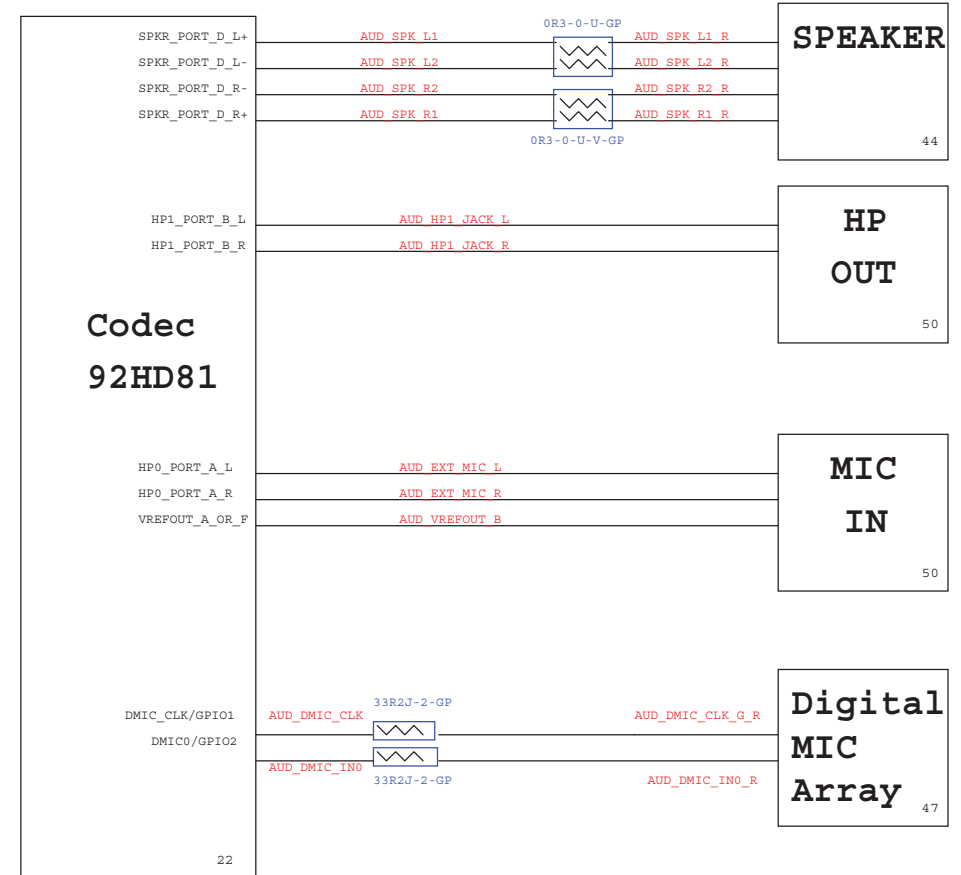
## N11M-GE



## Thermal Block Diagram



## Audio Block Diagram



## PCH Strapping

Calpella Schematic Checklist Rev.0\_7

| Name                  | Schematics Notes                                                                                                                                                                                                                                                                  |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SPKR                  | <b>Reboot option at power-up</b><br><b>Default Mode:</b> Internal weak Pull-down.<br><b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.                                                                                        |
| INIT3_3V#             | Weak internal pull-down. Do not pull high.                                                                                                                                                                                                                                        |
| GNT3#/GPIO55          | <b>Default Mode:</b> Internal pull-up.<br><b>Low (0) = Top Block Swap Mode:</b> Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ do not stuff resistor.                                                                                                     |
| INTVRMEN              | <b>High (1) = Integrated VRM is enabled</b><br><b>Low (0) = Integrated VRM is disabled</b>                                                                                                                                                                                        |
| GNT0#, GNT1#/GPIO51   | <b>Default (SPI):</b> Left both GNT0# and GNT1# floating. No pull up required.<br><b>Boot from PCI:</b> Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating.<br><b>Boot from LPC:</b> Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor. |
| GNT2#/GPIO53          | <b>Default - Internal pull-up.</b><br><b>Low (0) =</b> Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).                                                                                                                                   |
| GPIO33                | <b>Default:</b> Do not pull low.<br><b>Disable ME in Manufacturing Mode:</b> Connect to ground with 1-kΩ pull-down resistor.                                                                                                                                                      |
| SPI_MOSI              | <b>Enable iTPM:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.<br><b>Disable iTPM:</b> Left floating, no pull-down required.                                                                                                                                            |
| NV_ALE                | <b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.<br><b>Disable Danbury:</b> Connect to ground with 4.7-kΩ weak pull-down resistor.                                                                                                                     |
| NC_CLE                | Weak internal pull-up. Do not pull low.                                                                                                                                                                                                                                           |
| HAD_DOCK_EN#/GPIO[33] | <b>Low (0):</b> Flash Descriptor Security will be overridden.<br><b>High (1) :</b> Flash Descriptor Security will be in effect.                                                                                                                                                   |
| HDA_SDO               | Weak internal pull-down. Do not pull high.                                                                                                                                                                                                                                        |
| HDA_SYNC              | Weak internal pull-down. Do not pull high.                                                                                                                                                                                                                                        |
| GPIO15                | Weak internal pull-down. Do not pull high.                                                                                                                                                                                                                                        |
| GPIO8                 | Weak internal pull-up. Do not pull low.                                                                                                                                                                                                                                           |
| GPIO27                | <b>Default = Do not connect (floating)</b><br><b>High(1) =</b> Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.<br><b>Low (0) =</b> Disables the VccVRM. Need to use on-board filter circuits for analog rails.       |

## PCIE Routing

|       |               |
|-------|---------------|
| LANE1 | Card reader   |
| LANE2 | MiniCard WLAN |
| LANE3 | LAN           |
| LANE4 | MiniCard WWAN |
| LANE5 | New Card      |

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## Processor Strapping

Calpella Schematic Checklist Rev.0\_7

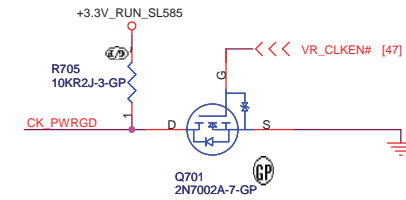
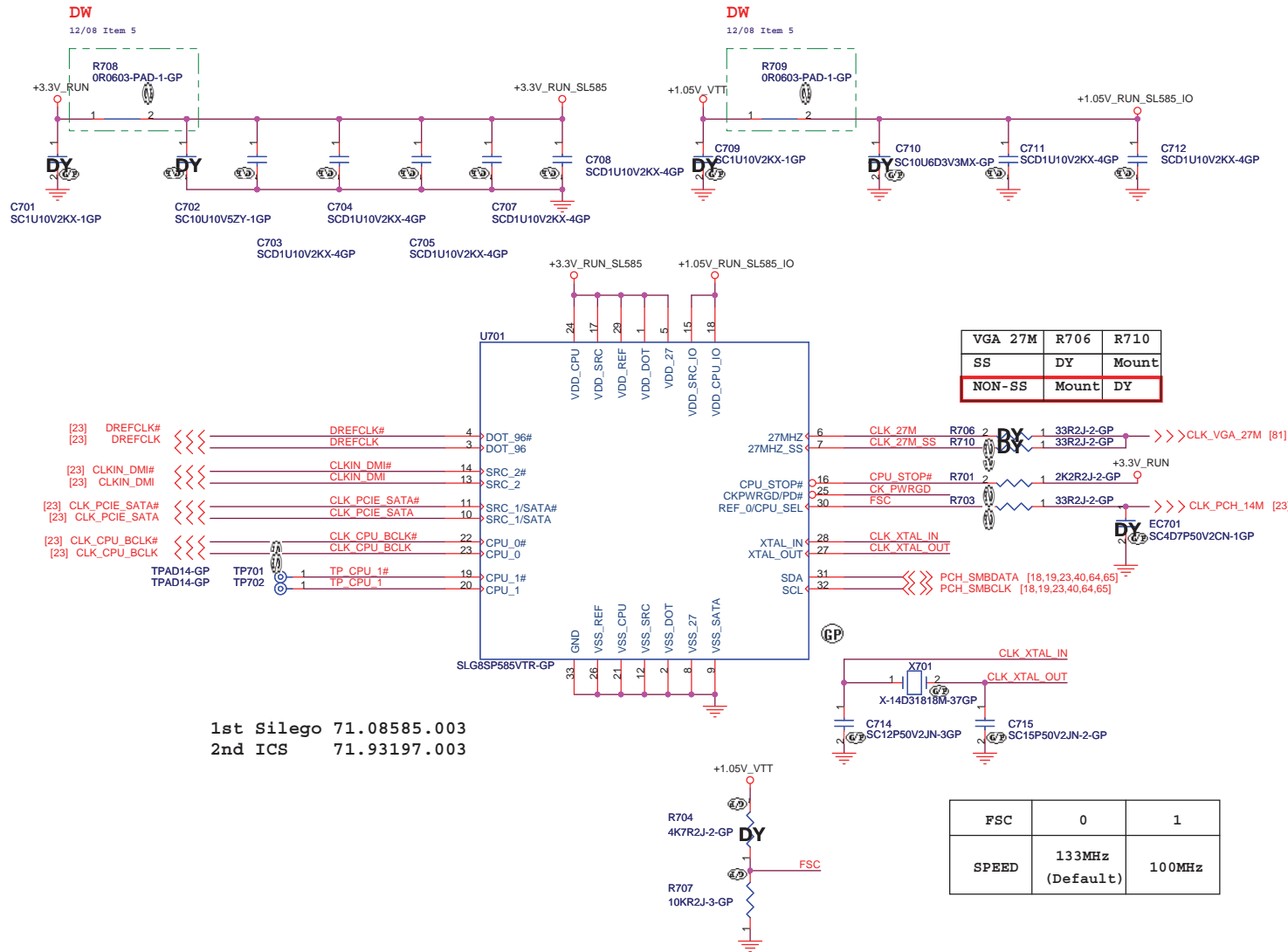
| Pin Name | Strap Description                                                 | Configuration (Default value for each bit is 1 unless specified otherwise)                                                                                                                                                                                                                                                                                      | Default Value |
|----------|-------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| CFG[4]   | <b>Embedded DisplayPort Presence</b>                              | <b>1:</b> Disabled - No Physical Display Port attached to Embedded DisplayPort.<br><b>0:</b> Enabled - An external Display Port device is connected to the Embedded Display Port.                                                                                                                                                                               | 1             |
| CFG[3]   | <b>PCI-Express Static Lane Reversal</b>                           | <b>1:</b> Normal Operation.<br><b>0:</b> Lane Numbers Reversed 15 -> 0, 14 -> 1, ...                                                                                                                                                                                                                                                                            | 1             |
| CFG[0]   | <b>PCI-Express Configuration Select</b>                           | <b>1:</b> Single PCI-Express Graphics<br><b>0:</b> Bifurcation enabled                                                                                                                                                                                                                                                                                          | 1             |
| CFG[7]   | <b>Reserved - Temporarily used for early Clarksfield samples.</b> | <b>Clarksfield (only for early samples pre-ES1) -</b> Connect to GND with 3.01K Ohm/5% resistor<br><b>Note:</b> Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report].<br>For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality. | 0             |

<Core Design>

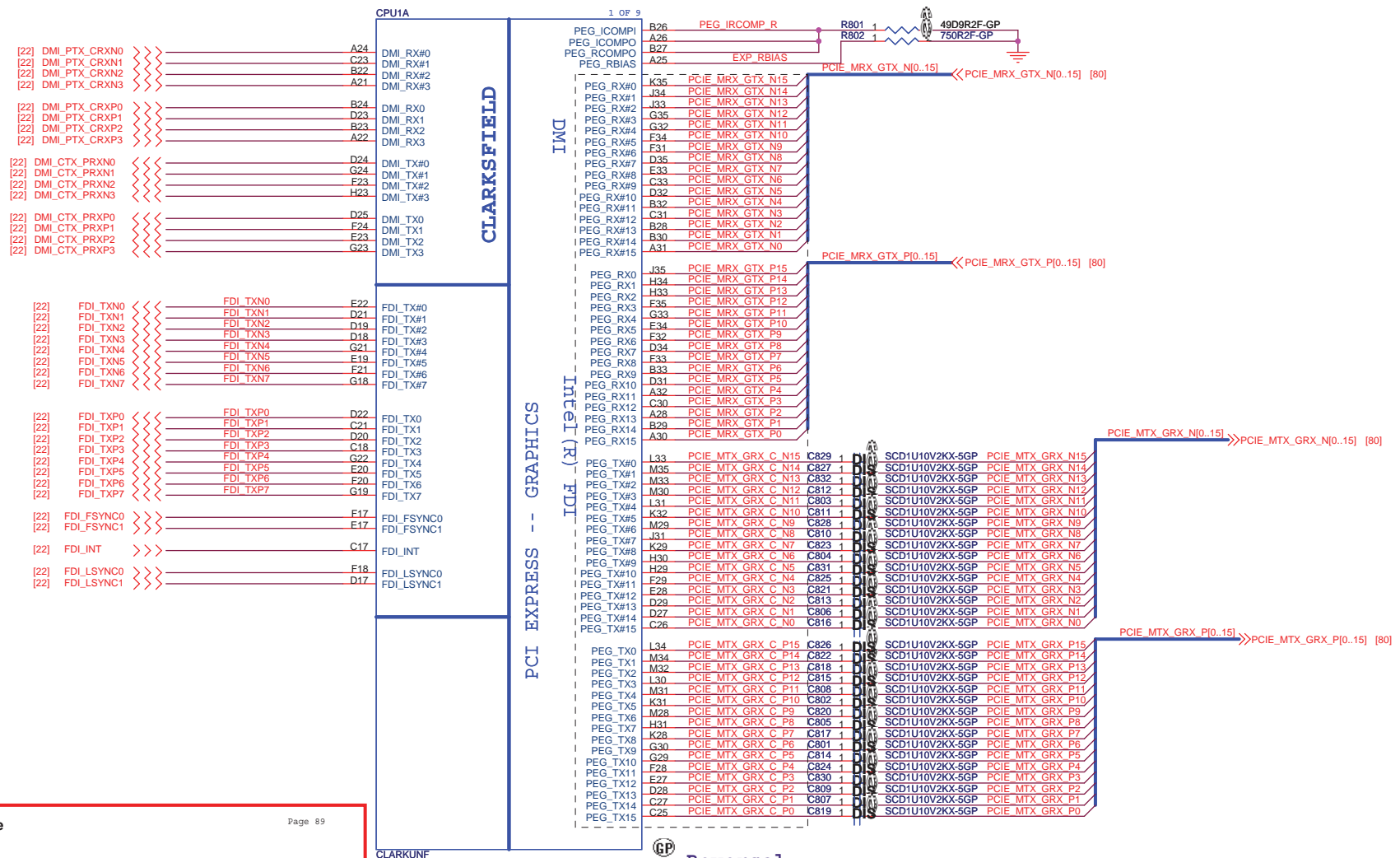


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| Title  |                          |  | <b>Table of Content</b> |   |       |
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**Calpella Platform Design Guide**  
**Revision 1.6**

## 2.4 Arrandale Graphics Disable Guideline

It applies to Arrandale and Clarksfield discrete graphic designs.

FDI\_TX[7:0] and FDI\_TX#[7:0] can be left floating on the Arrandale. The GFX\_IMON, FDI\_FSYNC[0], FDI\_FSYNC[1], FDI\_LSYNC[0], FDI\_LSYNC[1], and FDI\_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

## Reversal

### 1. PCI-Express Static Lane Reversal (15 -> 0, 14 -> 1, ...)

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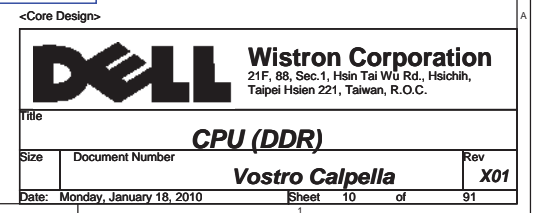


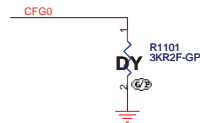
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| Title                     |                          |  |               |
| <b>CPU (PCIE/DMI/FDI)</b> |                          |  |               |
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|                           | <b>Vostro Calpella</b>   |  | <b>X0</b>     |
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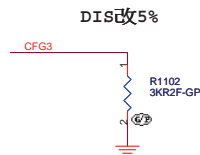




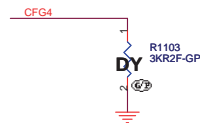




| PCI-Express Configuration Select |                                       |
|----------------------------------|---------------------------------------|
| CFG0                             | 1:Single PEG<br>0:Bifurcation enabled |



| CFG3 - PCI-Express Static Lane Reversal |                                                                        |
|-----------------------------------------|------------------------------------------------------------------------|
| CFG3                                    | 1:Normal Operation<br>0:Lane Numbers Reversed<br>15 -> 0, 14 -> 1, ... |



| CFG4 - Display Port Presence |                                                                                                                                                                |
|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFG4                         | 1:Disabled; No Physical Display Port attached to Embedded Display Port<br>0:Enabled; An external Display Port device is connected to the Embedded Display Port |

#### Calpella Platform Design Guide Revision 1.6

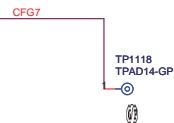
##### 4.8.3.1 LVDS Switching

Switchable GFX, just like integrated GFX only, to enable LVDS it is required that the OEM set the LDVS (L\_DDC\_DATA) strap to present (pulled up) and the eDP strap (CFG[4]) to disabled (not pulled down).

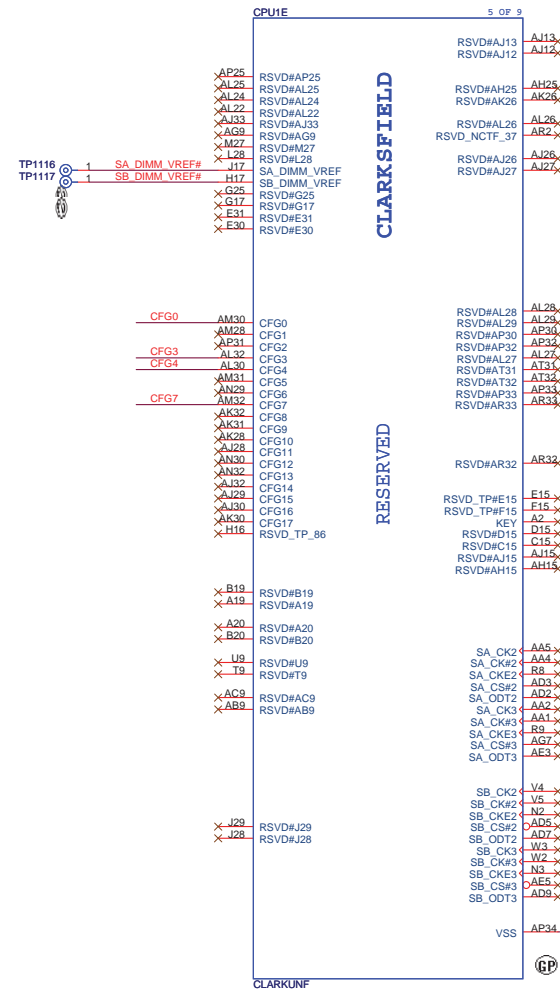
##### 4.8.3.2 eDP Switching

eDP for Switchable GFX can only be driven out of Port D of PCH. To configure Port D for embedded DP it is required to set the DDPD\_CTRLDATA strap high to 3.3V Core rail through 2.2 kΩ ±5% resistor, LVDS (L\_DDC\_DATA) strap as no connect and the eDP strap CFG[4] as no connect.

Page 482,486



| CFG7(Reserved) - Temporarily used for early Clarksfield samples. |                                                                                                                                                                                                                                                                                                                                               |
|------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFG7                                                             | Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.<br><br>Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report].<br>For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality. |

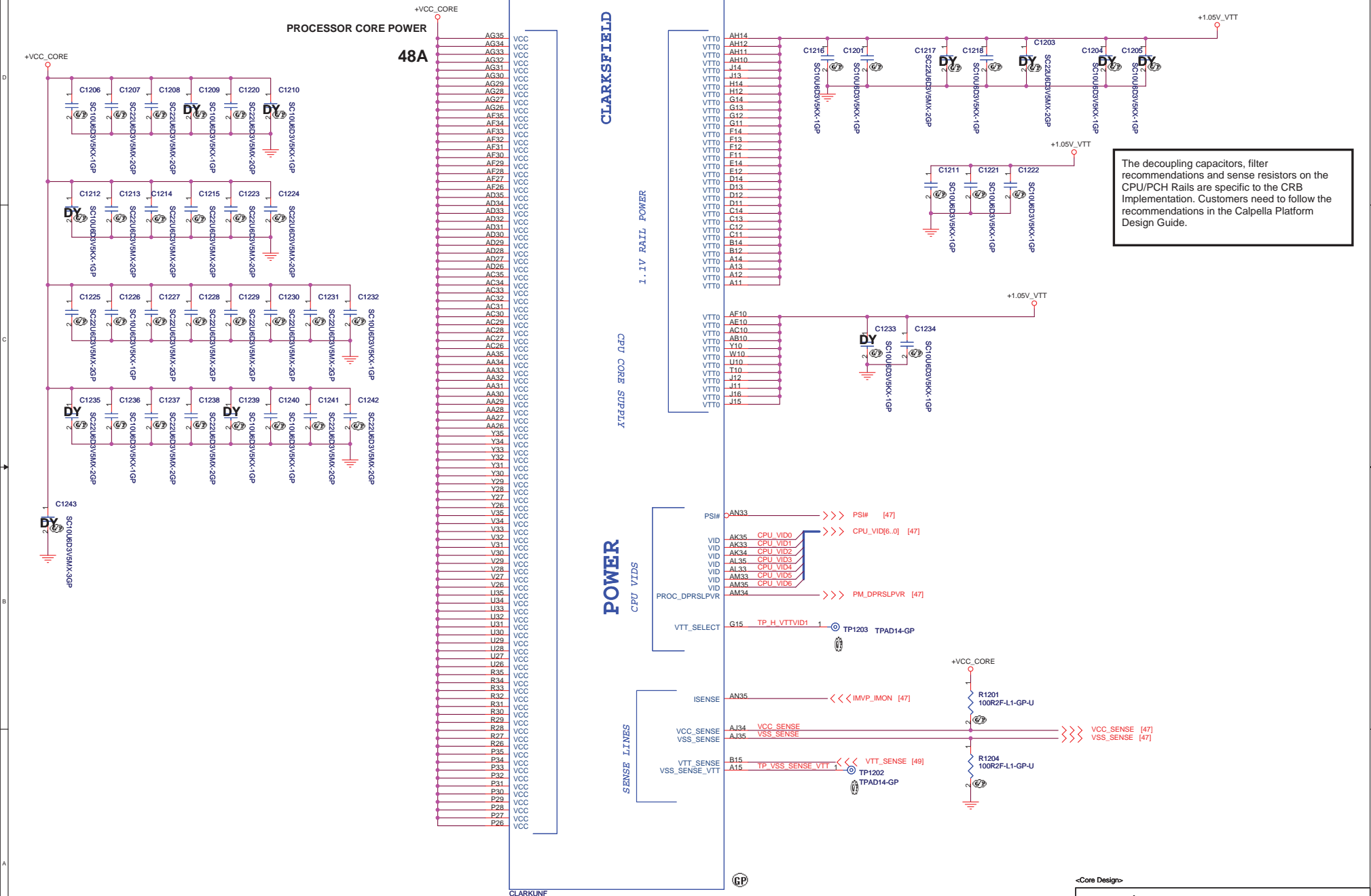


VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

<Core Design>



| Title          |                          |       |          |
|----------------|--------------------------|-------|----------|
| CPU (RESERVED) |                          |       |          |
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|                |                          |       | X01      |
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Title **CPU (VCC\_CORE)**

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|------|-----------------|------------|
|      |                 | <b>X01</b> |

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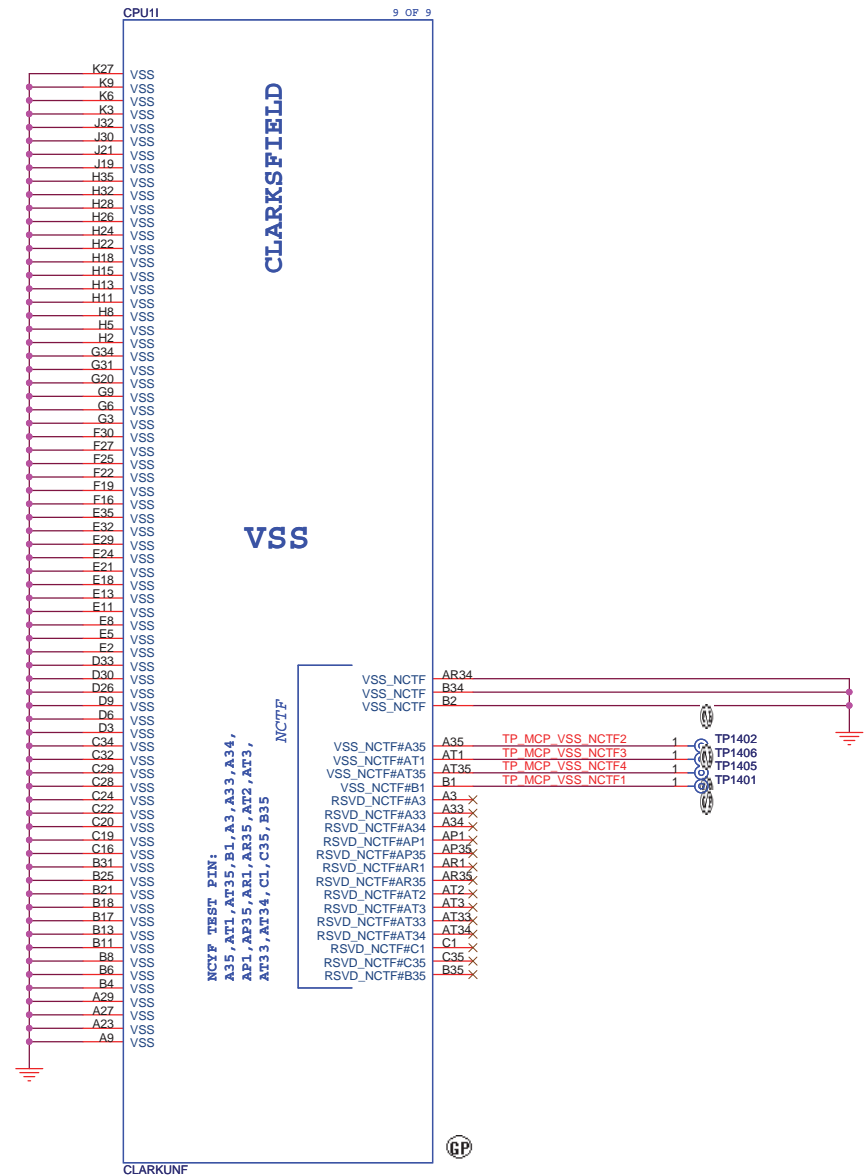


35A

+1.8V\_RUN

C1322

SC10U6D3V5MX-3GP



h t t p : / / l a p t o p b l u e . v n

(Blanking)

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**Vostro Calpella**

Rev  
**X01**

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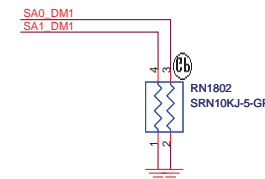
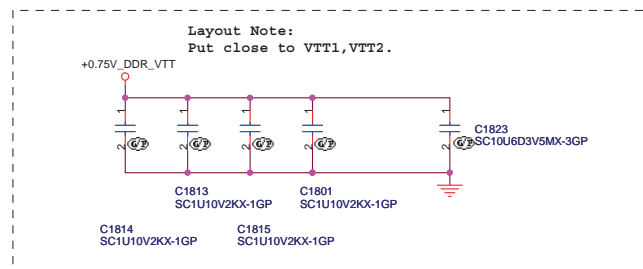
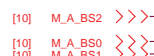
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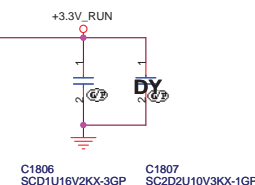
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| (Reserve)                                                                             |                 |                                                                                                             |     |
| Size                                                                                  | Document Number | Rev                                                                                                         |     |
| Custom                                                                                | Vostro Calpella |                                                                                                             |     |
| Unit                                                                                  | Model           | Part                                                                                                        | Rev |
| 1                                                                                     | 18              | 1                                                                                                           | 1   |
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h t t p : / / l a p t o p - m o t h e r b o a r d - s c h e m a t i c . b l o g s p o t . c o m /

Diagram illustrating a network connection between a laptop and a server (blue). The connection is labeled `http://laptop.blue.vn`. The connection is shown as a blue line with a red line above it. The red line is labeled `DM1` and the blue line is labeled `NP1`.

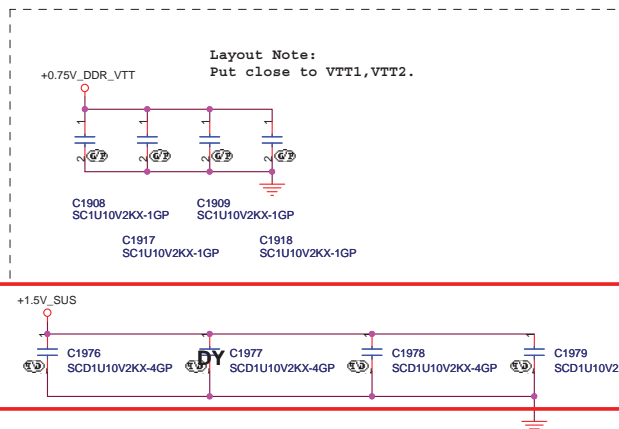


SMBUS address:A0

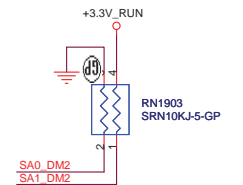
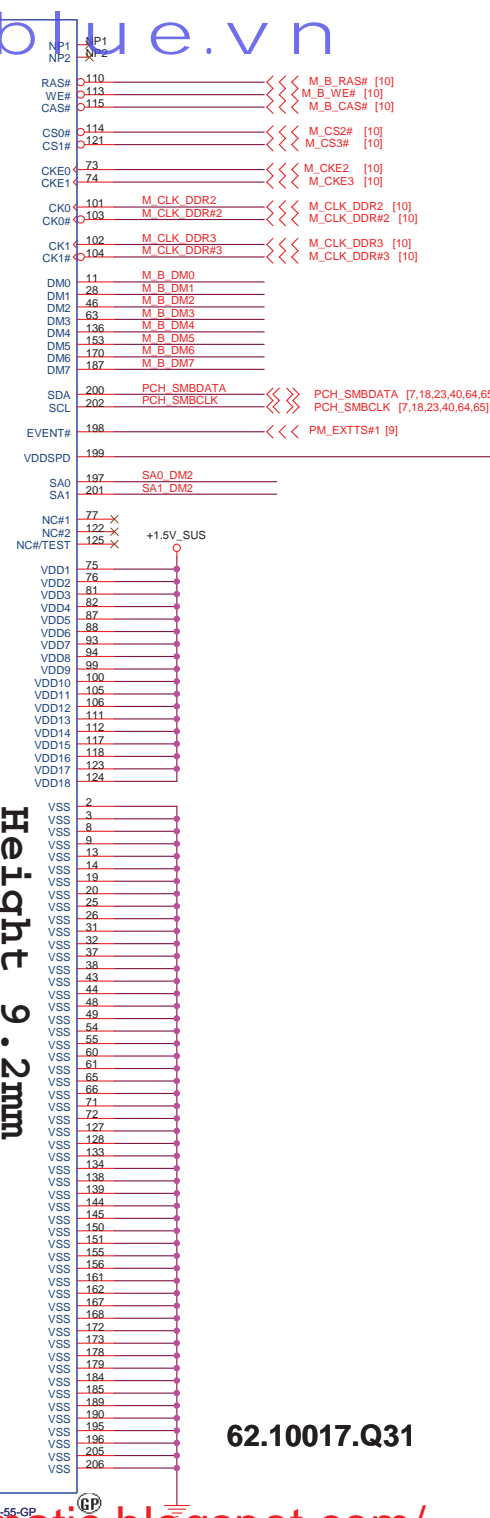
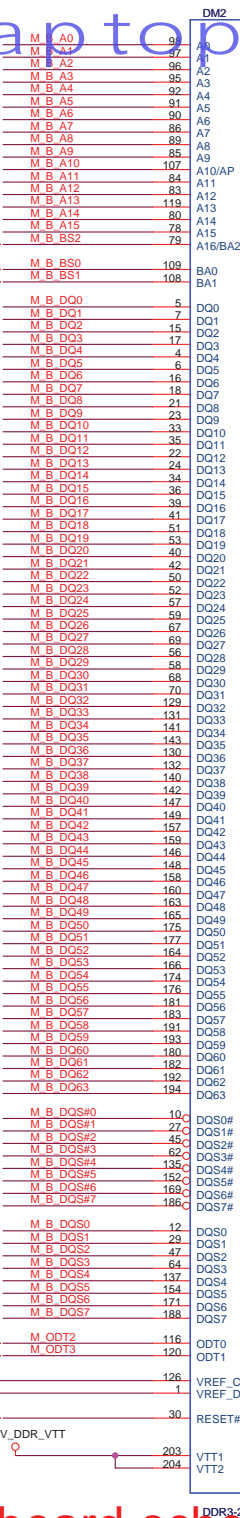


http://lapobtube.vn

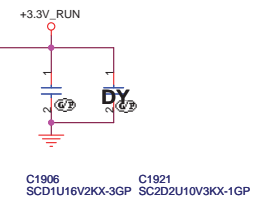
```
[10] M_B_BS2 >>>
[10] M_B_BS0 >>>
[10] M_B_BS1 >>>
```



The figure contains two schematic diagrams. The top diagram is for the SCD1U16V2KX-3GPs and shows a +V\_DDR\_REF signal line. A capacitor C1907 is connected between the signal line and ground. A diode labeled 'DY' is connected between the signal line and another capacitor C1914, which is also connected to ground. The bottom diagram is for the SCD2U10V3KX-1GPs and shows a similar +V\_DDR\_REF signal line. A capacitor C1910 is connected between the signal line and ground. A diode labeled 'DY' is connected between the signal line and another capacitor C1912, which is also connected to ground.



SMBUS address:A4



```
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
If SA0_DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4
```

Height 9.2mm

**62.10017.Q31**

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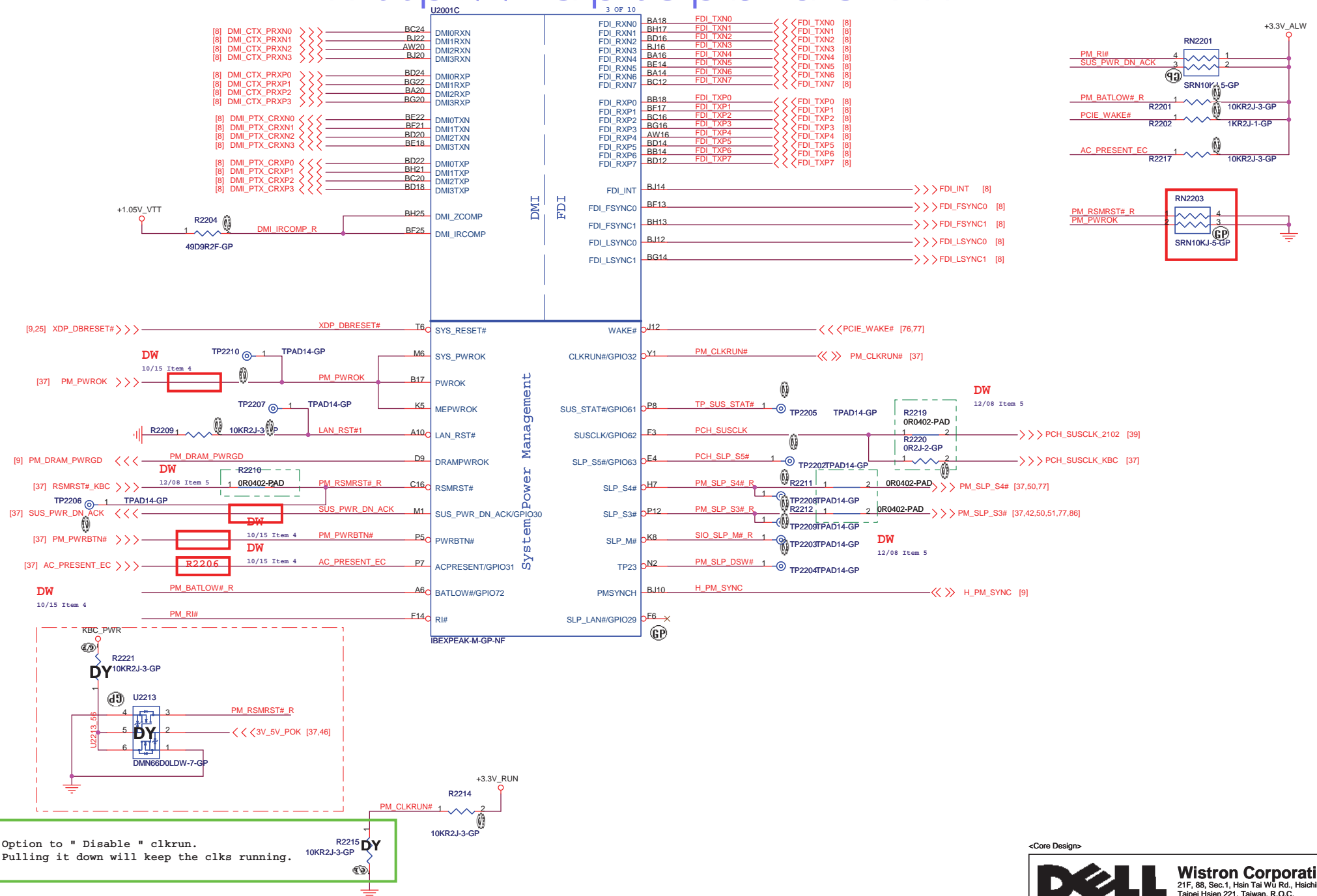
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| <b>DDRIII-SODIMM SLOT2</b>     |                        |            |       |
| Size                           | Document Number        | Rev        |       |
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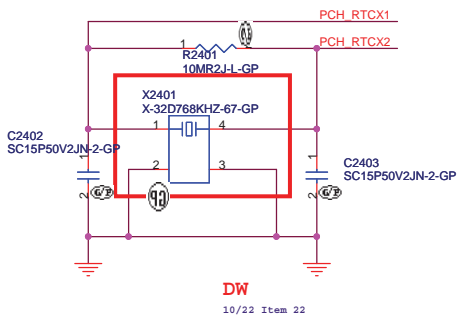






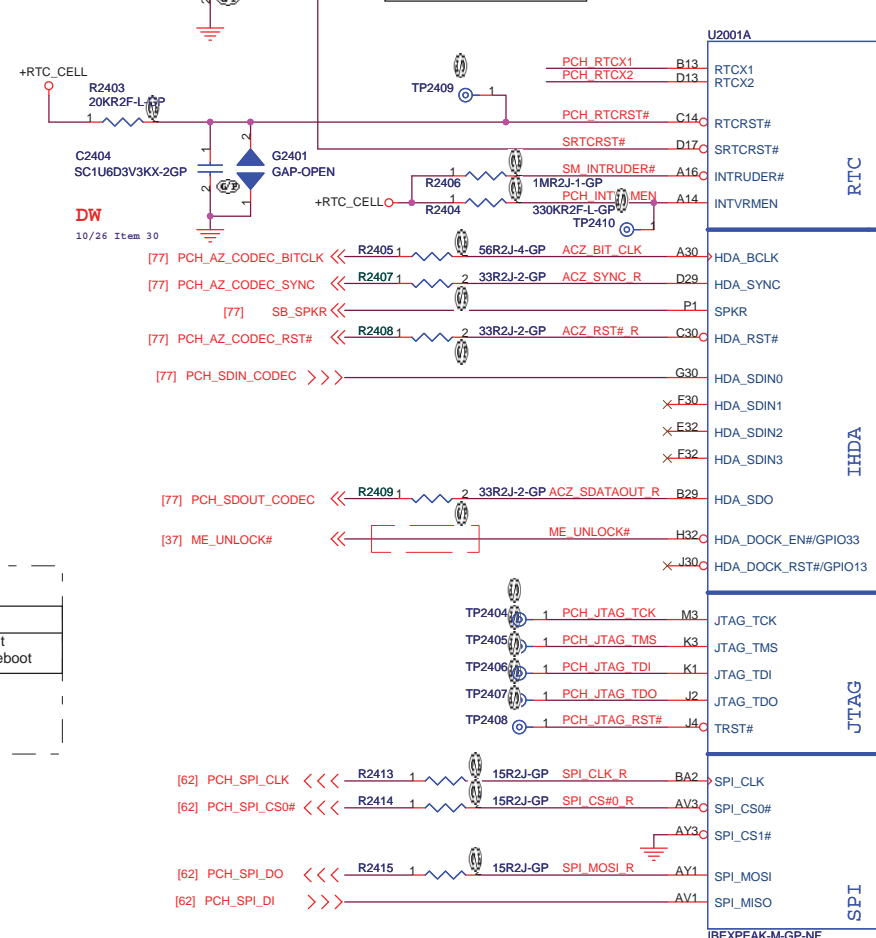






<http://laptopblue.vn>

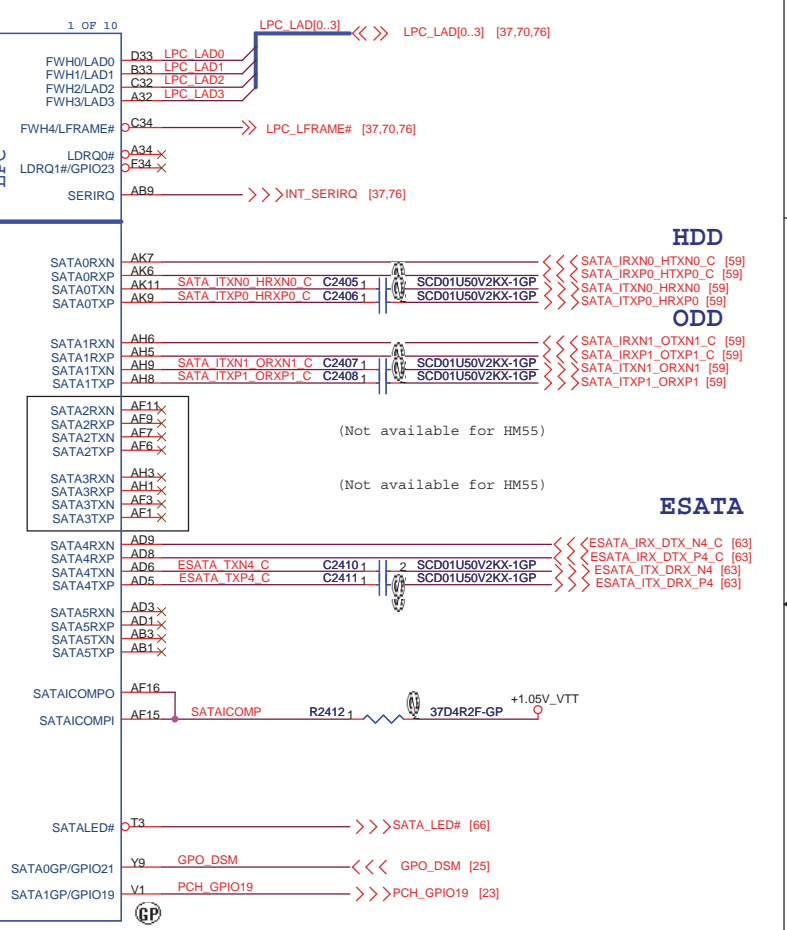
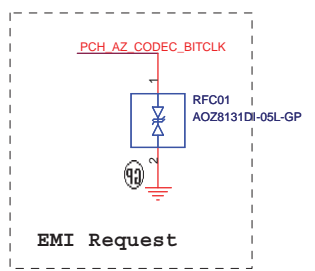
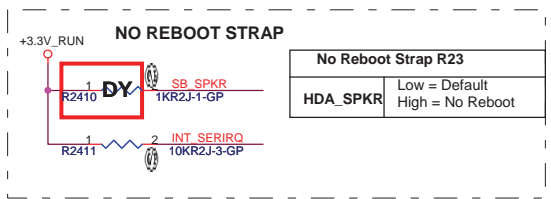
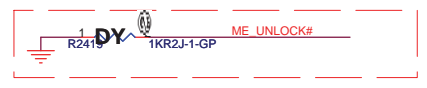
INTVRMEN- Integrated SUS  
1.1V VRM Enable  
High - Enable internal VRs



**Flash Descriptor Security  
Override/ ME Debug Mode**

**ME\_UNLOCK#**

This strap should only be asserted low via external pull down in manufacturing/debug environments ONLY.



**HDD**

**ODD**

**ESATA**

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Title: **PCH (SPI/RTC/LPC/SATA/IHDA)**

Size: Document Number Rev: **X01**

Date: Monday, January 18, 2010 Sheet 24 of 91

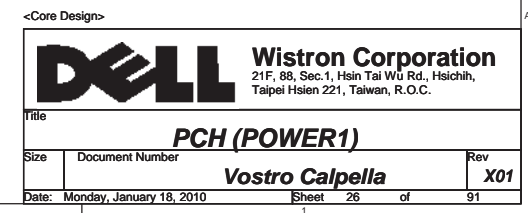
**Vostro Calpella**

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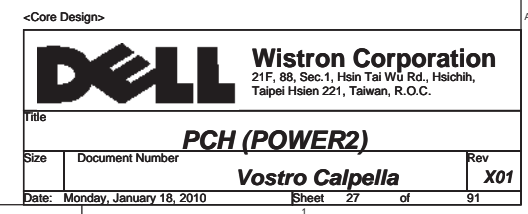


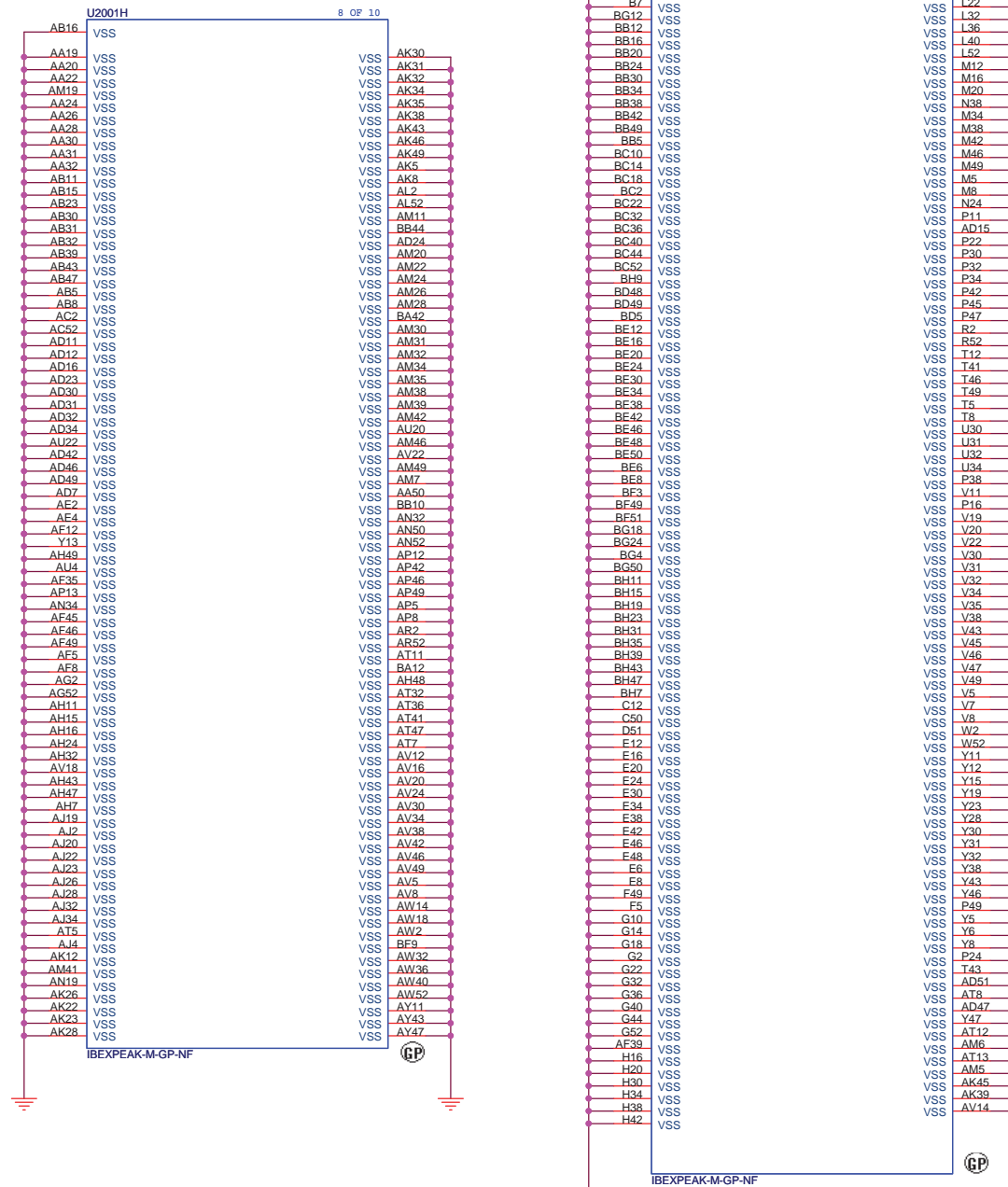
DW 10/15 Item 1





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| <Core Design>                                                                                                                                                                                     |                                           |                   |
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| Title                                                                                                                                                                                             |                                           |                   |
| (Reserve)                                                                                                                                                                                         |                                           |                   |
| Size<br>Custom                                                                                                                                                                                    | Document Number<br><b>Vostro Calpella</b> | Rev<br><b>X01</b> |
| Date: Monday, January 18, 2010                                                                                                                                                                    |                                           |                   |
| Sheet 29 of 91                                                                                                                                                                                    |                                           |                   |

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| Title                                                                                 |                                           |                                                                                                             |
| (Reserve)                                                                             |                                           |                                                                                                             |
| Size<br>Custom                                                                        | Document Number<br><b>Vostro Calpella</b> | Rev<br><b>X01</b>                                                                                           |
| Date: Monday, January 18, 2010                                                        |                                           | Sheet 30 of 91                                                                                              |

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| Title                                                                                                                                                                                             |                                           |                   |
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| Date: Monday, January 18, 2010                                                                                                                                                                    |                                           |                   |
| Sheet 31 of 91                                                                                                                                                                                    |                                           |                   |

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<Core Design>



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Title

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Size  
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Document Number

**Vostro Calpella**

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**X01**

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| <div><div>DELL</div><div>Wistron Corporation<br/>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br/>Taipei Hsien 221, Taiwan, R.O.C.</div></div> |                                           |                   |
| Title                                                                                                                                       |                                           |                   |
| (Reserve)                                                                                                                                   |                                           |                   |
| Size<br>Custom                                                                                                                              | Document Number<br><b>Vostro Calpella</b> | Rev<br><b>X01</b> |
| Date: Monday, January 18, 2010                                                                                                              |                                           |                   |
| Sheet 33 of 91                                                                                                                              |                                           |                   |

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| Title                                                                                                                                                                                             |                                           |                   |
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| Size<br>Custom                                                                                                                                                                                    | Document Number<br><b>Vostro Calpella</b> | Rev<br><b>X01</b> |
| Date: Monday, January 18, 2010                                                                                                                                                                    |                                           |                   |
| Sheet 34 of 91                                                                                                                                                                                    |                                           |                   |

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<Core Design>



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Document Number

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<Core Design>



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Title

**(Reserve)**

Size  
A3

Document Number

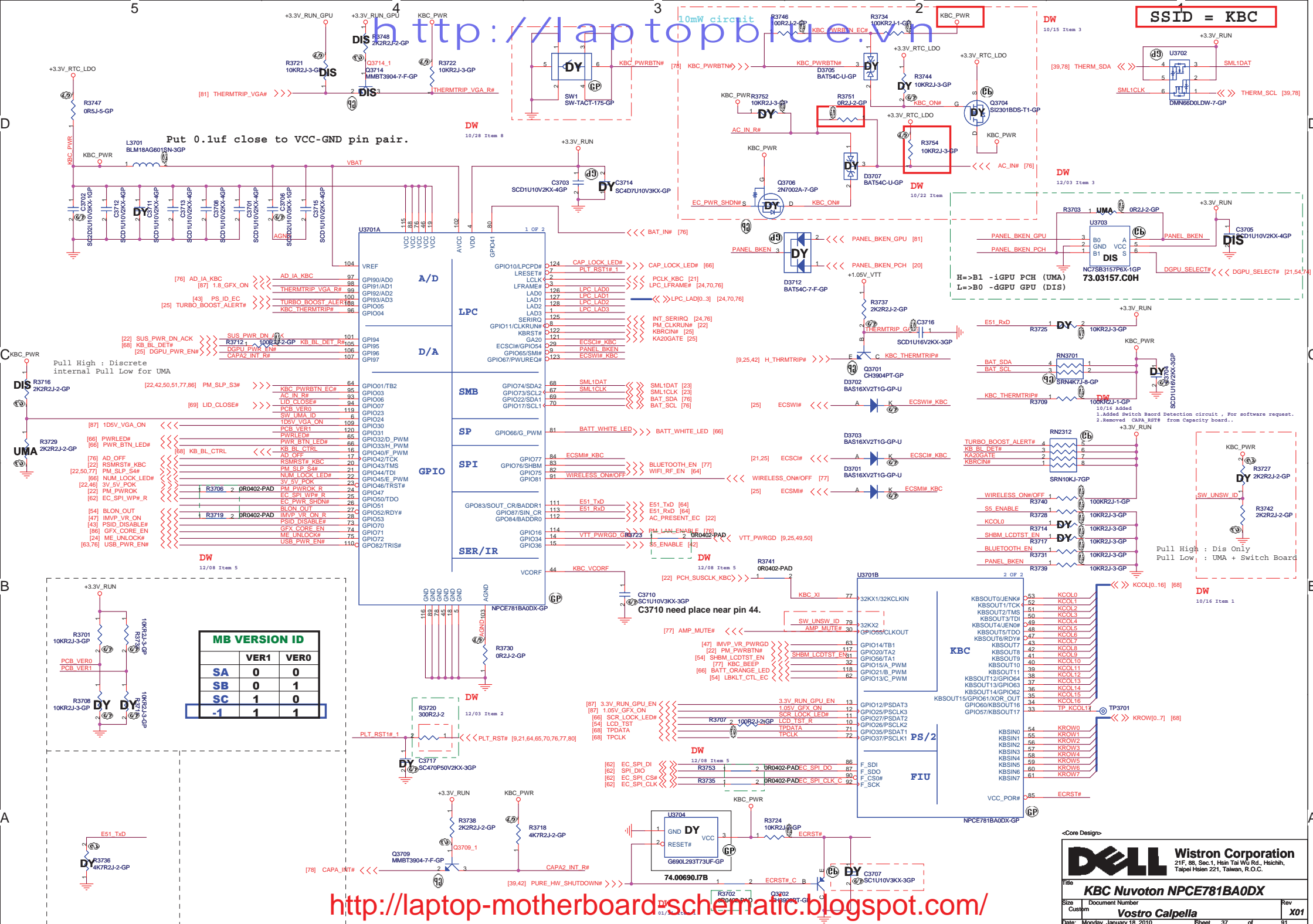
**Vostro Calpella**

Rev

**X01**

Date: Monday, January 18, 2010

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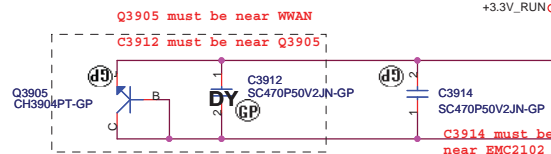
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| <Core Design>                                                                                                                                                                                     |                                           |                   |
|  <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                                           |                   |
| Title                                                                                                                                                                                             |                                           |                   |
| (Reserve)                                                                                                                                                                                         |                                           |                   |
| Size<br>Custom                                                                                                                                                                                    | Document Number<br><b>Vostro Calpella</b> | Rev<br><b>X01</b> |
| Date: Monday, January 18, 2010                                                                                                                                                                    |                                           |                   |
| Sheet 38 of 91                                                                                                                                                                                    |                                           |                   |

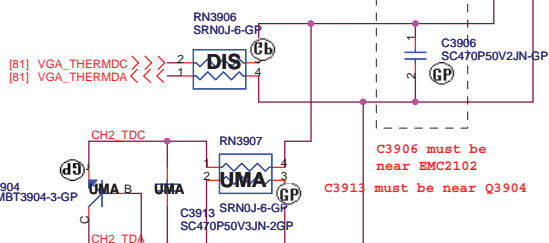
SSID = Thermal

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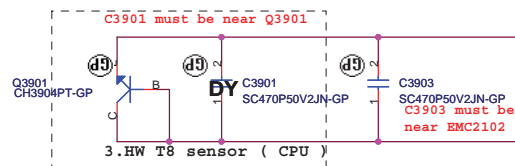
## 1. WWAN



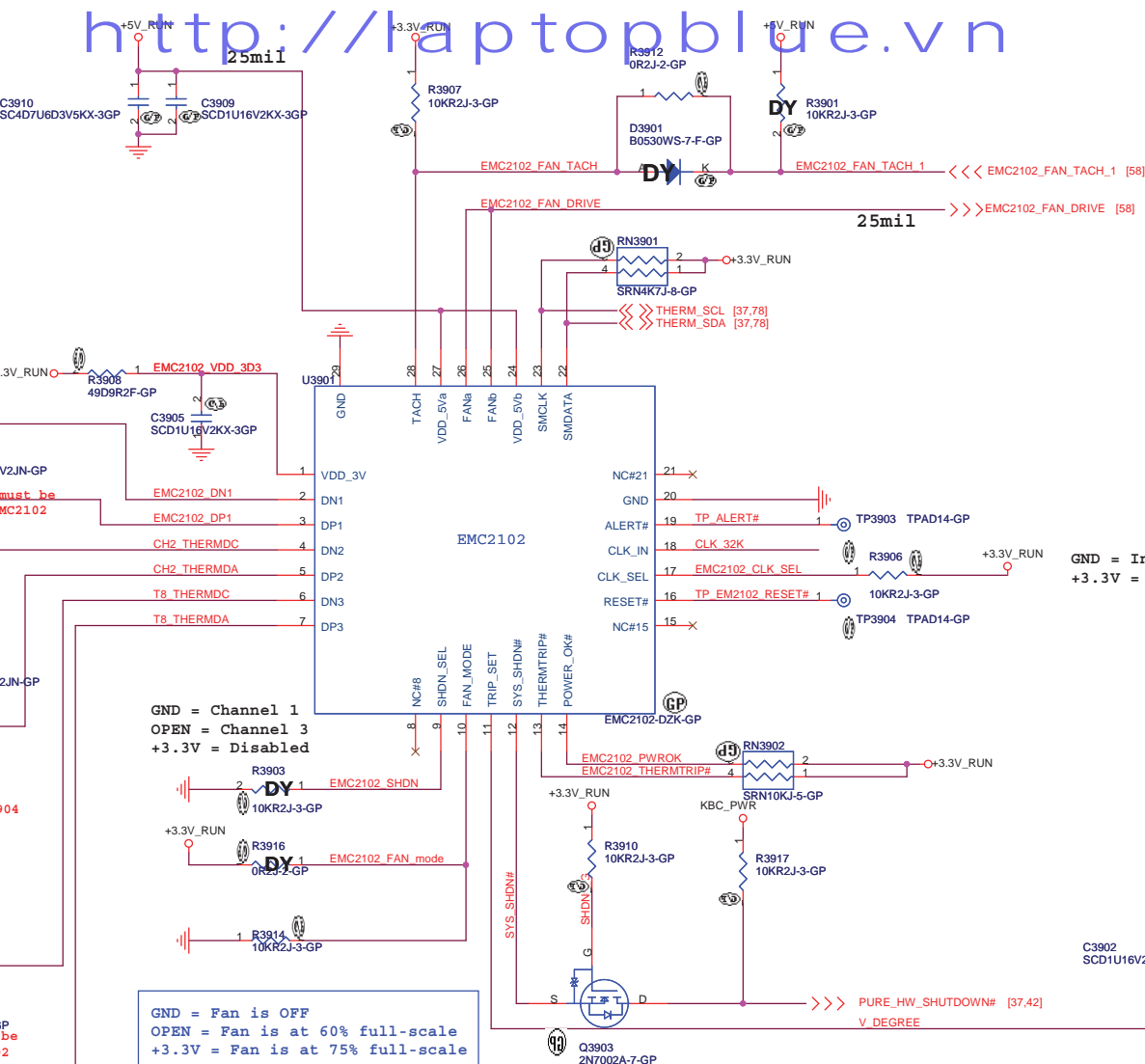
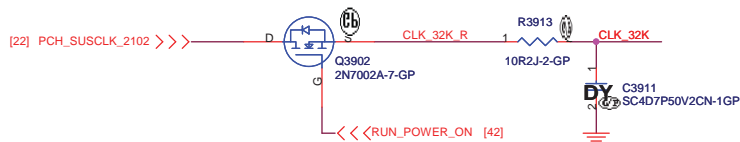
## 2. GPU Sensor



## 3. HW T8 sensor (CPU)



32K suspend clock output



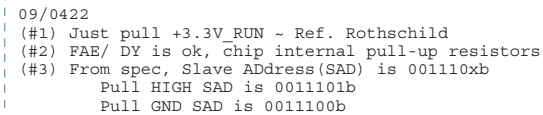
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| Title                                                                                 |                          |                                                                                                             |            |
| <b>Thermal/Fan Controller EMC2102</b>                                                 |                          |                                                                                                             |            |
| Size                                                                                  | Document Number          |                                                                                                             | Rev        |
| Custom                                                                                | <b>Vostro Calpella</b>   |                                                                                                             | <b>X01</b> |
| Date:                                                                                 | Monday, January 18, 2010 | Sheet 39 of 91                                                                                              |            |

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```
| Note
| - no via, trace, under the sensor (keep out area around 2mm)
| - stay away from the screw hole or metal shield soldering joints
| - design PCB pad based on our sensor LGA pad size (add 0.1mm)
| - solder stencil opening to 90% of the PCB pad size
| - mount the sensor near the center of mass of the NB as possible as you can
```



<Core Design>


|                                                                                       |                          |                                                                                                             |          |
|---------------------------------------------------------------------------------------|--------------------------|-------------------------------------------------------------------------------------------------------------|----------|
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| Title                                                                                 |                          |                                                                                                             |          |
| Size                                                                                  |                          | <b>Free Fall Sensor</b>                                                                                     |          |
| Custom                                                                                | Document Number          | Rev                                                                                                         |          |
| <b>Vostro Calpella</b>                                                                |                          | <b>X01</b>                                                                                                  |          |
| Date:                                                                                 | Monday, January 18, 2010 | Sheet                                                                                                       | 40 of 91 |



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| Title                                                                                                |                                    |            |
| (Reserve)                                                                                            |                                    |            |
| Size<br>Custom                                                                                       | Document Number<br>Vostro Calpella | Rev<br>X01 |
| Date: Monday, January 18, 2010                                                                       |                                    |            |
| Sheet 41 of 91                                                                                       |                                    |            |

SSID = Reset.Suspend

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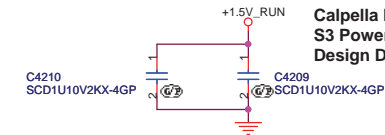
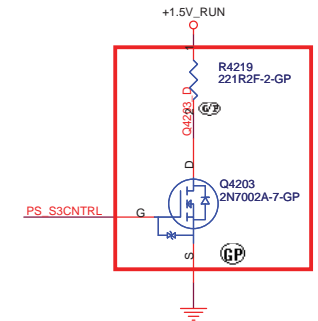
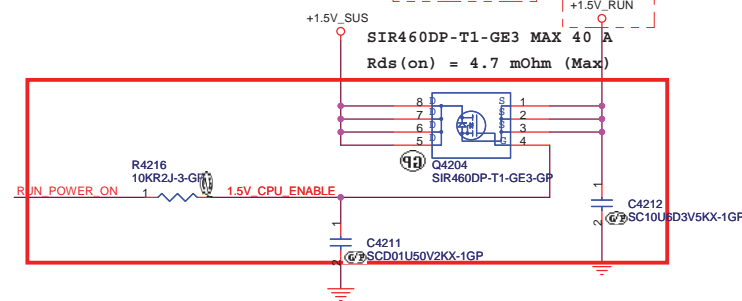
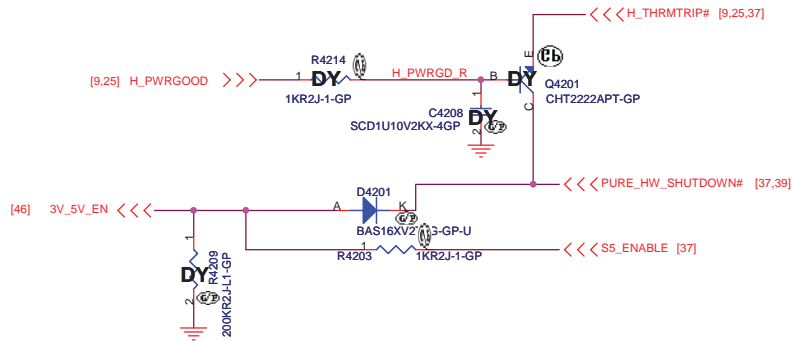
+1.5V\_RUN:

Peak current: 4650 mA

Design current: 3255 mA

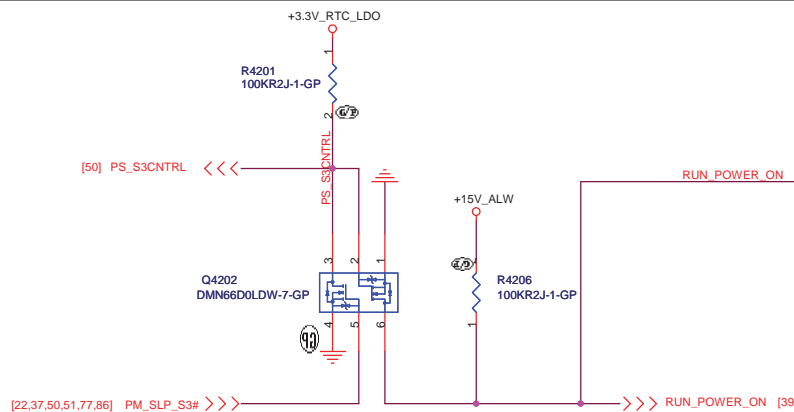
DW

10/26 Item 3



Calpella Platform S3 Power Reduction Platform  
S3 Power Reduction CRB Implementation  
Design Details

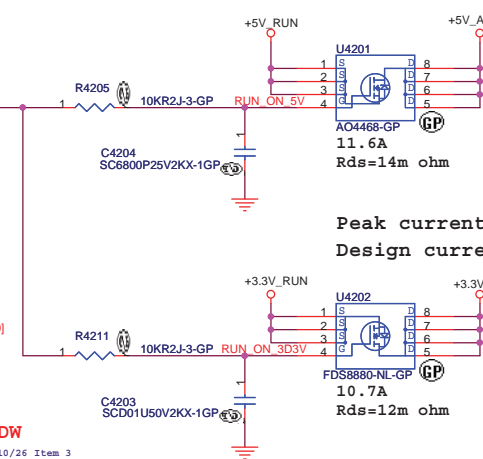
Revision 0.1



DW  
10/26 Item 3

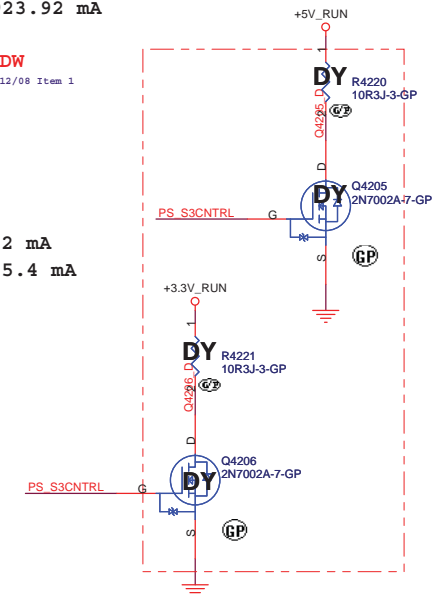
Peak current: 5605.6mA ( HD:1100 ODD:2500 )

Design current: 3923.92 mA



Peak current: 8379.2 mA  
Design current: 5865.4 mA

DW  
12/08 Item 1

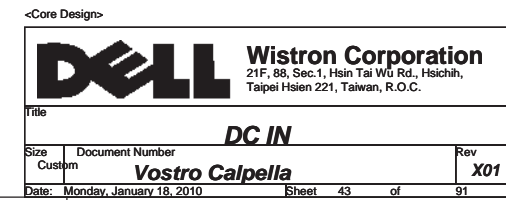


<Core Design>

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| <b>DELL</b>                                                                |                                         | <b>Wistron Corporation</b> |  |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |                                         |                            |  |
| Title: <b>Power Plane Enable</b>                                           |                                         |                            |  |
| Size: Custom                                                               | Document Number: <b>Vostro Calpella</b> | Rev: <b>X01</b>            |  |
| Date: Monday, January 18, 2010                                             | Sheet: 42                               | of: 91                     |  |

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| Title                                                                                 |                                           |                                                                                                              |                   |
| (Reserve)                                                                             |                                           |                                                                                                              |                   |
| Size<br>A3                                                                            | Document Number<br><b>Vostro Calpella</b> |                                                                                                              | Rev<br><b>X01</b> |
| Date: Monday, January 18, 2010                                                        | Sheet 1                                   | 44 of 91                                                                                                     |                   |

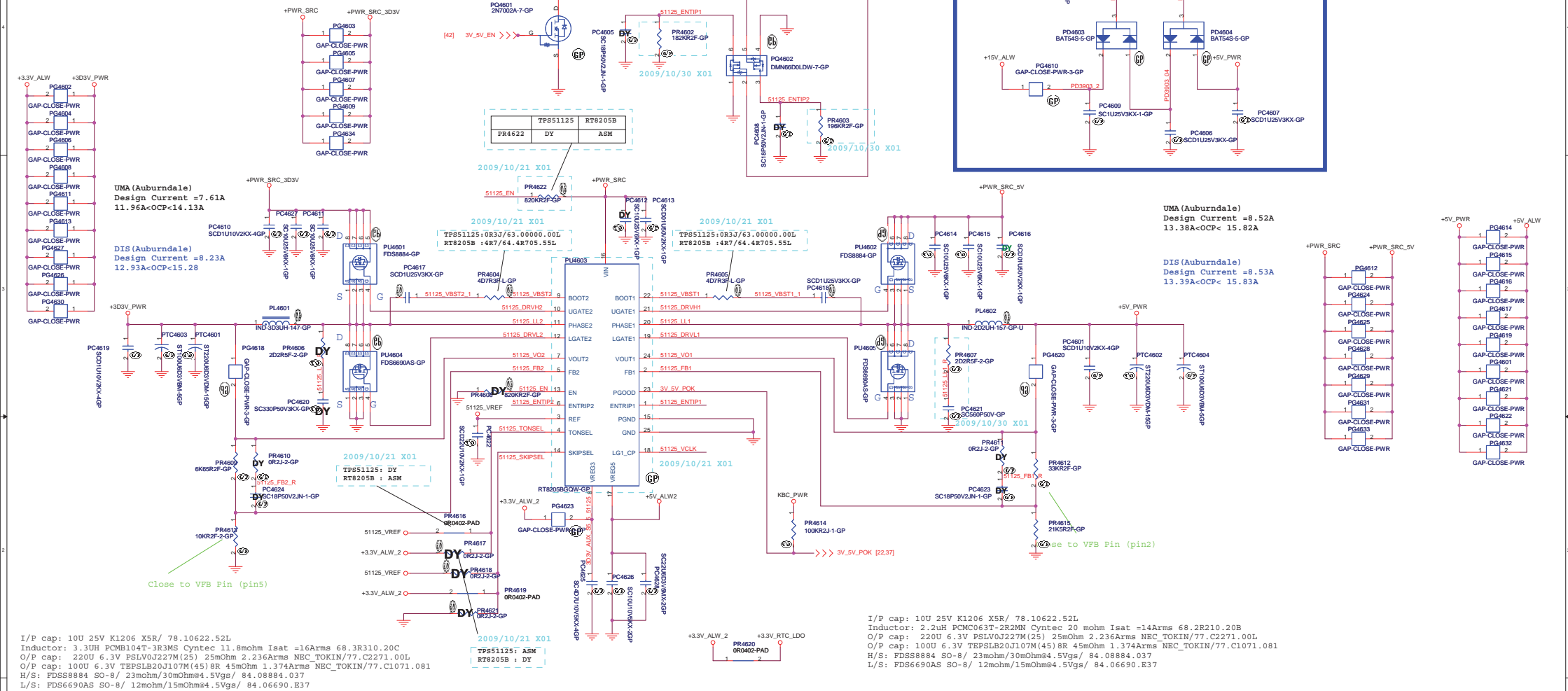
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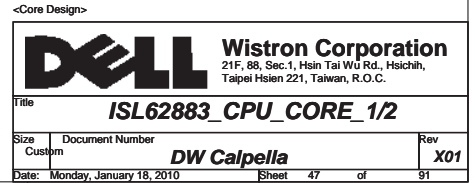
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|  |                                           | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                   |
| Title                                                                                 |                                           |                                                                                                             |                   |
| (Reserve)                                                                             |                                           |                                                                                                             |                   |
| Size<br>Custom                                                                        | Document Number<br><b>Vostro Calpella</b> |                                                                                                             | Rev<br><b>X01</b> |
| Date: Monday, January 18, 2010                                                        |                                           | Sheet 45 of 91                                                                                              |                   |

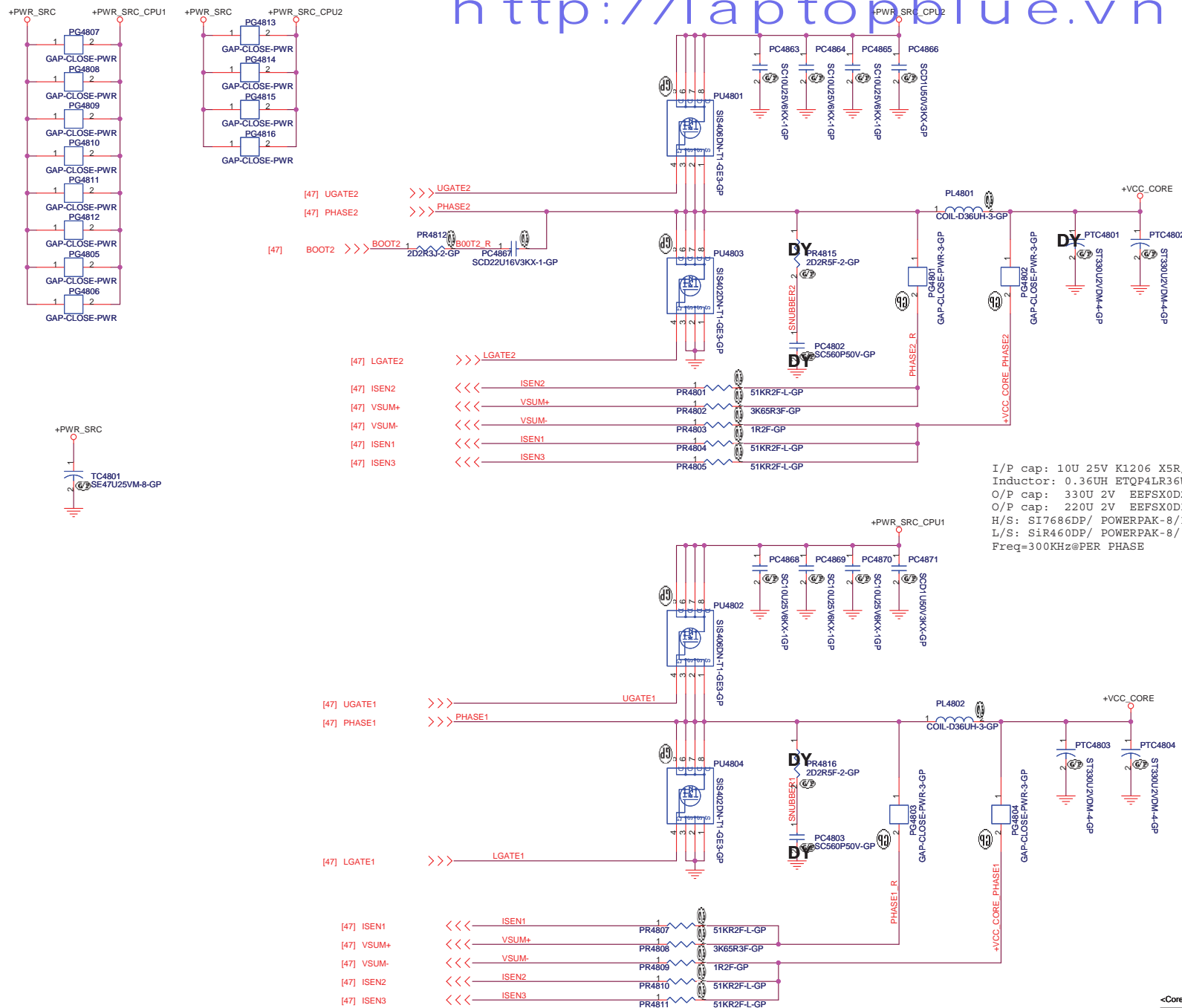


|        |        |        |                |                |           |          |
|--------|--------|--------|----------------|----------------|-----------|----------|
| TONSEL | CH1    | CH2    | SKIPSEL        | VREG3 or VREG5 | VREF (2V) | GND      |
| GND    | 200kHz | 265kHz | Operating Mode | OOA Auto Skip  | Auto Skip | PWM only |
| VREF   | 245kHz | 305kHz |                |                |           |          |
| VREG3  | 300kHz | 375kHz |                |                |           |          |
| VREG5  | 365kHz | 460kHz |                |                |           |          |

|                |                                                                  |                                                                   |                   |
|----------------|------------------------------------------------------------------|-------------------------------------------------------------------|-------------------|
| EN0            | Open                                                             | 820kΩ to GND                                                      | GND               |
| Operating Mode | enable both LDOs, VCLK on and ready to turn on switcher channels | enable both LDOs, VCLK off and ready to turn on switcher channels | disable a circuit |





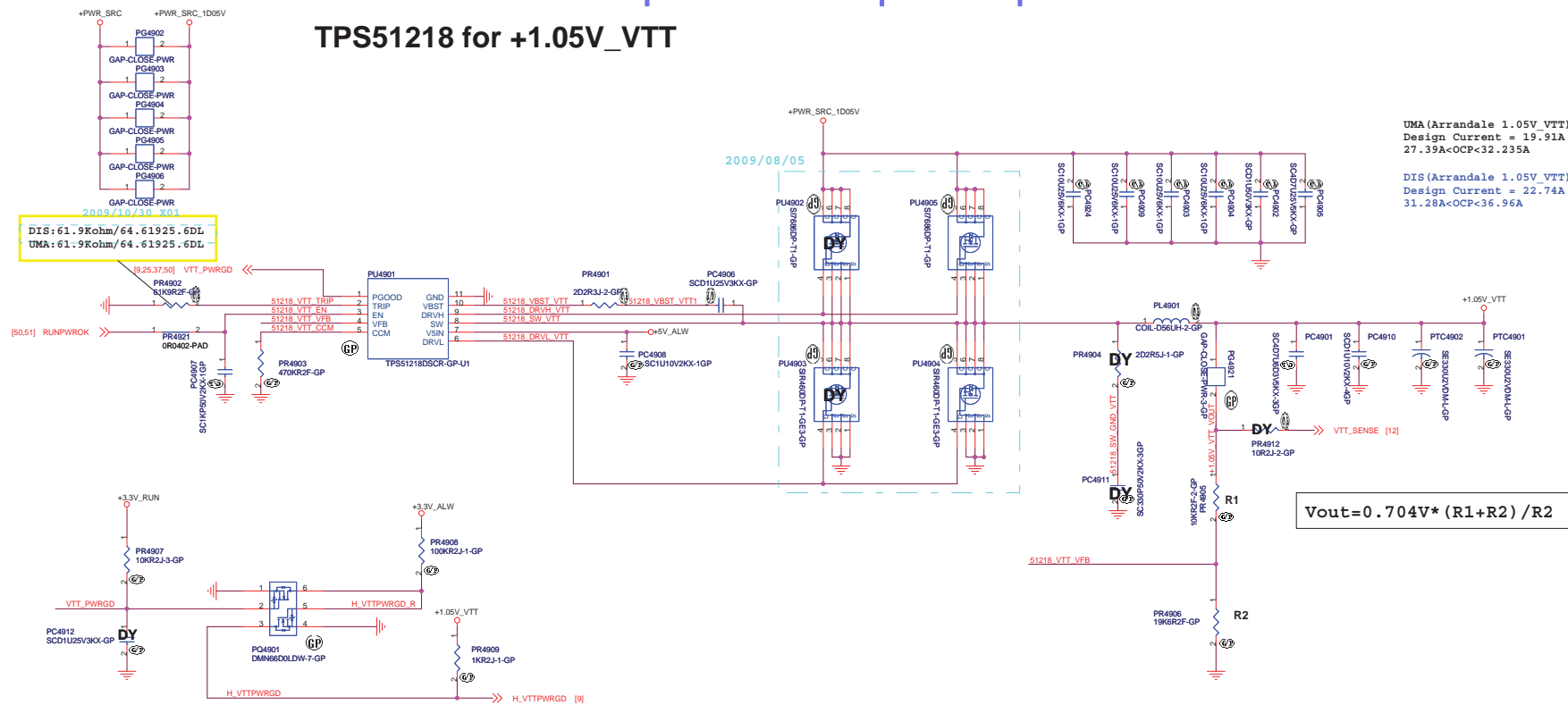
DIS(Auburndale)  
Design Current = 34A  
Peak Current=48A  
57.6A<OCP< 67.2A

UMA(Auburndale)  
Design Current = 34A  
Peak Current=48A  
57.6A<OCP< 67.2A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm/ 68.R3610.20A  
O/P cap: 330U 2V BEFSX0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L  
O/P cap: 220U 2V BEFSX0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L  
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037  
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037  
Freq=300KHz@PER PHASE



## TPS51218 for +1.05V\_VTT



```
Frequency setting
470K  -->290KHz
200K  -->340KHz
100K  -->380KHz
 39K  -->430KHz
```

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 0.56uH PCMC104T-R56M1N Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D  
O/P cap: 330U 2.5V EEP50X0331ER 50mOhm 3Arms PANASONIC/ 79.33719.101  
H/S: SR474DP-T1-GE3/3.0mohm/ 12mOhm@4.5Vgs/ 84.0474.037  
L/S: SR1710DP-T1-GE3/3.0mOhm/ 4.3mohm@4.5Vgs/ 84.01710.037

$$V_{out} = 0.704V * (R1 + R2) / R2$$

UMA(Arrandale 1.05V\_VTT)  
Design Current = 19.91A  
27.39A<OCP<32.235A

DIS(Arrandale 1.05V\_VTT)  
Design Current = 22.74A  
31.28A<OCP<36.96A

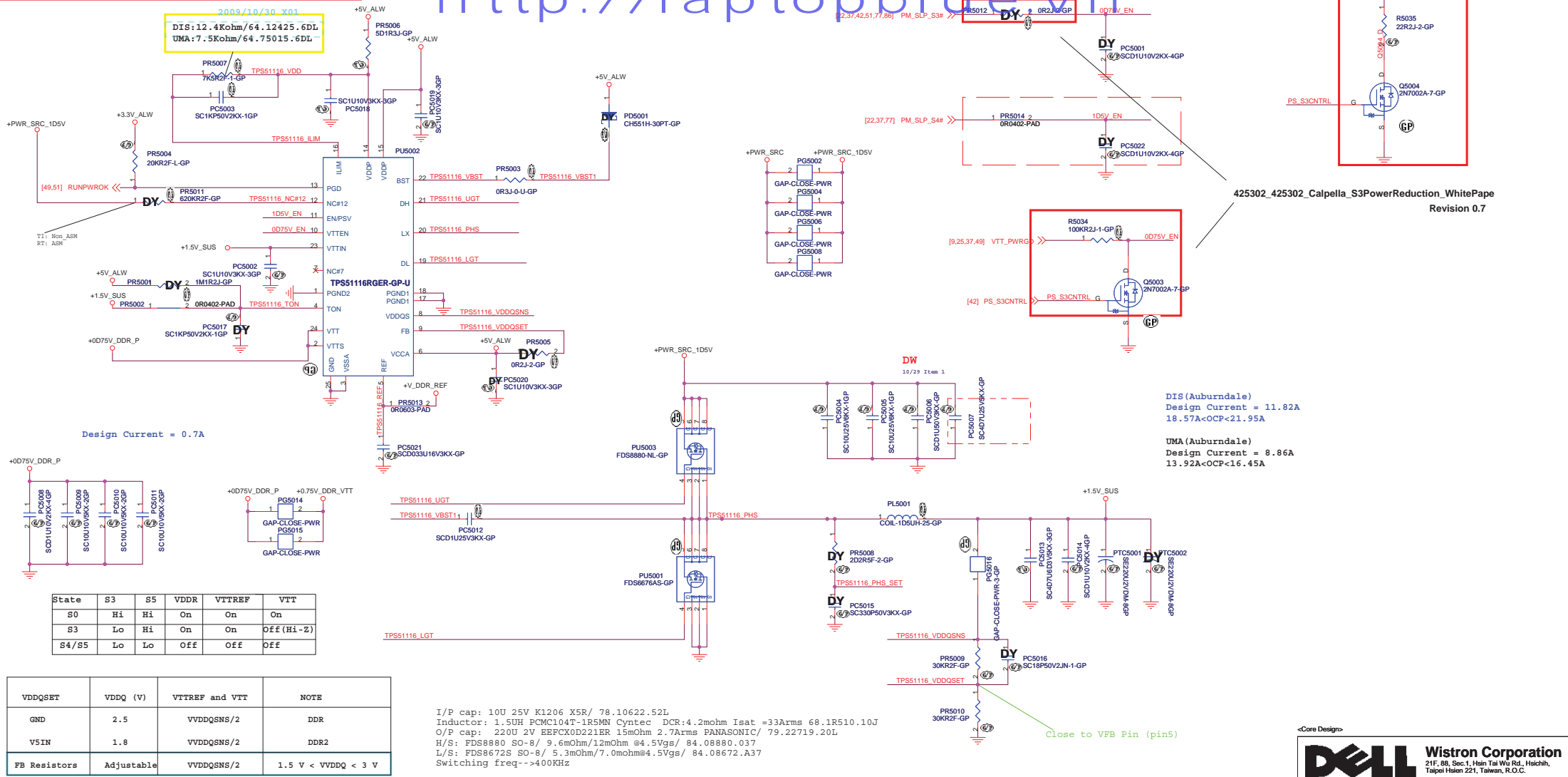
◀Core Design▶



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| Title                      |                          |             |           |
| <b>TPS51218 +1.05V VTT</b> |                          |             |           |
| Size                       | Document Number          |             | Rev       |
| Custom                     | <b>DW Calpella</b>       |             | <b>X0</b> |
| Date:                      | Monday, January 18, 2010 | Sheet 49 of | 91        |

SSID = PWR.Plane.Regulator\_1p5v0p75v

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

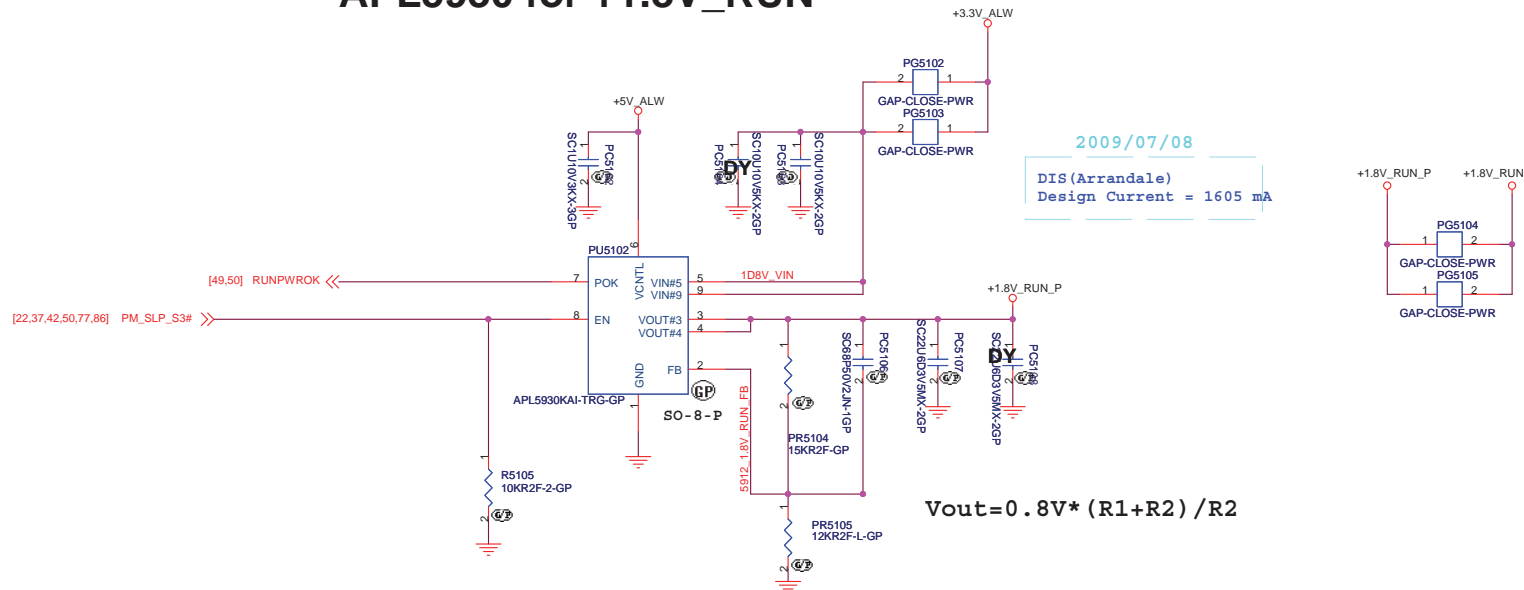
Title: **TPS51116 +1.5V\_SUS**

| Size   | Document Number    | Rev        |
|--------|--------------------|------------|
| Custom | <b>DW Calpella</b> | <b>X01</b> |

Date: Monday, January 18, 2010 Sheet 50 of 91

SSID = PWR.Plane.Regulator\_1p8v

## APL5930 for +1.8V\_RUN



<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

|          |                 |                   |                |     |
|----------|-----------------|-------------------|----------------|-----|
| Title    |                 | APL5930 +1.8V RUN |                | Rev |
| Size     | Document Number | DW Calpella       |                | X01 |
| Customer | Date            | January 18, 2010  | Sheet 51 of 91 |     |

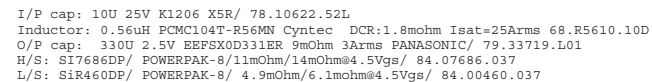
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| Title                                                                                 |                                           |                                                                                                             |                   |
| (Reserve)                                                                             |                                           |                                                                                                             |                   |
| Size<br>Custom                                                                        | Document Number<br><b>Vostro Calpella</b> |                                                                                                             | Rev<br><b>X01</b> |
| Date: Monday, January 18, 2010                                                        |                                           | Sheet 52 of 91                                                                                              |                   |

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|                                |                        |                |            |
|--------------------------------|------------------------|----------------|------------|
| Title                          |                        |                |            |
| <b>ADP3211 CPU GFXCORE</b>     |                        |                |            |
| Size                           | Document Number        |                | Rev        |
| Custom                         | <b>DW Calpella UMA</b> |                | <b>X01</b> |
| Date: Monday, January 18, 2010 |                        | Sheet 53 of 91 |            |

<http://laptop-motherboard-schematic.blogspot.com/>

SSID = VIDEO

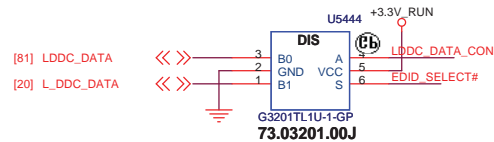
Close PCH

Close GPU

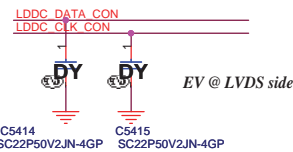
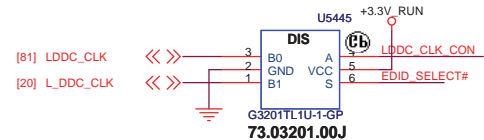
SSID = Inverter

UMA/DIS LVDS DDC CLK/DAT select circuit

H=>B1 -iGPU PCH (UMA)  
L=>B0 -dGPU GPU (DIS)



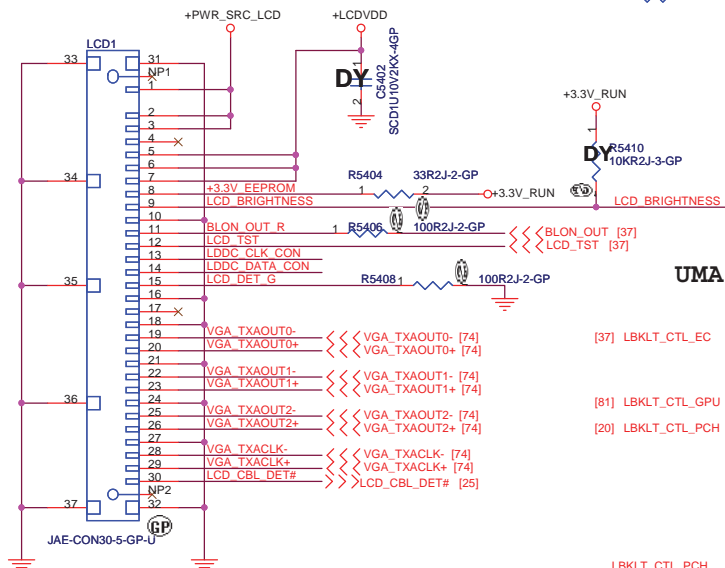
[21,55,57] EDID\_SELECT# >>> EDID\_SELECT#



EV @ LVDS side

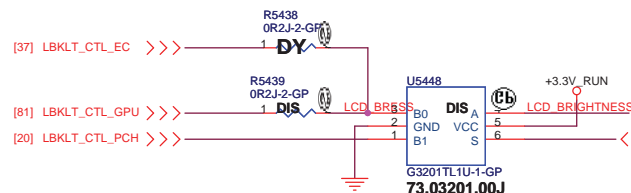
L DDC DATA R5421 1 UMA 0R2J-2-GP LDDC\_DATA\_CON  
L DDC CLK R5420 1 UMA 0R2J-2-GP LDDC\_CLK\_CON

LVDS CONNECTOR



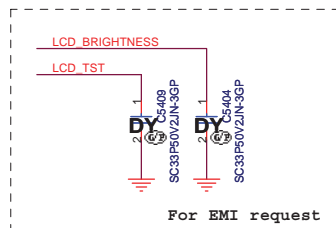
20.F1555.030

UMA/DIS LVDS PWM select circuit

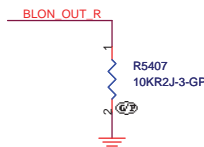


H=>B1 -iGPU PCH (UMA)  
L=>B0 -dGPU GPU (DIS)

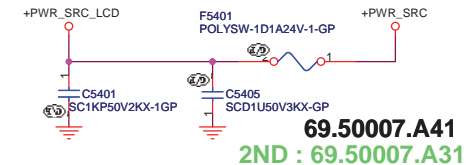
LBKLT\_CTL\_PCH R5422 1 UMA 0R2J-2-GP LCD\_BRIGHTNESS  
LBKLT\_CTL\_EC R5424 1 DY 0R2J-2-GP



For EMI request

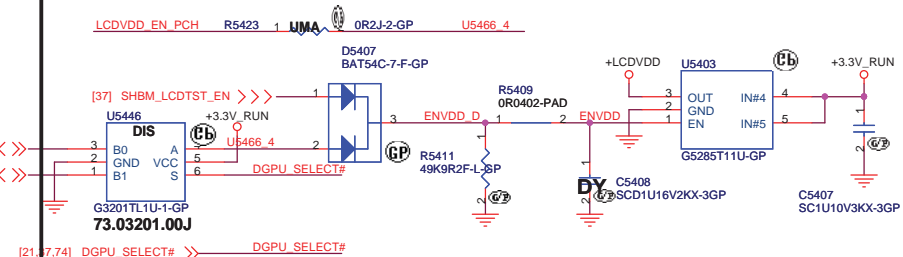
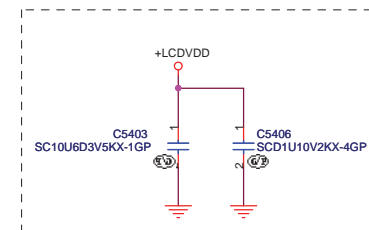


INVERTER POWER



SSID = VIDEO

LCD POWER



H=>B1 -iGPU PCH (UMA)  
L=>B0 -dGPU GPU (DIS)

<Core Design>

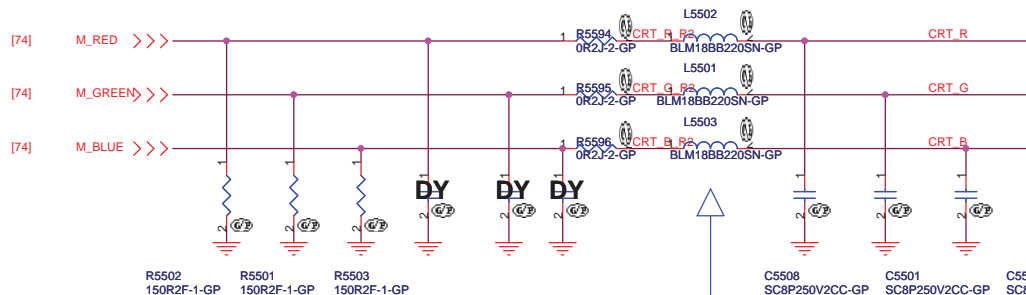
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Taipei Hsien 221, Taiwan, R.O.C.

| Title                  |                          |        | Rev |       |
|------------------------|--------------------------|--------|-----|-------|
| LCD/Inverter Connector |                          |        | X01 |       |
| Size                   | Document Number          | Custom |     |       |
| Vostro Calpella        |                          |        |     |       |
| Date:                  | Monday, January 18, 2010 | Sheet  | 54  | of 91 |

<http://laptop-motherboard-schematic.blogspot.com/>

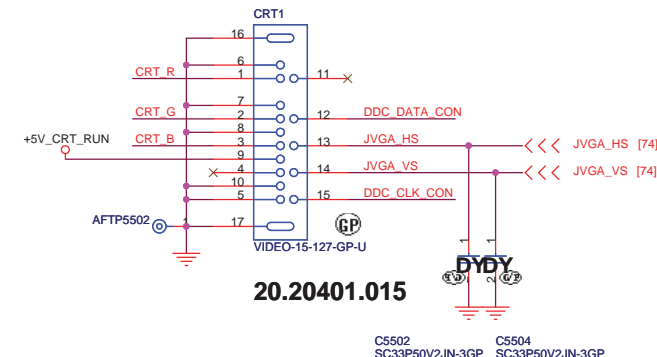
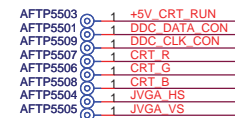
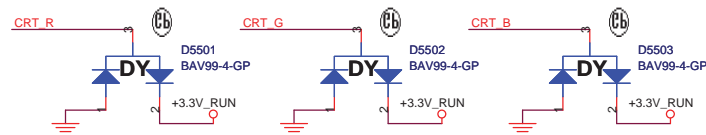
SSID = VIDEO

http://laptopblue.vn

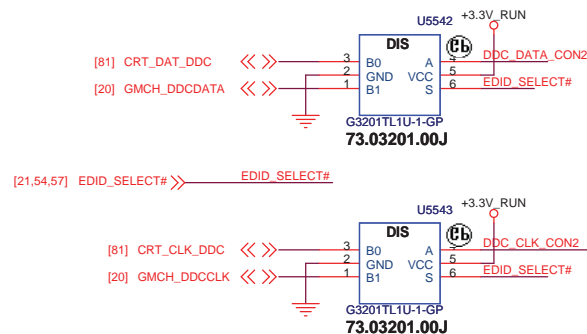
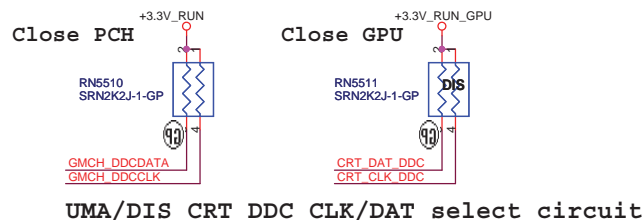


**Layout Note:**

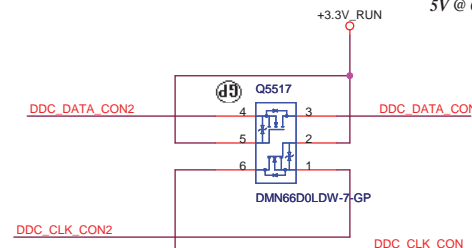
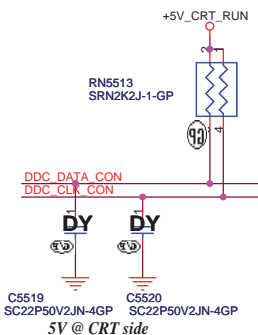
- \*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- \* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



20.20401.015



H=>B1 -iGPU PCH (UMA)  
L=>B0 -dGPU GPU (DIS)



<Core Design>

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| Title         |                          |                |
|---------------|--------------------------|----------------|
| CRT Connector |                          |                |
| Size          | Document Number          | Rev            |
| A3            | Vostro Calpella          | X01            |
| Date:         | Monday, January 18, 2010 | Sheet 55 of 91 |

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h t t p : / / l a p t o p b l u e . v n

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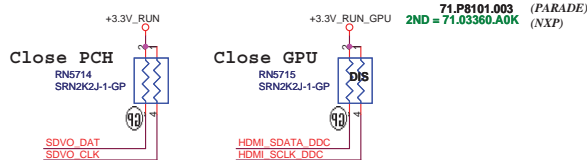
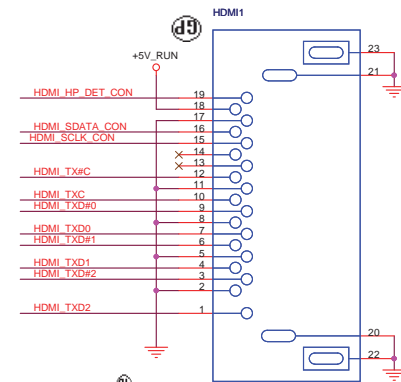
h t t p : / / l a p t o p - m o t h e r b o a r d - s c h e m a t i c . b l o g s p o t . c o m /

|                                                                                       |                                           |                                                                                                             |
|---------------------------------------------------------------------------------------|-------------------------------------------|-------------------------------------------------------------------------------------------------------------|
| <Core Design>                                                                         |                                           |                                                                                                             |
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| Title                                                                                 |                                           |                                                                                                             |
| (Reserve)                                                                             |                                           |                                                                                                             |
| Size<br>Custom                                                                        | Document Number<br><b>Vostro Calpella</b> | Rev<br><b>X01</b>                                                                                           |
| Date: Monday, January 18, 2010                                                        |                                           | Sheet 56 of 91                                                                                              |

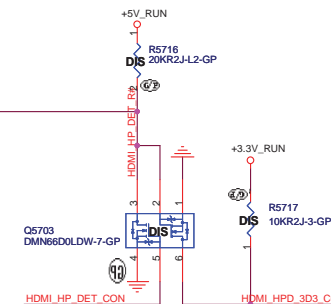




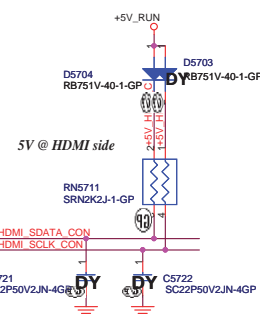
C5772 SCD1U10V2KX-4GP C5774 SCD1U10V2KX-4GP +3.3V\_RUN R5749 R5750 4K7R2J-2-GP 4K7R2J-2-GP +3.3V\_RUN

[illegible][illegible]

Close HDMI Connec

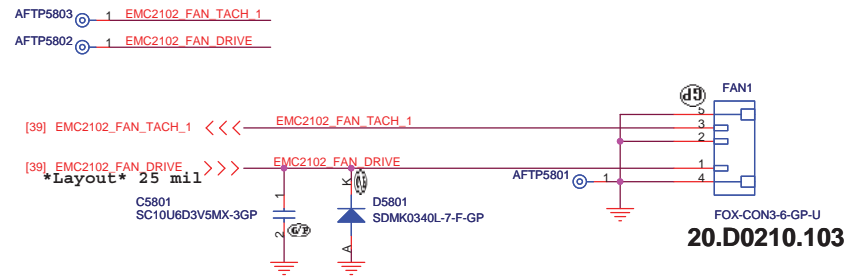


The schematic diagram illustrates the GPU selection circuit. It features a GPU chip (73.03201.00J) with pins B0, GND, B1, and B2. Pin B0 is connected to HDMI\_HPD\_DET\_VGA. Pin B1 is connected to HDMI\_HPD\_DET. Pin B2 is connected to EDID\_SELECT#. The chip is also connected to a +3.3V\_RUN supply. The circuit is labeled 'Close GPU' and 'Close PCH'.



SSID = Thermal

## Fan Connector



<Core Design>



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Title

**FAN**

Size  
A3

Document Number

**Vostro Calpella**

Rev

**X01**

Date: Monday, January 18, 2010

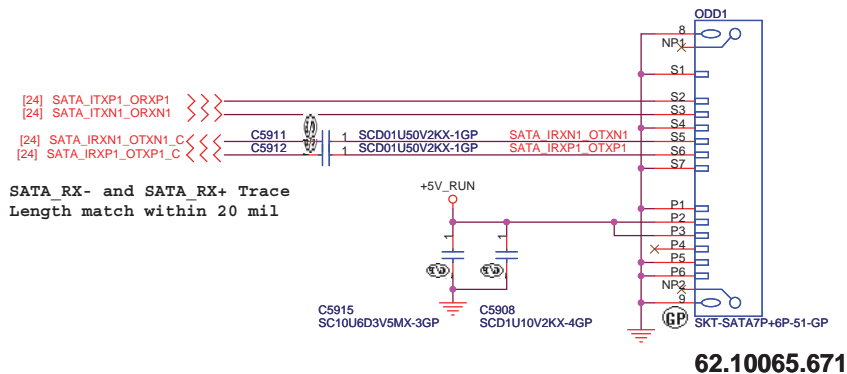
Sheet 58 of 91

SSID = SATA

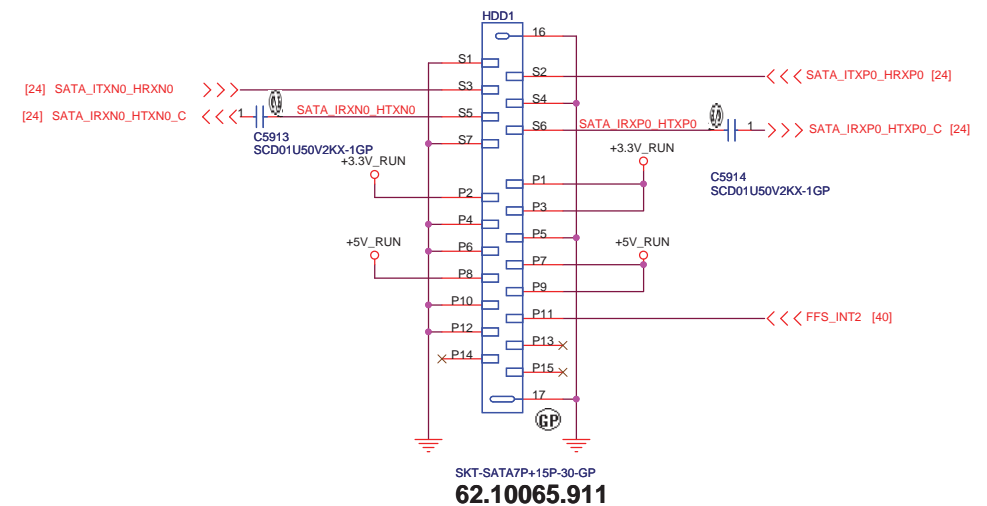
http://laptopblue.vn

SSID = SATA

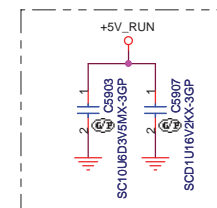
## ODD Connector



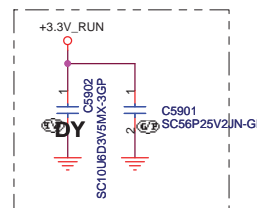
## SATA HDD Connector



Close to CONN  
5V power pin



Close to CONN  
3.3V power pin



<Core Design>



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| Title             |                          |                 | Rev      |
|-------------------|--------------------------|-----------------|----------|
| HDD/ODD Connector |                          |                 | X01      |
| Size              | Document Number          | Vostro Calpella |          |
| A3                |                          |                 |          |
| Date:             | Monday, January 18, 2010 | Sheet           | 59 of 91 |

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h t t p : / / l a p t o p b l u e . v n

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h t t p : / / l a p t o p - m o t h e r b o a r d - s c h e m a t i c . b l o g s p o t . c o m /

|                                                                                                                                                                                                   |                                           |                   |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|-------------------|
| <Core Design>                                                                                                                                                                                     |                                           |                   |
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| Title                                                                                                                                                                                             |                                           |                   |
| (Reserve)                                                                                                                                                                                         |                                           |                   |
| Size<br>Custom                                                                                                                                                                                    | Document Number<br><b>Vostro Calpella</b> | Rev<br><b>X01</b> |
| Date: Monday, January 18, 2010                                                                                                                                                                    |                                           |                   |
| Sheet 60 of 91                                                                                                                                                                                    |                                           |                   |

h t t p : / / l a p t o p b l u e . v n

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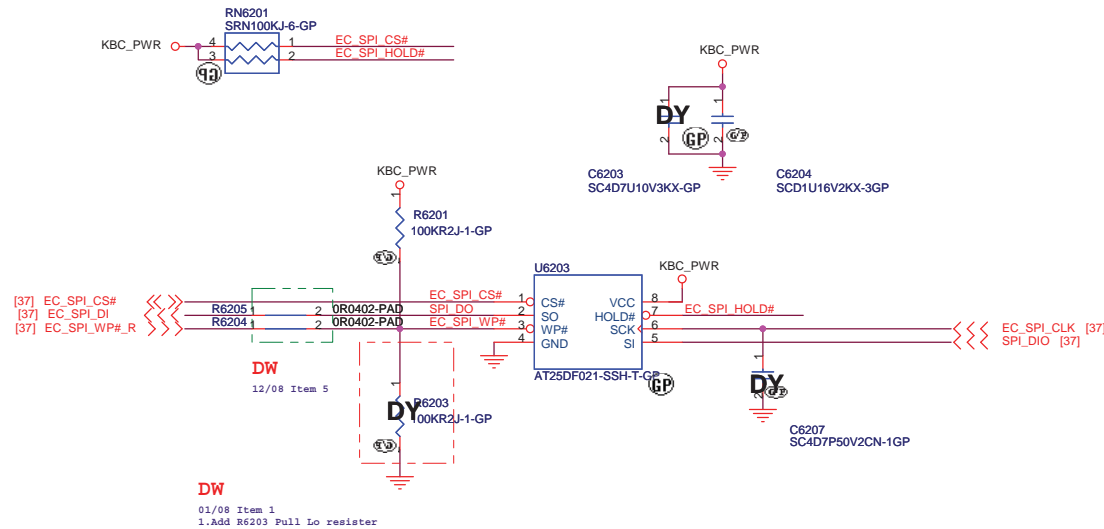
h t t p : / / l a p t o p - m o t h e r b o a r d - s c h e m a t i c . b l o g s p o t . c o m /

|                                                                                                                                                                                                   |                                           |                   |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|-------------------|
| <Core Design>                                                                                                                                                                                     |                                           |                   |
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| Title                                                                                                                                                                                             |                                           |                   |
| (Reserve)                                                                                                                                                                                         |                                           |                   |
| Size<br>Custom                                                                                                                                                                                    | Document Number<br><b>Vostro Calpella</b> | Rev<br><b>X01</b> |
| Date: Monday, January 18, 2010                                                                                                                                                                    |                                           |                   |
| Sheet 61 of 91                                                                                                                                                                                    |                                           |                   |

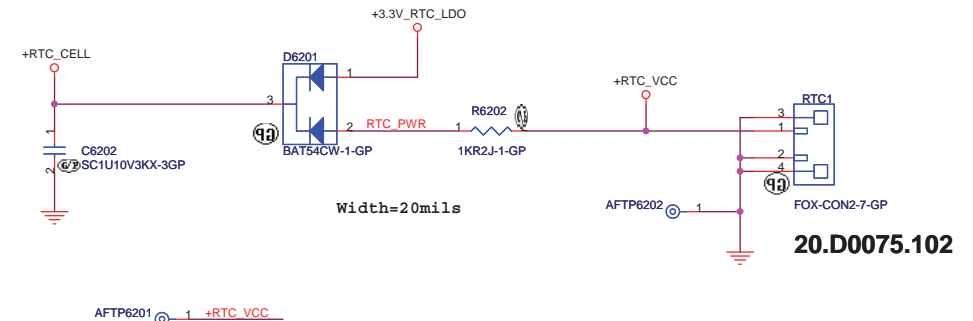
SSID = Flash.ROM

SSID = RBATT

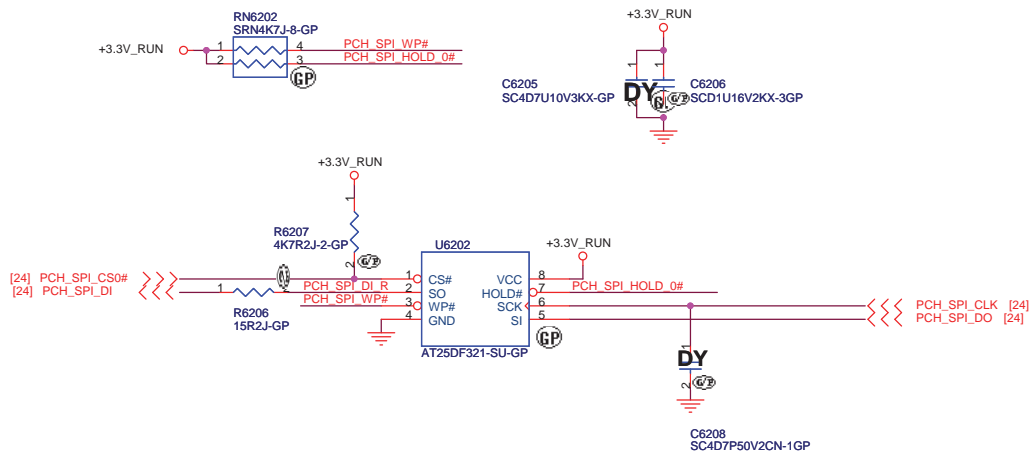
## SPI FLASH ROM (256K bytes) for KBC



## RTC Connector



## SPI FLASH ROM (4M bytes) for PCH

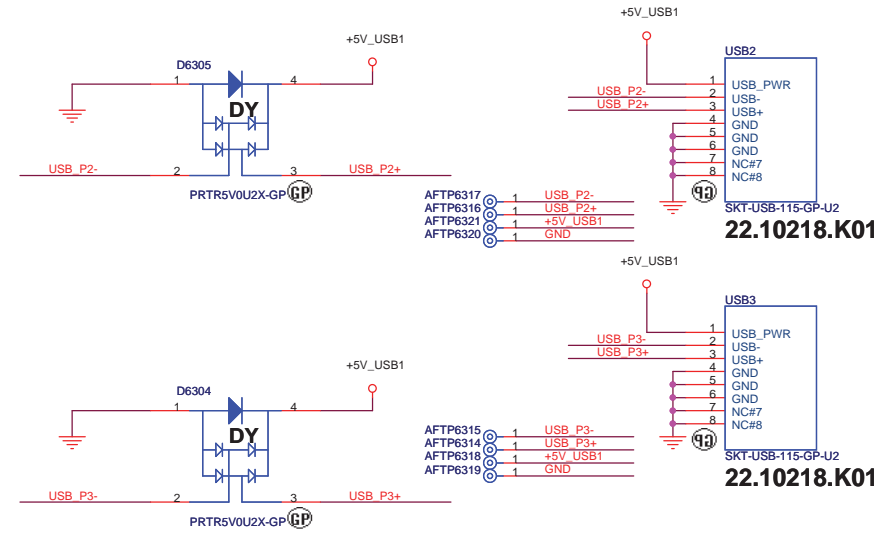
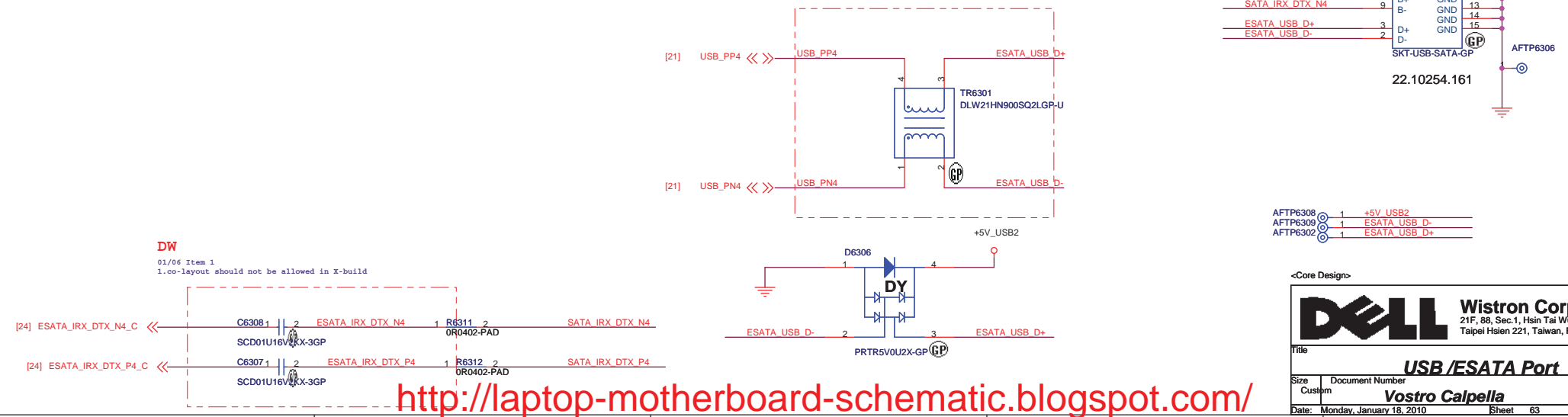


<Core Design>

|                                                                                       |                                           |                                                                                                             |                   |
|---------------------------------------------------------------------------------------|-------------------------------------------|-------------------------------------------------------------------------------------------------------------|-------------------|
|  |                                           | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                   |
| Title                                                                                 |                                           |                                                                                                             |                   |
| <b>EEPROM/RTC Connector</b>                                                           |                                           |                                                                                                             |                   |
| Size<br>A3                                                                            | Document Number<br><b>Vostro Calpella</b> |                                                                                                             | Rev<br><b>X01</b> |
| Date:                                                                                 | Monday, January 18, 2010                  | Sheet 62 of                                                                                                 | 91                |

<http://laptopblue.vn>

The schematic diagram illustrates the USB power management circuit. It features a 15V ALW input connected to a USB Type-C connector. The circuit includes a USB PWR\_EN# signal, a USB\_OC2\_3 signal, and a USB1 input. Key components include a TPS2062AD-GP (U6303) and a TC6303 (ST100U6D3V8ML1GP). The diagram also shows various capacitors and ground connections.

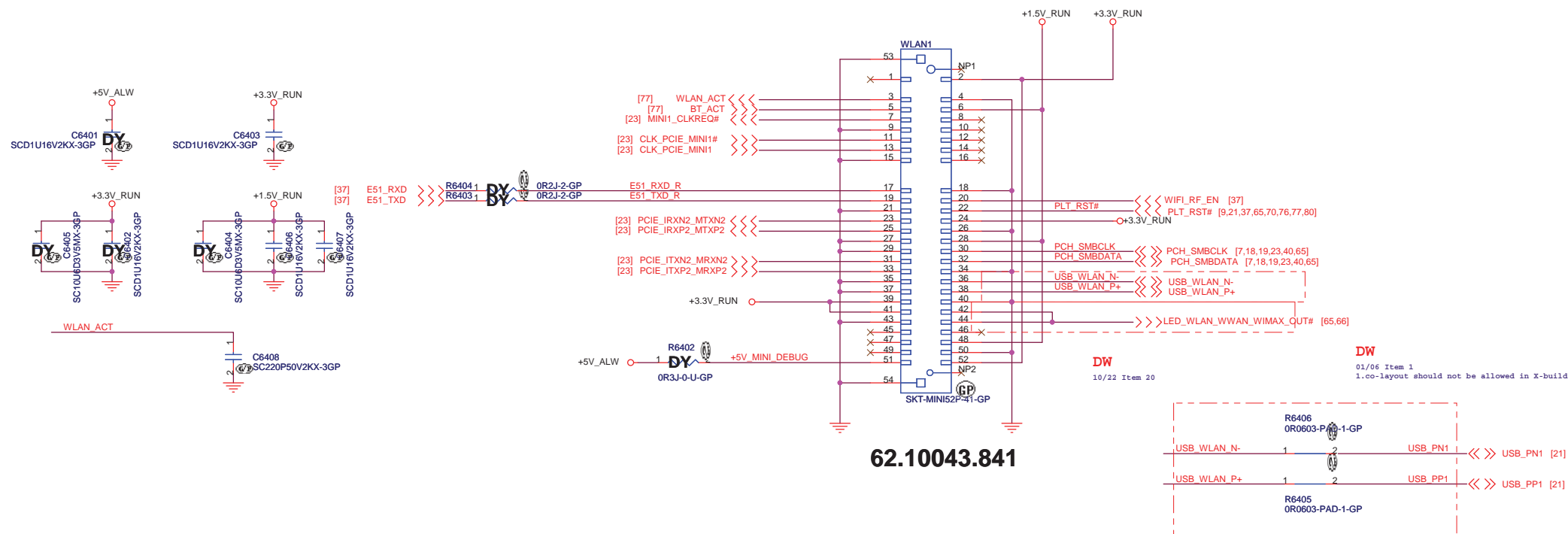
[illegible]

<http://laptop-motherboard-schematic.blogspot.com/>

SSID = Wireless

http://laptopblue.vn

## Mini Card Connector(802.11a/b/g/n)



DW  
01/06 Item 1  
1.co-layout should not be allowed in X-build

DW  
10/22 Item 20

<Core Design>



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Title

**MINICARD(WLAN)/ITP CONN**

Size

Document Number

**Vostro Calpella**

Rev

**X01**

Date: Monday, January 18, 2010

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91

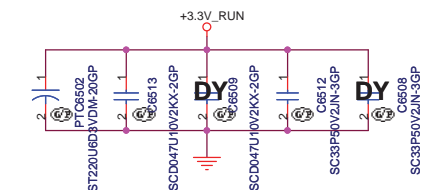
http://laptop-motherboard-schematic.blogspot.com/



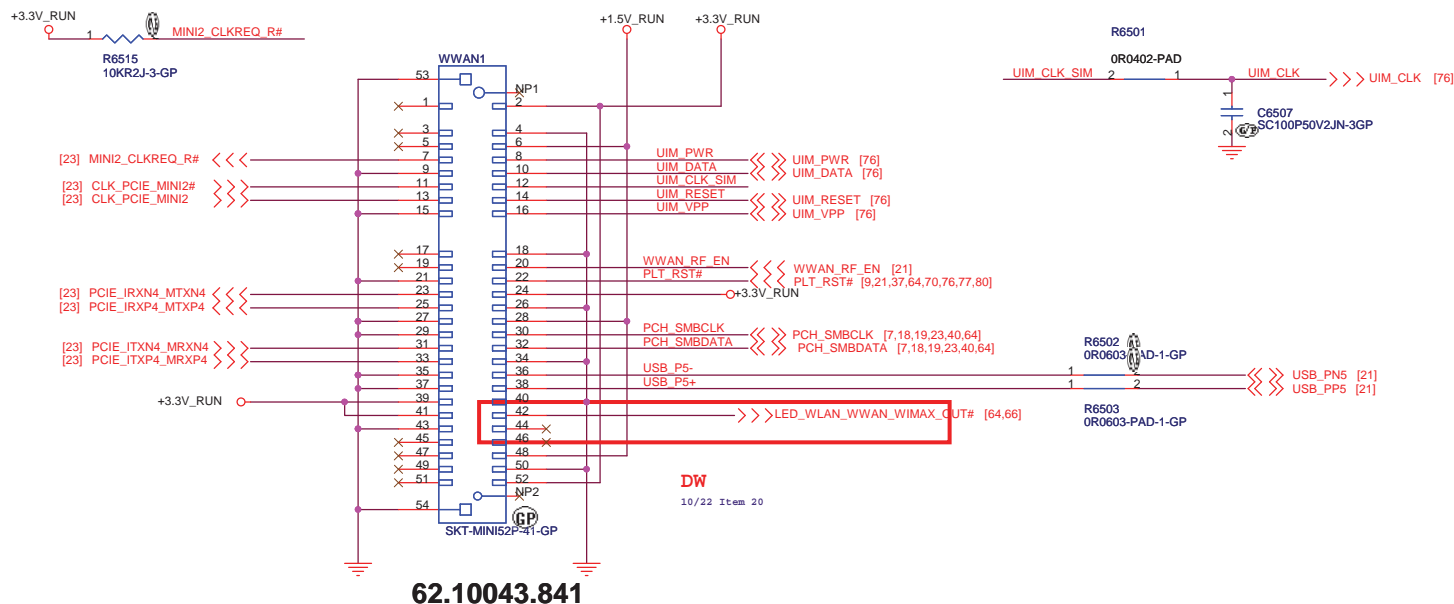
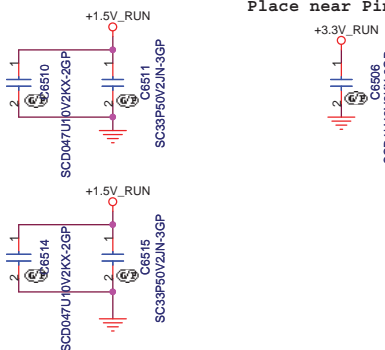
SSID = Wireless

http://laptopblue.vn  
Mini Card Connector(WWAN)

Place near MINI Card CONN



Place near Pin 24

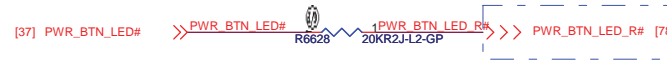


http://laptop-motherboard-schematic.blogspot.com/

## For LED & Capacity board:

| LED Type            | Color | Power rail |
|---------------------|-------|------------|
| SCRL LED            | White | ALW        |
| CAP LED             | White | ALW        |
| NUM LED             | White | ALW        |
| PWR BTN LED         | White | ALW        |
| SATA ACT LED1       | White | RUN        |
| BT ACT LED          | White | RUN        |
| WLAN WWAN WIMAX LED | White | RUN        |
|                     |       |            |

### PWR BTN LED



### For LED & Capacity board:

### SCRLK LED



### For LED & Capacity board:

### CAPS LED



### NUM LED



Remove BJT to daughter board

### Bluetooth LED

### For LED & Capacity board:



## For IO board

| LED Type     | Color              | Power rail |
|--------------|--------------------|------------|
| PWR LED2     | White(Multi-color) | ALW        |
| BATTERY LED2 | Amber(Multi-color) | ALW        |
|              | White(Multi-color) | ALW        |

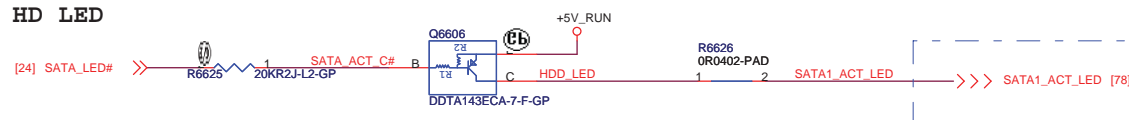
### WLAN WWAN WIMAX LED

DW  
10/22 Item 20



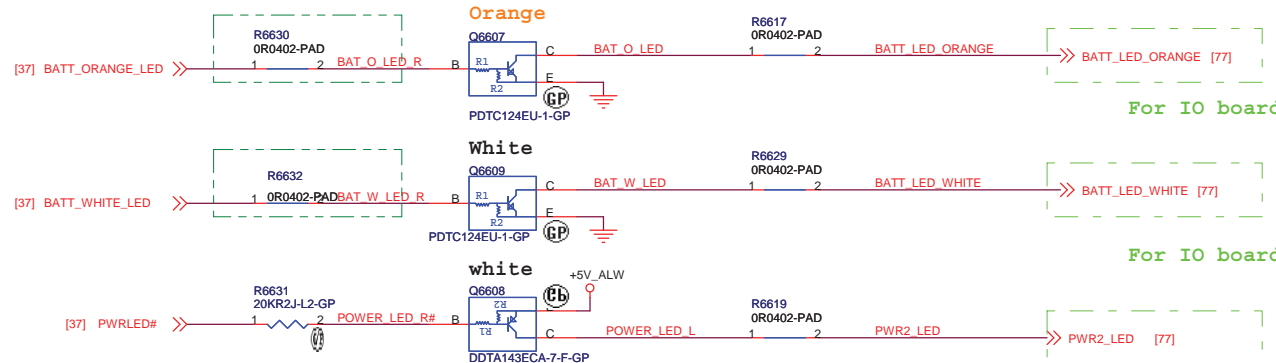
### For LED&Capacity board:

### HD LED



### Battery & Power LED

DW  
12/08 Item 5



For IO board

For IO board


For IO board

<Core Design>

h t t p : / / l a p t o p b l u e . v n

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h t t p : / / l a p t o p - m o t h e r b o a r d - s c h e m a t i c . b l o g s p o t . c o m /

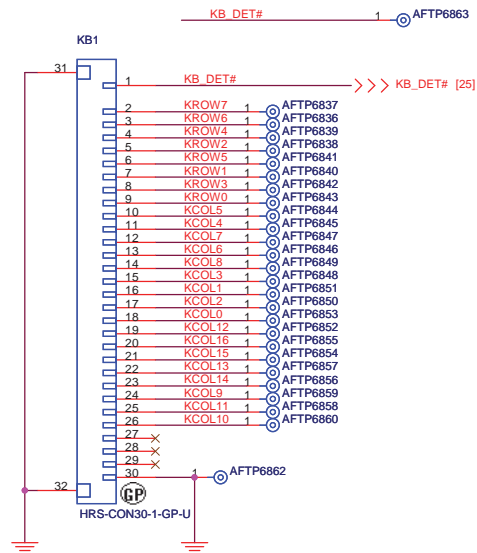
|                                                                                                                                                                                                   |                                           |                   |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|-------------------|
| <Core Design>                                                                                                                                                                                     |                                           |                   |
|  <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                                           |                   |
| Title                                                                                                                                                                                             |                                           |                   |
| (Reserve)                                                                                                                                                                                         |                                           |                   |
| Size<br>Custom                                                                                                                                                                                    | Document Number<br><b>Vostro Calpella</b> | Rev<br><b>X01</b> |
| Date: Monday, January 18, 2010                                                                                                                                                                    |                                           |                   |
| Sheet 67 of 91                                                                                                                                                                                    |                                           |                   |

SSID = KBC

http://laptopblue.vn

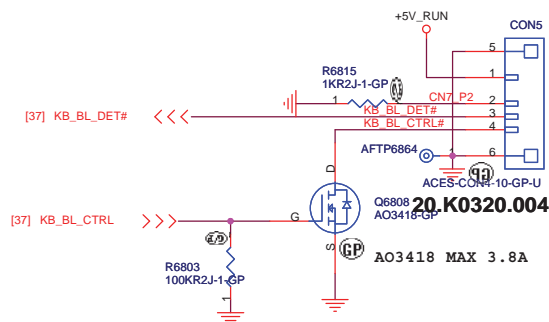
SSID = Touch.Pad

### Internal Keyboard Connector



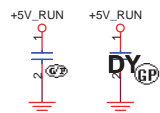
20.K0259.030

### KB Backlight CONN



20.K0320.004

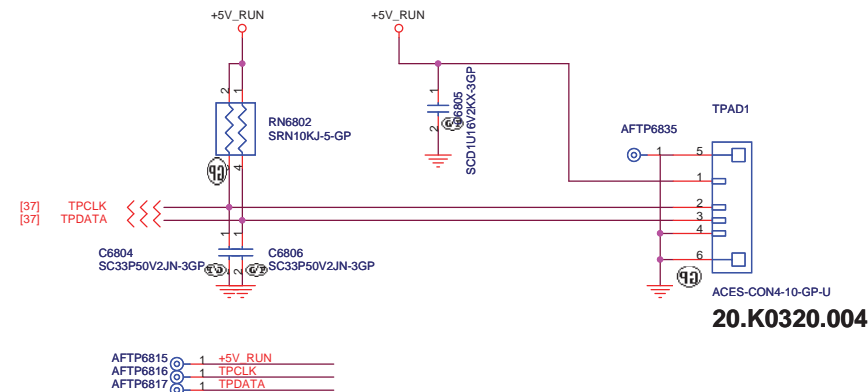
AFTP6833 1 +5V\_RUN  
AFTP6832 1 CN7 P2  
AFTP6834 1 KB\_BL\_DET#  
AFTP6861 1 KB\_BL\_CTRL#



C6812 SCD1U25V2ZY-1GP C6895 SC4D7U10V5KX-1GP

Place near CON5

### TouchPad Connector



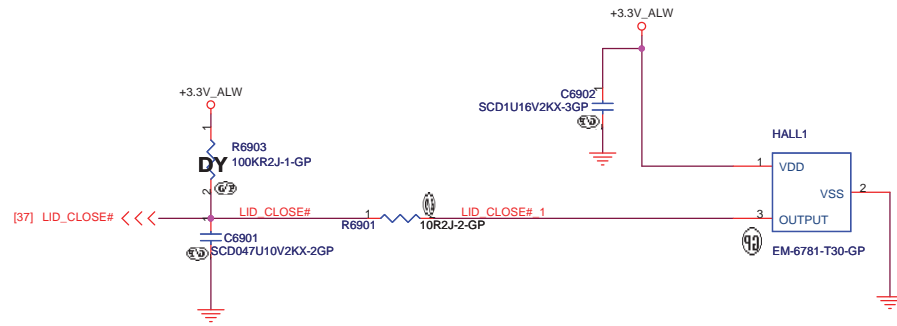
AFTP6815 1 +5V\_RUN  
AFTP6816 1 TPCLK  
AFTP6817 1 TPDATA

<Core Design>

|                                                                                                                  |                                           |                   |
|------------------------------------------------------------------------------------------------------------------|-------------------------------------------|-------------------|
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| Title<br><b>Keyboard/Touch Pad</b>                                                                               |                                           |                   |
| Size<br>Custom                                                                                                   | Document Number<br><b>Vostro Calpella</b> | Rev<br><b>X01</b> |
| Date: Monday, January 18, 2010 Sheet 68 of 91                                                                    |                                           |                   |

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## Hall Sensor Connector

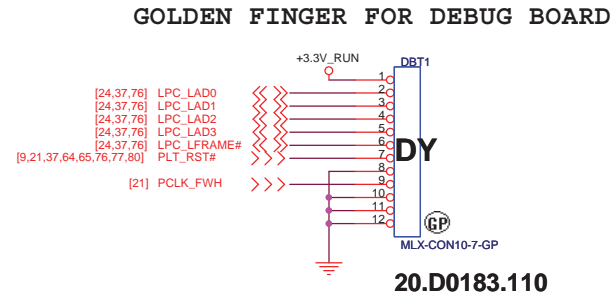


<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

|        |                          |            |                    |       |
|--------|--------------------------|------------|--------------------|-------|
| Title  |                          |            | <b>Hall sensor</b> |       |
| Size   | Document Number          | Rev        |                    |       |
| Custom | <b>Vostro Calpella</b>   | <b>X01</b> |                    |       |
| Date:  | Monday, January 18, 2010 | Sheet      | 69                 | of 91 |



h t t p : / / l a p t o p b l u e . v n

(Blank)

h t t p : / / l a p t o p - m o t h e r b o a r d - s c h e m a t i c . b l o g s p o t . c o m /

|                                                                                                      |                                           |                   |
|------------------------------------------------------------------------------------------------------|-------------------------------------------|-------------------|
| <Core Design>                                                                                        |                                           |                   |
|                 |                                           |                   |
| Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                                           |                   |
| Title                                                                                                |                                           |                   |
| (Reserve)                                                                                            |                                           |                   |
| Size<br>Custom                                                                                       | Document Number<br><b>Vostro Calpella</b> | Rev<br><b>X01</b> |
| Date: Monday, January 18, 2010                                                                       |                                           |                   |
| Sheet 71 of 91                                                                                       |                                           |                   |

h t t p : / / l a p t o p b l u e . v n

(Blank)

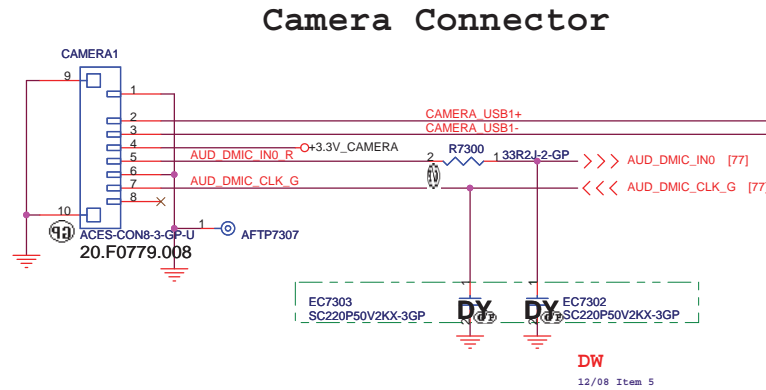
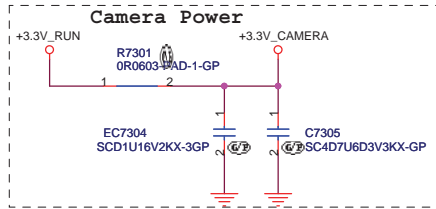
h t t p : / / l a p t o p - m o t h e r b o a r d - s c h e m a t i c . b l o g s p o t . c o m /

<Core Design>

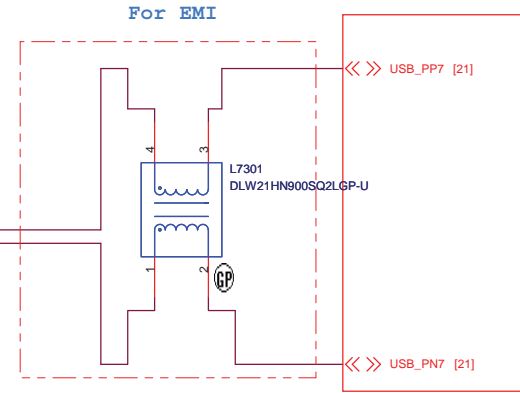
|                                                                                       |                 |                                                                                                             |       |
|---------------------------------------------------------------------------------------|-----------------|-------------------------------------------------------------------------------------------------------------|-------|
|  |                 | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |       |
| Title                                                                                 |                 |                                                                                                             |       |
| (Reserve)                                                                             |                 |                                                                                                             |       |
| Size                                                                                  | Document Number |                                                                                                             | Rev   |
| Custom                                                                                | Vostro Calpella |                                                                                                             | X01   |
| Date: Monday, January 18, 2010                                                        |                 | Sheet 72                                                                                                    | of 91 |



SSID = User.Interface



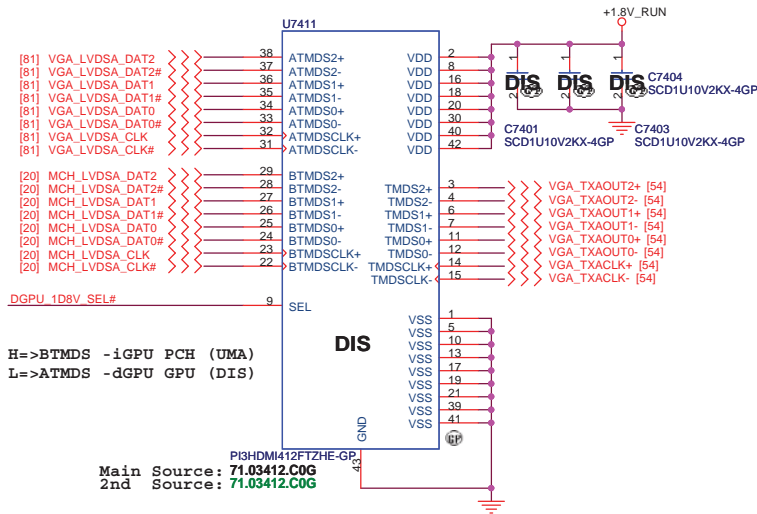
AFTP7303 1 AUD\_DMIC\_IN0\_R  
AFTP7304 1 +3.3V\_CAMERA  
AFTP7305 1 CAMERA\_USB1-  
AFTP7306 1 CAMERA\_USB1+



DW  
01/06 Item 1  
1.co-layout should not be allowed in X-build

DW  
01/18 Item 1

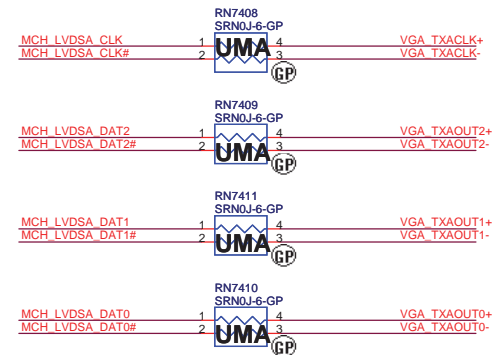
## UMA/DIS LVDS signal select circuit



FUNCTION TABLE

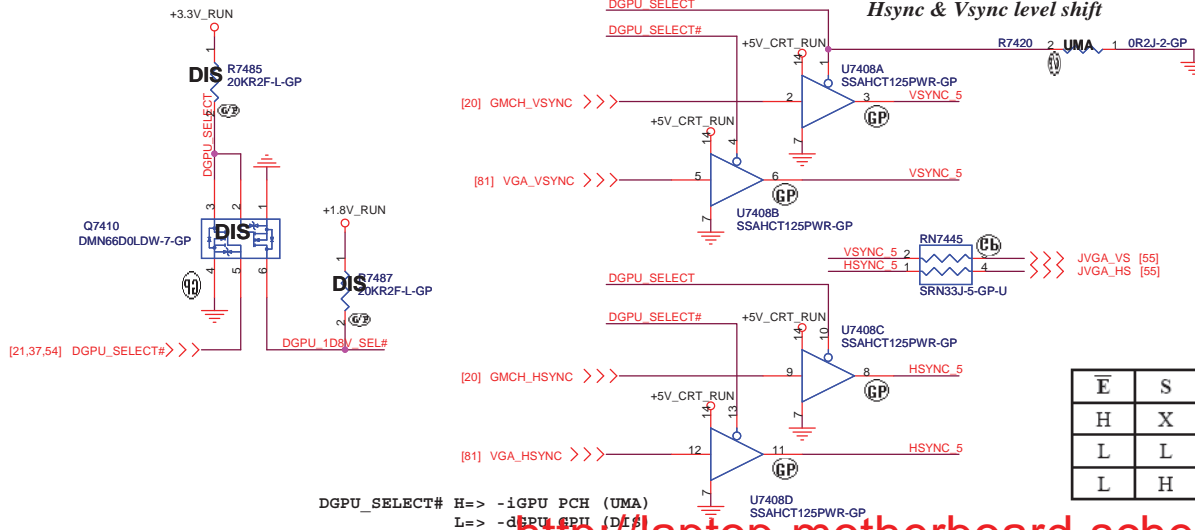
| SEL | FUNCTION                                                                                                                                                                                                 | OUTPUT                                   |
|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|
| L   | TMDSn+ = ATMDSn+<br>TMDSn- = ATMDSn-<br>TMDSCLK+ = ATMDSCLK+<br>TMDSCLK- = ATMDSCLK-<br>BTMDSn+ = High Impedance<br>BTMDSn- = High Impedance<br>BTMDSCLK+ = High Impedance<br>BTMDSCLK- = High Impedance | TMDSn+<br>TMDSn-<br>TMDSCLK+<br>TMDSCLK- |
| H   | TMDSn+ = BTMDSn+<br>TMDSn- = BTMDSn-<br>TMDSCLK+ = BTMDSCLK+<br>TMDSCLK- = BTMDSCLK-<br>ATMDSn+ = High Impedance<br>ATMDSn- = High Impedance<br>ATMDSCLK+ = High Impedance<br>ATMDSCLK- = High Impedance | TMDSn+<br>TMDSn-<br>TMDSCLK+<br>TMDSCLK- |

## UMA LVDS signal circuit

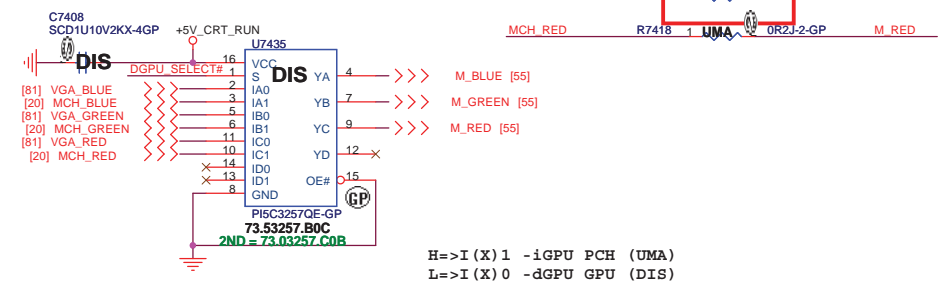


DW  
10/23 Item 25

## UMA/DIS CRT Hsync/Vsync select circuit Hsync & Vsync level shift



## UMA/DIS CRT signal select circuit



| E | S | YA   | YB   | YC   | YD   | Function |
|---|---|------|------|------|------|----------|
| H | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Disable  |
| L | L | IA0  | IB0  | IC0  | ID0  | S = 0    |
| L | H | IA1  | IB1  | IC1  | ID1  | S = 1    |

<Core Design>


|                                                                                                             |                                        |                |
|-------------------------------------------------------------------------------------------------------------|----------------------------------------|----------------|
| <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                                        |                |
| Title <b>Swith-1</b>                                                                                        |                                        |                |
| Size Custom                                                                                                 | Document Number <b>Vostro Calpella</b> | Rev <b>X01</b> |
| Date: Monday, January 18, 2010                                                                              | Sheet 74 of 91                         |                |

h t t p : / / l a p t o p b l u e . v n

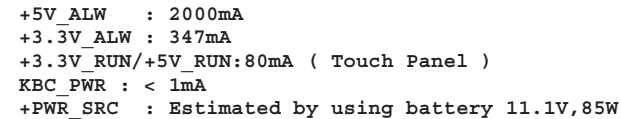
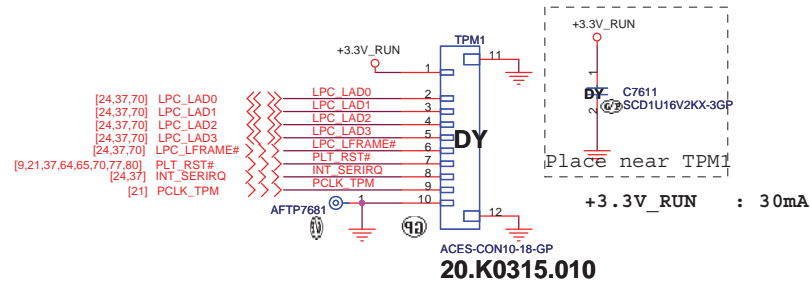
(Blank)

h t t p : / / l a p t o p - m o t h e r b o a r d - s c h e m a t i c . b l o g s p o t . c o m /

<Core Design>

|                                                                                       |                                           |                                                                                                             |                   |
|---------------------------------------------------------------------------------------|-------------------------------------------|-------------------------------------------------------------------------------------------------------------|-------------------|
|  |                                           | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                   |
| Title                                                                                 |                                           |                                                                                                             |                   |
| <b>Reserve</b>                                                                        |                                           |                                                                                                             |                   |
| Size<br>A3                                                                            | Document Number<br><b>Vostro Calpella</b> |                                                                                                             | Rev<br><b>X01</b> |
| Date: Monday, January 18, 2010                                                        |                                           | Sheet 75 of 91                                                                                              |                   |

Place near CON1

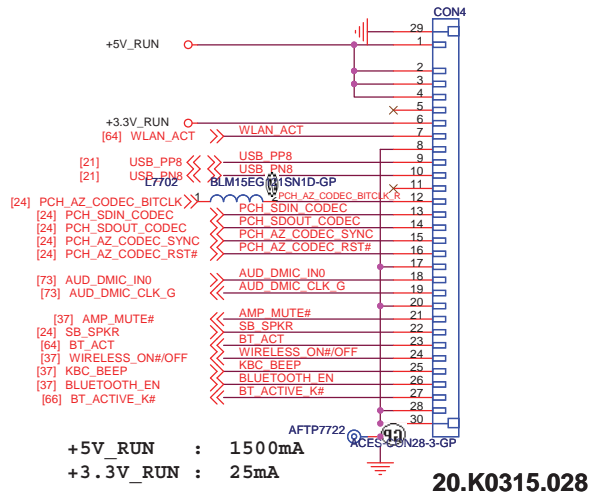


|                                                                                       |                               |                                                                                                             |                   |
|---------------------------------------------------------------------------------------|-------------------------------|-------------------------------------------------------------------------------------------------------------|-------------------|
|  |                               | <b>Wistron Corporation</b><br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |                   |
| Title <b><i>DC_IN/TPM board CON</i></b>                                               |                               |                                                                                                             |                   |
| Size                                                                                  | Document Number               |                                                                                                             | Rev               |
| Custom                                                                                | <b><i>Vostro Calpella</i></b> |                                                                                                             | <b><i>X01</i></b> |
| Date:                                                                                 | Monday, January 18, 2010      | Sheet 76 of                                                                                                 | 91                |

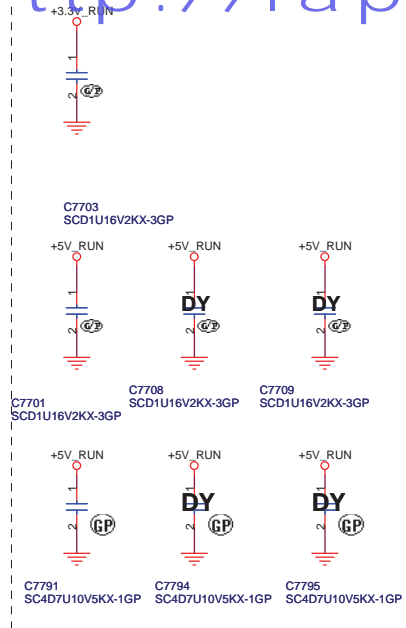
<http://laptop-motherboard-schematic.blogspot.com/>

SSID = User.Interface

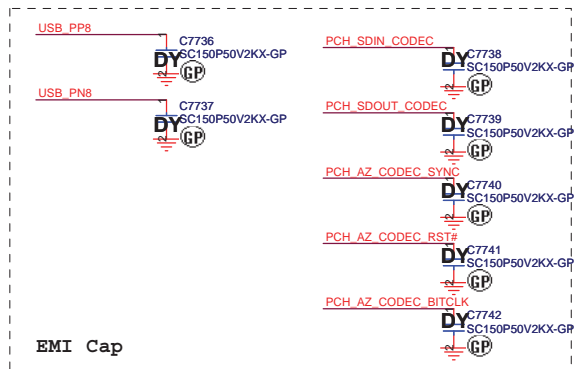
## Audio board CON



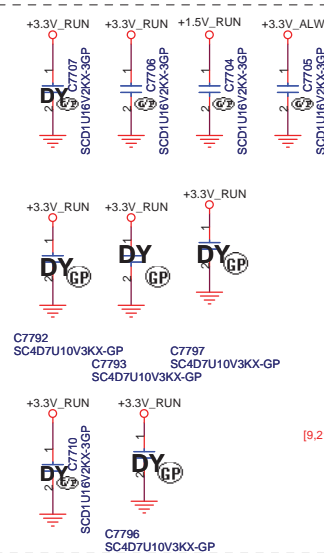
Place near CON4



|          |   |                       |
|----------|---|-----------------------|
| AFTP7710 | 1 | +5V_RUN               |
| AFTP7706 | 1 | +3.3V_RUN             |
| AFTP7709 | 1 | WIRELESS_ON#/OFF      |
| AFTP7702 | 1 | WLAN_ACT              |
| AFTP7703 | 1 | BLUETOOTH_EN          |
| AFTP7704 | 1 | BT_ACTIVE_K#          |
| AFTP7705 | 1 | BT_ACT                |
| AFTP7707 | 1 | USB_PP8               |
| AFTP7708 | 1 | USB_PN8               |
| AFTP7712 | 1 | PCH_AZ_CODEC_BITCLK_R |
| AFTP7713 | 1 | PCH_SDIN_CODEC        |
| AFTP7714 | 1 | PCH_SDOUT_CODEC       |
| AFTP7715 | 1 | PCH_AZ_CODEC_SYNC     |
| AFTP7716 | 1 | PCH_AZ_CODEC_RST#     |
| AFTP7718 | 1 | SB_SPKR               |
| AFTP7719 | 1 | KBC_BEEP              |
| AFTP7720 | 1 | AUD_DMIC_IN0          |
| AFTP7721 | 1 | AUD_DMIC_CLK_G        |
| AFTP7723 | 1 | AMP_MUTE#             |

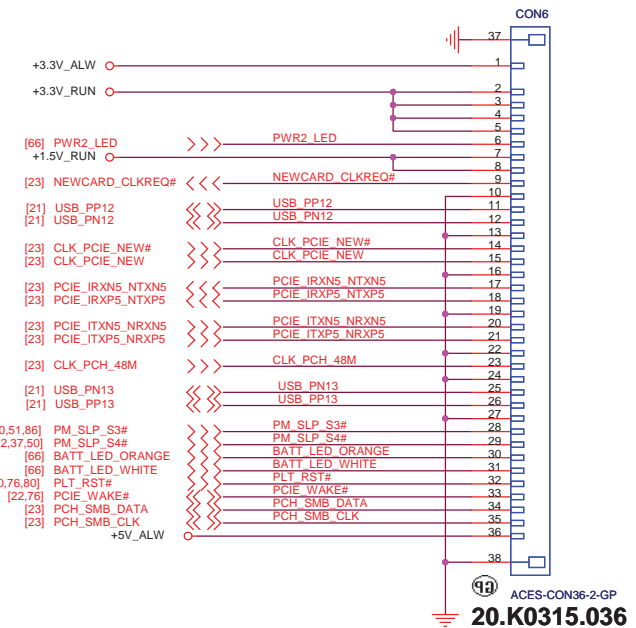


## Place near CON6



|          |   |                  |
|----------|---|------------------|
| AFTP7758 | 1 | +3.3V_ALW        |
| AFTP7757 | 1 | +3.3V_RUN        |
| AFTP7760 | 1 | +1.5V_RUN        |
| AFTP7762 | 1 | USB_PN12         |
| AFTP7759 | 1 | USB_PP12         |
| AFTP7769 | 1 | NEWCARD_CLKREQ#  |
| AFTP7768 | 1 | PCH_SMB_CLK      |
| AFTP7767 | 1 | PCH_SMB_DATA     |
| AFTP7777 | 1 | PM_SLP_S3#       |
| AFTP7776 | 1 | PM_SLP_S4#       |
| AFTP7773 | 1 | BATT_LED_ORANGE  |
| AFTP7772 | 1 | PWR2_LED         |
| AFTP7781 | 1 | PLT_RST#         |
| AFTP7785 | 1 | BATT_LED_WHITE   |
| AFTP7787 | 1 | +5V_ALW          |
| AFTP7771 | 1 | CLK_PCIE_NEW#    |
| AFTP7770 | 1 | CLK_PCIE_NEW     |
| AFTP7761 | 1 | PCIE_IRXN5_NTXN5 |
| AFTP7765 | 1 | PCIE_IRXP5_NTXP5 |
| AFTP7764 | 1 | PCIE_ITXN5_NRXN5 |
| AFTP7763 | 1 | PCIE_ITXP5_NRXP5 |
| AFTP7775 | 1 | USB_PN13         |
| AFTP7766 | 1 | USB_PP13         |
| AFTP7774 | 1 | PCIE_WAKE#       |
| AFTP7778 | 1 | CLK_PCH_48M      |

## IO board CON



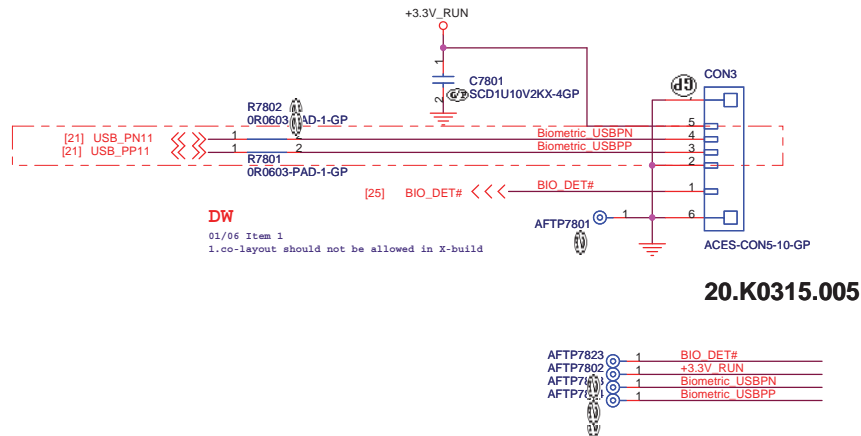
+1.5V\_RUN : 650mA  
+3.3V\_RUN : 1775mA  
+3.3V\_ALW : 275mA  
+5V\_ALW : 60mA

<http://laptop-motherboard-schematic.blogspot.com/>

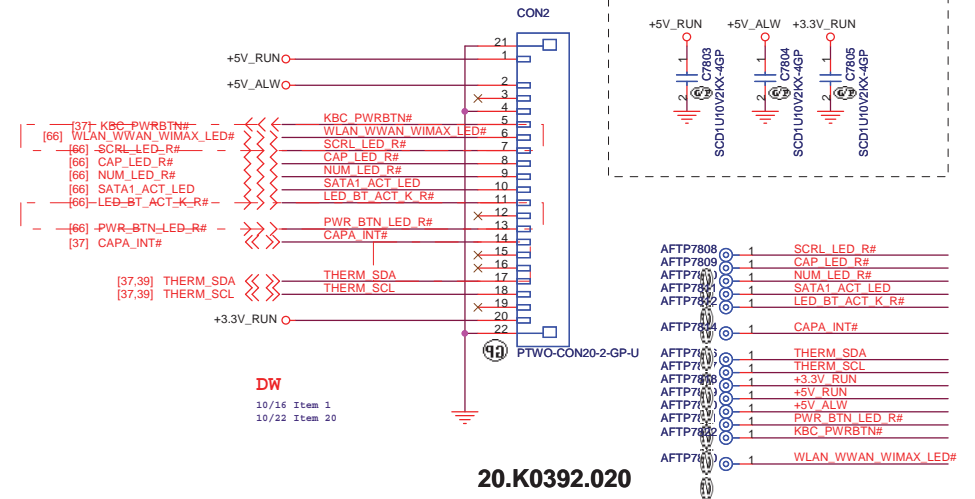
<Core Design>

|                                                                            |                                  |                            |            |
|----------------------------------------------------------------------------|----------------------------------|----------------------------|------------|
| <b>DELL</b>                                                                |                                  | <b>Wistron Corporation</b> |            |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |                                  |                            |            |
| Title <b>Audio BD/IO BD CONN</b>                                           |                                  |                            |            |
| Size                                                                       | Document Number                  | Rev                        |            |
| Custom                                                                     | <b>Vostro Montevina Discrete</b> |                            | <b>X01</b> |
| Date: Monday, January 18, 2010                                             | Sheet 77                         | of                         | 91         |

## Finger Printer Connector

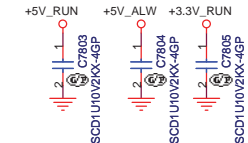


## LED&Capacity board CONN



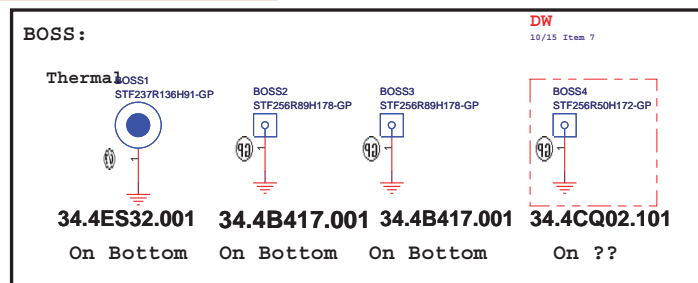
+3.3V\_RUN : 3.5mA  
+5V\_RUN : 240mA  
+5V\_ALW : 80mA

### Close to CON2

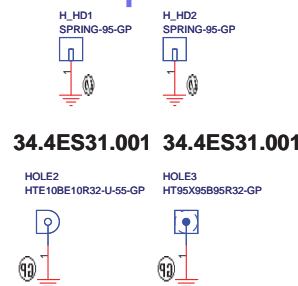


<Core Design>

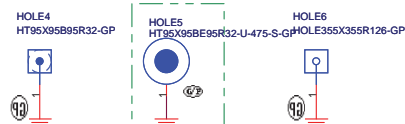
SSID = Mechanical



HOLE:



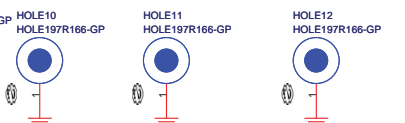
ZZ.00PAD.I71 ZZ.00PAD.K81 ZZ.00PAD.N81



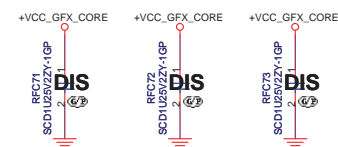
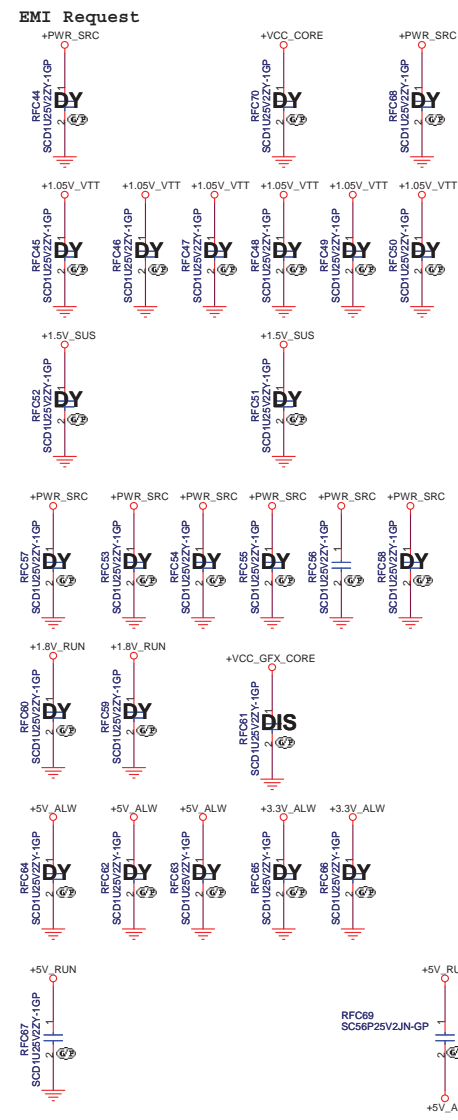
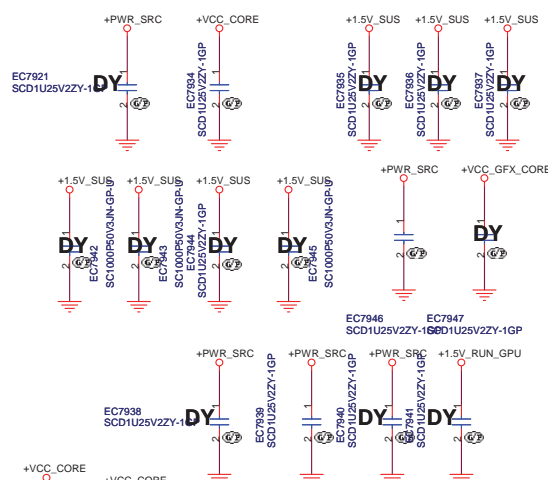
ZZ.00PAD.N81 ZZ.00PAD.Q41 ZZ.00PAD.I71



ZZ.00PAD.I71 ZZ.00PAD.N91 ZZ.00PAD.J01



34.4EM01.001 34.4EM01.001 34.4EM01.001



<http://laptopblue.vn>

PCIE\_MTX\_GRX\_N[0..15] << PCIE\_MTX\_GRX\_N[0..15] [8]

PCIE\_MRX\_GTX\_N[0..15] >> PCIE\_MRX\_GTX\_N[0..15] [8]



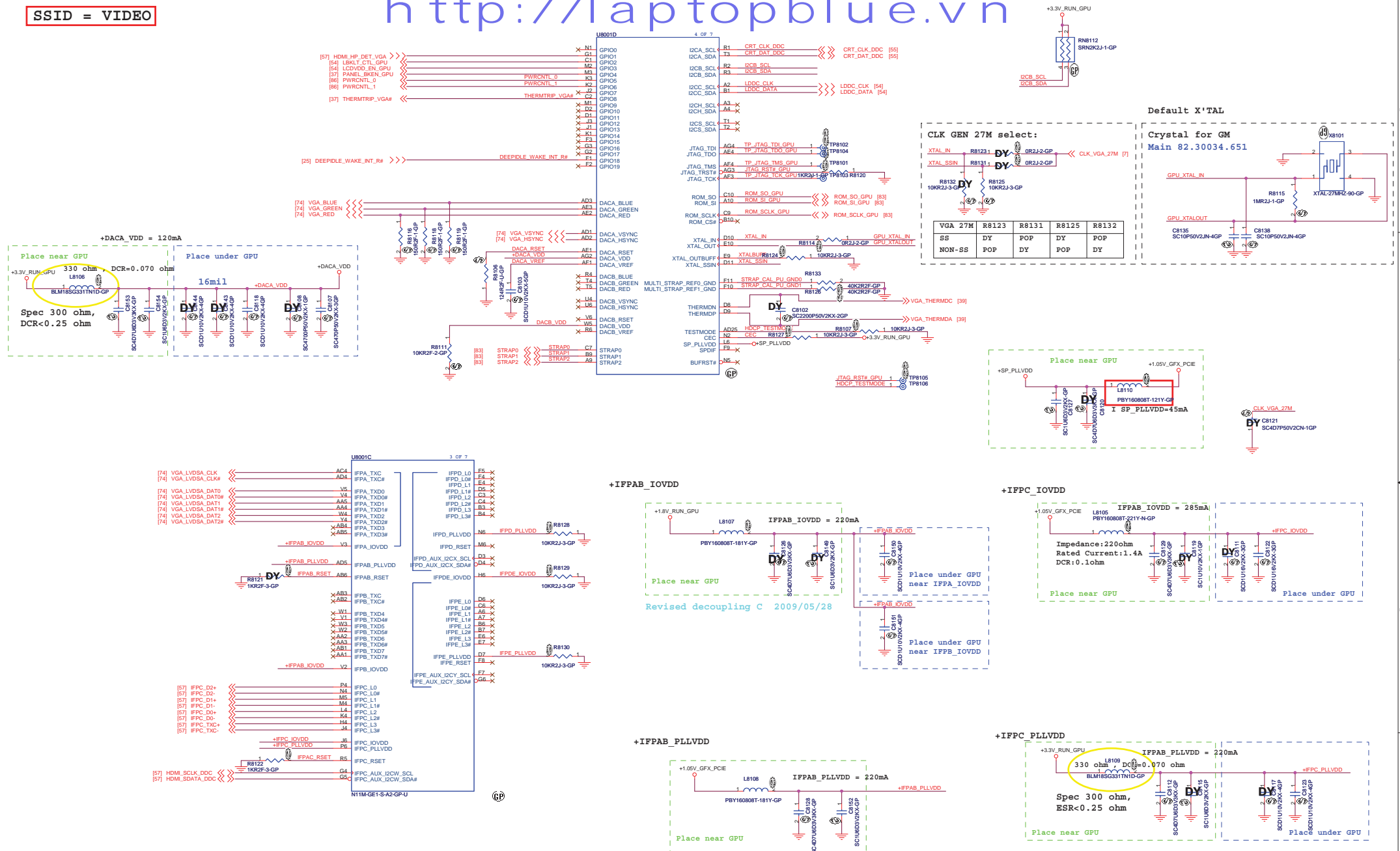
|                           |                          |             |            |
|---------------------------|--------------------------|-------------|------------|
| Title                     |                          |             |            |
| <b>VGA-PCIE/LVDS(1/4)</b> |                          |             |            |
| Size<br>A3                | Document Number          |             | Rev        |
|                           | <b>Vostro Calpella</b>   |             | <b>X01</b> |
| Date:                     | Monday, January 18, 2010 | Sheet 80 of | 91         |

<http://laptop-motherboard-schematic.blogspot.com/>



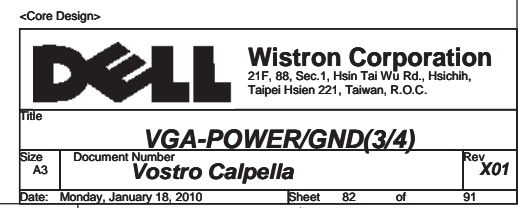
```
SSID = VIDEO
```

<http://laptopblue.vn>



<http://laptop-motherboard-schematic.blogspot.com/>

<http://laptopblue.vn>



<http://laptop-motherboard-schematic.blogspot.com/>

SSID = VIDEO

http://laptopblue.vn

Strap pin resistor need use 1% resistor (NV Design Guide)

+3.3V\_RUN\_GPU

[84,85] MDA[0..63] <<

U8001A

1 OF 7

MDA0 D22 FBA\_D0  
MDA1 E24 FBA\_D1  
MDA2 E22 FBA\_D2  
MDA3 D26 FBA\_D3  
MDA4 D27 FBA\_D4  
MDA5 C27 FBA\_D5  
MDA6 C27 FBA\_D6  
MDA7 B27 FBA\_D7  
MDA8 A21 FBA\_D8  
MDA9 C21 FBA\_D9  
MDA10 C21 FBA\_D10  
MDA11 C19 FBA\_D11  
MDA12 C18 FBA\_D12  
MDA13 D18 FBA\_D13  
MDA14 B18 FBA\_D14  
MDA15 C16 FBA\_D15  
MDA16 E21 FBA\_D16  
MDA17 E21 FBA\_D17  
MDA18 D20 FBA\_D18  
MDA19 F20 FBA\_D19  
MDA20 D17 FBA\_D20  
MDA21 F18 FBA\_D21  
MDA22 D16 FBA\_D22  
MDA23 E16 FBA\_D23  
MDA24 A22 FBA\_D24  
MDA25 C24 FBA\_D25  
MDA26 D21 FBA\_D26  
MDA27 B22 FBA\_D27  
MDA28 C22 FBA\_D28  
MDA29 A25 FBA\_D29  
MDA30 B25 FBA\_D30  
MDA31 A26 FBA\_D31  
MDA32 U24 FBA\_D32  
MDA33 V24 FBA\_D33  
MDA34 D24 FBA\_D34  
MDA35 R24 FBA\_D35  
MDA36 T23 FBA\_D36  
MDA37 R23 FBA\_D37  
MDA38 P24 FBA\_D38  
MDA39 P22 FBA\_D39  
MDA40 AC24 FBA\_D40  
MDA41 AB24 FBA\_D41  
MDA42 AB24 FBA\_D42  
MDA43 W24 FBA\_D43  
MDA44 AA22 FBA\_D44  
MDA45 W23 FBA\_D45  
MDA46 W22 FBA\_D46  
MDA47 V22 FBA\_D47  
MDA48 AA25 FBA\_D48  
MDA49 W27 FBA\_D49  
MDA50 W26 FBA\_D50  
MDA51 W25 FBA\_D51  
MDA52 AB25 FBA\_D52  
MDA53 AB26 FBA\_D53  
MDA54 AD26 FBA\_D54  
MDA55 AD27 FBA\_D55  
MDA56 V25 FBA\_D56  
MDA57 R25 FBA\_D57  
MDA58 V26 FBA\_D58  
MDA59 V27 FBA\_D59  
MDA60 R26 FBA\_D60  
MDA61 T25 FBA\_D61  
MDA62 N25 FBA\_D62  
MDA63 N26 FBA\_D63

F26 FBA\_CMD\_0 <<< FBA\_CMD\_0 [84]  
J24 RAS# [84,85]  
F25 FBA\_CMD\_2 <<< FBA\_CMD\_2 [84]  
M23 BA1 [84,85]  
N27 FBA\_CMD\_4 <<< FBA\_CMD\_4 [85]  
M27 FBA\_CMD\_5 <<< FBA\_CMD\_5 [85]  
K26 FBA\_CMD\_6 <<< FBA\_CMD\_6 [85]  
J25 FBA\_CMD\_7 <<< FBA\_CMD\_7 [85]  
J27 FBA\_CMD\_8 <<< FBA\_CMD\_8 [85]  
G23 MAA11 [84,85]  
G26 CAS# [84,85]  
J23 WE# [84,85]  
M25 BA0 [84,85]  
K27 FBA\_CMD\_13 <<< FBA\_CMD\_13 [85]  
G25 MAA12 [84,85]  
L24 MEM\_RST [84,85]  
K24 MAA7 [84,85]  
K24 MAA10 [84,85]  
G22 FBA\_CMD\_18 <<< FBA\_CMD\_18 [84]  
K25 MAA0 [84,85]  
H22 MAA9 [84,85]  
M26 MAA8 [84,85]  
H24 FBA\_CMD\_22 <<< FBA\_CMD\_22 [84]  
F27 MAA8 [84,85]  
J26 FBA\_CMD\_24 <<< FBA\_CMD\_24 [84]  
G24 MAA1 [84,85]  
G27 MAA13 [84,85]  
M24 BA2 [84,85]  
K22 FBA\_CMD\_28 <<< FBA\_CMD\_28 [85]  
J22 FBA\_CMD\_29 <<< FBA\_CMD\_29 [84]  
L22 FBA\_CMD\_30 <<< FBA\_CMD\_30 [84]

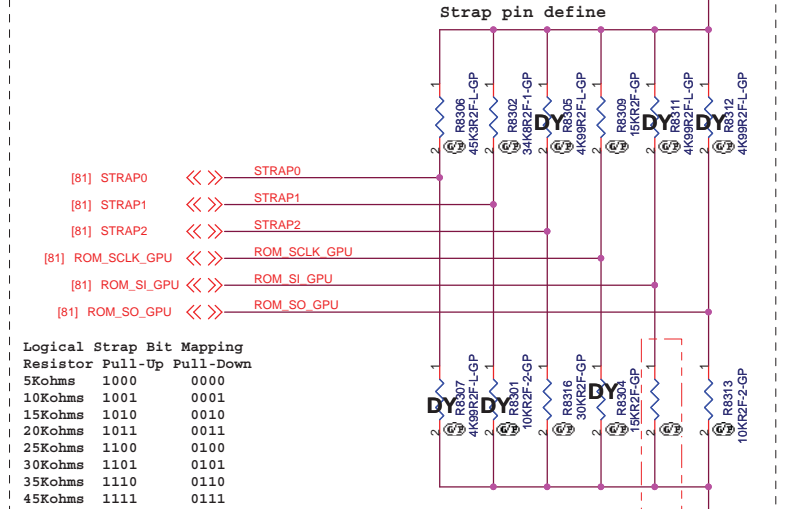
C26 DQMA#0 <<< DQMA#0 [84]  
B19 DQMA#1 <<< DQMA#1 [84]  
D19 DQMA#2 <<< DQMA#2 [84]  
D23 DQMA#3 <<< DQMA#3 [84]  
T24 DQMA#4 <<< DQMA#4 [85]  
AA23 DQMA#5 <<< DQMA#5 [85]  
AB27 DQMA#6 <<< DQMA#6 [85]  
T26 DQMA#7 <<< DQMA#7 [85]

D25 QSA#0 <<< QSA#0 [84]  
A18 QSA#1 <<< QSA#1 [84]  
E18 QSA#2 <<< QSA#2 [84]  
B24 QSA#3 <<< QSA#3 [84]  
R22 QSA#4 <<< QSA#4 [85]  
Y24 QSA#5 <<< QSA#5 [85]  
AA27 QSA#6 <<< QSA#6 [85]  
R27 QSA#7 <<< QSA#7 [85]

C25 QSA0 <<< QSA0 [84]  
A19 QSA1 <<< QSA1 [84]  
E19 QSA2 <<< QSA2 [84]  
A24 QSA3 <<< QSA3 [84]  
T22 QSA4 <<< QSA4 [85]  
AA24 QSA5 <<< QSA5 [85]  
AA26 QSA6 <<< QSA6 [85]  
T27 QSA7 <<< QSA7 [85]

F24 CLKA0 <<< CLKA0 [84]  
F23 CLKA0# <<< CLKA0# [84]  
N24 CLKA1 <<< CLKA1 [85]  
N23 CLKA1# <<< CLKA1# [85]

M22 FBA\_DEBUG  
A16 FBA\_VREF  
FB\_PLLAVDD FB\_PLLAVDD  
FB\_DLLAVDD FB\_DLLAVDD  
N11M-GE1-S-A2-GP-U



Strap0 Strap1 Strap2  
USER BIT0 1 3GIO\_PADCFG\_LUT\_ADR0 0 PCI\_DEVID\_0 1  
USER BIT1 1 3GIO\_PADCFG\_LUT\_ADR1 1 PCI\_DEVID\_1 0  
USER BIT2 1 3GIO\_PADCFG\_LUT\_ADR2 1 PCI\_DEVID\_2 1  
USER BIT3 1 3GIO\_PADCFG\_LUT\_ADR3 1 PCI\_DEVID\_3 0

EDID is used Reserved N11M-GE1 GPU Device ID=0x0A75

Default setting: SAMSUNG sDDR3 64Mx16BIT-->20K pull down (0x0011)

| RAM_CFG[3:0] | Config            | FB_BUS Width | Definitions |
|--------------|-------------------|--------------|-------------|
| 0000         |                   |              |             |
| 0001         |                   |              |             |
| 0010         | 64Mx16 DDR3 64Bit | Hynix        |             |
| 0011         | 04Mx16 DDR3 64Bit | Samsung      | Default     |
| 0100         |                   |              |             |
| 0101         |                   |              |             |
| 0110         |                   |              |             |
| 0111         |                   |              |             |

If use Hynix sDDR3 64Mx16BIT(0x0010), R8308 change to 15K

| SUB_VENDOR         | XCLK_417      | PEX_PLL_EN_TERM |
|--------------------|---------------|-----------------|
| 0 No VBIOS ROM     | 0 277MHz(POR) | 0 Disable (POR) |
| 1 BIOS ROM present | 1 Reserved    | 1 Enable        |

3GIO\_PADCFG USER[3:0]  
0000 Desktop 1111 Use EDID to detect panel settings  
1110 Notebook (POR)

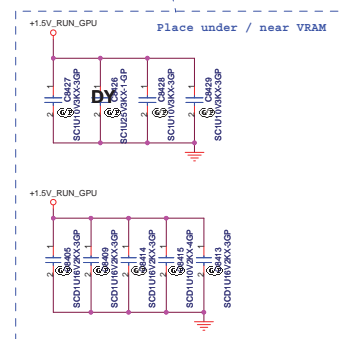
SLOT\_CLOCK\_CFG  
0 GPU and MCH do not share a common reference clock  
1 GPU and MCH share a common reference clock (POR)

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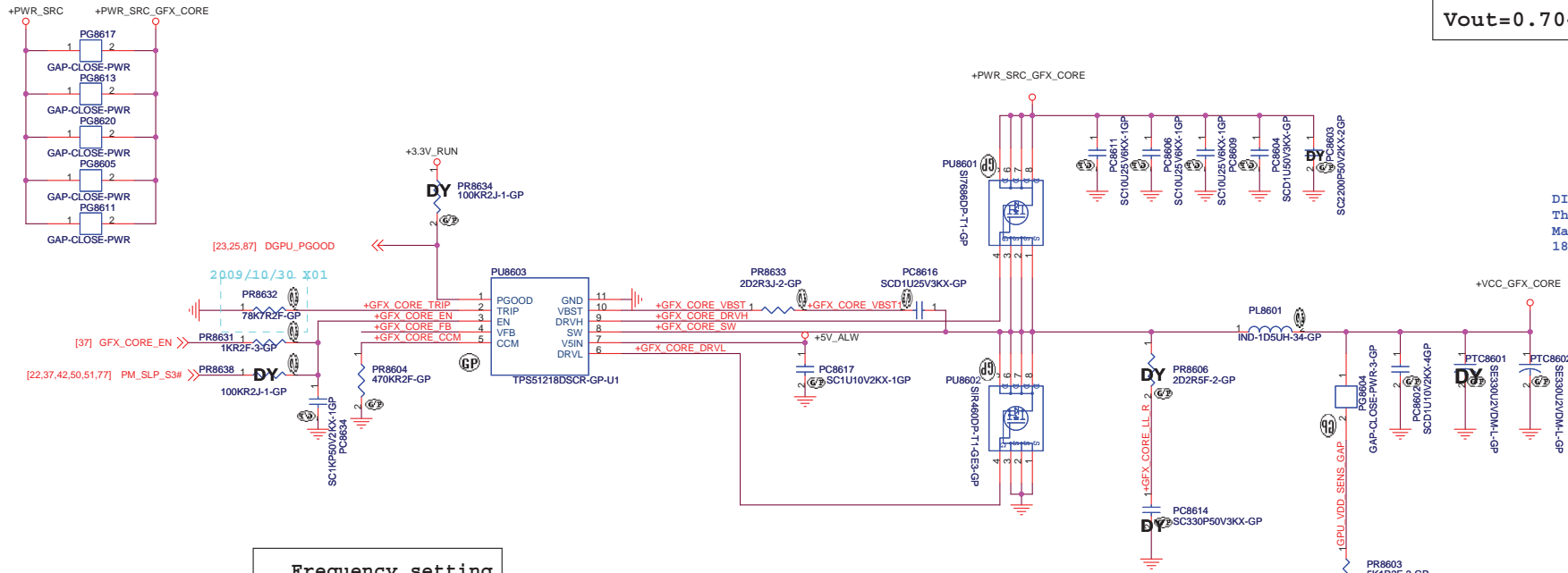


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$$V_{out} = 0.704V * (R1 + R2) / R2$$



DIS  
Thermal Design Current = 12.9A  
Max Current = 16.77A  
18.45A < OCP < 21.81A

#### Frequency setting

470K --> 290KHz  
200K --> 340KHz  
100K --> 380KHz  
39K --> 430KHz

| PWRCNTL_0 | PWRCNTL_1 | +VCC_GFX_CORE |
|-----------|-----------|---------------|
| L         | H         | 1.03V         |
| L         | L         | 0.85V         |

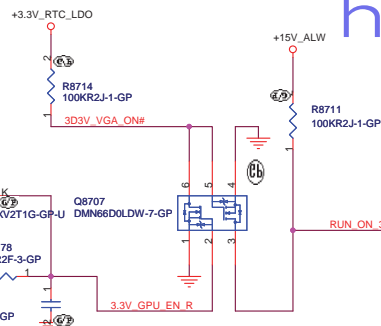
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 1.5UH PCMC104T-1R5MN Cynotec DCR:4.2mohm Isat =33Arms 68.1R510.10J  
O/P cap: 330U 2V EEPFX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01  
H/S: SI7686DP/ POWERPAK-8/ 11mOhm/ 14mOhm@4.5Vgs/ 84.07686.037  
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/ 6.1mohm@4.5Vgs/ 84.00460.037  
Switching freq-->350KHz

DW  
12/07 Item 1

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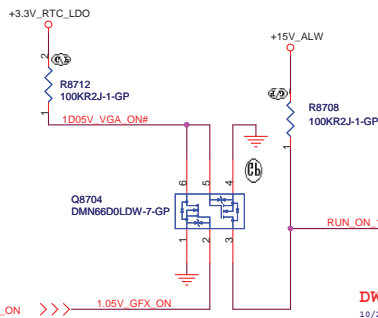
|                               |                                   |                                                                                                             |            |
|-------------------------------|-----------------------------------|-------------------------------------------------------------------------------------------------------------|------------|
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| Title                         |                                   |                                                                                                             |            |
| <b>TPS51218 +VCC GFX CORE</b> |                                   |                                                                                                             |            |
| Size                          | Document Number                   |                                                                                                             | Rev        |
| Custom                        | <b>Vostro Calpella (Discrete)</b> |                                                                                                             | <b>X01</b> |
| Date:                         | Monday, January 18, 2010          | Sheet                                                                                                       | 86 of 91   |

### +3.3V\_RUN\_GPU



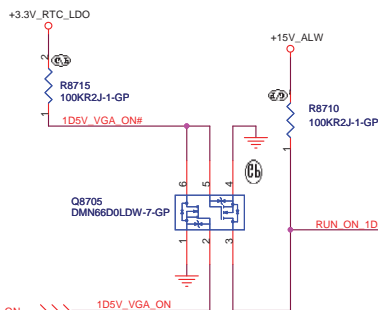
Peak current: 1140 mA  
Design current: 798 mA

### +1.05V\_GFX\_PCIE:



Peak current: 3550 mA  
Design current: 2485 mA

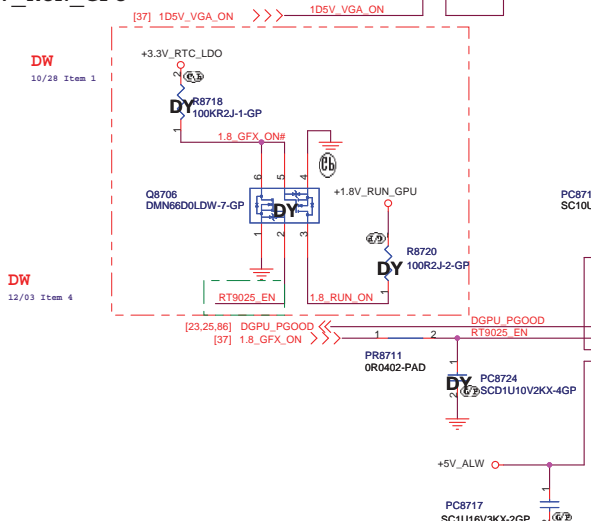
### +1.5V\_RUN\_GPU:



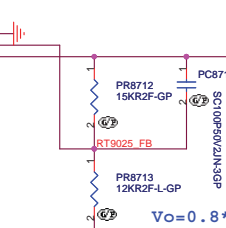
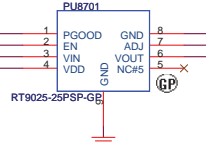
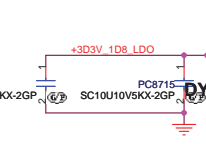
Place near device side(VGA chip),  
use 10 mil trace between power  
rail and Q8701 Drain

Peak current: 4230 mA  
Design current: 2961 mA

### +1.8V\_RUN\_GPU



DIS:  
Peak current: 300 mA  
Design current: 210 mA



$$Vo = 0.8 * (1 + (R1/R2))$$

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|             |                          |                                                                               |          |
|-------------|--------------------------|-------------------------------------------------------------------------------|----------|
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| Title       |                          | <b>LDO 1.8V</b>                                                               |          |
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| Date:       | Monday, January 18, 2010 | Sheet                                                                         | 87 of 91 |




| DATE       | VERSION | ITEM | PAGE  | Modify List                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Issue Description                                                                         | OWNER |
|------------|---------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|-------|
| 2009/10/15 | X01     | 1    | 25    | Swapped Q2515 C,E Pin                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | For correct.                                                                              | EE    |
|            |         | 2    | All   | Combine pull-up/down resistors from single to series resistor                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | For save more part counts                                                                 | EE    |
|            |         | 3    | 37    | Update 10mW circuit.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | For DC mode power consumption can be less than 10mW under S5.                             | EE    |
|            |         | 4    | 22    | Add U2213,R2221                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Added 3v/5v S5 power good to control resume reset sequence circuit prevent RTC data loss. | EE    |
|            |         | 5    | 51    | stuffed PC5105 with 1uF                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | For power sequencing of +1.8V_RUN , Delay timing                                          | EE    |
|            |         | 6    | 23    | Added 25M Crystal                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | For DCI ( DisplayClock_Integration )                                                      | EE    |
|            |         | 7    | 79    | Added BOSS4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | For Steady the thermal module                                                             | EE    |
|            |         | 9    | All   | BOSS1 from 34.4W005.001 to 34.4CQ03.101<br>CON3 from 20.K0315.005 to 20.K0293.006<br>CON4 from 20.K0315.028 to 20.K0275.028<br>CON6 from 20.K0315.036 to 20.K0276.036<br>DM1 from 62.10017.U81 to 62.10017.P31<br>DM2 from 62.10017.U71 to 62.10017.Q31<br>HOLE1 from ZZ.00PAD.I71 to ZZ.00PAD.G51<br>HOLE2 from ZZ.00PAD.K81 to ZZ.00PAD.E11<br>HOLE3 from ZZ.00PAD.N81 to ZZ.00PAD.D71<br>HOLE4 from ZZ.00PAD.N81 to ZZ.00PAD.D71<br>HOLE5 from ZZ.00PAD.K11 to ZZ.00PAD.E11<br>HOLE6 from ZZ.00PAD.I71 to ZZ.00PAD.G51<br>HOLE7 from ZZ.00PAD.I71 to ZZ.00PAD.G51<br>HOLE8 from ZZ.00PAD.N91 to ZZ.00PAD.D31<br>HOLE9 from ZZ.00PAD.J01 to ZZ.00PAD.D11<br>LCD1 from 20.F1093.040 to 20.F1555.030<br>TPAD1 from 20.K0320.004 to 20.K0265.004 | For ME request Changed connect PN:                                                        | ME    |
|            |         |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                           |       |
|            |         |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                           |       |
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|            |         |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                           |       |
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|            |         |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                           |       |
| 2009/10/16 |         | 1    | 37,87 | Removed CAPA_RST# from Capacity board                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                           | EE    |
|            |         |      |       | Added Switch Baord Detection circuit                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | For software request.                                                                     | EE    |
| 2009/10/19 |         | 1    | 77    | Reversal CON6 Pin 36 <-> 1 ; 35 <-> 2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | For new connect pin define.                                                               | EE    |
|            |         | 2    | 9,27  | Changed RN907,L2701,L2704                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | For update components                                                                     | EE    |
|            |         | 3    | 74    | Swapped the RN7408,RN7409,RN7410,RN7411                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | For Layout request.                                                                       | EE    |
|            |         |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                           |       |
|            |         |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                           |       |
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| Title <b>Change List - EE(2)</b>                                                      |                                                                                                             |

|          |                          |               |
|----------|--------------------------|---------------|
| Size     | Document Number          | Rev           |
| Customer | <b>Vostro Calpella</b>   | X1            |
| Date     | Friday, January 15, 2010 | Sheet 89 of 9 |

| DATE       | VERSION | ITEM | PAGE  | Modify List                                                                            | Issue Description    | OWNER |
|------------|---------|------|-------|----------------------------------------------------------------------------------------|----------------------|-------|
| 2009/10/19 | X01     |      |       |                                                                                        |                      |       |
|            |         |      |       |                                                                                        |                      |       |
|            |         |      |       |                                                                                        |                      |       |
|            |         | 2    | 81    | Remove R8149                                                                           | For EMI team request | EMI   |
|            |         |      | 21    | PCLK_FWH、CLK_PCI_FB、PCLK_KBC、PCLK_TPM reserve by pass cap                              |                      |       |
|            |         |      | 23    | CLK_PCH_48M reserve by pass cap                                                        |                      |       |
| 2009/10/22 |         |      | 23    | Romove R2350 and C2324                                                                 |                      |       |
|            |         |      | 37    | Romove R3726 and C3704                                                                 |                      |       |
|            |         |      | 79    | Reserve +PWR_SRC to GND cap                                                            |                      |       |
|            |         | 3    | 79    | Add EC7934 0.1u in +VCC_CORE                                                           | For EMI team request | EMI   |
|            |         |      |       | Add EC7911 0.1u +1.5V_SUS to GND cap*1                                                 |                      |       |
|            |         |      |       | Add EC7935,EC7936 0.1u +1.5V_SUS to GND cap*2                                          |                      |       |
|            |         |      |       | Add EC7937 0.1u +1.5V_SUS to GND cap*1                                                 |                      |       |
| 2009/10/23 |         |      |       | Add EC7938 0.1u +PWR_SRC to GND cap*1                                                  |                      |       |
|            |         |      |       | Update TR6304,TR6305 p/n to 68.00201.141                                               |                      |       |
|            |         | 4    | 73    | Move EC7302                                                                            | For EMI team request | EMI   |
|            |         |      | 79    | dummy 0.1u x 2 in green area 6135,195 ----EC7939,EC7940                                |                      |       |
|            |         |      |       | dummy 0.1u cap in red area 1755,4435 -----EC7941                                       |                      |       |
|            |         |      |       | dummy 1000p in green area 5225,6950----EC7942                                          |                      |       |
|            |         |      |       | dummy 1000p in green area 3780,6180-----EC7943                                         |                      |       |
|            |         |      |       | dummy 104p and 1000p in green area 5385,7010---EC7944,EC7945                           |                      |       |
|            |         |      |       | dummy 0.1u in green area 3400,6300---EC7946                                            |                      |       |
|            |         |      |       | dummy 0.1u in green area 1240,4035--EC7947                                             |                      |       |
| 2009/12/08 | SC      |      | 55    | add damping 33ohm on R,G,B Singel---R5594,R5595,R5596                                  |                      |       |
| 2009/12/09 | SC      | 1    | 79    | mount EC7948,EC7949,EC7934                                                             | For RF Team request  | RF    |
|            |         | 1    | 73    | mount LECM2012H-900QT-GP in L7301                                                      | For EMI team request | EMI   |
|            |         | 2    | 24,77 | change R2405 from 10 ohm to 56 ohm and mount 120 ohm bead bead p/n:BLM15EG121SN1 L7702 |                      |       |
|            |         | 3    | 73    | mount 220p cap on EC7302 and EC7303                                                    |                      |       |
|            |         | 4    | 79    | Add EC7950                                                                             |                      |       |
|            |         |      |       |                                                                                        |                      |       |
|            |         |      |       |                                                                                        |                      |       |
|            |         |      |       |                                                                                        |                      |       |
|            |         |      |       |                                                                                        |                      |       |
|            |         |      |       |                                                                                        |                      |       |

| DATE       | VERSION | ITEM | PAGE | Modify List                                   | Issue Description                      | OWNER      |
|------------|---------|------|------|-----------------------------------------------|----------------------------------------|------------|
| 2009/10/22 | X011    | 1    | 46   | PR4604,PR4605 --> 4.7ohm for RT, 0 ohm for TI | Change PU4603 from TPS51125 to RT8205B | Power Team |
|            |         |      |      | PR4622 --> 820k ohm for RT, DY for TI         |                                        |            |
|            |         |      |      | PR4616 --> ASM for RT, DY for TI              |                                        |            |
|            |         |      |      | PR4617 --> DY for RT, ASM for TI              |                                        |            |
| 2009/10/29 |         |      | 53   | PC5307 change to 68nF for Intel spec          | Improve Jitter issue                   | Power Team |
|            |         | 2    | 50   | Add 4.7uF at +PWR_SRC_1D5V                    |                                        |            |
|            |         |      |      |                                               |                                        |            |
|            |         |      |      |                                               |                                        |            |
|            |         |      |      |                                               |                                        |            |
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|            |         |      |      |                                               |                                        |            |
|            |         |      |      |                                               |                                        |            |
|            |         |      |      |                                               |                                        |            |
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|            |         |      |      |                                               |                                        |            |
|            |         |      |      |                                               |                                        |            |

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|--------------------------------|------------------------|------------|----|----------------------------|----|
| Title                          |                        |            |    | <b>Change List - Power</b> |    |
| Size                           | Document Number        | Rev        |    |                            |    |
| Custom                         | <b>Vostro Calpella</b> | <b>X01</b> |    |                            |    |
| Date: Monday, January 18, 2010 |                        | Sheet      | 91 | of                         | 91 |