

RYU2-13 CALPELLA UMA Schematics

Intel ULV CPU-Arrandale SFF

Intel Ibex Peak-M

2010-09-28

REV : A00

DY : Nopop Component

<Core Design>



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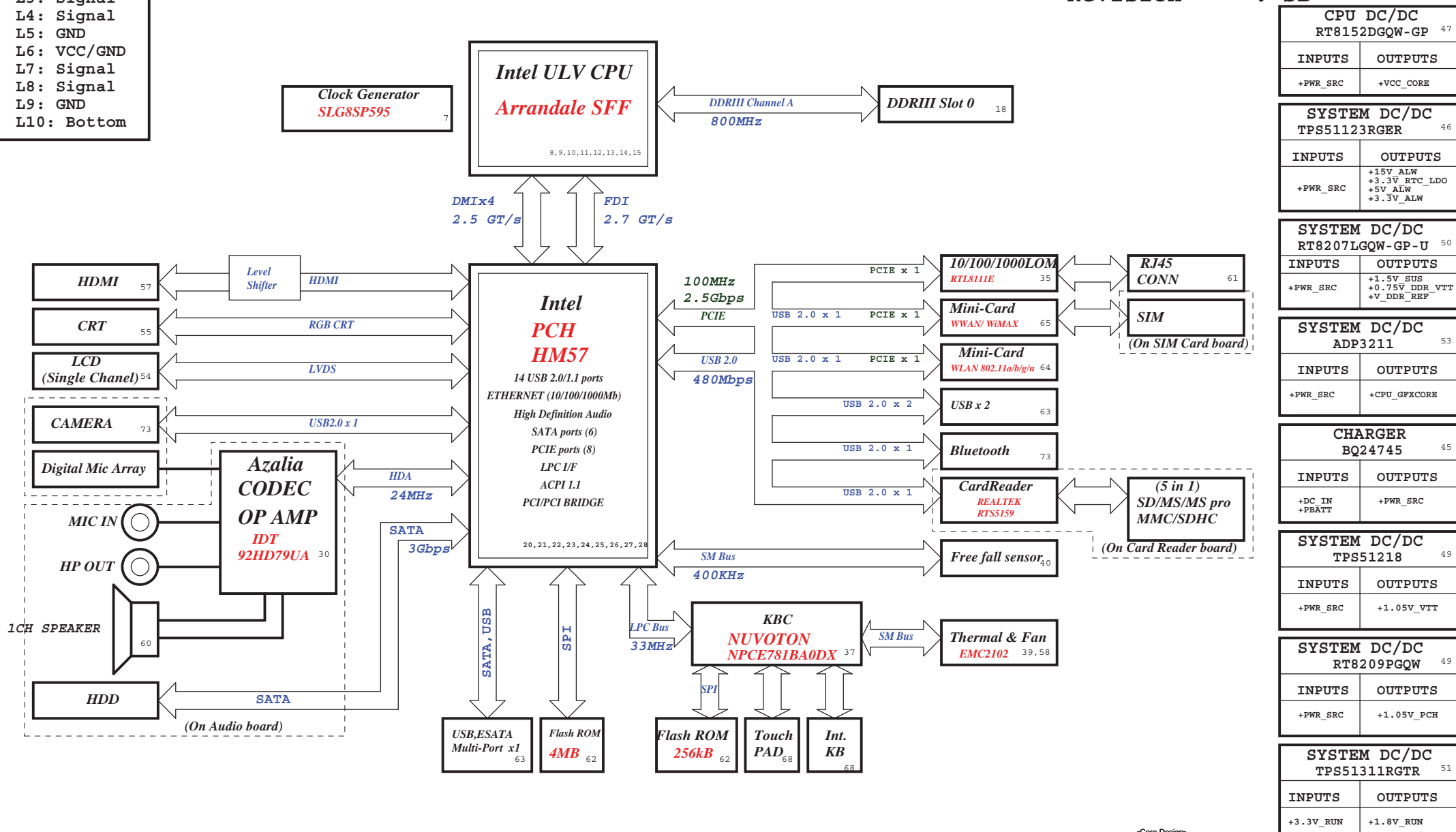
Title		
Cover Page		
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PCB LAYER
L1: Top
L2: GND
L3: Signal
L4: Signal
L5: GND
L6: VCC/GND
L7: Signal
L8: Signal
L9: GND
L10: Bottom

- L1: Top
L2: GND
L3: Signal
L4: Signal
L5: GND
L6: VCC/GND
L7: Signal
L8: Signal
L9: GND
L10: Bottom

RYU2 <http://hobi.cadktronika.net>

Project code : 91.4M101.001
Part Number : 48.4M101.0SB
PCB P/N : 10251
Revision : SB

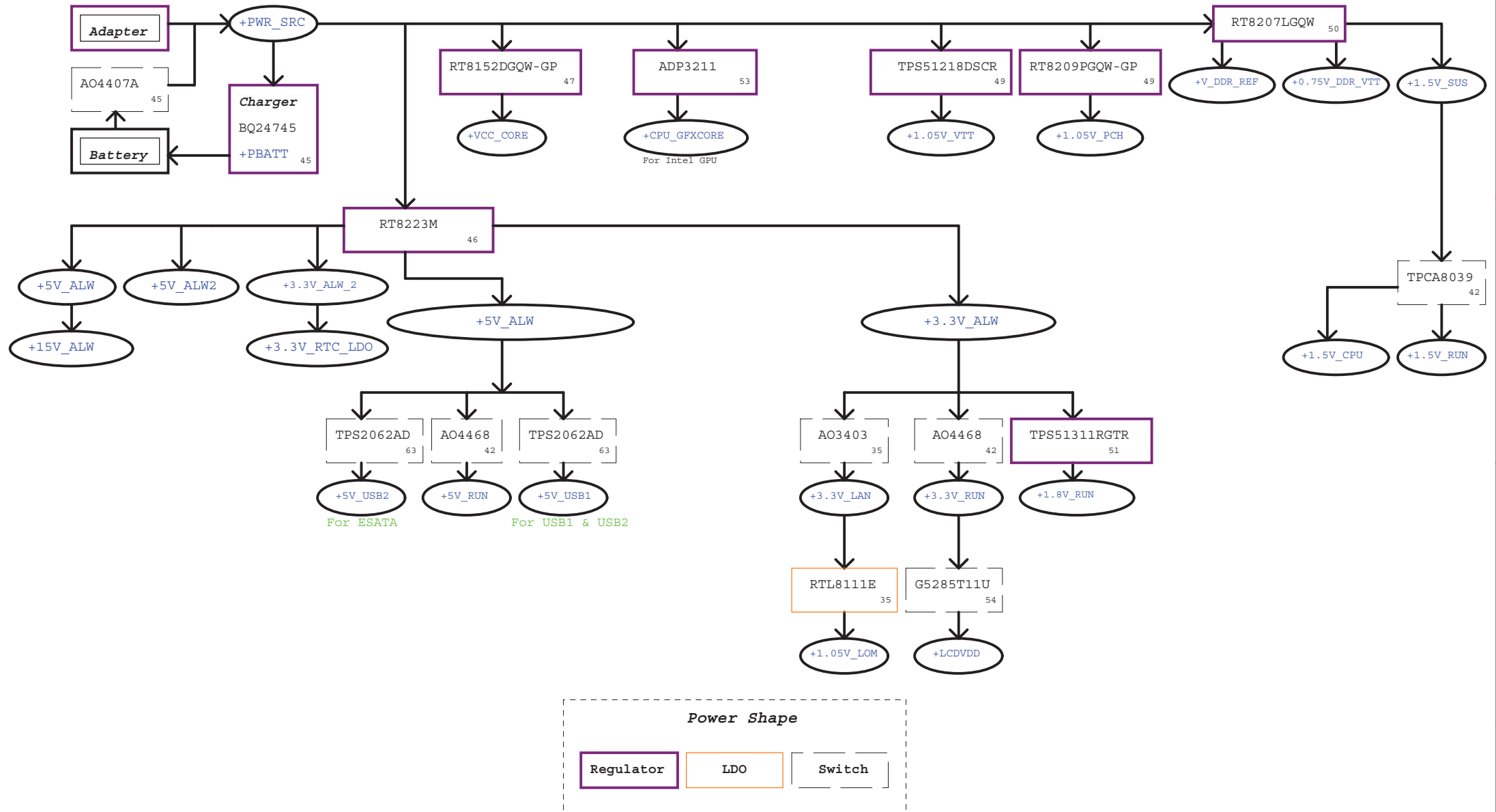


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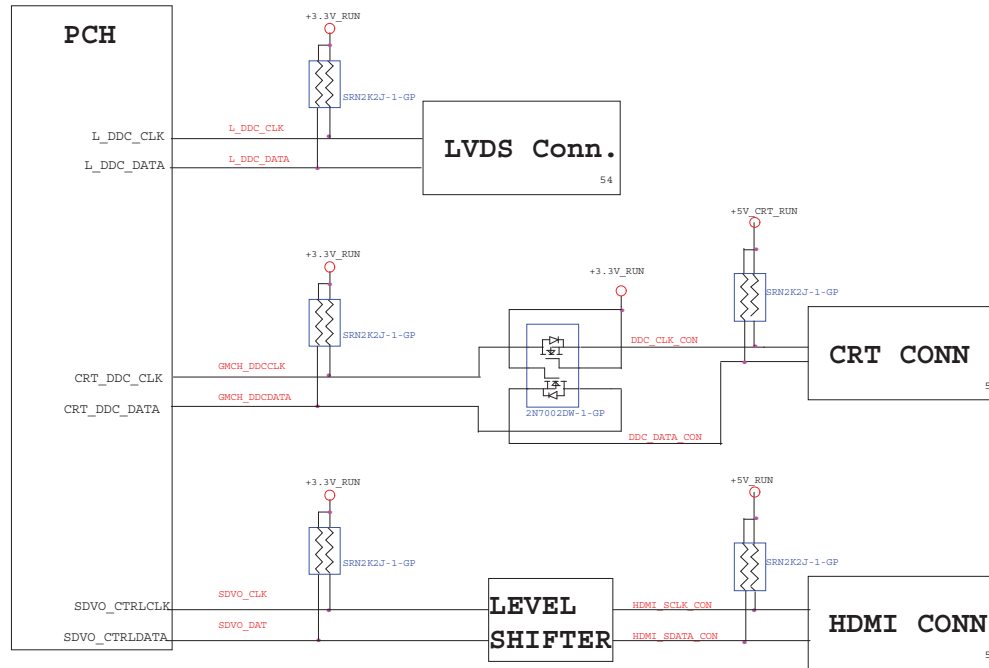
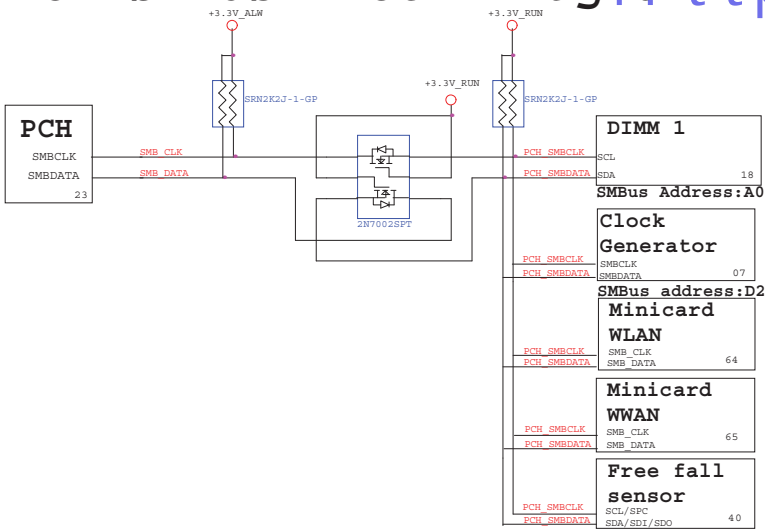
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Title			
Block Diagram			
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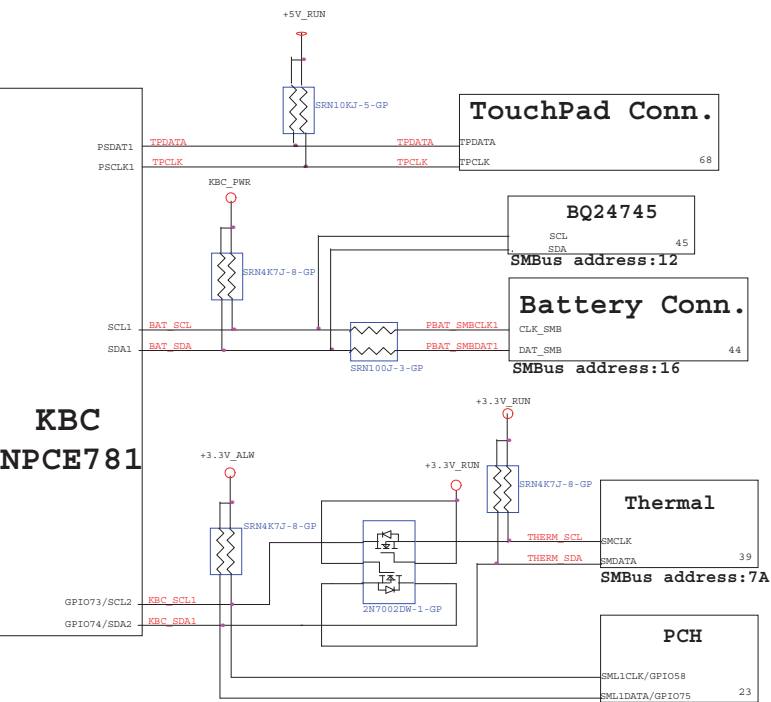


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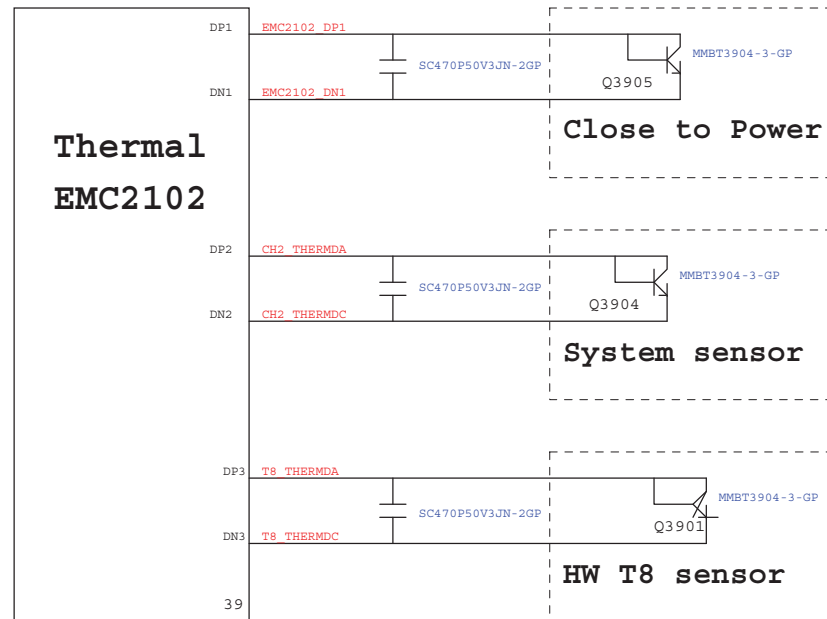
PCH SMBus Block Diagram



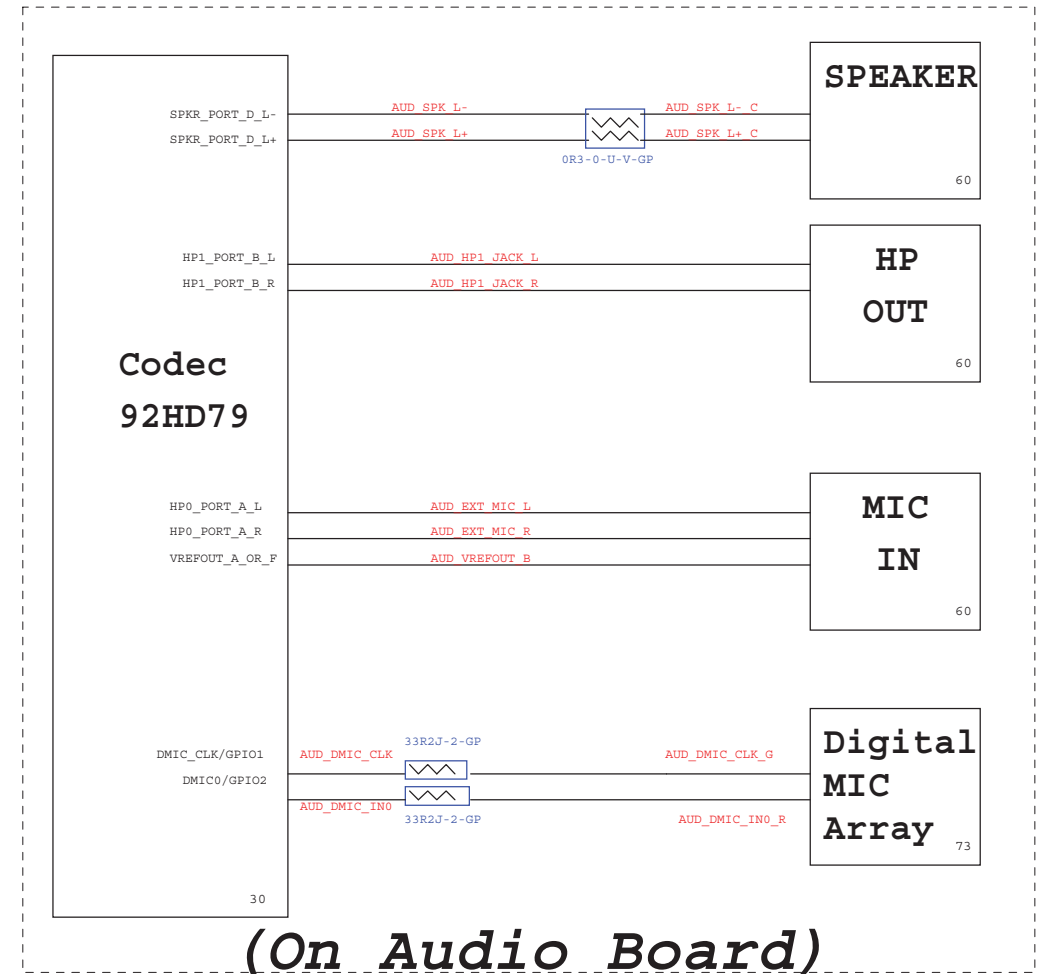
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor. Intel suggest 1K resistor (Fonseca)
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode Note: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ; do not stuff resistor.
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled Note: CRB uses a 330-kΩ resistor.
GNT0#, GNT1#	Default (SPI): Leave both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor. Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating.
GNT2#/GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	Enable Intel Anti-Theft Technology: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Intel Anti-Theft Technology: Left floating, no pull-down required.
NV_ALE	Enable Intel Anti-Theft Technology: Connect to +NVRAM_Vccq with 8.2-kΩ weak pull-up resistor.[CRB has it pulled up with 1-kΩ no-stuff resistor] Disable Intel Anti-Theft Technology: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HDA_DOCK_EN#/GPIO[33]	Low (0)- Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1)-. Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kΩ pull-down for PD Override. There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (0)- Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1)-. Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note: This is an unmuxed signal. This signal has a weak internal pull-down of 20 KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kΩ pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	Default = Do not connect (floating). Internal pull-up. High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1:Disabled - No Physical DisplayPort attached to Embedded DisplayPort 0:Enabled - An external DisplayPort device is connected to the Embedded DisplayPort	1
CFG[3]	PCI-Express Static Lane Reversal	1:Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 -> 1	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1


PCIE Routing

LANE1	RESERVE
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	MiniCard WWAN
LANE5	RESERVE

USB Table

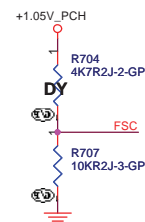
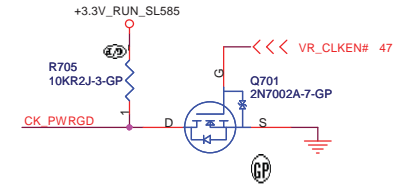
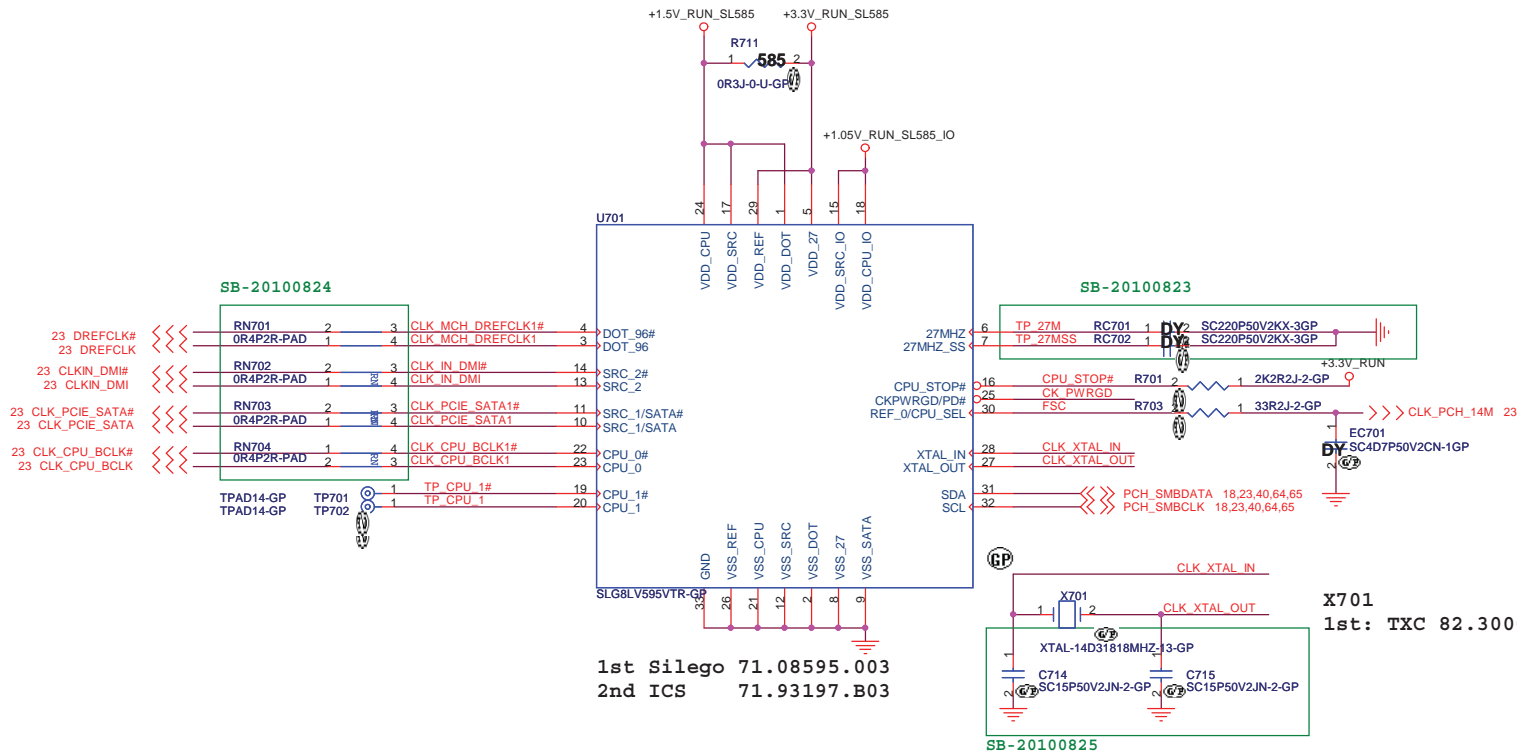
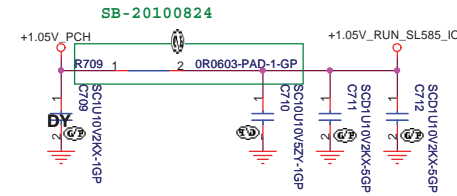
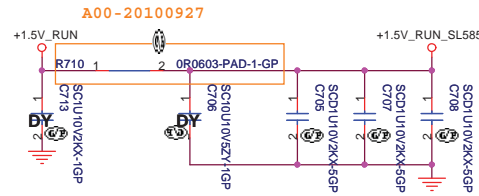
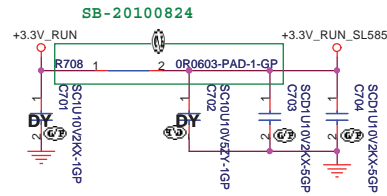
USB	
Pair	Device
0	USB1
1	USB2
2	USB for ESATA
3	RESERVE
4	WLAN
5	WWAN
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BLUETOOTH
9	Card Reader
10	RESERVED
11	CAMERA
12	RESERVED
13	RESERVED

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Title			
Table of Content			
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SSID = Clock GEN

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FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title			
Clock Generator SLG8SP585			
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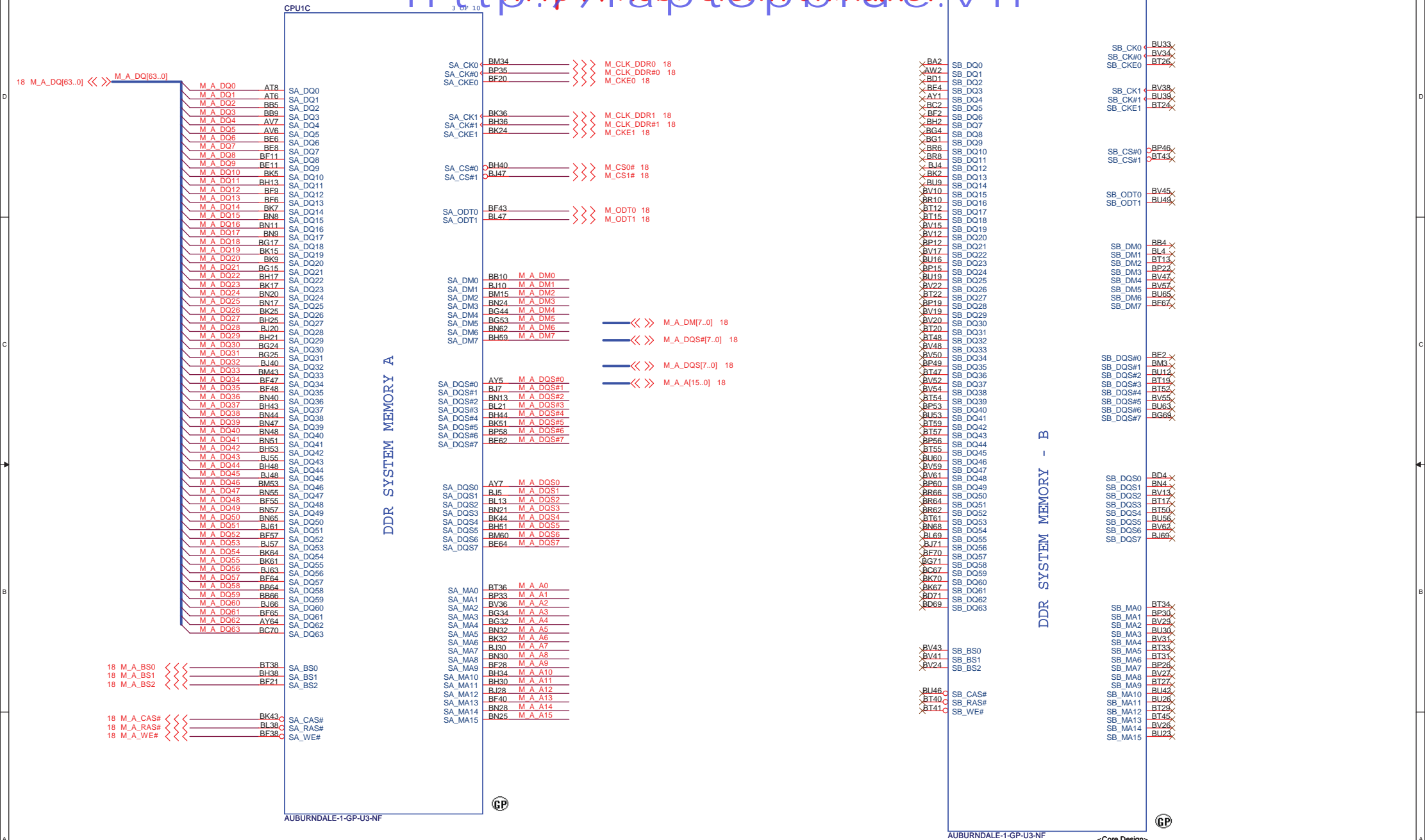
**CPU (PCIE/DMI/FDI)-1/8*****RYU2 13 UMA***

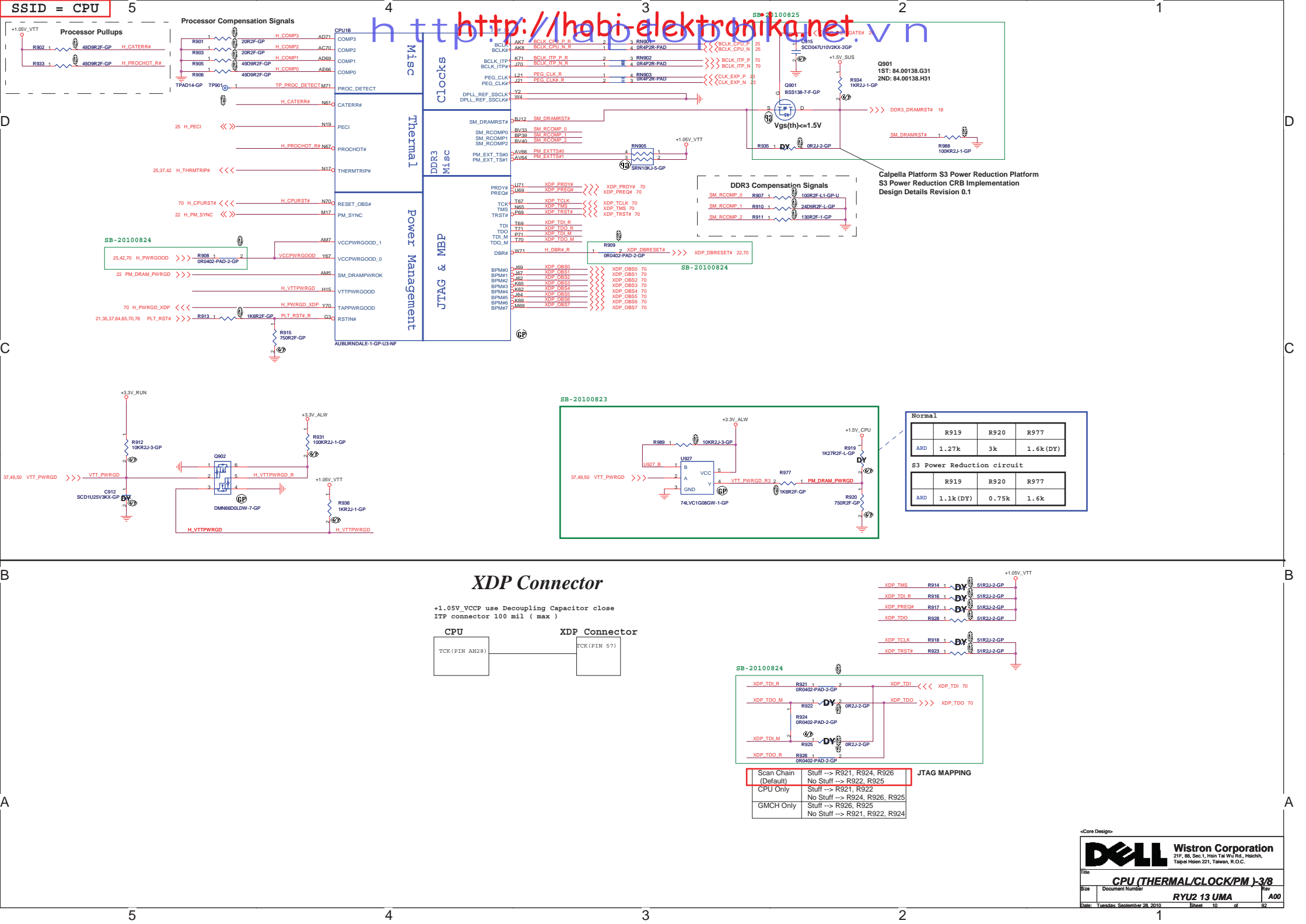
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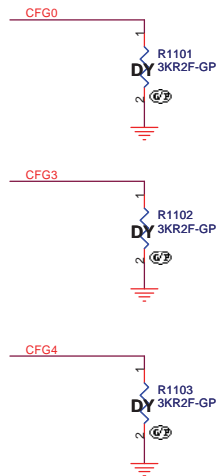
SSID = CPU

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CPUID 4 OF 10



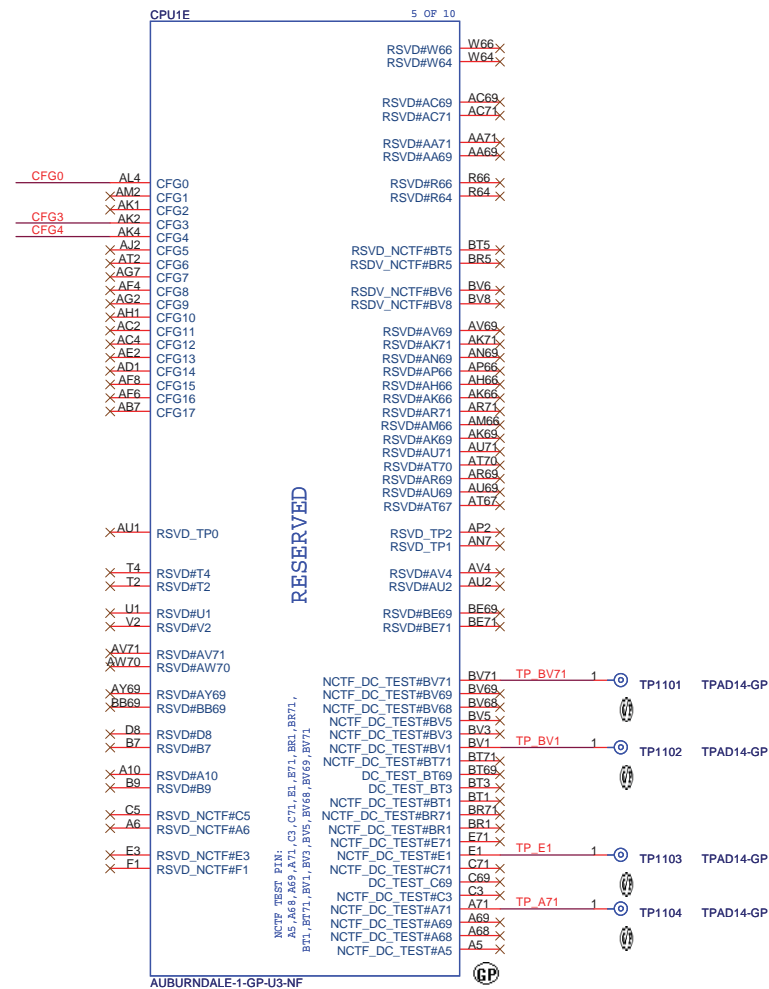




PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

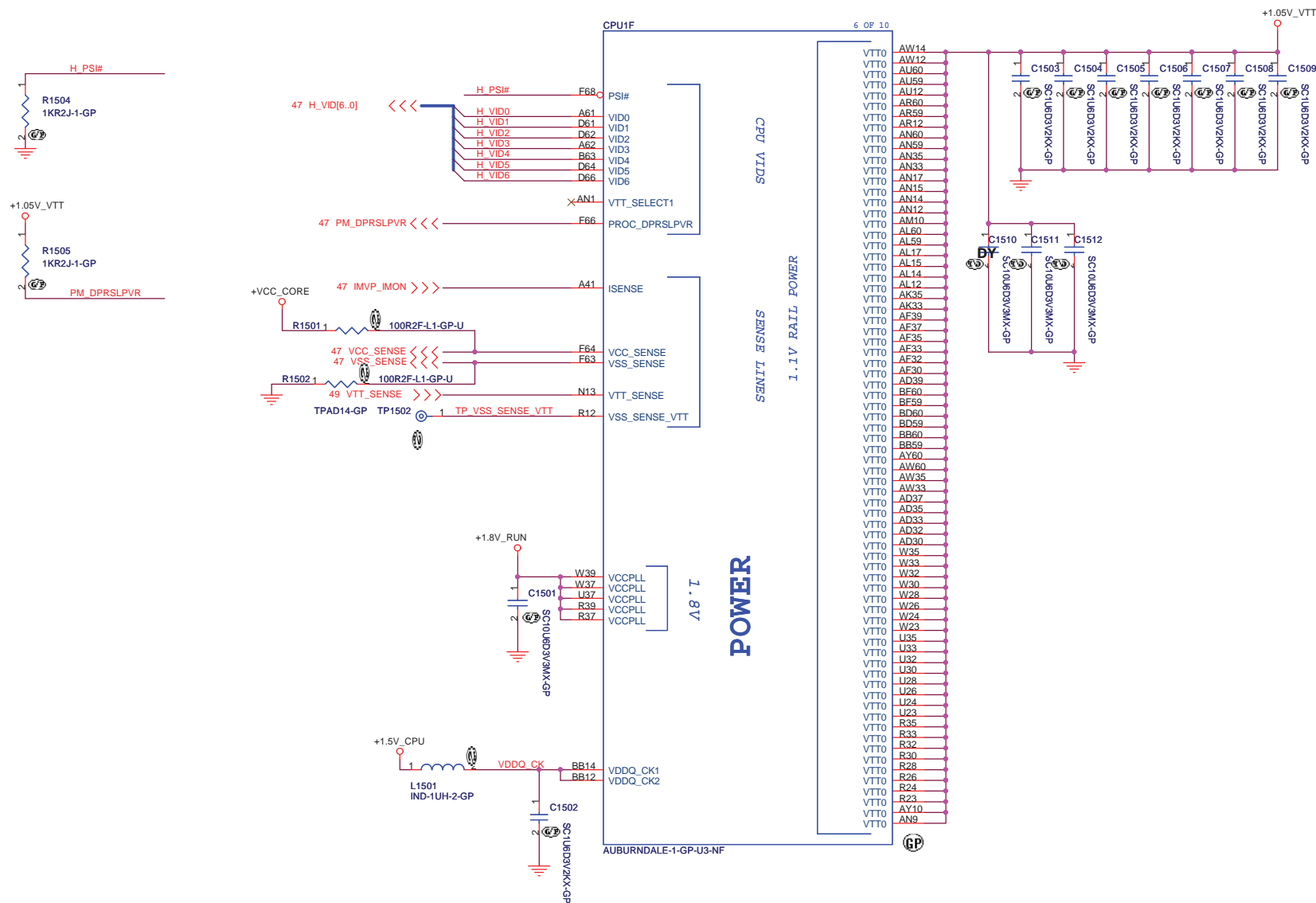
CFG4 - Embedded DisplayPort Presence	
CFG4	1:Disabled - No Physical Display Port attached to Embedded DisplayPort 0:Enabled - An external DisplayPort device is connected to the Embedded DisplayPort



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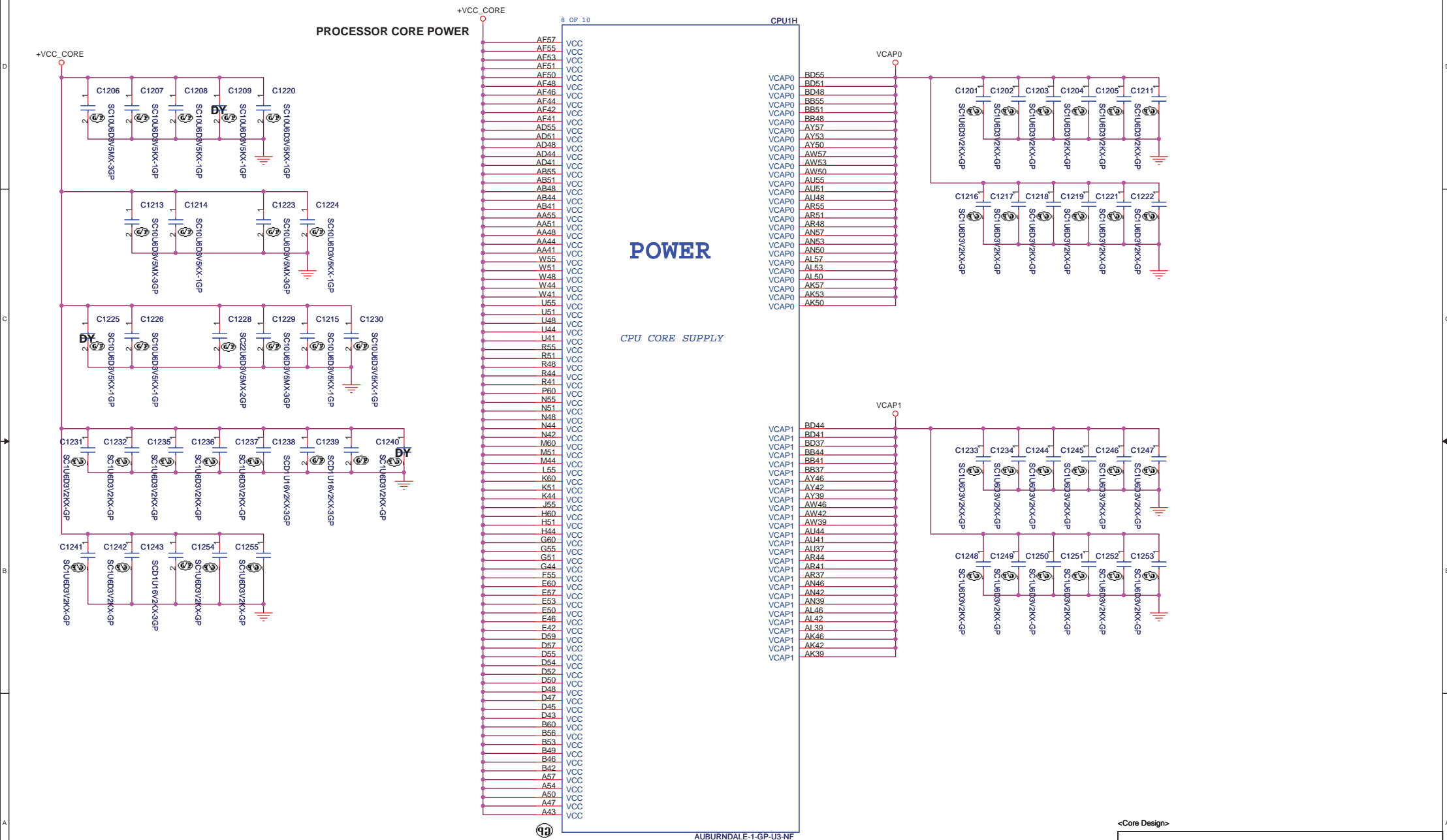


Title		CPU (RESERVED)-4/8	
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SSID = CPU

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Title		CPU (VCC CORE)-6/8	
Size	Document Number	Rev	A00
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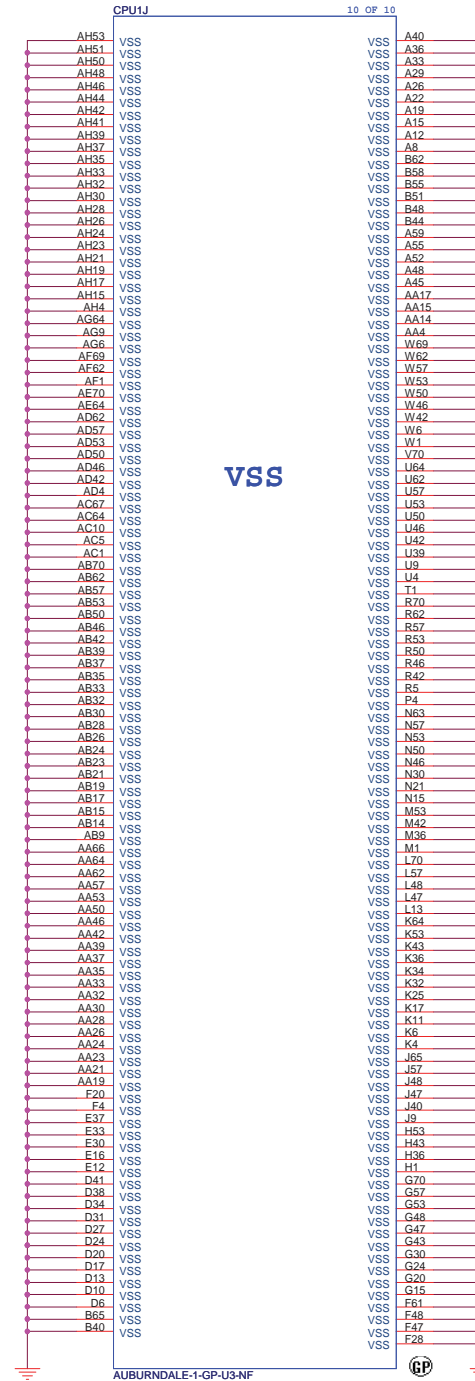
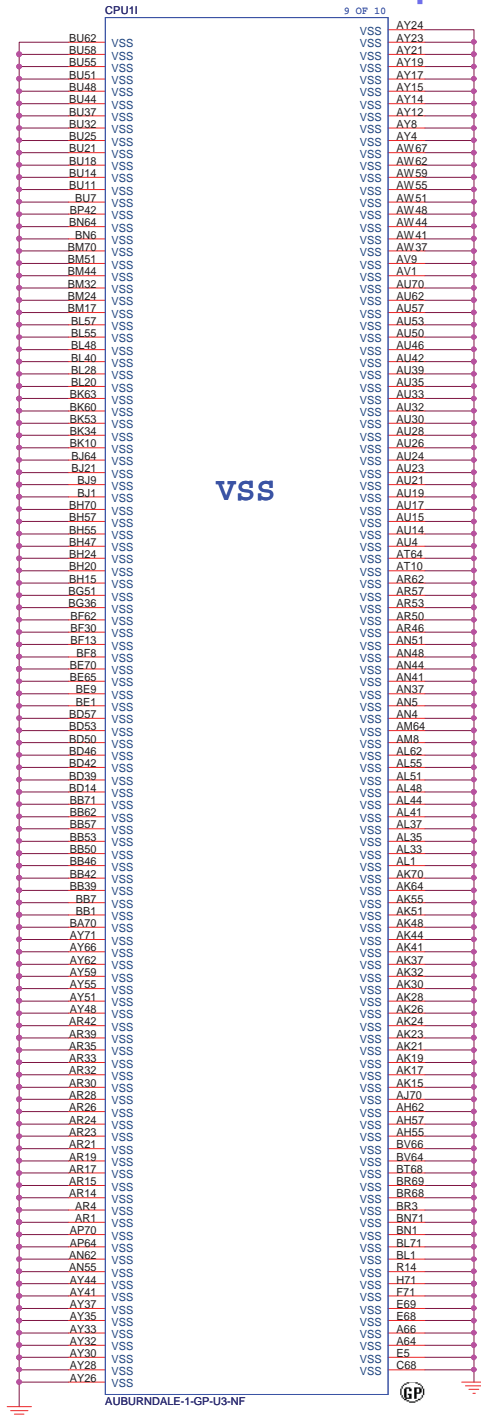
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CPU (VCC GFXCORE)-7/8

RYU2 13 UMA

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RYU2 13 UMA


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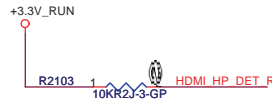
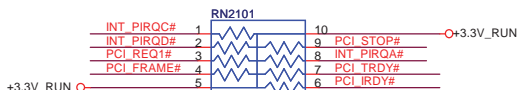
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Size A4	Document Number RYU2 13 UMA	Rev A00
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Title			
PCH (LVDS/CRT/DDI)			
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SSID = PCH

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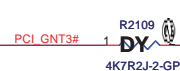


BOOT BIOS Strap

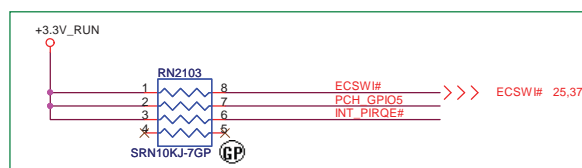
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)

A16 swap override Strap/Top-Block
Swap Override jumper

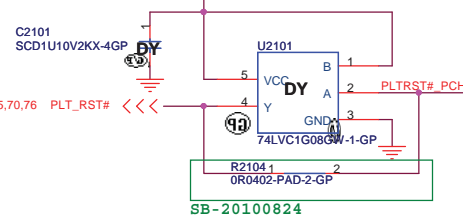
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default
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SB-20100824



10,35,37,64,65,70,76 PLT_RST# <<<



SB-20100824

SB-20100824

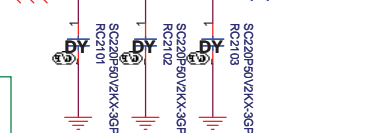
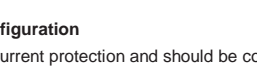
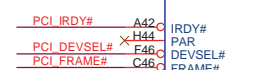
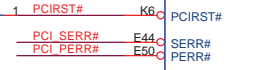
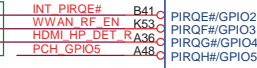
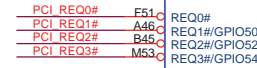
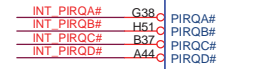
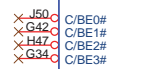
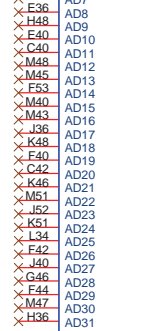
70 PCLK_FWH
23 CLK_PCI_FB
37 PCLK_KBCCalpella Platform Design Guide
Revision 1.6

Table 111. Overcurrent Pin Example Configuration

These OC7# pins are not used for USB overcurrent protection and should be configured as GPIOs. The unused USB ports can be left as no connect.



NVDRAM

PCI

USB

USB

IBEXPEAK-M-GP-NF

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RP2101

SRN10KJ-L3-GP

+3.3V_ALW

+3.3V_ALW

+3.3V_ALW

+3.3V_ALW

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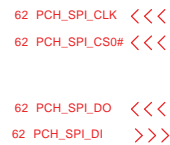
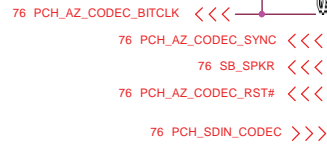
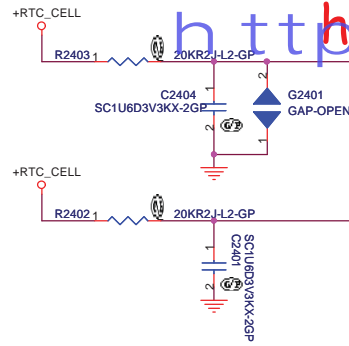
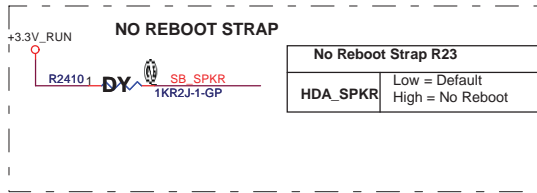
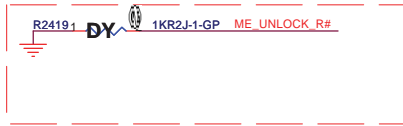
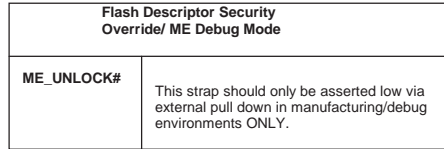
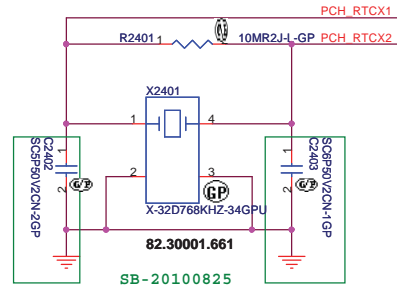
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NV_CLE

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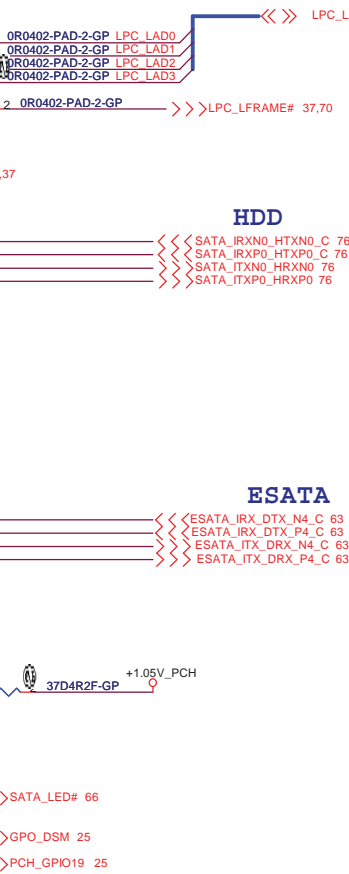
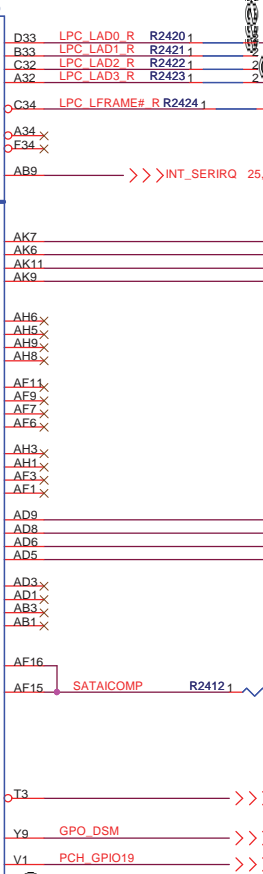
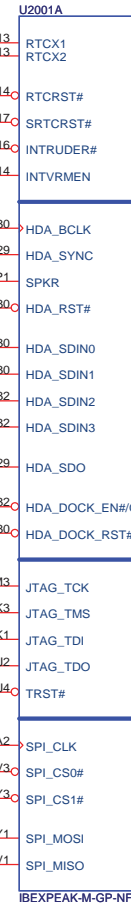


SSID = PCH



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1.1V VRM Enable
High - Enable internal VRs



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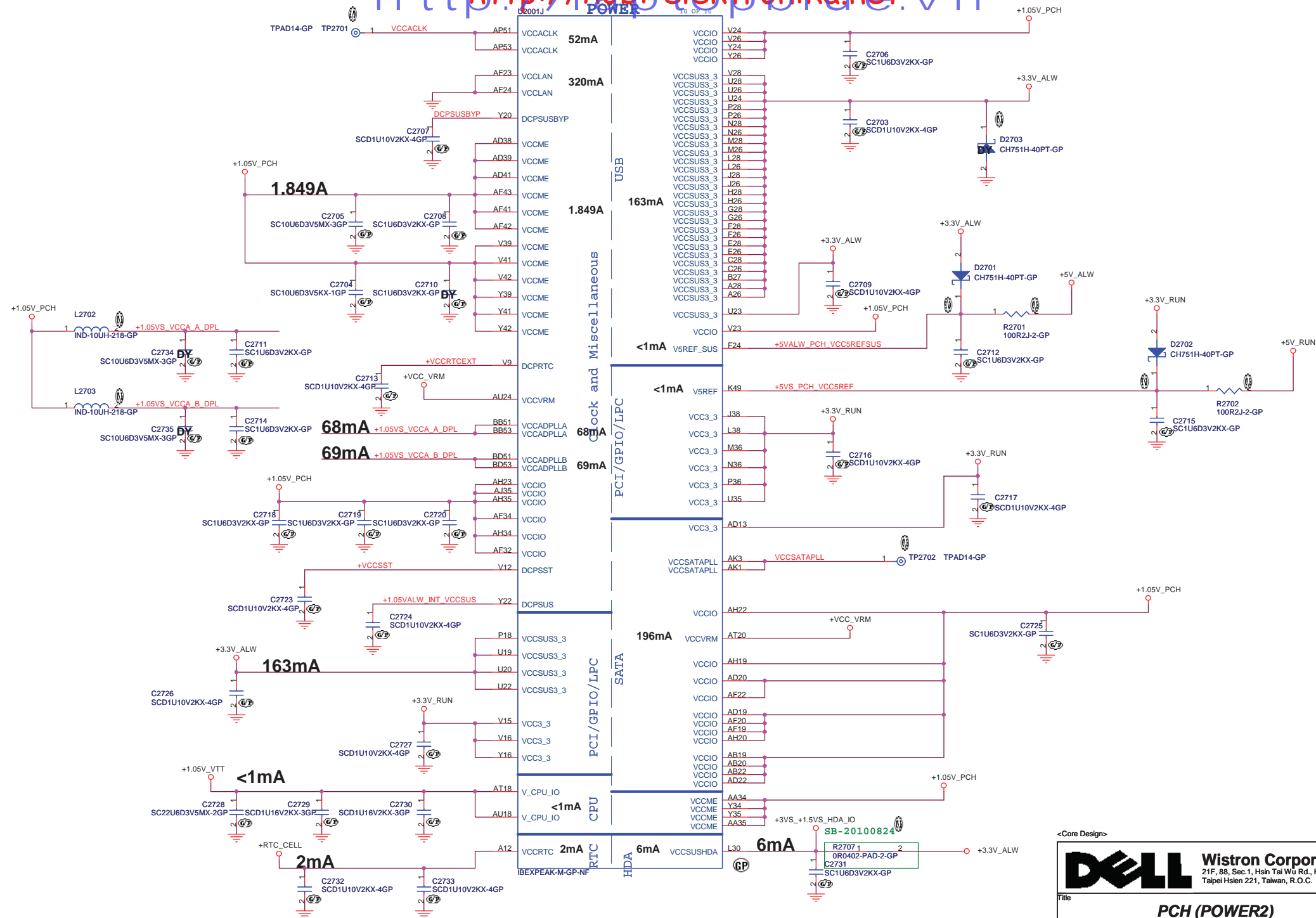
PCH (POWER1)

RYU2 13 UMA

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SSID = PCH

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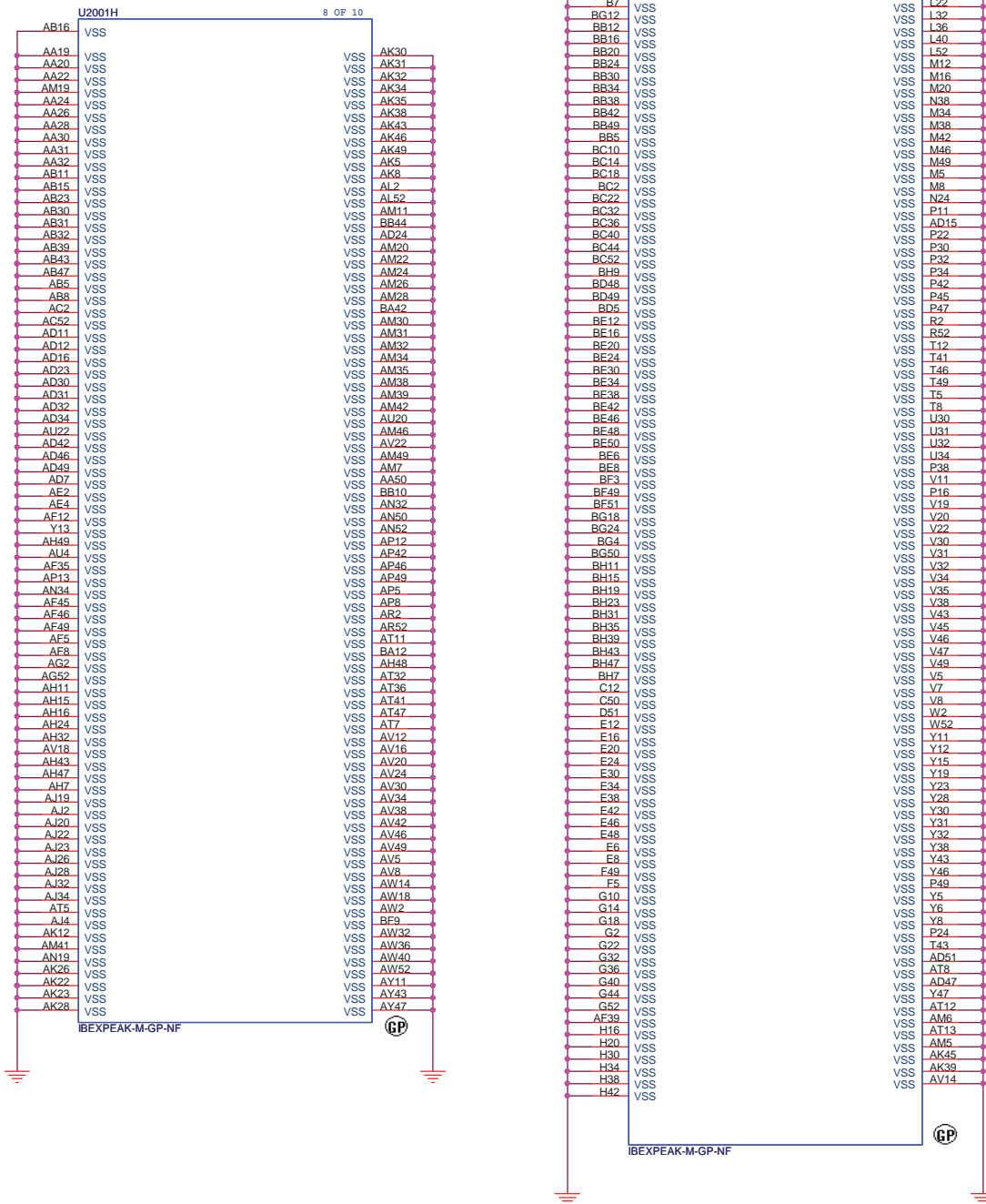
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Size: Document Number: **RYU2 13 UMA** Rev: **A00**
Date: Tuesday, September 28, 2010 Sheet 27 of 92

SSID = PCH

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<Core Design>

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Title: **PCH (VSS)**

Size: Document Number: **RYU2 13 UMA** Rev: **A00**

Date: Tuesday, September 28, 2010 Sheet 28 of 92


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Title (Reserved)			
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Title

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Size
A4

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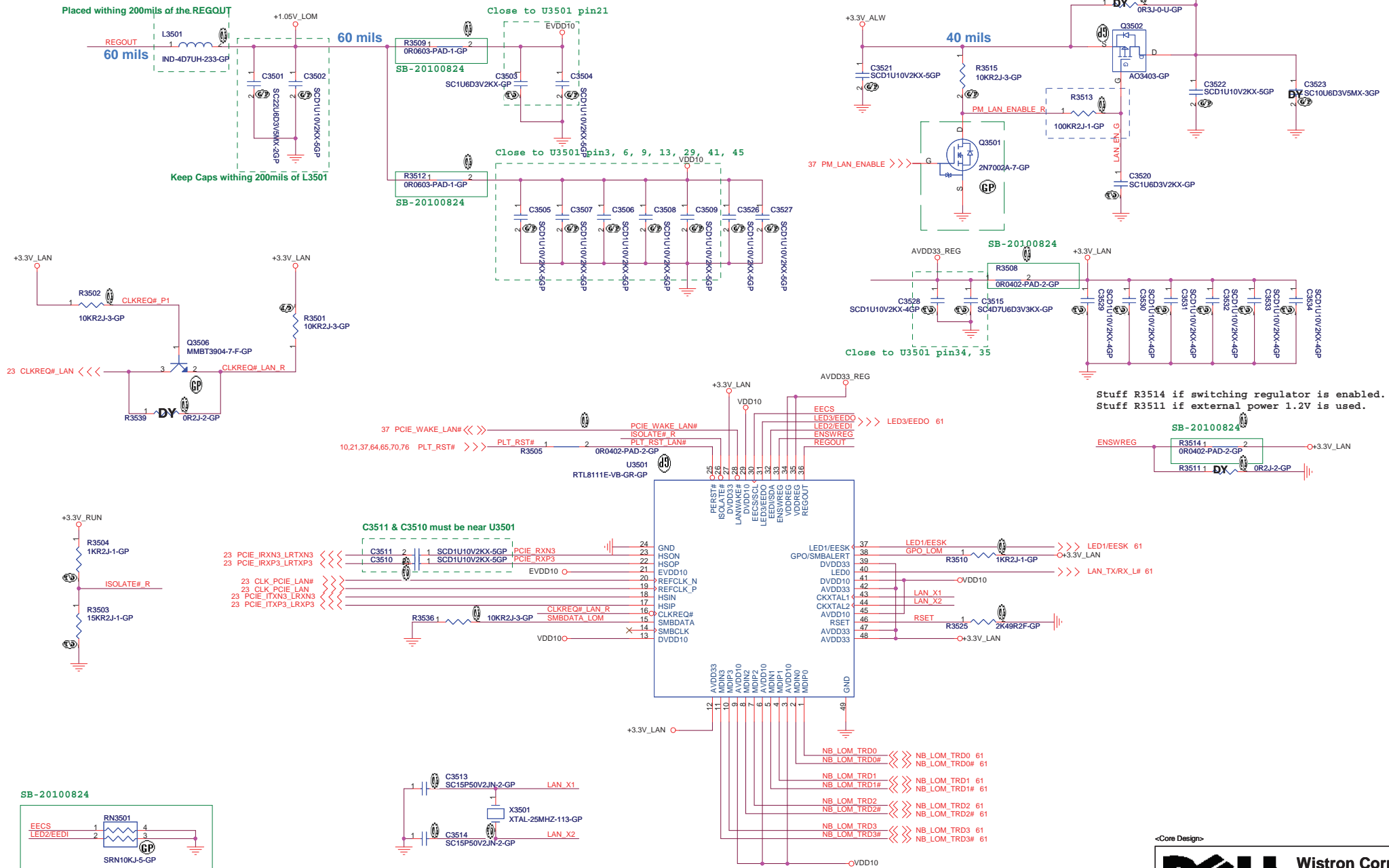
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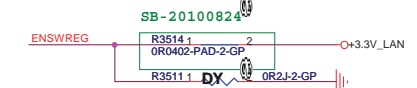
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Title (Reserved)			
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SSID = LOM

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Stuff R3514 if switching regulator is enabled.
Stuff R3511 if external power 1.2V is used.



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Title **(Reserved)**

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Size
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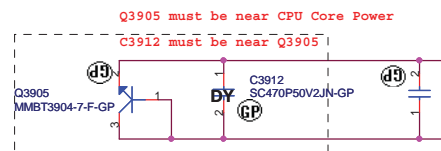
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RYU2 13 UMA

Rev
A00

Date: Tuesday, September 28, 2010

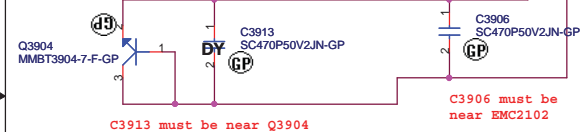
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1. CPU CORE POWER

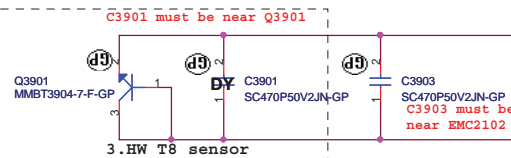


Layout notice:
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

2. System Sensor

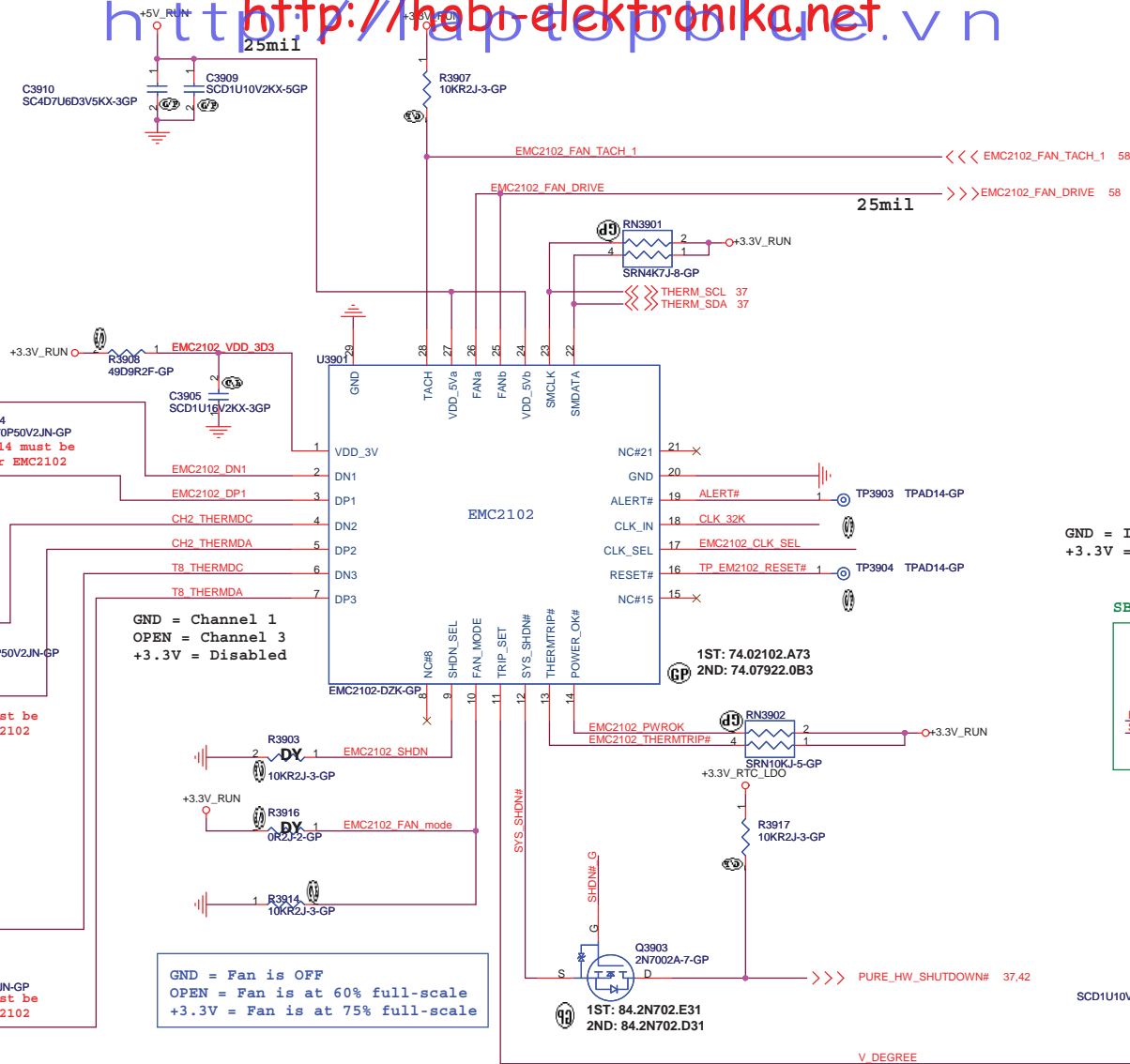
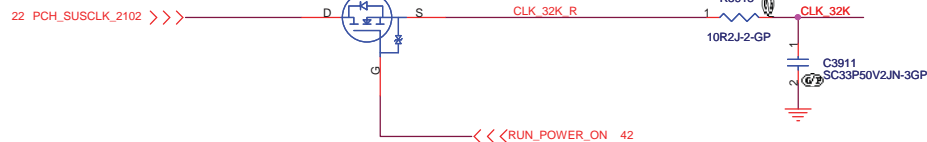


Layout notice :
Both VGA_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing.



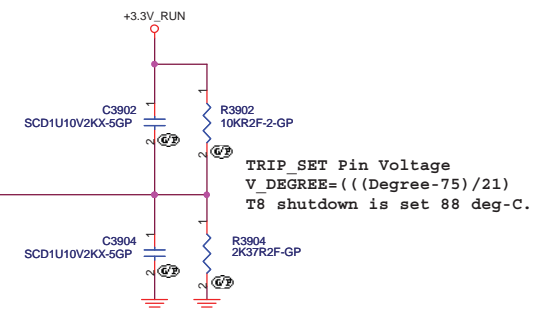
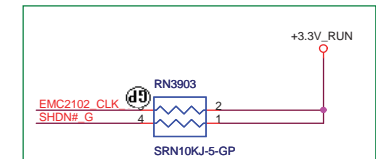
Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

32K suspend clock output



GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

SB-20100824



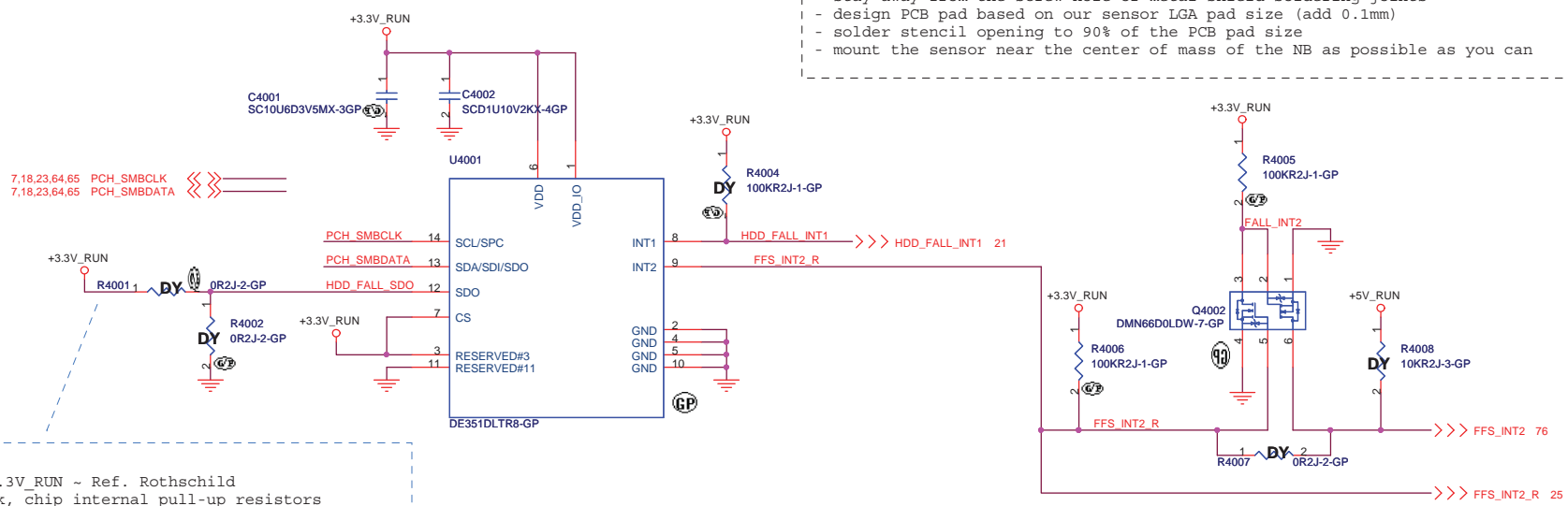
TRIP_SET Pin Voltage
 $V_DEGREE = ((Degree - 75) / 21)$
T8 shutdown is set 88 deg-C.

<Core Design>

Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



09/0422

(#1) Just pull +3.3V_RUN ~ Ref. Rothschild

(#2) FAE/ DY is ok, chip internal pull-up resistors

(#3) From spec, Slave Address(SAD) is 001110xb

Pull HIGH SAD is 0011101b

Pull GND SAD is 0011100b

Note

(1) Keep all signals are the same trace width. (included VDD, GND).

(2) No VIA under IC bottom.

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<Core Design>

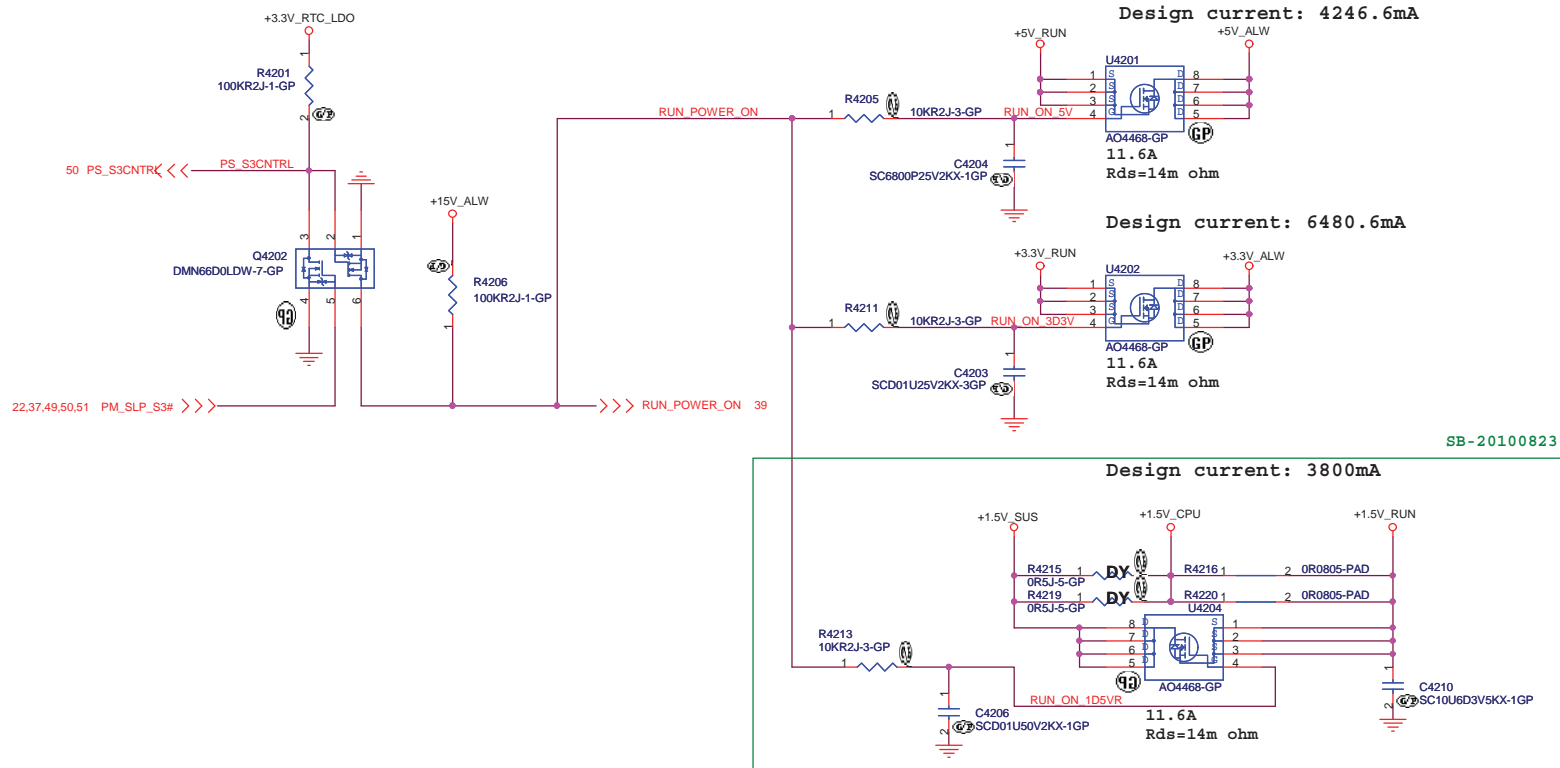
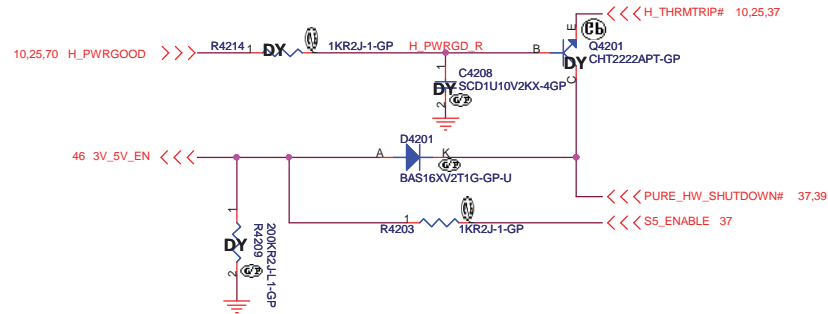


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Title	Author	Date	Page
Title	Author	Date	Page

Power Plane Enable

Size	1
Custom	

Document Number **BYU**

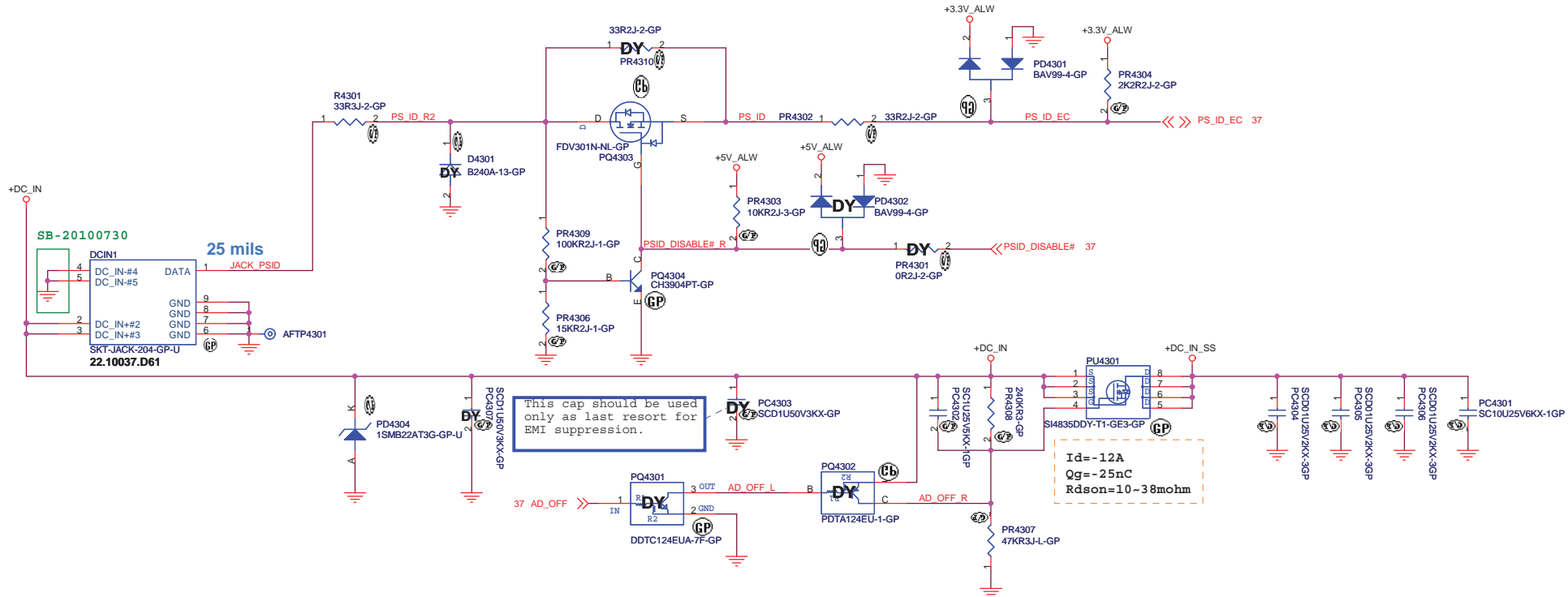
RYU2 13 UMARev
A00

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SSID = DCIN

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<Core Design>



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Batt Connector



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Title

Batt Connector

Size
A4

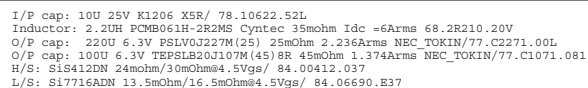
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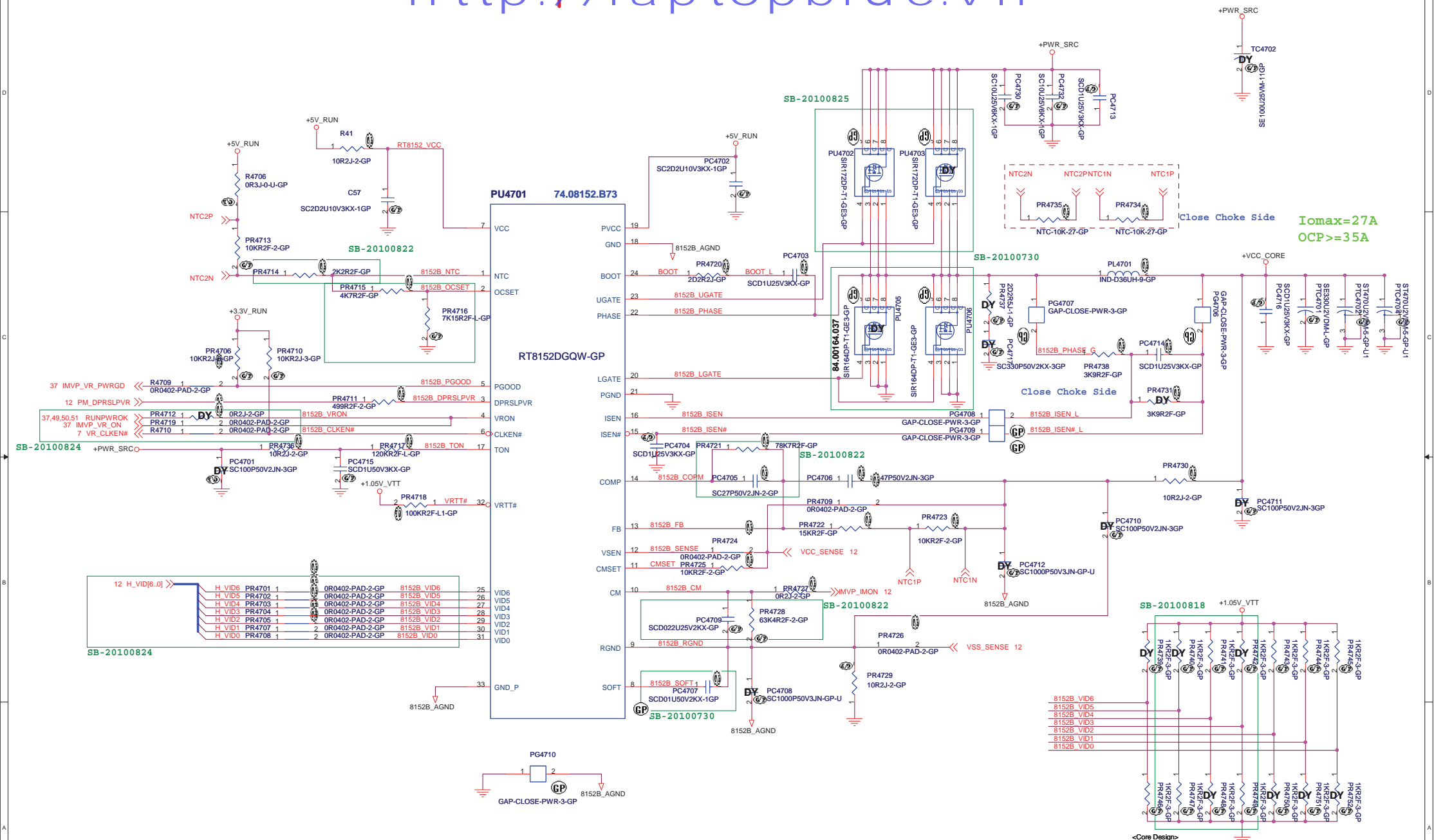
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```
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH PCMB061H-2R2MS Cyntec 35mohm Idc =6Arms 68.2R210.20V
O/P cap: 220U 6.3V PSLV0J22M5(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: S18412DN 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: S17716ADN 13.5mOhm/16.mOhm@4.5Vgs/ 84.06690.E37
```



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: CHOKO 036UH PCMC104T-R36 Cyntec 1.05mohm I_{dc} =30Arms 68.R3610.20C
 O/P cap: EEFLX0D331R EL 330U 2V M.7.3*4.3 6mOhm 3.5Arms PANASONIC/79.33719.2EL
 O/P cap: EL330U2V EEFSX0D331ER 9mOhm 3 Arms PANASONIC/79.33719.L01
 H/S: SI7686DP 10mohm/14mOhm@4.5Vgs/ 84.07686.A37
 L/S: SIR164DP 2.6mOhm/3.2mOhm@4.5Vgs/ 84.00164.037

<Core Design>			
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Size	Document Number	Rev	
Custom	<i>RYU2 13 UMA</i>	<i>A00</i>	
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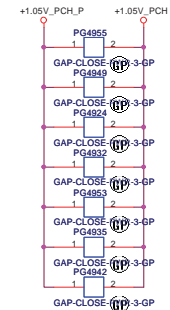
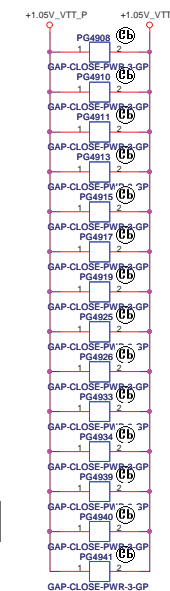
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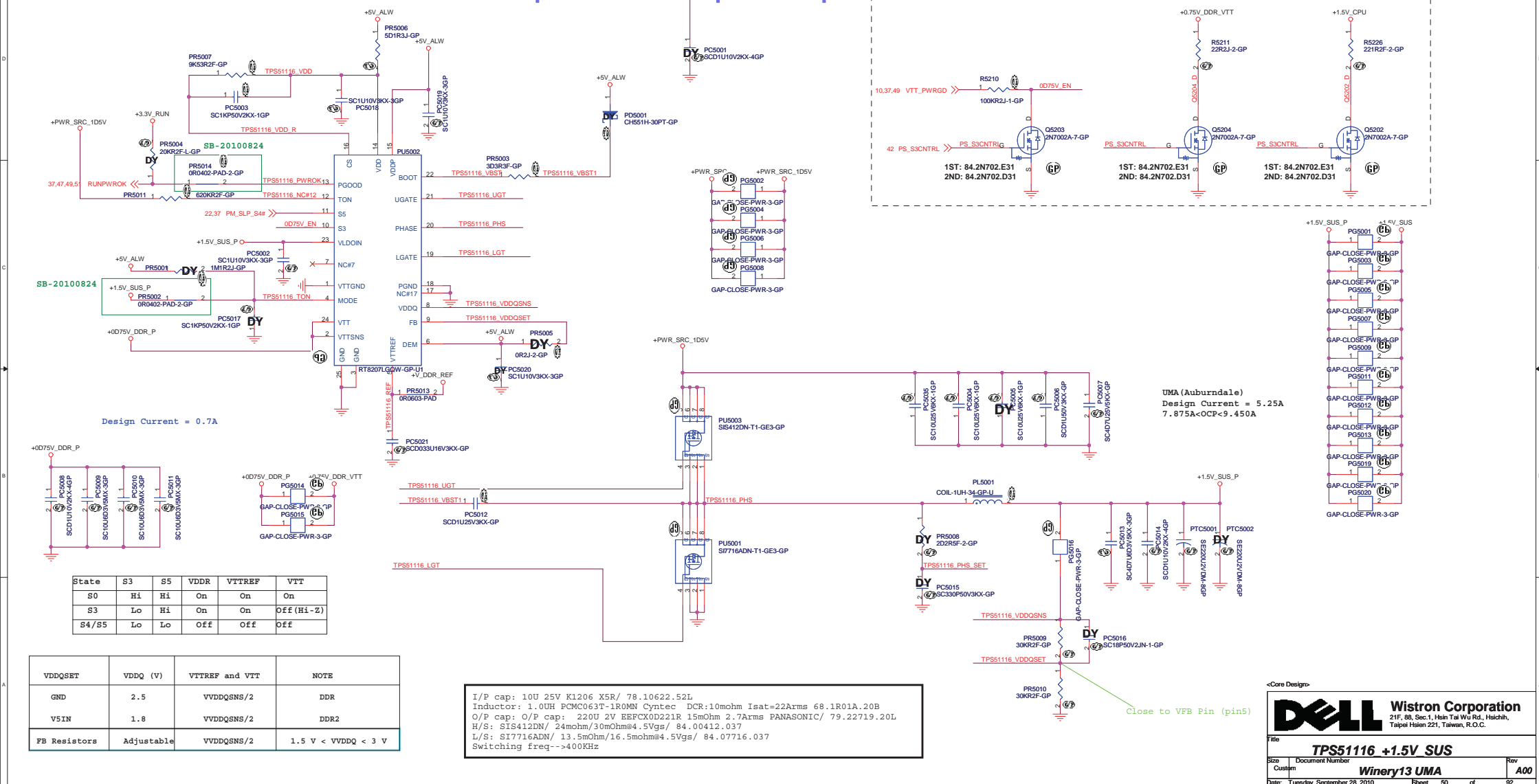


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TI	PR5218, PR5211	PR5217, PR5216
RT	PR5217, PR5216	PR5218, PR5211

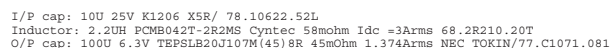
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I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1UH PCMB061H-1R0MS Cyntheq DCR:17mohm Isat =14Arms 68.1R010.20E
O/P cap: 220U 2V EBFXC0221R 15mohm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI8412DN/ 24mohm/30mOhm4.5Vgs/ 84.00412.037
L/S: SI7716ADN/ 13.5mOhm/16.5mohm4.5Vgs/ 84.07716.037
Switching freq-->320KHz
```

$$V_{out} = 0.75V * (R2 + R3) / R3$$

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File	
TPS51218 +1.05V VTT	
Size	Rev
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TPS51311RSGR 1.0V - PUM



Title			
TPS51311 +1.8V RUN			
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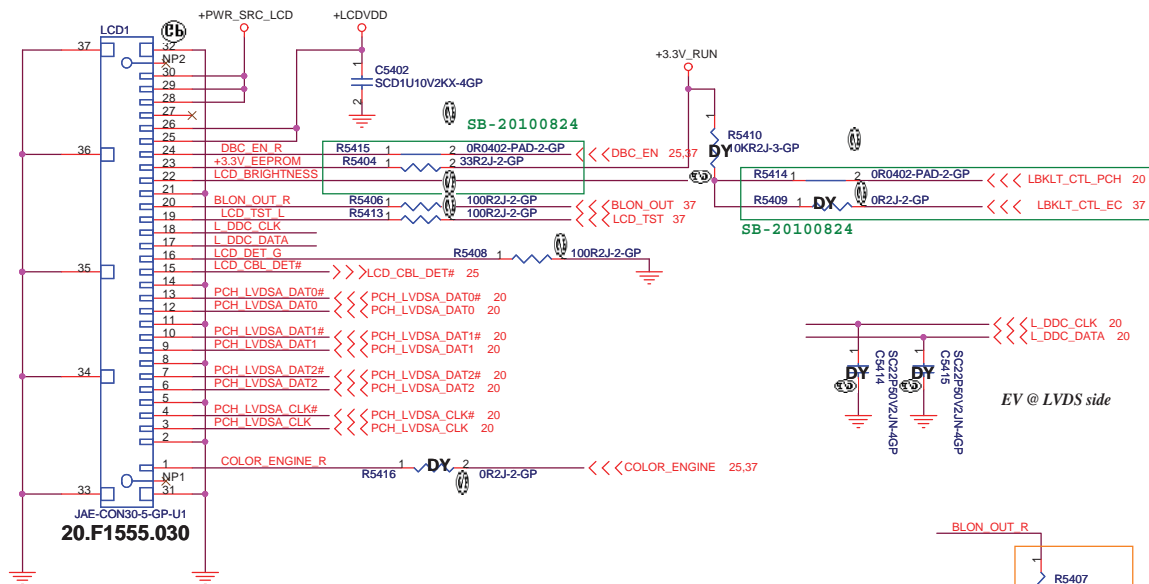
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ADP3211 CPU GFXCORE			
Size	Document Number	Rev	
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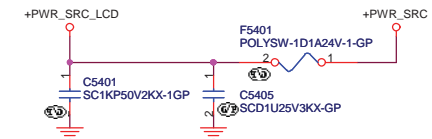
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SSID = Inverter

LVDS CONNECTOR

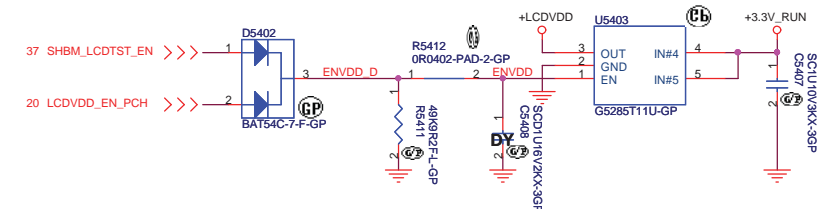
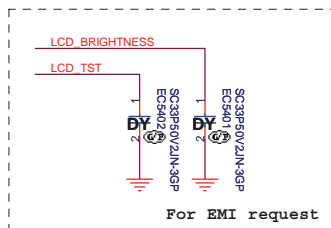
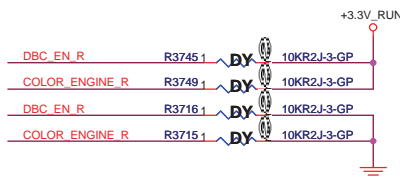
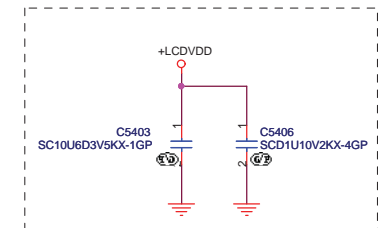


INVERTER POWER



SSID = VIDEO

LCD POWER

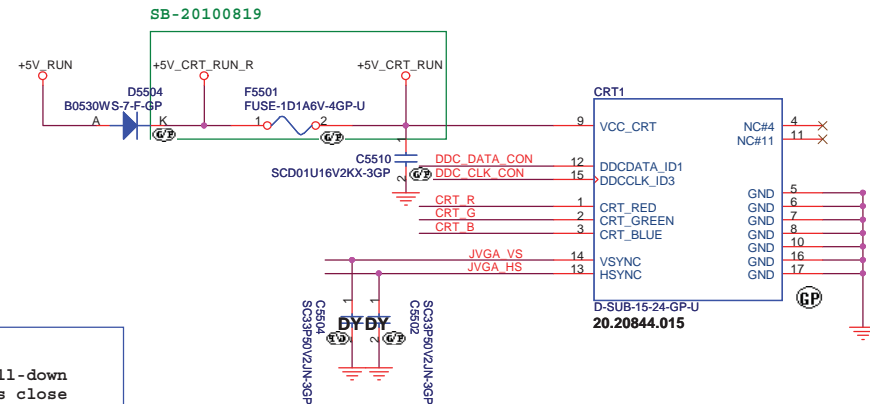


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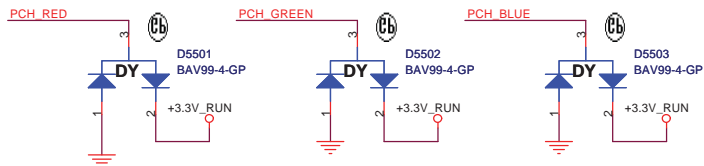


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Title				
LCD/Inverter Connector				
Size	Document Number			Rev
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- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.




The schematic diagram illustrates the CRT section of a monitor, showing the connection of the CRT board to the main board. The diagram includes the following components and connections:

- U5501 and U5502:** 74AHCT1G125GW-1-GP inverters. U5501 is connected to PCH_HSYNC and U5502 is connected to PCH_VSYNC. Both inverters have their OE# pins connected to GND and their VCC pins connected to +5V_CRT_RUN. The Y pins of both inverters are connected to JVGA_HS_R and JVGA_VS_R, which are then connected to JVGA_HS and JVGA_VS via 10R2J-2-GP resistors.
- R5504 and R5505:** 10R2J-2-GP resistors connected in series with the JVGA_HS and JVGA_VS signals.
- EC5501:** A 3.3V regulator (SCD1U10V2KX-4GP) connected to +3.3V_RUN and GND. Its output is connected to the DDC_DATA line.
- Q5517:** A DMN66D0LDW-7-GP MOSFET connected to the DDC_DATA line and the DDC_CLK line.
- SC22PB0V2JN-4GP:** A 5V regulator connected to +5V_CRT_RUN and GND. Its output is connected to the DDC_CLK line.
- 5V @ CRT side:** A 5V regulator (C5520, SC10P50V2JN-4GP) connected to the DDC_CLK line and GND.
- Other components:** R5506 (1KR2F-3-GP) is connected to the OE# pin of U5501 and GND. R5513 (SRN2K2J-1-GP) is connected to the DDC_DATA line and GND.

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Title

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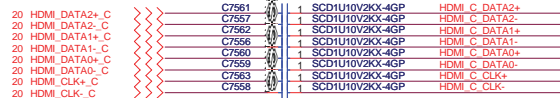
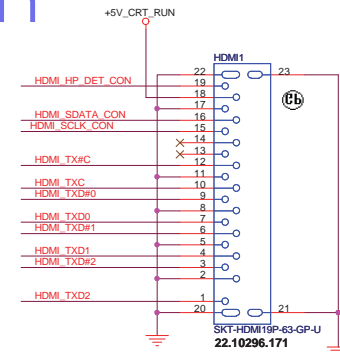
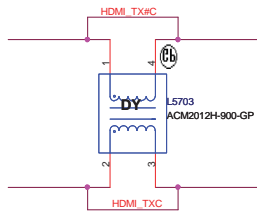
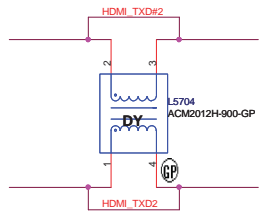
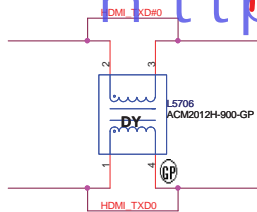
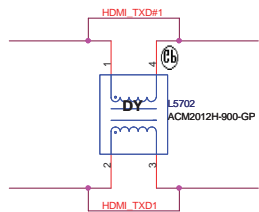
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Rev
A00

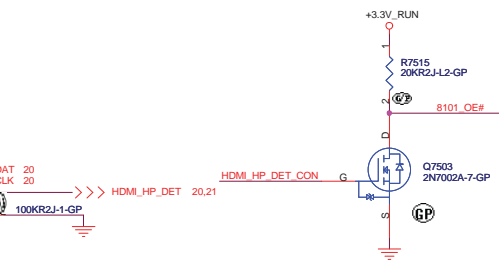
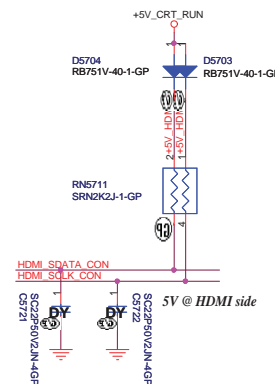
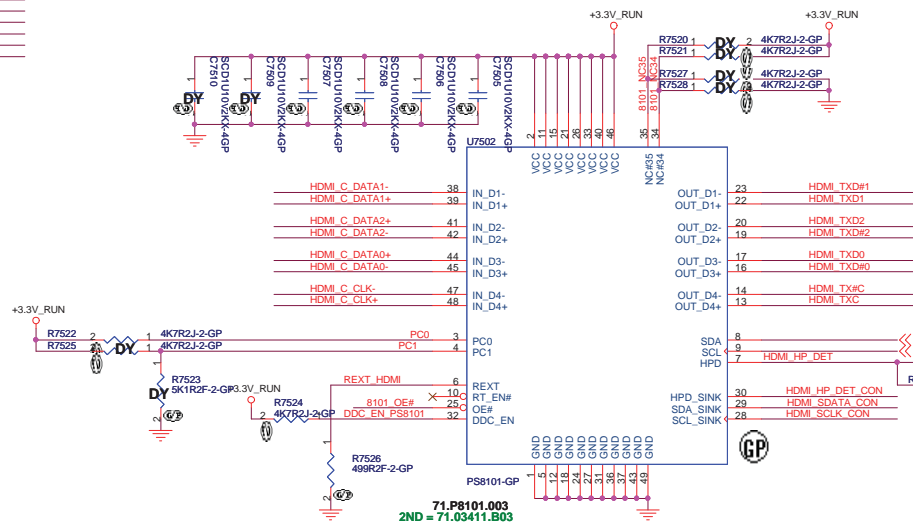
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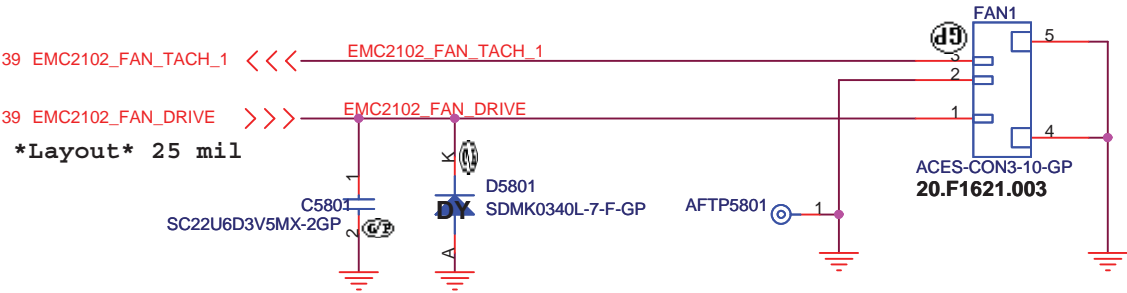
Close to PCH

UMA HDMI level shift circuit




Fan Connector

AFTP5803 1 EMC2102_FAN_TACH_1
AFTP5802 1 EMC2102_FAN_DRIVE



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Title FAN					
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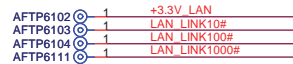
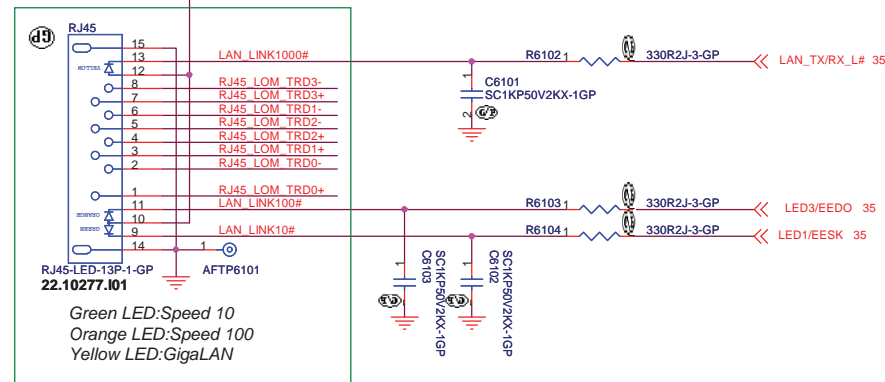
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SSID = LOM

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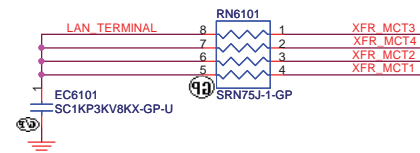
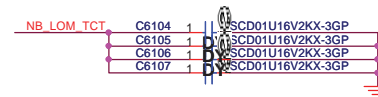
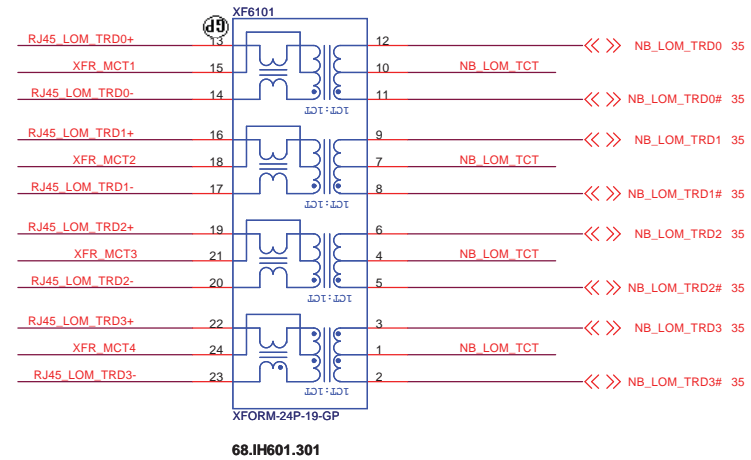
SB-20100823



- 1.Route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.Pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

Off /No link – no light
10Mbps – Green
100Mbps – Orange
1000Mbps – Yellow (Orange/Green Combination)
Activity LED - Separate blinking yellow LED to indicate traffic

10/100/1000M Lan Transformer



<Core Design>



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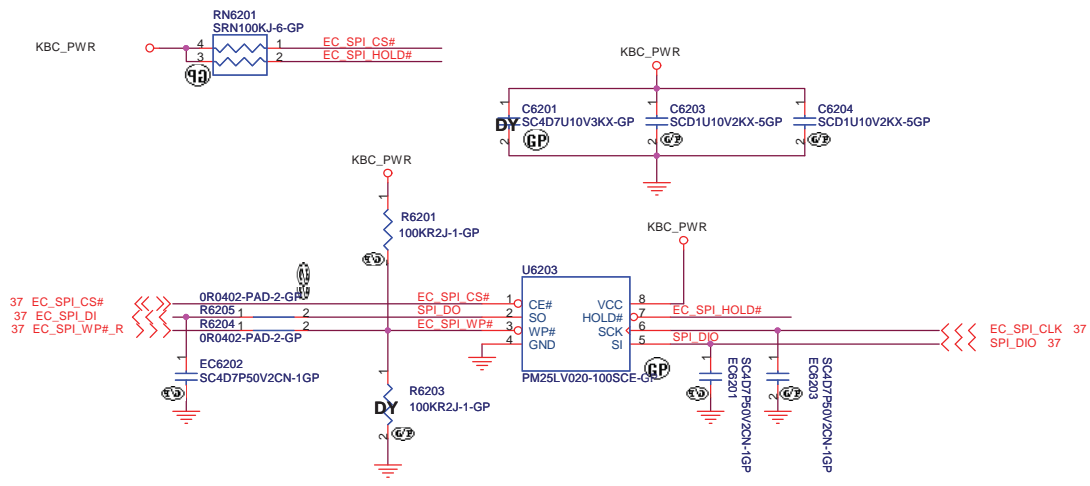
Title				
RJ45/Transformer				
Size	Document Number			Rev
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SSID = Flash.ROM

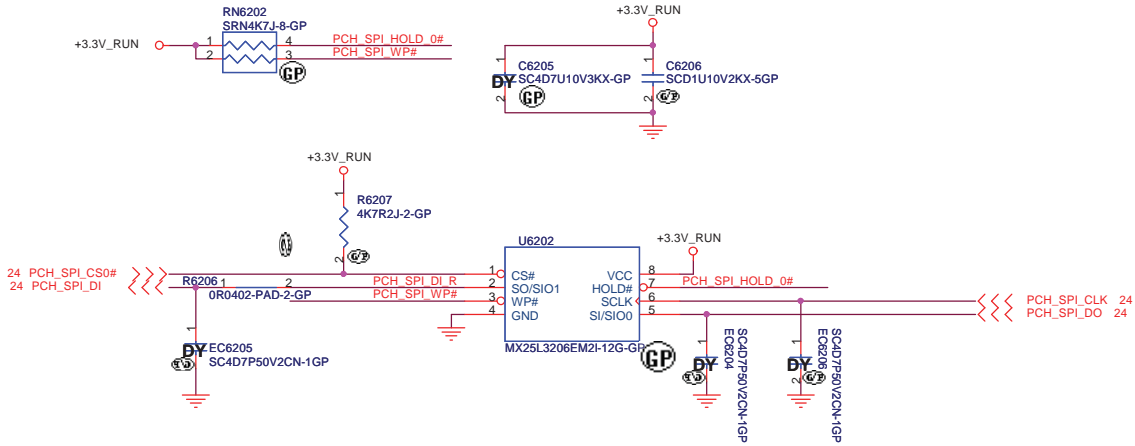
http://hobi-elektronika.net

SSID = PBATT

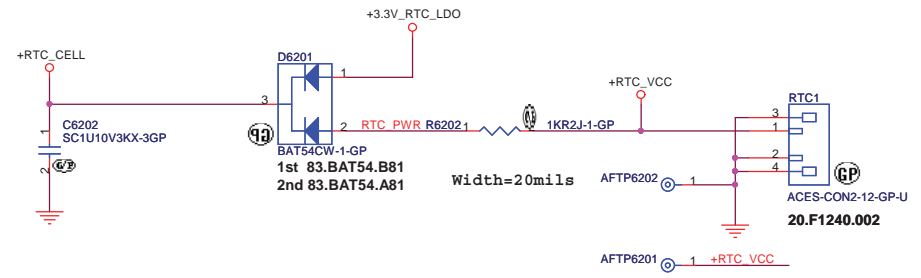
SPI FLASH ROM (2M bits) for KBC



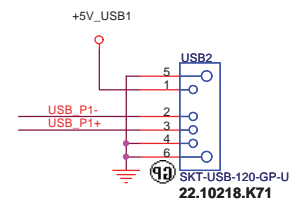
SPI FLASH ROM (32M bits) for PCH



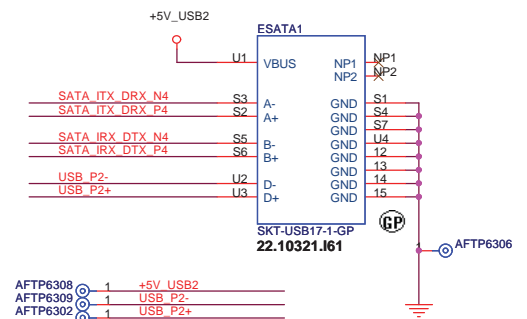
RTC Connector



<http://hobi-elektronika.net>



SB-20100824



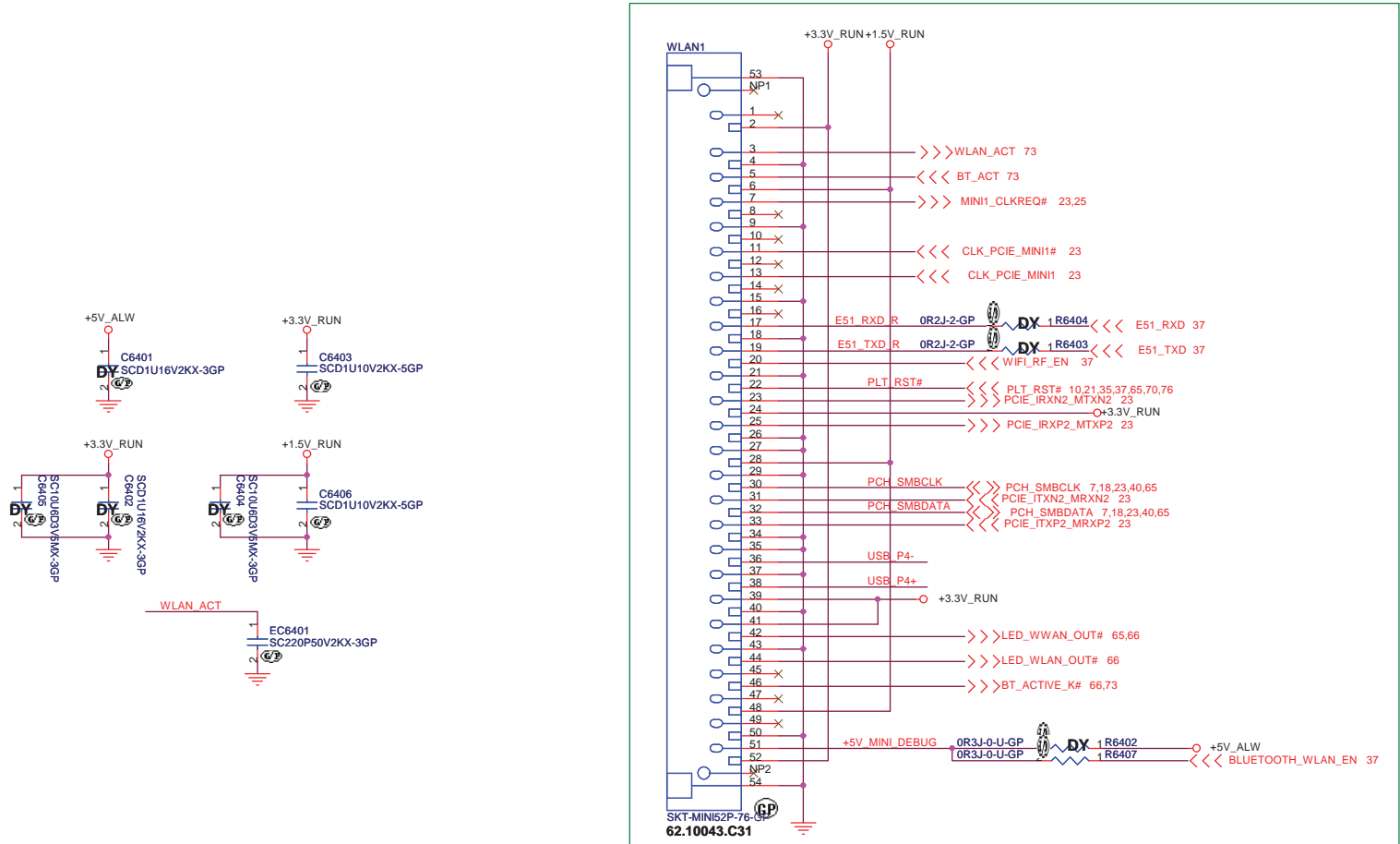
SB-20100824



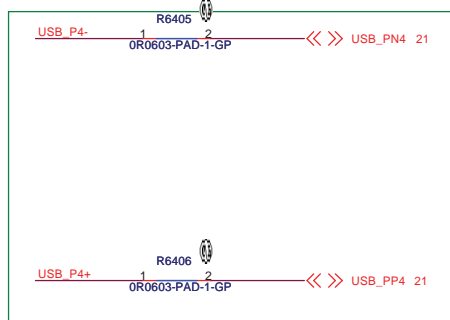
SSID = Wireless

http://laptopproline.vn

SB-20100823



SB-20100825

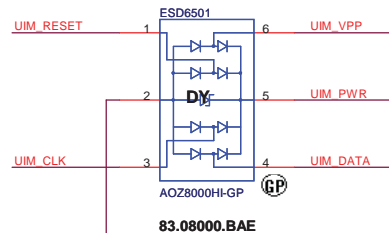
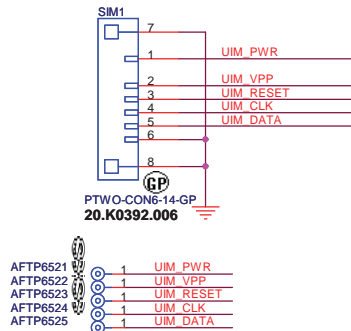
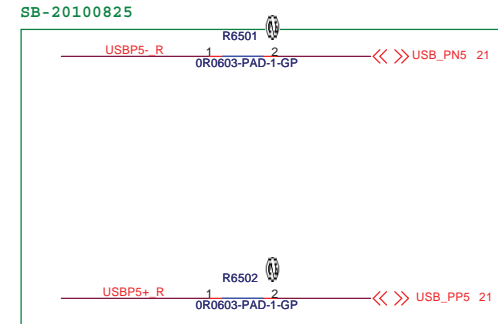
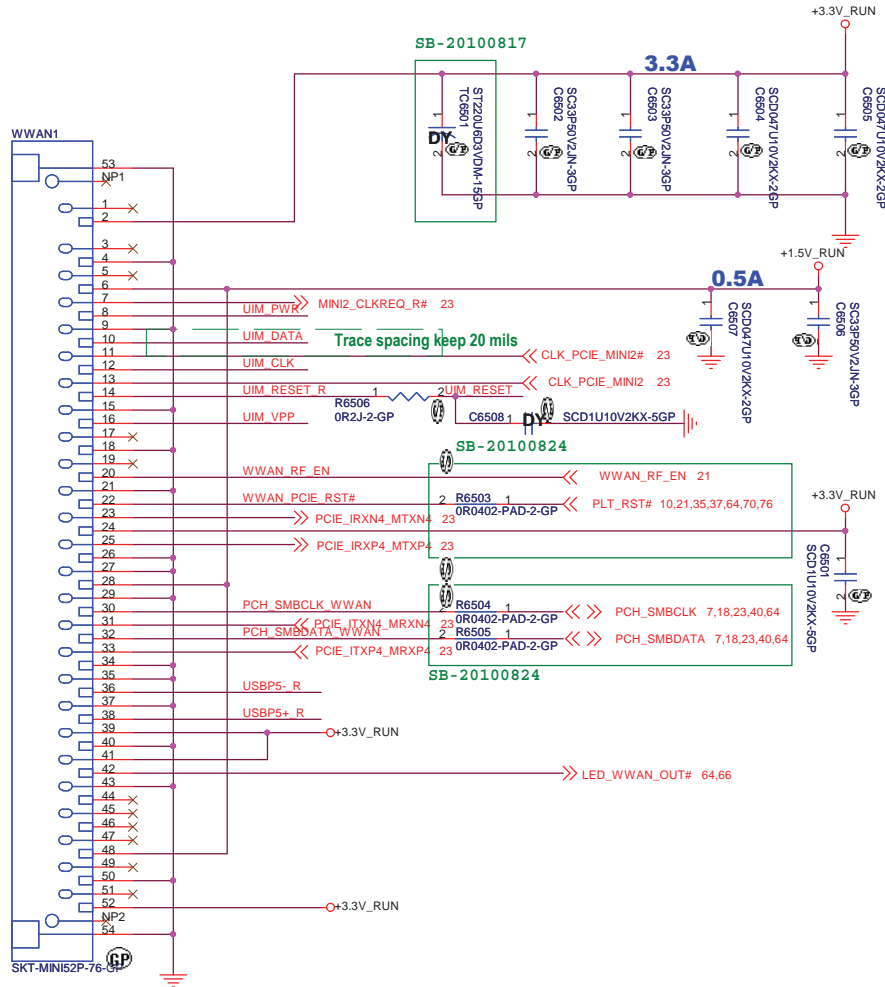


SSID = WWAN

Layout note: Place caps C6501-C6507, TC6501 close WWAN1 connector.

http://hobi-elektronika.net

MiniCard WWAN connector



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Title

WWAN Connector

Size

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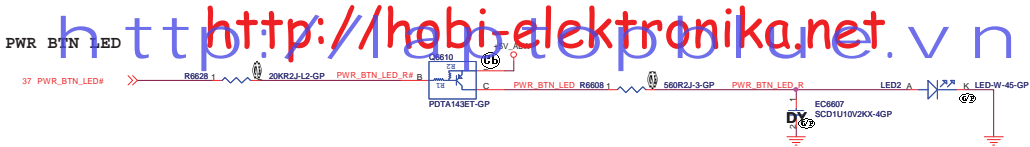
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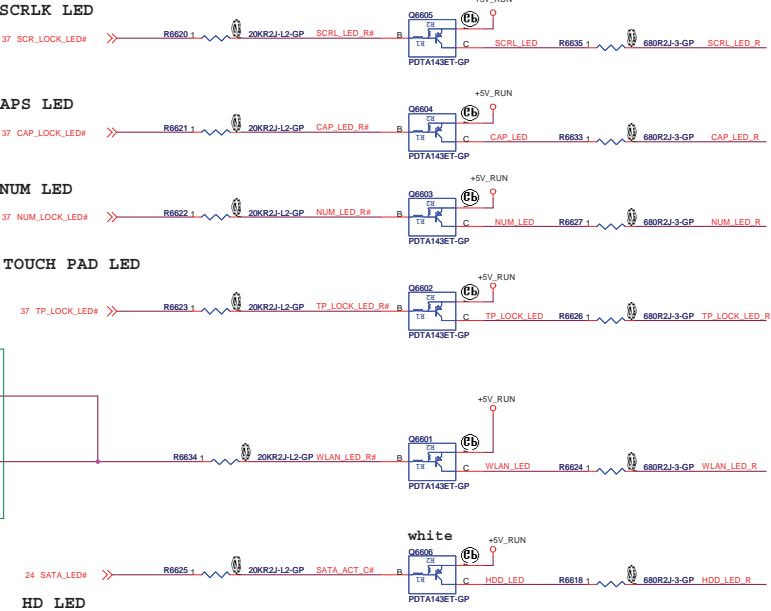
SSID = LED

For LED & Capacity board:

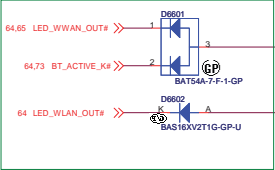
LED Type	Color	Power rail
BATTERY LED1	Amber(Multi-color)	ALW
SCRLL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WLAN/WWAN ACT LED	White	RUN



LED Board to Board

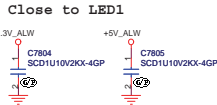
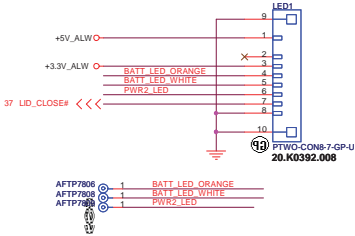
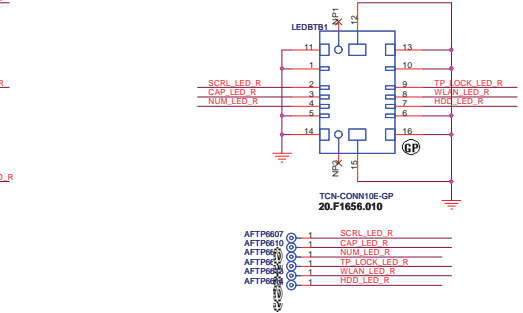
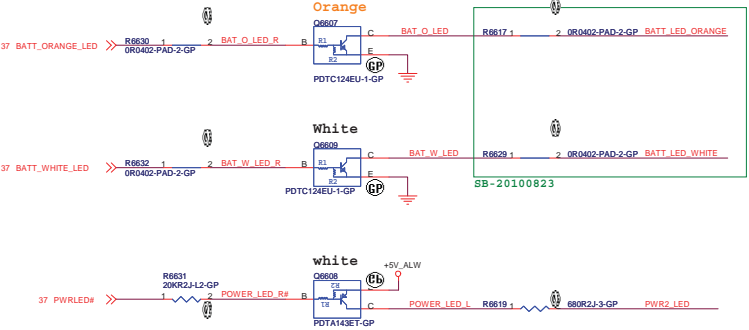


WLAN WIMAX LED Bluetooth LED WWAN LED




SB-20100822

External LED



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<Core Design>

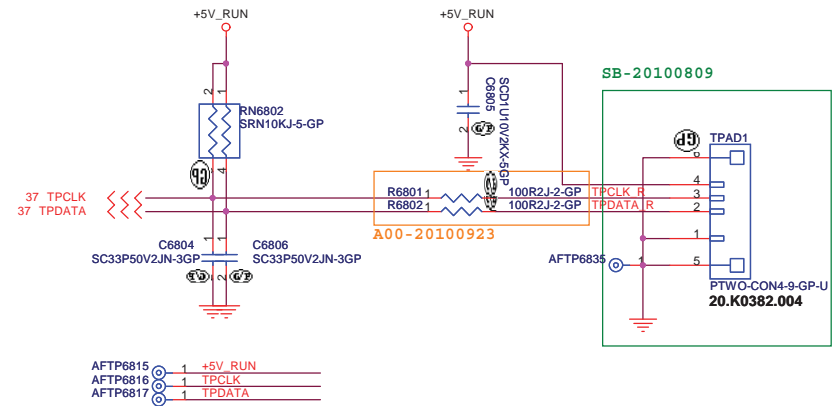
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Title (Reserved)			
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4 3 2

h t t p : // h o b i - e l e k t r o n i k a . n e t


SSID = Touch Pad

SSD = Tough Pad

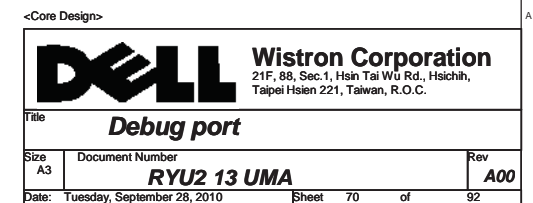


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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>Hall sensor</i>			
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<http://hobi-elektronika.net>
GOLDEN FINGER FOR DEBUG BOARD



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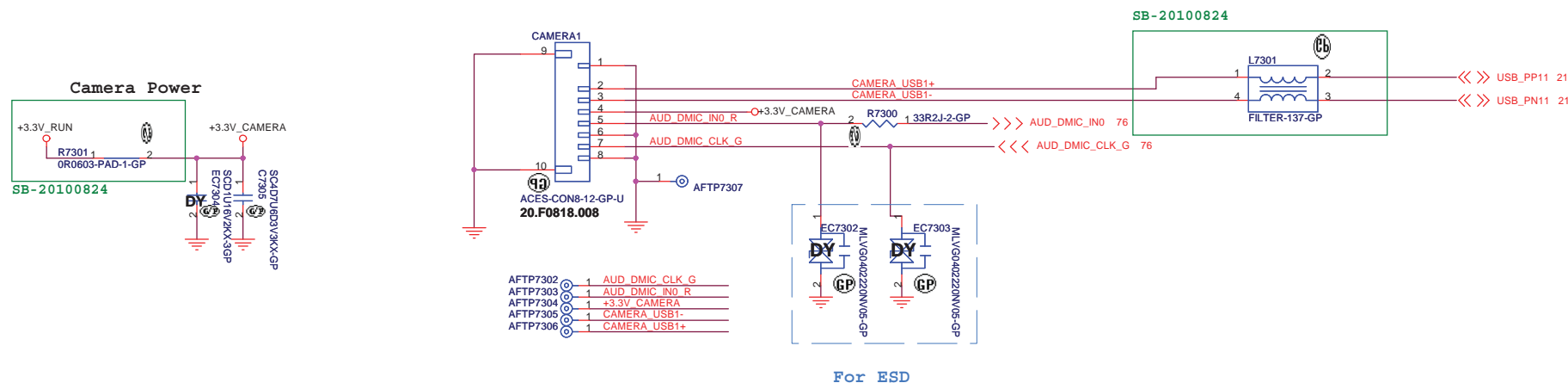
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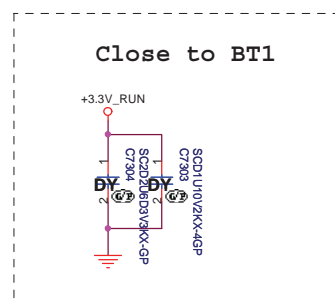
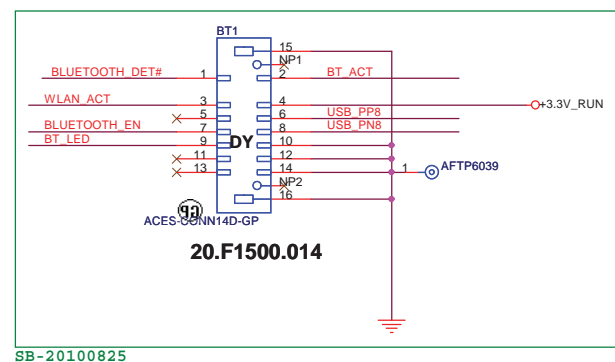
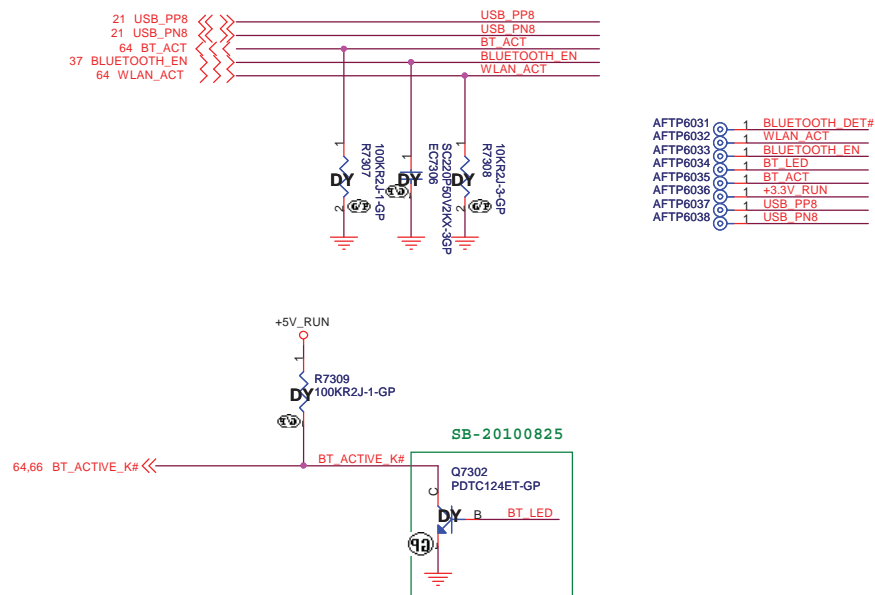
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<http://hobi-elektronika.net>



```
SSID = User.Interface
```

Bluetooth cable conn.



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DELL

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Title

Camera CONN

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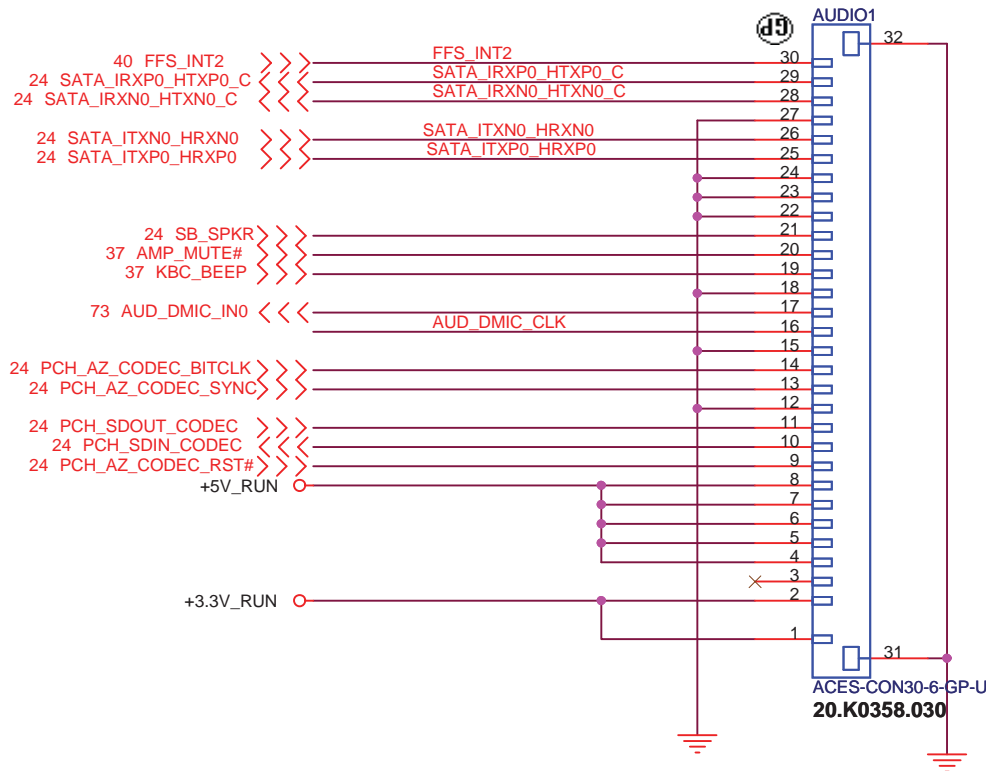
Wistron Corporation
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Title

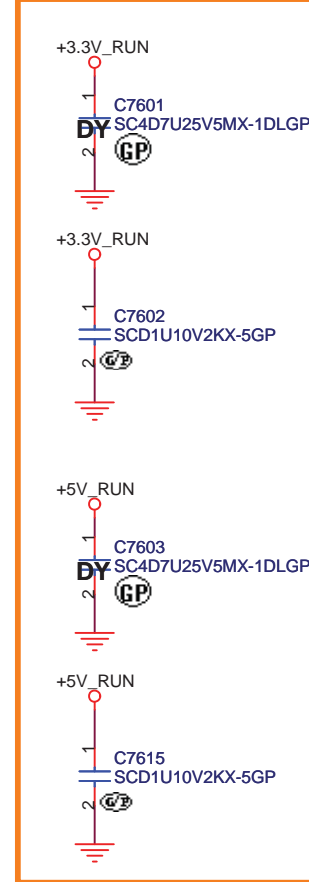
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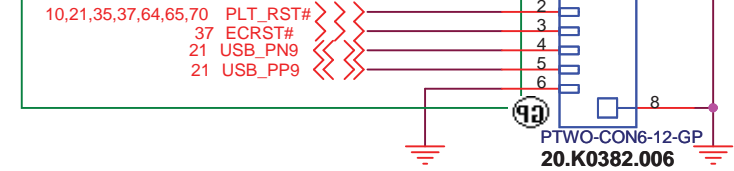
Audio board CONN



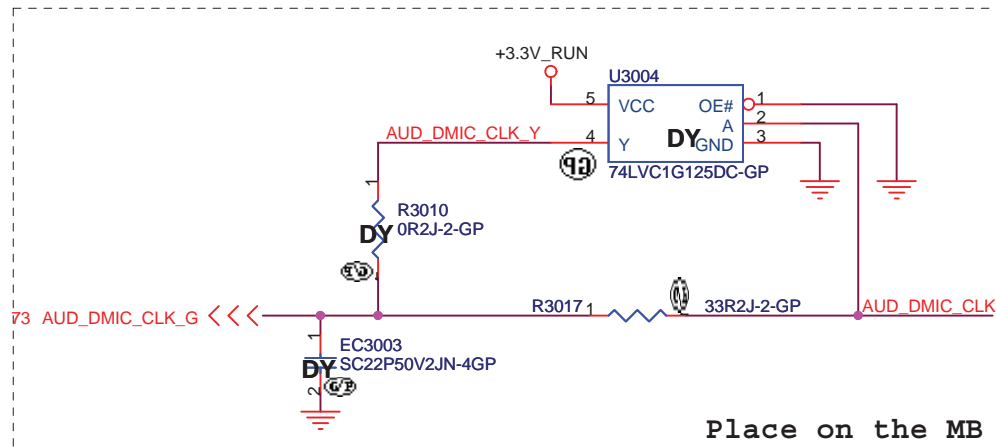
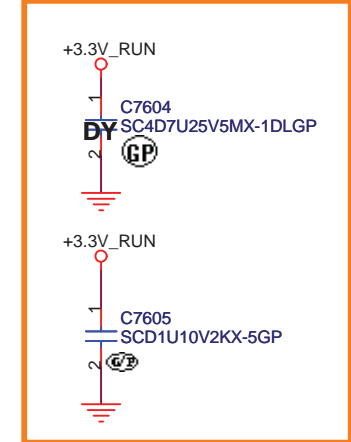
Place near AUDIO1



SB-20100817



Place near CARD1



Place on the MB

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Title **DC_IN Board BTB Connector**

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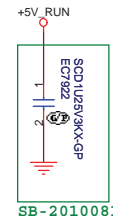
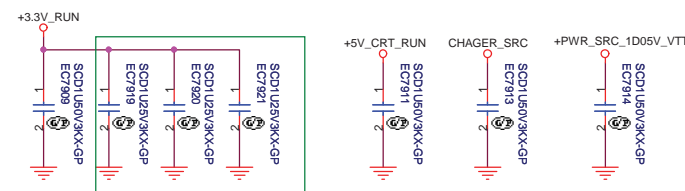
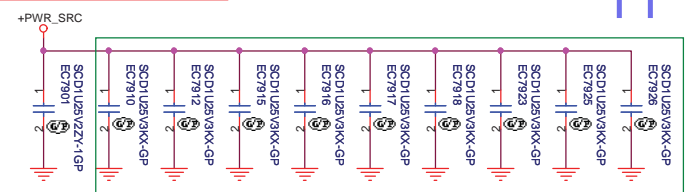
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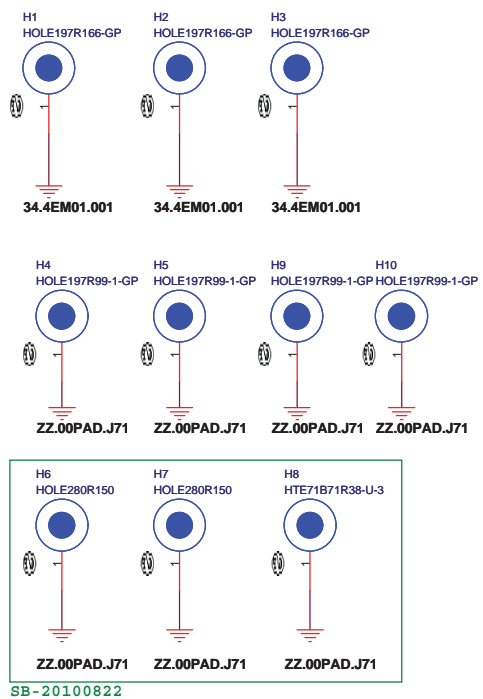
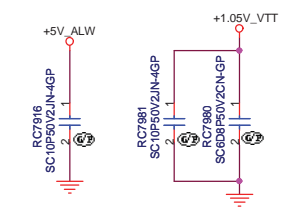
SSID = EMI

http://hobi-elektronika.net

SSID = Mechanical



SSID = RF



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Title

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Title

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Size
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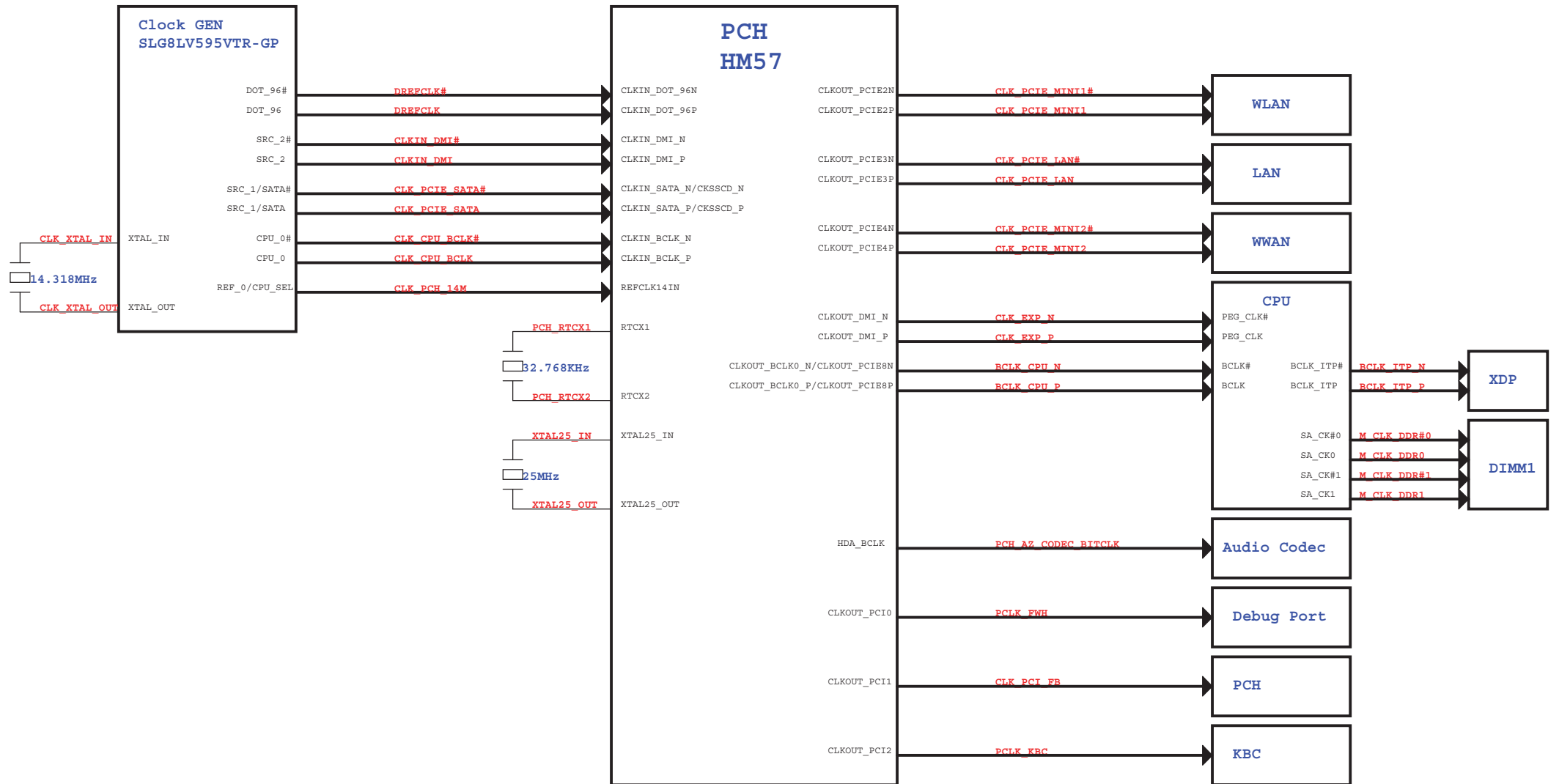
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Item	Page#	Date	Request By	Issue Description	Solution Description	Rev.
1	43	2010/07/30	EE	+DC_IN short to GND	Modify DCIN1 connector pin4, pin5 connect to GND.	SB
2	37	2010/07/30	EE	SW1 always short to GND.	Change pin 6 connect to GND.	SB
3	68	2010/08/09	EE		Change TPAD1 pin defined.	SB
4	68	2010/08/13	EE		Change KB1 connector to 20.K0320.030.	SB
5	76	2010/08/17	EE		Add ECRST# connect to CARD1 pin 3.	SB
6	79	2010/08/17	EMI		Between +PWR_SRC and GND add 0.1uf/50v cap X 9. Between +3.3V_RUN and GND add 0.1uf/50v cap X 3. Between +5V_RUN and GND add 0.1uf/50v cap X 1. Between +DC_IN and GND add 0.1uf/50v cap X 1. Between +DC_IN and GND add 0.1uf/50v cap.	SB
7	47	2010/08/18	Power		Change +VCC_CORE VID3~5 from 001 to 010.	SB
8	37	2010/08/19	EE		Add LID_CLOSE# pull high resistor to +3.3V_ALW.	SB
9	51	2010/08/19	EE		Co-lay +1.8V_RUN LDO power solution.	SB
10	55	2010/08/19	EE		Between +5V_RUN and +5V_CRT_RUN add Fuse.	SB
11	45	2010/08/22	ME		Change PC4532, PC4530, PC4533 from 1206 size to 0805 size for ME request.	SB
12	45	2010/08/22	Power		Change PU4505 from SIS7716 to SIS412DN (84.00412.037). For cost down.	SB
13	47	2010/08/22	Power		PR4714 change to 2.2K for OTP & OCP setting. PR4715 change to 4.7K for OTP & OCP setting. PR4716 change to 7.15K for OTP & OCP setting. PR4721 change to 78.7K for Load Line & COMP setting. PC4705 change to 27pF for Load Line & COMP setting. PR4728 change to 63.4K for Current Monitor setting. PC4709 change to 22nF for Current Monitor setting.	SB
14	66	2010/08/22	EE		Add D6601, D6602 for wireless function.	SB
15	7	2010/08/23	RF		Add RC701, RC702 for RF request.	SB
16	42	2010/08/23	EE		Change +1.5V_CPU power rail from +1.5V_RUN to +1.5V_SUS.	SB
17	53	2010/08/23	Power		PR5314 :7.5k change to 8.45K(64.84515.6DL) for GFX core imon.	
18	61	2010/08/23	EE		Change RJ45 connector to 22.10277.I01 for hi-port fail.	SB
19	64,65	2010/08/23	EE		Change WLAN1, WWAN1 connector to 62.10043.C31.	SB
					<div> <div>Core Design</div> <div>  <div> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div> </div> <div> <div>Title</div> <div>Change List(1/3)</div> </div> <div> <div>Size A3</div> <div>Document Number RYU2 13 UMA</div> <div>Rev A00</div> </div> <div> <div>Date: Tuesday, September 28, 2010</div> <div>Sheet 88 of 89</div> </div> </div>	



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Title

Clock Block Diagram

Size
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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
20	66	2010/08/23	EE		Change R6617, R6629 to 0ohm.	SB
21	63,73	2010/08/24	EMI		Change USB port0, port1, port2 and camera from 0 ohm to common chock.	SB
22	73	2010/08/25	EE		Dummy BT 365 function.	SB
23	24	2010/08/25	EE		Change C2402 from 12PF to 5PF.For Vendor recommend. Change C2403 from 12PF to 6PF.For Vendor recommend.	SB
24	7	2010/08/25	EE		Change C714, C715 from 12PF to 15PF for vendor recommend.	SB
25	47,49	2010/08/25	Power	SI7686DP-T1-GE3-GP will EOL.	PU4702, PU4703, PU4902: (SI7686DP-T1-GE3-GP) change to SIR172DP-T1-GE3-GP 84.00172.037	SB
<div><Core Design>  Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. Title: Change List(1/3) Size: A3 Document Number: RYU2 13 UMA Rev: A00 Date: Tuesday, September 28, 2010 Sheet 90 of 89</div>						

Item	Page#	Date	Request By	Issue Description	Solution Description	Rev.
1	7	2010/08/24	EE	Cost down	Change R708, R709, RN701, RN702, RN703, RN704 from 0 ohm to short pad.	SB
2	10	2010/08/23	EE	Cost down	Dummy U927, R989, R977, Q901, C915, R934, R989. Add R935, R919. Change R920 to 3 K ohm.	SB
3	10	2010/08/24	EE	Cost down	Change R906, R909, R921, R924, R926 from 0 ohm to short pad.	SB
4	20	2010/08/24	EE	Cost down	Change R2011 from 0 ohm to short pad.	SB
5	21	2010/08/24	EE	Cost down	Change R2104, R2121 from 0 ohm to short pad.	SB
6	21	2010/08/24	EE	Cost down	Change R2519, R2102, R2105 from single resistor to array resistor.	SB
7	22	2010/08/24	EE	Cost down	Change R2207, R2210, R2218, R2213, R2216, R2219, R2220, R2211, R2212 from 0 ohm to short pad.	SB
8	23	2010/08/24	EE	Cost down	Change RN2311, RN2312, RN2314 from 0 ohm to short pad.	SB
9	23	2010/08/24	EE	Cost down	Change R2302, R2201, R2301, R2209 from single resistor to array resistor.	SB
10	24	2010/08/24	EE	Cost down	Change R2417 from 0 ohm to short pad.	SB
11	25	2010/08/24	EE	Cost down	Change R2521, R2334, R2522, R2512, R2411, R2513, R2217, R2538, R2304, R2533, R2416, R2503, R2535, R2214 from single resistor to array resistor.	SB
12	26	2010/08/24	EE	Cost down	Change R2606, R2605, R2601, R2609, R2602 from 0 ohm to short pad.	SB
13	27	2010/08/24	EE	Cost down	Change R2707 from 0 ohm to short pad.	SB
14	35	2010/08/24	EE	Cost down	Change R3509, R3512, R3508, R3514 from 0 ohm to short pad.	SB
15	35	2010/08/24	EE	Cost down	Change R3517, R3518 from single resistor to array resistor.	SB
16	37	2010/08/24	EE	Cost down	Change R3706, R3730, RR3720, R3707, R3753, R3702, R3723, R3727 from 0 ohm to short pad.	SB
17	37	2010/08/24	EE	Cost down	Change R3742, R3743 from single resistor to array resistor.	SB
18	39	2010/08/24	EE	Cost down	Change R3910, R3906 from single resistor to array resistor.	SB
19	44	2010/08/24	EE	Cost down	Change R4401 from 0 ohm to short pad.	SB
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