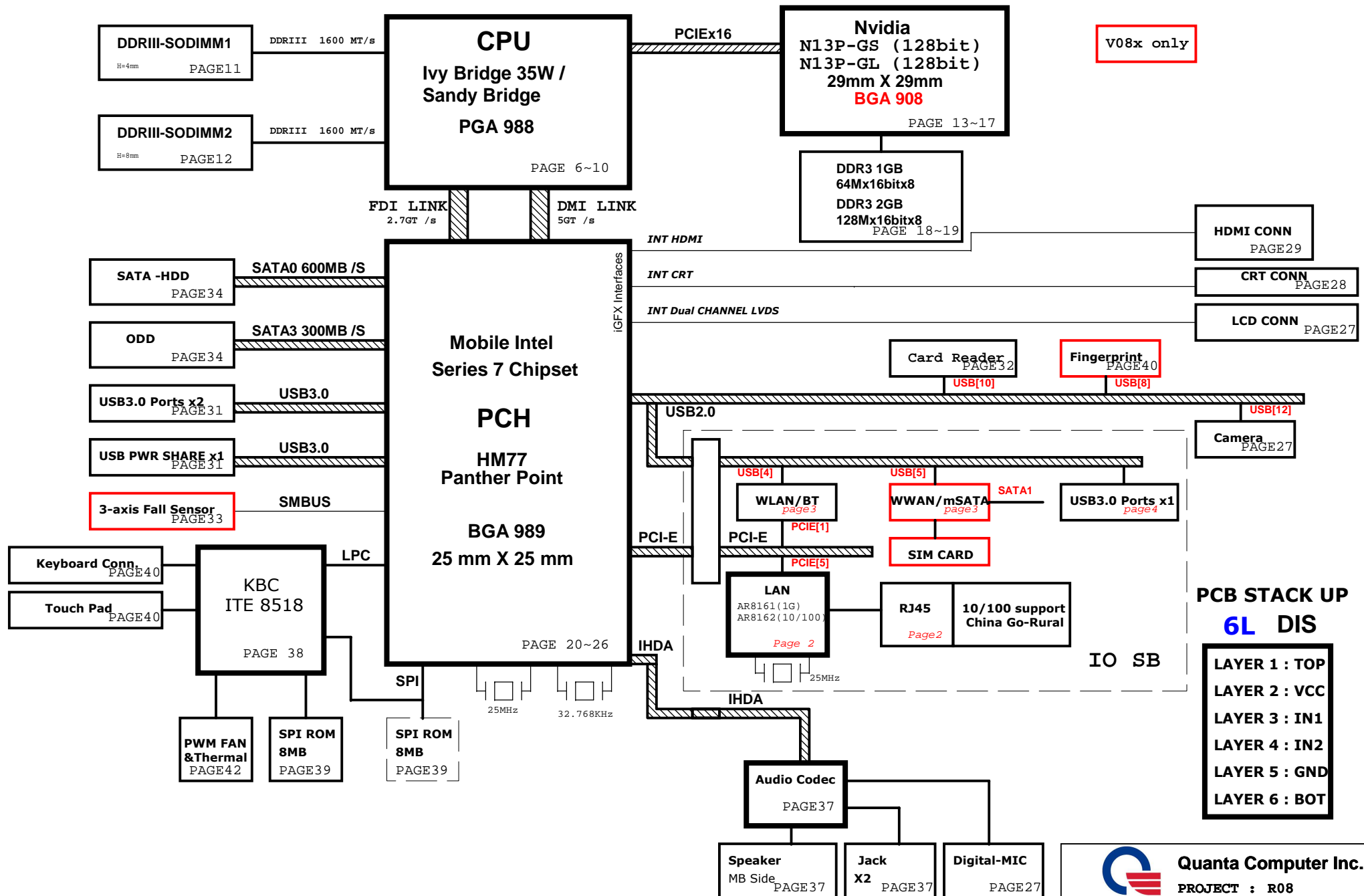
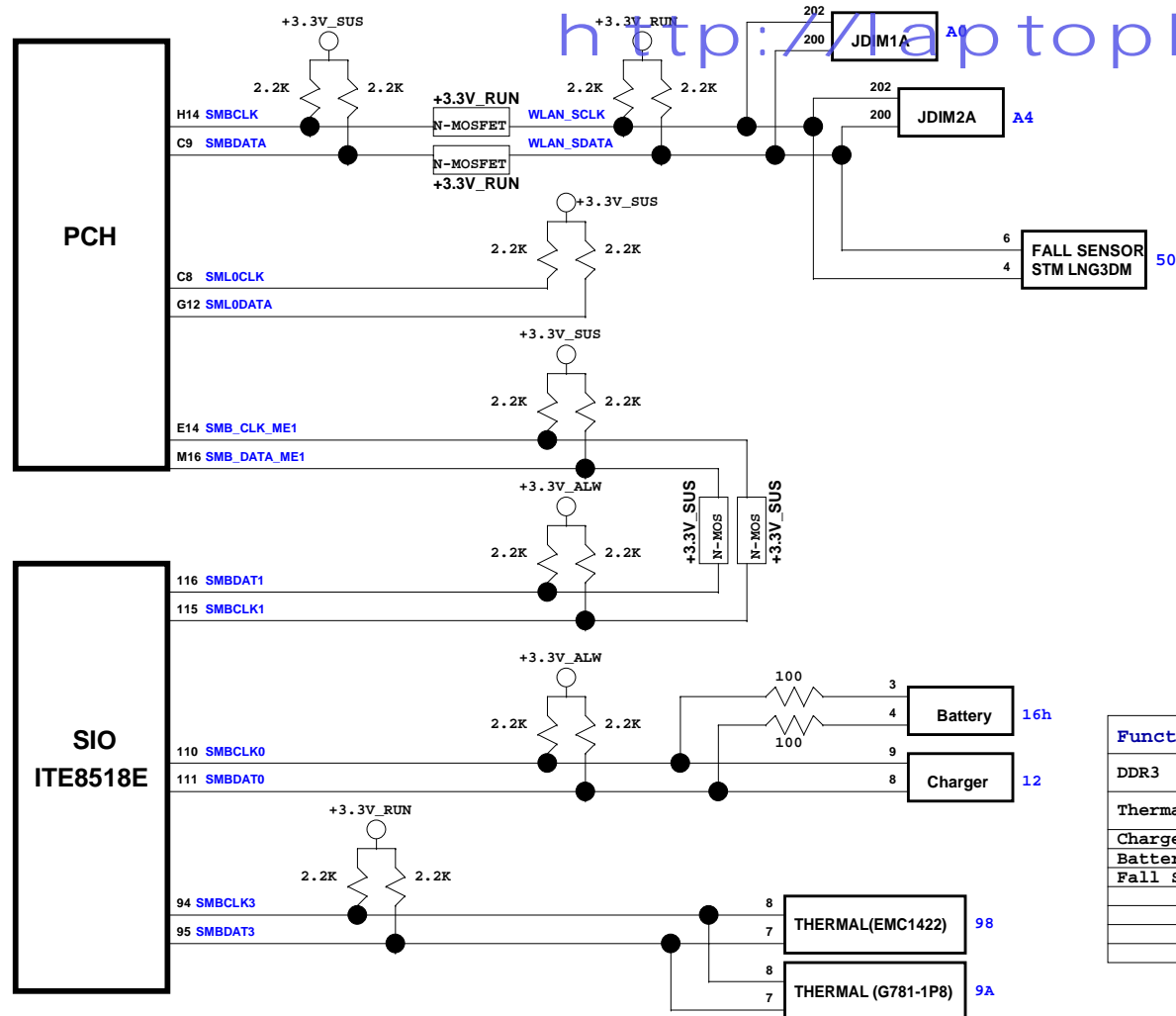


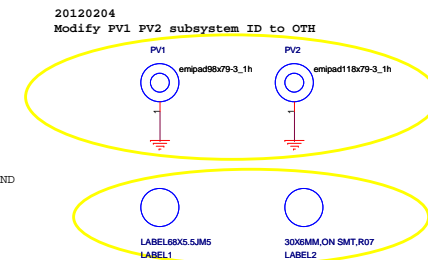
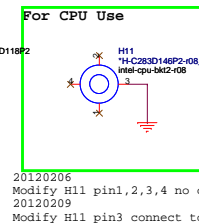
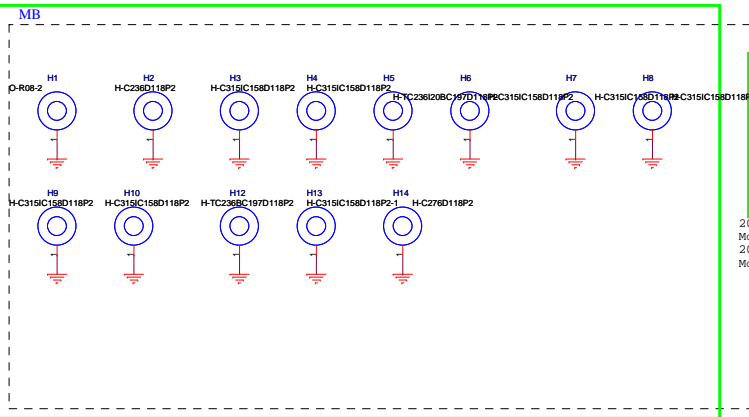
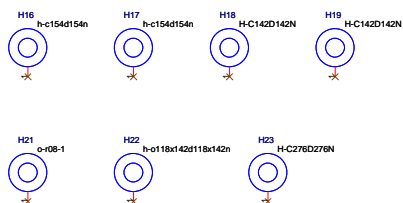
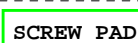
R08/V08 BLOCK DIAGRAM



Quanta Computer Inc.
PROJECT : R08



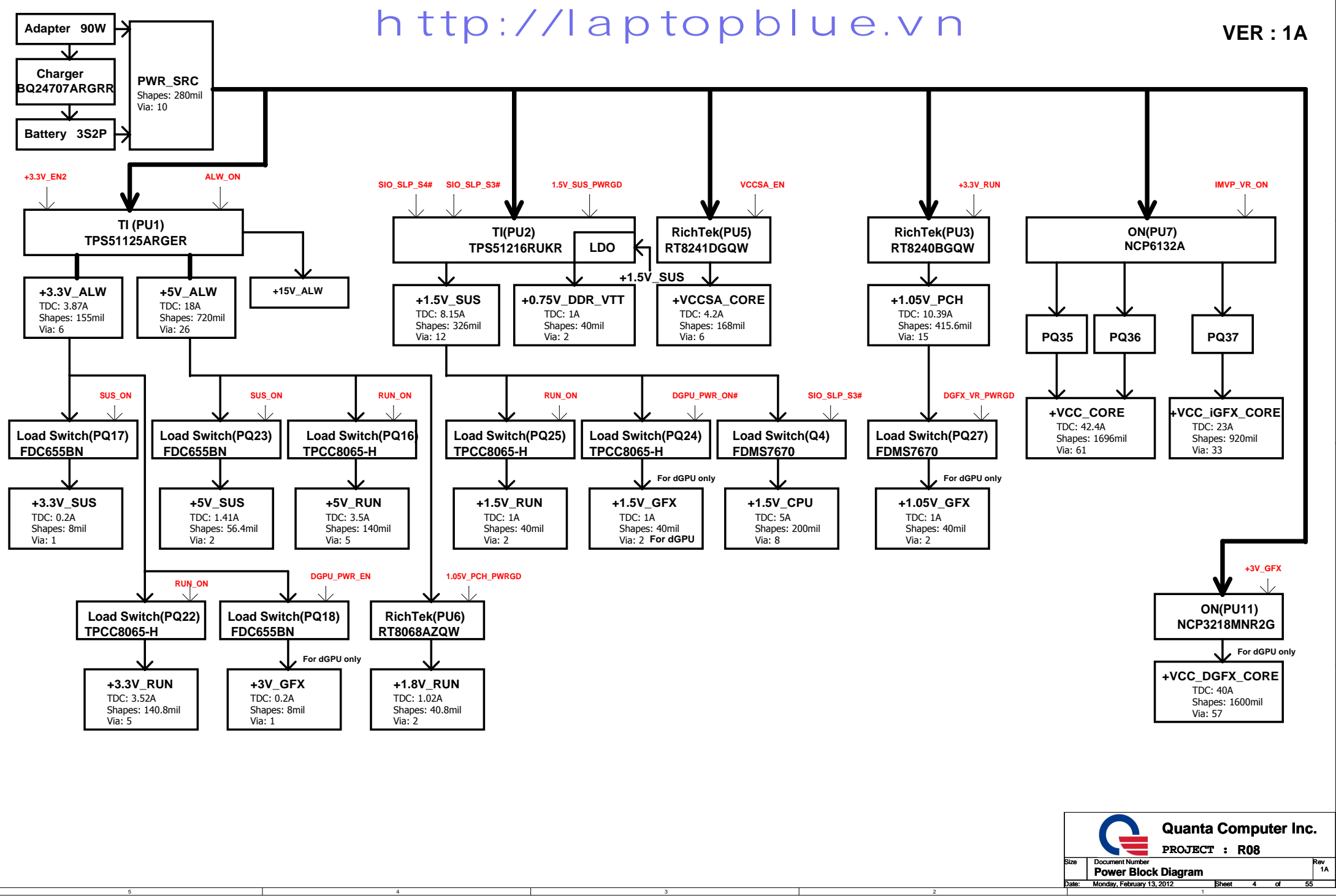
Function	IC	SMBus Address
DDR3	JDIM1A JDIM2A	A0h A4h
Thermal IC	EMC1422 G781-1P8	1001100xb (98h) 1001101xb (9Ah)
Charge IC	BQ24707ARGRR	0b0001001x (0x12h)
Battery	Battery	16h
Fall Sensor	STM LNG3DM	01010000 (50h)



USB Master	Port Assignment
USB0	External port#1 (USB3.0)
USB1	External port#2 (USB3.0/eSATA/ Power share/ debug port)
USB2	External port#3 (USB3.0)
USB3	External port#4 (USB3.0)
USB4	MiniCard 1 (WLAN/BT)
USB5	MiniCard 2 (WWAN/WiMAX)
USB6	X(FOR HM77)
USB7	X(FOR HM77)
USB8	Fingerprint
USB9	Touch panel (NC, for debug)
USB10	Card Reader
USB11	Express Card (NC)
USB12	Camera
USB13	NC

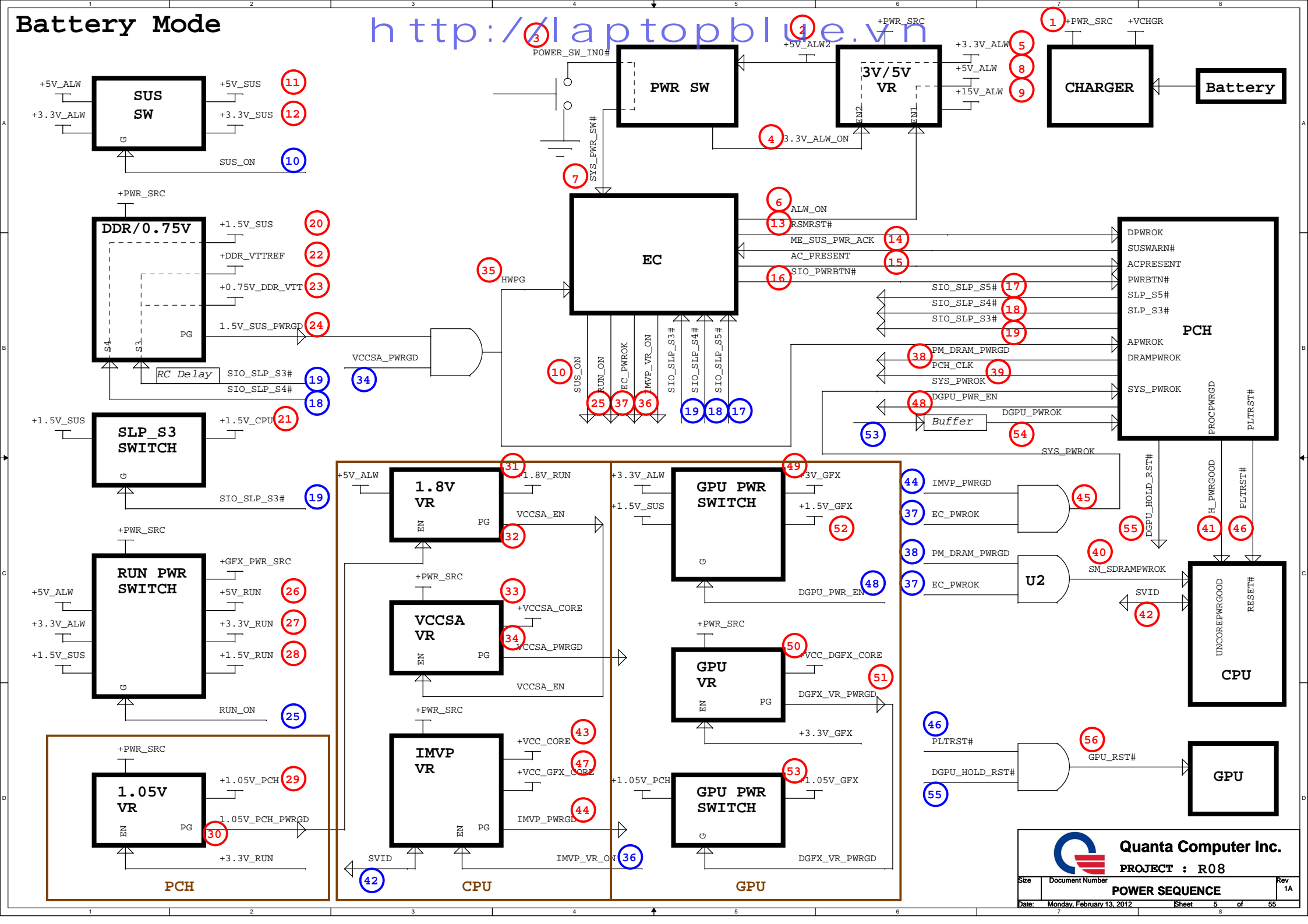
SATA Master	Port Assignment
SATA0	HDD
SATA1	mSATA
SATA2	NC
SATA3	ODD
SATA4	eSATA (NC)
SATA5	NC

PCIE Master	Port Assignment
PCIE 1	WLAN
PCIE 2	WWAN (NC)
PCIE 3	Card reader (NC)
PCIE 4	NC
PCIE 5	LAN
PCIE 6	Express card (NC)
PCIE 7	NC
PCIE 8	NC



Battery Mode

http://laptopblue.vn



eDP_COMP and ICOMPO signals should be shorted near balls and routed within 500 mils



This signal can be left as no connect if entire eDP interface is disabled.



0.1uF AC coupling Caps for PCIE GEN1/2

VGA(U3)	AC coupling Cap	PN	TX location	RX location(page1)
N13P-GL	0.1uF	CH4103K1B08	C1~C32	C144 C145 C147 C149 C150 C152 C154 C156 C157 C158 C159 C160 C161 C162 C163 C164 C165 C166 C167 C168 C169 C171 C173 C175 C176 C177 C178 C179 C180 C182 C184 C185
N13P-GS	0.22uF	CH4223K1B00	C1~C32	C144 C145 C147 C149 C150 C152 C154 C156 C157 C158 C159 C160 C161 C162 C163 C164 C165 C166 C167 C168 C169 C171 C173 C175 C176 C177 C178 C179 C180 C182 C184 C185

Ivy Bridge Processor (CLK, MISC, JTAG)

http://laptopblue.vn

SNB_IVB# N.A at SNB EDS #27637 0.7v1

23 H_SNB_IVB# ← H_SNB_IVB# C26
38 H_CPUDET# ← H_CPUDET# AN34

TP1 CATERR# ← CATERR# AL33

38 PECI_EC ← PECI_EC R6 1 2 43 4 PECI_EC_R AN33

38,52,54 IMVP7_PROCHOT# ← IMVP7_PROCHOT# R7 1 2 56 4 H_PROCHOT# AL32

Over 130 degree C will drive low
25 PM_THRMTRIP# ← PM_THRMTRIP# AN32

20 H_PM_SYNC ← H_PM_SYNC AM34

25 H_PWRGOOD ← H_PWRGOOD AP33

10K 4 2 1 R17

SM_DRAMPWROK V8

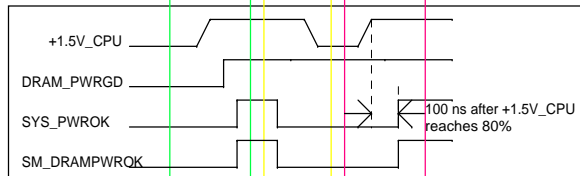
13,23,35,38 PLTRST# ← PLTRST# R19 2 1 1.5K F 4

CPU_PLTRST# R AR33

R20 750F 4

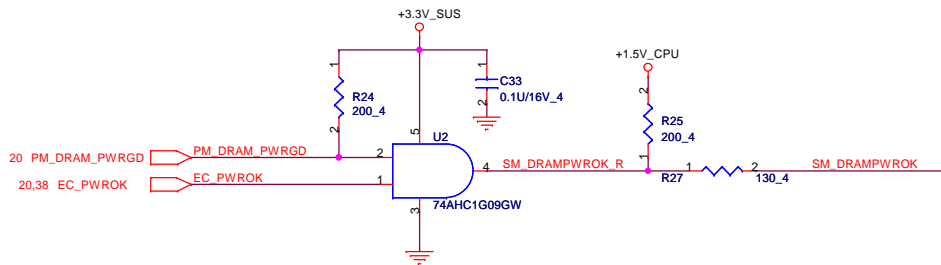
Intel spec VinH min = VCCIO X 0.7

C854 2 1 *100P/50V 4 NC H_PROCHOT#
C860 2 1 *100P/50V 4 NC CPU_PLTRST# R



Follow #DG1.5 471984 P119

Follow #DG1.5 471984 P128
DDR Power Gating Topology



MISC

CLOCKS

THERMAL

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

BCLK BCLK#

DPLL_REF_CLK DPLL_REF_CLK#

SM_DRAMRST#

SM_RCOMP[0] SM_RCOMP[1] SM_RCOMP[2]

PRDY# PREQ#

TCK TMS TRST#

TDI TDO

DBR#

BPM#[0] BPM#[1] BPM#[2] BPM#[3] BPM#[4] BPM#[5] BPM#[6] BPM#[7]

AT28 AR29 AR30 AT31 AR32

AR26 XDP_TCLK TP28

AR27 XDP_TMS TP37

AP30 XDP_TRST# TP38

AR28 XDP_TDI TP41

AP26 XDP_TDO TP42

AL35 XDP_DBRST# R18 1 2 1K 4

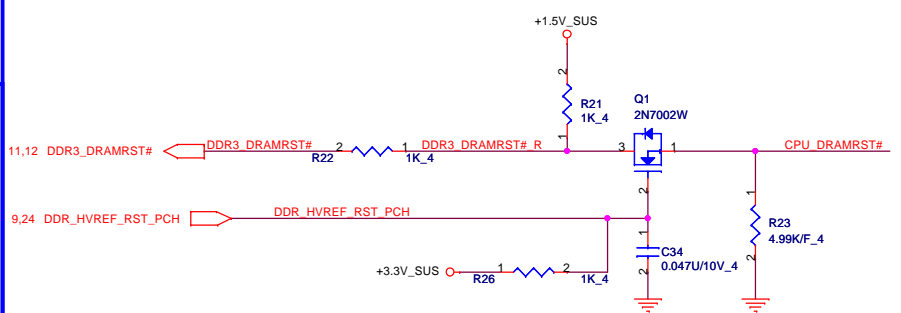
+3.3V_RUN

+1.05V_PCH

IMVP7_PROCHOT# R14 2 1 62 4

SM_RCOMP_0, SM_RCOMP_1 20mil / SM_RCOMP_2 15mil.

Follow #DG1.5 471984 P130
DRAMRST# Routing Illustration



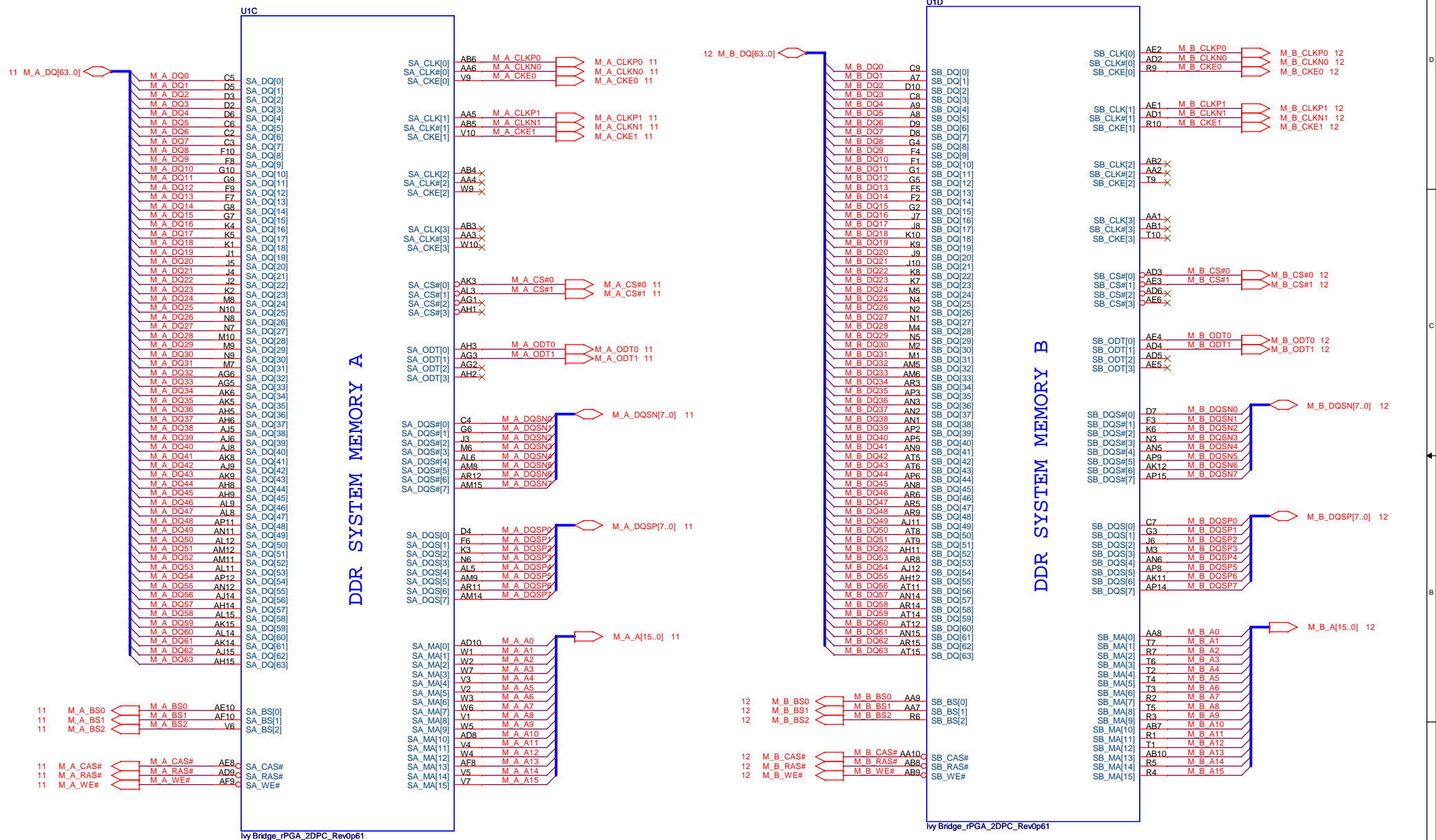
Quanta Computer Inc.

PROJECT : R08

Size	Document Number	Rev
	Ivy Bridge 2/5	1A
Date:	Monday, February 13, 2012	Sheet 7 of 55

Ivy Bridge Processor (DDR3)

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PROJECT : R08

Ivy Bridge Processor

CPU Core Power
SNB: 53A
IVY: 53A
10uF x 24

POWER

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

0.05V_PCH
SNB: 8.5A
IVY: 8.5A
10F x12

CPU VGT
SNB: 21.5A
IVY: 33A
10uF x 12

Ivy Bridge Processor (GRAPHIC POWER)

POWER

GRAPHICS

1.8V RAIL

SENSE LINES

VREF

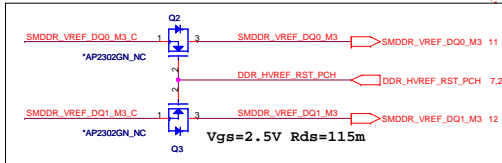
DDR3 - 1.5V RAILS

SA RAIL

MISC

Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
VCC_SENSE / VSS_SENSE	100Ω	27-33Ω	<25 mils
VCCAXG_SENSE / VSSAXG_SENSE	100Ω		
VCCIO_SENSE / VSS_SENSE_VCCIO	10Ω	55Ω	
VCCSA	100Ω		

M3 VREF



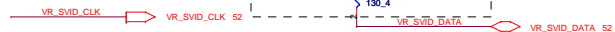
Place PU resistor close to CPU

SVID ALERT



Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK



Place PU resistor close to CPU

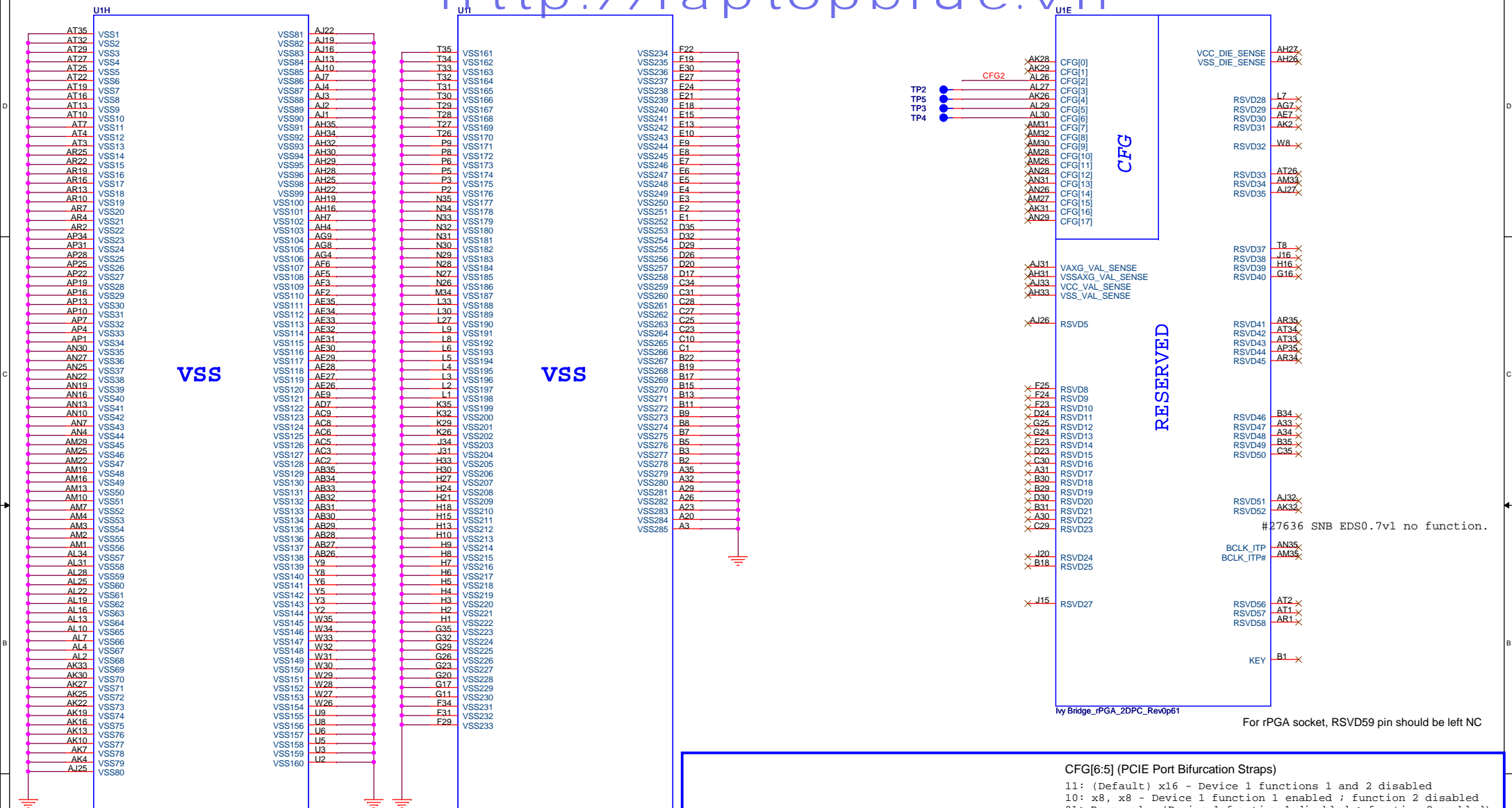
SVID DATA



Take care Q3 Vgs(MAX)=2.5

Ivy Bridge Processor (GND)

Ivy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

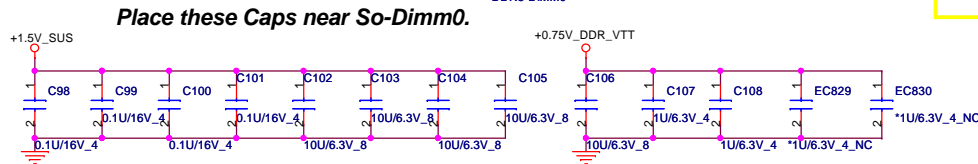
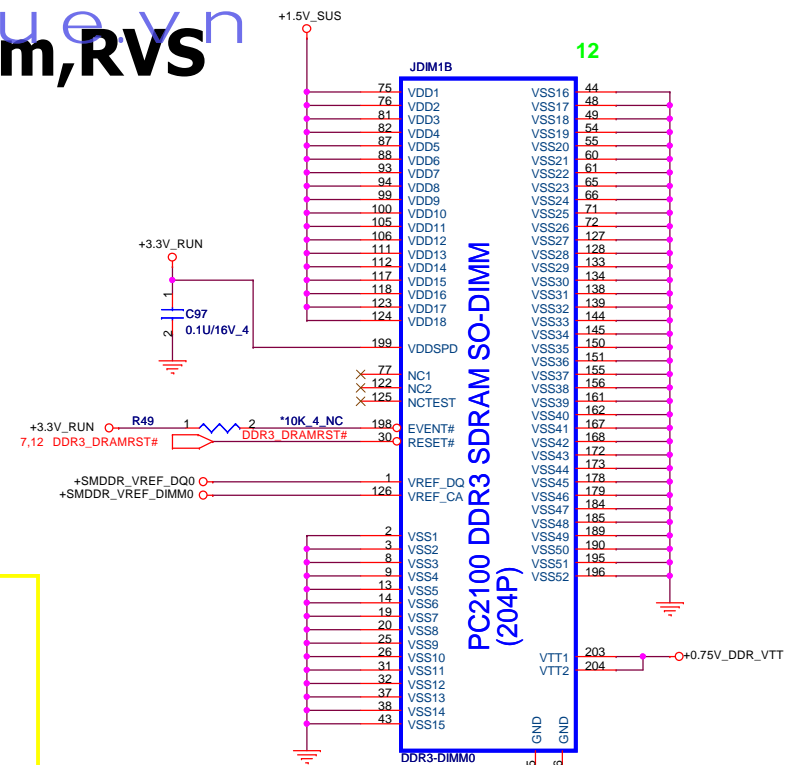
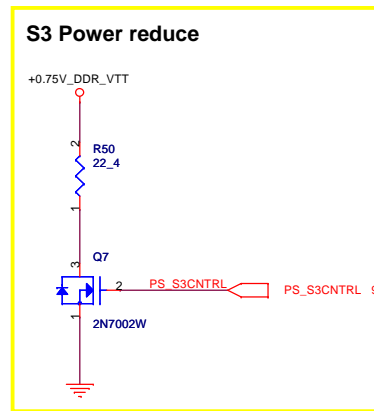
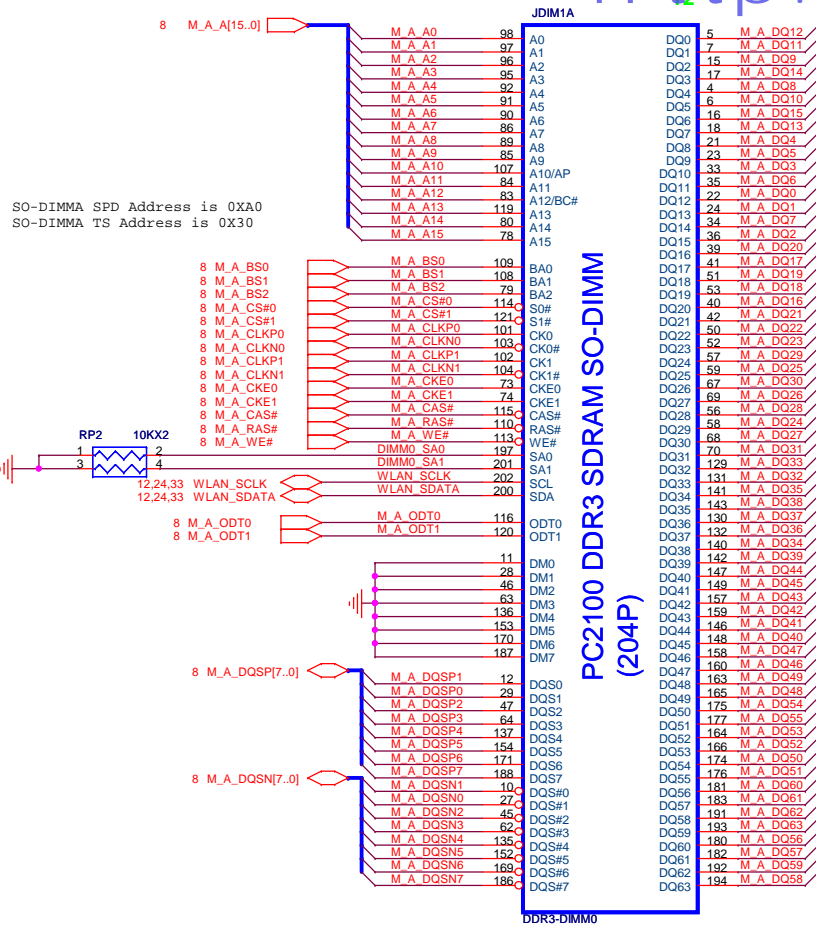
	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



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PROJECT : R08

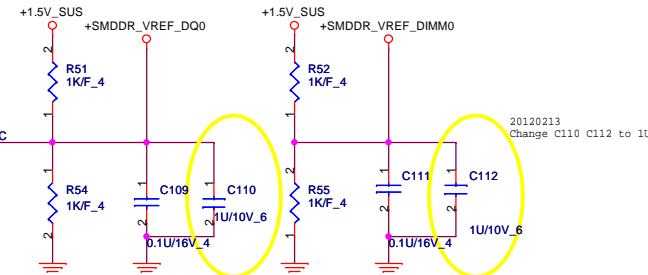
H=8mm,RVS



9 SMDDR_VREF_DQ0_M3
SMDDR_VREF_DQ0_M3
R53
*0.4_NC

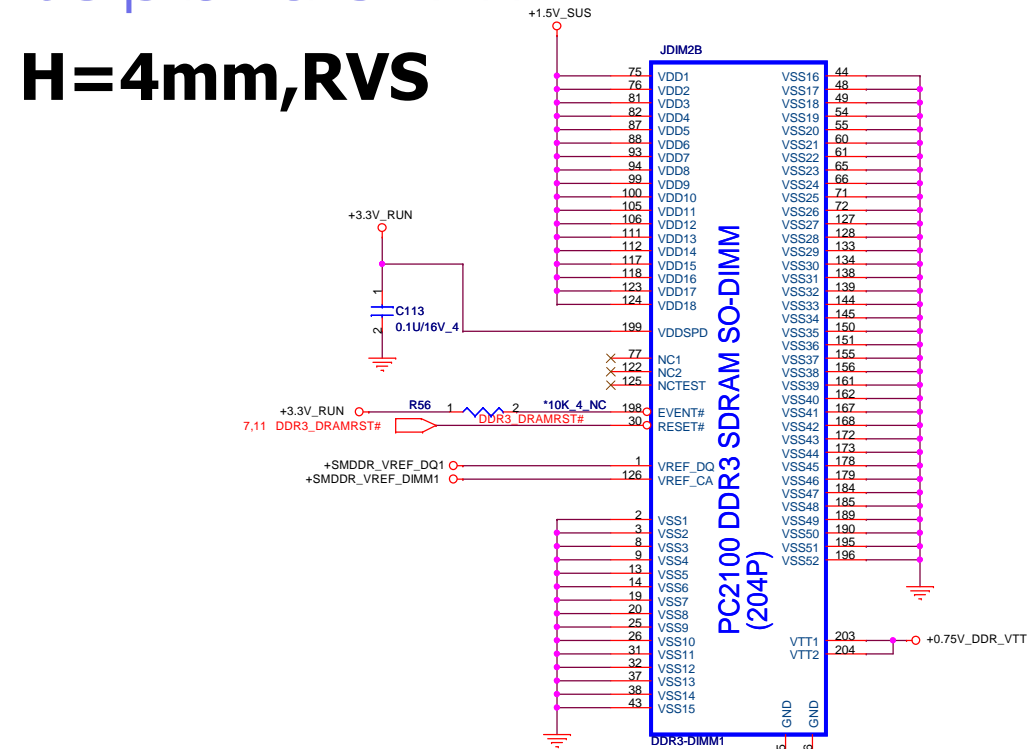
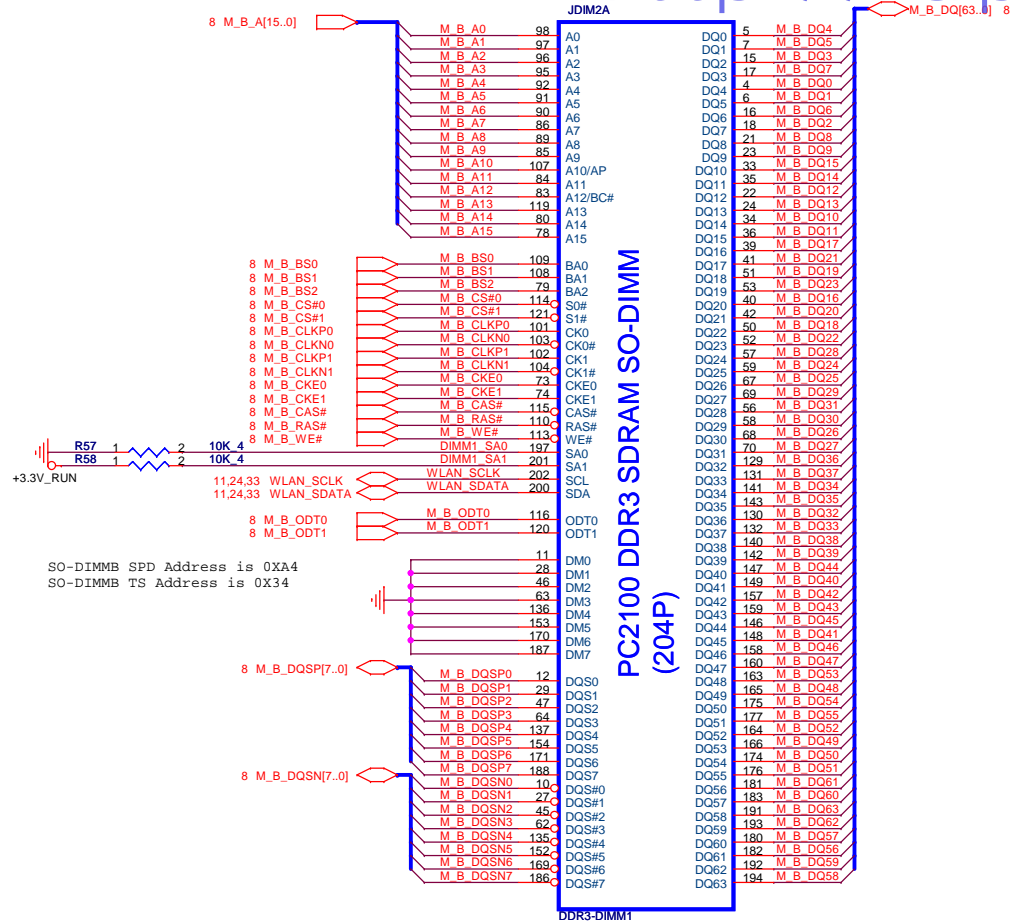
M3 VREF

M1 VREF

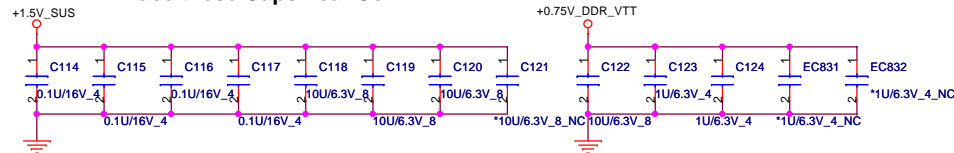


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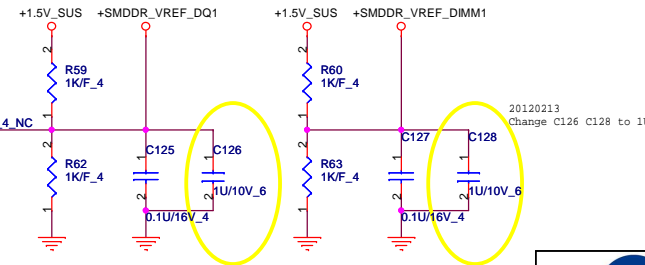
H=4mm,RVS



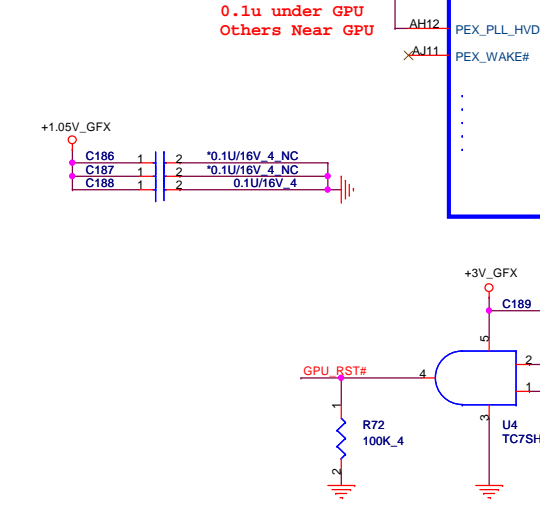
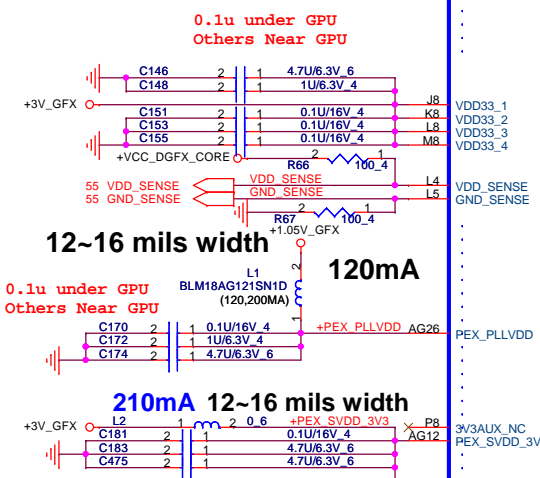
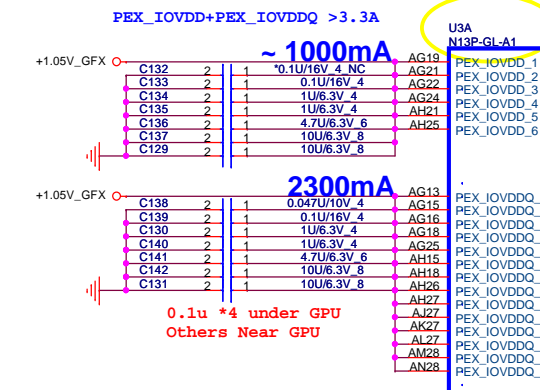
Place these Caps near So-Dimm1.



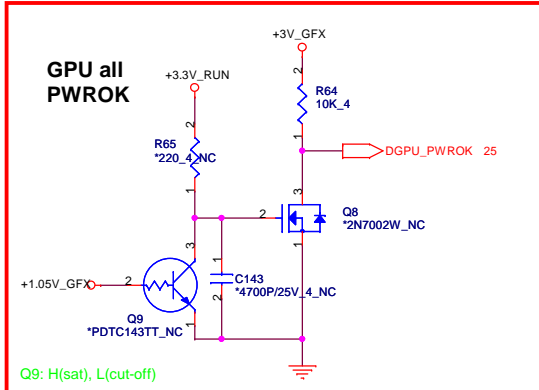
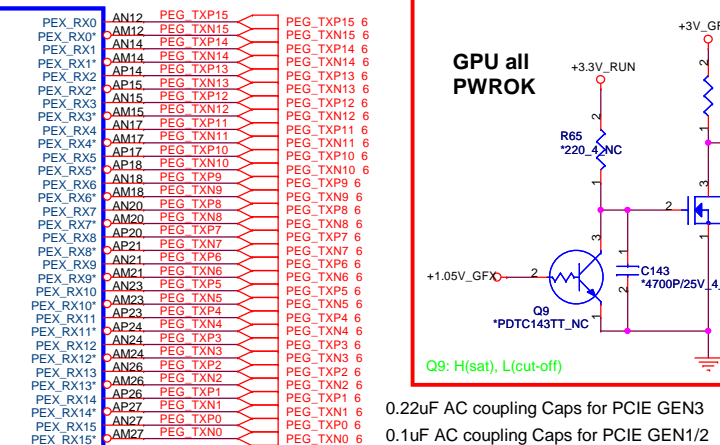
M1 VREF



M3 REF

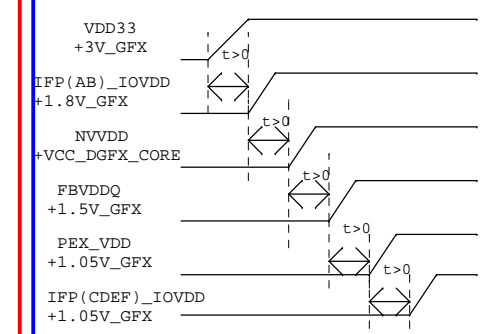


GB4-128 PCI EXPRESS



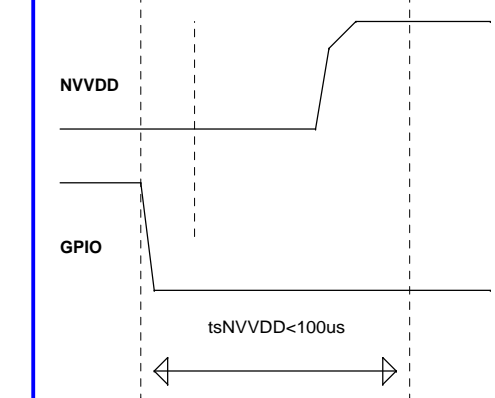
0.22uF AC coupling Caps for PCIE GEN3
0.1uF AC coupling Caps for PCIE GEN1/2

Power up sequence

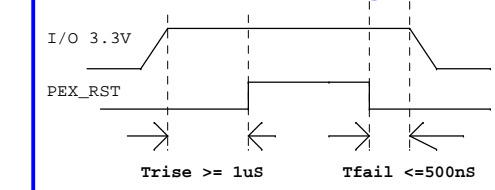


NB9M: VGACORE +0.90V (Normal) , +1.09V

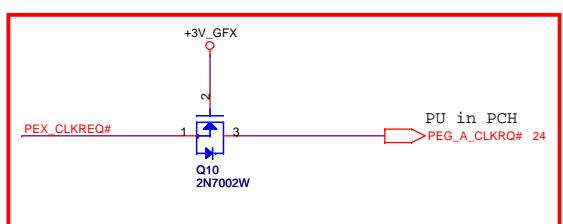
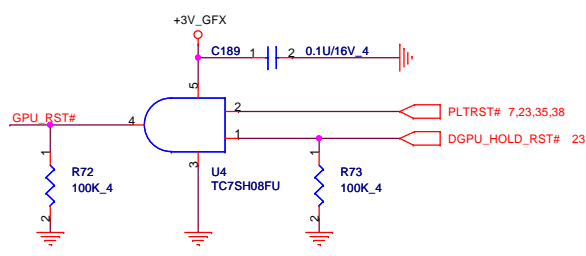
NVVDD Maximum Settling Time

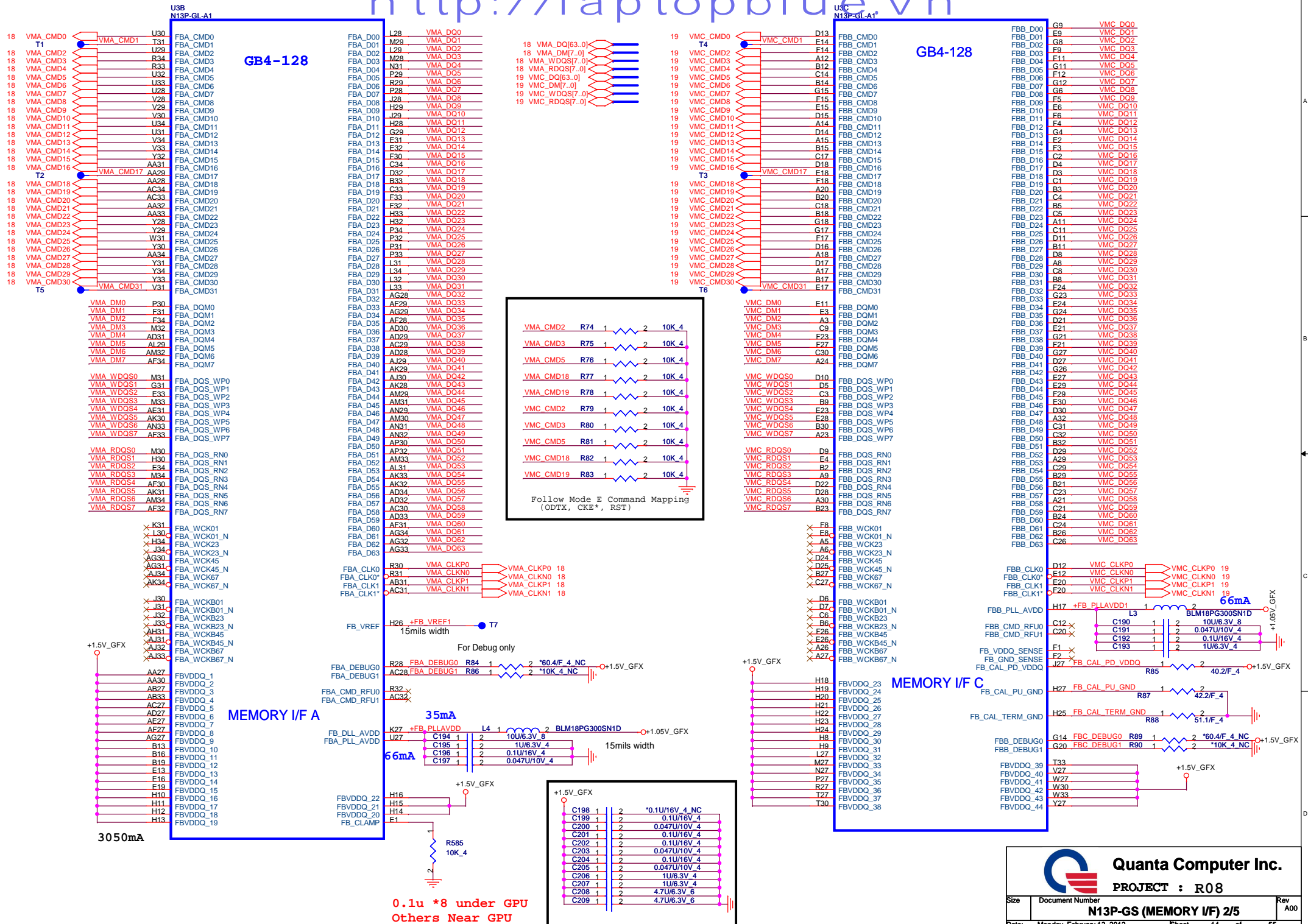


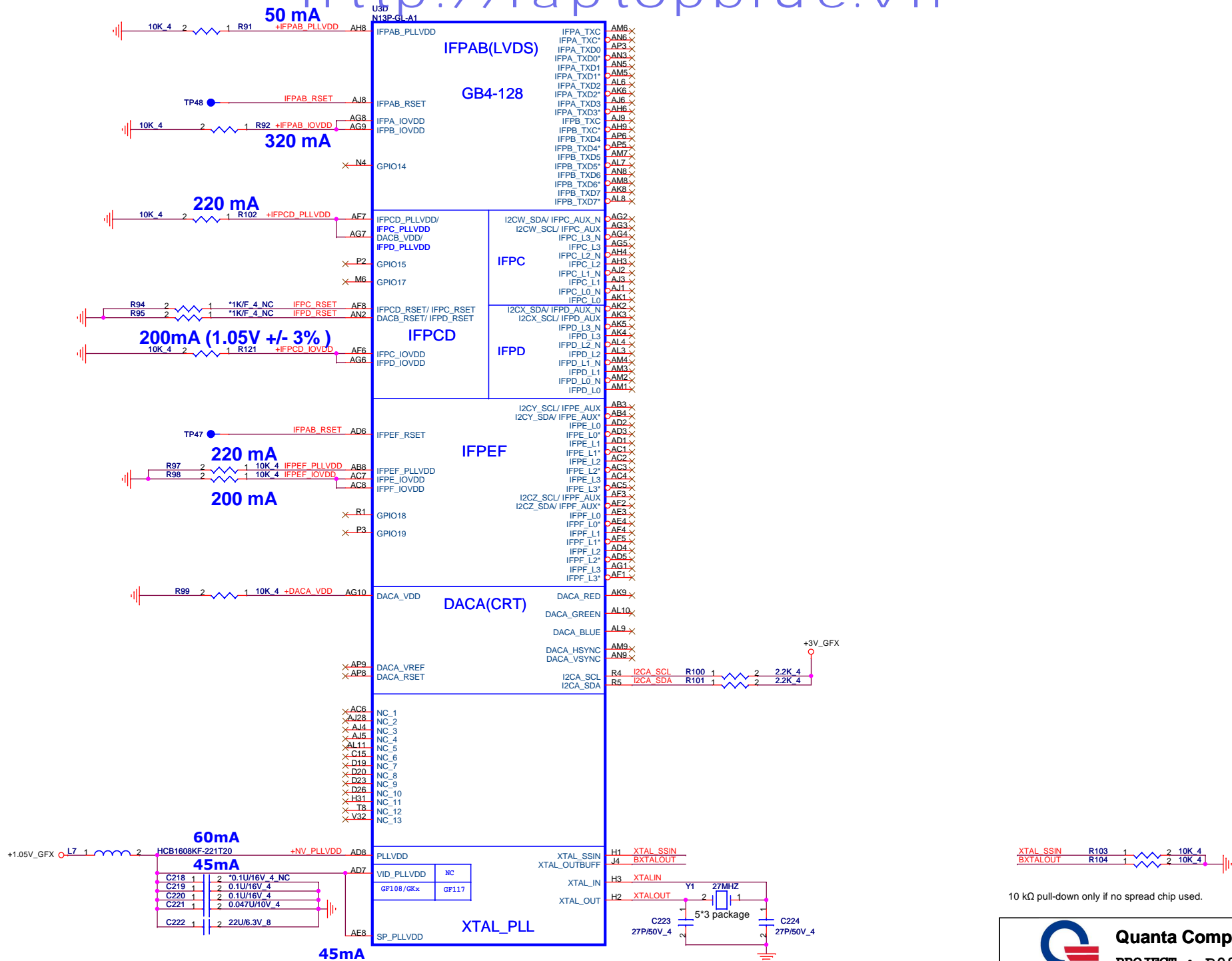
PEX_RST timing



20120203
Change C144 C145 C147 C149 C150
C152 C154 C156 C157 C158
C159 C160 C161 C162 C163
C164 C165 C166 C167 C168
C169 C171 C173 C175 C176
C177 C178 C179 C180 C182
C184 C185 to 0.1U/16V_4(CH4103K1B08)



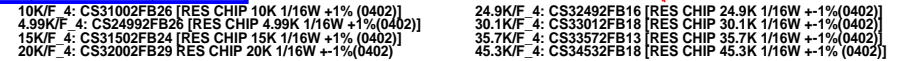




10 kΩ pull-down only if no spread chip used.

	CHIP	PCI_DEVICE:	STRAP2	ROM_SCLK	ROM_SO
	N13P-GS	0x0FD2(QS)	0010 PD 15K	1000 PU 5K	1001 PU 10K
	N13P-LP	0x0FD3	0011 PD 20K	1000 PU 5K	
	N13M-GS	0x1142	0010 PD 15K	0000 PD 5K	
	N13P-GL	0x0DE9	1001 PU 10K	0010 PD 15K	0001 PD 10K

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Default: Hynix VRAM 2G (0110) [VRAM Configuration Table](#)

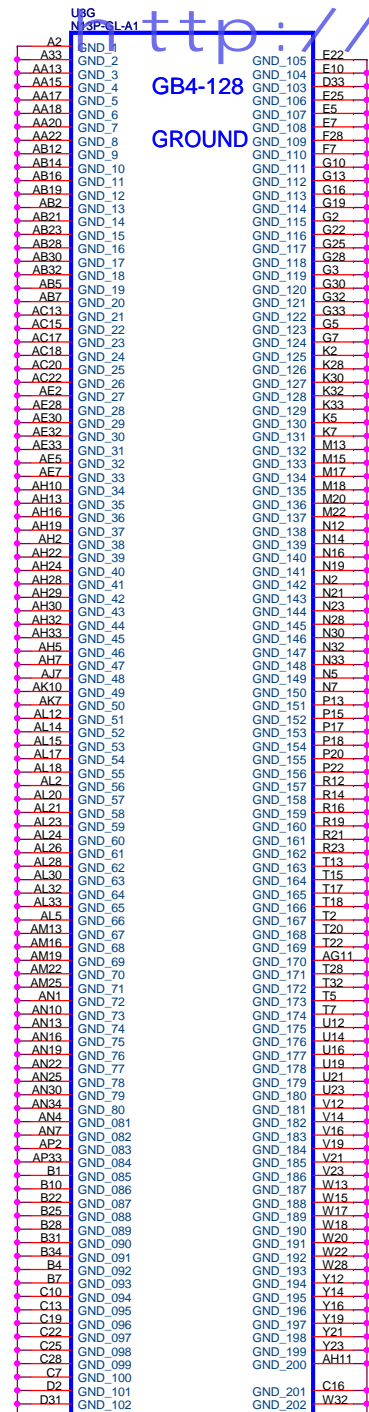
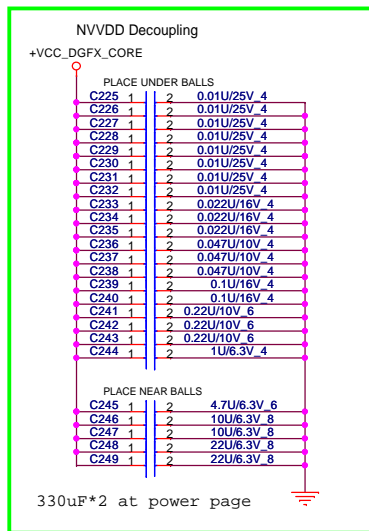
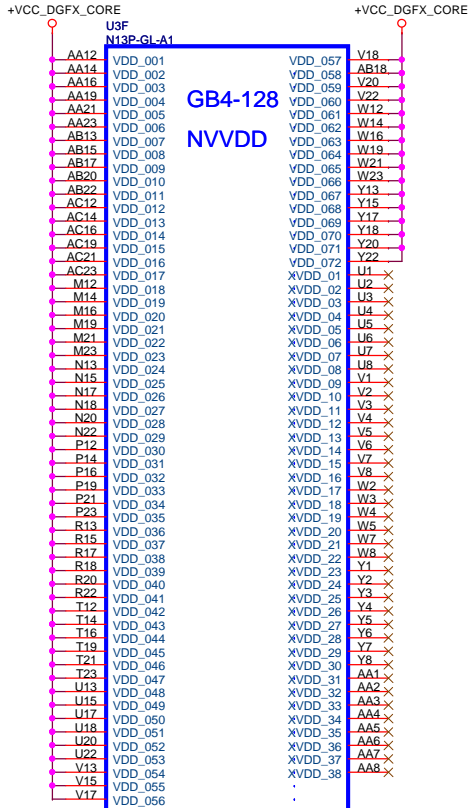
GPIO	Pin	Function	Signal	Value
GPIO0	P6	DGPU VID4	DGPU_VID4	55
GPIO1	M3	DGPU VID3	DGPU_VID3	55
GPIO2	L6	X		
GPIO3	P7	X		
GPIO4	P7	X		
GPIO5	M7	DGPU VID1	DGPU_VID1	55
GPIO6	L7	DGPU VID2	DGPU_VID2	55
GPIO7	N8	X		
GPIO8	M1	VGA OVT#		
GPIO9	M2	VGA ALERT		
GPIO10	L1	X		
GPIO11	M5	DGPU VID0	DGPU_VID0	55
GPIO12	N3	VGA_PWR_LEVEL#	VGA_PWR_LEVEL#	38,55
GPIO13	M4	DGPU VID5	DGPU_VID5	55



Signal	Pin	Function	Pin	Function
JTAG TMS	*10K_4_NC	1	2	R123
JTAG TDI	*10K_4_NC	1	2	R126
VGA DVT#	10K_4	1	2	R129
DGPU_VID0	*10K_4_NC	1	2	R596
DGPU_VID1	*10K_4_NC	1	2	R597
DGPU_VID2	10K_4	1	2	R598
DGPU_VID3	10K_4	1	2	R599
DGPU_VID4	*10K_4_NC	1	2	R600
DGPU_VID5	10K_4	1	2	R601
VGA_ALERT	10K_4	1	2	R132
VGA_PWR_LEVEL#	10K_4	1	2	R133
DGPU_VID0	10K_4	1	2	R607
DGPU_VID1	10K_4	1	2	R606
DGPU_VID2	*10K_4_NC	1	2	R605
DGPU_VID3	*10K_4_NC	1	2	R604
DGPU_VID4	10K_4	1	2	R603
DGPU_VID5	*10K_4_NC	1	2	R602
VGA_PWR_LEVEL#	C861	1	2	100P/50V_4
JTAG TCK	*10K_4_NC	1	2	R136
JTAG TRST#	10K_4	1	2	R138

	Output	VID0	VID1	VID2	VID3	VID4	VID5
N13P-GL	0.95V	0	0	1	1	0	1
N13P-GS	0.9V	0	0	0	0	1	1

N13P-GS 50 A
N13P-LP 40 A



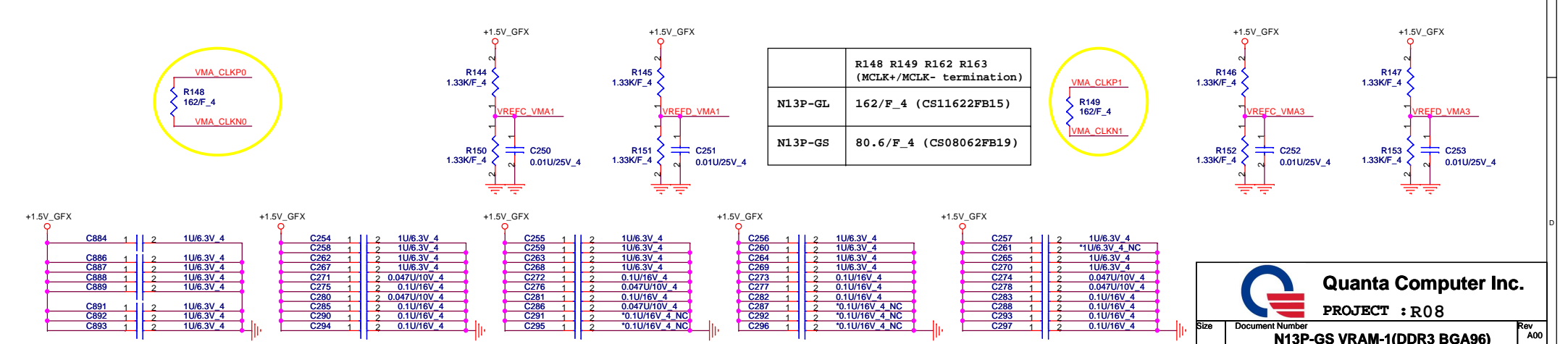
Change U6~U13 to AKD5LZWTW07 (hynix 1G)

```

14 VMA_DQ[63..0]
14 VMA_DM[7..0]
14 VMA_WDQS[7..0]
14 VMA_RDQS[7..0]

```

CHANNEL A: 512MB/1024MB DDR3



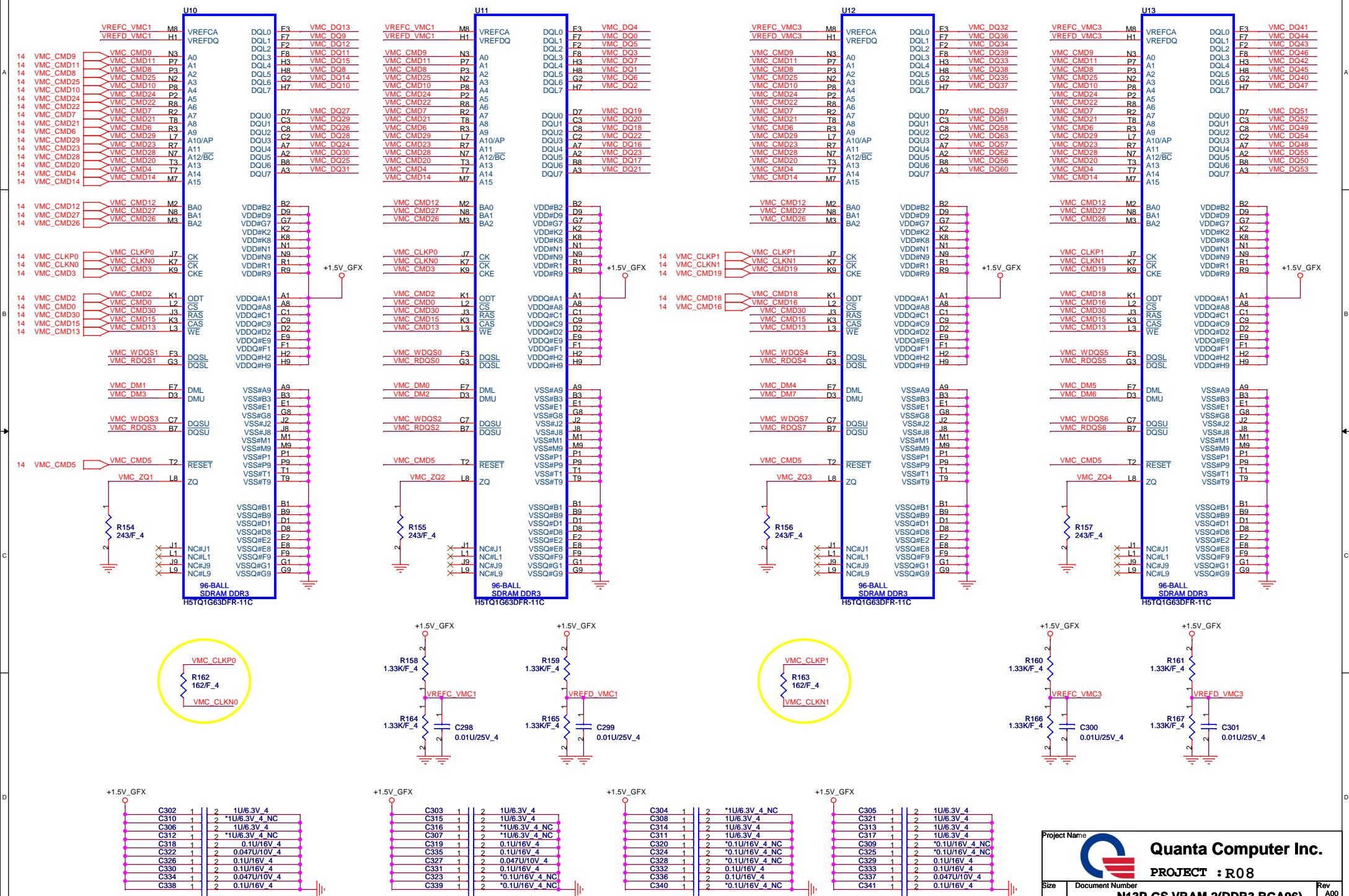
	R148 R149 R162 R163 (MCLK+/MCLK- termination)
N13P-GL	162/F_4 (CS11622FB15)
N13P-GS	80.6/F_4 (CS08062FB19)

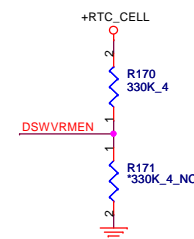
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PROJECT : R08

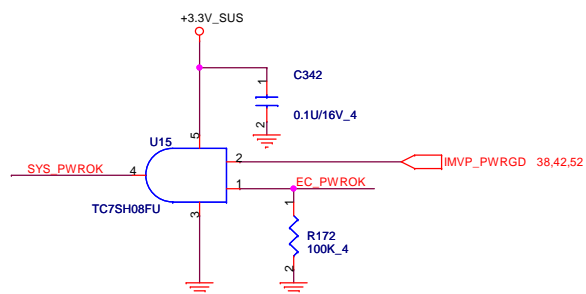
Size	Document Number	Rev
	N13P-GS VRAM-1(PDDR3 BGA96)	A00

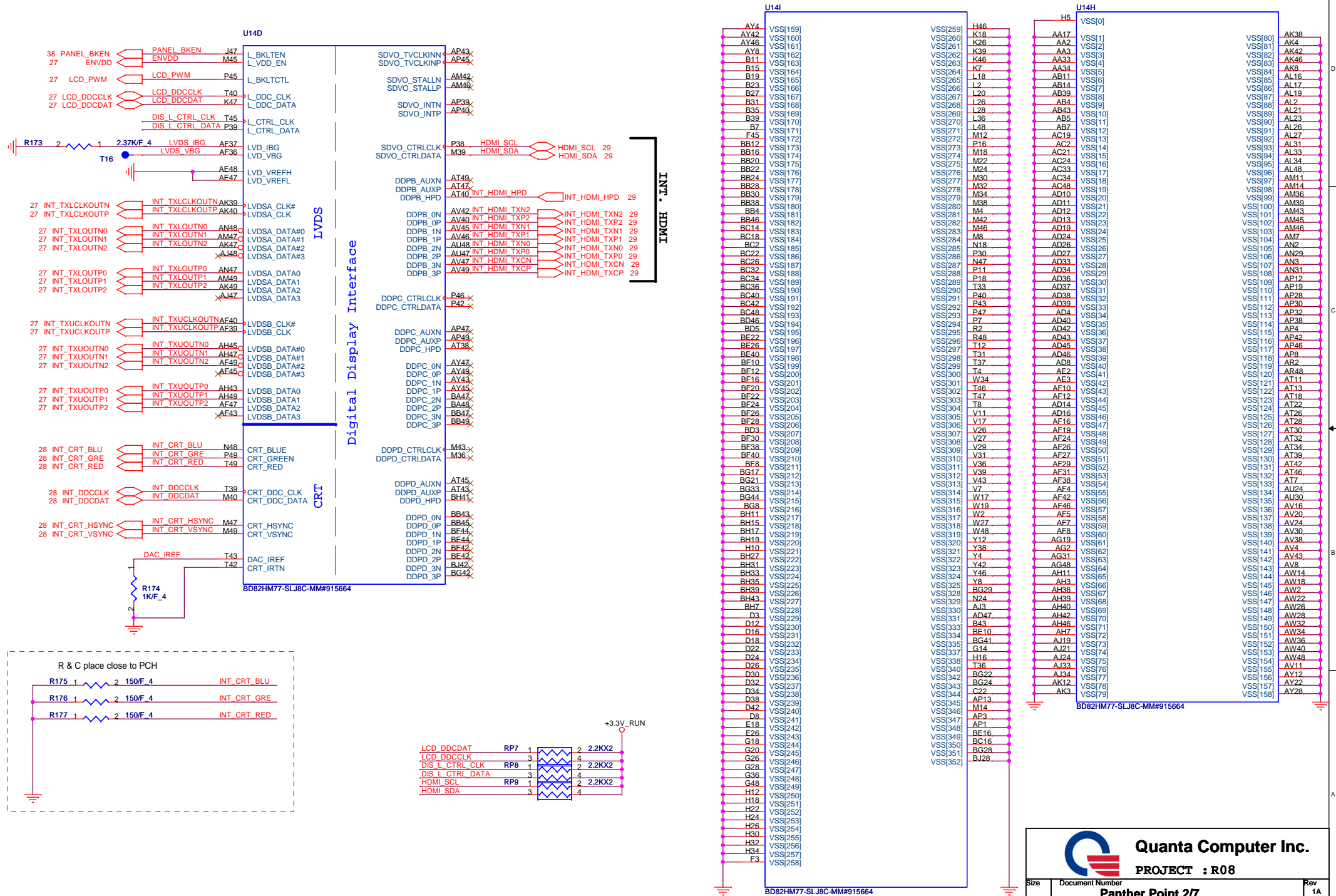
CHANNEL B: 512MB/1024MB DDR3





On Die DSW VR Enable
High = Enable (Default)
Low = Disable





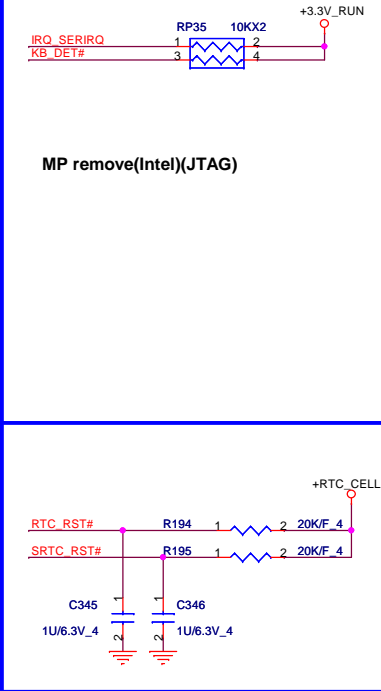
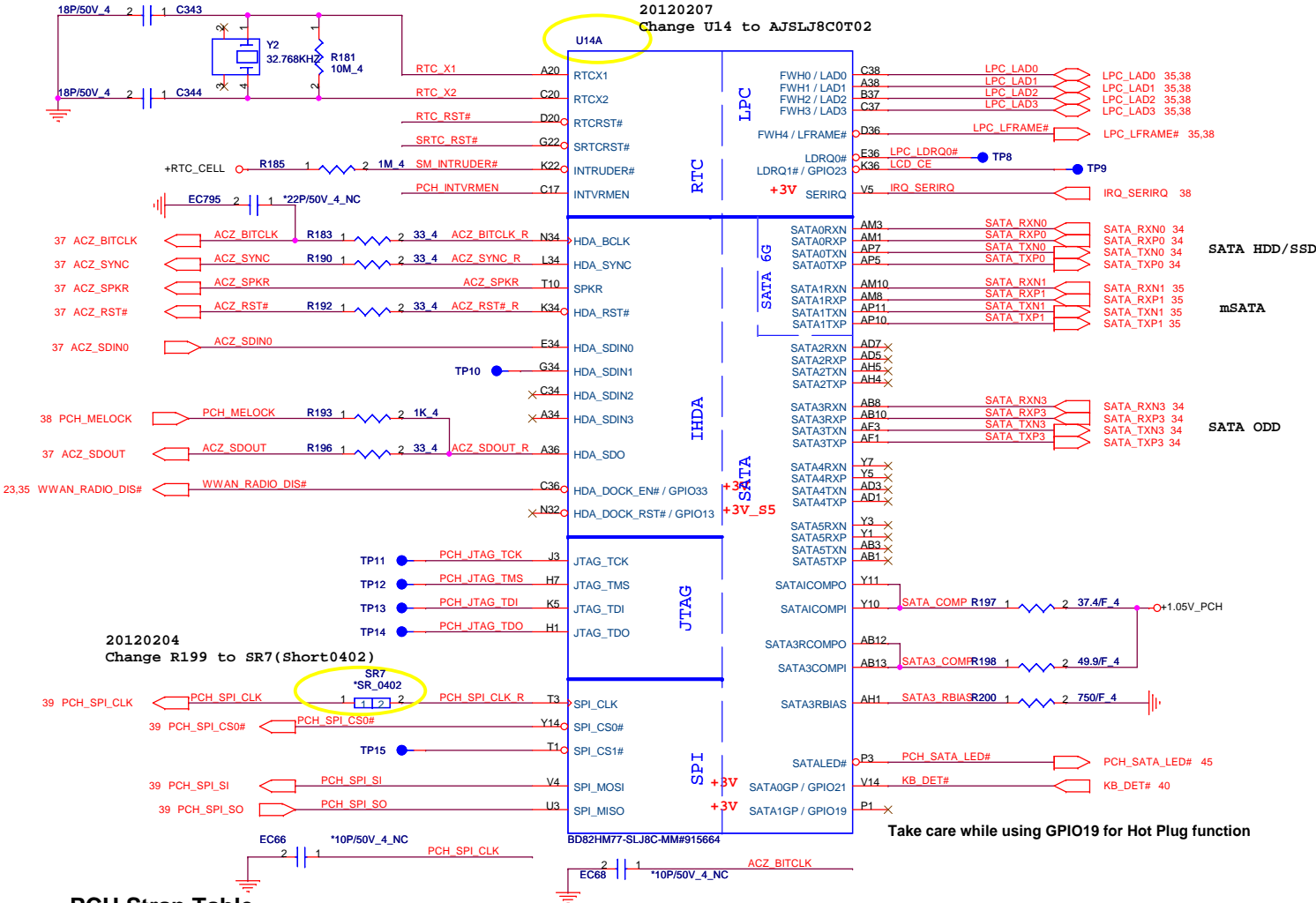
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PROJECT : R08

Panther Point 2/7

Cougar Point/Panther Point (HDA,JTAG,SATA)

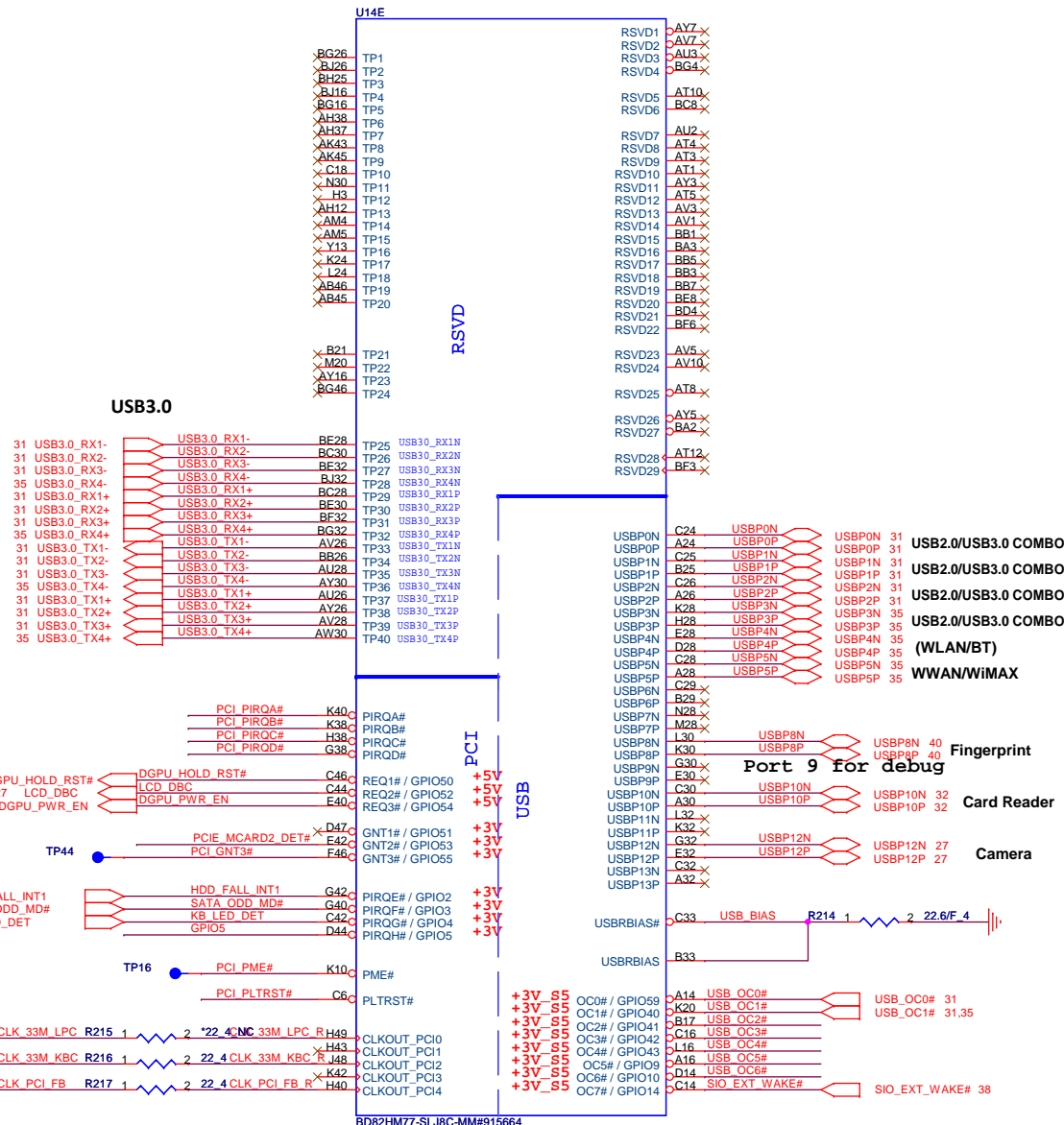
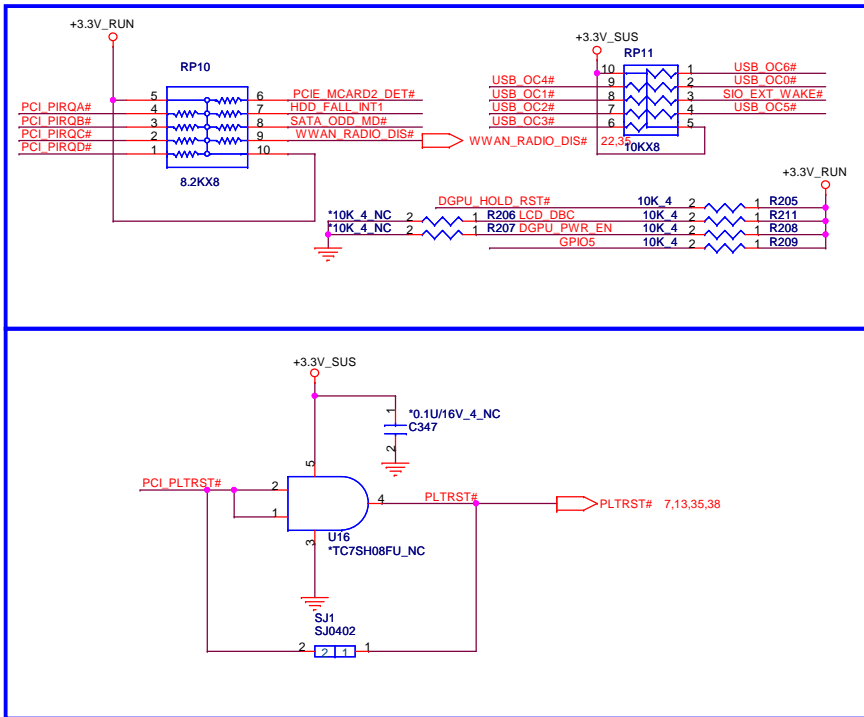
20120204
Change U14 to AJ0QPEG0T07(WINCON)
20120207
Change U14 to AJSLJ8C0T02



PCH Strap Table

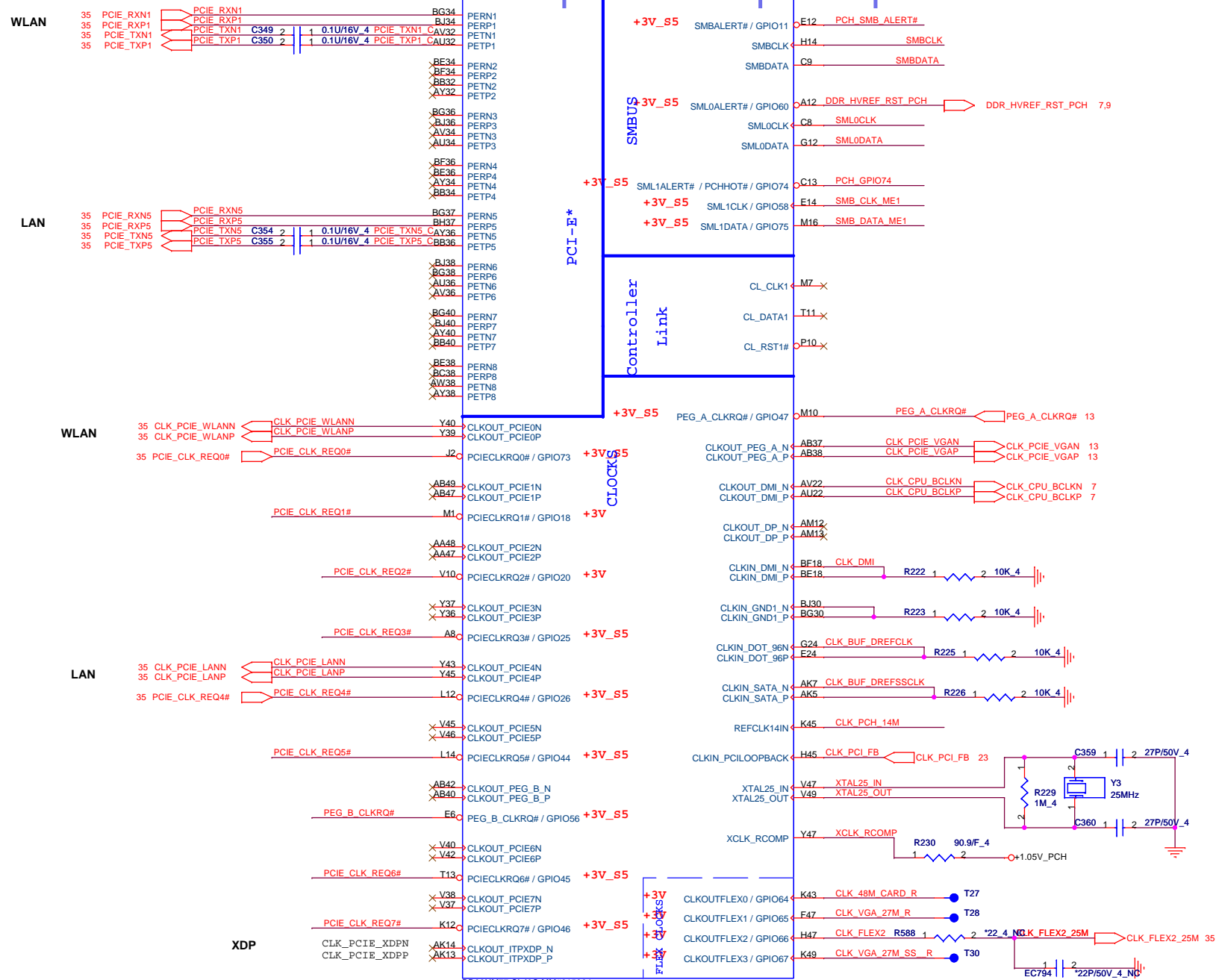
Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL ○ R203 1 2 330K 4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS ○ R204 1 2 1K 4 ACZ_SYNC_R

Cougar Point-M/Panther Point (PCI,USB,NVRAM)

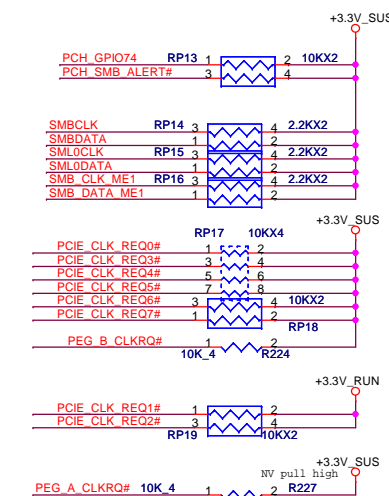
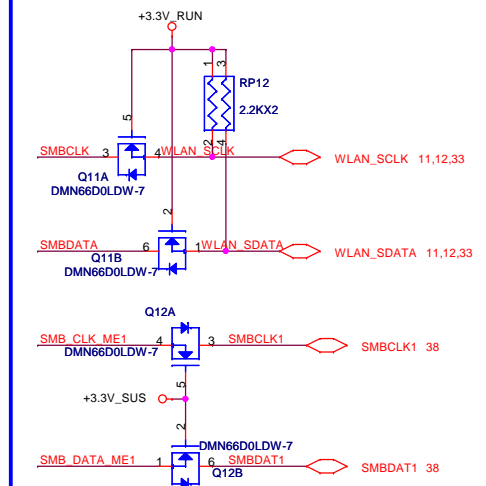


Pin Name	Strap description	Sampled	Configuration									
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><td>Bit 0</td><td>Bit 1</td><td>Boot Location</td></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	Bit 0	Bit 1	Boot Location	1	1	SPI *	0	0	LPC
Bit 0	Bit 1	Boot Location										
1	1	SPI *										
0	0	LPC										
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK										
Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]												
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm									
<p>The diagram shows two resistors connected to a common node. The top resistor is labeled R220 with a value of 2.2K, connected to +1.8V_RUN. The bottom resistor is labeled R221 with a value of 1K, connected to H_SNB_IVB#. The common node is connected to DF_TVS (pin 25) and H_SNB_IVB# (pin 7).</p>												

0148 Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)

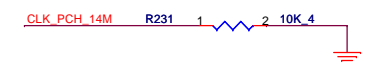


CLKOUTFLEX0 /GPIO64	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX1 /GPIO65	• 33 /27 /48/ 14.318 MHz / DC Output logic '0'
CLKOUTFLEX2 /GPIO66	unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC /48/24 MHz
CLKOUTFLEX3 /GPIO67	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
	• 27/14.318 output to SIO/48/24 MHz (Default)



CLK_REQ/Strap Pin(CLG)

Stuff for Integrated CLK Gen Mode



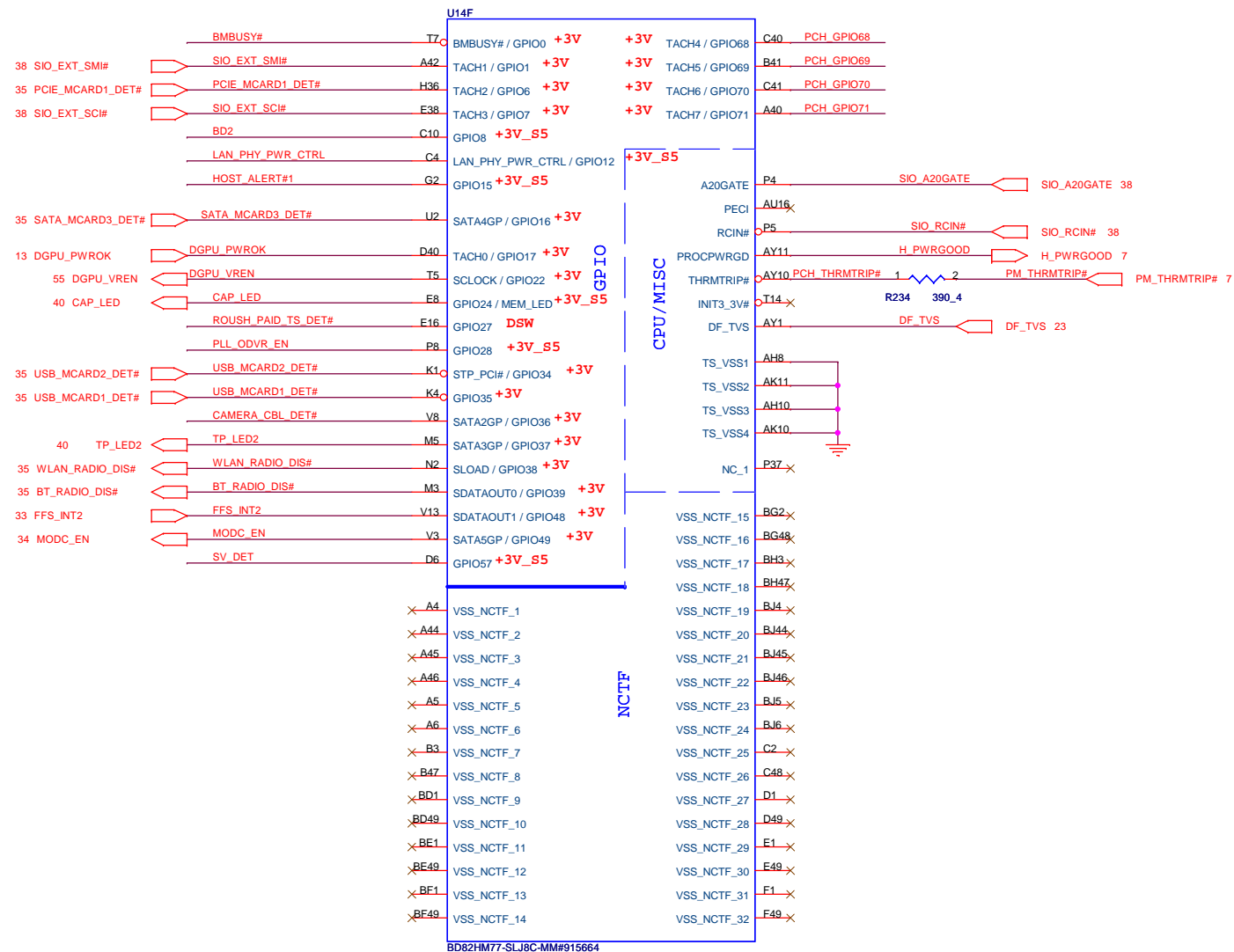
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PROJECT : R08

Panther Point 5/7

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	Panther Point 5/7	1A
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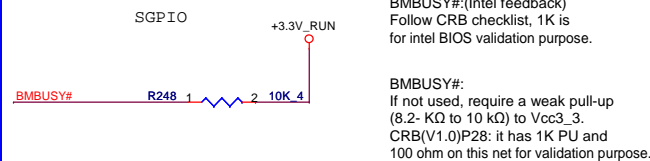
FRSVD) <http://laptopblue.vn>



HOST_ALERT#1 R244 1 2 1K 4 +3.3V_SUS

+3.3V_SUS R245 1 2 10K 4 SV_DET

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

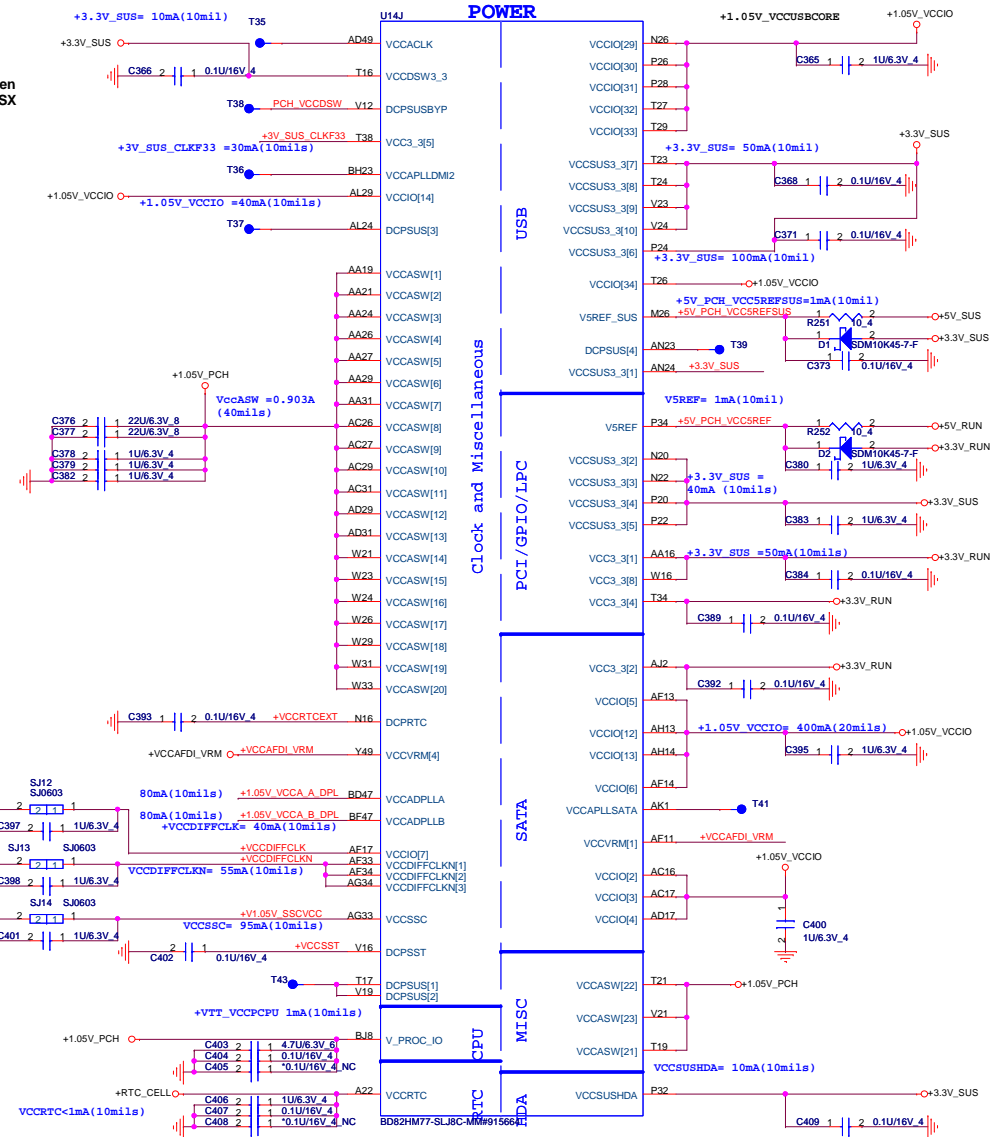


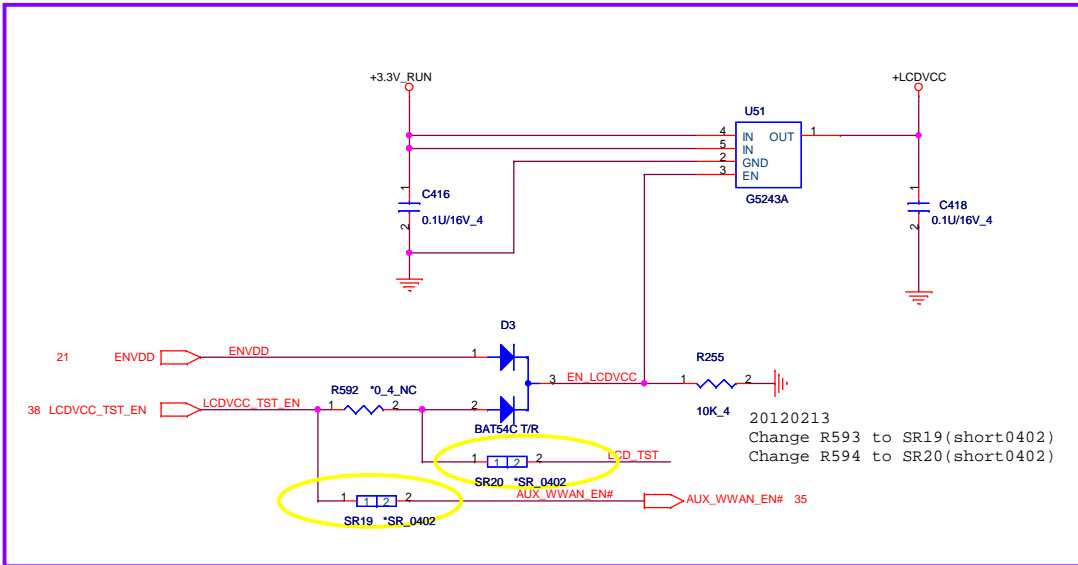
WLAN_RADIO_DIS# R249 1 2 10K 4
R250 1 2 *0.4 NC



Size	Document Number	Rev
	Panther Point 6/7	1A
Date:	Monday, February 13, 2012	Sheet 25 of 55

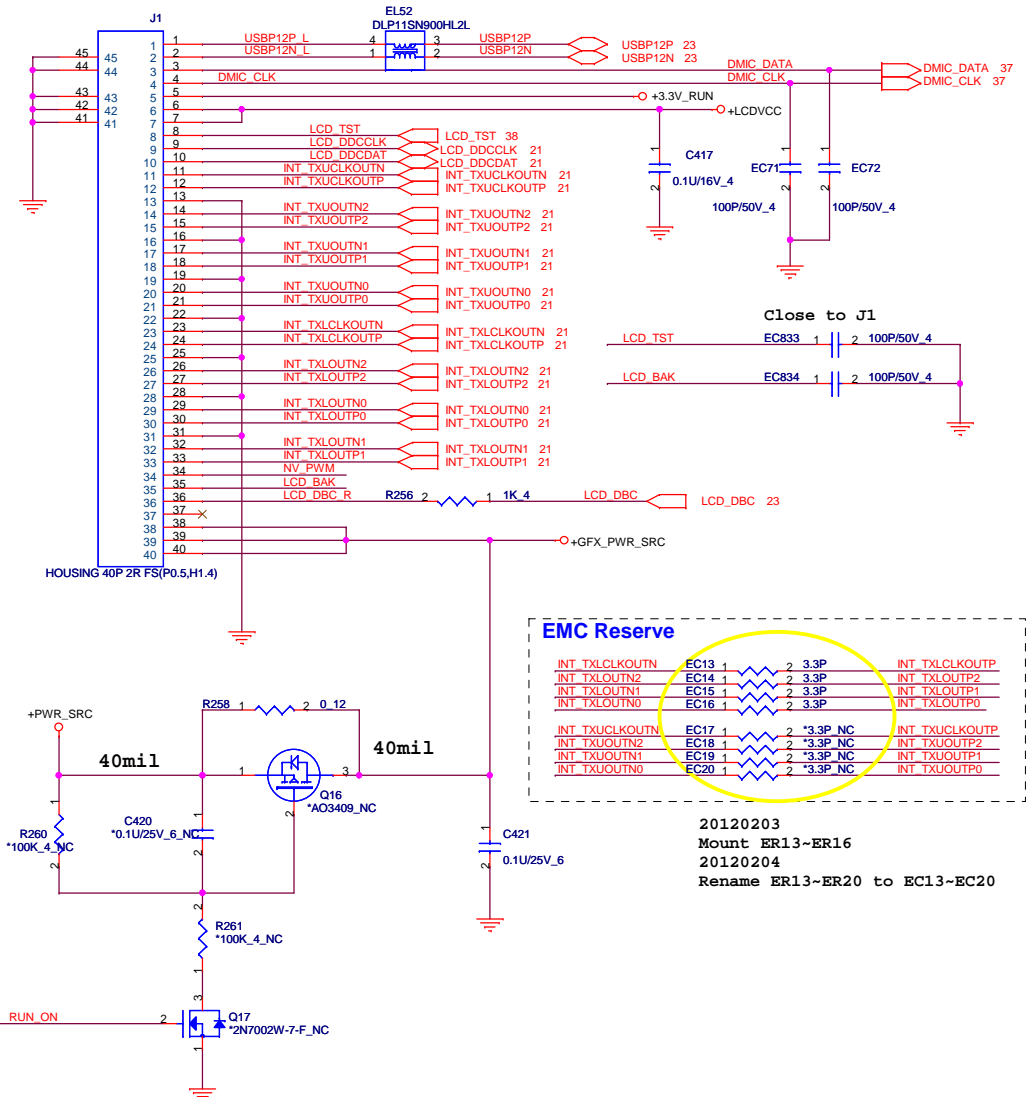
Cougar Point/Panther Point (POWER)





Backlight Enable

Brightness Control

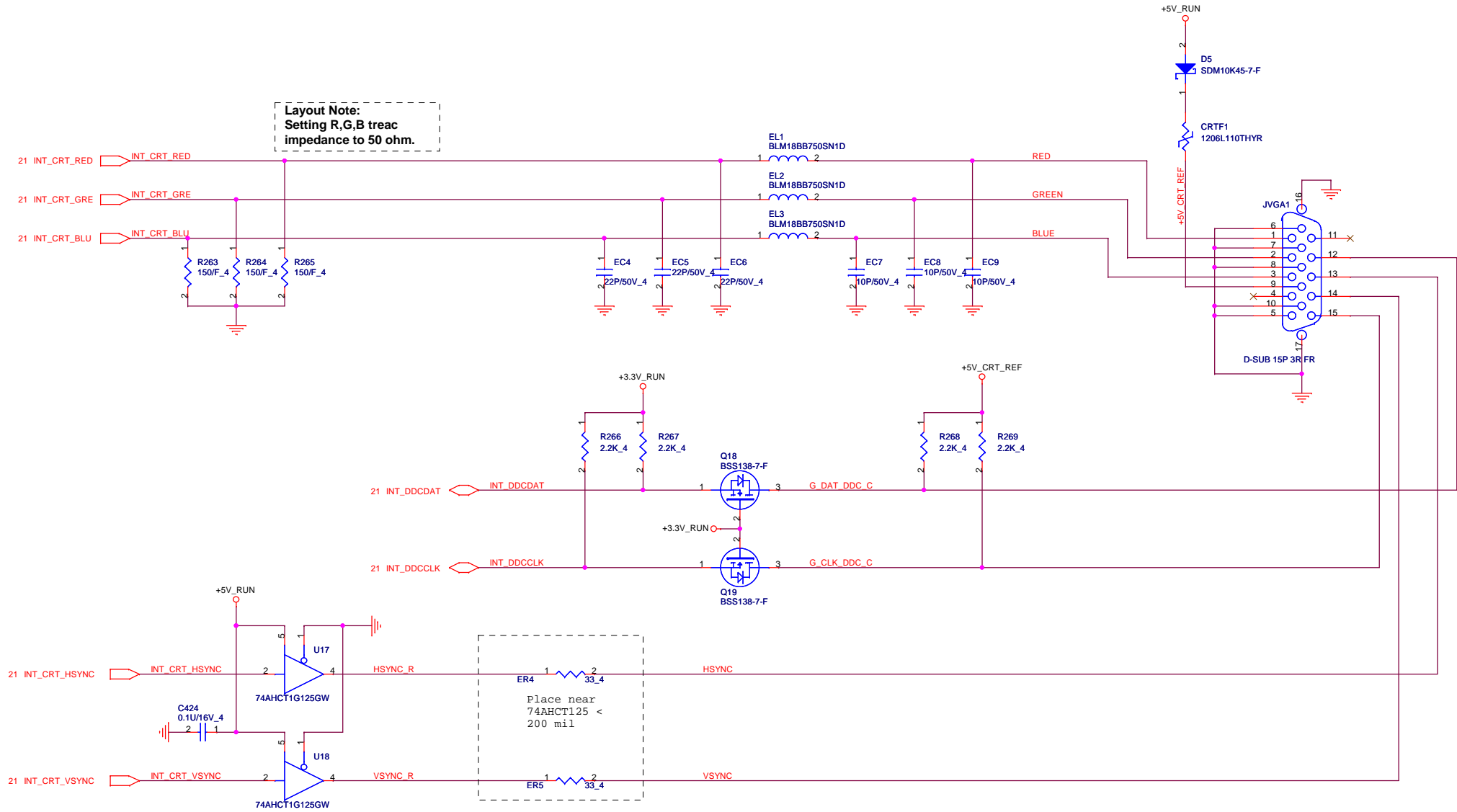


EMC Reserve

INT_TXCLKOUTN	EC13	1	2	3.3P	INT_TXCLKOUTP
INT_TXCLKOUTN	EC14	1	2	3.3P	INT_TXCLKOUTP
INT_TXCLKOUTN	EC15	1	2	3.3P	INT_TXCLKOUTP
INT_TXCLKOUTN	EC16	1	2	3.3P	INT_TXCLKOUTP
INT_TXCLKOUTN	EC17	1	2	*3.3P NC	INT_TXCLKOUTP
INT_TXCLKOUTN	EC18	1	2	*3.3P NC	INT_TXCLKOUTP
INT_TXCLKOUTN	EC19	1	2	*3.3P NC	INT_TXCLKOUTP
INT_TXCLKOUTN	EC20	1	2	*3.3P NC	INT_TXCLKOUTP

20120203
Mount ER13~ER16
20120204
Rename ER13~ER20 to EC13~EC20

Layout Note:
Setting R,G,B treac
impedance to 50 ohm.

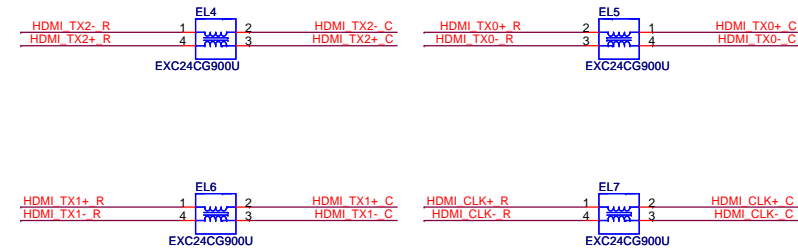


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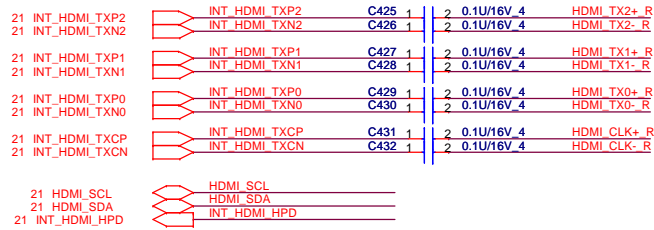
PROJECT : R08

VGA BOARD

Reserve for EMI and close to HDMI CONN

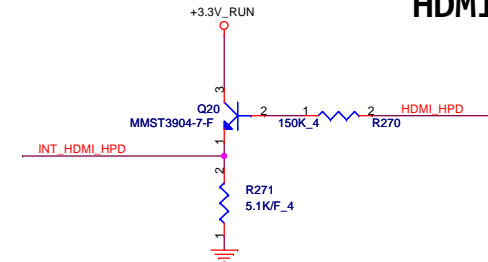


HDMI



HDMI_HPD spec VinH_min=2.0V

HDMI HPD

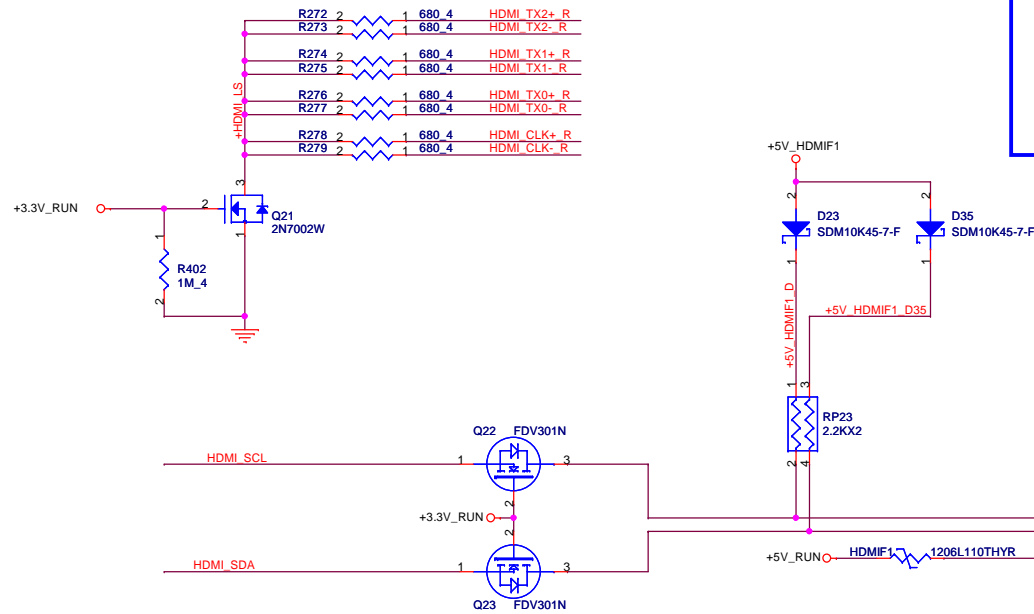


$$IB = (5V - 0.7V) / (150K + (70 + 1) 5.1K) = 8.4\mu A$$

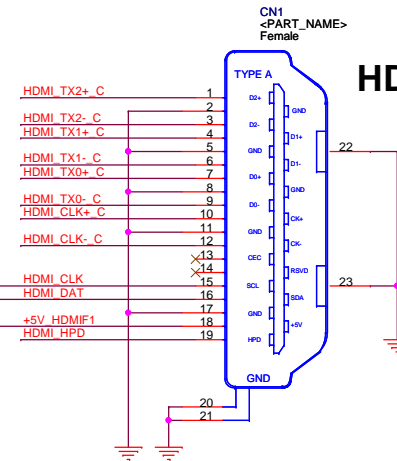
$$IE = (1 + 70) \times 8.4\mu A = 596.4\mu A$$

$$VE = 596.4\mu A \times 5.1K = 3.04V$$

$$B = 70$$



HDMI Conn.



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<http://laptopblue.vn>



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USB Power share

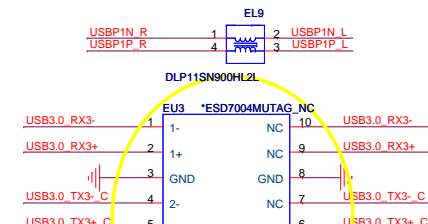
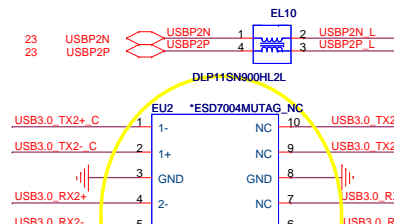
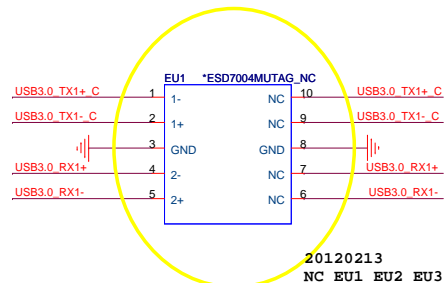
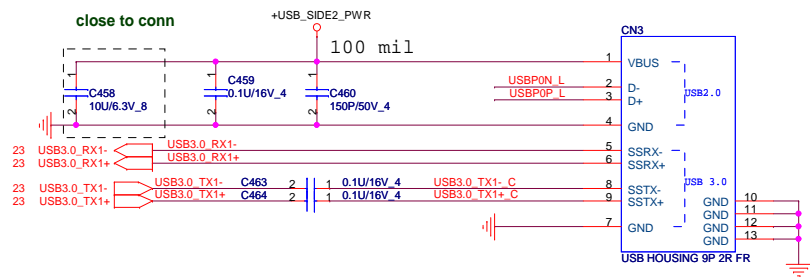
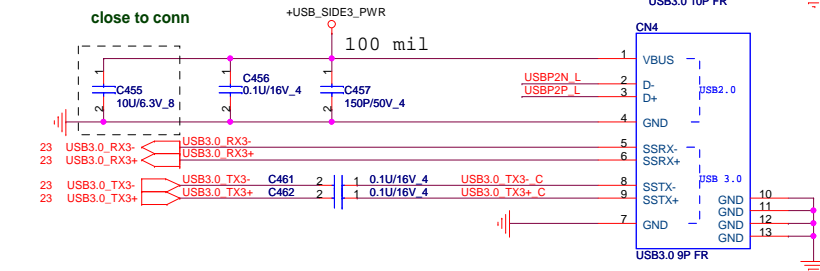
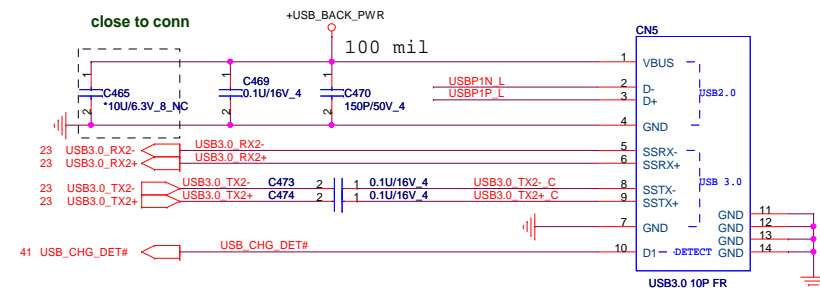
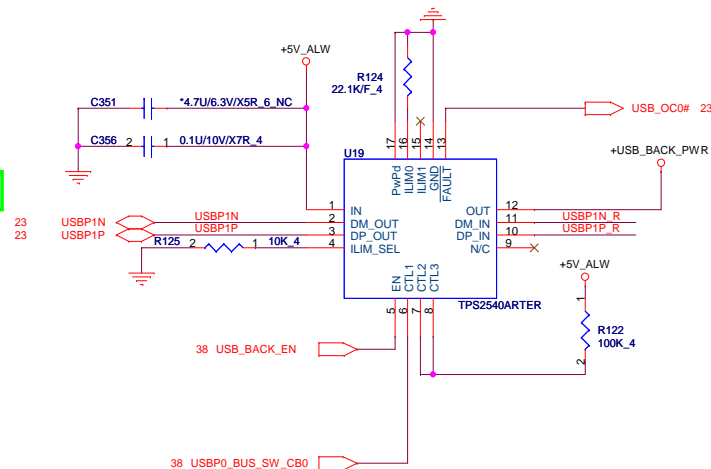
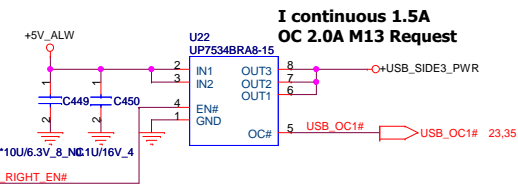
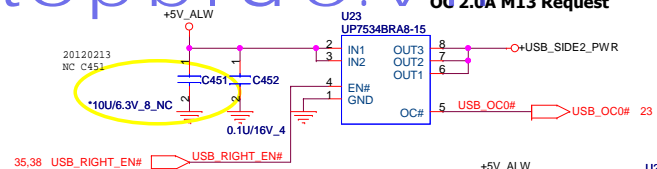
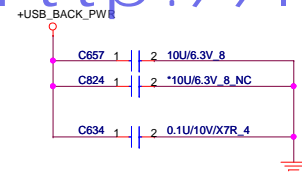
<http://laptopblue.vn>

I continuous 1.5A
OC 2.0A M13 Request

USBP0_BUS_SW_CB0	Mode	Operating at
Low	DCP, Auto-detect	S3/S4/S5, 1.5 A
High	CDP, BC Spec 1.1	S0, 1.5 A

	R109	mA
OC limitation	100k ohm	480
	22.1k ohm	2171

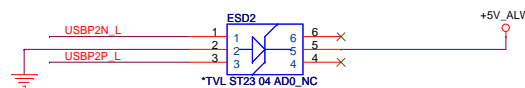
Applied Now



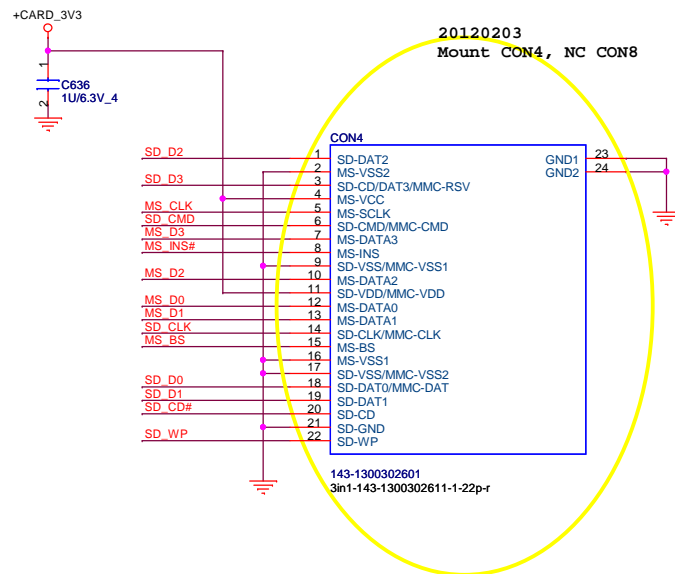
ESD Function

ESD Function

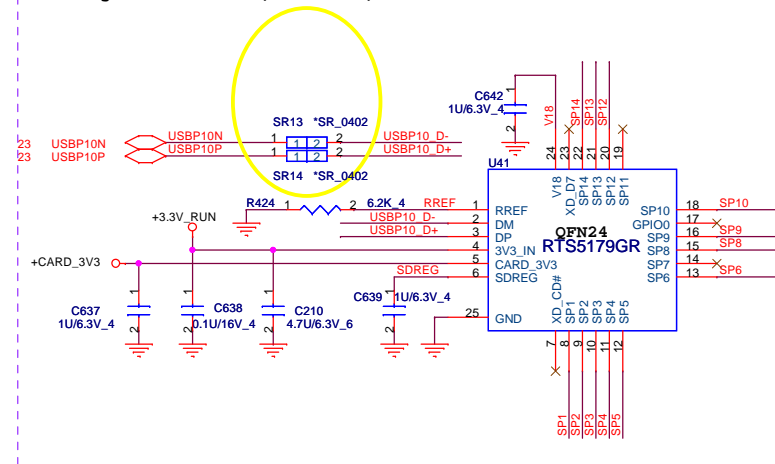
Place ESD diodes as close as USB connector.



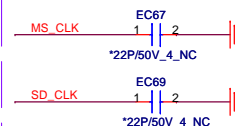
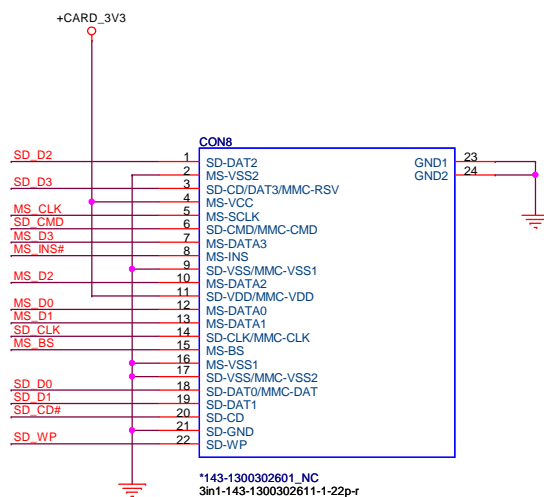
For Vostro Placement(V08,V08A)-Far ODD



20120206
Remove EL47
Change R210 to SR13(short0402)
Change R212 to SR14(short0402)



For INSPIRON Placement (R08,R08A,R08T)-Near ODD

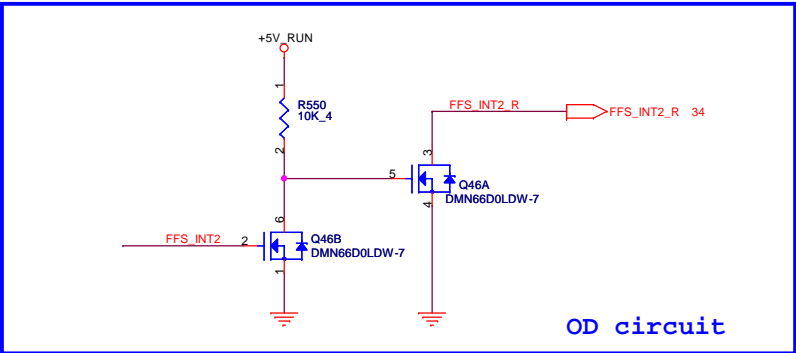


Share Pin

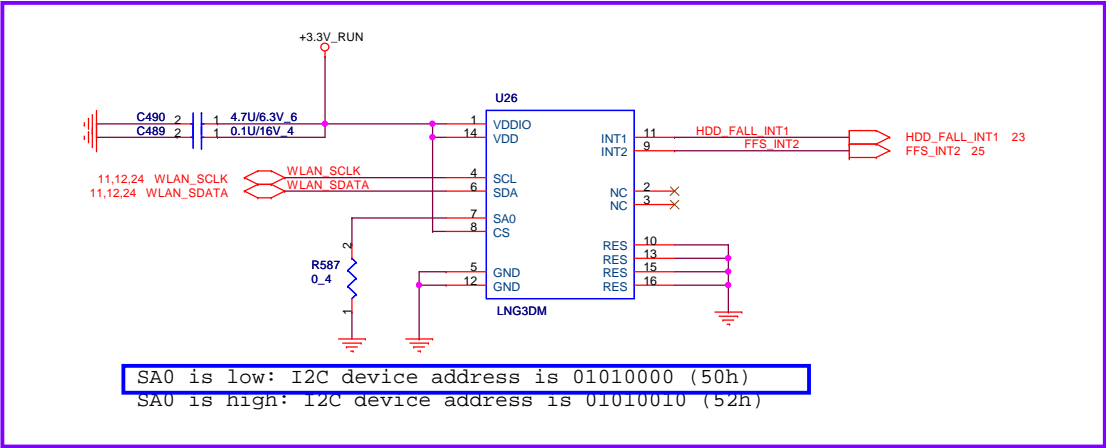
3-axis Fall Sensor

http://laptopblue.vn

If you have two HDD,need add two OD circuit for Fall sensor interrupt circuit



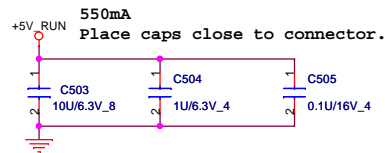
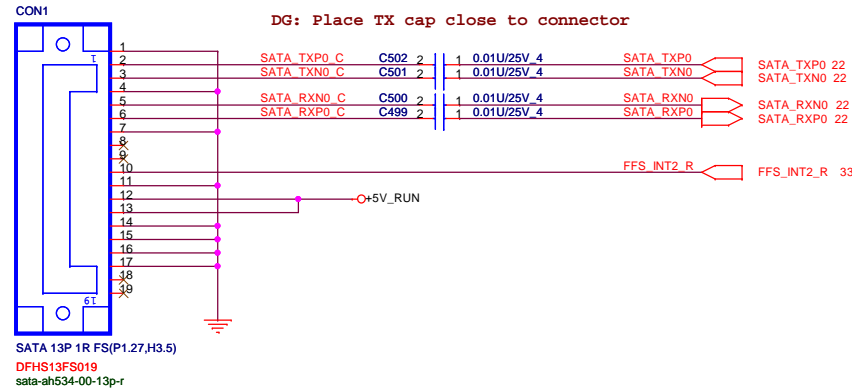
20120203
Mount Function code "FFS" part



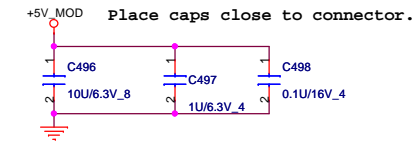
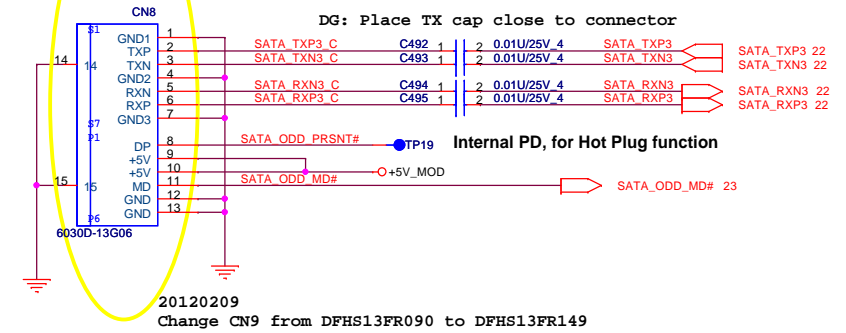
HDD

http://laptopblue.vn

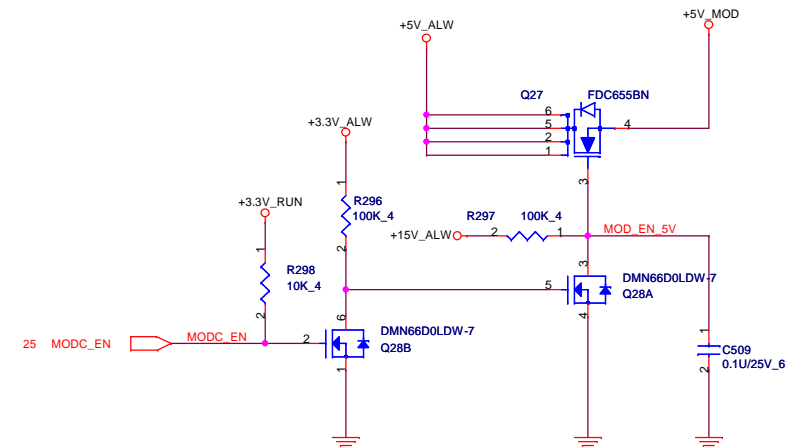
ODD



ODD Connector



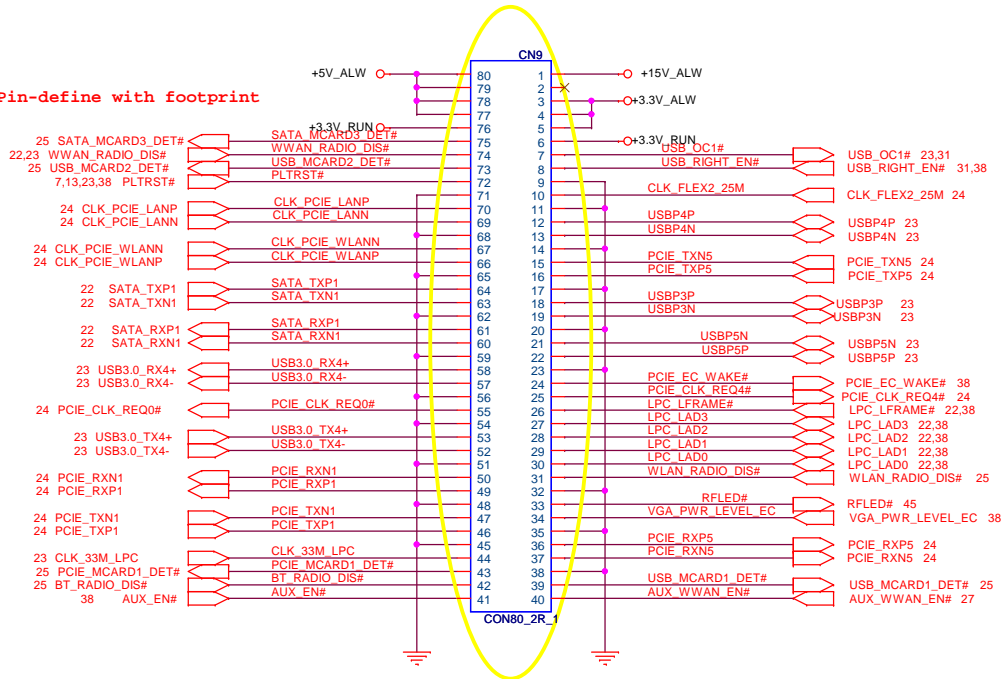
Support Zero power ODD



20120203

Change CN9 footprint from "88069-8001b-bs-80p-ldh" to "88069-8001b-bs-80p-ldh-smt"

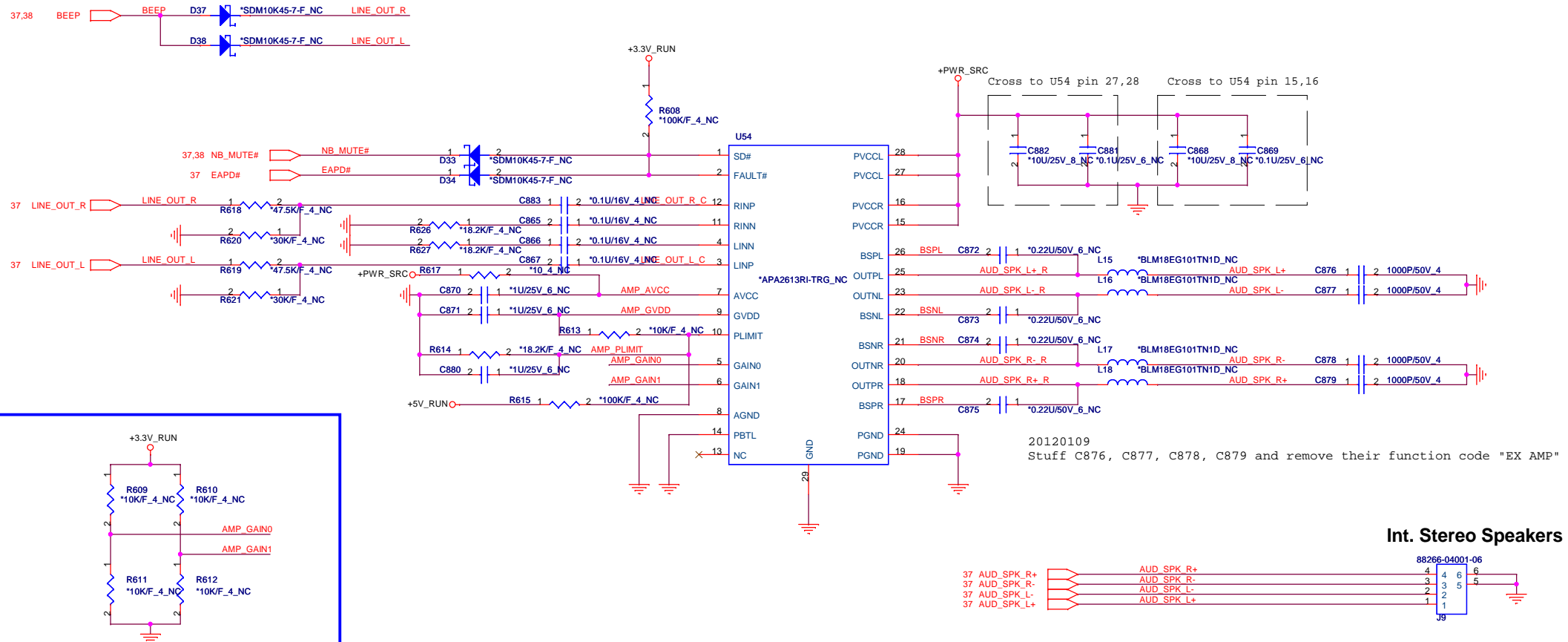
Check Pin-define with footprint



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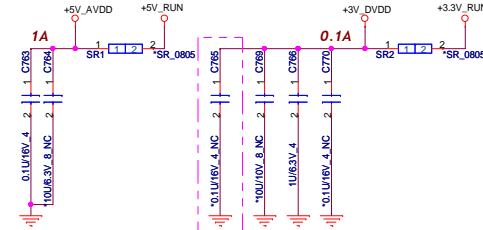
PROJECT : R08

ANPEC APA2613 is P2P to TI TPA3113
Default use APA2613

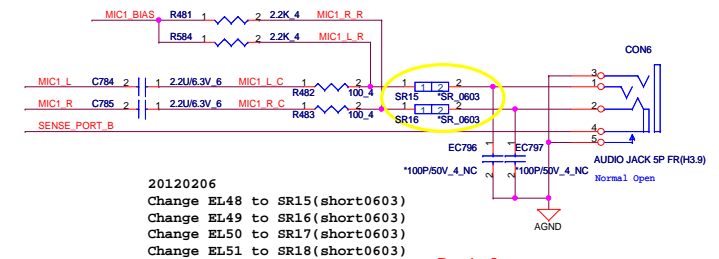


GAIN1	GAIN0	AMPLIFIER GAIN (dB)
		TYP
0	0	20
0	1	26
1	0	32
1	1	36

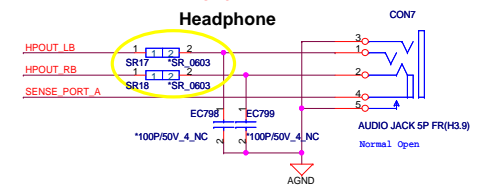
	Amplifier	Function code
R08/R08A/V08/V08A	CODEC CX20672	Mount "IN AMP"
R08T	APA2613 or TPA3113	Mount "EX AMP"



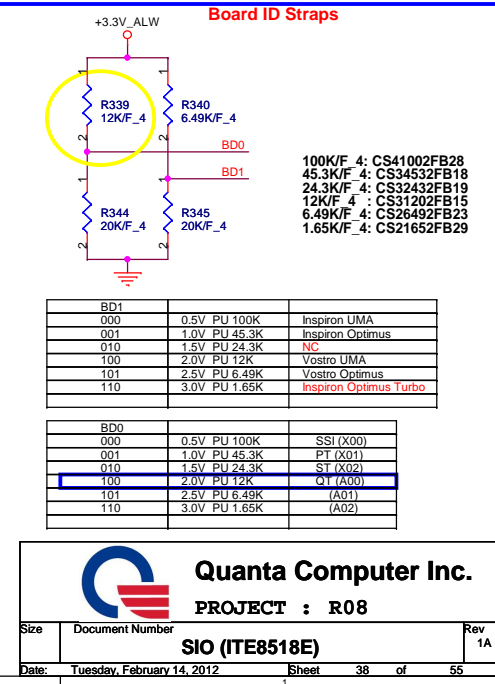
Port B
External Stereo microphone



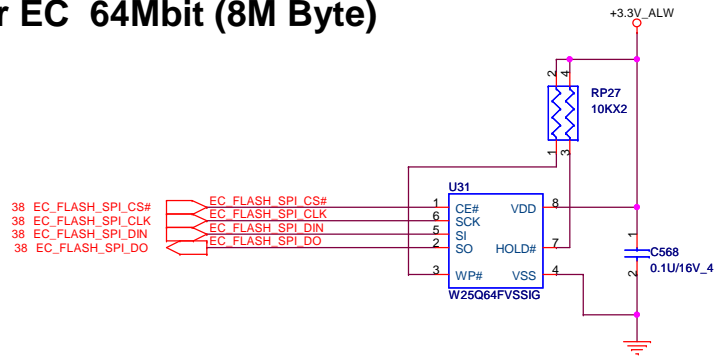
Port A
Headphone CON7



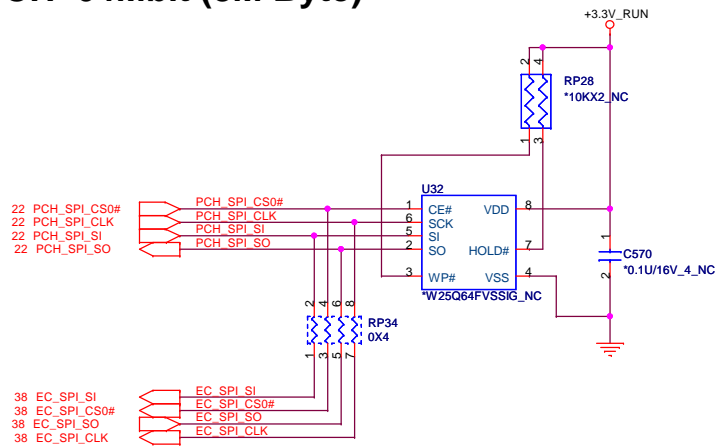
Flow PDC pin define



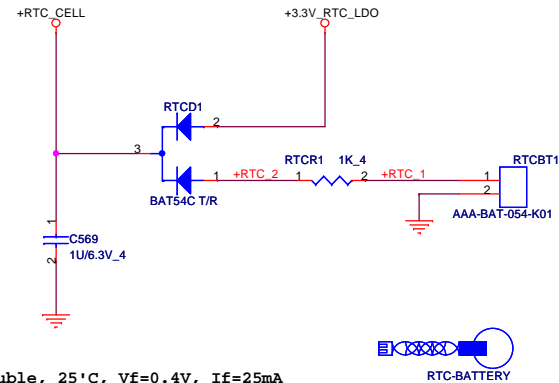
For EC 64Mbit (8M Byte)



For PCH 64Mbit (8M Byte)



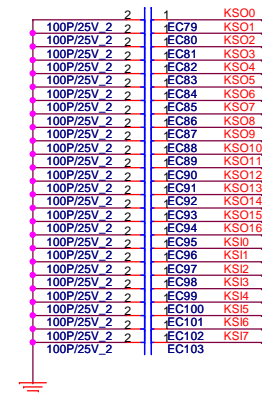
RTC



Double, 25°C, Vf=0.4V, If=25mA
one, 25°C, Vf=0.35V, If=15.8mA

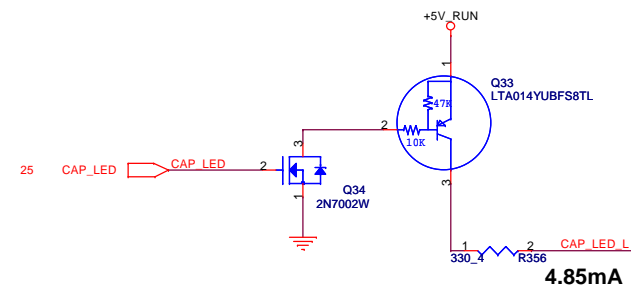
HotKey CONN

Pin connection diagram for the FZ46-30BC-60-H LED strip. The diagram shows a blue PCB with 32 pins. Pin 1 is labeled 'JKB1'. Pins 2-31 are labeled with various signals: KS17, KS18, KS19, KS14, KS12, KS15, KS11, KS13, KS10, KS09, KS04, KS07, KS06, KS08, KS03, KS01, KS02, KS00, KS012, KS016, KS015, KS013, KS014, KS09, KS011, KS010, CAP_LED_L, and pins 28-30. Pins 31 and 32 are labeled '31' and '32' respectively. The diagram also shows a red wire connected to pin 22, labeled 'KB_DET#'. A blue wire is connected to pin 38, labeled 'KSO[0..16]'. A red wire is connected to pin 39, labeled 'KS[0..7]'. The bottom of the diagram shows a red wire connected to pin 30, labeled 'FZ46-30BC-60-H'.

[illegible]

20120203
Mount C575 J5

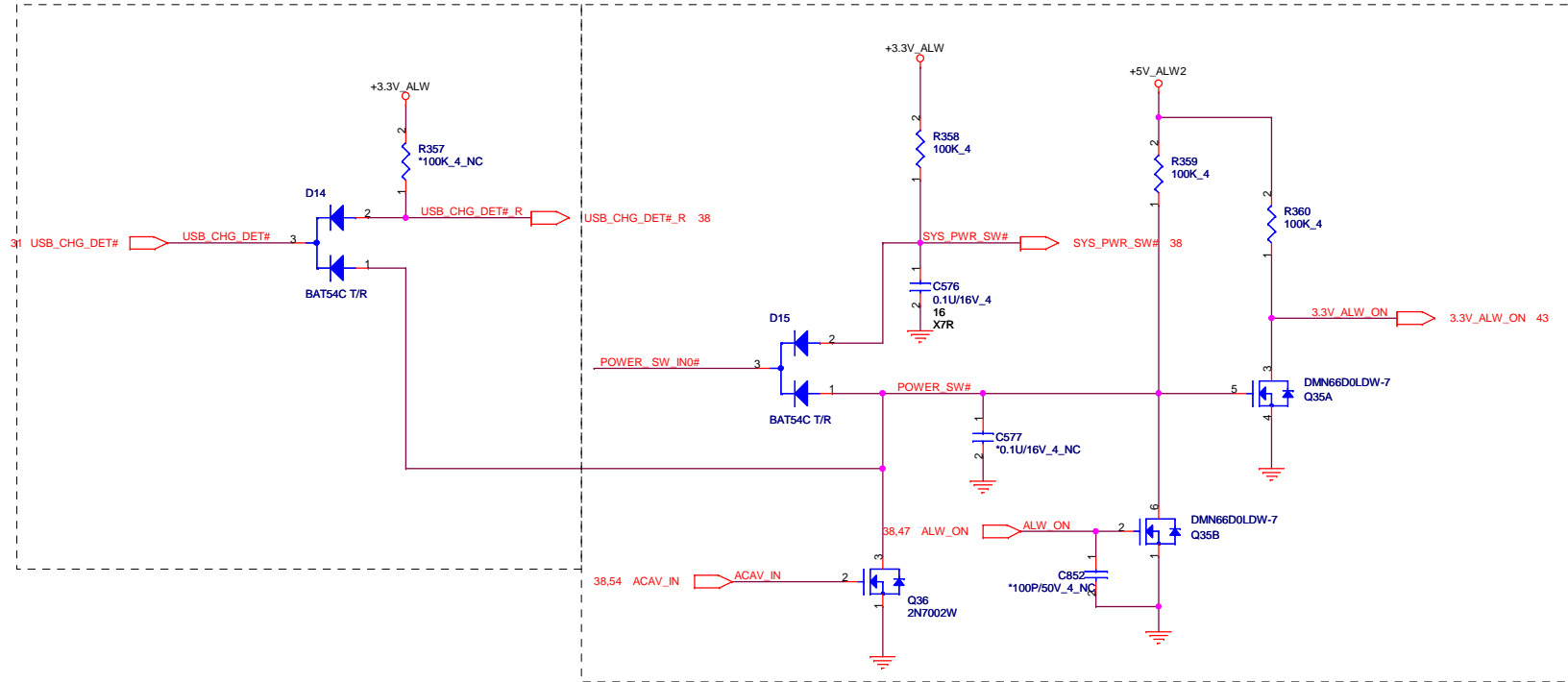
Vi(on_max)= -1.4V
Vi(off_min)=-0.3



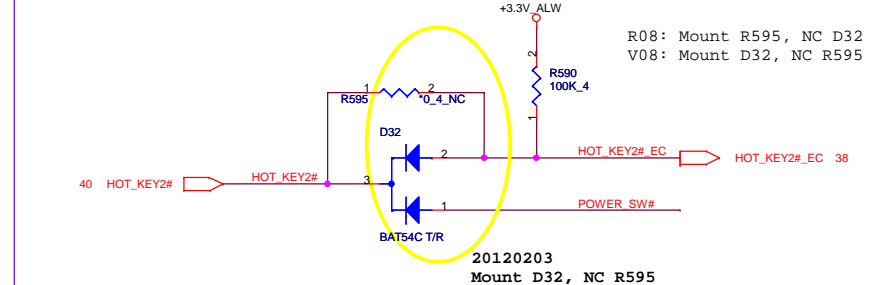
Sheet 40 of 55

For USB charger usage

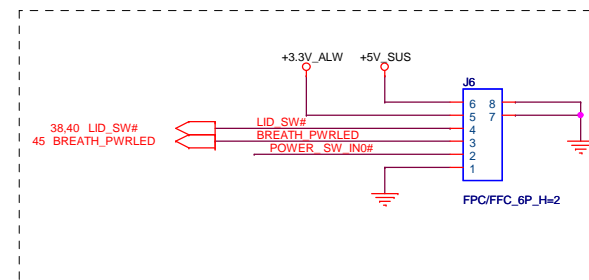
3V ALW ON POWER LOGIC

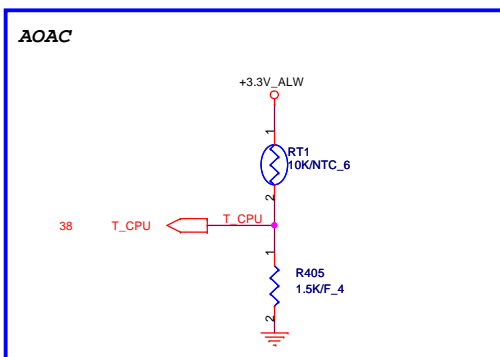


HOT_KEY2 support Pre-Boot Recovery



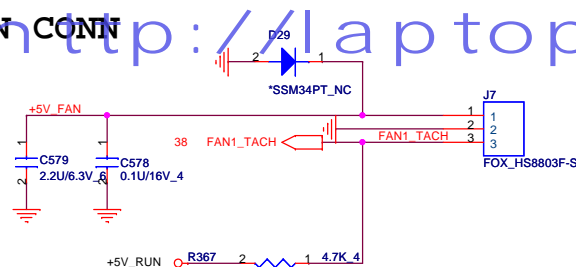
TO PWR button board





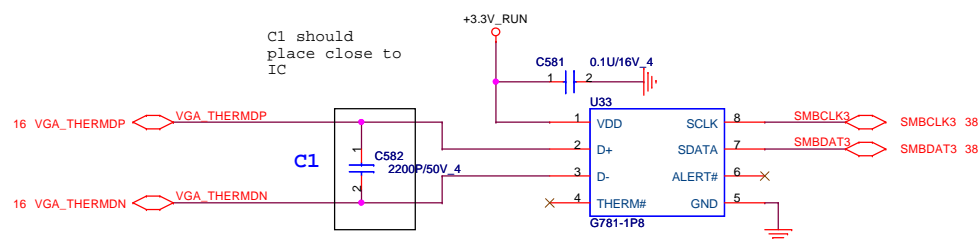
20120203
Mount RT1 R405 for V08A SKU

FAN CONT



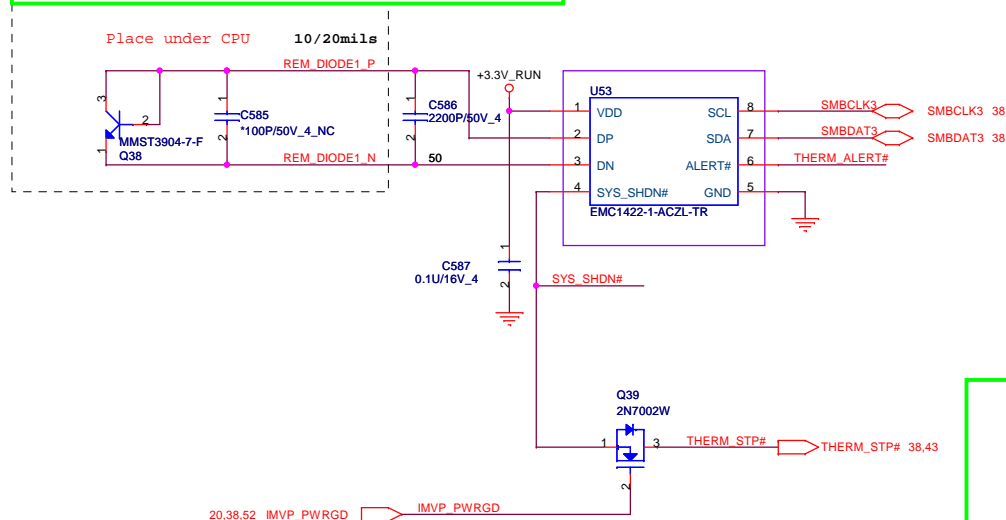
G781-1P8

SMBus address is 1001101xb (9Ah) (x is R/W bit).



THERMAL IC

1. Place C586 close to EMC1422-U1
 2. Place C585 to be close to Q38
- Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C586, then C585 should be dummy

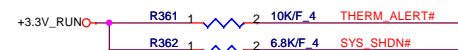


EMC1422 SMBus address is 1001_100xb (98h) (x is R/W bit).

SYS_SHD#	4.7K	6.8K	10K	15K	22K	33K
ALERT#	4.7K	77'C	83'C	89'C	95'C	101'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C

CHECK OTP WITH Thermal.

OTP 85 degree C



EMC1422

OTP 85 degree : R361 = 10K, R362 = 6.8K
OTP 90 degree : R361 = 6.8K, R362 = 10K

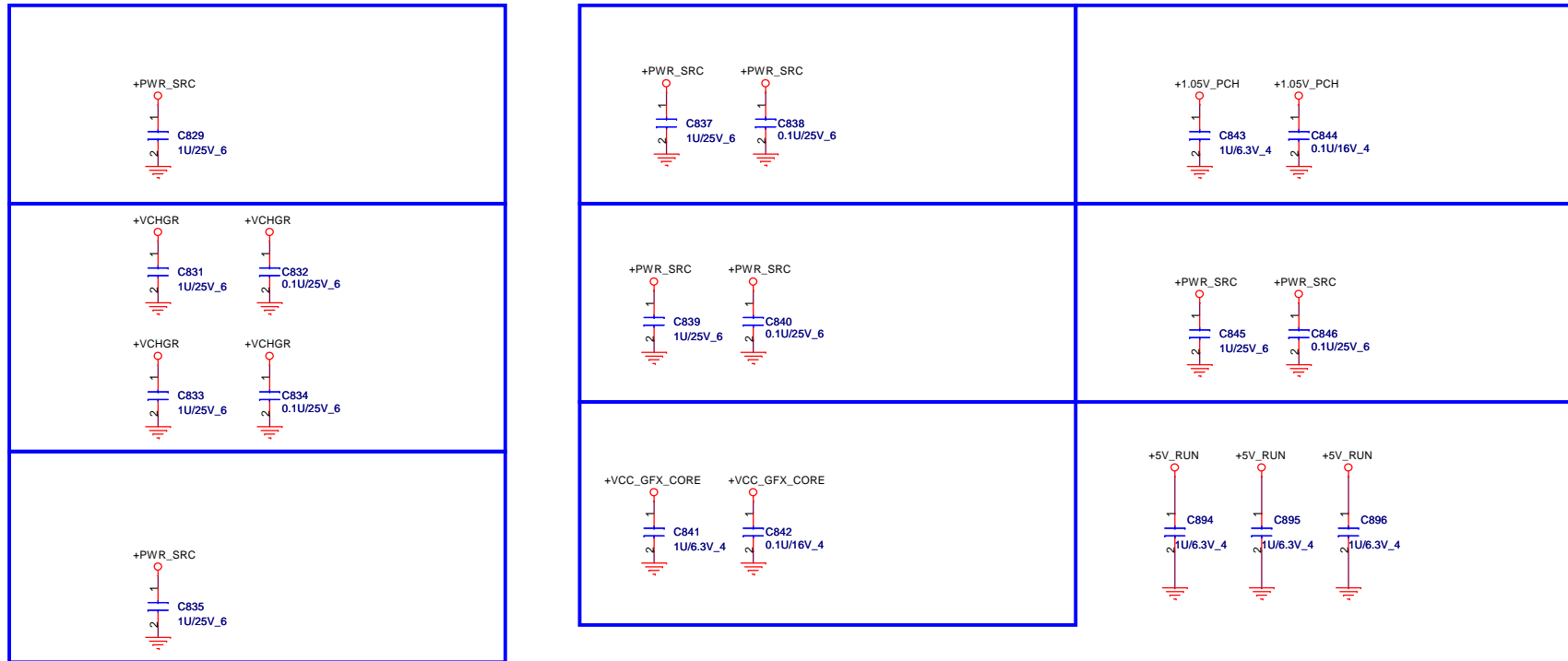
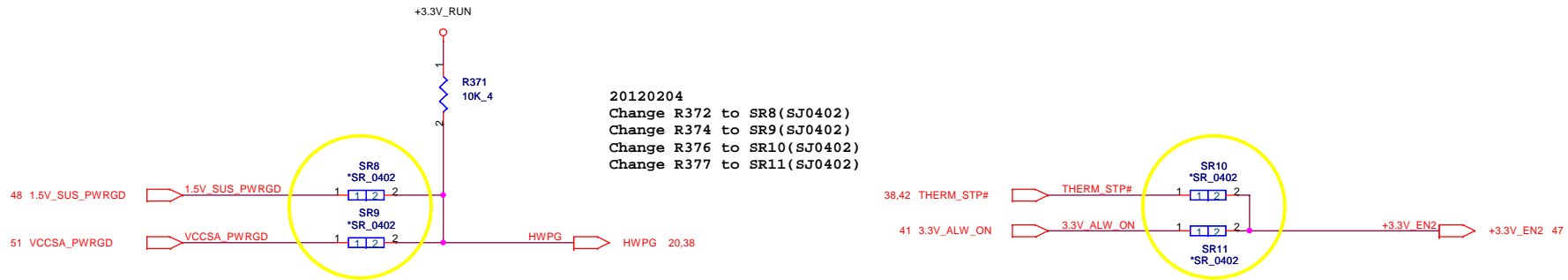
NTC7718W

OTP 85 degree : R361 = 18.7K, R362 = 2K
OTP 91 degree : R361 = 10.5K, R362 = 7.5K



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PROJECT : R08



h t t p : / / l a p t o p b l u e . v n

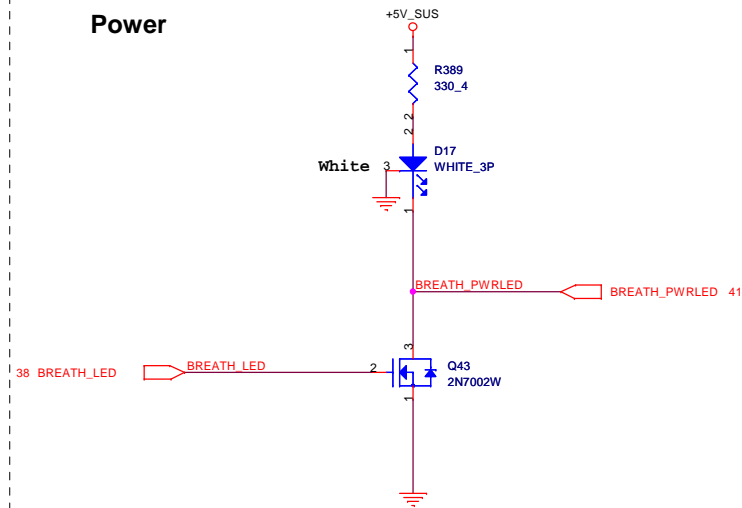


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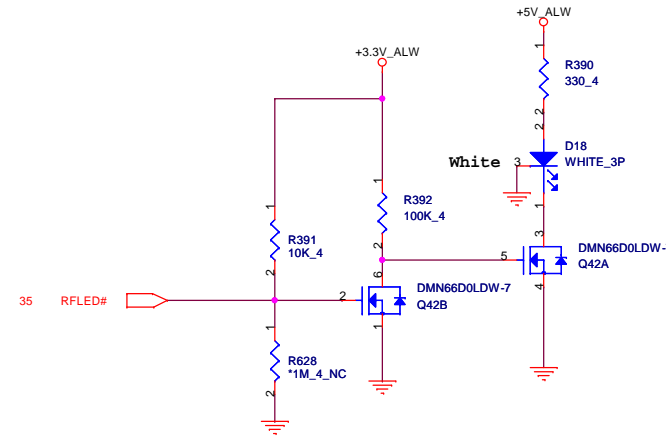
PROJECT : R08

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	MiniCard	1A
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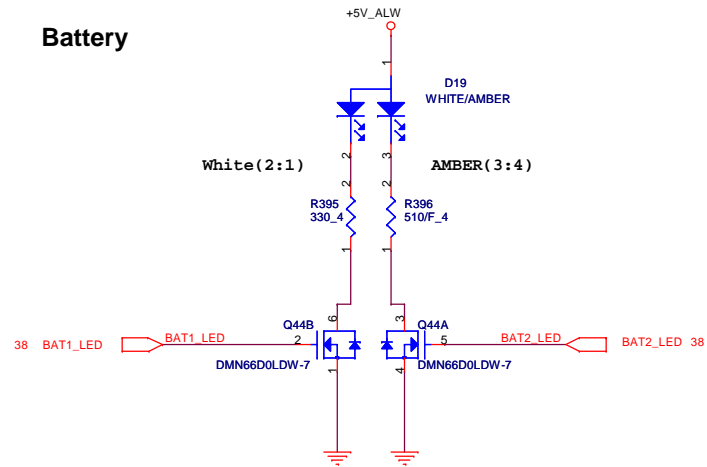
Power



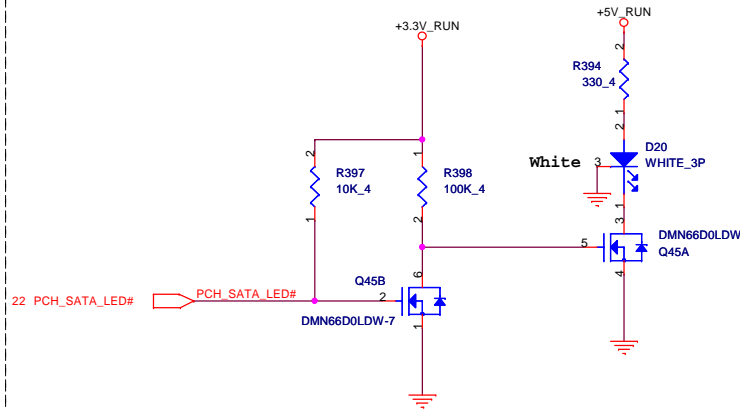
Bluetooth / WLAN on/off LED



Battery



HDD activity LED.

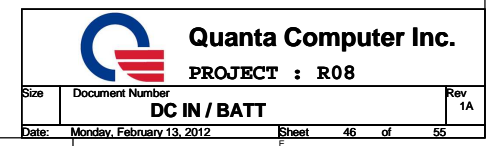


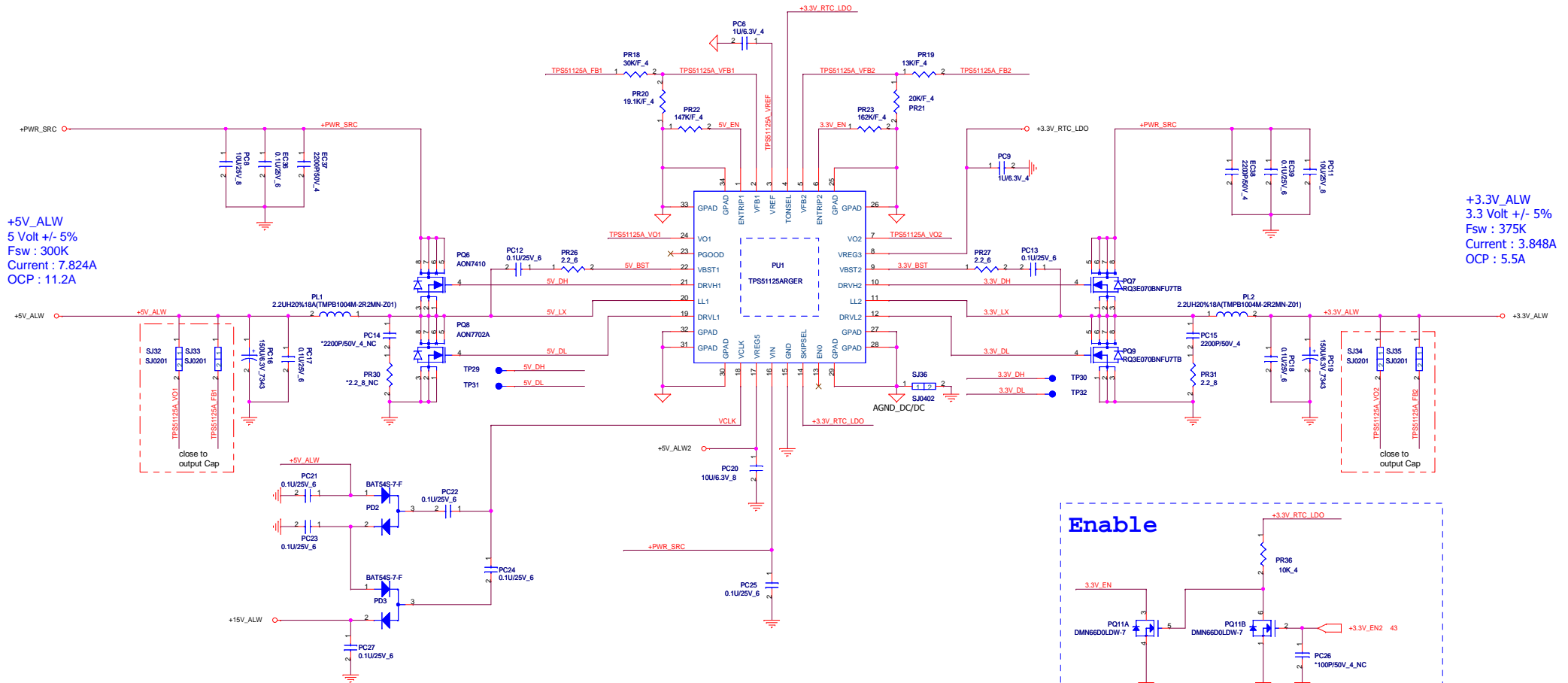
Quanta Computer Inc.

PROJECT : R08

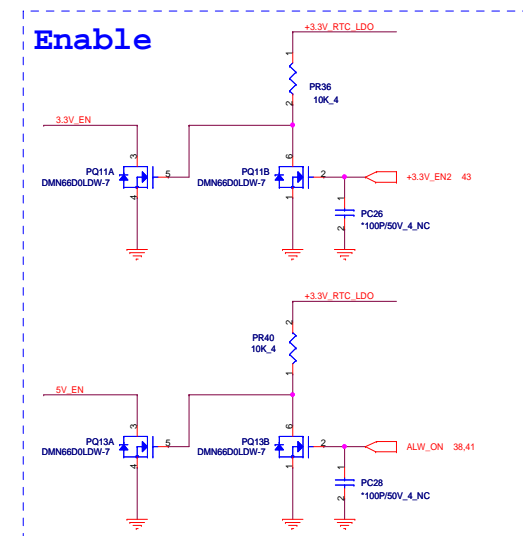
Size	Document Number	Rev
		1A
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LED

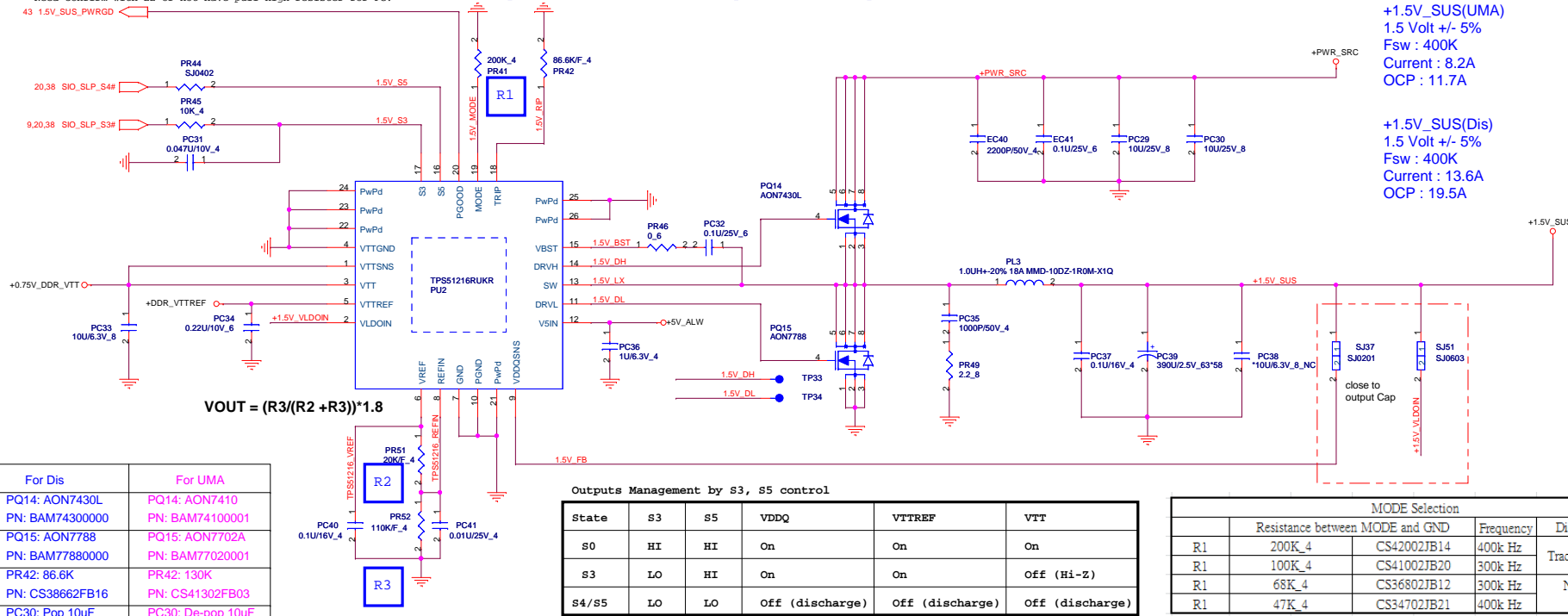




TPS51125A TONSEL Connection and Switching Frequency				
Ton	REG5	REG3	VREF	GND
Channel1 Fs	365 kHz	300 kHz	245 kHz	200 kHz
Channel2 Fs	460 kHz	375 kHz	305 kHz	250 kHz



Need confirm with EE or not have pull high resistor for PG.

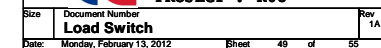


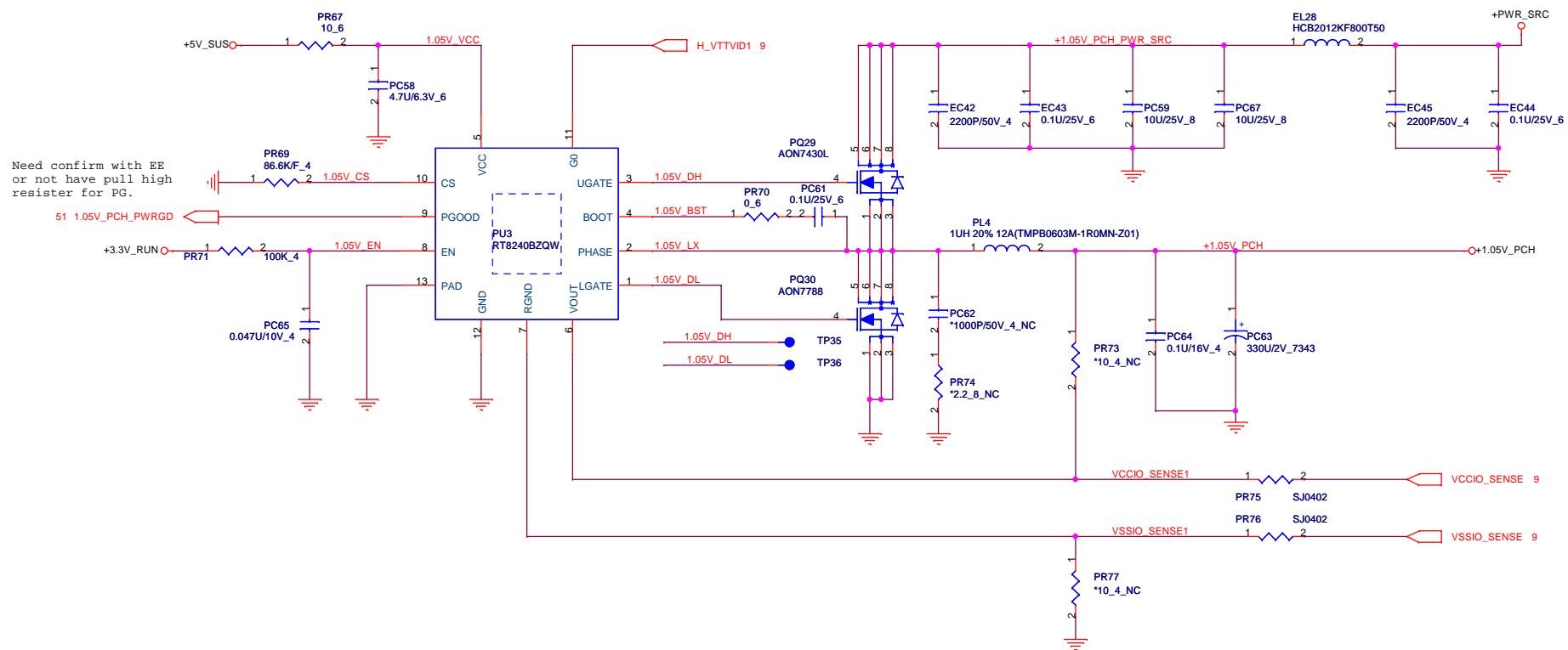
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PROJECT : R08

Size	Document Number	Rev
1.5	SUS/0.75_DDR_VTT (TPS51216RUKR)	1A

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+1.05V_PCH
1.05 Volt DC +/- 2%
Fsw : 400K
TDC : 13.5A
OCP : 19.5A

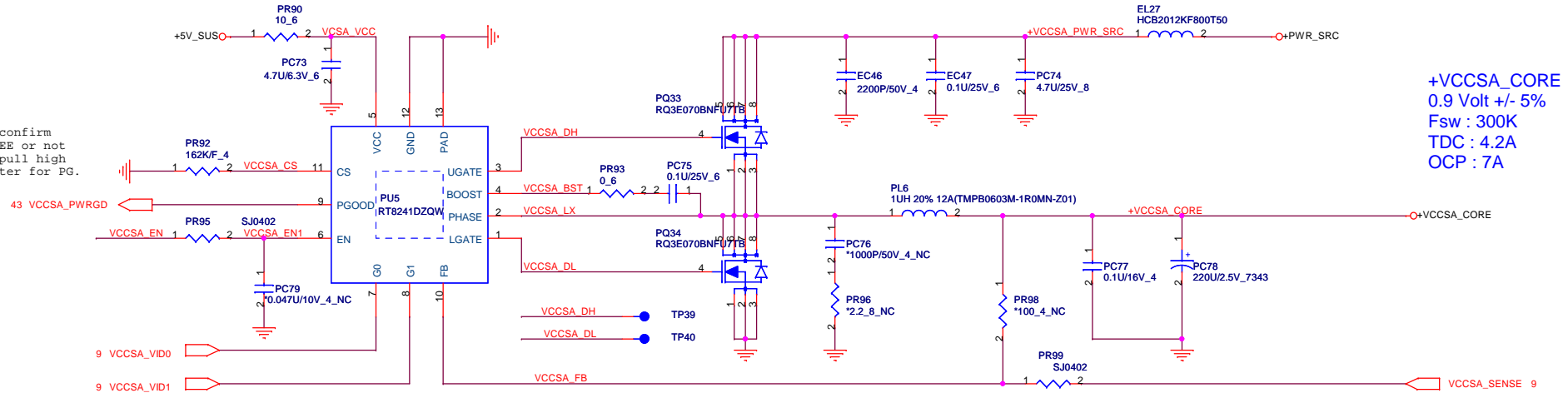


Quanta Computer Inc.

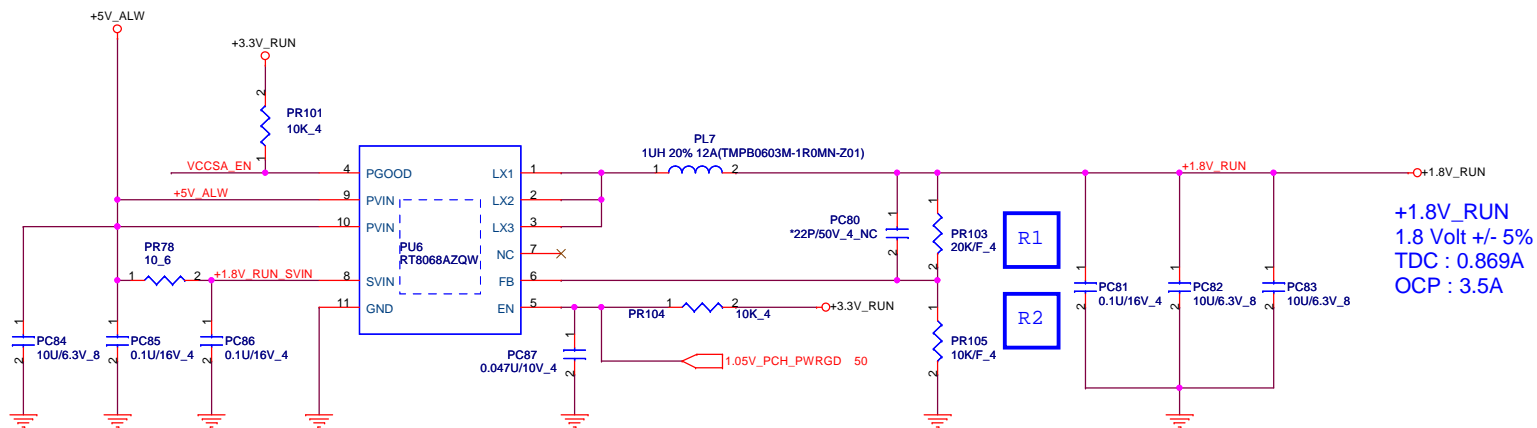
PROJECT : R08

Size	Document Number	Rev
	+1.05V_PCH / VTT (RT8240BGQW)	1A
Date:	Monday, February 13, 2012	Sheet 50 of 55

Need confirm
with EE or not
have pull high
resistor for PG.



VCCSA_VID1	VCCSA_VID0	VCCSA_CORE
Low	Low	0.9V
High	Low	0.8V
Low	High	0.725V
High	High	0.675V



$$VOUT = 0.6(1+R1/R2)$$

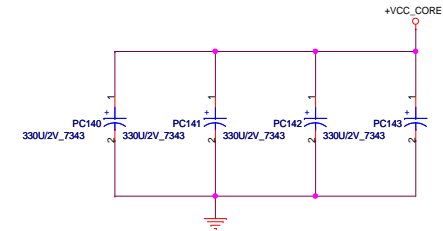
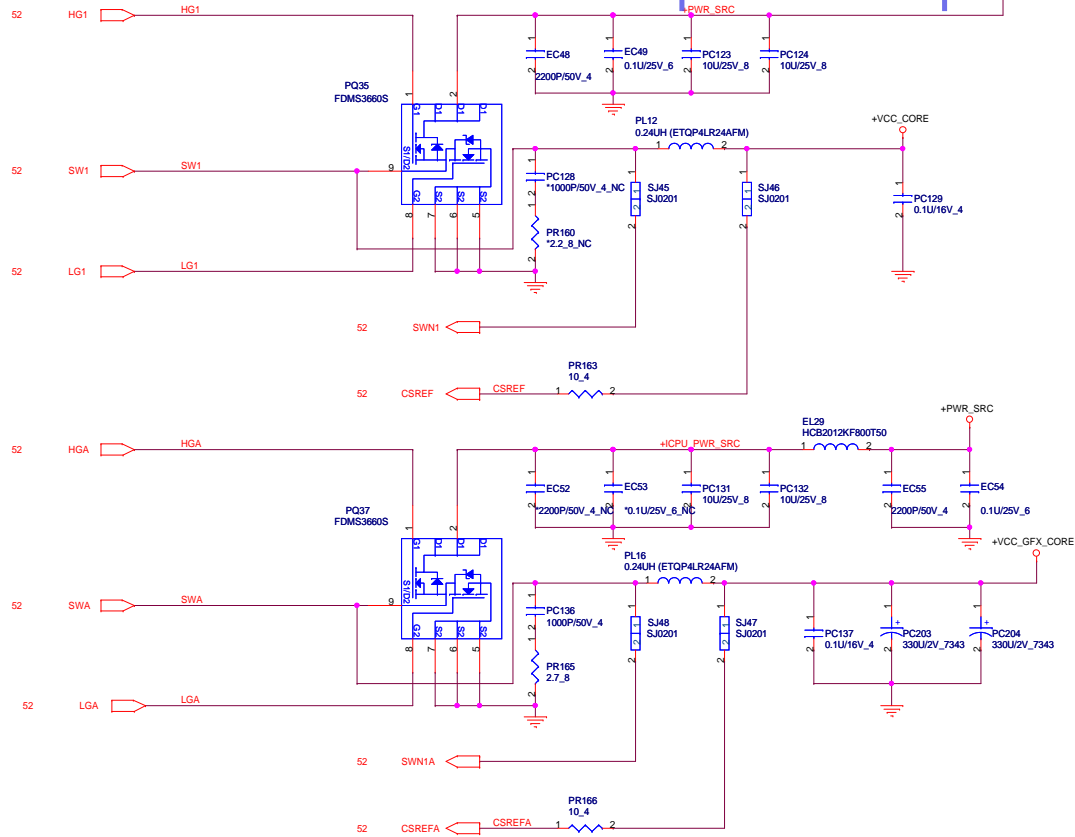


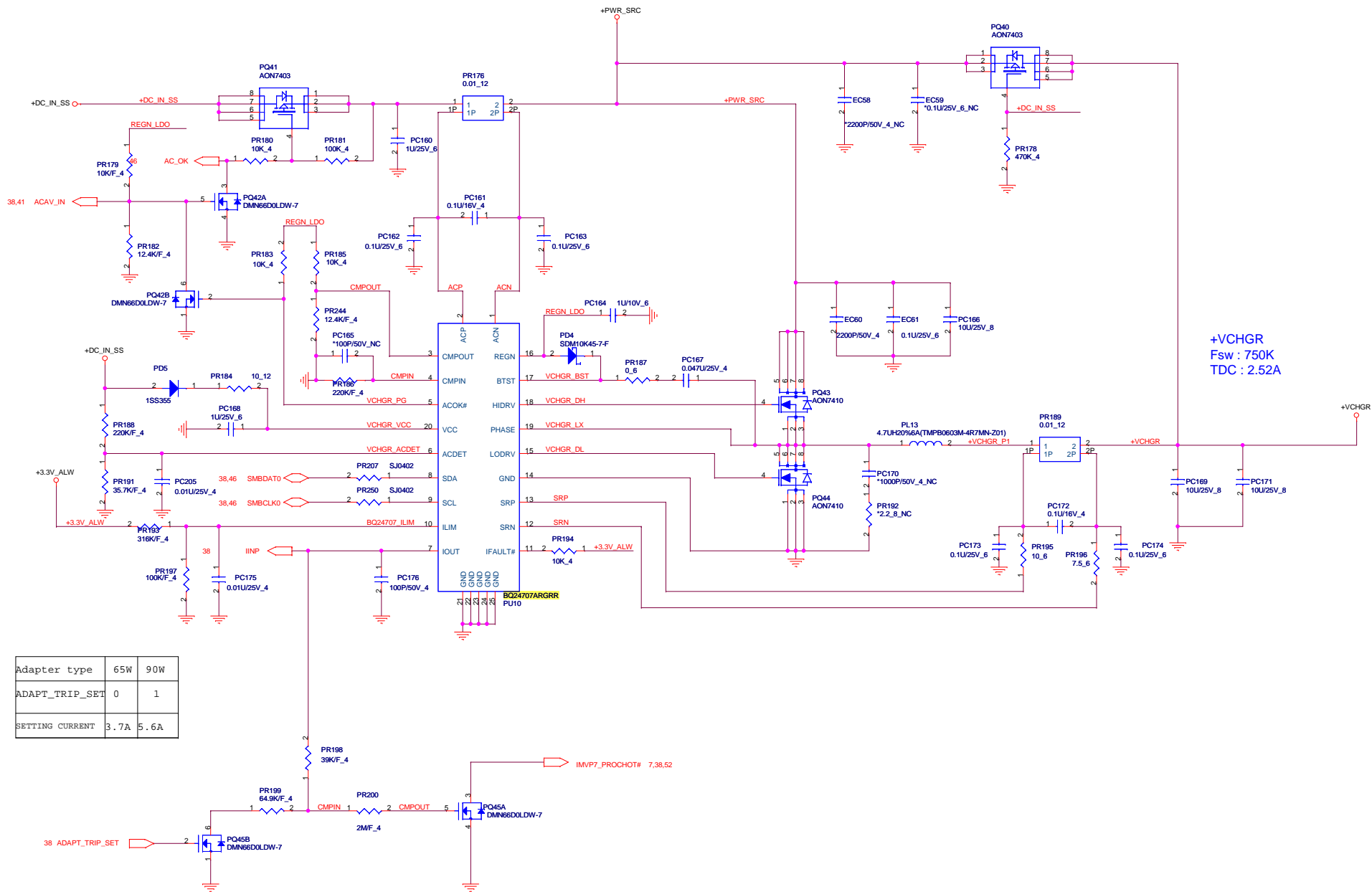
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PROJECT : R08

CPU Power

<http://laptopblue.vn>





Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A

+VCC_GFX_CORE
Fsw : 400K
Current : 50A
OCP : 60A

