SAMOA(DDR3)

CPU : PENRYN SFF
Chip Set : CANTIGA GS & ICH9M SFF
Remarks : INTEL MONTEVINA SFF

Model Name : SAMOA
PCB Part No : BA41-00905A(Nanya)
BA41-00906A(GCE)
Dev. Step : PR/MP
Revision : 1.1
T.R. Date :

DRAW	CHECK	APPROVAL
Jun PARK	HJ KIM	JS EUH

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DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN COVER	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
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BLOCK DIAGRAM

Revision 1.0

CPU
PENRYN SFF(ULV)
1.2GHz/1.4GHz
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800MHz FSB

CLOCK GENERATOR
CK-505M
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LED LCD(AMLCD)
13.3" (1280x800)
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LVDS

LPC I/F
LPC47N207
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TPM 1.2
SLB9635TT1.2
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GMCH
CANTIGA GS
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VGA — MUX PI5V330QX

PCI E GFX(Channel B) — MUX & LEVEL SHIFTER PI3HDMI412AD

PCI E GFX(Channnel C)

800/1066 MHz

DDR3-SODIMM x 2
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HDA 2nd

1.8" SATA HDD
Page 25

SATA0

652 BGA Type

ICH
ICH9M SFF
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SATA1

USB2.0

P8 — USB2.0

BLUETOOTH

P4

MINI CARD2
HSDPA
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P11 — Channel 2

MINI CARD1
Wireless LAN
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P10 — Channel 1 — PCIe

PCIe — Channel 4

SPI

SPI ROM
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Gigabit LAN Controller
88E8055

MUX
PI3L500ZFE

RTC Batt.

2P
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HDA 1st

LPC

MICOM
H8S/2111B
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SYNAPTICS
TOUCHPAD

KEYBOARD
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SUB_RIGHT

CRT
Page sub_9

HDMI
Page sub_10

Power S/W

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P6 — USB (RIGHT2)
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P5 — **CARDREADER**
ALCOR AU6371
Page sub_12

7-in-1
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FINGER PRINT BOARD

P9 — **FINGER PRINT**
Page sub_14

SUB_LEFT

Phone Int MIC

AC'97 CODEC
ALC262-VC2-GR
Page sub_4

HDA 1st

Audio AMP
TPA6017A2
Page sub_5

L — R

Page sub_7 — **EXPRESS CARD** — P7 — Channel 3

USB (LEFT)
Page sub_7 — P0

LAN BOARD

Transformer

RJ45

LAN JACK
Page sub_13

DOCK

DOCK CONNECTOR

P2, P3

- CRT
- DVI
- DP
- eSATA
- HUB x 2
- DOCK LAN Transformer

DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN BLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
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POWER SEQUENCE

Revision 1.0

DDR3 Memory (Sheet 16-17)
9) P1.5V_AUX
29) KBC3_CPURST#

RTC Battery
PRTC_BAT
CHP3_RTCRST#
6) P3.3V_AUX
PRTC PRTC
LAN100_SLP
INTVRMEN

POWER S/W
5) KBC3_CHKPWRSW#

KBC
110ms Delay
11) CHP3_SLPS5#/4#/3#
10) KBC3_RSMRST#
10) KBC3_PWRBTN#
26) KBC3_PWRGD
28) CHP3_SUSSTAT#
24) VRM3_CPU_PWRGD
6) KBC3_SUSPWR
13) KBC3_PWRON
20) KBC3_VRON

ICH9-M (Sheet 22-25)
18) P1.05V
16) P1.5V
25) CHP3_CLK_PWRGD
24) VRM3_CPU_PWRGD
VRMPWRGD
PWROK
27) CPU1_PWRGDCPU
30) PLT3_RST#
PCI3_RST#

CK-505M (Sheet 6)

Pre FCT PORT
2) VDC
18) P1.05V
14) P3.3V
15) P5.0V
6) KBC3_SUSPWR
16) P1.5V
24) VRM3_CPU_PWRGD
27) CPU1_PWRGDCPU
31) CPU1_CPURST#
GND

WLAN
16) P1.5V
14) P3.3V
30) PLT3_RST#

WLAN
7) P3.3V_AUX
14) P3.3V

LCD
LCD_VDD3.3V
LED_VOUT

HDD
14) P3.3V
15) P5.0V

Adapter
Battery
AC_DC / Battery
ISL6256
2) VDC
2-1) P12.0V_ALW
4) MICOM_P3V
6) KBC3_SUSPWR

P3.3V_AUX & P5V_AUX
TPS51120
7) P3.3V_AUX
8) P5.0V_AUX
3) P5.0V_ALW
4) MICOM_P3V

CHP3_DPRSLPVR
CPU1_DPRSTP#
IGFX_CORE
SC472 (Sheet 38)
2) VDC
14) P3.3V
19) VCCP3_PWRGD
23) VCC_CORE
24) VRM3_CPU_PWRGD

CPU (Sheet 7-9)
23) VCC_CORE
18) P1.05V
16) P1.5V
31) CPU1_CPURST#

P1.5V_AUX
For DDR3 Power
SC486 (Sheet 36)
7) P3.3V_AUX
6) KBC3_SUSPWR
9) P1.5V_AUX
MEM1_VREF
P0.75V

GMCH (Sheet 11-15)
26) KBC3_PWRGD
PWROK
CL_PWROK
30) PLT3_RST#
9) P1.5V_AUX
14) P3.3V
22) IGFX_CORE

P1.05V
For VCCP_CORE
SC4624 (Sheet 37)
8) P5.0V_AUX
20) KBC3_VRON
18) P1.05V
19) VCCP3_PWRGD

SI3456 (Sheet 41)
7) P3.3V_AUX
13) KBC3_PWRON
13-1) KBC3_PWRON_INV#
14) P3.3V

IGFX_CORE
SC472 (Sheet 38)
2) VDC
14) P3.3V
21) MCH3_GFX_VR_EN
22) IGFX_CORE
VCCP3_PWRGD

PCIe Devices
10-1) P3.3V
10-1) P1.8V
10) P1.5V

AP6680GAM (Sheet 41)
8) P5.0V_AUX
13-1) KBC3_PWRON_INV#
15) P5.0V

MIC5219B (Sheet 41)
10-1) P3.3V
13) KBC3_PWRON
17) P1.8V

SI3456 (Sheet 41)
9) P1.5V_AUX
13) KBC3_PWRON
16) P1.5V

For LCD Power
TPS61181 (Sheet 40)
2) VDC
2-2) VDC_LED
0 ohm
LCD3_BKLTON
LCD3_PWMBIA
LED_VOUT

DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN POWER SEQUENCE	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
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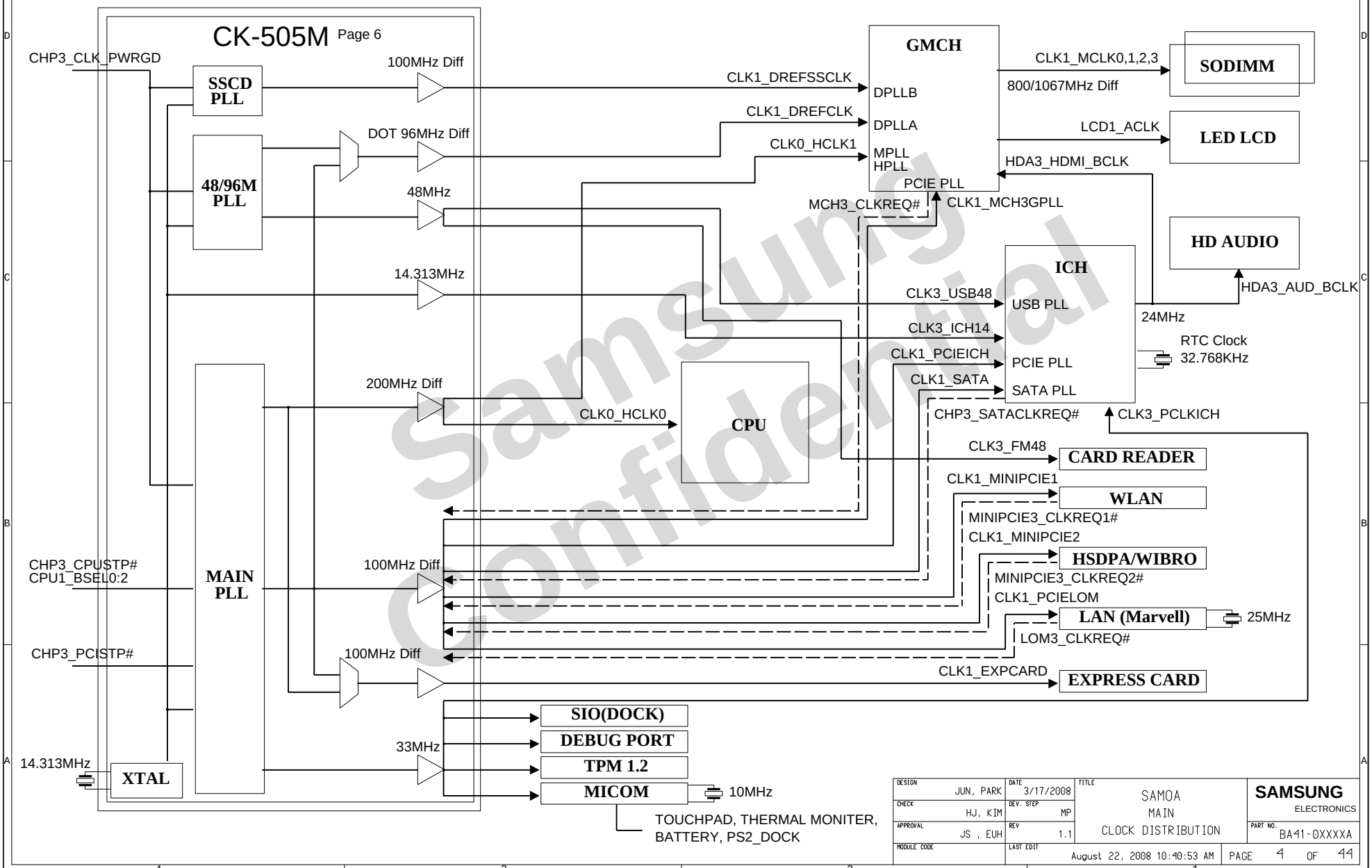
CLOCK DISTRIBUTION

Revision 1.0



DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN CLOCK DISTRIBUTION	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
USB	AD29(internal)	Programable	
LPC Bridge/IDE/AC97/SMBUS	AD31(internal)		
Internal MAC	AD24(internal)		

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9M	**Master**		**SMBUS Master**
CK-505M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000X	A0h	-
SODIMM1	1010 001X	A4h	
PI3HDMI412AD	1010 001X	C0h	
MICOM	**Master**		-
			-
BATTERY	0001 011X	16h	
EMC2102	0111 101X	7Ah	

USB PORT Assign

Port Number		ASSIGNED TO	Port Number		ASSIGNED TO
UHCI_0	0	USB PORT (LEFT)	UHCI_3	6	USB PROT (RIGHT2)
	1	USB PORT (RIGHT1)		7	EXPRESS CARD
UHCI_1	2	USB HUB1 (DOCK)	UHCI_4	8	CAMERA
	3	USB HUB2 (DOCK)		9	FINGER PRINT
UHCI_2	4	BLUETOOTH	UHCI_5	10	WLAN for Combo
	5	AU6371		11	HSDPA

System Power States

Power Rail	Devices (Page Number)
P5.0V	EMC2102 (10) ICH9M (21) 1.8" SATA HDD (25) MICOM (26) Pre FCT PORT (32) DISCHARGE, CAMERA, TOUCHPAD (33) SC472 (38) SC454 (39) AP6680 (41) PI5V330QX (24,42) HDMI CONN. (SUB_10) CRT CONN. (SUB_9)
P3.3V	CK505M (6) FAN (10) CANTIGA GS (14) SPI ROM (19) ICH9M (21) LED LCD (23) 1.8" SATA HDD (25) WLAN (29) HSDPA (30) PI3HDMI412AD (31) Pre FCT PORT (32) DEBUG PORT, Pre FCT PORT & WHITE LED (32) DISCHARGE & BLUETOOTH (33) SWITCHED (41) LPC47N207 (43) ALC262-VC2 (SUB_4) R5538 (SUB_7) POWER S/W LED (SUB_11) AU6371 (SUB_12) AES1610 (SUB_14)
P1.8V	CANTIGA GS (14) DISCHARGE (33) SWITCHED (41)
P1.5V	CK505M (6) PENRYN ULV (8) CANTIGA GS (14) ICH9M (21) WLAN (29) HSDPA (30) Pre FCT PORT (32) DISCHARGE (33) SWITCHED (41) ALC262-VC2 (SUB_4) R5538 (SUB_7)
P1.05V	PENRYN ULV (8) CANTIGA GS (11,14) ICH9M (21) Pre FCT PORT (32) DISCHARGE (33) SC4624 (37)
P0.75V	DDR3 (16, 17) SC486 (36)
P5V_AUX	ICH9M (21) TPS51120 (35) SC486 (36) SC4624 (37) SWITCHED (41) USB PORT (7,11)
P3.3V_AUX	EMC2102 (10) ICH9M (21) 88E8055 (27) STMUX1000 (28) WLAN (29) LAN JACK LED (32) TPS51120 (35) SWITCHED (41) SLB9635 (43) R5538 (SUB_7)
P1.5V_AUX	CANTIGA GS (14) DDR3 (16, 17) ICH9M (21) SC486 (36) SWITCHED (41)
VCC_CORE	PENRYN ULV (8,9) SC454 (39)
VCC_CORE	CANTIGA GS (12)

Voltage Rails

Power Rail	Descriptions	Power Rail	Descriptions
AD_DC	Primary DC system power supply (9 to 19V)	***P1.05V_PEG***	P1.05V (Direct Media Interface Compensation)
VDC		***P5.0V***	5.0V Power Rail (off in S3-S5)
CHG_REF	Charger Reference Voltage Source	***P3.3V***	3.3V Power Rail (off in S3-S5)
PRTC_BAT	3.3V supply for the RTC well.	***P1.8V***	1.8V Power Rail (off in S3-S5)
P5.0V_FILT	???	***P1.5V***	1.5V Power Rail (off in S3-S5)
P12.0V_ALW	???	***P1.05***	1.05V Power Rail (off in S3-S5)
P5.0V_ALW	???	***P0.75V***	DDR3 Termination
		P5.0V_AUX	5.0V Power Rail (off in S4-S5)
		P3.3V_AUX	3.3V Power Rail (off in S4-S5)
MICOM_P3V	Output voltage of ISL6256(Charger) (if VDC is removed, it will be off)	***P1.5_AUX***	1.5V Power Rail (off in S4-S5)
		VCC_CORE	Core Voltage for PENRYN ULV
		IGFX_CORE	Core Voltage for CANTIGA GS
LCD_VDD3V	3.3V (LED LCD)	***AUD_P5V***	5.0V switched power rail (off in S3-S5)
LED VOUT	7V-19V (LED LCD)	***AMP_VDD***	5.0V (Audio AMP)
VDC_LED	VDC (LED LCD)	***AVDD***	5.0V (ADI1986)
P5.0V_CRT	5.0V (CRT Conn.)		
VCC_CRT	5.0V (CRT)	***P1.5V_EXT***	1.5V (R5538, EXPRESS CARD)
		P3.3V_AUX_EXT	3.3V (R5538, EXPRESS CARD)
P1.2V_LAN	Internal Regulator's Power of LAN Controller	***P3.3V_EXT***	
P1.8V_P2.5V_LAN			
P3.3V_MCD	3.3V (7-in-1 Socket)	***3.3V_VDD***	3.3V (AES1610, FINGER PRINT)
		FP_P3.3V	3.3V (AES1610, FINGER PRINT)

GMCH Core Voltage

	EN	V4	V3	V2	V1	V0	Voltage
Render Performance States	1	0	0	0	0	0	1.250
	1	0	0	0	0	1	1.225
	1	0	0	0	1	0	1.200
	1	0	0	0	1	1	1.175
	1	0	0	1	0	0	1.150
	1	0	0	1	0	1	1.125
	1	0	0	1	1	0	1.100
	1	0	0	1	1	1	1.075
	1	0	1	0	0	0	1.050
	1	0	1	0	0	1	1.025
	1	0	1	0	1	0	1.000
	1	0	1	0	1	1	0.975
	1	0	1	1	0	0	0.950
	1	0	1	1	0	1	0.925
	1	0	1	1	1	0	0.900
	1	0	1	1	1	1	0.875
	1	1	0	0	0	0	0.850
	1	1	0	0	0	1	0.825
Render Suspend States	1	1	0	0	1	0	0.800
	1	1	0	0	1	1	0.775
	1	1	0	1	0	0	0.750
	1	1	0	1	0	1	0.725
	1	1	0	1	1	0	0.700
	1	1	0	1	1	1	0.675
	1	1	1	0	0	0	0.650
	1	1	1	0	0	1	0.625
	1	1	1	0	1	0	0.600
	1	1	1	0	1	1	0.575
	1	1	1	1	0	0	0.550
	1	1	1	1	0	1	0.525
	1	1	1	1	1	0	0.500
	1	1	1	1	1	1	0.400
	0	X	X	X	X	X	0.000

CPU Core Voltage Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125

Active Mode

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125

Active / Deeper Sleep Dual Mode

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000

Deeprer Sleep / Deep Power Down Mode

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000

Programmable Deep Power Down

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000

DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN BOARD INFORMATION	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
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FSC BSEL2	FSB BSEL1	FSA BSEL0	HOST CLK
0	0	0	266 MHz
0	0	1	RSVD
0	1	0	200 MHz
0	1	1	166 MHz
1	0	0	RSVD
1	0	1	RSVD
1	1	0	RSVD
1	1	1	RSVD

CK505

P3.3V P1.5V P3.3V

nostuff R684 0

B10 BLM18PG181SN1

B9 BLM18PG181SN1

C668 C107 C671 C672 C663 C158 C664 C159 C674 C673 C639 C667 C665 C106 C108 C637 C72 C73

CLOCK500 IDTCV179BNLG

VDD_IO VDD_SRC_IO1 VDD_SRC_IO2 VDD_SRC_IO3 VDD_CPU_IO VDD_PLL3_IO NC USB_FS_A FSB_TESTMODE REF_FS_C_TEST_SEL CPUSTOP# PCISTOP# CLKPWRGD_PWRDN# PCIF_5_ITP_EN PCI_4_SEL_LCDCLK# PCI_3 PCI_2 PCI_1_CLKREQ_B# PCI_0_CLKREQ_A# SCL SDA XTAL_IN XTAL_OUT VSS_48 VSS_CPU VSS_IO VSS_PCI VSS_PLL3 VSS_REF VSS_SRC1 VSS_SRC2 VSS_SRC3

VDD_REF VDD_48 VDD_PCI VDD_PLL3 VDD_SRC VDD_CPU

CPU0 CPU0# CPU1_MCH CPU1_MCH# SRC11_CLKREQH# SRC11#_CLKREQG# SRC10 SRC10# SRC9 SRC9# SRC8_ITP SRC8#_ITP# SRC7_CLKREQF# SRC7#_CLKREQE# SRC6 SRC6# SRC4 SRC4# SRC3_CLKREQC# SRC3#_CLKREQD# SRC2 SRC2# LCDCLK_27M LCDCLK#_27M_SS SRC0_DOT96 SRC0#_DOT96#

CLK0_HCLK0 CLK0_HCLK0# CLK0_HCLK1 CLK0_HCLK1# MINIPCIE3_CLKREQ2# LOM3_CLKREQ# CLK1_MINIPCIE2 CLK1_MINIPCIE2# CLK1_PCIELOM CLK1_PCIELOM# CLK1_EXPCARD CLK1_EXPCARD# EXP3_CLKREQ# MINIPCIE3_CLKREQ1# CLK1_MINIPCIE1 CLK1_MINIPCIE1# CLK1_MCH3GPLL CLK1_MCH3GPLL# CLK1_PCIEICH CLK1_PCIEICH# CLK1_SATA CLK1_SATA# CLK1_DREFSSCLK CLK1_DREFSSCLK# CLK1_DREFCLK CLK1_DREFCLK#

1205-003159

Silego : 1205-003156

nostuff

CLK3_FM48 CLK3_USB48 R77 33 R78 33

CPU1_BSEL0 CPU1_BSEL1 CPU1_BSEL2 R649 2.2K R647 10K 1% 1/20W

CLK3_ICH14 CLK3_SIO14 CHP3_CPUSTP# CHP3_PCISTP# R52 22.6 1% R53 22.6 1%

CHP3_CLK_PWRGD R646 0

CLK3_PCLKICH R654 22.6 1%

CLK3_PCLKSIO CLK3_PCLKSIO_DS CLK3_TPMLPC R652 22.6 1% R55 22.6 1% R650 22.6 1%

CLK3_PCLKMICOM CLK3_DBGLPC MCH3_CLKREQ# R648 22.6 1% R656 22.6 1% R651 475 1%

CHP3_SATACLKREQ# R54 475 1%

SMB3_CLK SMB3_DATA

Y1 14.31818MHz 2801-004518

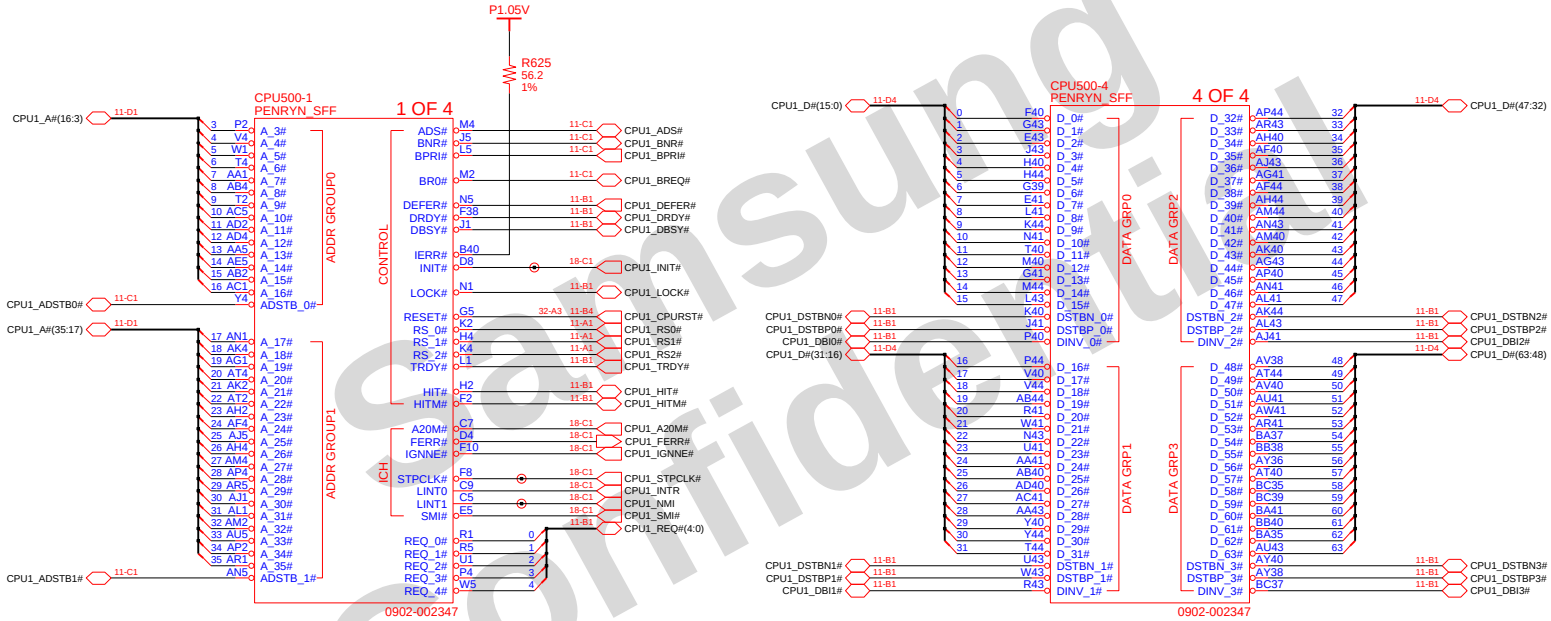
C105 0.018nF 50V C104 0.018nF 50V

R653 10K 1% 1/20W R655 10K 1% 1/20W

Place 14.318MHz within 500mils of CK-505

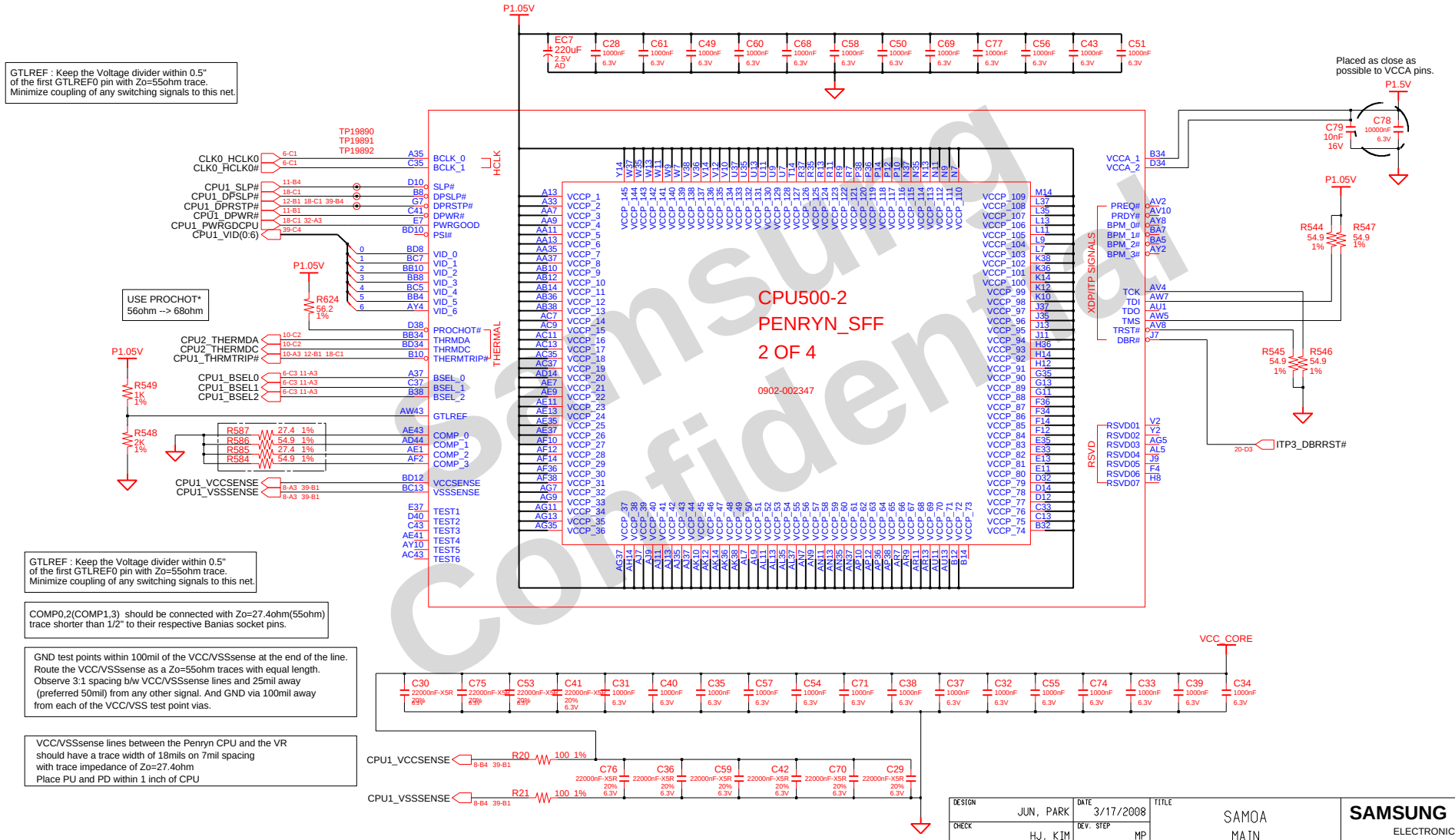
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE:	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 6 OF 44	

ULV CPU(Penryn SFF)



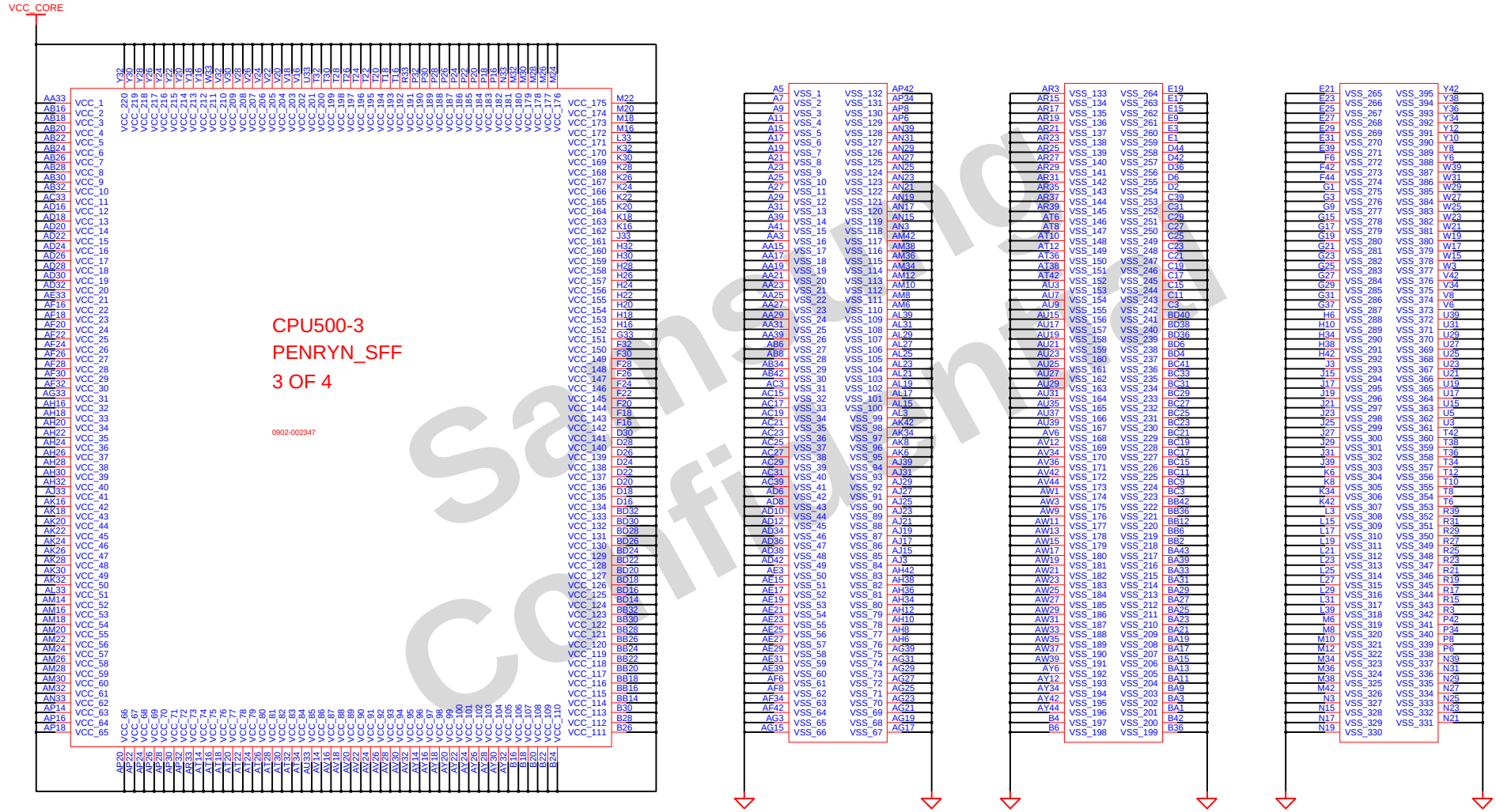
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN PENRYN ULV CPU(1/3)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE:	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 7 OF 44	

ULV CPU(Penryn SFF)



DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN PENRYN ULV CPU(2/3)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 8 OF 44	

ULV CPU(Penryn SFF)

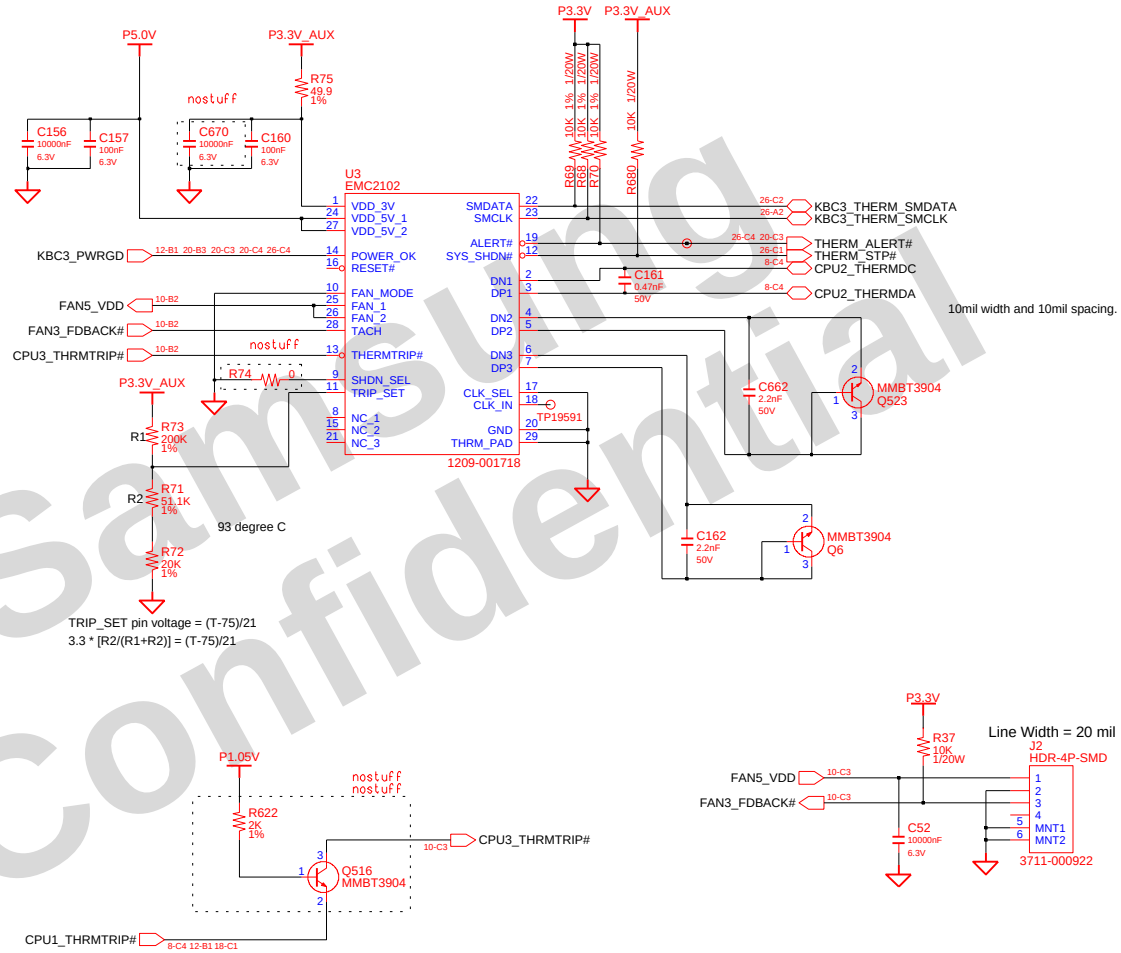


DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN PENRYN ULV CPU(3/3)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 9 OF 44	

THERMAL MONITOR

FAN MODE	
0	0% Drive
Open	60% drive after spin up routine
1	75% drive after spin up routine

SHDN_SEL	
0	Intel Mode
High-Z	Diode Mode
1	Disabled



DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN THERMAL MONITOR	SAMSUNG ELECTRONICS		
CHECK: HJ, KIM	DEV. STEP: MP				
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA		
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 10 OF 44			

GMCH(CANTIGA GS)

GMCH500-1
CANTIGA-GS
1 OF 5
0904-002394

P1.05V
C130 22000nF-X5R 20% 6.3V
C139 220nF 10V
C137 220nF 10V
C140 100nF 6.3V
C63 470nF 16V
C594 2200nF 10V
C592 4700nF 10V
C593 4700nF 10V
EC500 220uF 2.5V AD

CPU1_D#(63:0) 7-B1 7-B2 7-C1 7-C2
HOST DATA BUS
H_D#_0 H_D#_1 H_D#_2 H_D#_3 H_D#_4 H_D#_5 H_D#_6 H_D#_7 H_D#_8 H_D#_9 H_D#_10 H_D#_11 H_D#_12 H_D#_13 H_D#_14 H_D#_15 H_D#_16 H_D#_17 H_D#_18 H_D#_19 H_D#_20 H_D#_21 H_D#_22 H_D#_23 H_D#_24 H_D#_25 H_D#_26 H_D#_27 H_D#_28 H_D#_29 H_D#_30 H_D#_31 H_D#_32 H_D#_33 H_D#_34 H_D#_35 H_D#_36 H_D#_37 H_D#_38 H_D#_39 H_D#_40 H_D#_41 H_D#_42 H_D#_43 H_D#_44 H_D#_45 H_D#_46 H_D#_47 H_D#_48 H_D#_49 H_D#_50 H_D#_51 H_D#_52 H_D#_53 H_D#_54 H_D#_55 H_D#_56 H_D#_57 H_D#_58 H_D#_59 H_D#_60 H_D#_61 H_D#_62 H_D#_63

VCC CORE
VTT
HOST ADDRESS BUS
H_A#_3 H_A#_4 H_A#_5 H_A#_6 H_A#_7 H_A#_8 H_A#_9 H_A#_10 H_A#_11 H_A#_12 H_A#_13 H_A#_14 H_A#_15 H_A#_16 H_A#_17 H_A#_18 H_A#_19 H_A#_20 H_A#_21 H_A#_22 H_A#_23 H_A#_24 H_A#_25 H_A#_26 H_A#_27 H_A#_28 H_A#_29 H_A#_30 H_A#_31 H_A#_32 H_A#_33 H_A#_34 H_A#_35
7-C4 CPU1_A#(35:3)

HOST CONTROL
H_ADS# H_ADSTB#_0 H_ADSTB#_1 H_BNR# H_BPRI# H_BREQ#
CPU1_ADS# CPU1_ADSTB0# CPU1_ADSTB1# CPU1_BNR# CPU1_BPRI# CPU1_BREQ#
H_DEFER# H_DBSY# H_DPWR# H_DRDY#
CPU1_DEFER# CPU1_DBSY# CPU1_DPWR# CPU1_DRDY#
H_HIT# H_HITM# H_LOCK# H_TRDY#
CPU1_HIT# CPU1_HITM# CPU1_LOCK# CPU1_TRDY#
HPLL_CLK HPLL_CLK#
CLK0_HCLK1 CLK0_HCLK1#
H_DINV#_0 H_DINV#_1 H_DINV#_2 H_DINV#_3
CPU1_DBI0# CPU1_DBI1# CPU1_DBI2# CPU1_DBI3#
H_DSTBN#_0 H_DSTBN#_1 H_DSTBN#_2 H_DSTBN#_3
CPU1_DSTBN0# CPU1_DSTBN1# CPU1_DSTBN2# CPU1_DSTBN3#
H_DSTBP#_0 H_DSTBP#_1 H_DSTBP#_2 H_DSTBP#_3
CPU1_DSTBP0# CPU1_DSTBP1# CPU1_DSTBP2# CPU1_DSTBP3#
H_REQ#_0 H_REQ#_1 H_REQ#_2 H_REQ#_3 H_REQ#_4
CPU1_REQ#(4:0)
H_RS#_0 H_RS#_1 H_RS#_2
CPU1_RS0# CPU1_RS1# CPU1_RS2#

P1.05V
Placed as close to the CANTIGA GS pin as possible
R588 221 1%
R589 100 1%
C591 100nF 6.3V
11-A4 MCH1_HSWING

P1.05V
R33 1K 1%
R42 2K 1%
11-A4 MCH1_HVREF

CPU1_CPURST# 7-C3
CPU1_SLP# 8-C4 32-A3
H_CPURST# H_CPUSLP#

MCH1_HSWING 11-C4
R592 24.9 1%
H_SWING H_RCOMP

MCH1_HVREF 11-C4
H_DVREF H_AVREF

VTTLF_1 VTTLF_2 VTTLF_3 VTTLF
470nF 16V 470nF 16V 470nF 16V
C90 C92 C94

CFG
CFG_0 CFG_1 CFG_2 CFG_3 CFG_4 CFG_5 CFG_6 CFG_7 CFG_8 CFG_9 CFG_10 CFG_11 CFG_12 CFG_13 CFG_14 CFG_15 CFG_16 CFG_17 CFG_18 CFG_19 CFG_20
CPU1_BSEL0 6-C3 8-C4
CPU1_BSEL1 6-C3 8-B4
CPU1_BSEL2 6-C3 8-B4
MCH3_CFG16 15-C1
MCH3_CFG7 15-C1
MCH3_CFG6 15-C1

NC
VCC_NCTF_1 VCC_NCTF_2 VCC_NCTF_3 VCC_NCTF_4 VCC_NCTF_5 VCC_NCTF_6 VCC_NCTF_7 VCC_NCTF_8 VCC_NCTF_9 VCC_NCTF_10 VCC_NCTF_11 VCC_NCTF_12 VCC_NCTF_13 VCC_NCTF_14 VCC_NCTF_15 VCC_NCTF_16 VCC_NCTF_17 VCC_NCTF_18 VCC_NCTF_19 VCC_NCTF_20 VCC_NCTF_21 VCC_NCTF_22 VCC_NCTF_23 VCC_NCTF_24 VCC_NCTF_25 VCC_NCTF_26 VCC_NCTF_27 VCC_NCTF_28 VCC_NCTF_29 VCC_NCTF_30 VCC_NCTF_31 VCC_NCTF_32 VCC_NCTF_33 VCC_NCTF_34 VCC_NCTF_35 VCC_NCTF_36 VCC_NCTF_37 VCC_NCTF_38 VCC_NCTF_39

P1.05V

DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN CANTIGA GS(1/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE:	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 11 OF 44	

GMCH(CANTIGA GS)

GMCH500-2
CANTIGA-GS
2 OF 5
0904-002394

VR Enalbe Signal to support Graphics Render Stanby Mode
Cantiga GS chipset integrates the VID straps.
However, straps on enable-pin are still needed.
Option A : GFX_VR_EN signal to graphic VR enable pin.
Add a 100-kOhm pull-down on the board on this signal.
Option B : Leave GFX_VR_EN no connect and route SLP_S3# to GFX VR Enable pin

DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN CANTIGS GS(2/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 12 OF 44	

GMCH(CANTIGA GS)

GMCH500-3
CANTIGA-GS
3 OF 5
0904-002394

SM_DRAMRST#	Leave as NC in DDR2 mode. Used only in DDR3 mode.
SM_PWROK	Connect to GND in DDR2 mode.

SYSTEM MEMORY A

SYSTEM MEMORY B

MEM1_ADQ(63:0)

MEM1_ABS(2:0) 16-C4 — SA_BS_0, SA_BS_1, SA_BS_2

MEM1_ADM(7:0) 16-B4 — SA_DM_0 … SA_DM_7

MEM1_ADQS#(7:0) 16-A4 — SA_DQS#_0 … SA_DQS#_7

MEM1_ADQS(7:0) 16-B4 — SA_DQS_0 … SA_DQS_7

MEM1_AMA(14:0) 16-D4 — SA_MA_0 … SA_MA_14

MEM1_ACAS# 16-C4 — SA_CAS#
MEM1_ARAS# 16-C4 — SA_RAS#
MEM1_AWE# 16-B4 — SA_WE#

MEM1_CS0# 16-C4 — SA_CS#_0
MEM1_CS1# 16-C4 — SA_CS#_1

MEM1_ODT0 16-B4 — SA_ODT_0
MEM1_ODT1 16-B4 — SA_ODT_1

MEM1_CKE0 16-C4 — SA_CKE_0
MEM1_CKE1 16-C4 — SA_CKE_1

CLK1_MCLK0 16-C4 — SA_CK_0
CLK1_MCLK0# 16-C4 — SA_CK#_0
CLK1_MCLK1 16-C4 — SA_CK_1
CLK1_MCLK1# 16-C4 — SA_CK#_1

P1.5V_AUX
R628 80.6 1%

SM_RCOMP
SM_RCOMP#
R43 80.6 1%

SM_RCOMP_VOH
SM_RCOMP_VOL
P1.5V_AUX
R673 1K 1%
R671 3.01K 1%
R672 1K 1%
C642 10nF 16V
C644 2200nF 10V
C645 10nF 16V
C646 2200nF 10V

Cantiga
SM_RCOMP : 80 ohm to P1.5V_AUX
SM_RCOMP# : 80 ohm to VSS
P1.8V_AUX FOR DDR2

PLACE EACH CAP NEAR BC51 PIN
C184 100nF 6.3V
C183 100nF 6.3V
nostuff
R45 499 1%

SM_REXT BH20
SM_VREF BC51 — MEM1_VREF (36-B4 17-C2 17-B2 16-C2 16-B2)

SM_DRAMRST# BA37 (17-A3 16-A3) — MCH3_DDR_RST#
SM_PWROK AY37 (36-C2) — VRM3_DDR_PWRGD

SB_CAS# BH14 (17-C4) — MEM1_BCAS#
SB_RAS# BE21 (17-C4) — MEM1_BRAS#
SB_WE# BK14 (17-B4) — MEM1_BWE#

SB_CS#_0 BE23 (17-C4) — MEM1_CS2#
SB_CS#_1 BC19 (17-C4) — MEM1_CS3#

SB_ODT_0 BC17 (17-B4) — MEM1_ODT2
SB_ODT_1 BE17 (17-B4) — MEM1_ODT3

SB_CKE_0 BE37 (17-C4) — MEM1_CKE2
SB_CKE_1 BC37 (17-C4) — MEM1_CKE3

SB_CK_0 BA33 (17-C4) — CLK1_MCLK2
SB_CK#_0 BC33 (17-C4) — CLK1_MCLK2#
SB_CK_1 BA23 (17-C4) — CLK1_MCLK3
SB_CK#_1 BB24 (17-C4) — CLK1_MCLK3#

SB_DM_0 AP52 0
SB_DM_1 AY54 1
SB_DM_2 BJ49 2
SB_DM_3 BJ43 3
SB_DM_4 BH12 4
SB_DM_5 BD2 5
SB_DM_6 AY2 6
SB_DM_7 AJ3 7
(17-B4) — MEM1_BDM(7:0)

SB_DQS#_0 AT54 0
SB_DQS#_1 BB54 1
SB_DQS#_2 BJ51 2
SB_DQS#_3 BH42 3
SB_DQS#_4 BK8 4
SB_DQS#_5 BC3 5
SB_DQS#_6 AW3 6
SB_DQS#_7 AN3 7
(17-A4) — MEM1_BDQS#(7:0)

SB_DQS_0 AR53 0
SB_DQS_1 BA53 1
SB_DQS_2 BH50 2
SB_DQS_3 BK42 3
SB_DQS_4 BH8 4
SB_DQS_5 BB2 5
SB_DQS_6 AV2 6
SB_DQS_7 AM2 7
(17-B4) — MEM1_BDQS(7:0)

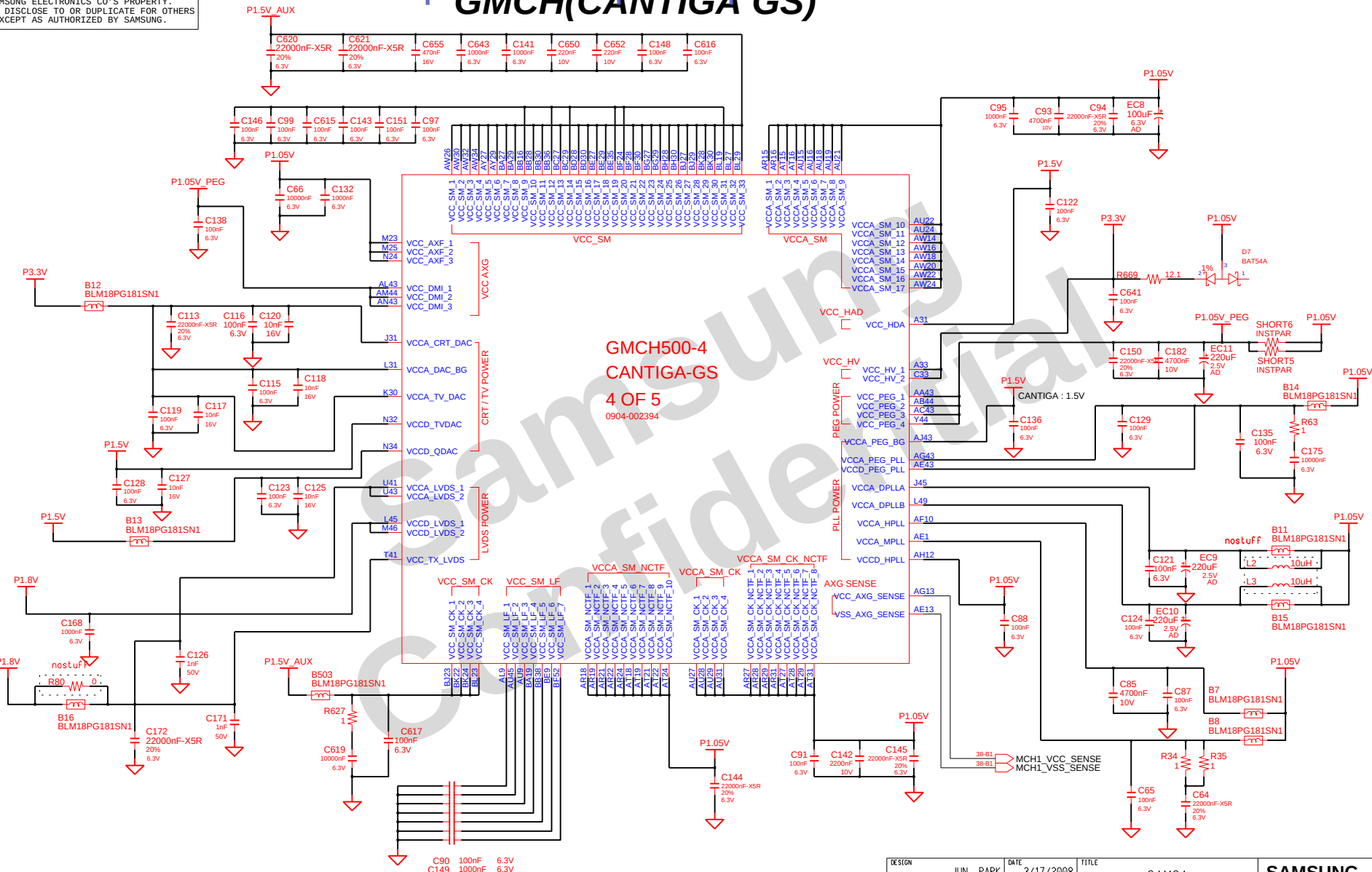
SB_MA_0 BJ15 0
SB_MA_1 BJ33 1
SB_MA_2 BH24 2
SB_MA_3 BA17 3
SB_MA_4 BF36 4
SB_MA_5 BH36 5
SB_MA_6 BF34 6
SB_MA_7 BK34 7
SB_MA_8 BJ37 8
SB_MA_9 BH40 9
SB_MA_10 BH16 10
SB_MA_11 BK36 11
SB_MA_12 BH38 12
SB_MA_13 BJ11 13
SB_MA_14 BL37 14
(17-D4) — MEM1_BMA(14:0)

SB_BS_0 BJ13 0
SB_BS_1 BK12 1
SB_BS_2 BK38 2
(17-C4) — MEM1_BBS(2:0)

SB_DQ_0 … SB_DQ_63 — MEM1_BDQ(63:0) (17-D3)

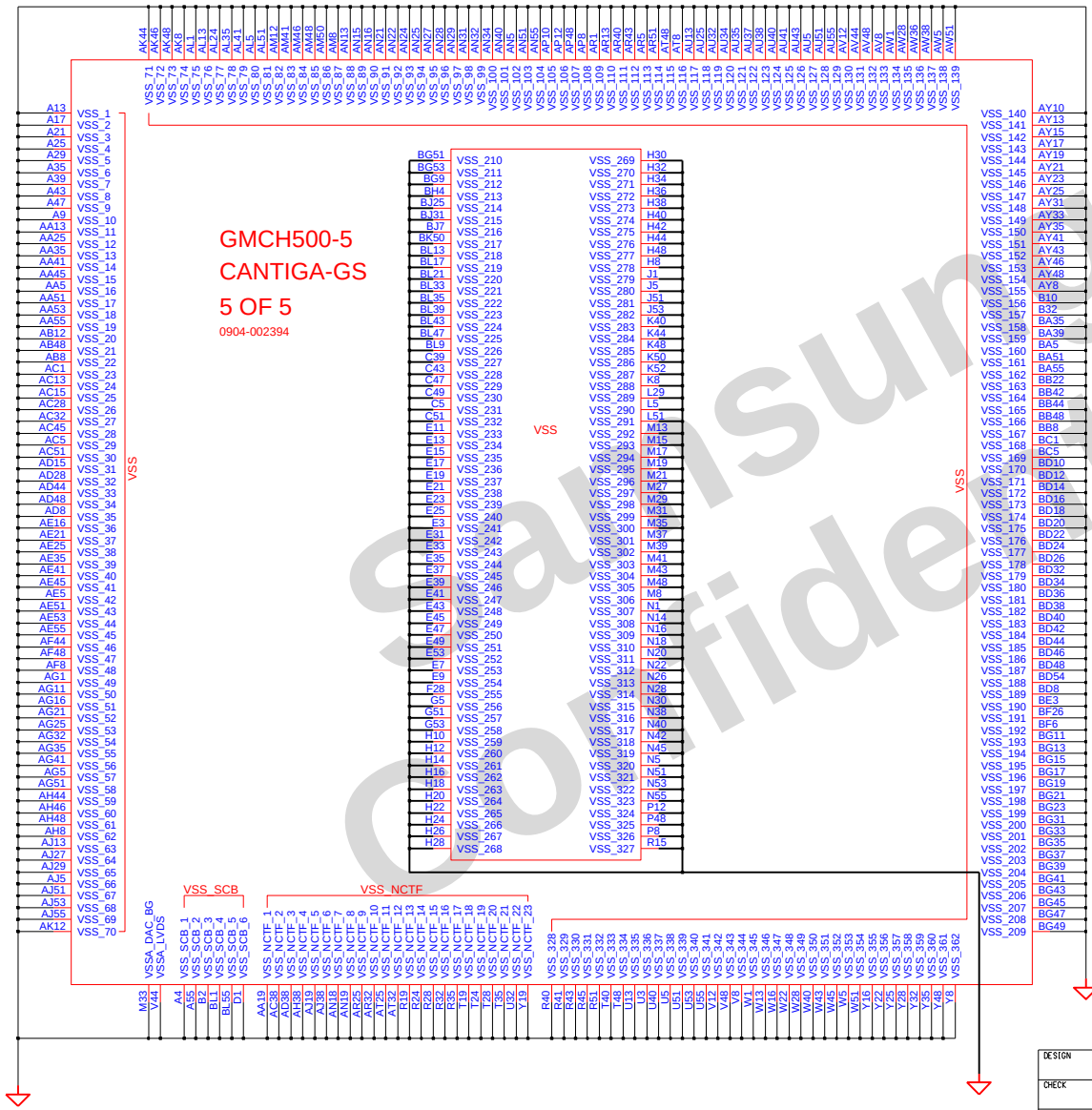
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN CANTIGS GS(3/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-OXXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 13 OF 44	

GMCH(CANTIGA GS)

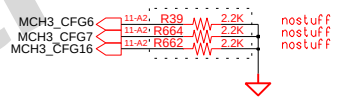


DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN CANTIGA GS(4/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-OXXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 14 OF 44	

GMCH(CANTIGA GS)



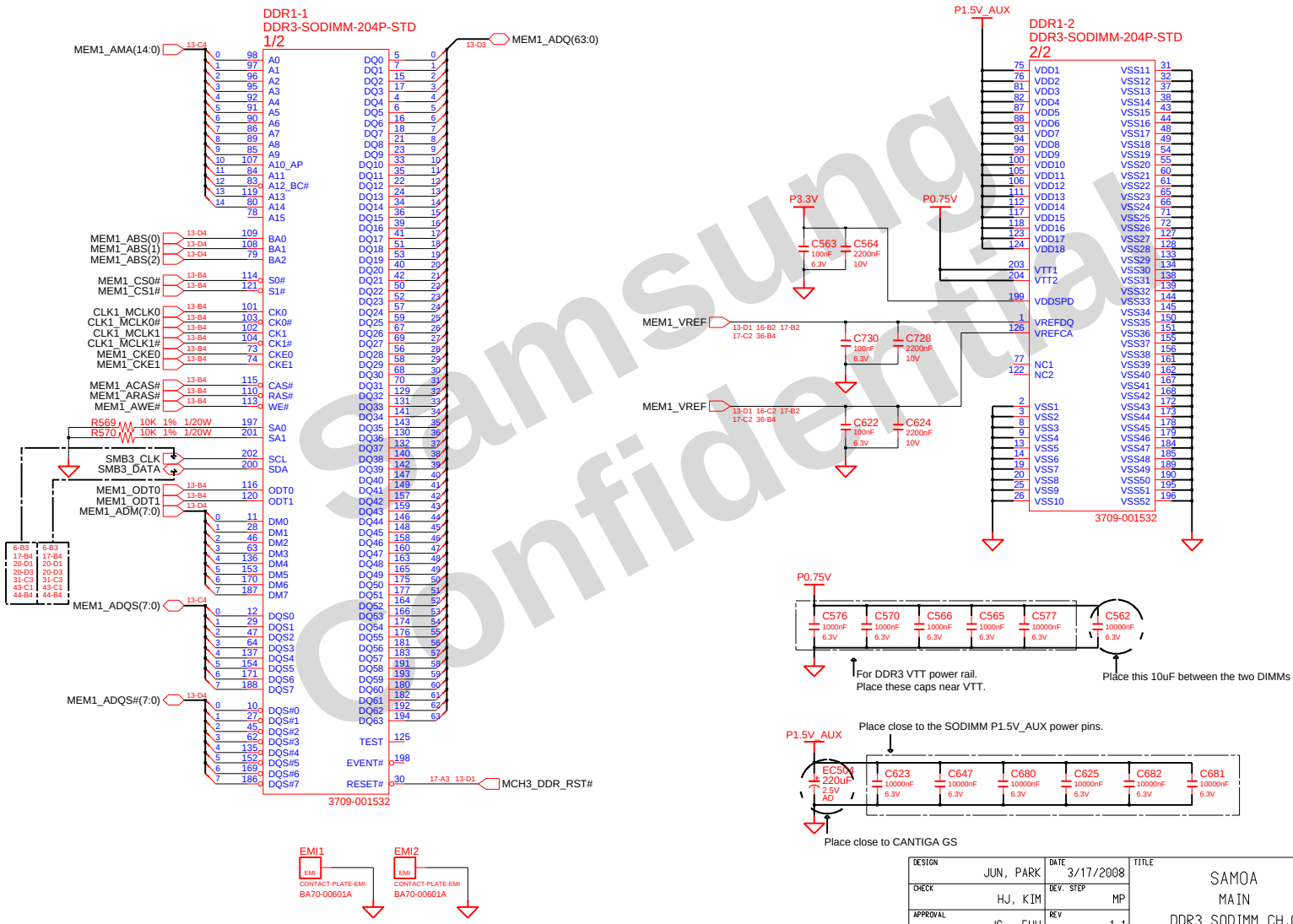
	Current Setting (def. : default Option)	
CFG#	Low	High
CFG(6)	iTPM Host Interface Enable	**iTPM Host Interface Disable (def.)**



DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN CANTIGS GS(5/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 15 OF 44	

DDR3 SO-DIMM #0

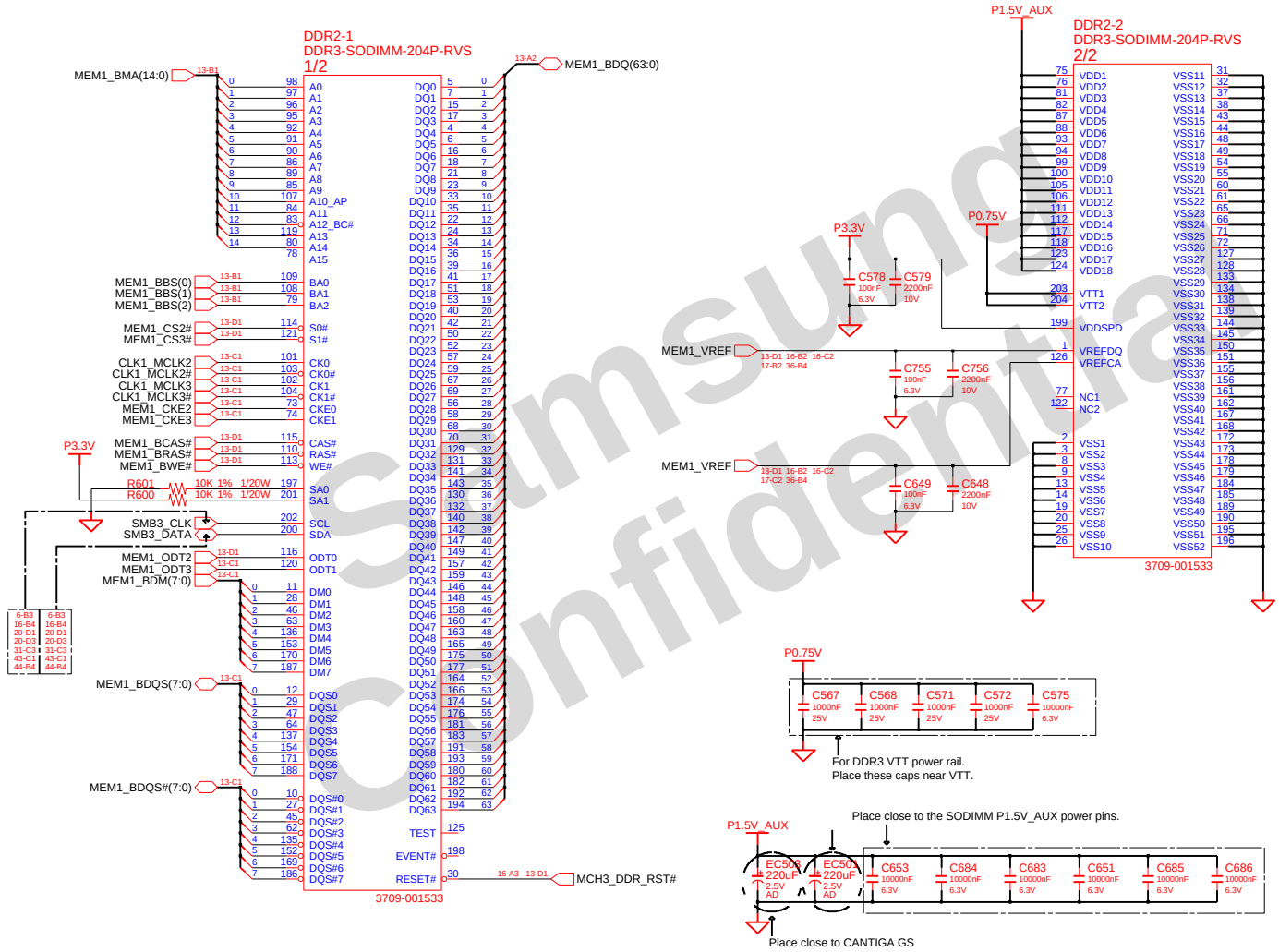
Height : 4.0mm (Standard)



DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN DDR3 SODIMM CH.0	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE:	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 16 OF 44	

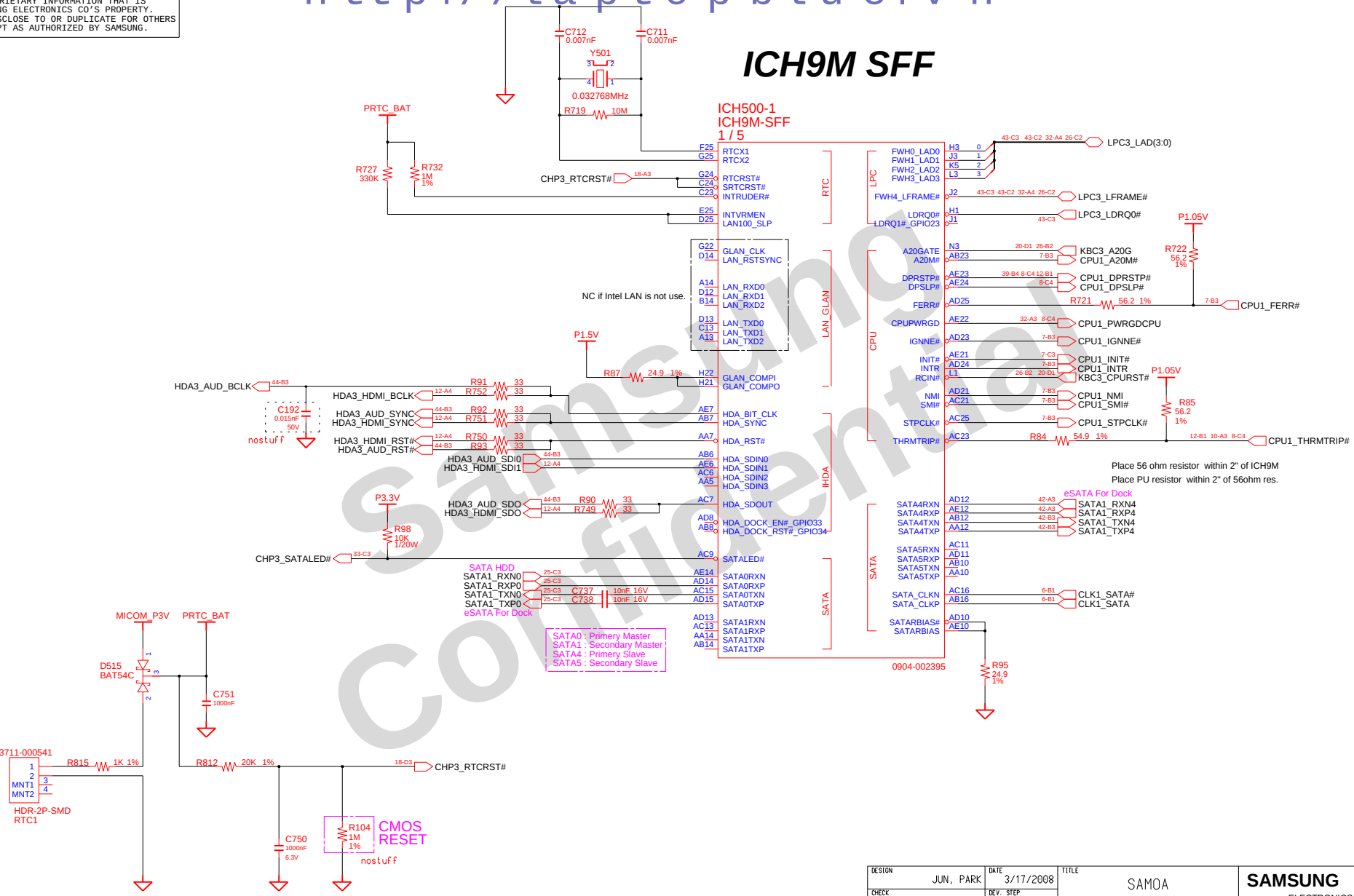
DDR3 SO-DIMM #1

Height : 4.0mm (Reverse)



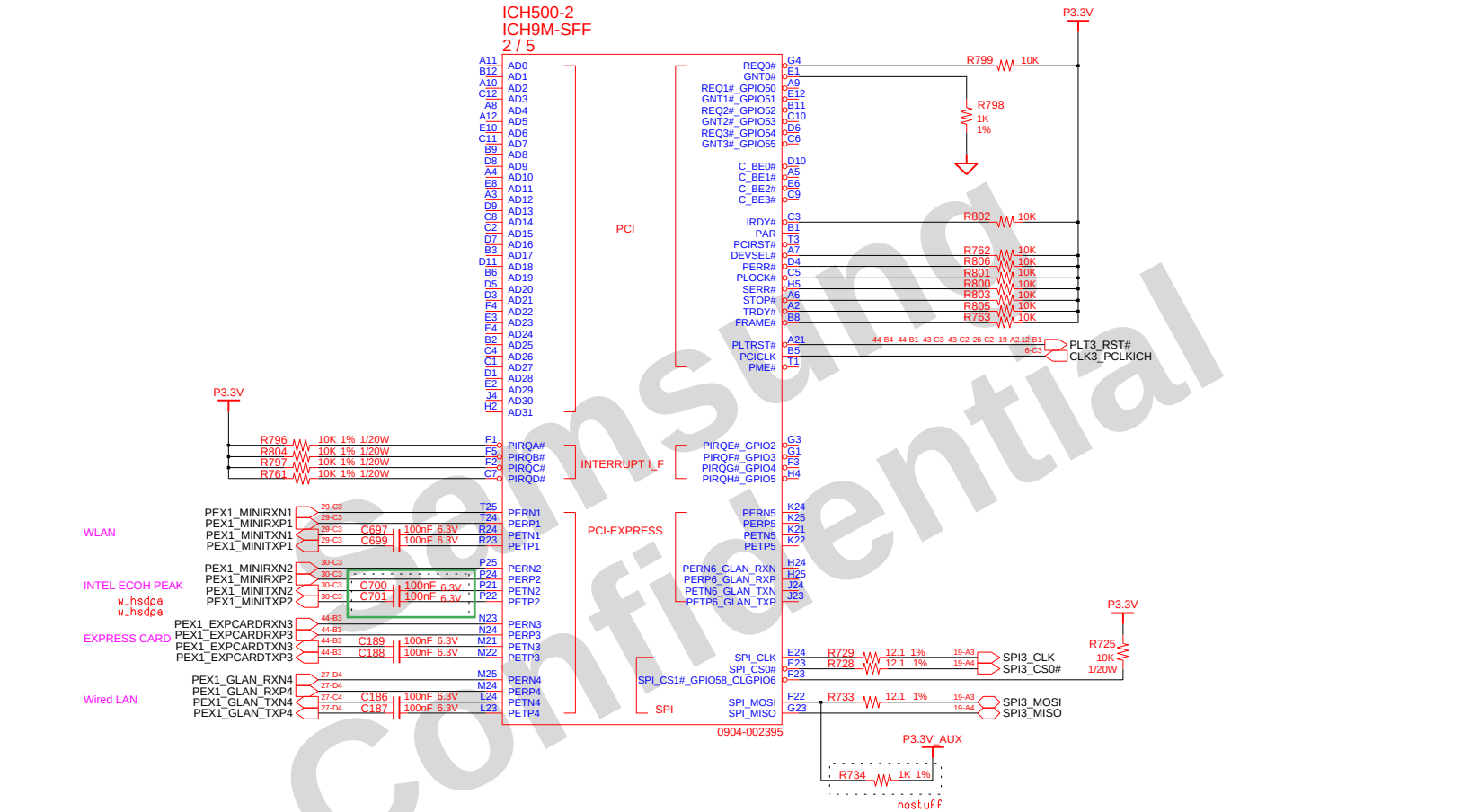
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN DDR3 SODIMM CH.1	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 17 OF 44	

ICH9M SFF

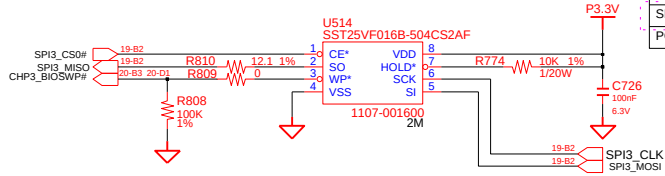


DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN ICH9M SFF(1/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 18 OF 44	

ICH9M SFF



SPI ROM



Boot BIOS Select

BIOS	PCI3_GNT0#	SPI_CS1#
LPC	HIGH	HIGH
SPI	LOW	HIGH
PCI	HIGH	LOW

PLT3_RST# R770 0 PLT3_RSTF#

DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN ICH9M SFF(2/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 19 OF 44	

ICH9M SFF

ICH500-3
ICH9M SFF
3 / 5

SYS_RESET# is P3.3V tolerant and should be pulled up to P3.3V_AUX by the front panel header

Place clsely to ICH

When using Cantiga SFF, GPIO49 should be left as NC.

BIOS CRISIS RECOVER STRAP
PLACE NEAR KEYBOARD
(Put it a debugger connector)

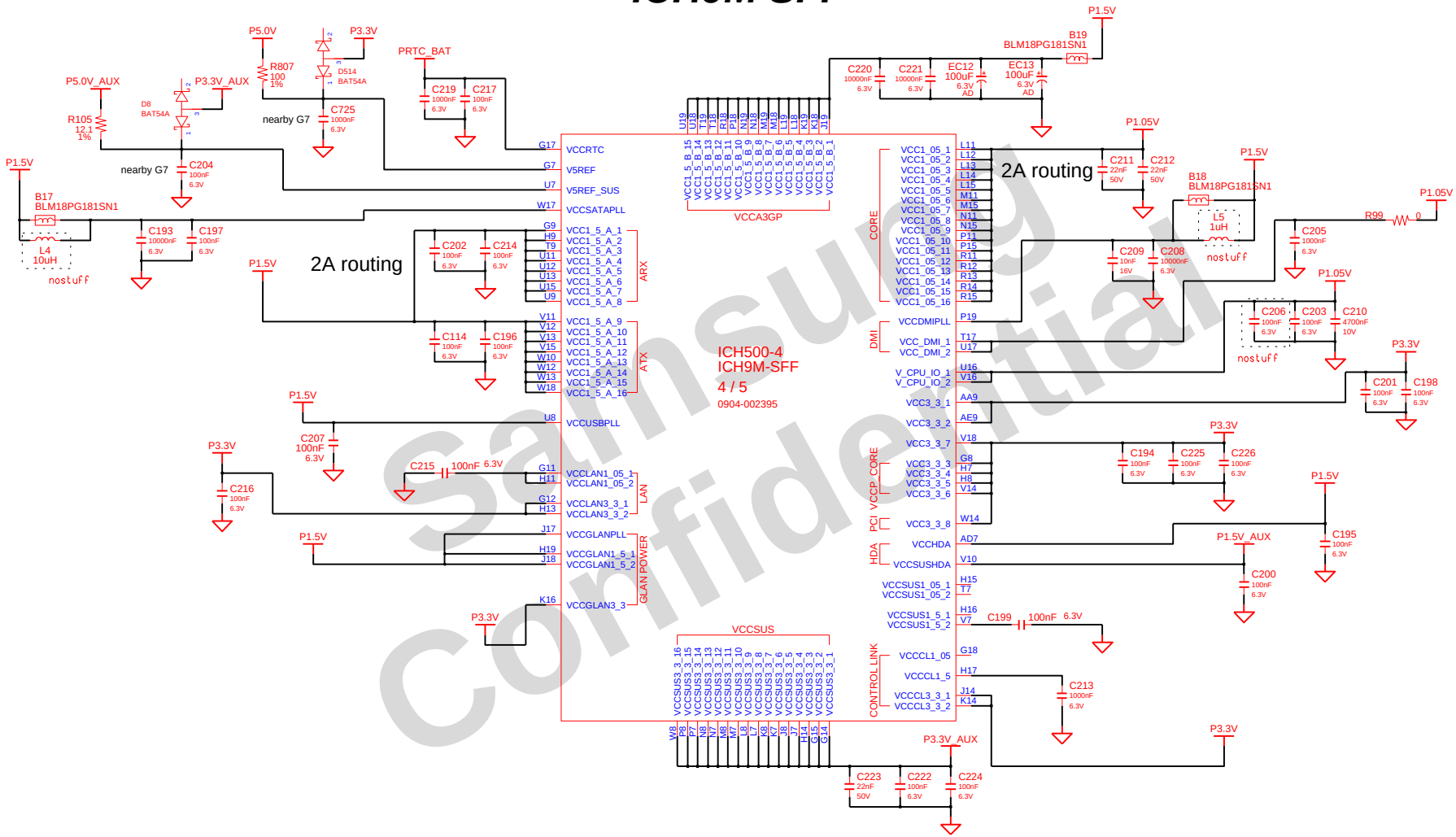
Place this registor within 500-mils of the ICH9M
Avoid routing next to clock/high speed signals.

R743 nostuff
R713 nostuff
R716 nostuff
R744 stuff for eSATA Hot Plug Detection Enable

0904-002395

DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN ICH9M SFF(3/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 20 OF 44	

ICH9M SFF

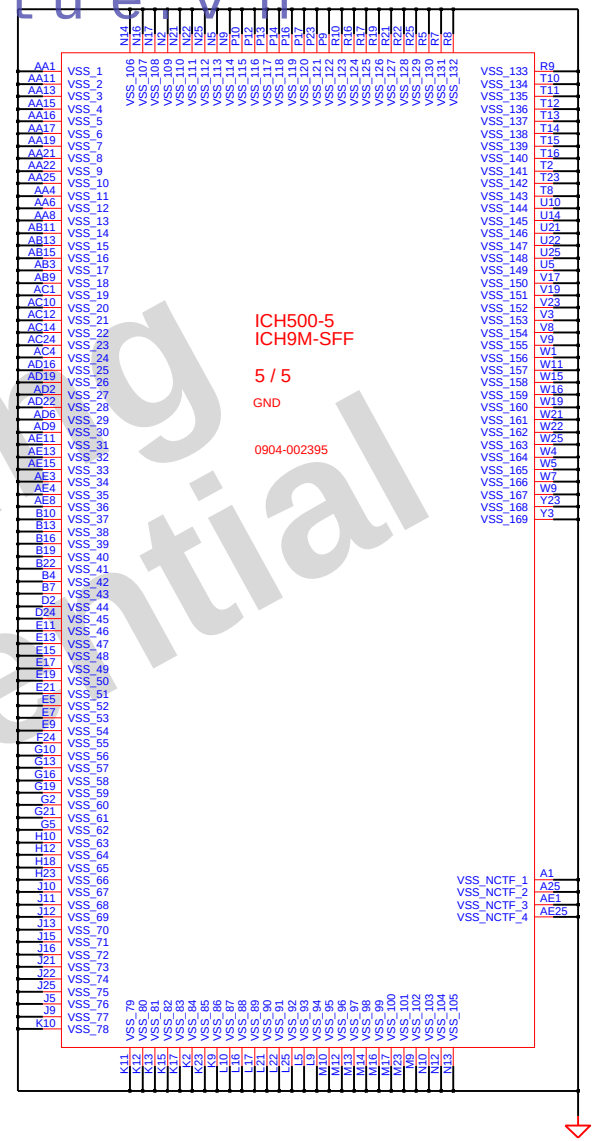


DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN ICH9M SFF(4/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 21 OF 44	

ICH9M SFF

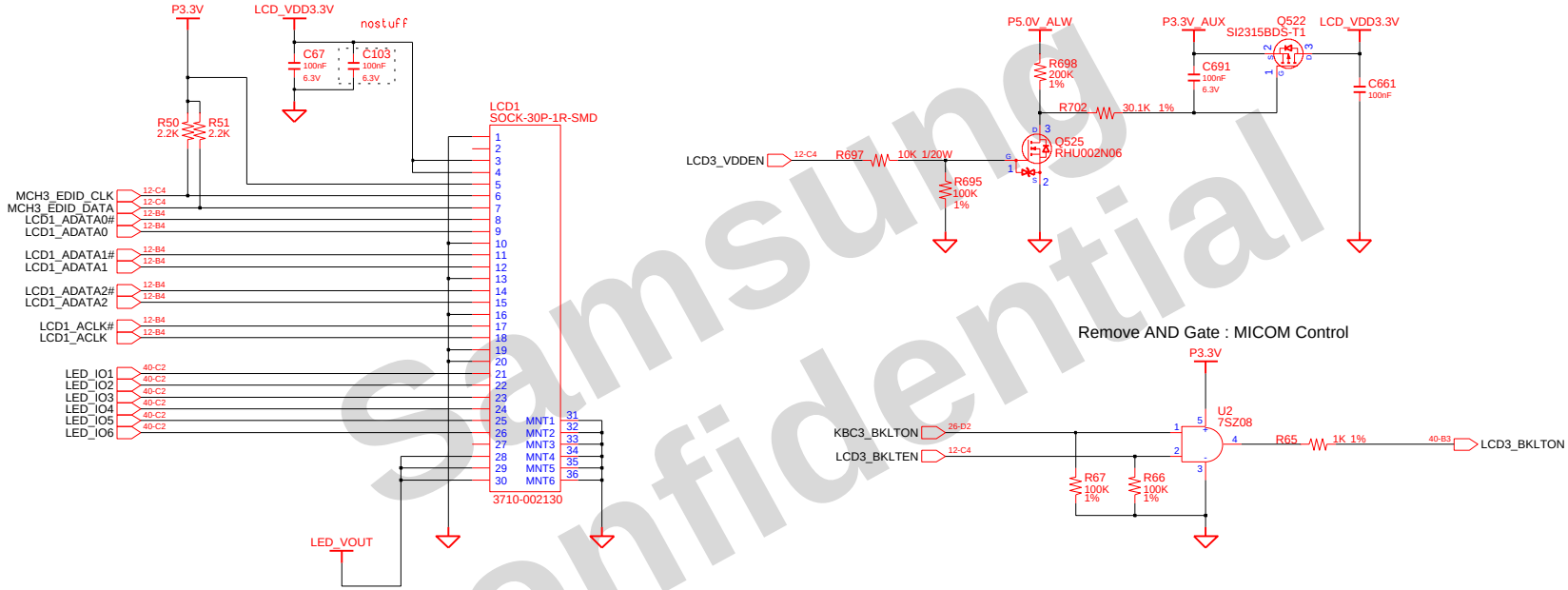
BIOS CODE

02	VERIFY REAL MODE
03	DISABLE NMI
04	GET CPU TYPE
06	INIT. SYSTEM H/W
08	INIT. CHIPSET REG.
09	SET IN POST FLAG
0A	INIT CPU.REG
0B	CPU CACHE ON
0C	INIT.CACHE TO POST
OE	INIT. I/O VALUE
0F	ENABLE THE L-BUS IDE
10	INIT. POWER MANAGER
11	LOAD ALTERNATE REG.
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE
14	INIT. KEYBOARD CONTROLLER
16	CHECK CHECKSUM
18	8254 TIMER INIT.
1A	8237 DMA CONTROLLER INIT.
1C	RESET INTERRUP CONTROLLER
20	TEST DRAM REFRESH
22	TEST 8742 KEYBOARD CONTROLLER
24	SET ES SEGMENT REG. TO 4GB
26	ENABLE A20
28	AUTO SIZING DRAM
32	COMPUTE THE CPU SPEED
34	TESET CMOS RAM
38	SHADOW SYSTEM BIOS ROM
3A	AUTO SIZING CACHE
3C	CONFIGURE ADVANCED CHIPSET REG.
3D	LOAD ALTER REG. WITH CMOS VALUE
42	INIT. INTERRUPT VECTOR
44	INIT. BIOS INTERRUPT
46	CHECK ROM COPYRIGHT NOTICE
47	INIT. I20 SUPPORT IF INSTALLED
48	CHECK VIDEO CONFIGURE AGAINST CMOS
49	INIT. PCI BUS AND DEVICE
4A	INIT. ALL VIDEO BIOS ROM
4C	SHADOW VIDEO BIOS ROM
50	DISPLAY CPU TYPE AND SPEED
52	TEST KEYBOARD
54	SET KEYCLICK IF ENABLED
56	ENABLE KEYBOARD
58	TEST FOR UNEXPECTED INTERRUPTS
5A	DISPLAY " PRESS ..... SETUP"
5C	TEST RAM GETWEEN 512K AND 640K
60	TEST EXTENDED MEMORY
62	TEST EXTENDED MEMORY ADDRESS LINE
64	JUMP TO USER PATCH 1
66	CONFIGURE ADVANCE CACHE REG.
6A	DISPLAY EXTERNAL CACHE SIZE
6C	DISPLAY SHADOW MESSAGE
6E	DISPLAY NON-DISPOSABLE SEGMENT
70	DISPLAY ERROR MESSAGE
72	CHECK FOR CONFIGURATION ERROR
74	TEST REAL-TIME CLOCK
76	CHECK FOR KEYBOARD EERROR
7C	SETUP HARDWARE INTERRUPT VECTOR
7E	TEST COPROCESSER IF PRESENT
80	DISABLE ON-BOARD I/O PORT
82	DETECT AND INSTALL EXT.RS232C
84	DETECT AND INSTALL EXT.PARALLEL
86	RE-INIT. ON-BOARD I/O PORT
88	INIT. BIOS DATA ROM
8A	INIT.EXTENDED BIOS DATA AREA
8C	INIT. FDD CONTROLLER
9A	SHADOW OPTION ROMS
9C	SETUP POWER MANAGEMENT
9E	ENABLE H/W INTERRUPT
A0	SET TIME OF DAY
A4	INIT. TYPEMATIC RATE
A8	ERASE F2 PROMPT
AA	SCAN FOR F2 KEY STROKE
AC	ENTER SETUP
AE	CLEAR IN POST FLAG
B0	CHECK FOR ERRORS
B2	POST DONE-PREPARE TO BOOT O/S
B4	ONE BEEP
B6	CHECK PASSWORD (OPTION)
B7	ACPI INIT
BA	DMI INIT
BE	CLEAR SCREEN
C0	TRY BOOT WITH INT19
D0	INTERRUPT HANDLER ERROR
D2	UNKNOWN INTERRUPT ERROR
D4	PENDING INTERRUPT ERROR
D6	SHUTDOWN 5
D8	SHUTDOWN ERROR
DA	EXTENDED BLOCK MOVE
DC	SHUTDOWN 10
89	ENABLE NMI
90	INIT. HDD CONTROLLER
91	INIT. LOCAL BUS HDD CONTROLLER
92	JUMP TO USER PATCH 2
94	DISABLE A20 ADDRESS LINE
96	CLEAR HUGE ES SEGMENT REG.
98	SEARCH FOR OPTION ROMS



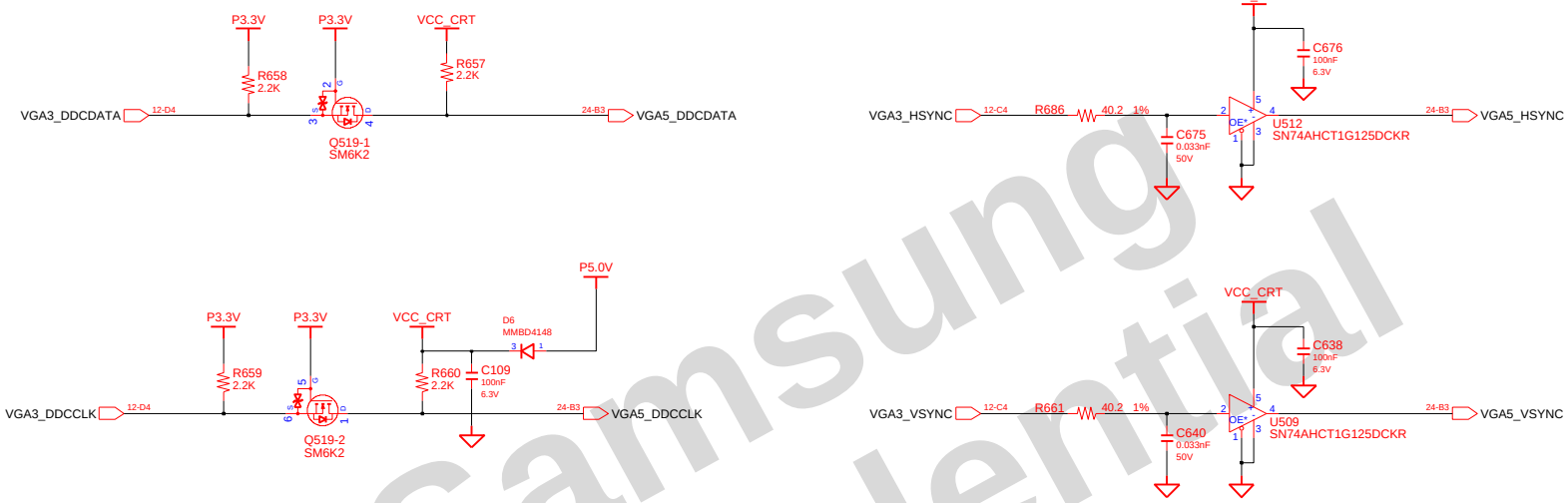
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN ICH9M SFF(5/5)	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 22 OF 44	

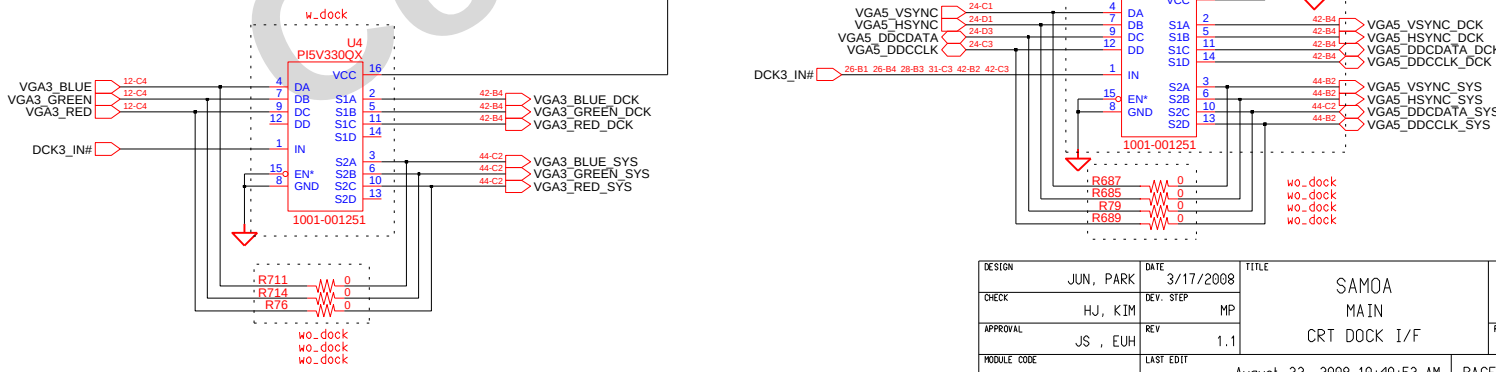
LED LCD CONNECTOR



DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN LED LCD I/F	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE:	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 23 OF 44	

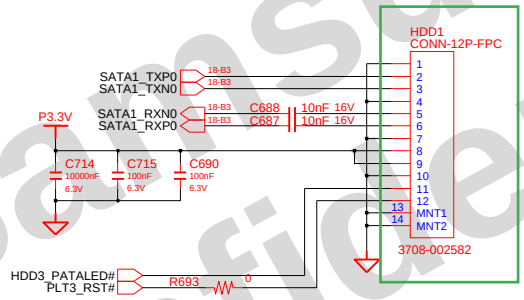
CRT DOCK I/F





DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN CRT DOCK I/F	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 24 OF 44	

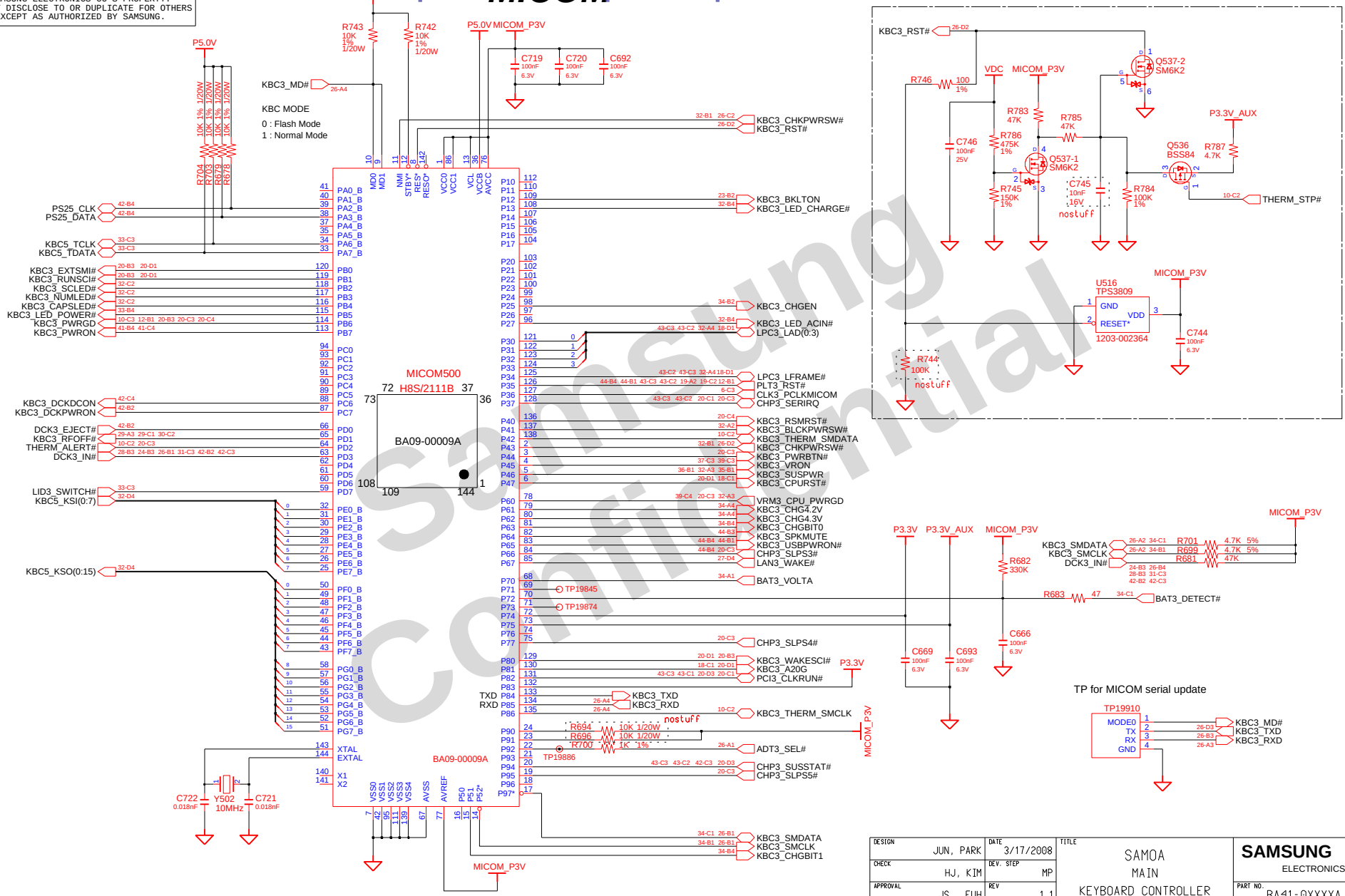
1.8" SATA HDD I/F



DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN 1.8inch SATA HDD I/F	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE:	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 25 OF 44	

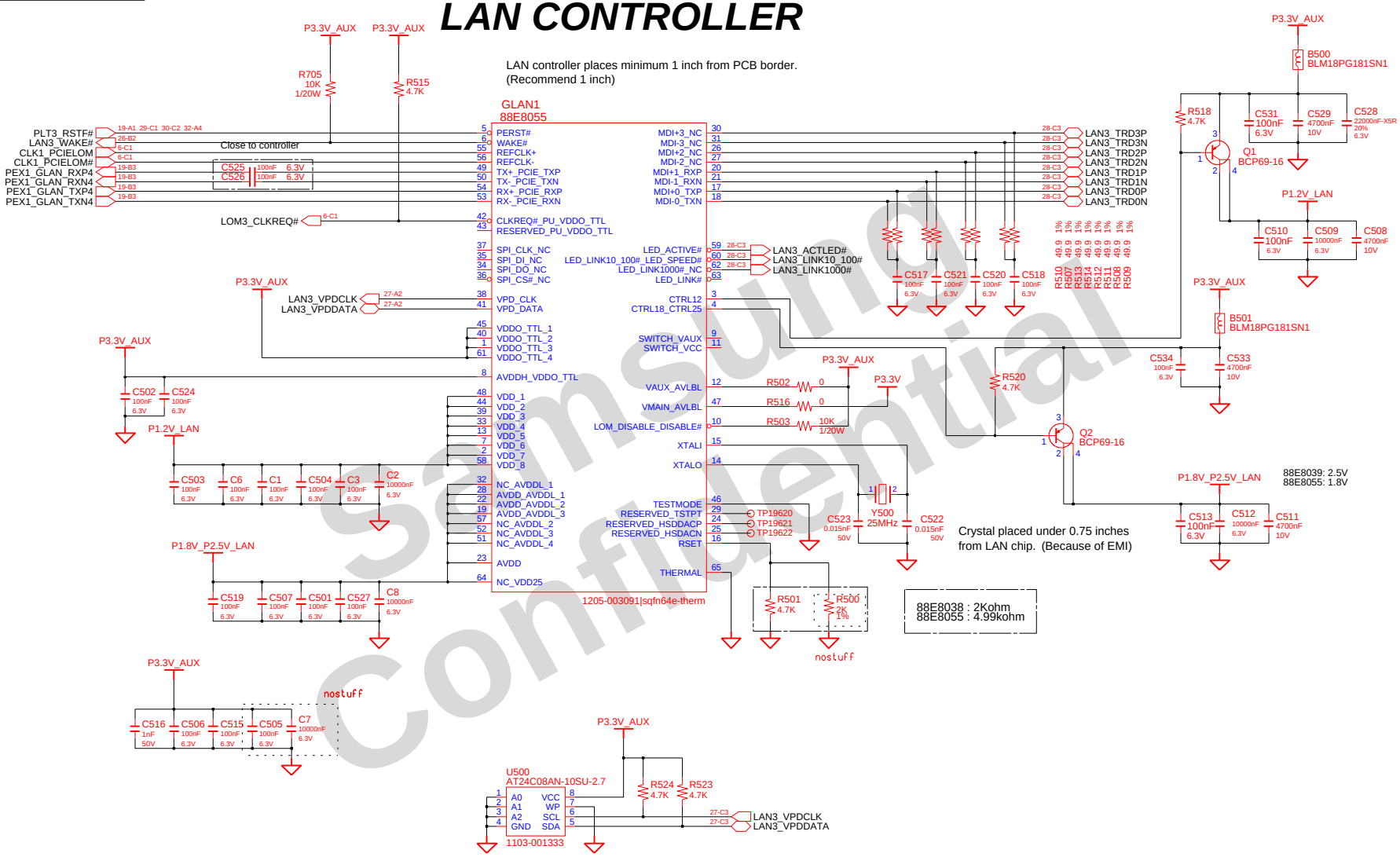
MICOM

MICOM RESET



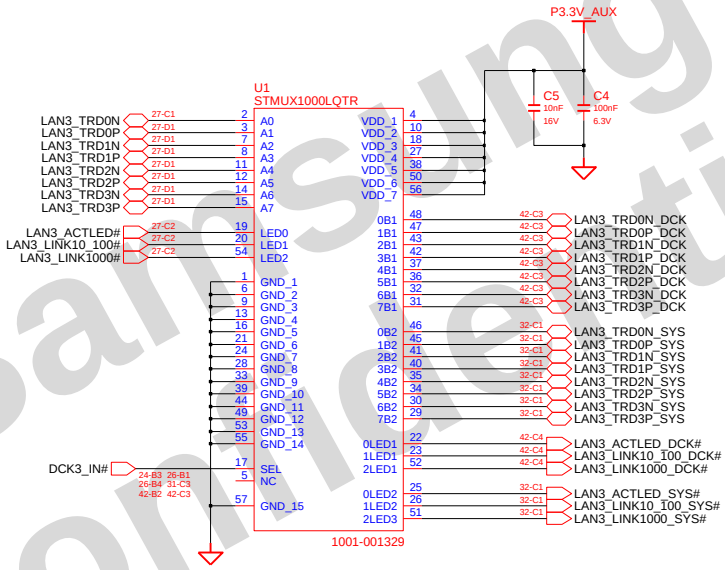
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN KEYBOARD CONTROLLER	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 26 OF 44	

LAN CONTROLLER



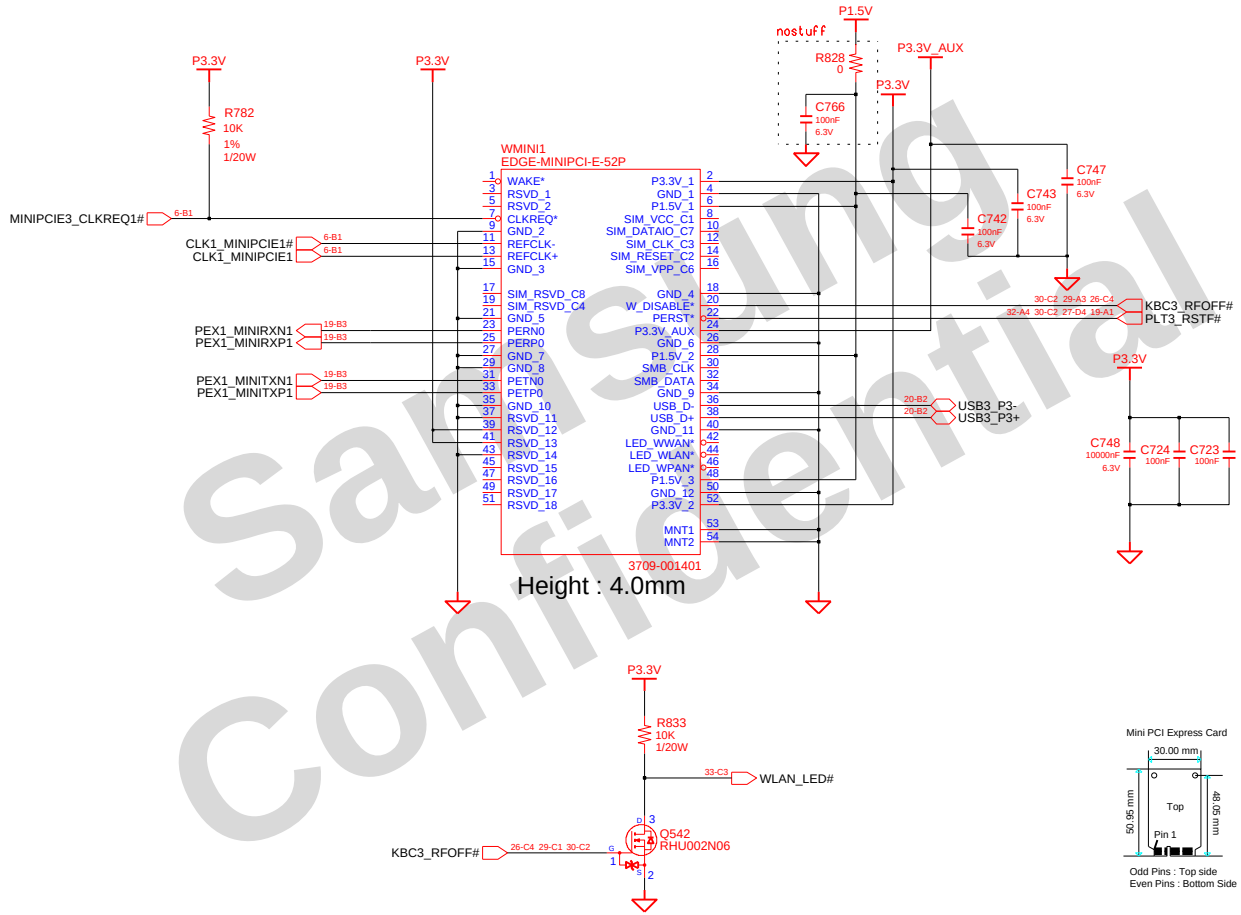
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN LAN CONTROLLER	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE:	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 27 OF 44	

LAN PASSTHRU BRIDGE CHIP



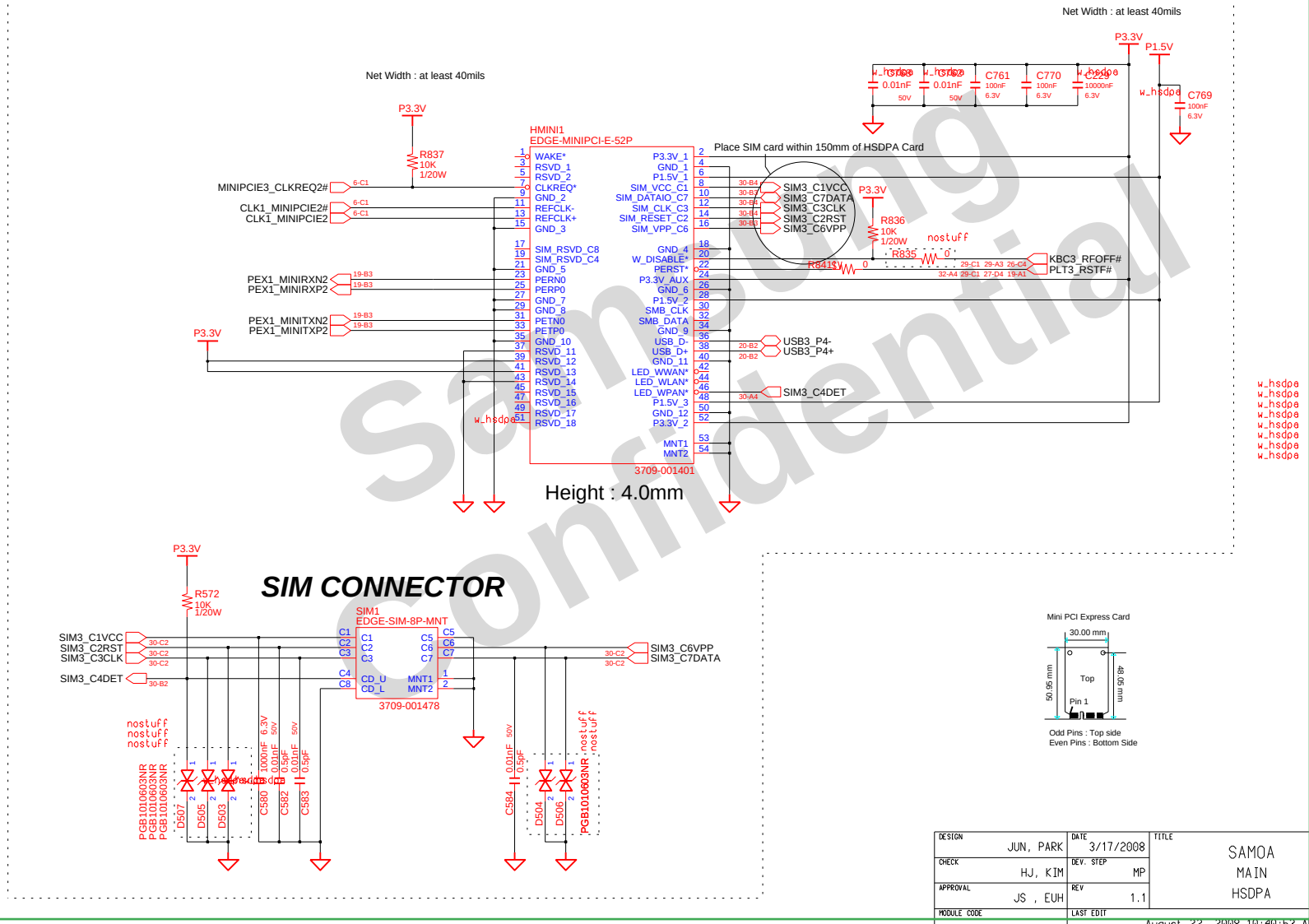
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN LAN DOCK I/F	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE:	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 28 OF 44	

MINICARD(WLAN)



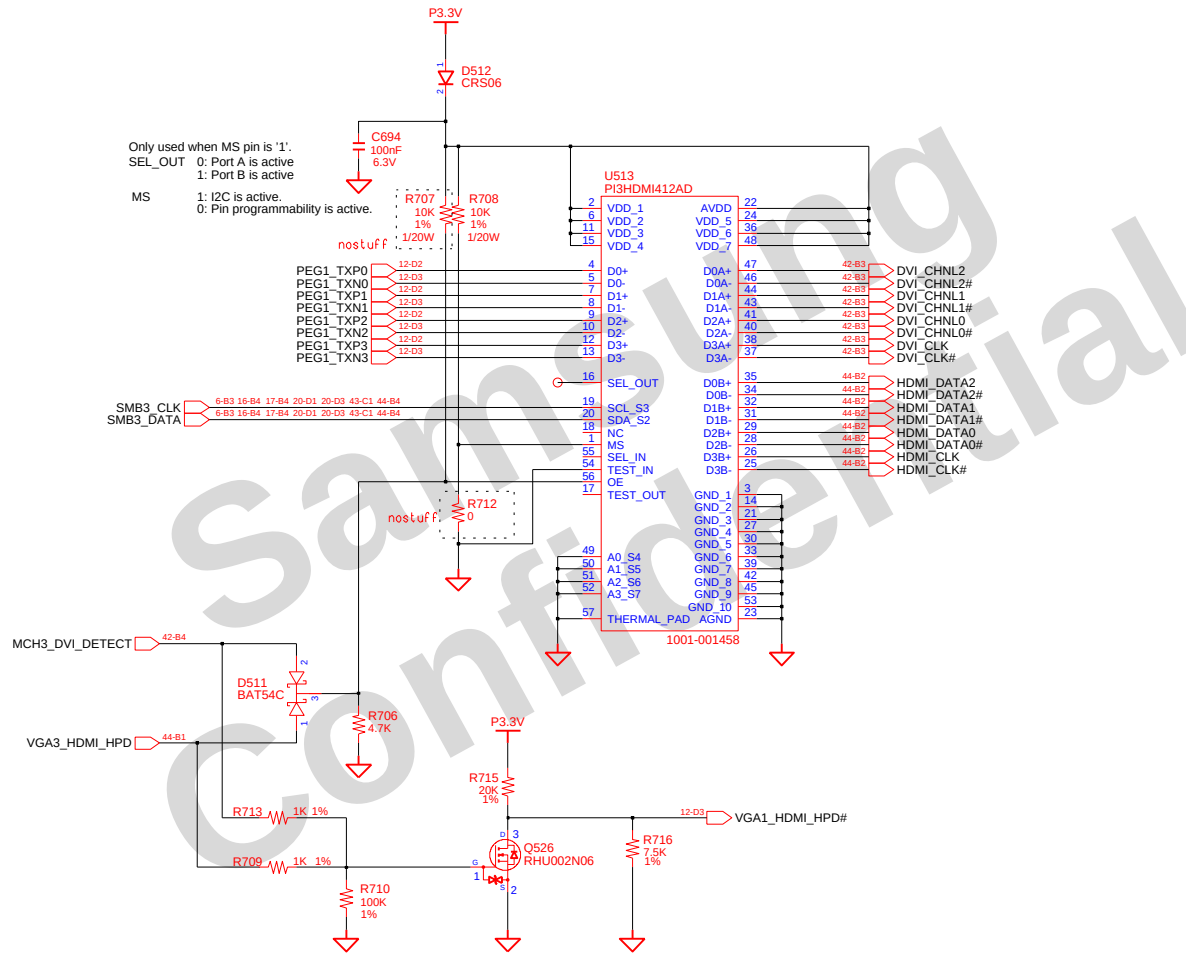
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN WIRELESS LAN	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE:	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 29 OF 44	

MINICARD(HSDPA)



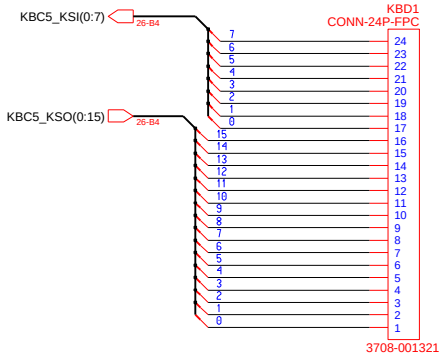
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN HSDPA	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM		PAGE 30 OF 44

HDMI & DVI I/F

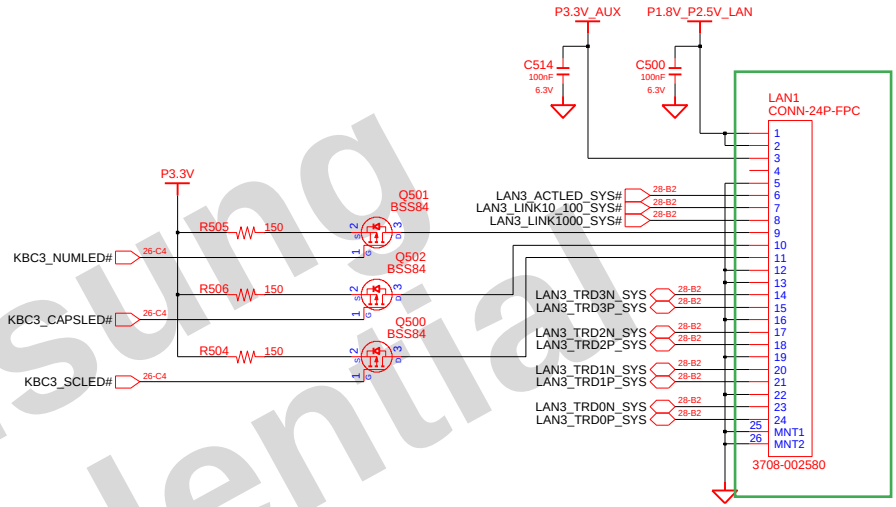


DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN HDMI & DVI I/F	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE:	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 31 OF 44	

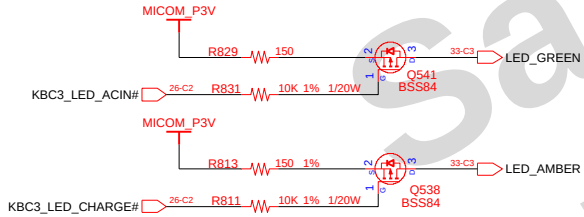
KEYBOARD CONNECTOR



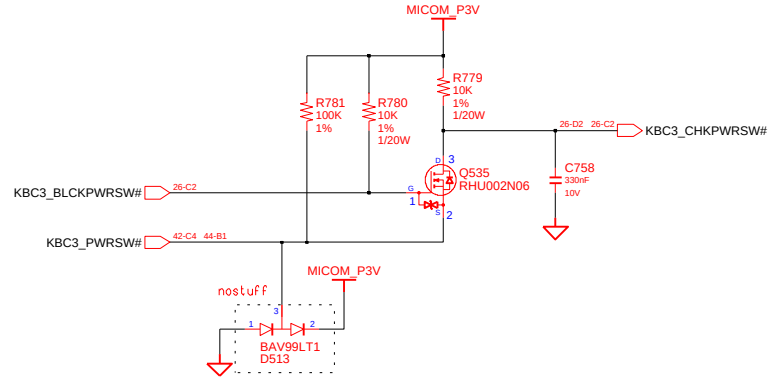
LAN BOARD CONNECTOR



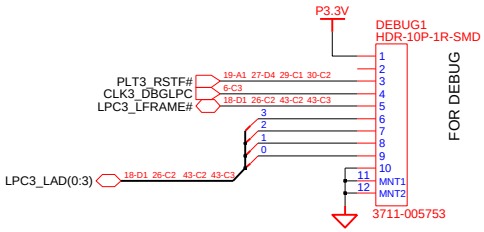
ADAPTERIN / CHARGING LED



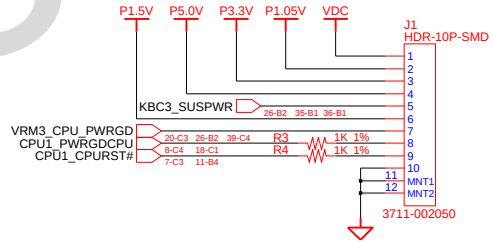
POWER S/W



DEBUG PORT

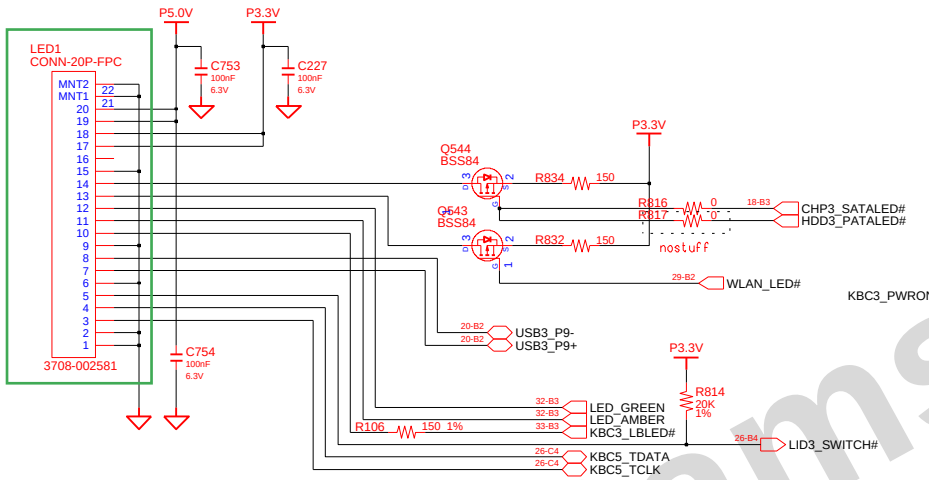


Pre FCT PORT

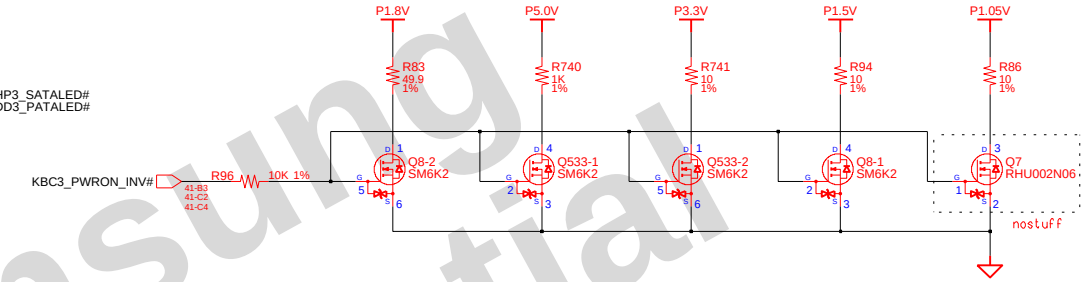


DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN KBD/LED/DEBUG/SUB CONN.	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 32 OF 44	

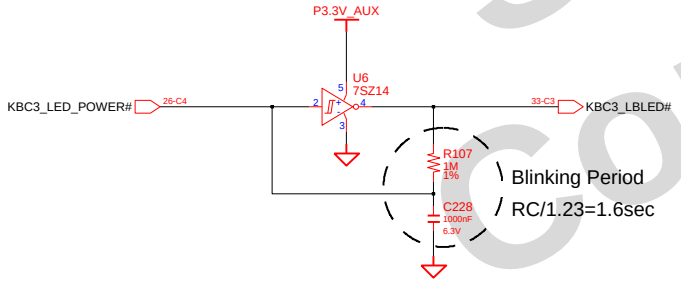
LED & T/P FPC CONNECTOR



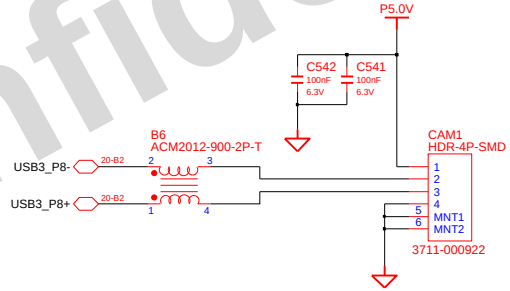
DISCHARGE



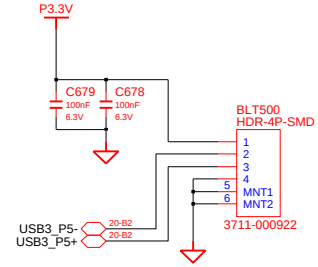
POWR ON / LB LED

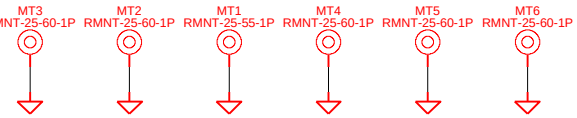


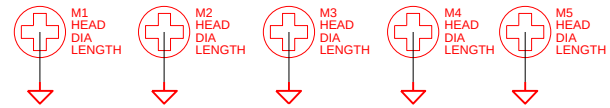
CAMERA



BLUETOOTH





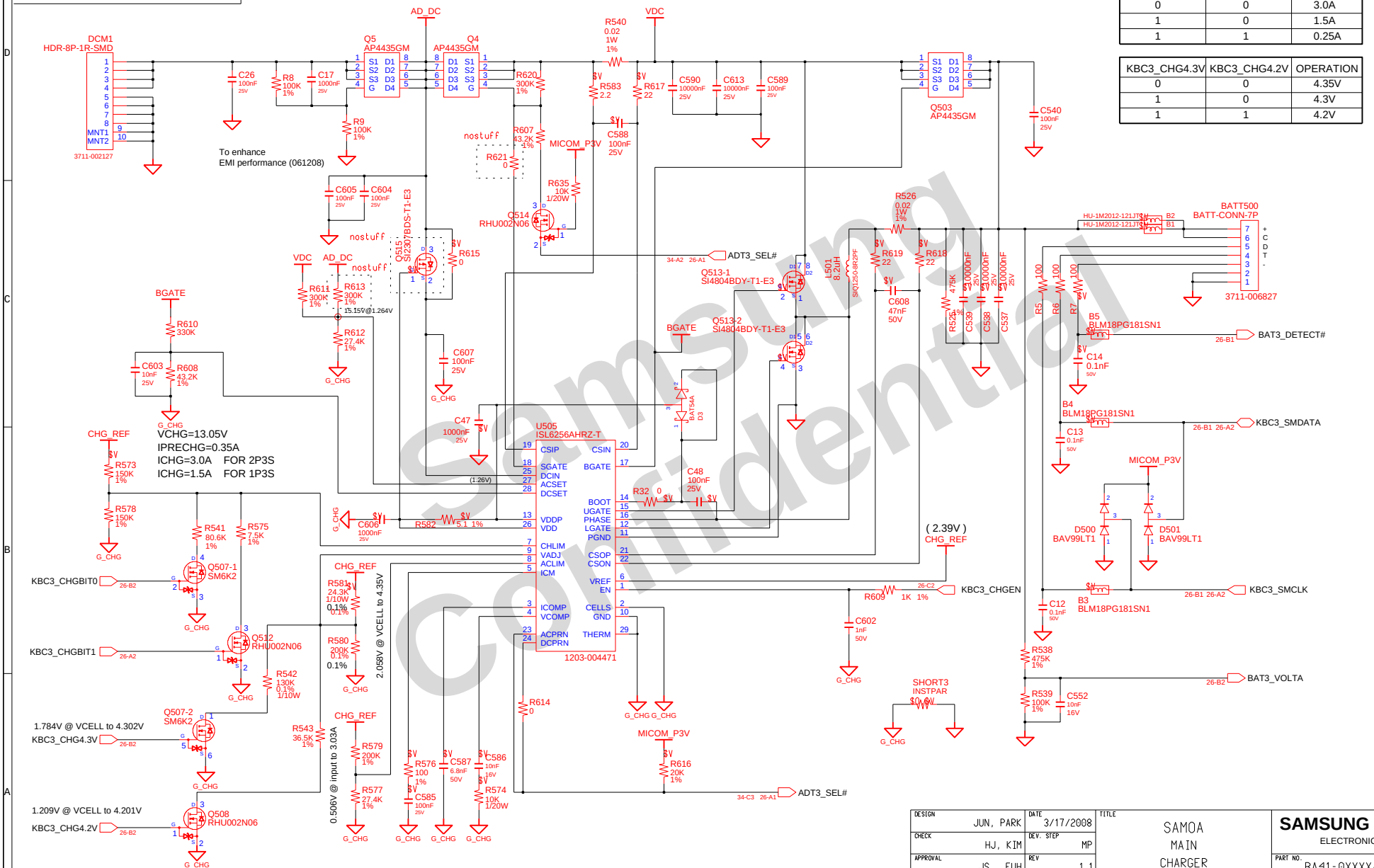


DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN CAMERA, BLUETOOTH & LED	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 33 OF 44	

CHARGER & POWER MANAGEMENT

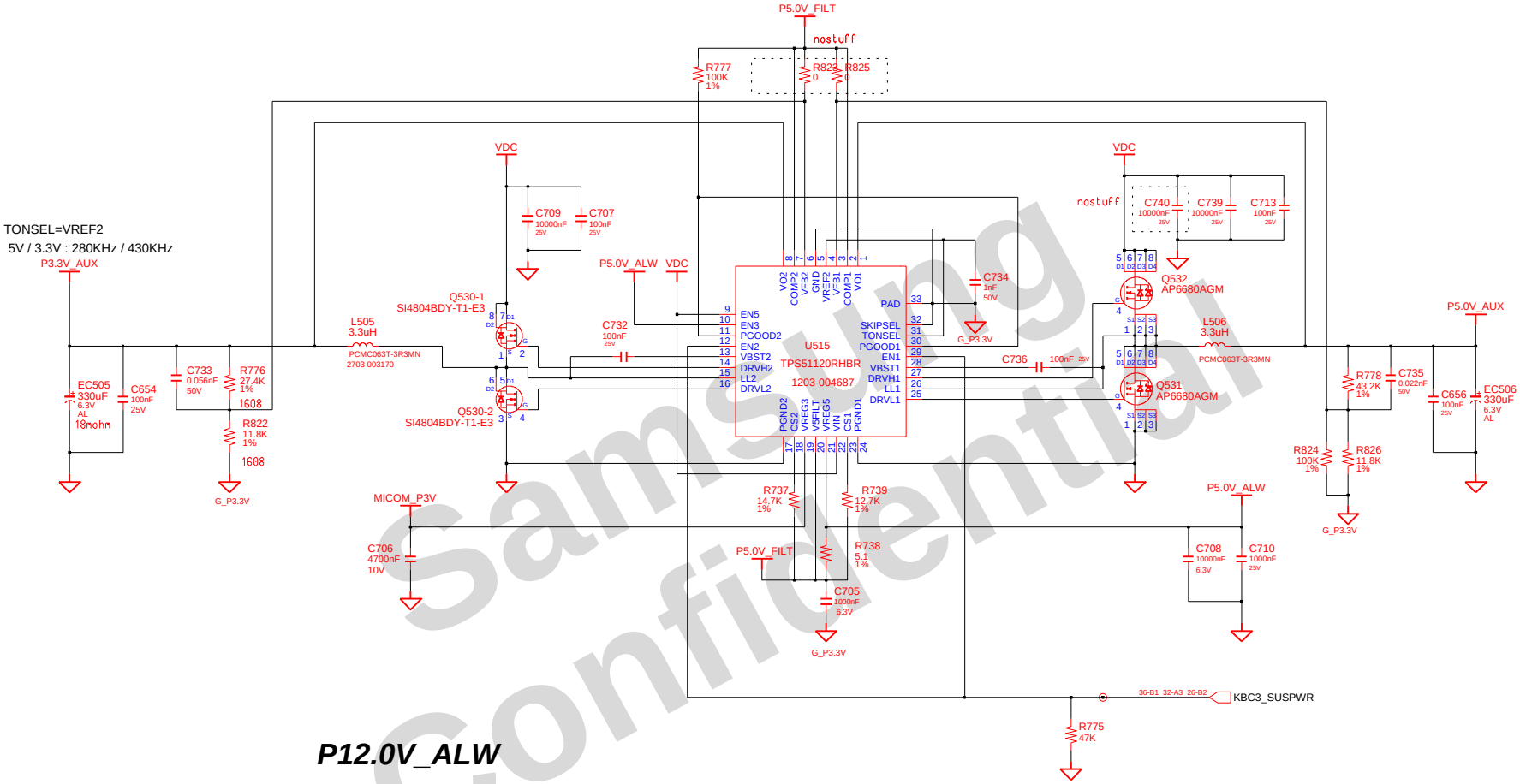
KBC3_CHGBIT0	KBC3_CHGBIT1	OPERATION
0	0	3.0A
1	0	1.5A
1	1	0.25A

KBC3_CHG4.3V	KBC3_CHG4.2V	OPERATION
0	0	4.35V
1	0	4.3V
1	1	4.2V

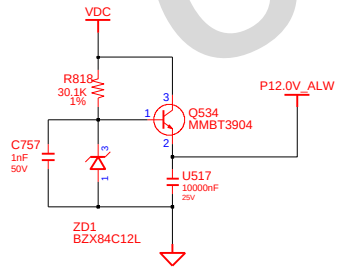


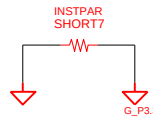
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN CHARGER	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 34 OF 44	

P5.0V_AUX & P3.3V_AUX



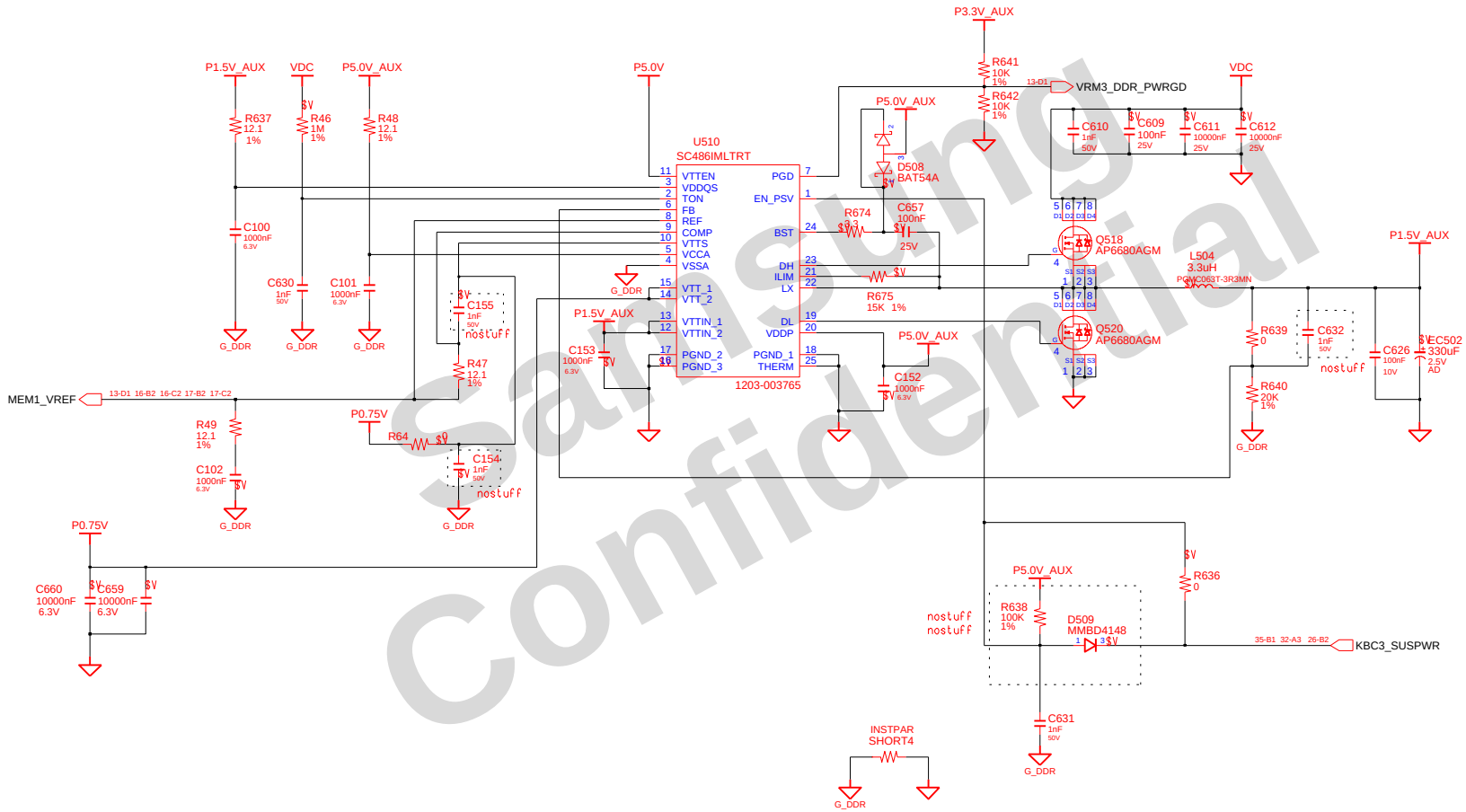
P12.0V_ALW





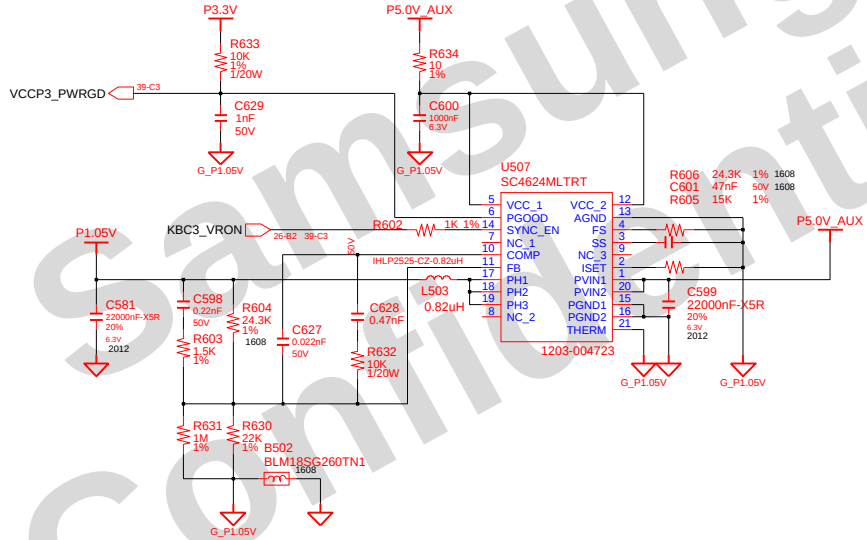
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN P5.0V & P3.3V	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 35 OF 44	

DDR3 Power



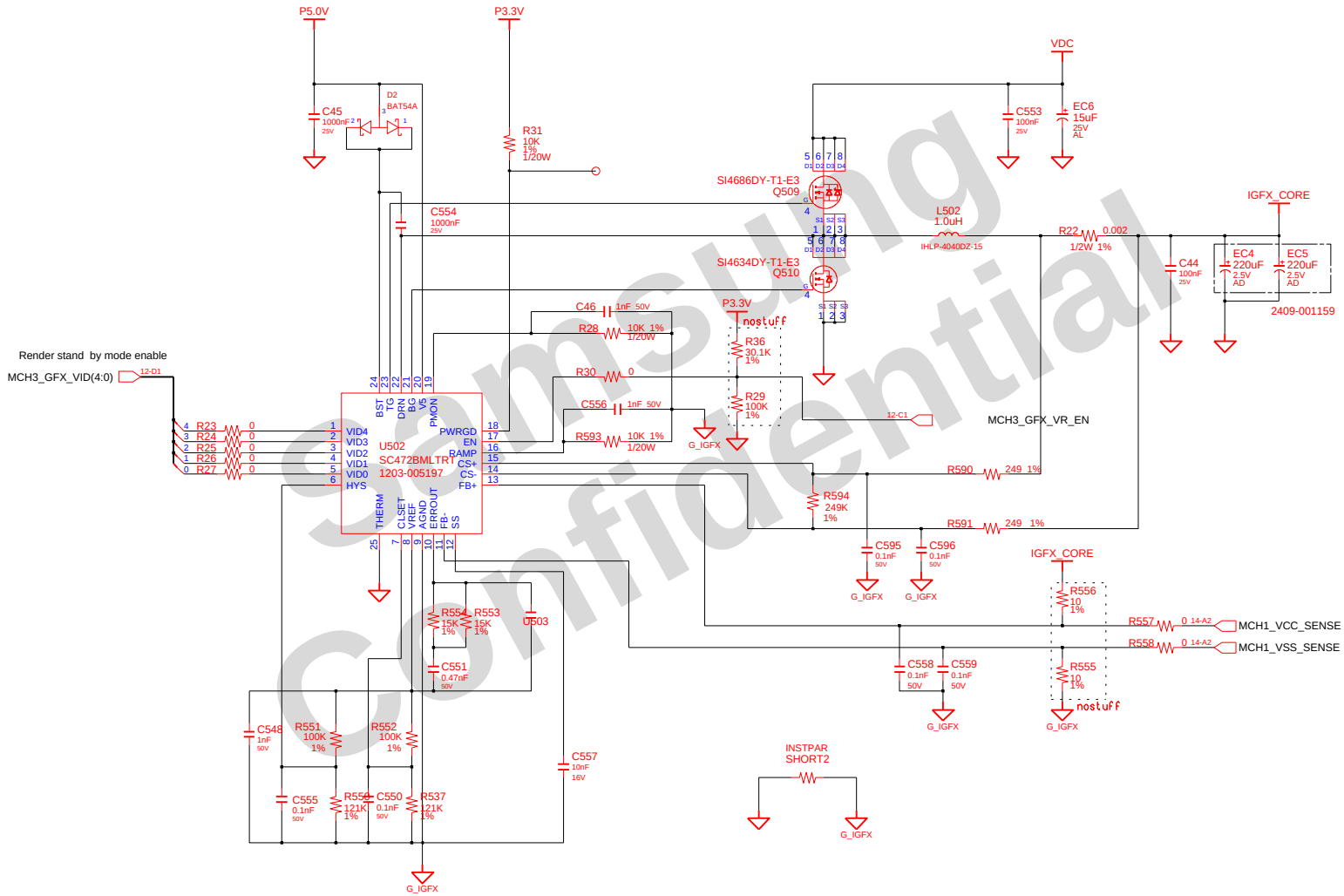
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN DDR3 POWER	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE:	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 36 OF 44	

VCCP_CORE



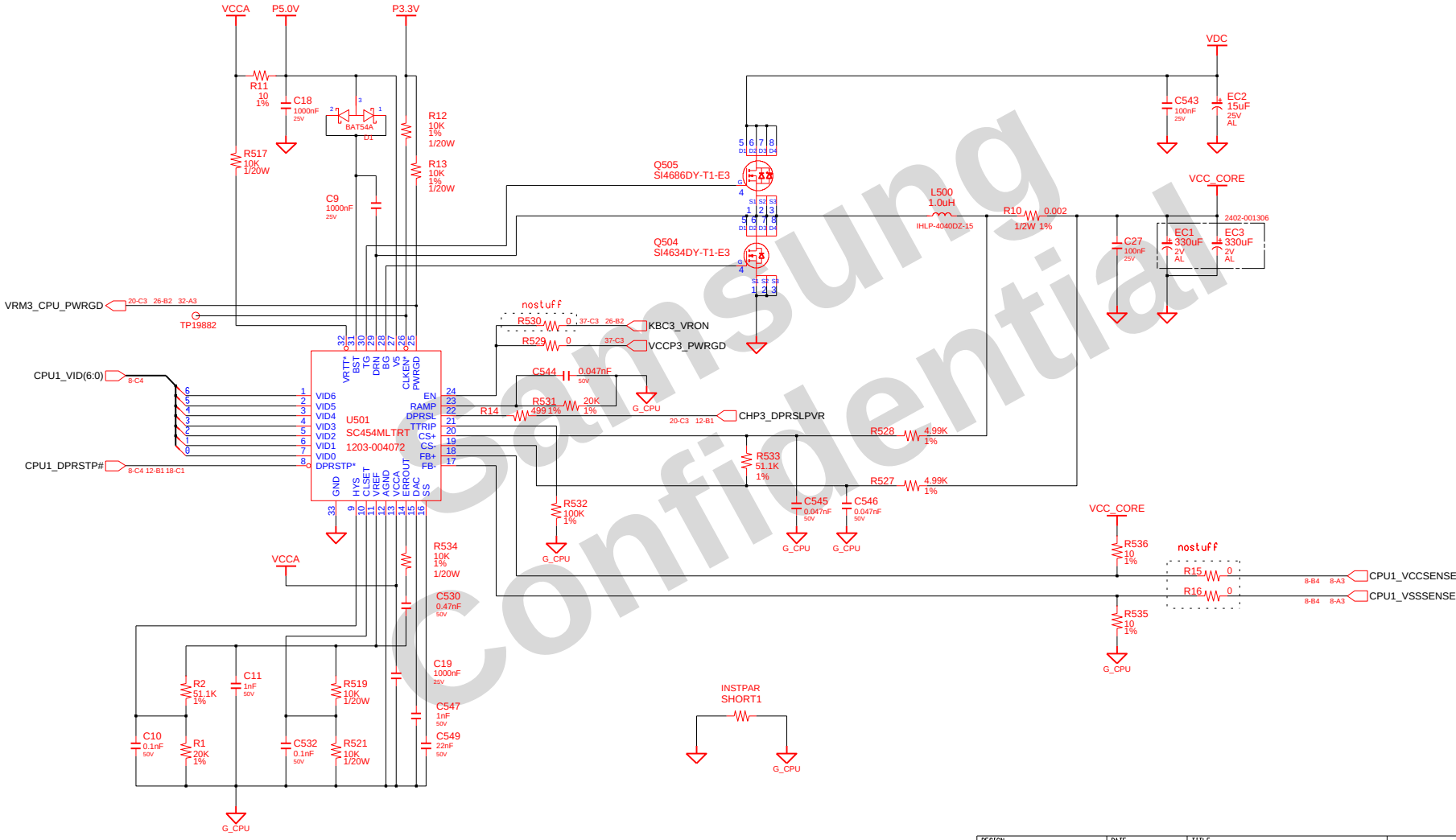
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN DDR2 POWER	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE:	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 37 OF 44	

INTERNAL GFX CORE



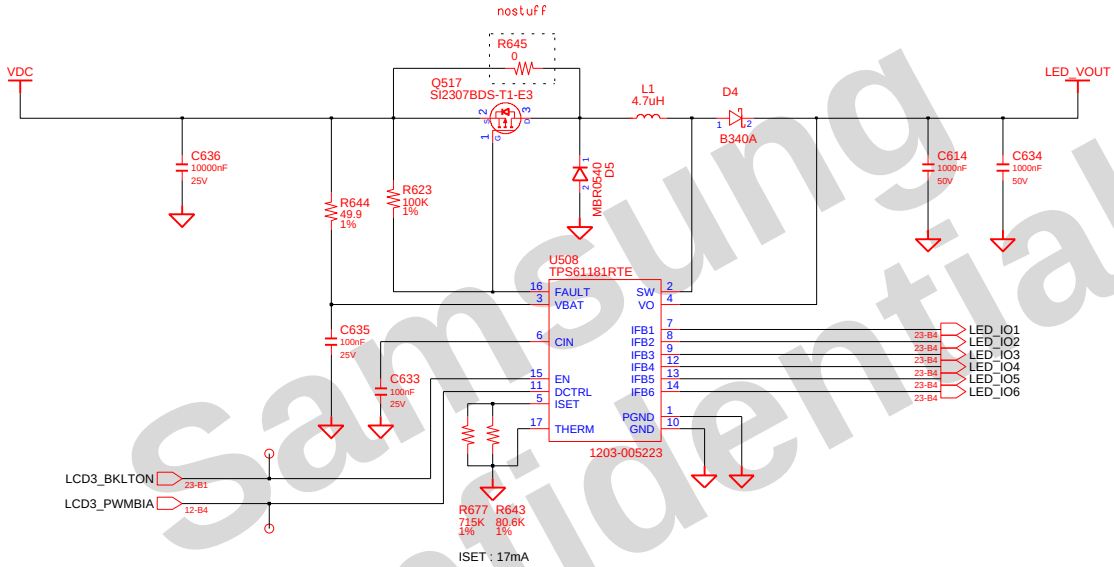
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN INTERNAL GFX CORE	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE:	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 38 OF 44	

CPU VRM POWER



DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA / MAIN / CPU VRM POWER	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE:	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 39 OF 44	

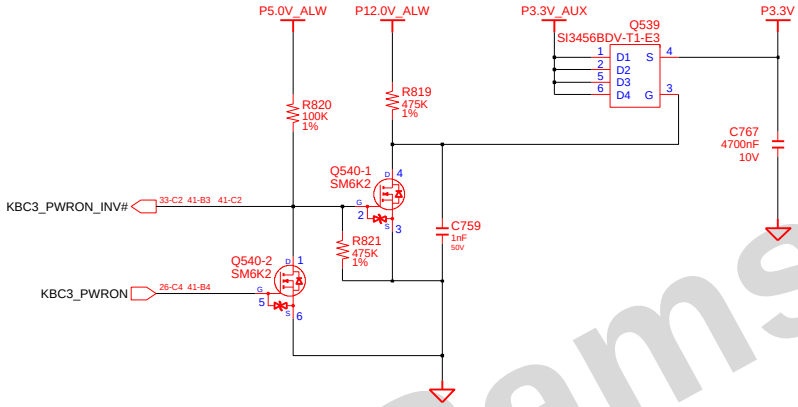
LED DRIVER



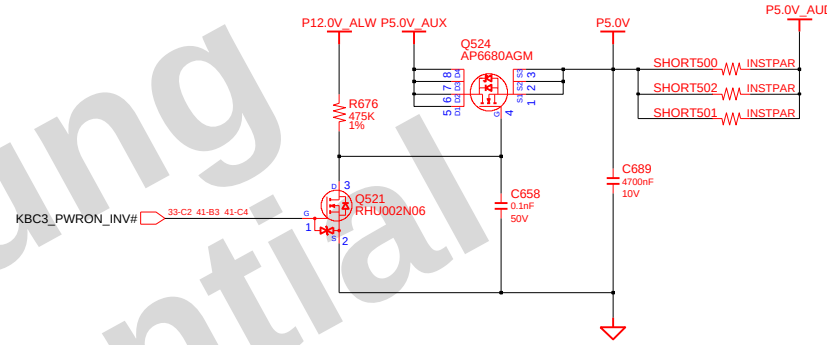
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN LED DRIVER	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE:	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 40 OF 44	

SWITCHED POWER

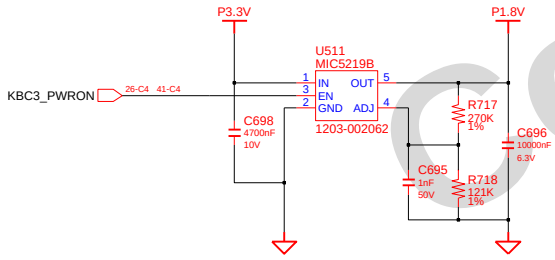
Switched Power On (P3.3V)



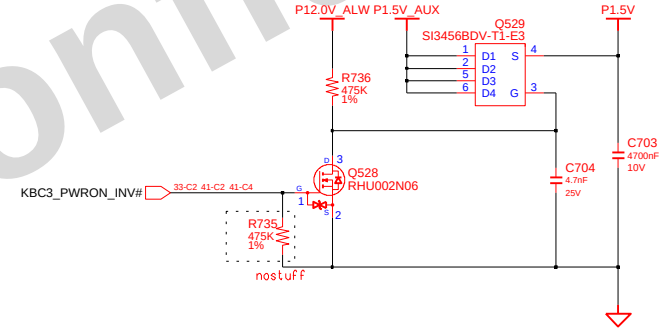
Switched Power On (P5V)



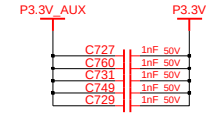
Switched Power On (P1.8V)



Switched Power On (P1.5V)

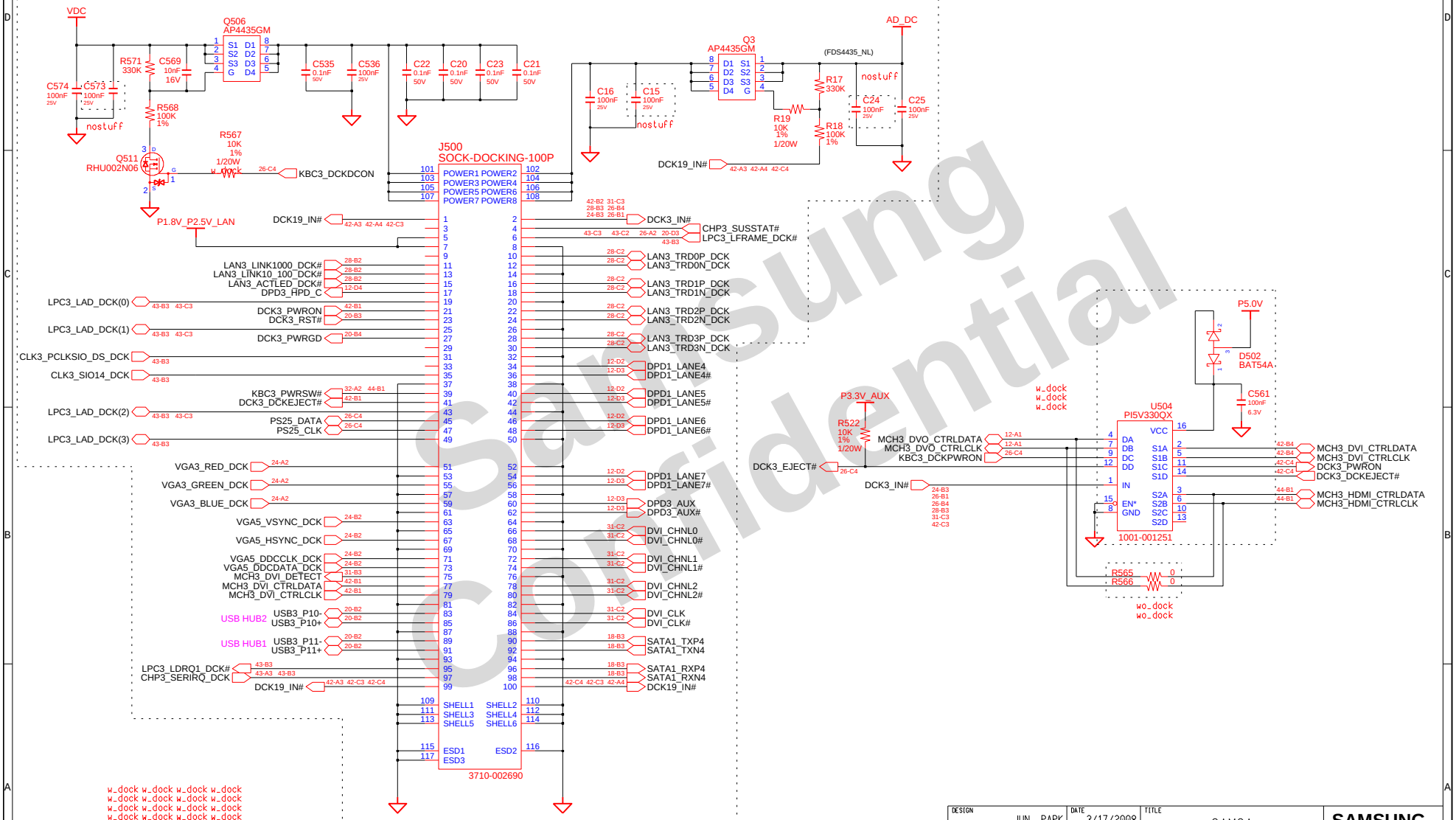


Stiching caps(For EMC)



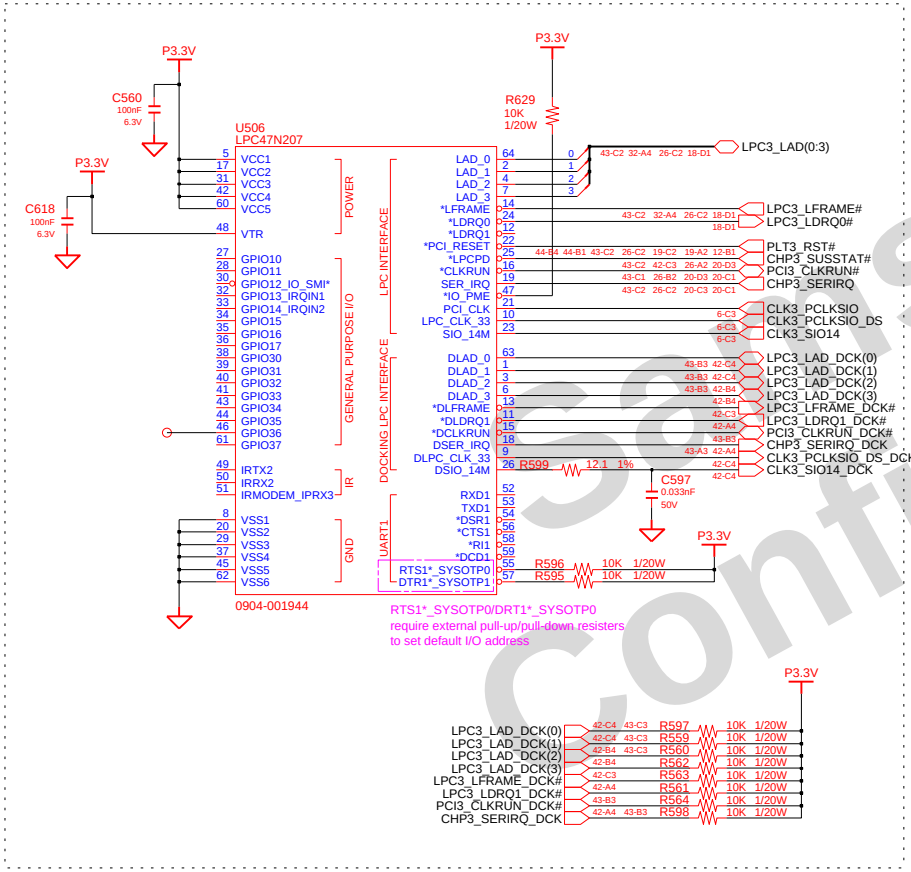
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE:	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 41 OF 44	

DOCKING CONNECTOR

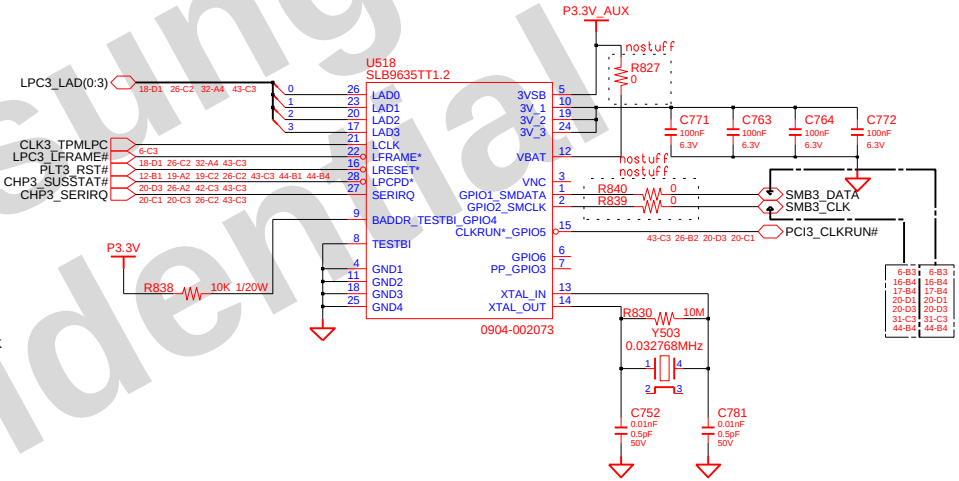


DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN DOCKING I/F	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 42 OF 44	

LPC I/F



TPM 1.2



w_dock w_dock
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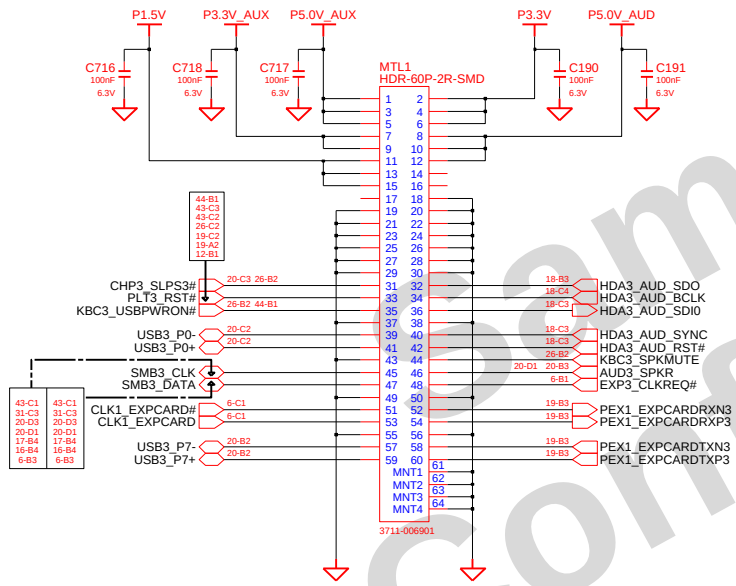
w_dock w_dock

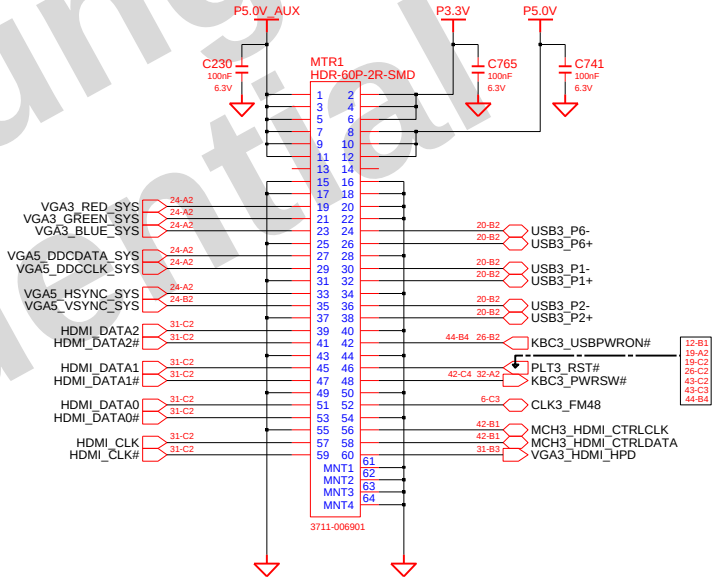
DESIGN: JUN, PARK	DATE: 3/17/2008	TITLE: SAMOA MAIN LPC I/F	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-OXXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 43 OF 44	

MAIN to SUB CONNECTOR

FOR SUB_LEFT BOARD



FOR SUB_RIGHT BOARD



DESIGN: JUN, PARK	DATE: 1/4/2008	TITLE: SAMOA MAIN LEFT SUB CONNECTOR	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS , EUH	REV: 1.1		PART NO.: BA41-0XXXXA
MODULE CODE	LAST EDIT: August 22, 2008 10:40:53 AM	PAGE 44 OF 44	

SAMOA SUB

CPU : PENRYN SFF
Chip Set : CANTIGA GS & ICH9M SFF
Remarks : INTEL MONTEVINA SFF

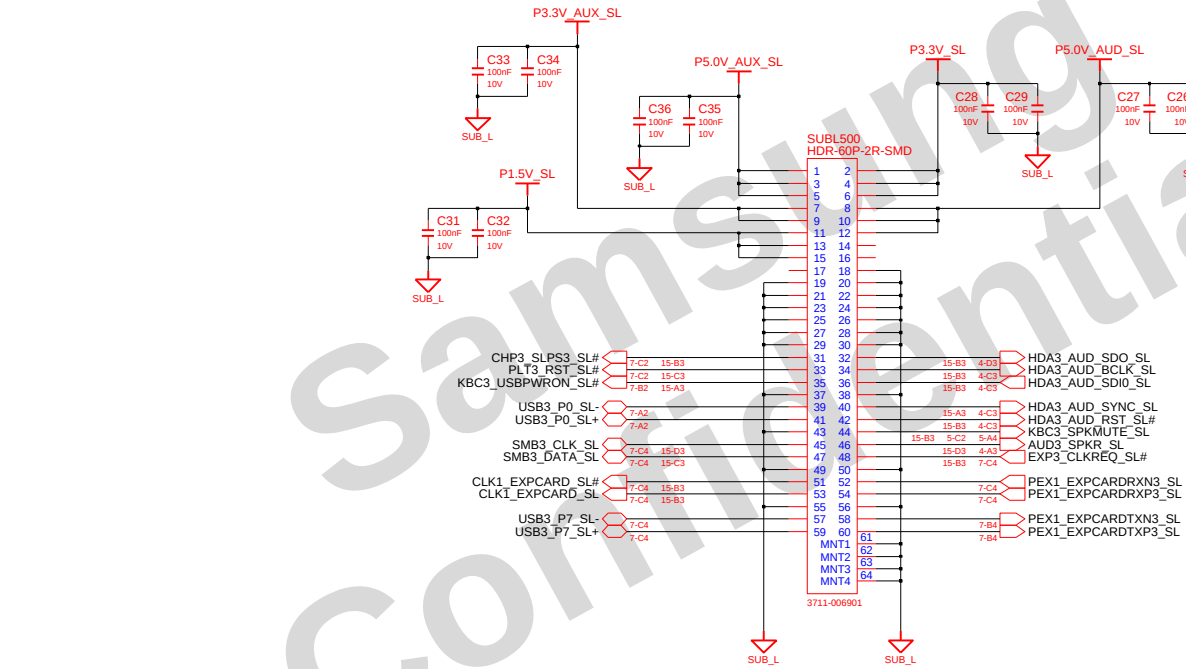
Model Name : SAMOA SUB BOARD
PCB Code : BA41-00903A(Nanya_CHN)
BA41-00904A(GCE_CHN)
Dev. Step : PR/MP
Revision : 1.1
T.R. Date :

DESIGN	CHECK	APPROVAL
Jun PARK	HJ KIM	JS EUH

Table of Contents

DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB BOARD COVER	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS, EUH	REV: 1.1		PART NO.: BA41-#####A
MODULE CODE:	LAST EDIT: August 22, 2008 10:42:11 AM	PAGE 1 OF 15	

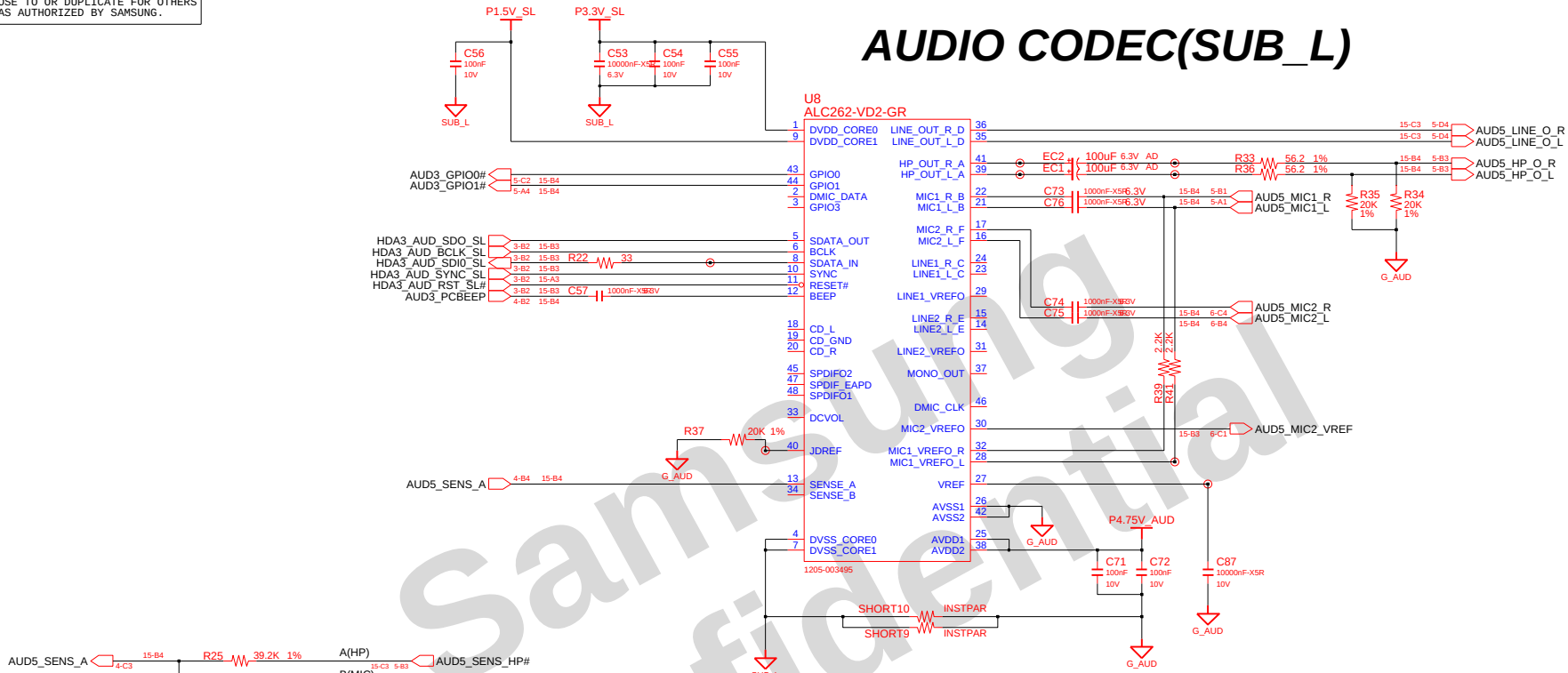
MAIN to SUB CONNECTOR(SUB_L)



MT1 RMNT-25-50-1P
MT2 RMNT-25-50-1P
MT4 RMNT-25-50-1P
SUB_L

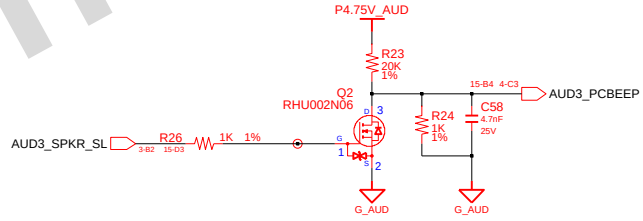
DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB LEFT MAIN TO SUB_L CONNECTOR	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS, EUH	REV: 1.1		PART NO.: BA41-######A
MODULE CODE:	LAST EDIT: August 22, 2008 10:42:11 AM	PAGE 3 OF 15	

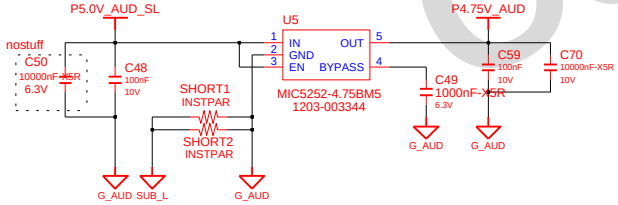
AUDIO CODEC(SUB_L)



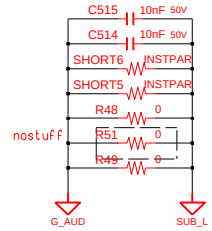
1.AGND_AUD	Aduio Ground
2.GND	Digital Ground

PC BEEP SOUND(SUB_L)





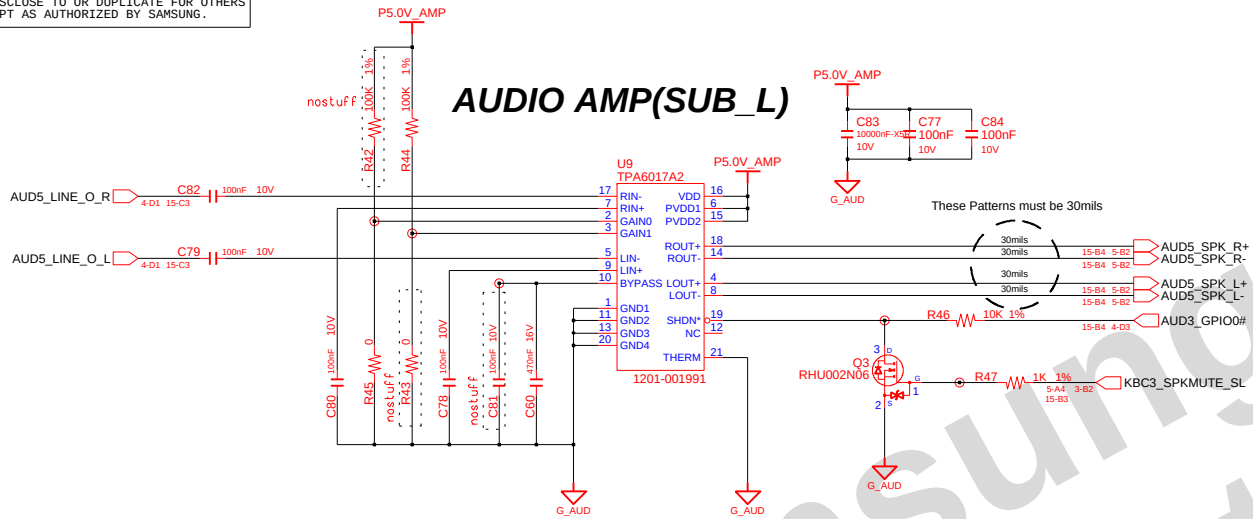
ALL 1608 SIZE



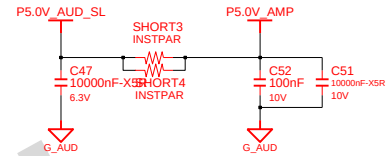
DESIGN	JUN, PARK	DATE	1/17/2008	TITLE	SAMOA SUB LEFT AUDIO CONDEC
CHECK	HJ, KIM	DEV. STEP	MP		
APPROVAL	JS, EUH	REV	1.1		
MODULE CODE		LAST EDIT	August 22, 2008 10:42:11 AM	PAGE	4 OF 15

SAMSUNG ELECTRONICS
PART NO. BA41-######A

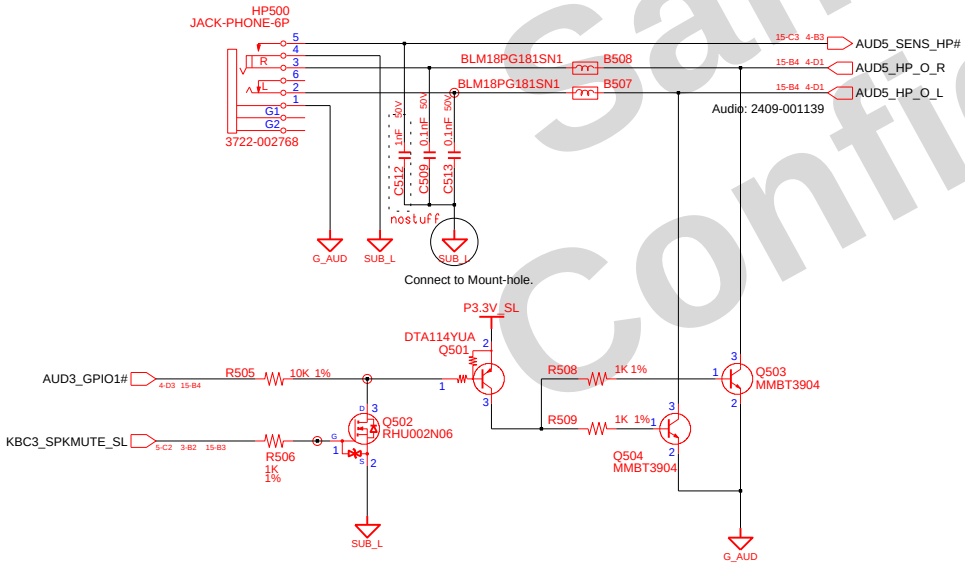
AUDIO AMP(SUB_L)



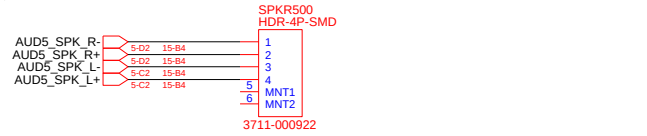
AMP_VDD(SUB_L)



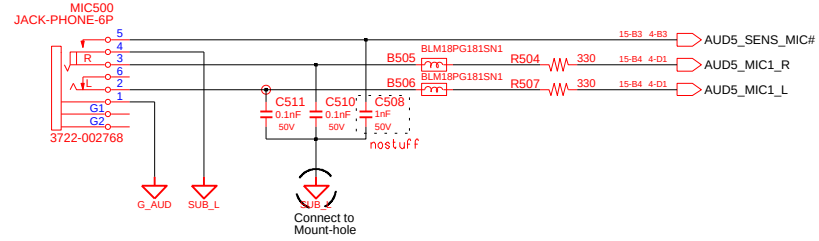
HEADPHONE(SUB_L)



INTERNAL STEREO SPEAKERS(SUB_L)



MIC JACK(SUB_L)



DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB LEFT AUDIO AMP & JACK	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS, EUH	REV: 1.1		PART NO.: BA41-#####A
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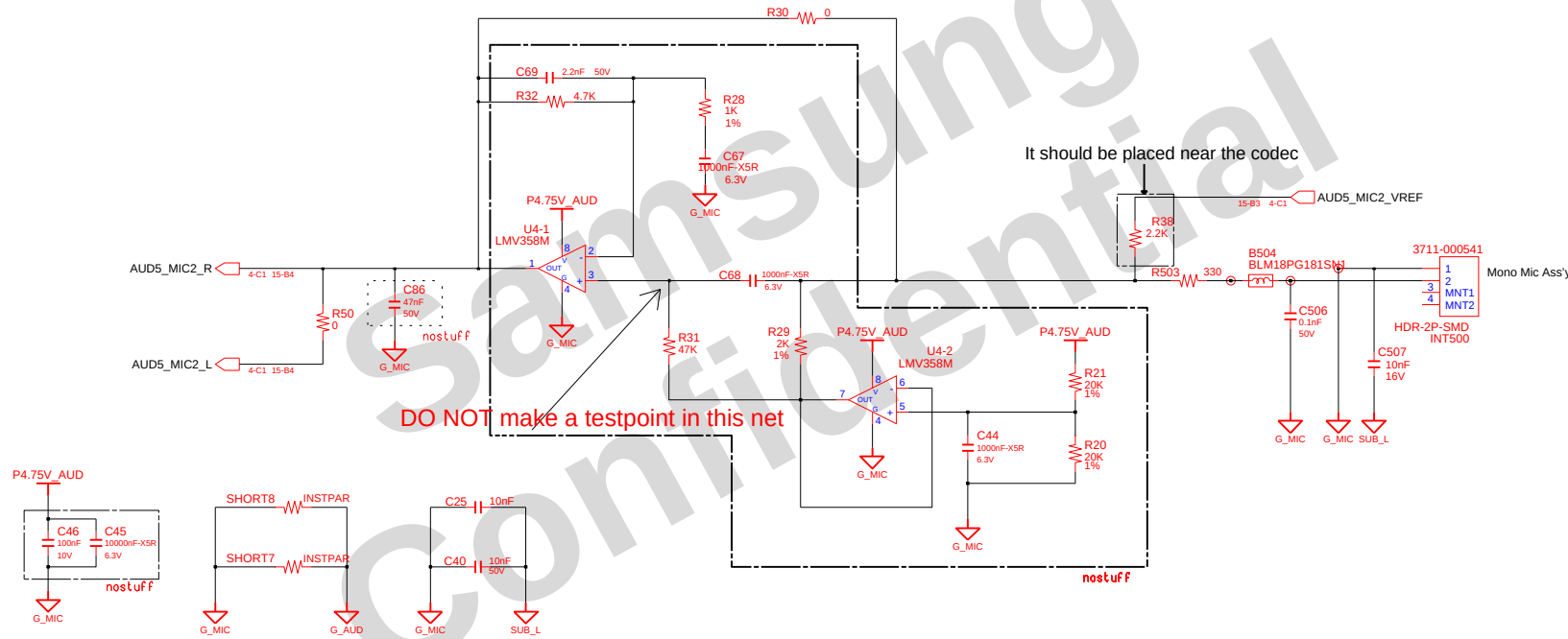
INTERNAL MIC(SUB_L)



DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB LEFT INTERNAL MIC	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS, EUH	REV: 1.1		PART NO.: BA41-######A
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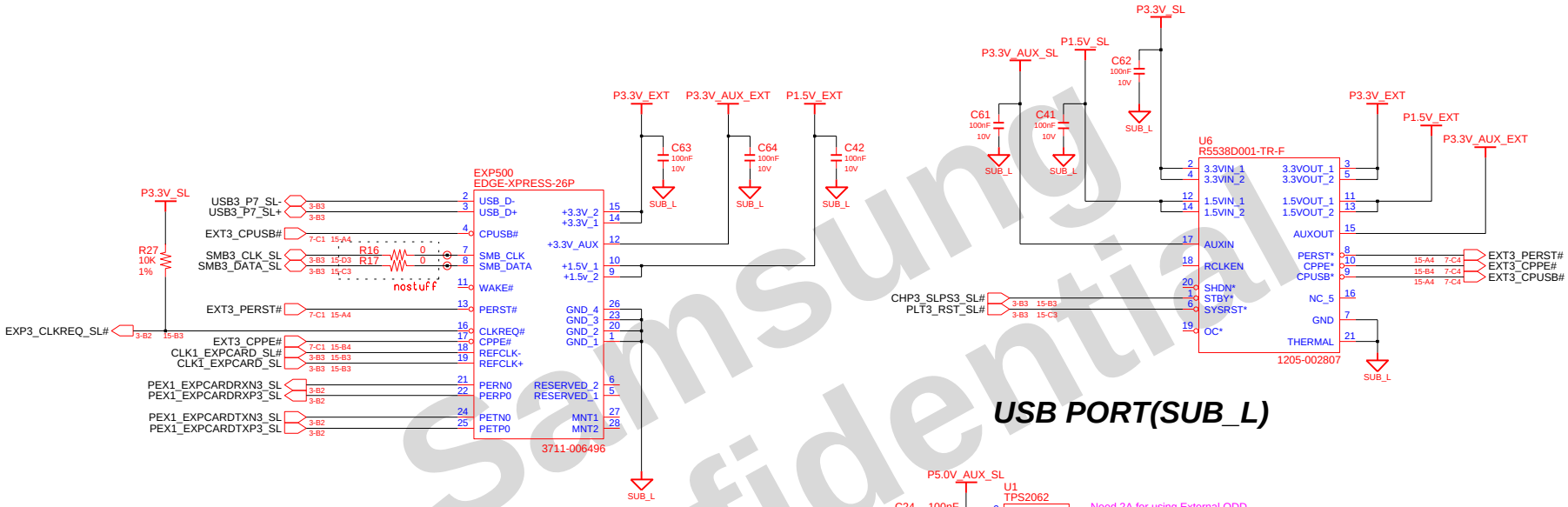
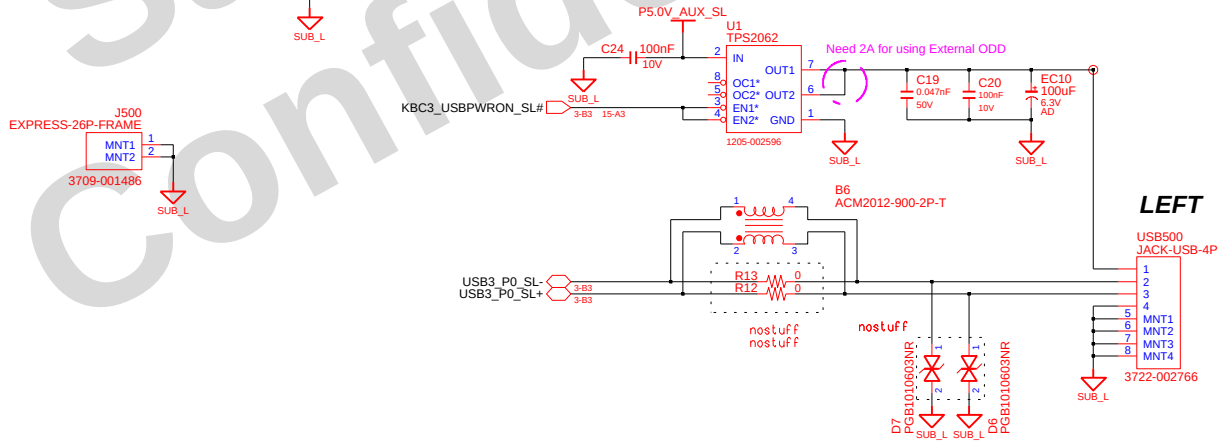
EXPRESS CARD(SUB_L)

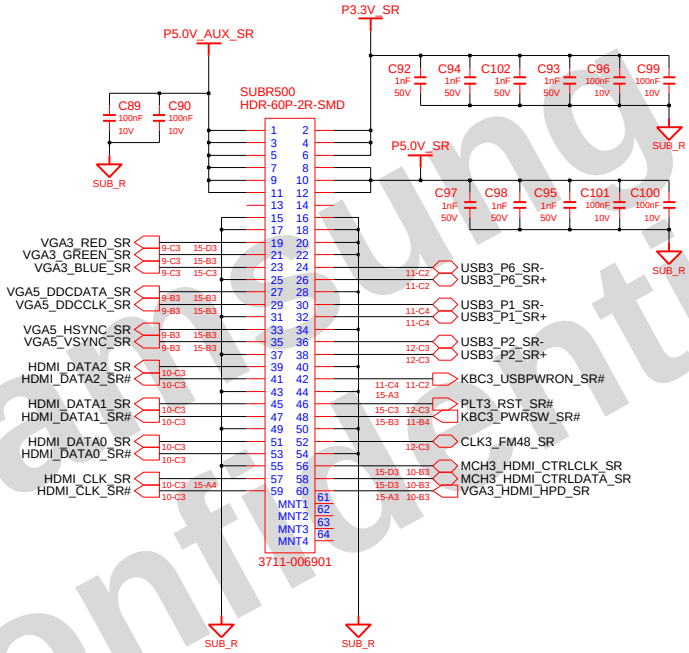


USB PORT(SUB_L)

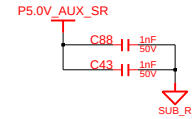


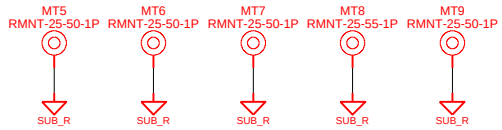
DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA / SUB LEFT / EXPRESS CARD & USB PORT	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		PART NO.: BA41-#####A
APPROVAL: JS, EUH	REV: 1.1		
MODULE CODE:	LAST EDIT: August 22, 2008 10:42:11 AM	PAGE 7 OF 15	

MAIN to SUB CONNECTOR(SUB_R)



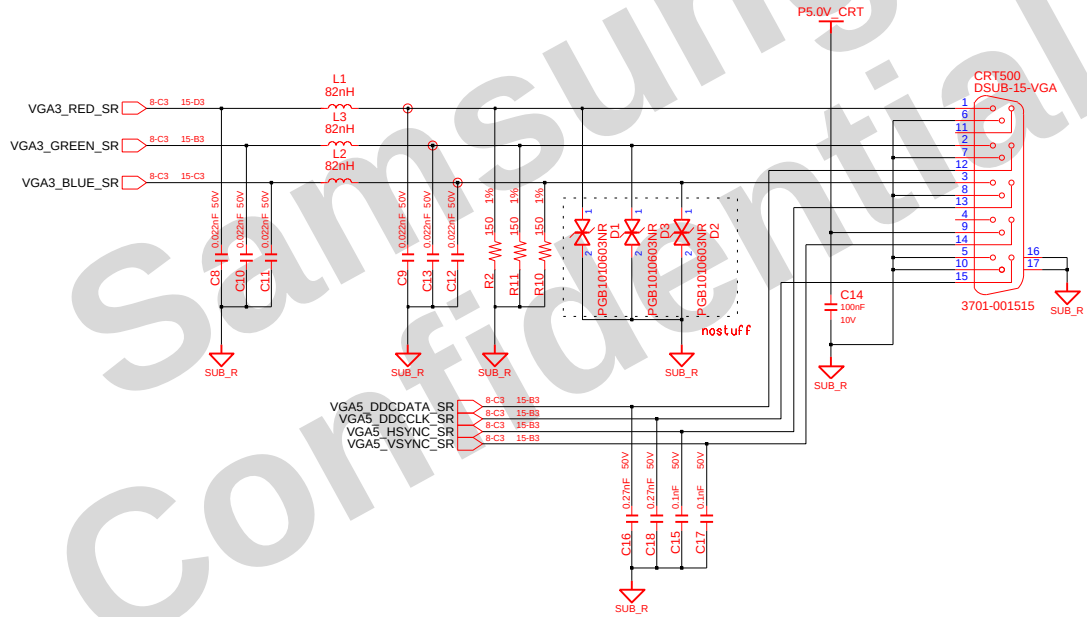
Stiching caps(For EMC)





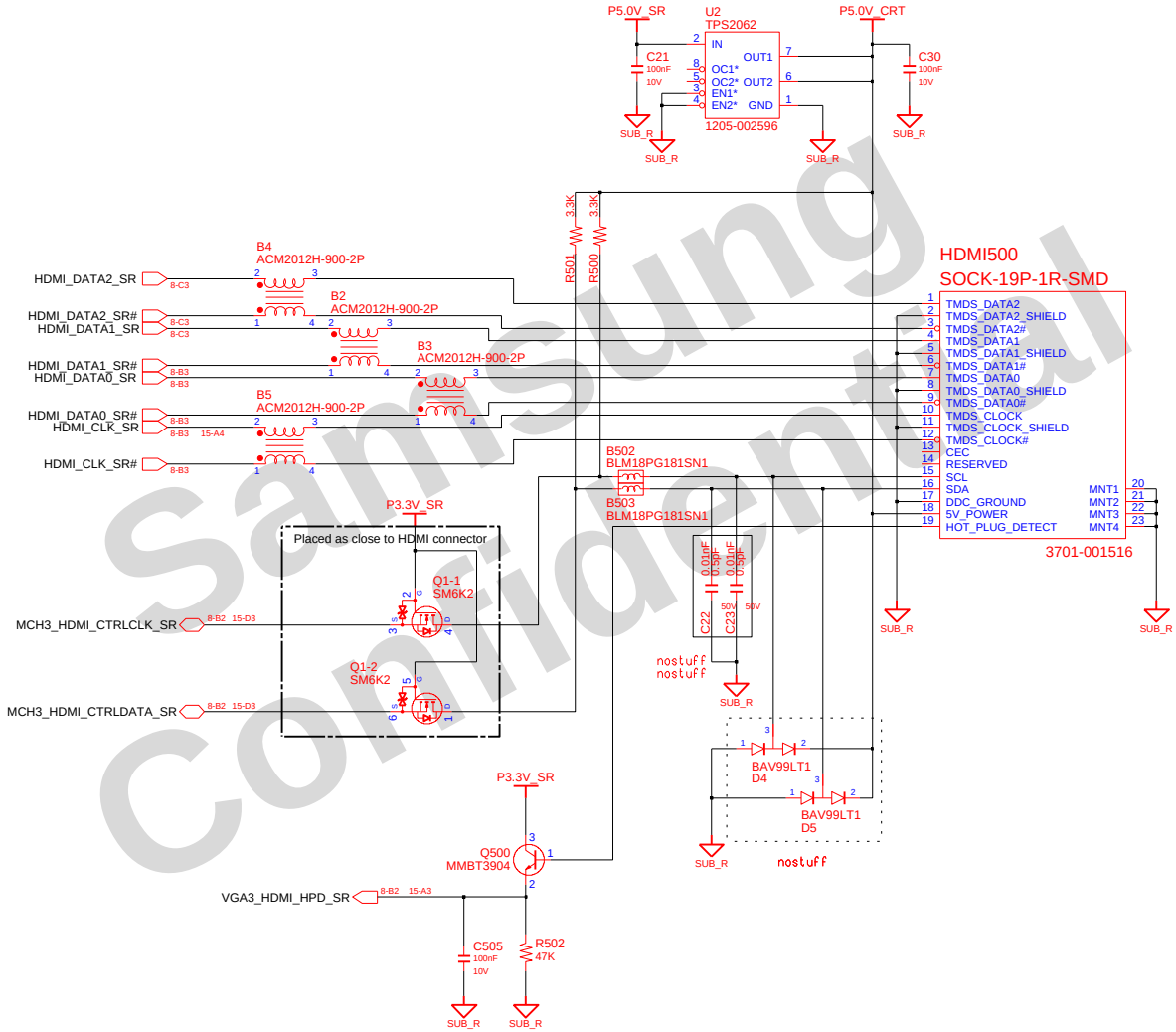
DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB RIGHT MAIN TO SUB CONNECTOR	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS, EUH	REV: 1.1		PART NO.: BA41-######A
MODULE CODE:	LAST EDIT: August 22, 2008 10:42:11 AM	PAGE 8 OF 15	

CRT CONNECTOR(SUB_R)



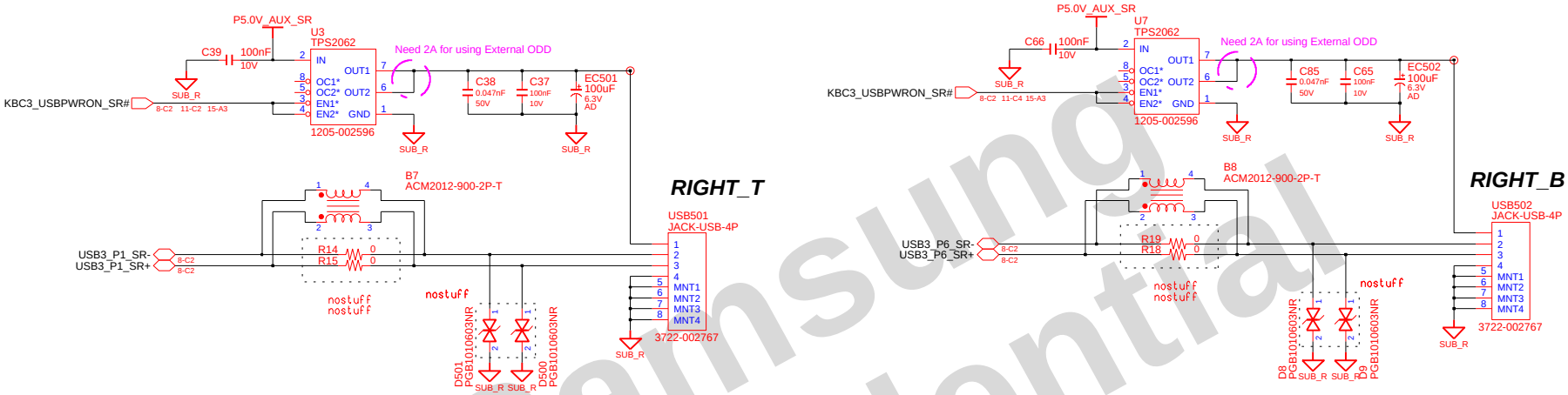
DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB RIGHT CRT CONNECTOR	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS, EUH	REV: 1.1		PART NO.: BA41-######A
MODULE CODE:	LAST EDIT: August 22, 2008 10:42:11 AM	PAGE 9 OF 15	

HDMI CONNECTOR(SUB_R)

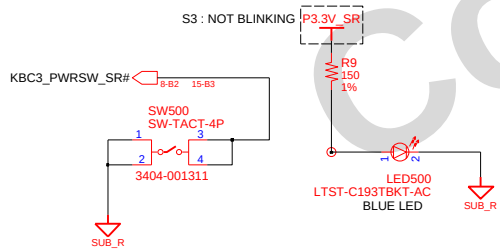


DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB RIGHT HDMI CONNECTOR	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS, EUH	REV: 1.1		PART NO.: BA41-#####A
MODULE CODE:	LAST EDIT: August 22, 2008 10:42:11 AM	PAGE 10 OF 15	

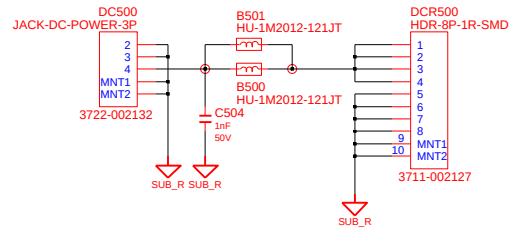
USB PORT(SUB_R)



POWER S/W(SUB_R)



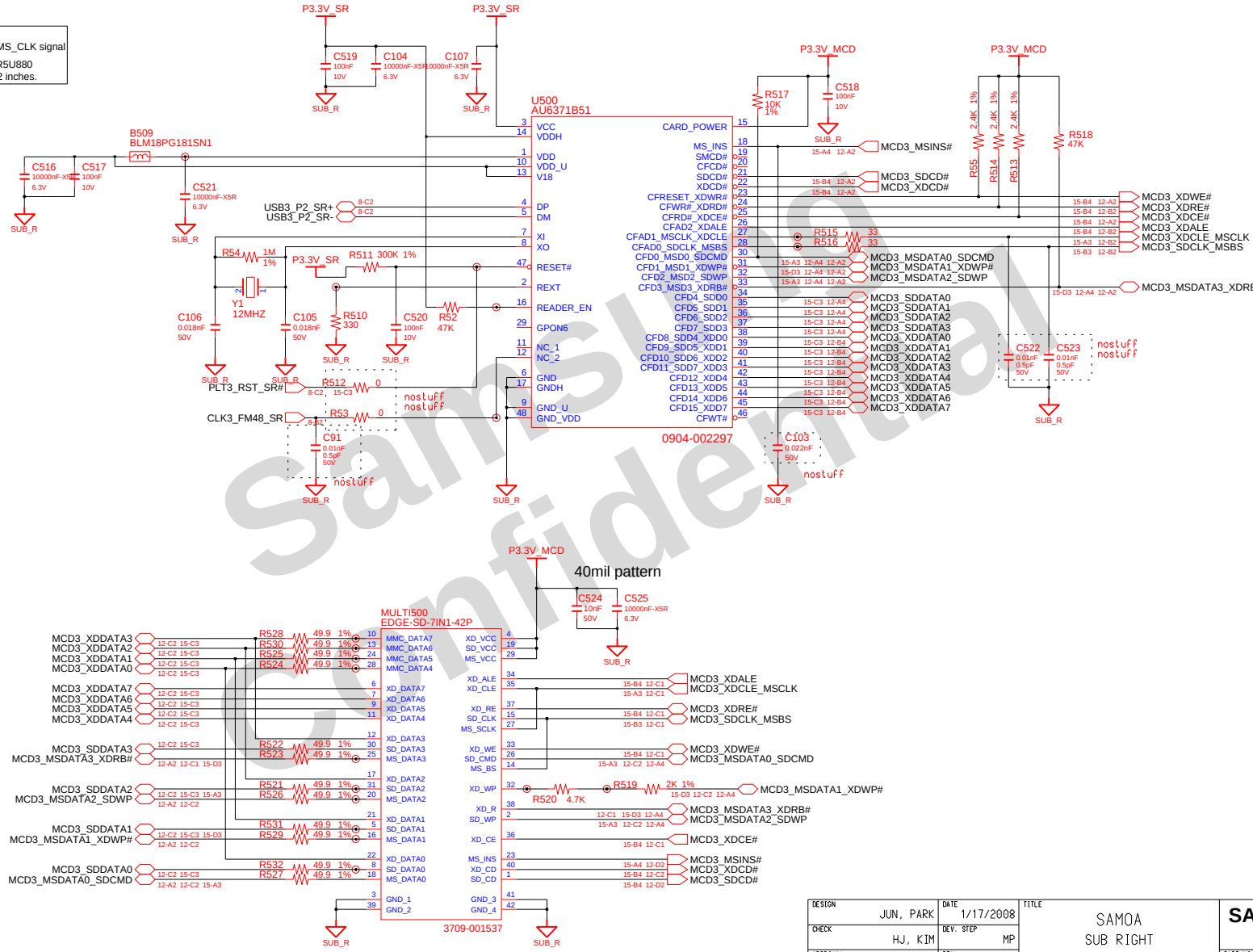
DC JACK(SUB_R)



DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB RIGHT USB,POWER S/W&DC JACK	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS, EUH	REV: 1.1		PART NO.: BA41-#####A
MODULE CODE:	LAST EDIT: August 22, 2008 10:42:11 AM	PAGE 11 OF 15	

CARD READER(AU6371, SUB_R)

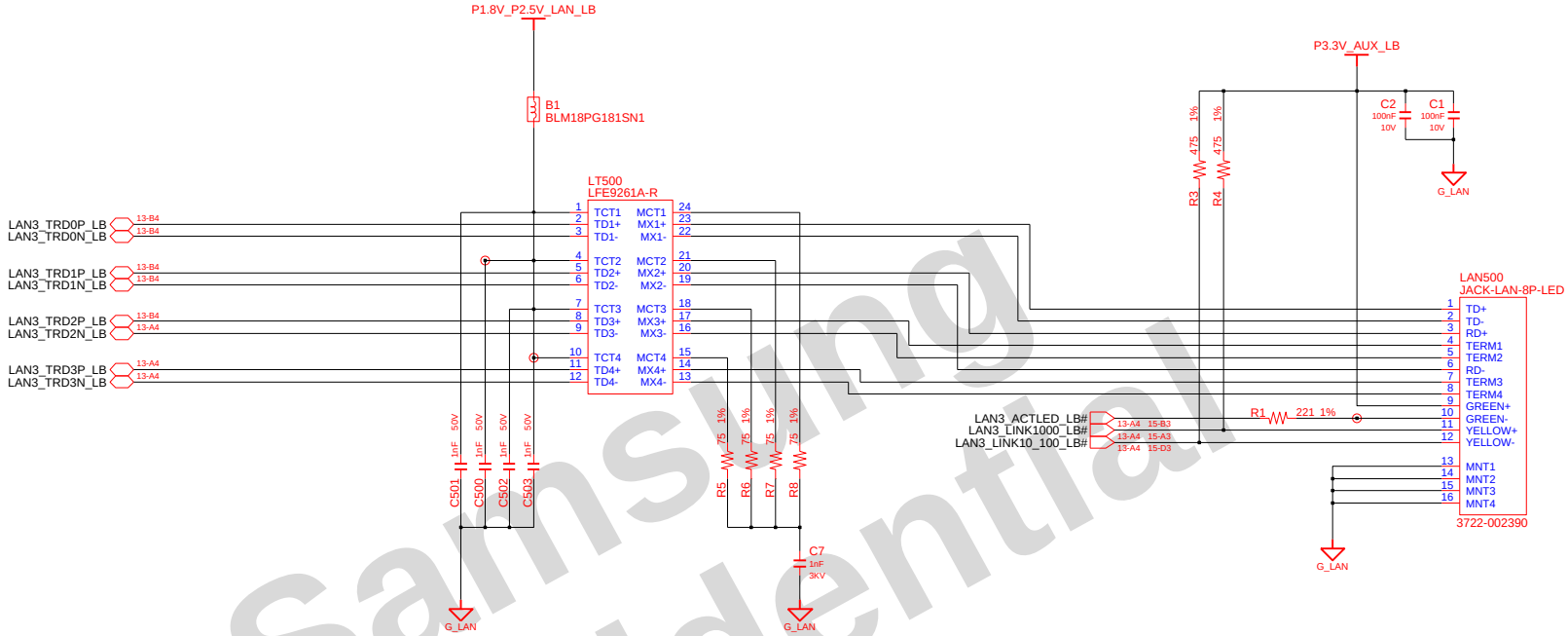
40mil pattern
Apply shield GND for SD/MMC/MS_CLK signal
P3.3V_MCD distance between R5U880 and socket should be less than 2 inches.



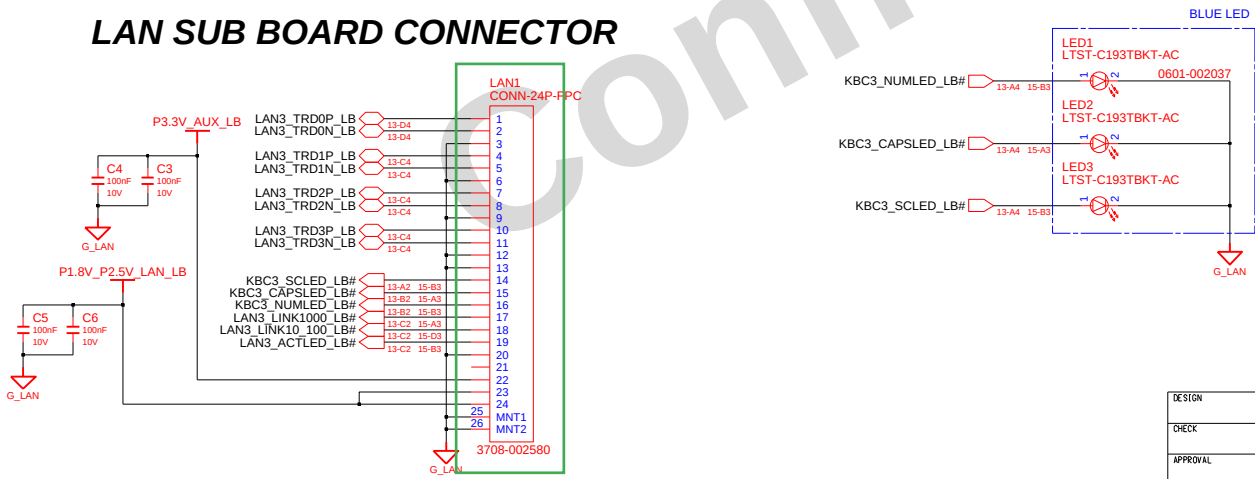
40 mil trace for medica card socket ground

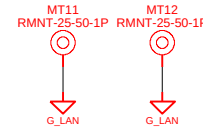
DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB RIGHT CARD READER & 7-IN-1	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS, EUH	REV: 1.1		PART NO.: BA41-#####A
MODULE CODE	LAST EDIT: August 22, 2008 10:42:11 AM	PAGE 12 OF 15	

LAN JACK BOARD



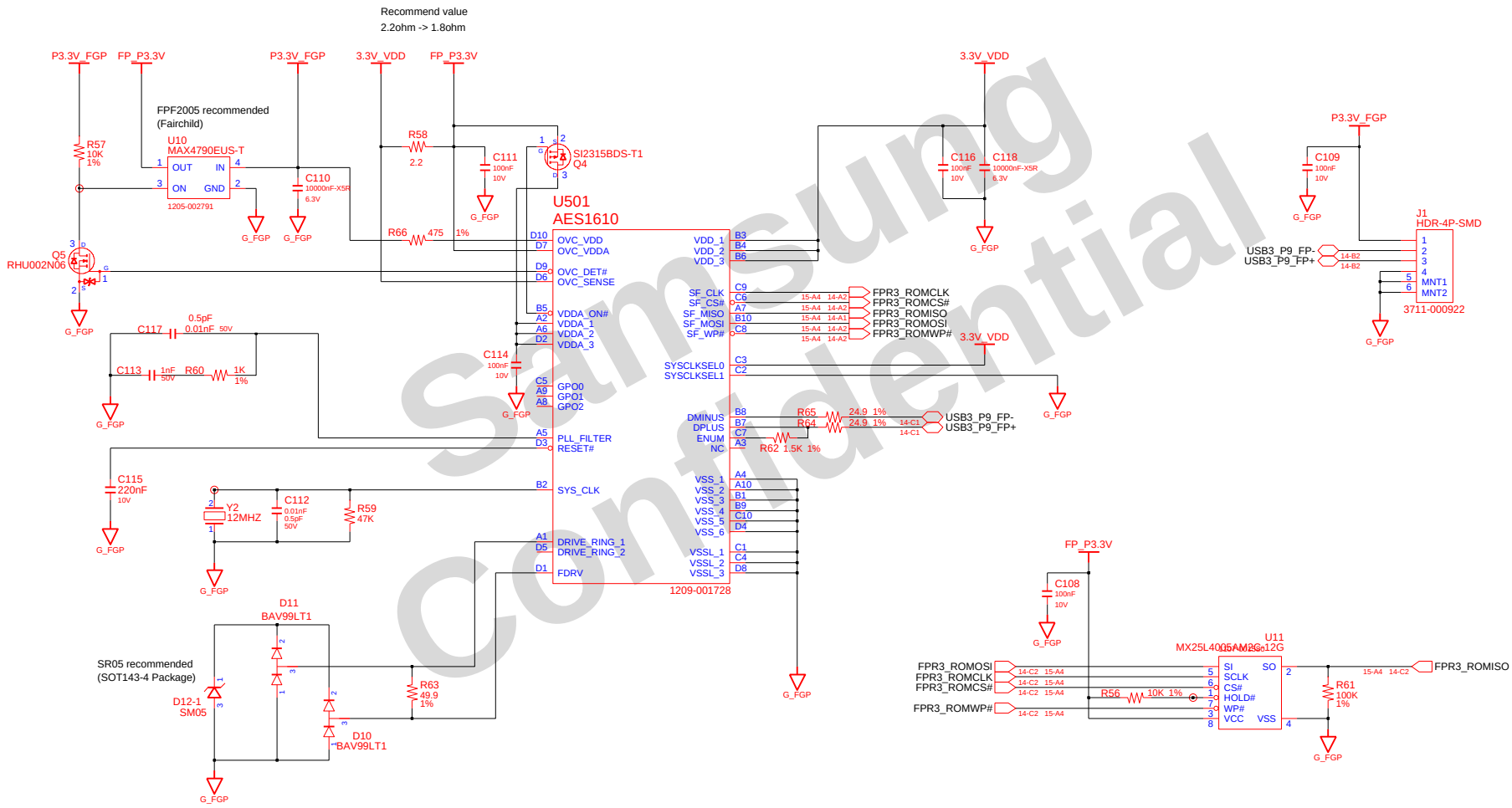
LAN SUB BOARD CONNECTOR





DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB LAN LAN I/F	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS, EUH	REV: 1.1		PART NO.: BA41-######A
MODULE CODE	LAST EDIT: August 22, 2008 10:42:11 AM	PAGE 13 OF 15	

FINGER PRINT BOARD



DESIGN: JUN, PARK	DATE: 1/17/2008	TITLE: SAMOA SUB FINGER PRINT FINGER PRINT I/F	SAMSUNG ELECTRONICS
CHECK: HJ, KIM	DEV. STEP: MP		
APPROVAL: JS, EUH	REV: 1.1		PART NO.: BA41-######A
MODULE CODE	LAST EDIT: August 22, 2008 10:42:11 AM	PAGE 14 OF 15	