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CYGNUS C

CPU : Intel Dothan533 / Yonah(TBD)
Chip Set : Intel Alviso & ICH6-M
Remarks : Mobility Platform

Model Name : CYGNUS C
PBA Name : MAIN
PCB Code : BA41-00451A
Dev. Step : MP
Revision : 1.0
T.R. Date : NOV 29 2004

DRAW	CHECK	APPROVAL

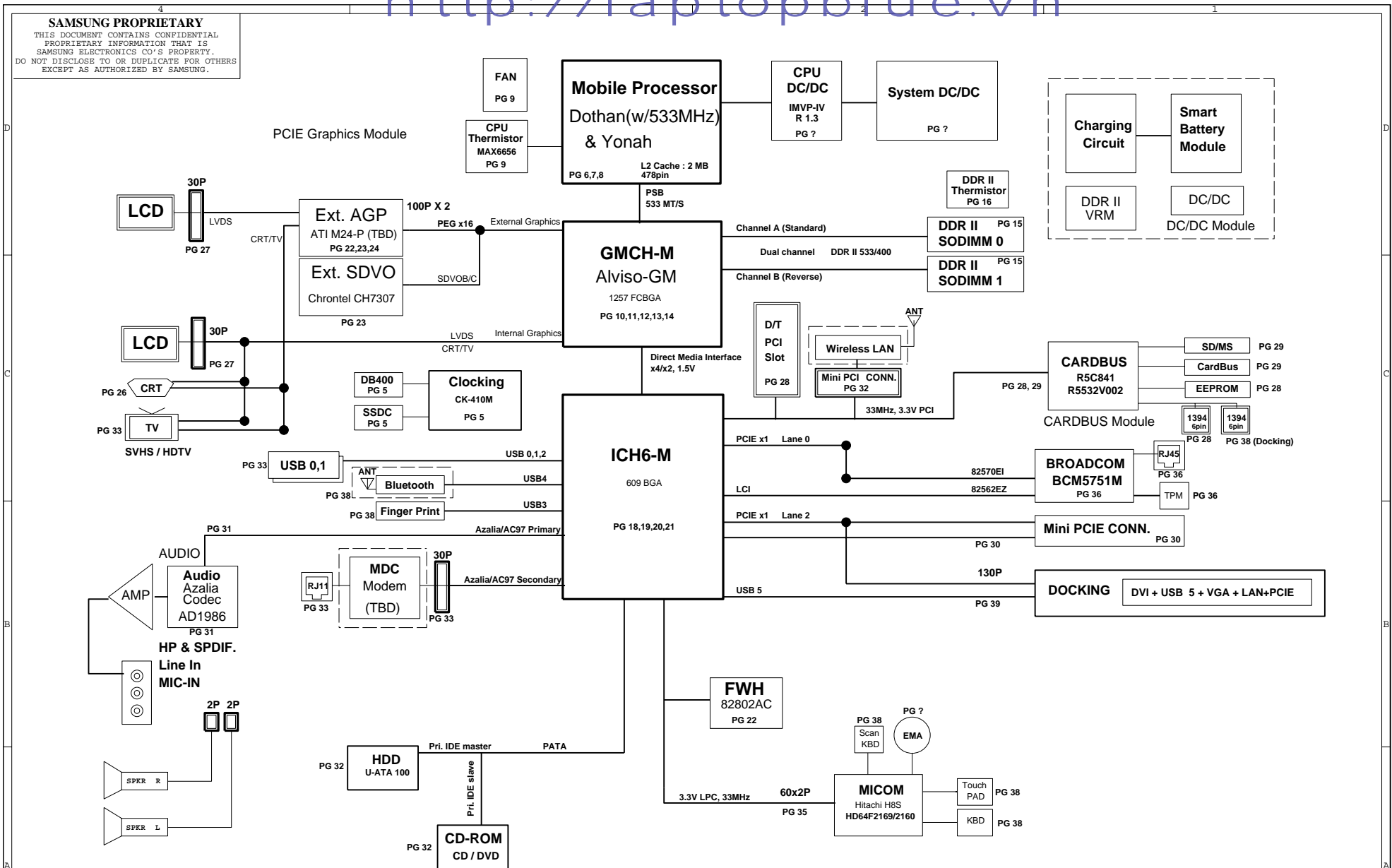
Owner : SEC Mobile R & D Signature : X

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DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG
CHECK	BIN, KK	DEV. STEP	MP			ELECTRONICS
APPROVAL	KIM, DW	REV	1.0		COVER	PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	1 OF 49	

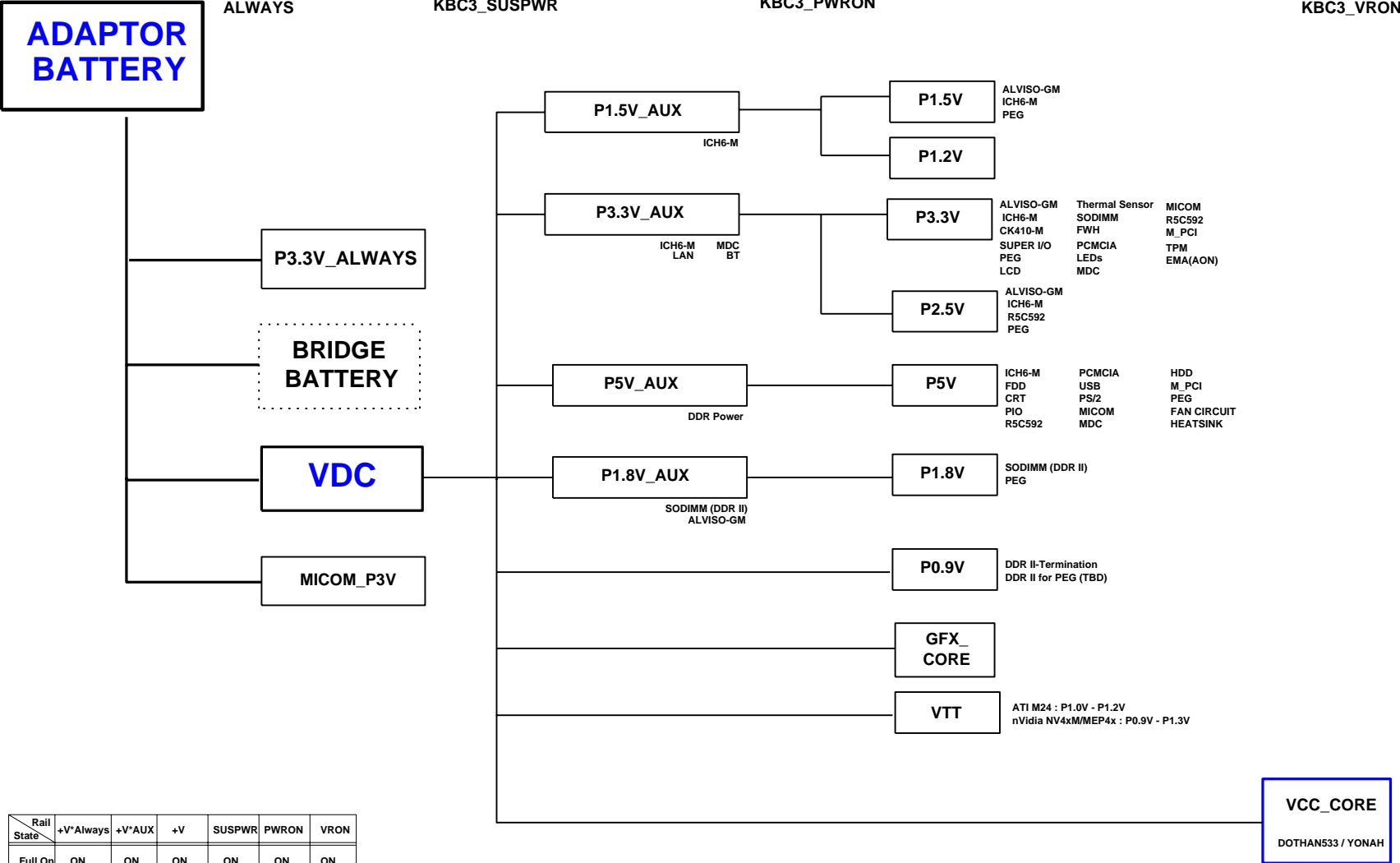
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DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP		MAIN	
APPROVAL	KIM, DW	REV	1.0	OPERATION BLOCK DIAGRAM	PART NO. BA41-00451A	
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	2 OF 49	

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Power Diagram



Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF	OFF
S4	ON	ON	OFF	ON	OFF	OFF
S5	ON	OFF	OFF	OFF	OFF	OFF

DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP			PART NO. BA41-00451A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	3 OF 49	

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	A,B,C
MiniPCI SLOT1 USB	AD21	3	D,E
	AD23	2	USB2.0 #0 : A
	AD29(internal)	-	USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI LPC bridge/IDE/AC97/SMBUS	AD30(internal)	-	-
	AD31(internal)	-	B
Internal MAC AC Link	AD24(internal)	-	A,B
	-	-	E
			B

CPU Core Voltage Table

	V1D5	V1D4	V1D3	V1D2	V1D1	V1D0	Voltage	V1D5	V1D4	V1D3	V1D2	V1D1	V1D0	Voltage	
	0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V	Northwood-B
	0	0	0	0	0	1	1.692 V	1	0	0	0	0	0	1.180 V	(Interposer B'd)
	0	0	1	1	0	0	1.676 V	1	0	0	0	0	0	1.164 V	
	0	0	0	0	1	1	1.660 V	1	0	0	0	1	1	1.148 V	
	0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V	
	0	0	1	0	0	0	1.628 V	1	0	0	1	0	0	1.116 V	
	0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V	
	0	0	0	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V	
	0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V	
	0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V	
	0	0	1	0	0	0	1.548 V	1	0	1	0	0	0	1.036 V	
	0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V	
	0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V	
	0	0	1	1	0	0	1.500 V	1	0	1	1	0	1	0.988 V	
	0	0	1	1	1	0	1.484 V	1	0	1	1	0	0	0.972 V	
	0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V	
	0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V	
	0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V	
	0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V	
	0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V	
	0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V	
	0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V	
Highest Freq.	0	1	0	1	1	0	1.356 V	1	1	0	1	1	0	0.844 V	
	0	1	0	1	1	1	1.340 V	1	1	0	1	1	1	0.828 V	Lowest Freq.
	0	1	1	0	0	0	1.324 V	1	1	1	0	0	0	0.812 V	
	0	1	1	0	0	1	1.308 V	1	1	1	0	0	1	0.796 V	
	0	1	1	1	0	0	1.292 V	1	1	1	0	0	0	0.780 V	
	0	1	1	1	0	1	1.276 V	1	1	1	0	1	0	0.764 V	
	0	1	1	1	1	0	1.260 V	1	1	1	1	0	0	0.748 V	Deeper Sleep
	0	1	1	1	1	0	1.244 V	1	1	1	1	0	1	0.732 V	
	0	1	1	1	1	1	1.228 V	1	1	1	1	1	0	0.716 V	
	0	1	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V	

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308-1.068V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V)
	MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)

2 I C / SMB Address

Devices	Address	Hex	Bus
ICH6	Master	-	SMBUS Master
EM6CBN300(CPU Thermal Sensor)	1001 110x	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	
SODIMM1	1010 001x	A2h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable


USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1,2	SYSTEM PORT B
3	BLUETOOTH
4	FINGER PRINT
	OPTION OPTION

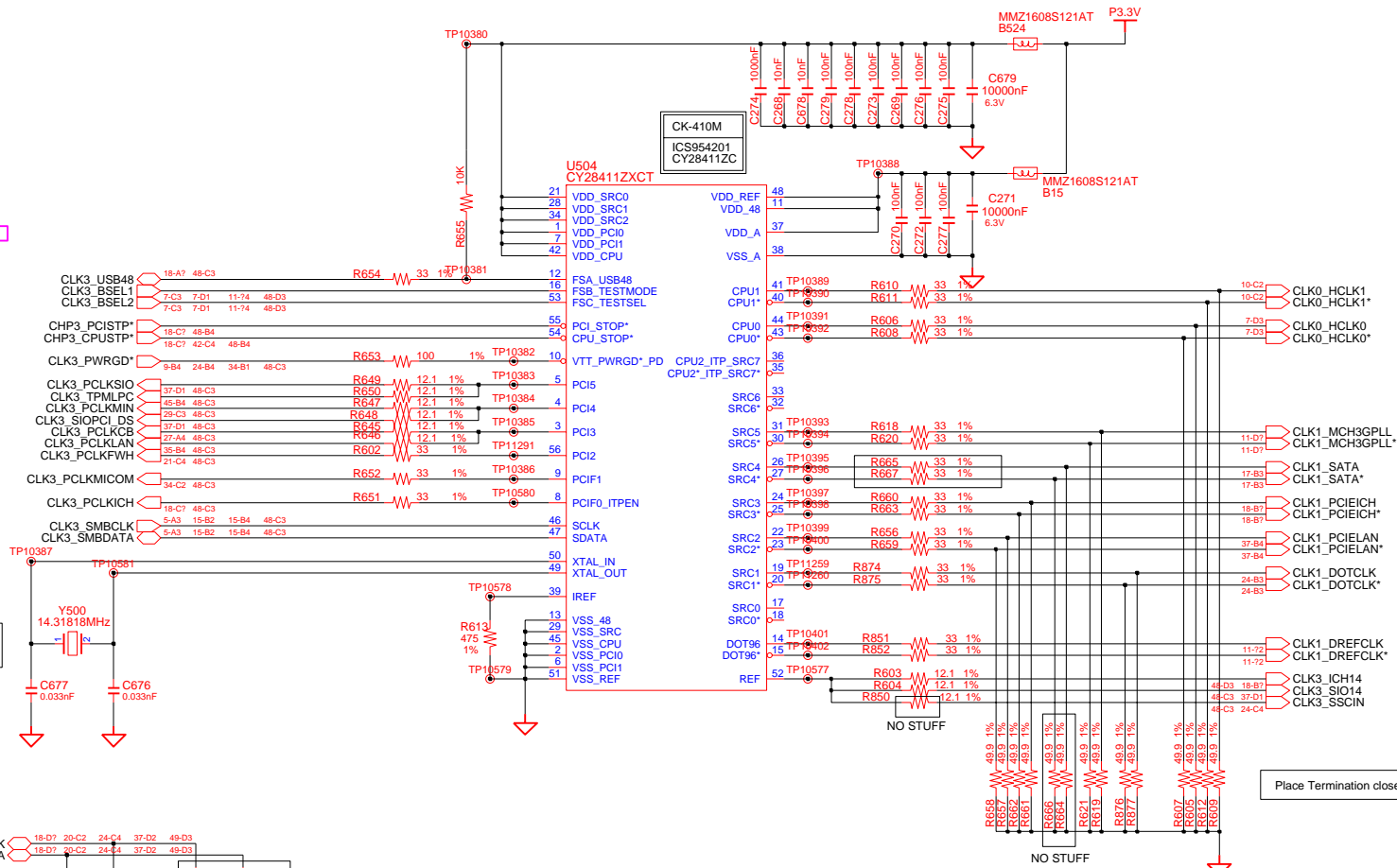
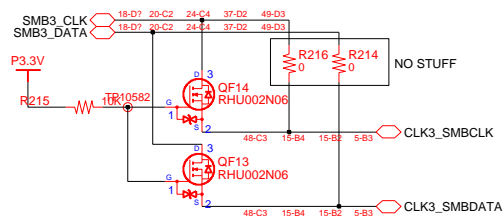
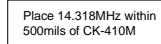
System Power States

CHP3_SLP51*	S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768kHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
CHP3_SLP3*	S3, Suspend-to-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
CHP3_SLP4*	S4, Suspend-to-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
CHP3_SLP5*	S5, Deep Sleep : The system appears same as S3, but may have different wake events.
CHP3_SLP5*	S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

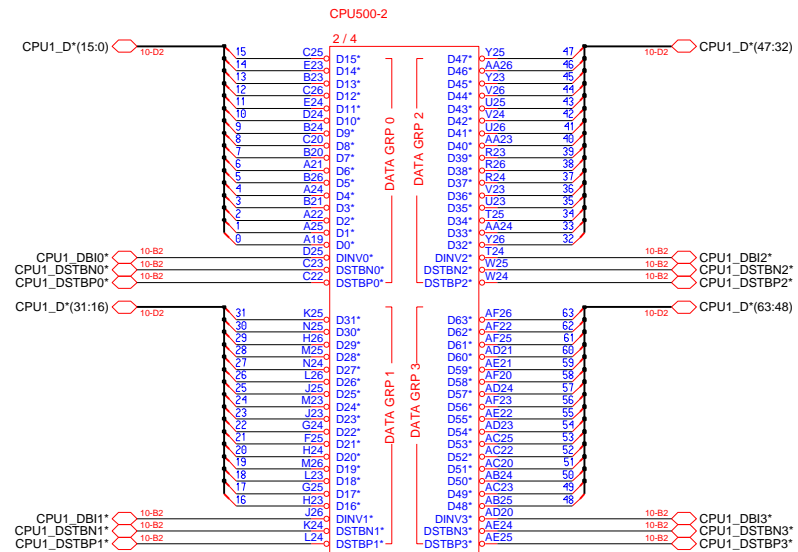
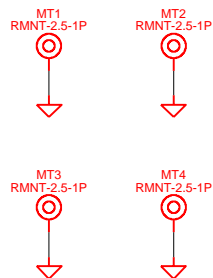
See rev notes in the changes file for more information.

DRAW		DATE	TITLE		
IM, KI		11/29/2004	CYGNUS C		
CHECK	BIN, KK	DEV. STEP	MAIN		
APPROVAL	KIM, DW	REV	BOARD INFORMATION		
		1.0			PART NO.
					BA41-00451A
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FSA BSEL2	FSB BSEL1	FSC BSEL0	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

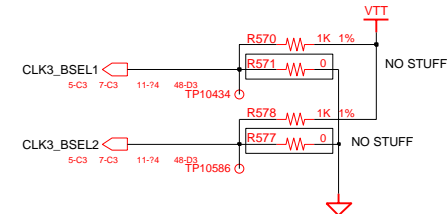
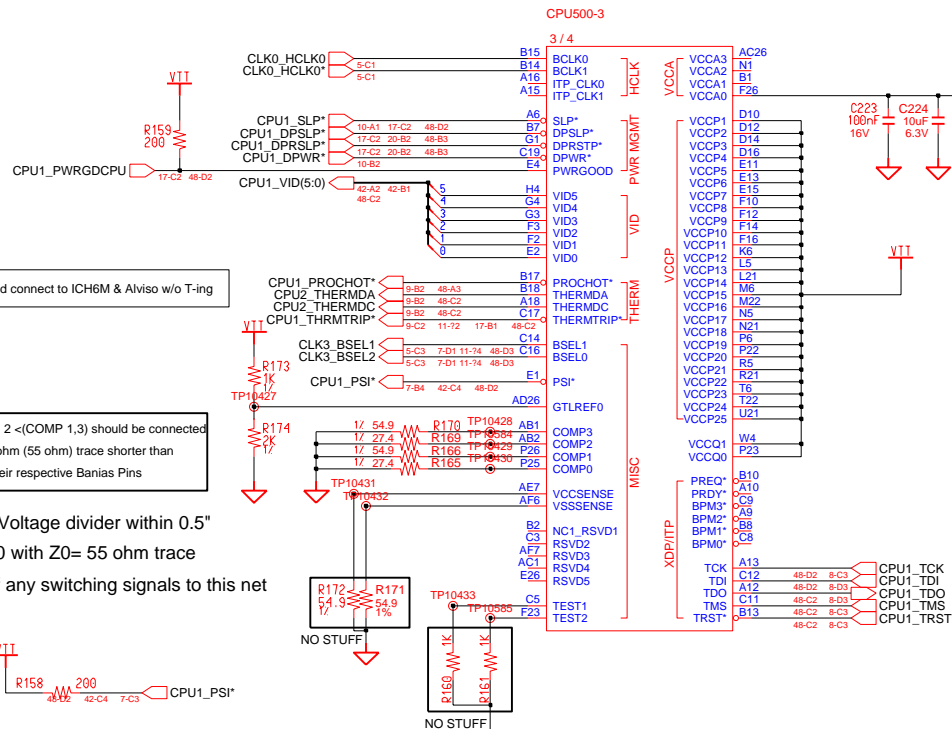


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CHECK		BIN, KK	DEV. STEP	MP					
APPROVAL		KIM, DW	REV	1.0					
MODULE CODE		LAST EDIT			November 29, 2004 10:05:41 AM				
								PART NO. BA41-00451A	



DRAW		IM, K1	DATE	11/29/2004		TITLE		CYGNUS C		SAMSUNG ELECTRONICS	
CHECK		BJN, KK	DEV. STEP	MP		MAIN					
APPROVAL		KIM, DW	REV	1.0		DOTHAN CPU (1/3)					
MODULE CODE		LAST EDIT		November 29, 2004 10:05:41 AM				PAGE	6	OF	49

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CPU Core Voltage Table

VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0 0	1.708 V	1 0 0 0 0 0	1.196 V
0 0 0 0 0 1	1.692 V	1 0 0 0 0 1	1.180 V
0 0 0 0 1 0	1.676 V	1 0 0 0 1 0	1.164 V
0 0 0 0 1 1	1.660 V	1 0 0 0 1 1	1.148 V
0 0 0 1 0 0	1.644 V	1 0 0 1 0 0	1.132 V
0 0 0 1 0 1	1.628 V	1 0 0 1 0 1	1.116 V
0 0 0 1 1 0	1.612 V	1 0 0 1 1 0	1.100 V
0 0 0 1 1 1	1.596 V	1 0 0 1 1 1	1.084 V
0 0 1 0 0 0	1.580 V	1 0 1 0 0 0	1.068 V
0 0 1 0 0 1	1.564 V	1 0 1 0 0 1	1.052 V
0 0 1 0 1 0	1.548 V	1 0 1 0 1 0	1.036 V
0 0 1 0 1 1	1.532 V	1 0 1 0 1 1	1.020 V
0 0 1 1 0 0	1.516 V	1 0 1 1 0 0	1.004 V
0 0 1 1 0 1	1.500 V	1 0 1 1 0 1	0.988 V
0 0 1 1 1 0	1.484 V	1 0 1 1 1 0	0.972 V
0 0 1 1 1 1	1.468 V	1 0 1 1 1 1	0.956 V
0 1 0 0 0 0	1.452 V	1 1 0 0 0 0	0.940 V
0 1 0 0 0 1	1.436 V	1 1 0 0 0 1	0.924 V
0 1 0 0 1 0	1.420 V	1 1 0 0 1 0	0.908 V
0 1 0 0 1 1	1.404 V	1 1 0 0 1 1	0.892 V
0 1 0 1 0 0	1.388 V	1 1 0 1 0 0	0.876 V
0 1 0 1 0 1	1.372 V	1 1 0 1 0 1	0.860 V
0 1 0 1 1 0	1.356 V	1 1 0 1 1 0	0.844 V
0 1 0 1 1 1	1.340 V	1 1 0 1 1 1	0.828 V
0 1 1 0 0 0	1.324 V	1 1 1 0 0 0	0.812 V
0 1 1 0 0 1	1.308 V	1 1 1 0 0 1	0.796 V
0 1 1 0 1 0	1.292 V	1 1 1 0 1 0	0.780 V
0 1 1 0 1 1	1.276 V	1 1 1 0 1 1	0.764 V
0 1 1 1 0 0	1.260 V	1 1 1 1 0 0	0.748 V
0 1 1 1 0 1	1.244 V	1 1 1 1 0 1	0.732 V
0 1 1 1 1 0	1.228 V	1 1 1 1 1 0	0.716 V
0 1 1 1 1 1	1.212 V	1 1 1 1 1 1	0.700 V

Highest Freq. of Dothan400(1.8GHz)
* Highest Freq. of Dothan533(?? GHz : TBD)

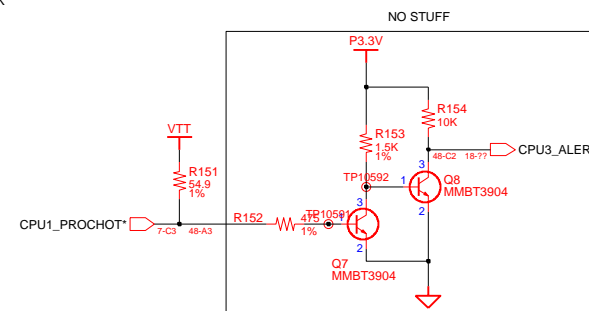
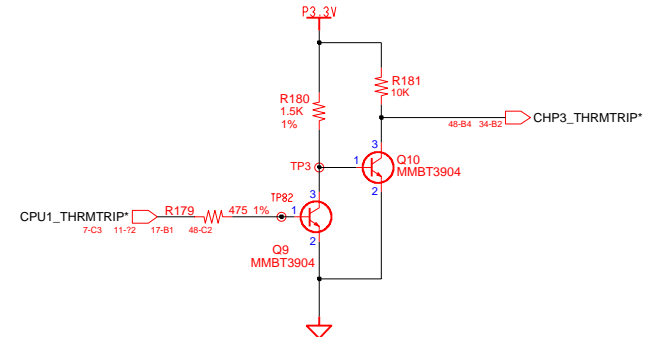
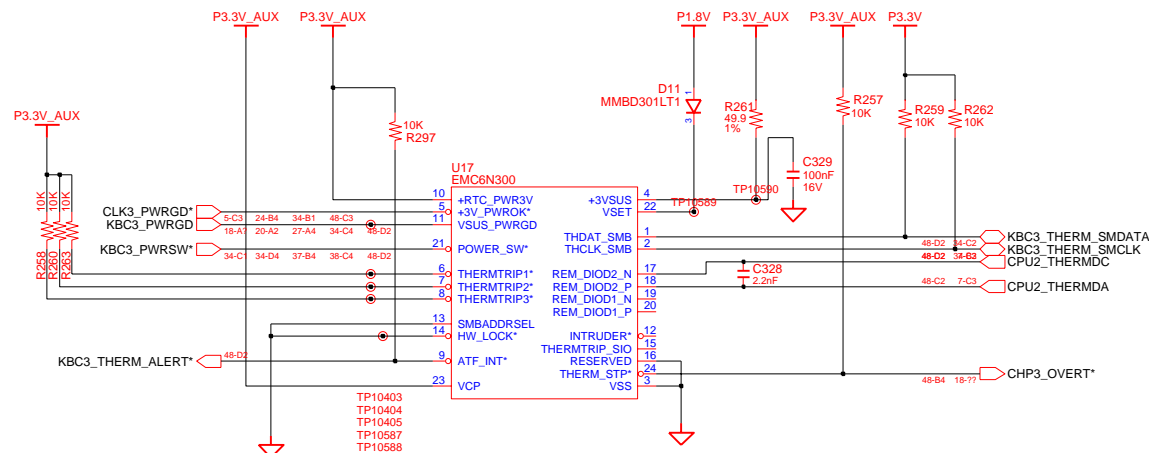
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CHECK	BIN, KK	DEV. STEP	MP		MAIN	
APPROVAL	KIM, DW	REV	1.0		DOTHAN CPU(2/3)	PART NO.
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM			BA41-00451A
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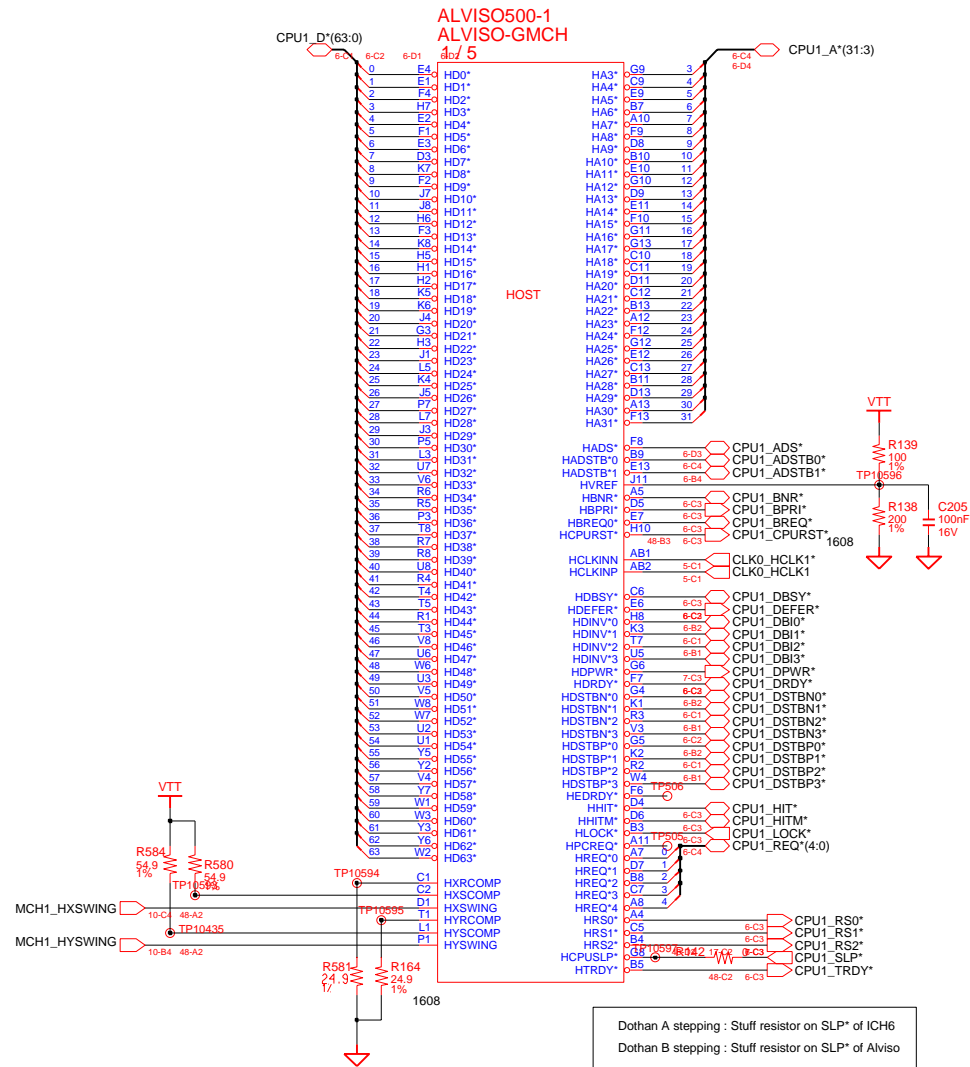
Refer To Thermal Sensor Layout Guidelines.

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND

CPU / DDR Thermal Sensor

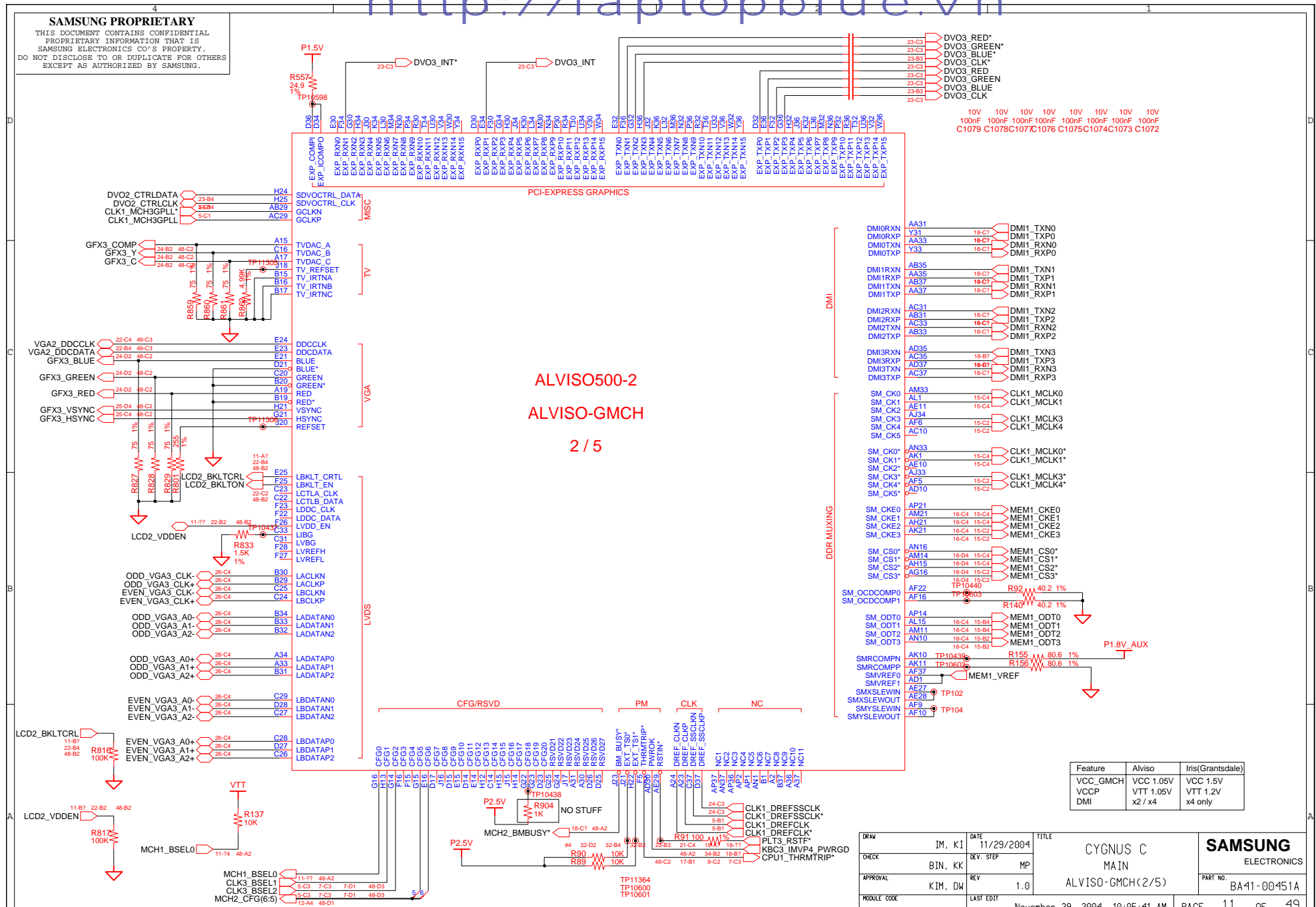


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CHECK	BIN, KK	DEV. STEP	MP		MAIN	
APPROVAL	KIM, DW	REV	1.0	THERMAL SENSOR/FAN CONTRL	PART NO.	BA41-00451A
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	9	OF 49



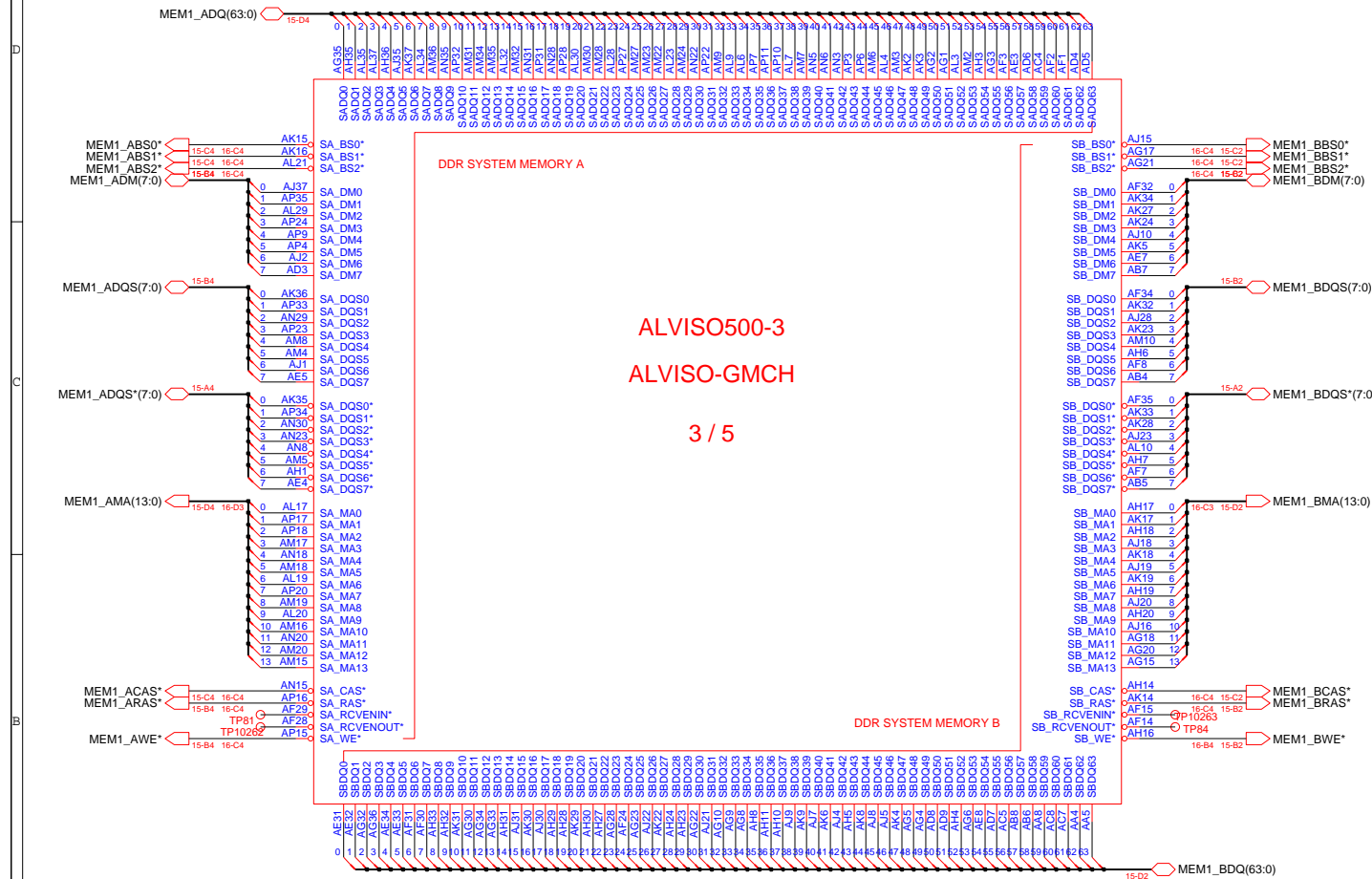
Dothan A stepping : Stuff resistor on SLP* of ICH6
Dothan B stepping : Stuff resistor on SLP* of Alviso

DRAM	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAIN ALVISO-GMCH(1/5)	SAMSUNG ELECTRONICS PART NO. BA1A-00451A
CHECK	BIN, KK	DEV. STEP	MP			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE	LAST EDIT		November 29, 2004 10:05:41 AM			



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DDR-II ONLY	DDR-I
SA_DQS(7:0)*	NC
SB_DQS(7:0)*	NC
SM_ODT(3:0)	NC

Dual Channel	Ch. A (So-DIMM A)	Ch. B (So-DIMM B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)*	SA_CS(1:0)*	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)*	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVO_RED	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN	EXP_TXP_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE	EXP_TXP_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOC_ALPHA*	
SDVOC_RED	EXP_TXP_4
SDVOC_ALPHA	
SDVOC_GREEN*	EXP_TXN_5
SDVOC_GREEN	EXP_TXP_5
SDVOC_BLUE*	EXP_TXN_6
SDVOC_BLUE	EXP_TXP_6
SDVOC_CLK*	EXP_TXN_7
SDVOC_CLK	EXP_TXP_7
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

def. : default Option

CFG#	Low	High
CFG(5)	DMix2	DMix4 (def.)
CFG(6)	DDR-2	DDR-1
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(10)	TBD	TBD
CFG(11)	TBD	TBD
CFG(16)	Dynamic ODT Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	VTT 1.05V (def.)	VTT 1.2V
SDVODTA	No (def.)	SDVO Present

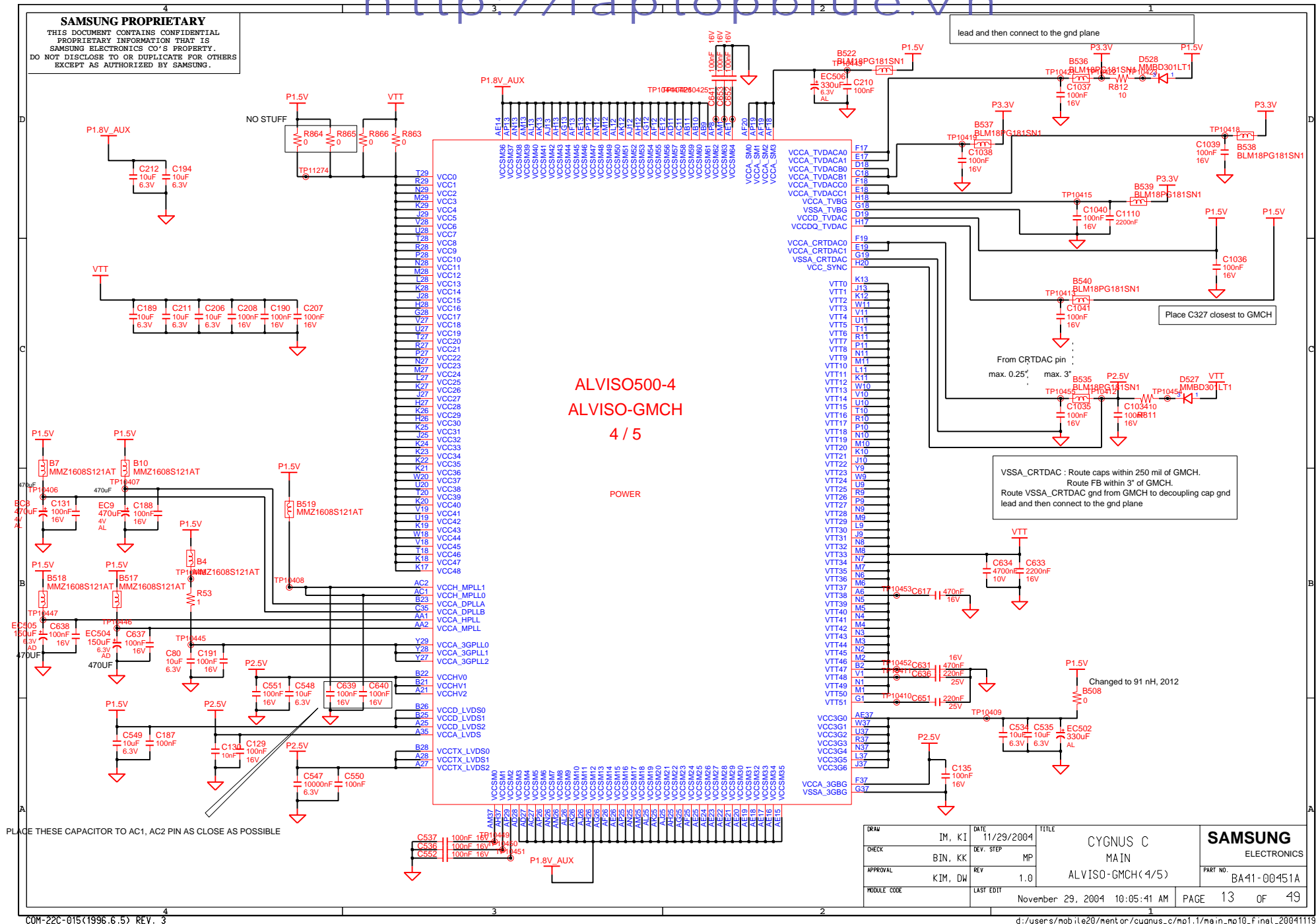
NO STUFF

MCH2_CFG(5) R136 11-74 48-01 1K 1%

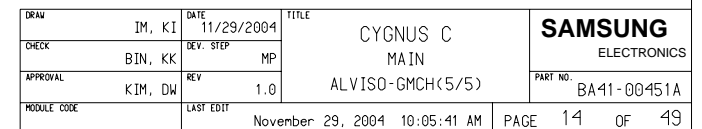
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DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP		MAIN	
APPROVAL	KIM, DW	REV	1.0		ALVISO-GMCH(3/5)	PART NO.
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				November 29, 2004 10:05:41 AM	PAGE	12 OF 49

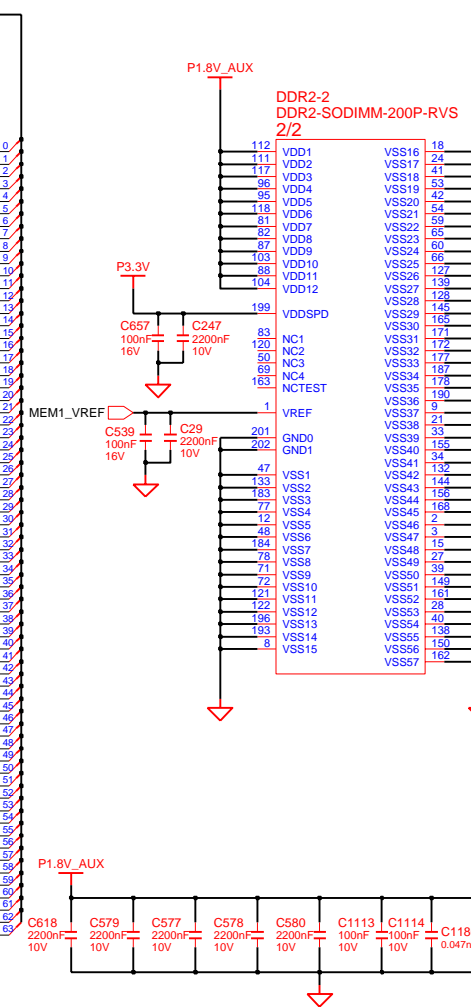
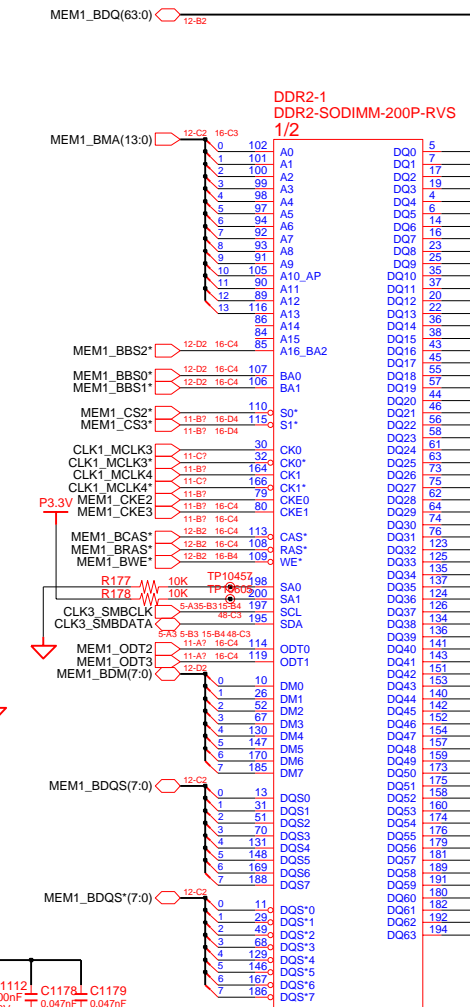
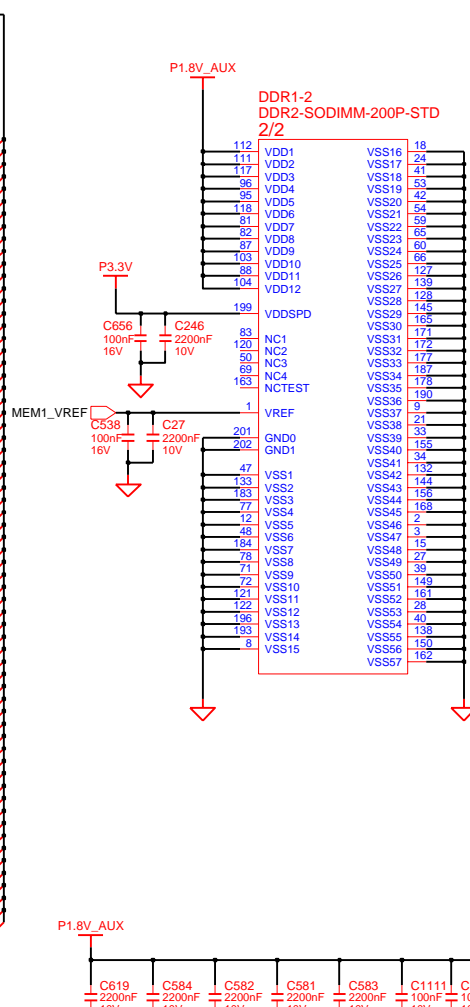
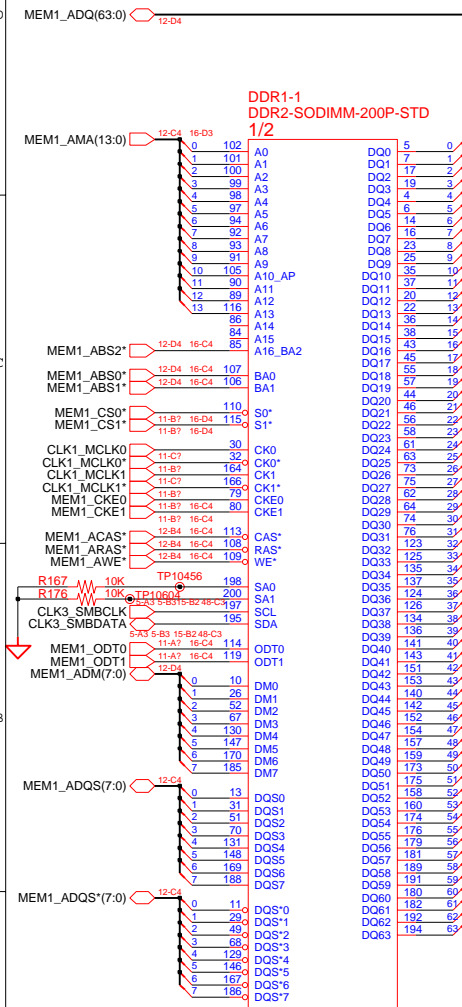
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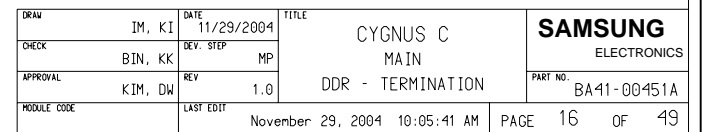
DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAIN ALVISO-GMCH(4/5)	SAMSUNG ELECTRONICS PART NO. BA41-00451A PAGE 13 OF 49
CHECK	BIN, KK	DEV. STEP	MP			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM			



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DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS PART NO. BA41-00451A
CHECK	BIN, KK	DEV. STEP	MP		MAIN	
APPROVAL	KIM, DW	REV	1.0		DDR - SODIMM	
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	15 OF 49	



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CPUSLP*
Dothan A stepping : Stuff resistor on SLP* of ICH6 Dothan B stepping ~ : Stuff resistor on SLP* of Alviso
DPRSLP*
Dothan A stepping : No Stuff Dothan B stepping ~ : Stuff

Enable intergated P1.5V_AUX VRM

U507-1
82801FBM
1/5

NO STUFF

PRTC_BAT

NO STUFF

TP10467

TP10468

TP10469

TP10470

TP10471

TP10472

TP10473

TP10474

TP10475

TP10476

TP10477

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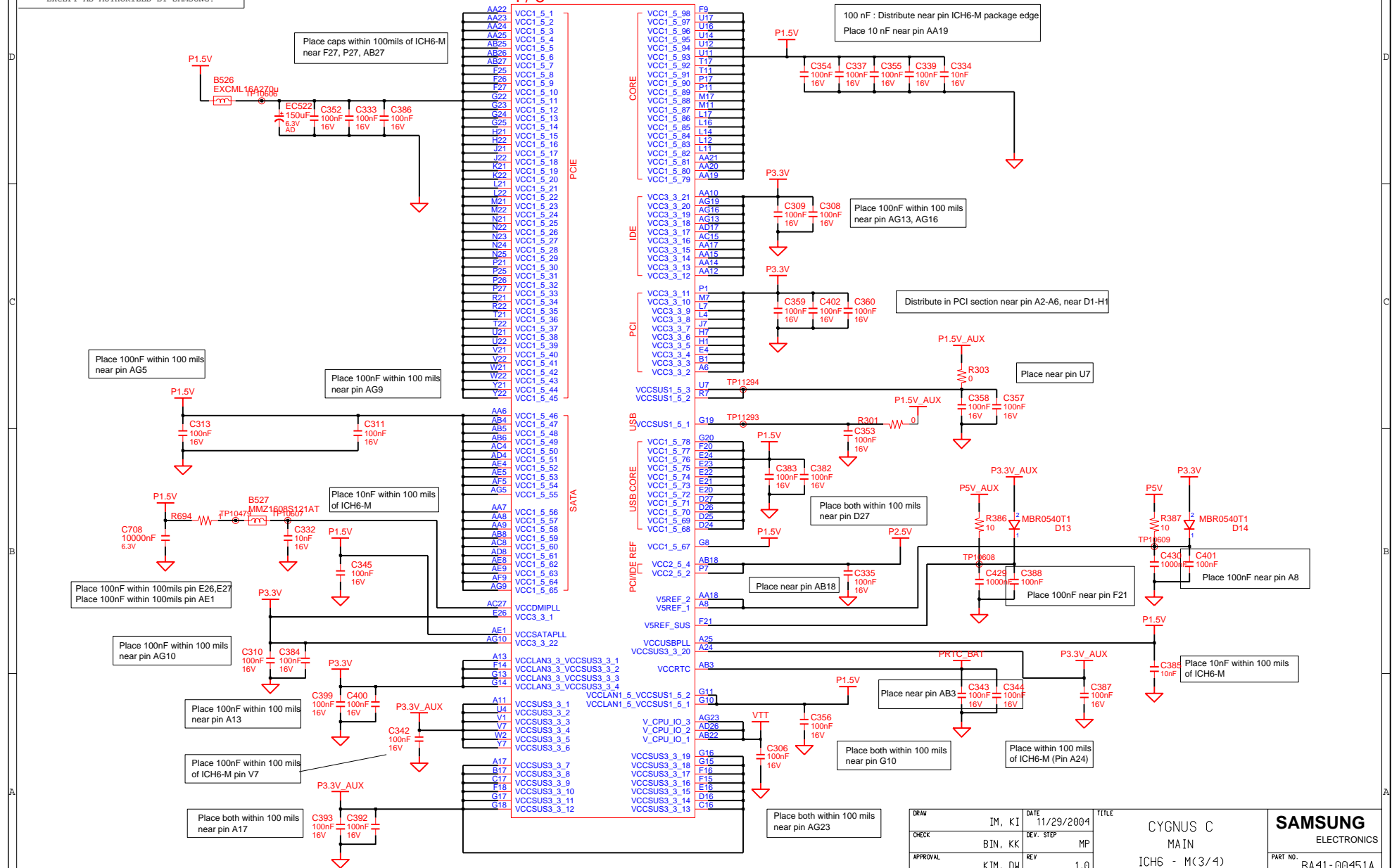
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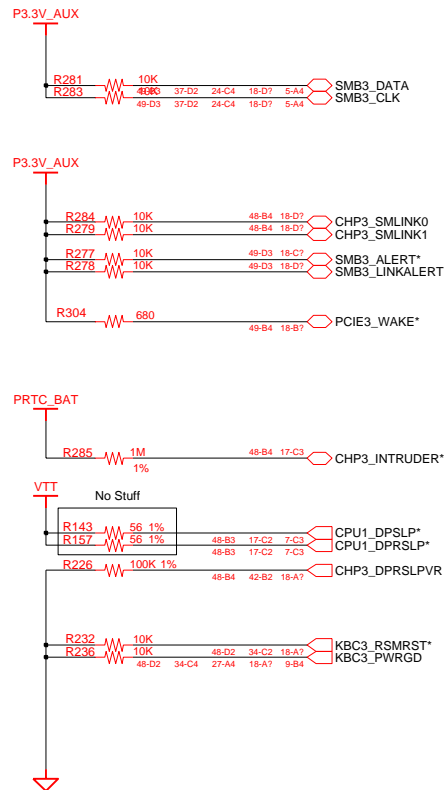
U507-4
82801FBM
4 / 5



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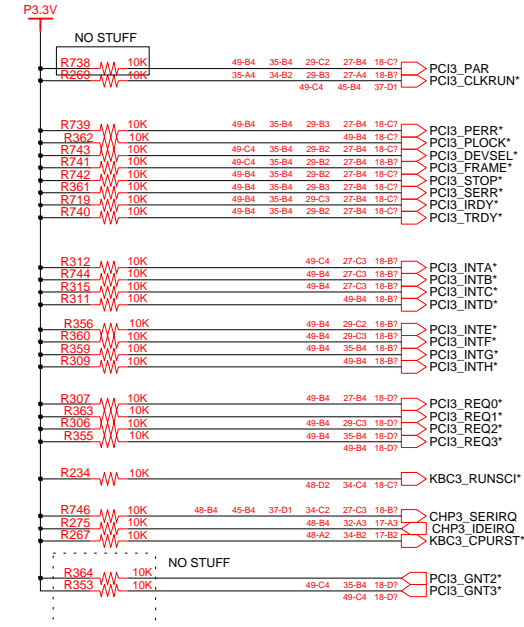
U507-5
82801FBM
5 / 5

AG22	VSS_172	VSS_86	P22
AG20	VSS_171	VSS_85	P16
AG17	VSS_170	VSS_84	P15
AG14	VSS_169	VSS_83	P14
AG12	VSS_168	VSS_82	P13
AG7	VSS_167	VSS_81	P12
AG3	VSS_166	VSS_80	N17
AG1	VSS_165	VSS_79	N16
AF26	VSS_164	VSS_78	N15
AF12	VSS_163	VSS_77	N14
AF10	VSS_162	VSS_76	N13
AF7	VSS_161	VSS_75	N12
AF3	VSS_160	VSS_74	N11
AF1	VSS_159	VSS_73	N7
AE25	VSS_158	VSS_72	N1
AE21	VSS_157	VSS_71	M27
AE11	VSS_156	VSS_70	M26
AE10	VSS_155	VSS_69	M23
AE7	VSS_154	VSS_68	M15
AE6	VSS_153	VSS_67	M13
AE2	VSS_152	VSS_66	M12
AD24	VSS_151	VSS_65	M11
AD18	VSS_150	VSS_64	M4
AD15	VSS_149	VSS_63	L25
AD10	VSS_148	VSS_62	L24
AD6	VSS_147	VSS_61	L23
AD2	VSS_146	VSS_60	L15
AD1	VSS_145	VSS_59	L13
AC24	VSS_144	VSS_58	K27
AC23	VSS_143	VSS_57	K26
AC22	VSS_142	VSS_56	K23
AC12	VSS_141	VSS_55	K7
AC10	VSS_140	VSS_54	K1
AC6	VSS_139	VSS_53	J25
AC3	VSS_138	VSS_52	J23
AB9	VSS_137	VSS_51	J4
AB10	VSS_136	VSS_50	H27
AB9	VSS_135	VSS_49	H23
AB7	VSS_134	VSS_48	G12
AB2	VSS_133	VSS_47	G11
AB1	VSS_132	VSS_46	G9
AA16	VSS_131	VSS_45	G7
AA13	VSS_130	VSS_44	G1
AA11	VSS_129	VSS_43	F22
AA4	VSS_128	VSS_42	F19
Y27	VSS_127	VSS_41	F17
Y26	VSS_126	VSS_40	F4
Y23	VSS_125	VSS_39	E27
Y6	VSS_124	VSS_38	E25
W25	VSS_123	VSS_37	E13
W24	VSS_122	VSS_36	E12
W23	VSS_121	VSS_35	E11
W1	VSS_120	VSS_34	E14
W7	VSS_119	VSS_33	D22
V27	VSS_118	VSS_32	D19
V26	VSS_117	VSS_31	D18
V23	VSS_116	VSS_30	D14
V4	VSS_115	VSS_29	D13
U25	VSS_114	VSS_28	D10
U24	VSS_113	VSS_27	D7
U23	VSS_112	VSS_26	D1
U13	VSS_111	VSS_25	C22
U15	VSS_110	VSS_24	C20
U11	VSS_109	VSS_23	C12
T27	VSS_108	VSS_22	C14
T26	VSS_107	VSS_21	C4
T23	VSS_106	VSS_20	B25
T16	VSS_105	VSS_19	B24
T15	VSS_104	VSS_18	B23
T14	VSS_103	VSS_17	B21
T13	VSS_102	VSS_16	B19
T12	VSS_101	VSS_15	B15
T7	VSS_100	VSS_14	B13
T1	VSS_99	VSS_13	A26
R25	VSS_98	VSS_12	A23
R24	VSS_97	VSS_11	A21
R23	VSS_96	VSS_10	A19
R17	VSS_95	VSS_9	A15
R16	VSS_94	VSS_8	A12
R15	VSS_93	VSS_7	A9
R14	VSS_92	VSS_6	A7
R13	VSS_91	VSS_5	A4
R12	VSS_90	VSS_4	A1
R11	VSS_89	VSS_3	
R4	VSS_88	VSS_2	
	VSS_87	VSS_1	



ICH6-m Strapping Options

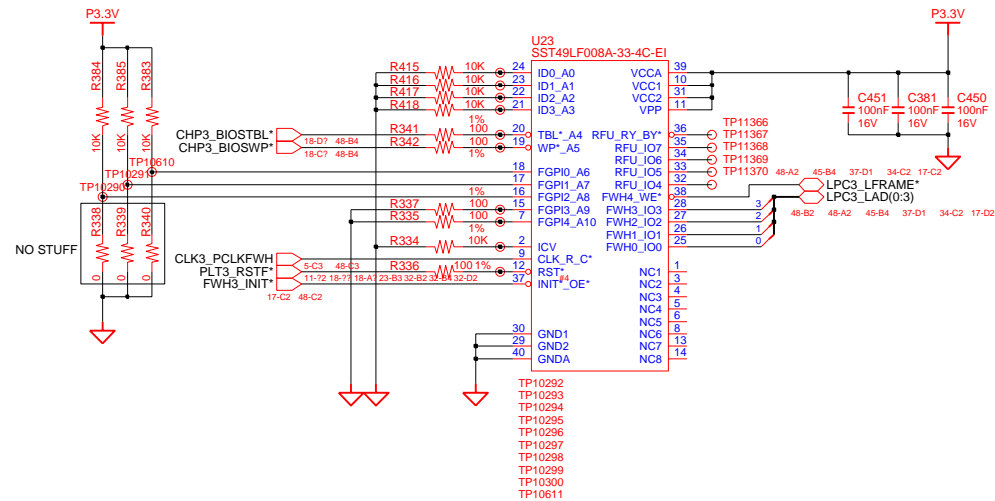
	Function	Default
CHP3_SPKR	No Reboot	No Stuff
CHP3_BIOSWP*	Boot BIOS	No Stuff
PC/PCI GNTA*	A16 swap override	No Stuff
AC97_SDOUT	Safe Mode	TBD
EEP_DOUT		TBD



DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP		MAIN	
APPROVAL	KIM, DW	REV	1.0		ICH6 - M(4/4)	PART NO.
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM			BA41-00451A
				PAGE	20	OF 49

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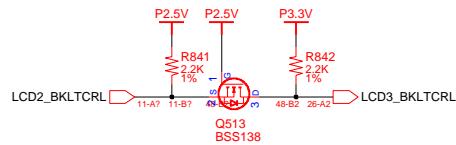
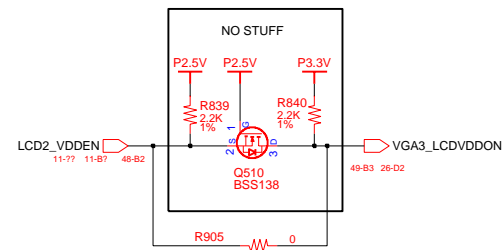
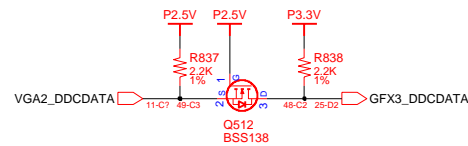
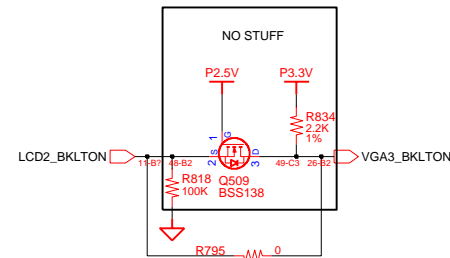
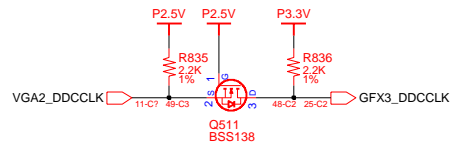


- | | | | |
|----|---|----|---------------------------------|
| 02 | VERIFY REAL MODE | 66 | CONFIGURE ADVANCE CACHE REG. |
| 03 | DISABLE NMI | 6A | DISPLAY EXTERNAL CACHE SIZE |
| 04 | GET CPU TYPE | 6C | DISPLAY SHADOW MESSAGE |
| 06 | INIT. SYSTEM H/W | 6E | DISPLAY NON-DISPOSABLE SEGMENT |
| 08 | INIT. CHIPSET REG. | 70 | DISPLAY ERROR MESSAGE |
| 09 | SET IN POST FLAG | 72 | CHECK FOR CONFIGURATION ERROR |
| 0A | INIT CPU.REG | 74 | TEST REAL-TIME CLOCK |
| 0B | CPU CACHE ON | 76 | CHECK FOR KEYBOARD ERROR |
| 0C | INIT.CACHE TO POST | 7C | SETUP HARDWARE INTERRUPT VECTOR |
| OE | INIT. I/O VALUE | 7E | TEST COPROCESSOR IF PRESENT |
| 0F | ENABLE THE L-BUS IDE | 80 | DISABLE ON-BOARD I/O PORT |
| 10 | INIT. POWER MANAGER | 82 | DETECT AND INSTALL EXT.RS232C |
| 11 | LOAD ALTERNATE REG. | 84 | DETECT AND INSTALL EXT.PARALLEL |
| 13 | PCI BUS MASTER RESET
WITH INITIAL POST VALUE | 86 | RE-INIT. ON-BOARD I/O PORT |
| 14 | INIT. KEYBOARD CONTROLLER | 88 | INIT. BIOS DATA ROM |
| 16 | CHECK CHECKSUM | 8A | INIT.EXTENDED BIOS DATA AREA |
| 18 | 8254 TIMER INIT. | 8C | INIT. FDD CONTROLLER |
| 1A | 8237 DMA CONTROLLER INIT. | 9A | SHADOW OPTION ROMS |
| 1C | RESET INTERRUPT CONTROLLER | 9C | SETUP POWER MANAGEMENT |
| 20 | TEST DRAM REFRESH | 9E | ENABLE H/W INTERRUPT |
| 22 | TEST 8742 KEYBOARD CONTROLLER | A0 | SET TIME OF DAY |
| 24 | SET ES SEGMENT REG. TO 4GB | A4 | INIT. TYPOMATIC RATE |
| 26 | ENABLE A20 | A8 | ERASE F2 PROMPT |
| 28 | AUTO SIZING DRAM | AA | SCAN FOR F2 KEY STROKE |
| 32 | COMPUTE THE CPU SPEED | AC | ENTER SETUP |
| 34 | TESET CMOS RAM | AE | CLEAR IN POST FLAG |
| 38 | SHADOW SYSTEM BIOS ROM | B0 | CHECK FOR ERRORS |
| 3A | AUTO SIZING CACHE | B2 | POST DONE-PREPARE TO BOOT O/S |
| 3C | CONFIGURE ADVANCED CHIPSET REG. | B4 | ONE BEEP |
| 3D | LOAD ALTER REG. WITH CMOS VALUE | B6 | CHECK PASSWORD (OPTION) |
| 42 | INIT. INTERRUPT VECTOR | B7 | ACPI INIT |
| 44 | INIT. BIOS INTERRUPT | BA | DMI INIT |
| 46 | CHECK ROM COPYRIGHT NOTICE | BE | CLEAR SCREEN |
| 47 | INIT. I20 SUPPORT IF INSTALLED | C0 | TRY BOOT WITH INT19 |
| 48 | CHECK VIDEO CONFIGURE AGAINST CMOS | D0 | INTERRUPT HANDLER ERROR |
| 49 | INIT. PCI BUS AND DEVICE | D2 | UNKNOWN INTERRUPT ERROR |
| 4A | INIT. ALL VIDEO BIOS ROM | D4 | PENDING INTERRUPT ERROR |
| 4C | SHADOW VIDEO BIOS ROM | D6 | SHUTDOWN 5 |
| 50 | DISPLAY CPU TYPE AND SPEED | D8 | SHUTDOWN ERROR |
| 52 | TEST KEYBOARD | DA | EXTENDED BLOCK MOVE |
| 54 | SET KEYCLICK IF ENABLED | DC | SHUTDOWN 10 |
| 56 | ENABLE KEYBOARD | 89 | ENABLE NMI |
| 58 | TEST FOR UNEXPECTED INTERRUPTS | 90 | INIT. HDD CONTROLLER |
| 5A | DISPLAY "PRESS SETUP" | 91 | INIT. LOCAL BUS HDD CONTROLLER |
| 5C | TEST RAM BETWEEN 512K AND 640K | 92 | JUMP TO USER PATCH 2 |
| 60 | TEST EXTENDED MEMORY | 94 | DISABLE A20 ADDRESS LINE |
| 62 | TEST EXTENDED MEMORY ADDRESS LINE | 96 | CLEAR HUGE ES SEGMENT REG. |
| 64 | JUMP TO USER PATCH 1 | 98 | SEARCH FOR OPTION ROMS |

DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP		MAIN	
APPROVAL	KIM, DW	REV	1.0		FIRMWARE HUB	
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	21 OF 49	

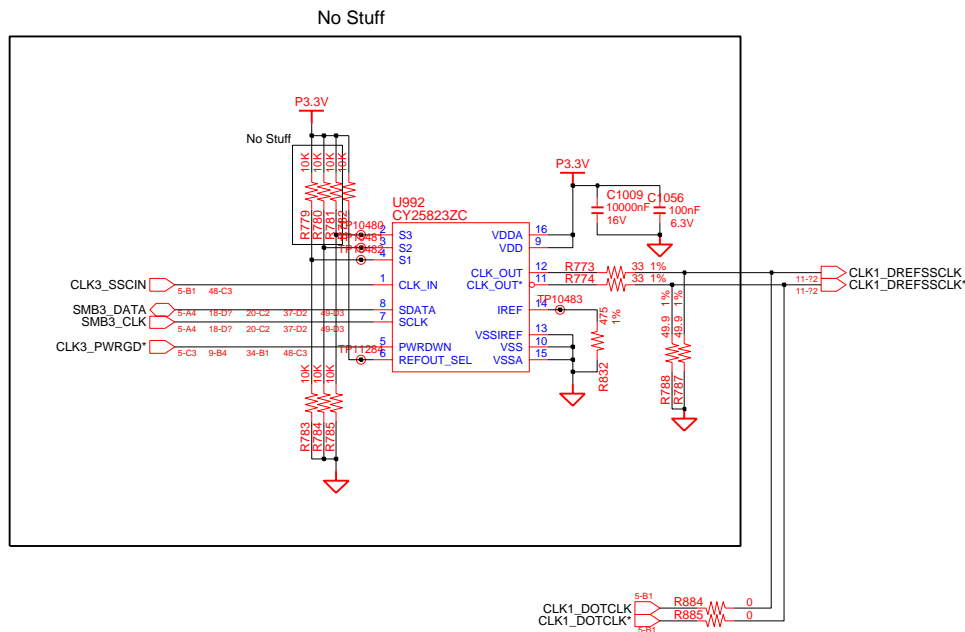
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LVDS Voltage Translation Logic (2.5V -> 3.3V)



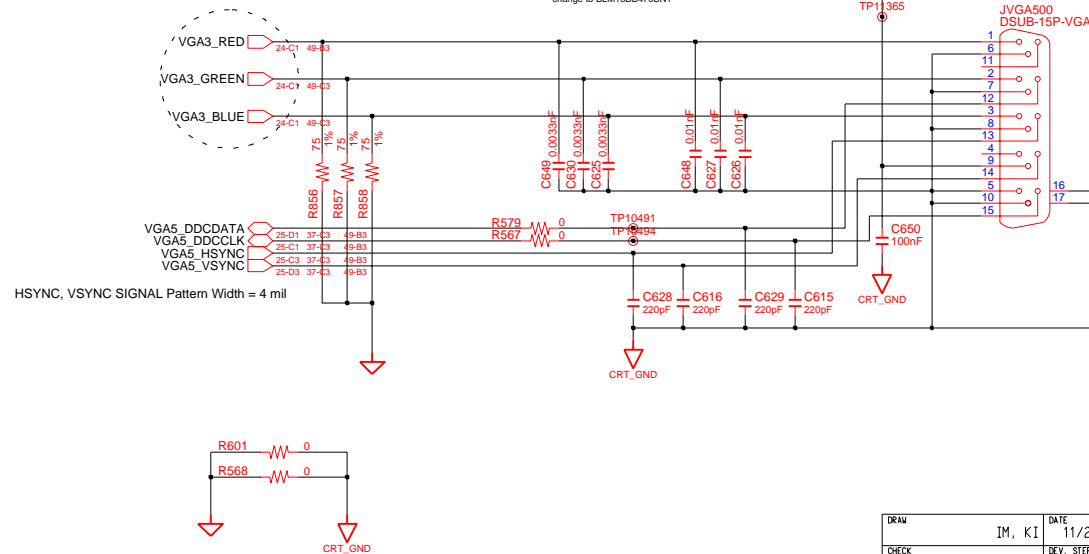
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CHECK	BIN, KK	DEV. STEP	MP		MAIN	
APPROVAL	KIM, DW	REV	1.0	ATI M24 GRAPHIC CONTROL1/4	PART NO.	BA41-00451A
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	22	OF 49

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change to BLM18BB470SN1

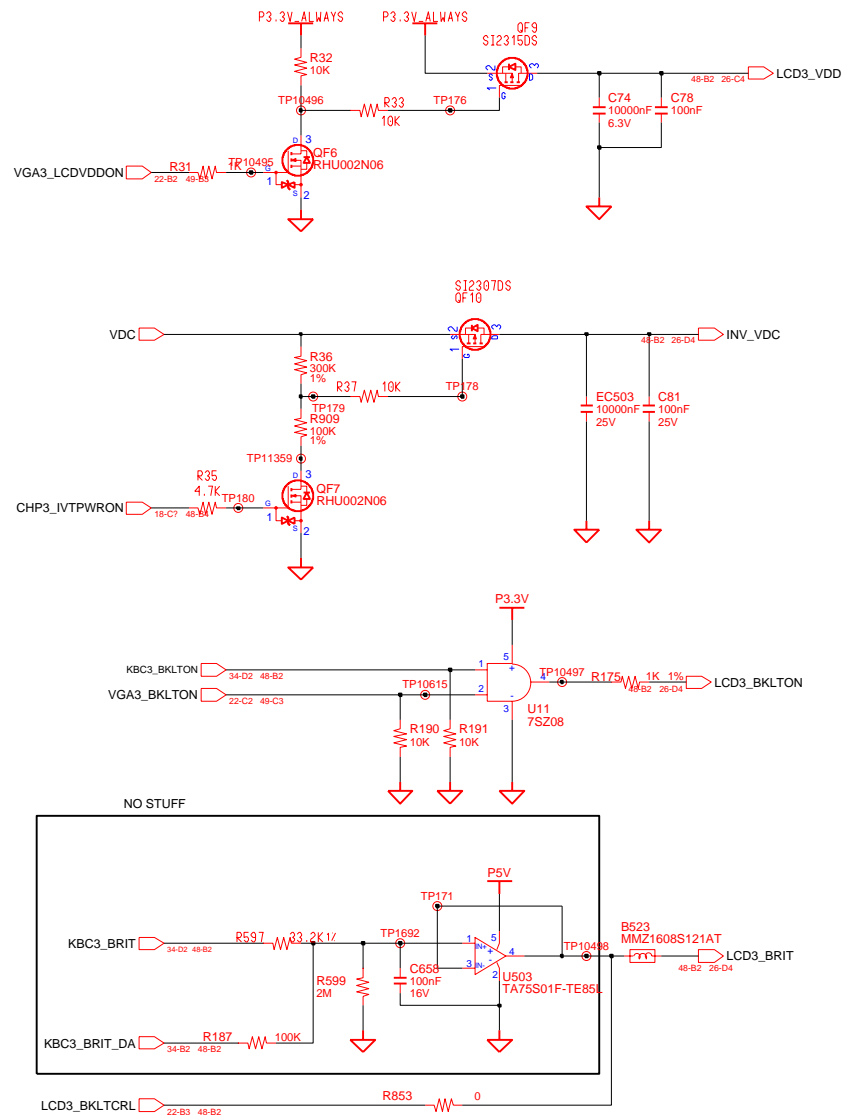
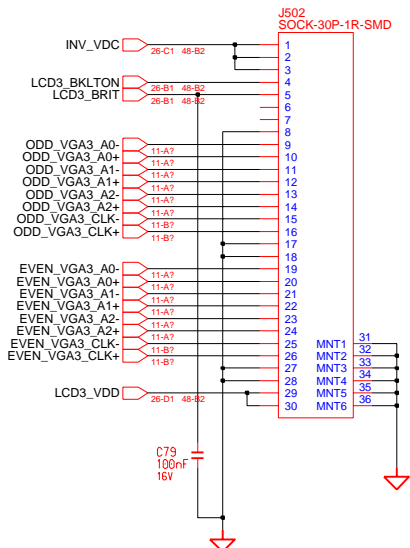


~~Optional External Thermal Sensor~~

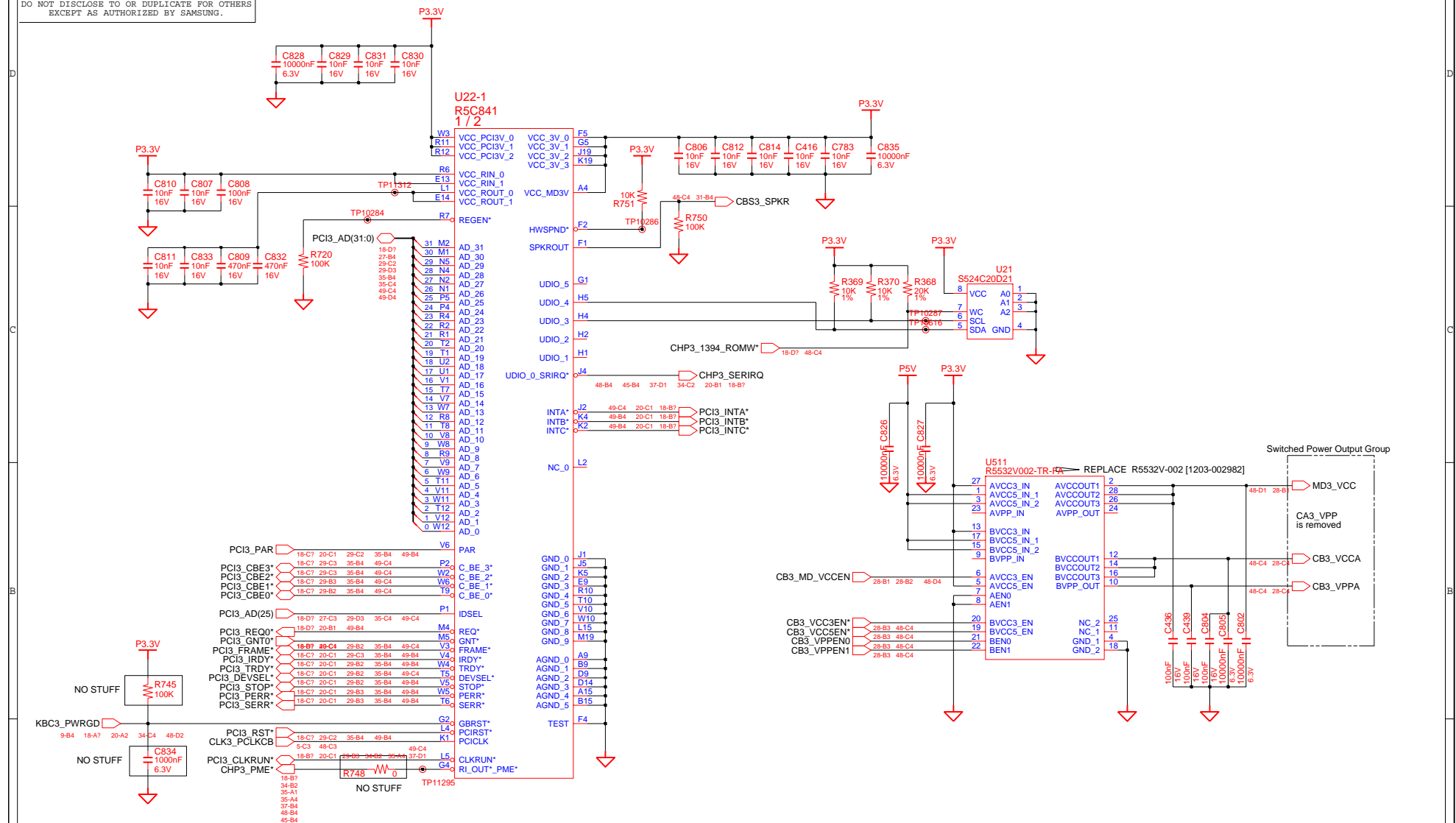
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CHECK		BIN, KK	DEV. STEP	MP			MAIN			
APPROVAL		KIM, DW	REV	1.0	CRT PORT/SPREAD SPECTRUM		PART NO.			
MODULE CODE		LAST EDIT		November 29, 2004 10:05:41 AM				PAGE	25	OF 49

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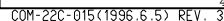
LCD CONNECTOR



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CHECK	BIN, KK	DEV. STEP	MP			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	26 OF 49	

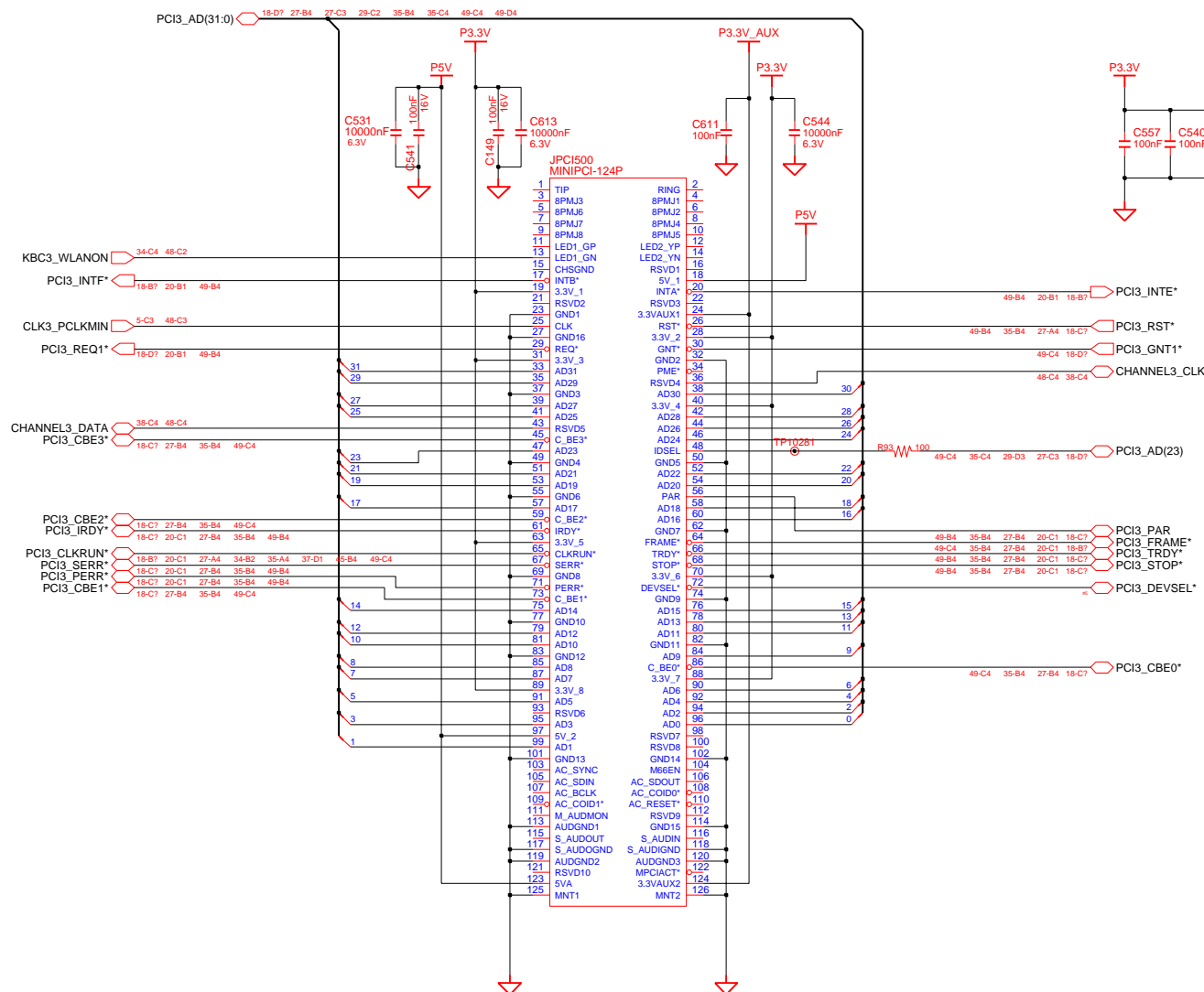


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IM, KI		11/29/2004	CYGNUS C		
CHECK	BIN, KK	DEV. STEP	MAIN		
APPROVAL		REV	CARDBUS / 1394		
KIM, DW		1.0			PART NO. BA41-00451A
MODULE CODE		LAST EDIT		November 29, 2004 10:05:41 AM	PAGE 27 OF 49



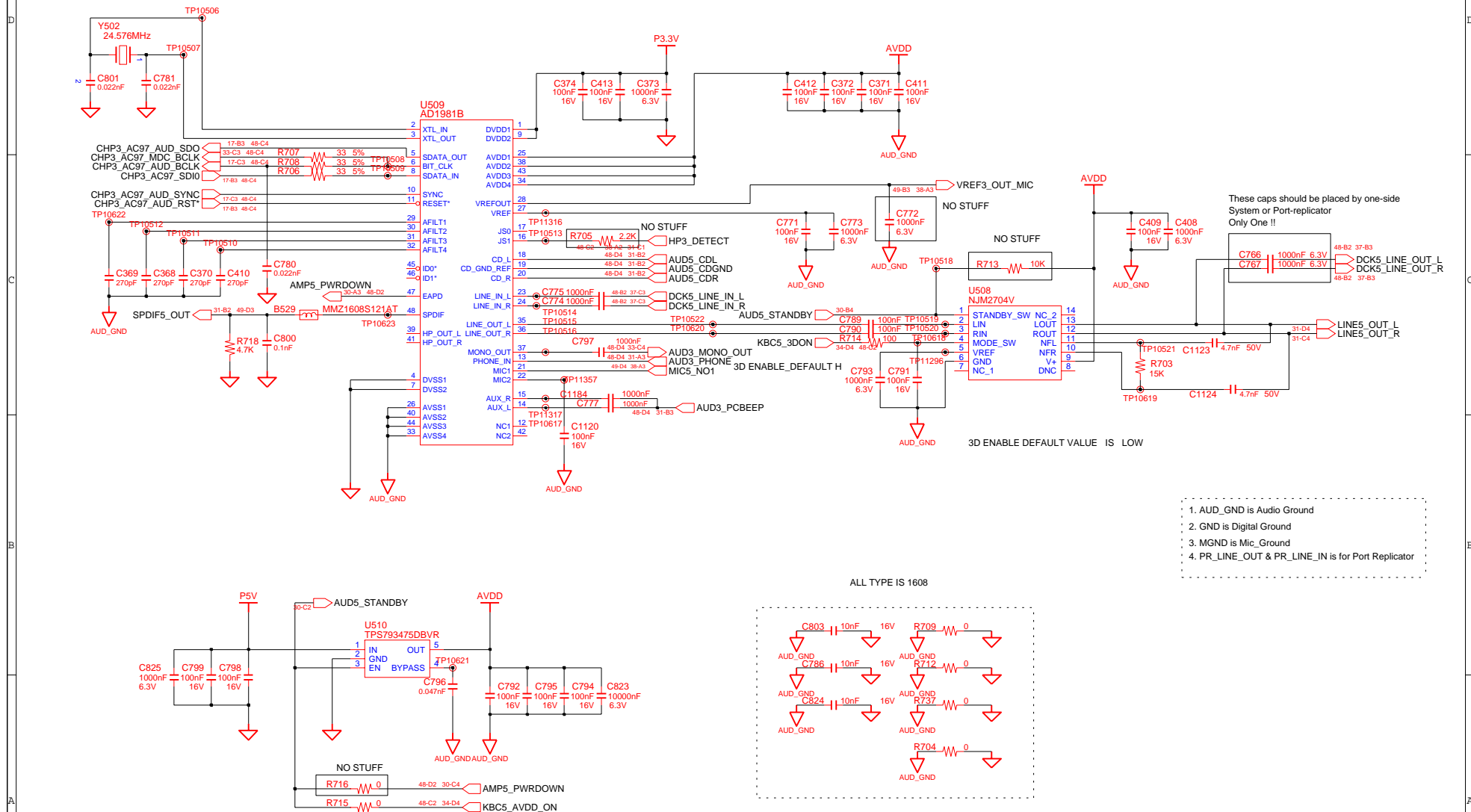
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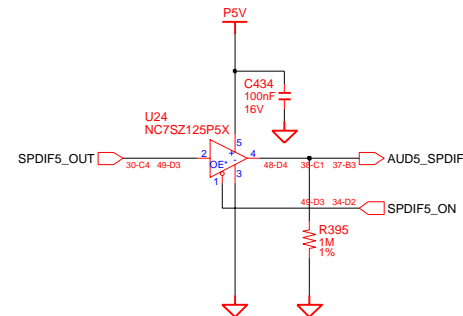
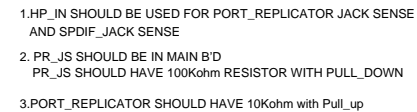


DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP		MAIN	
APPROVAL	KIM, DW	REV	1.0		MINI PCI	
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM			
						PART NO. BA41-00451A
						PAGE 29 OF 49

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DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP		MAIN	
APPROVAL	KIM, DW	REV	1.0		AUDIO CODEC & AMP	PART NO.
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	30	OF 49

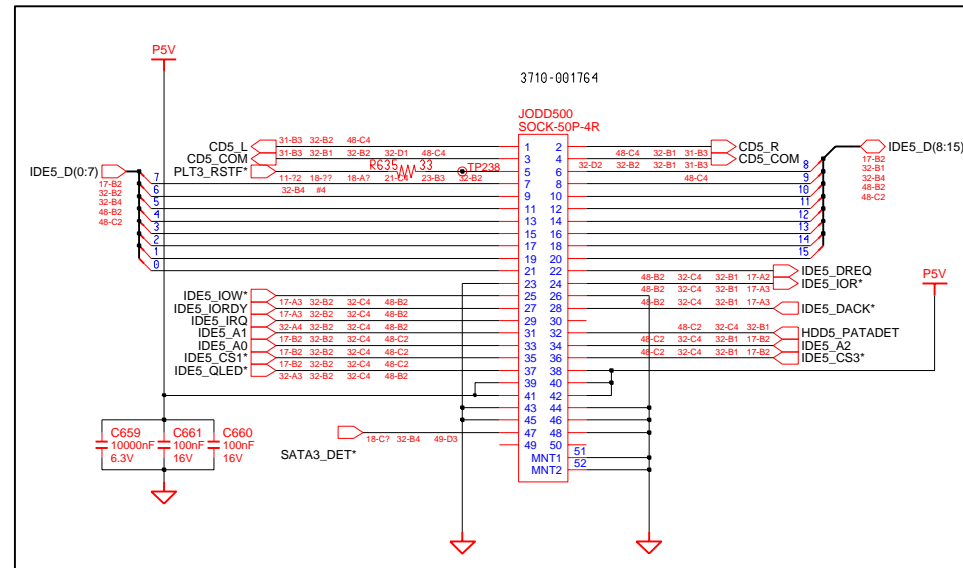


DRAW		IM, KI	DATE	11/29/2004		TITLE		<div style="text-align: center;"> CYGNUS C SAMSUNG ELECTRONICS </div>	
CHECK		BIN, KK	REV.	STEP	MP	MAIN			
APPROVAL		KIM, DW	REV	1.0		AUDIO CODEC & AMP			
MODULE CODE		LAST EDIT		November 29, 2004 10:05:41 AM		PAGE	31 OF 49		

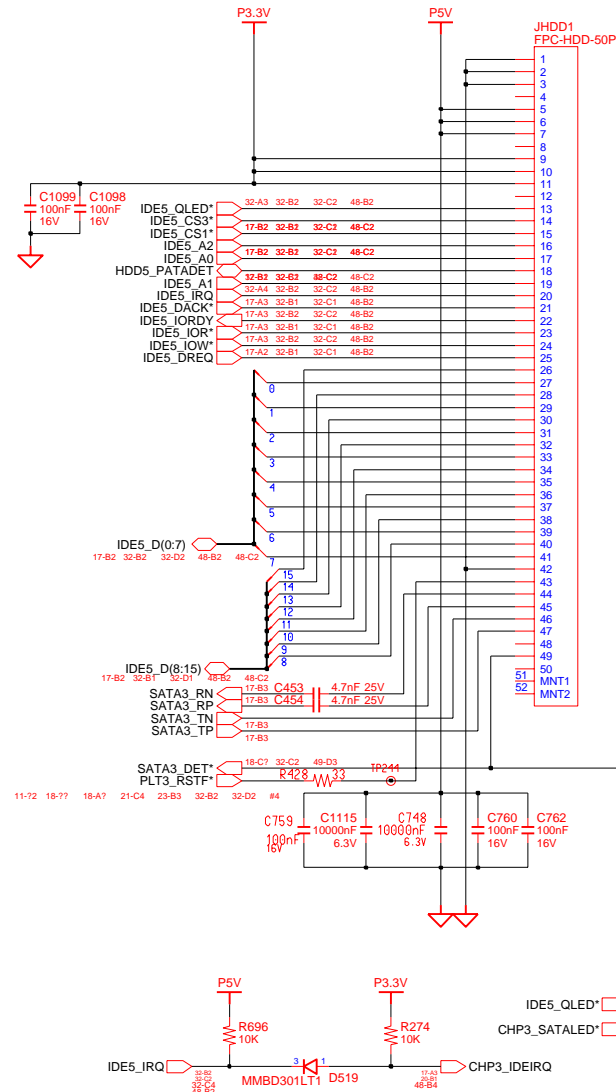
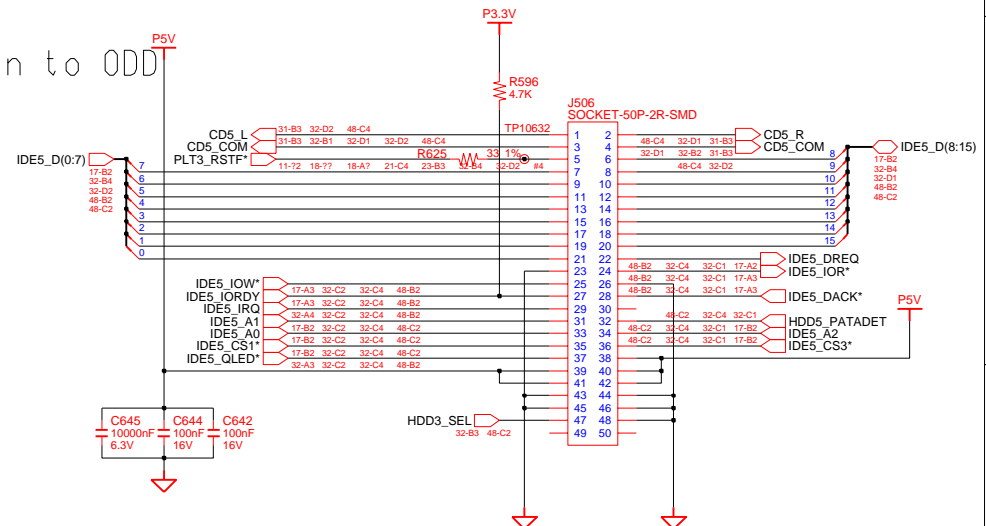
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Main to HDD

NO STUFF

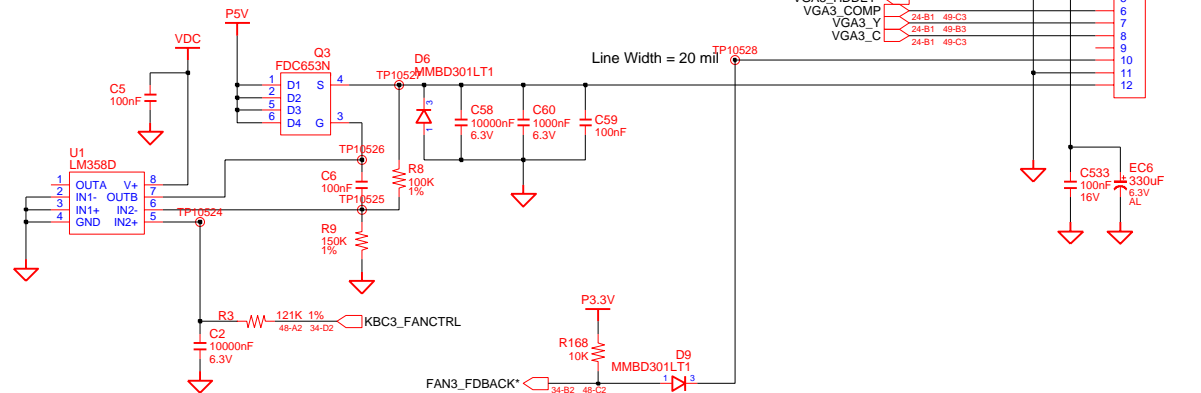
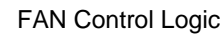


Main to ODD



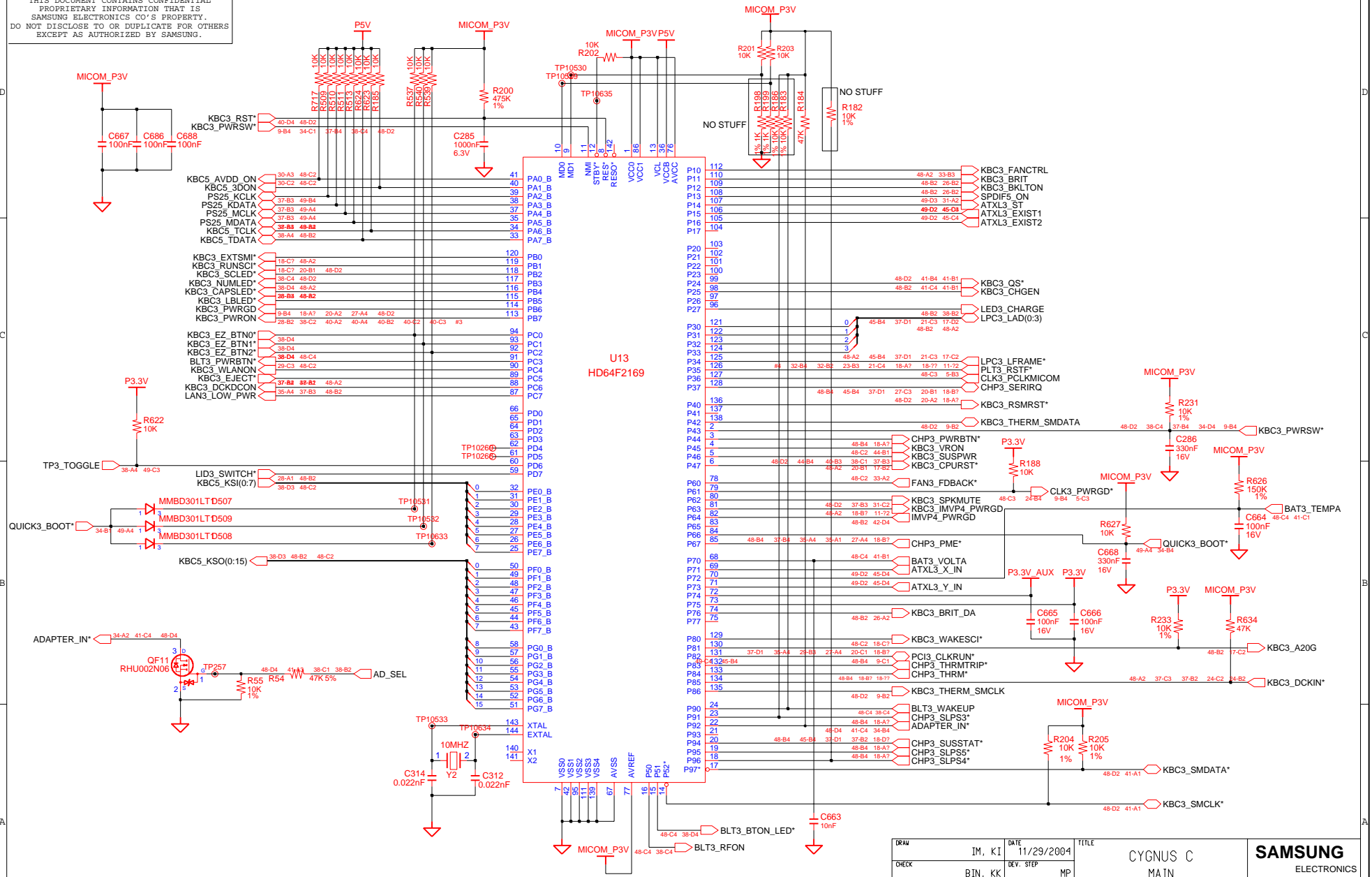
DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP	MAIN		
APPROVAL	KIM, DW	REV	1.0	HDD & ODD CONNECTOR		PART NO.
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM			BA41-00451A
					PAGE	32 OF 49

TV-OUT(S-VHS)

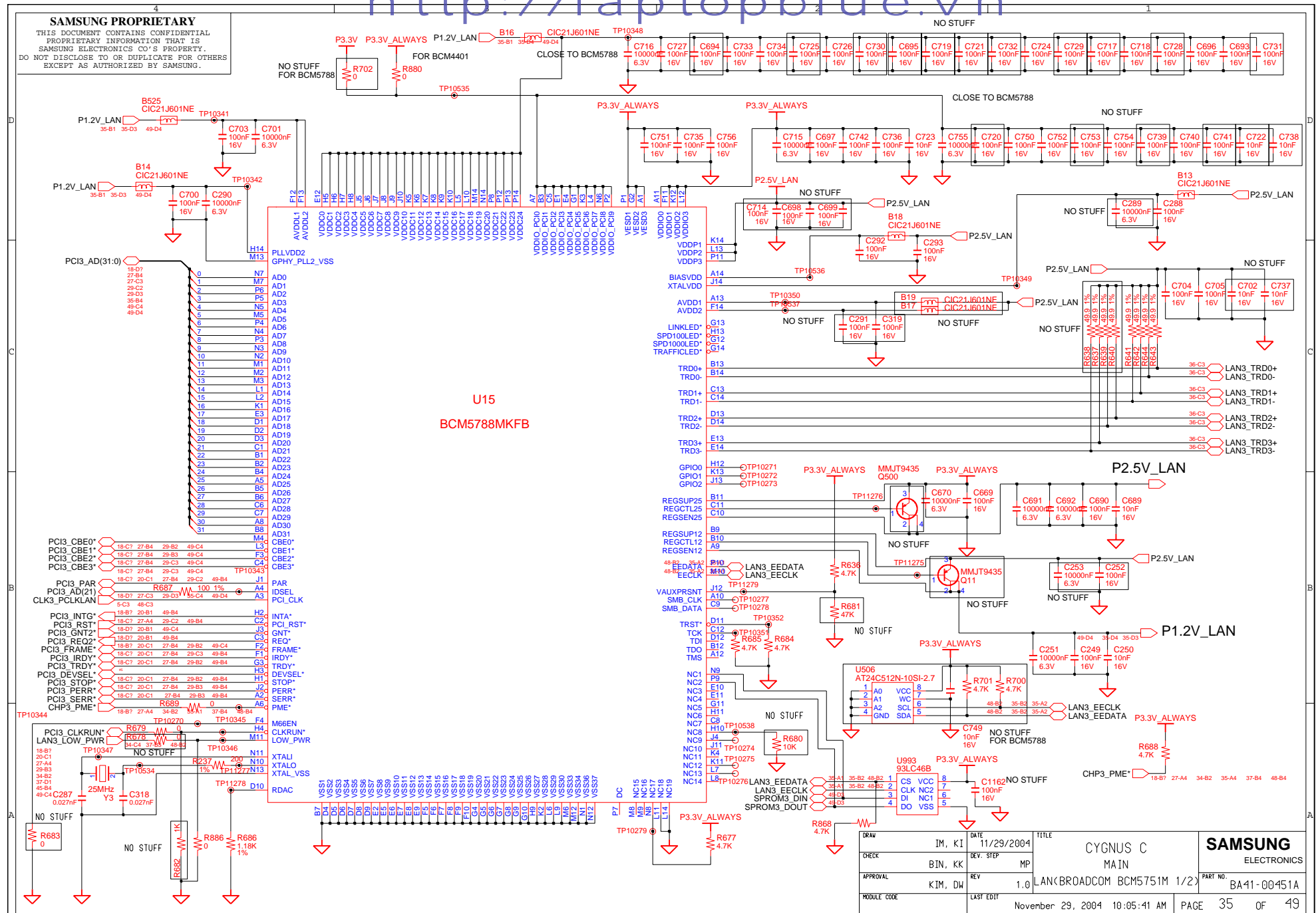


DRAW		IM, KI	DATE	11/29/2004		TITLE		CYGNUS C		SAMSUNG ELECTRONICS	
CHECK		BIN, KK	DEV. STEP	MP		MAIN					
APPROVAL		KIM, DW	REV	1.0		MDC MODEM / TV-OUT(SVHS)				PART NO.	BA41-00451A
MODULE CODE		LAST EDIT		November 29, 2004 10:05:41 AM				PAGE	33	OF	49

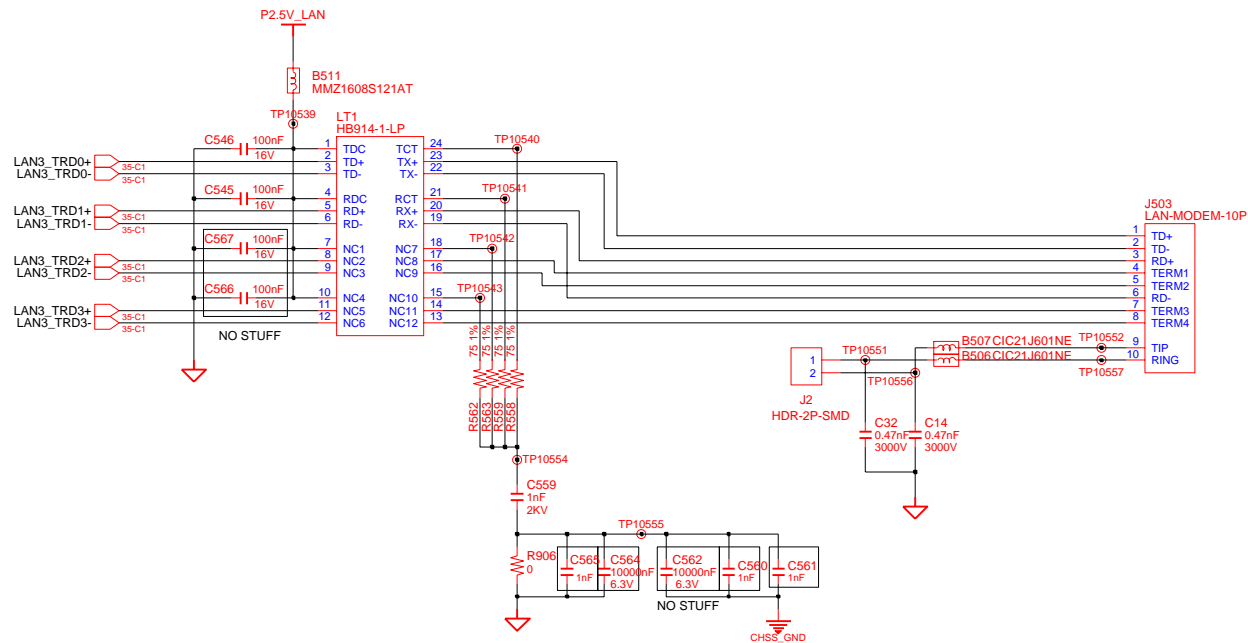
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DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP	MAIN	MAIN	
APPROVAL	KIM, DW	REV	1.0	MICOM	MICOM	PART NO.
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	34	BA41-00451A
				OF	49	

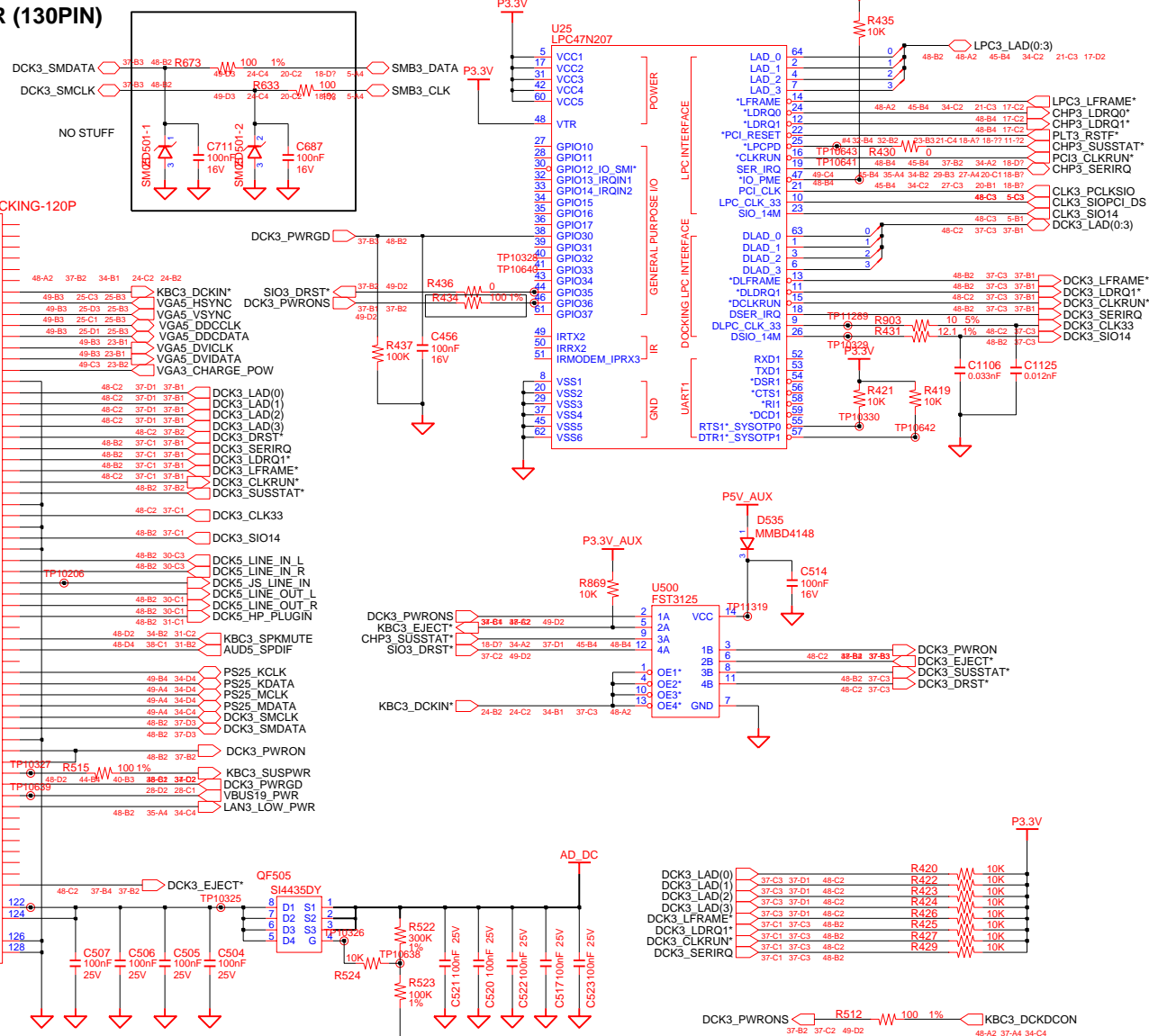


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DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP		MAIN	
APPROVAL	KIM, DW	REV	1.0	LAN(BROADCOM BCM5751M 2/2)	PART NO.	BA41-00451A
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	36	OF 49

Docking Placement			
PWR1	1	129	PWR4
Top View			
PWR3	2	130	PWR2



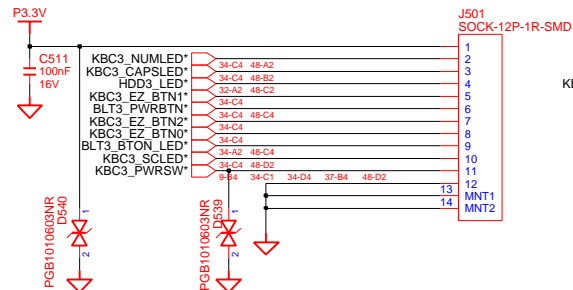
DRAM	IM, KI	DATE	11/29/2004	TITLE		CYGNUS C MAIN DOCKING CONNECTOR	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP				
APPROVAL	KIM, DW	REV	1.0			PART NO.	BA41-00451A
MODULE CODE		LAST EDIT		November 29, 2004 10:05:41 AM		PAGE	37 OF 49

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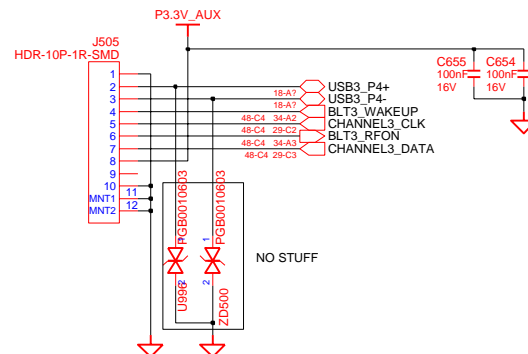
KEYBOARD

Main to DC/DC BOARD

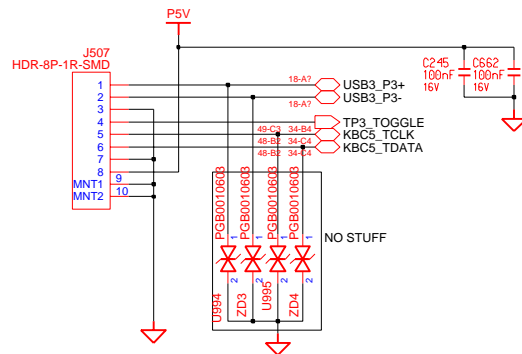
MAIN TO ON-TOP



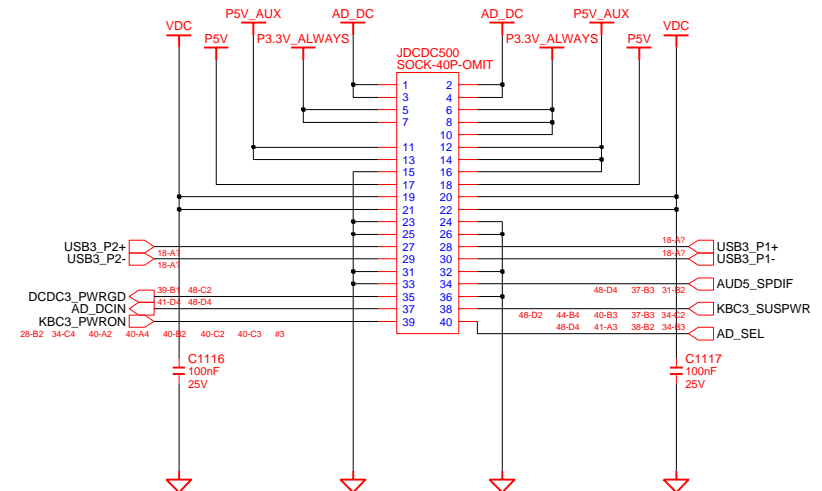
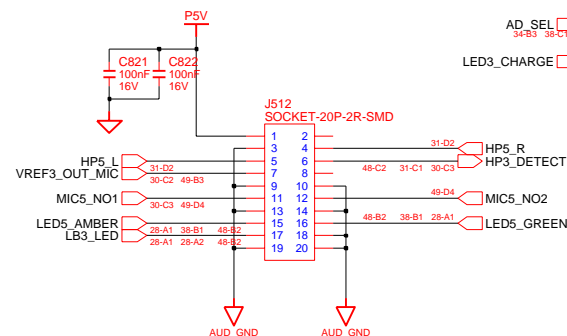
BLUETOOTH CONNECTOR



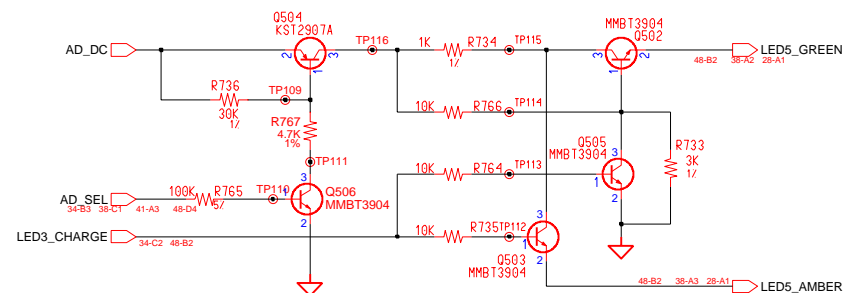
TOUCHPAD CONNECTOR



AUDIO CONNECTOR



ADAPTERIN/CHARGING LED

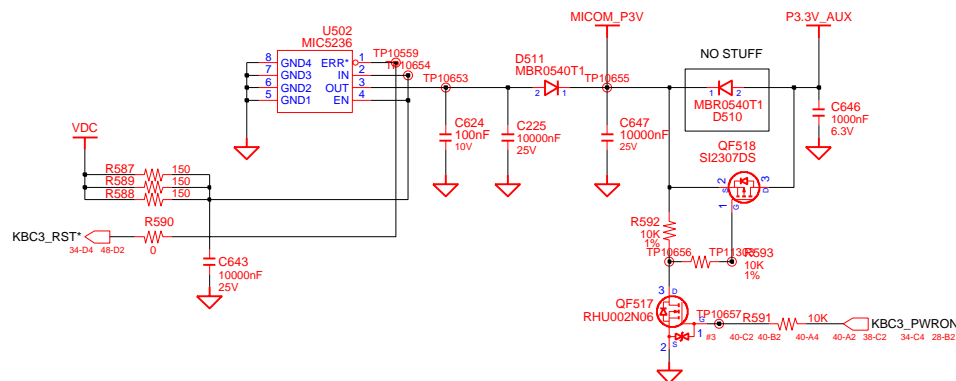


DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP	MAIN	MAIN	
APPROVAL	KIM, DW	REV	1.0	B'D TO B'D CONNECTOR	PART NO.	BA41-00451A
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	38	OF 49

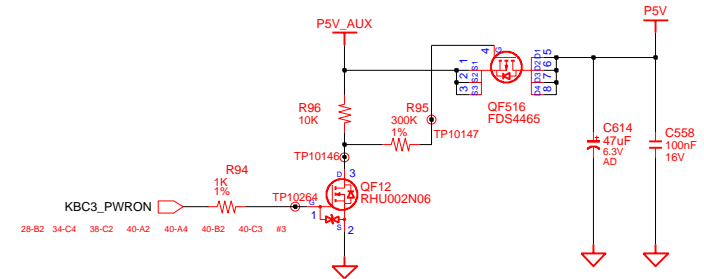
DRAW		IM, KI	DATE	11/29/2004	TITLE			CYGNUS C MAIN DDR POWER			SAMSUNG ELECTRONICS		
CHECK		BIN, KK	DEV. STEP	MP									
APPROVAL		KIM, DW	REV	1.0									
MODULE CODE		LAST EDIT			November 29, 2004 10:05:41 AM			PAGE	39	OF	49	PART NO.	BA41-00451A

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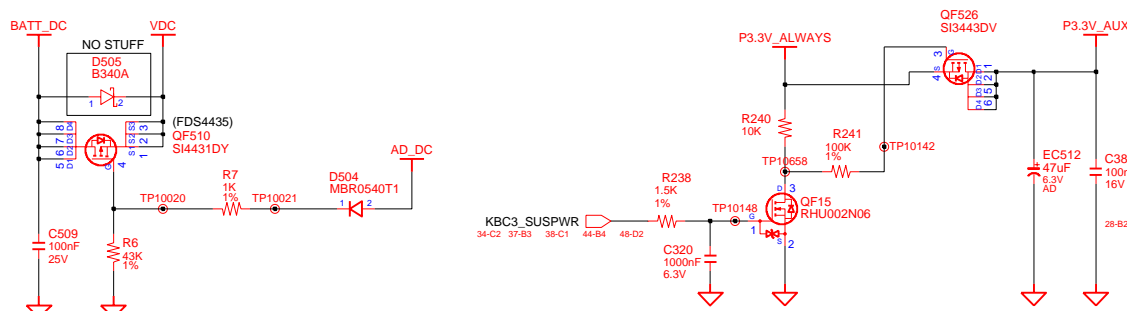
MICOM_P3V Power



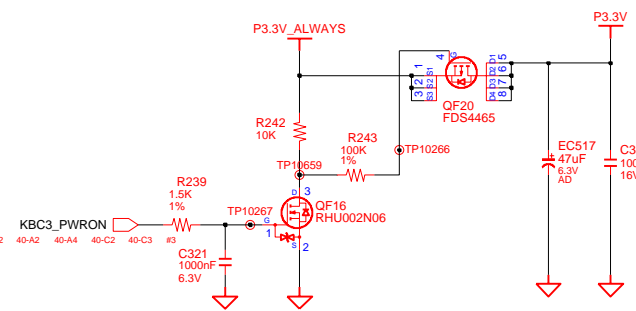
Switched Power On (P5V)



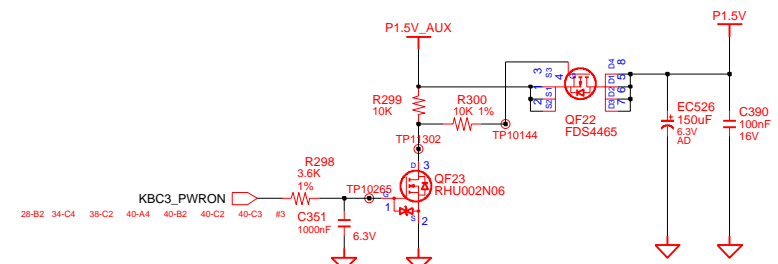
Switched Power On (P3.3V_AUX)



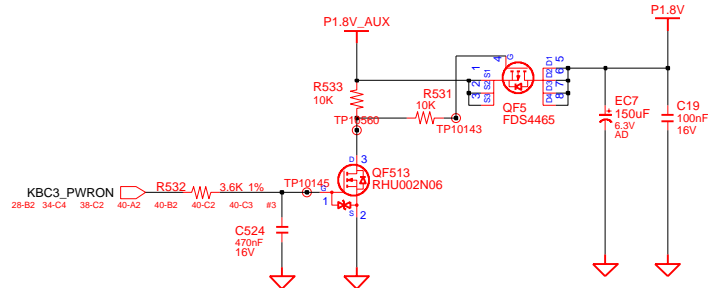
Switched Power On (P3.3V)



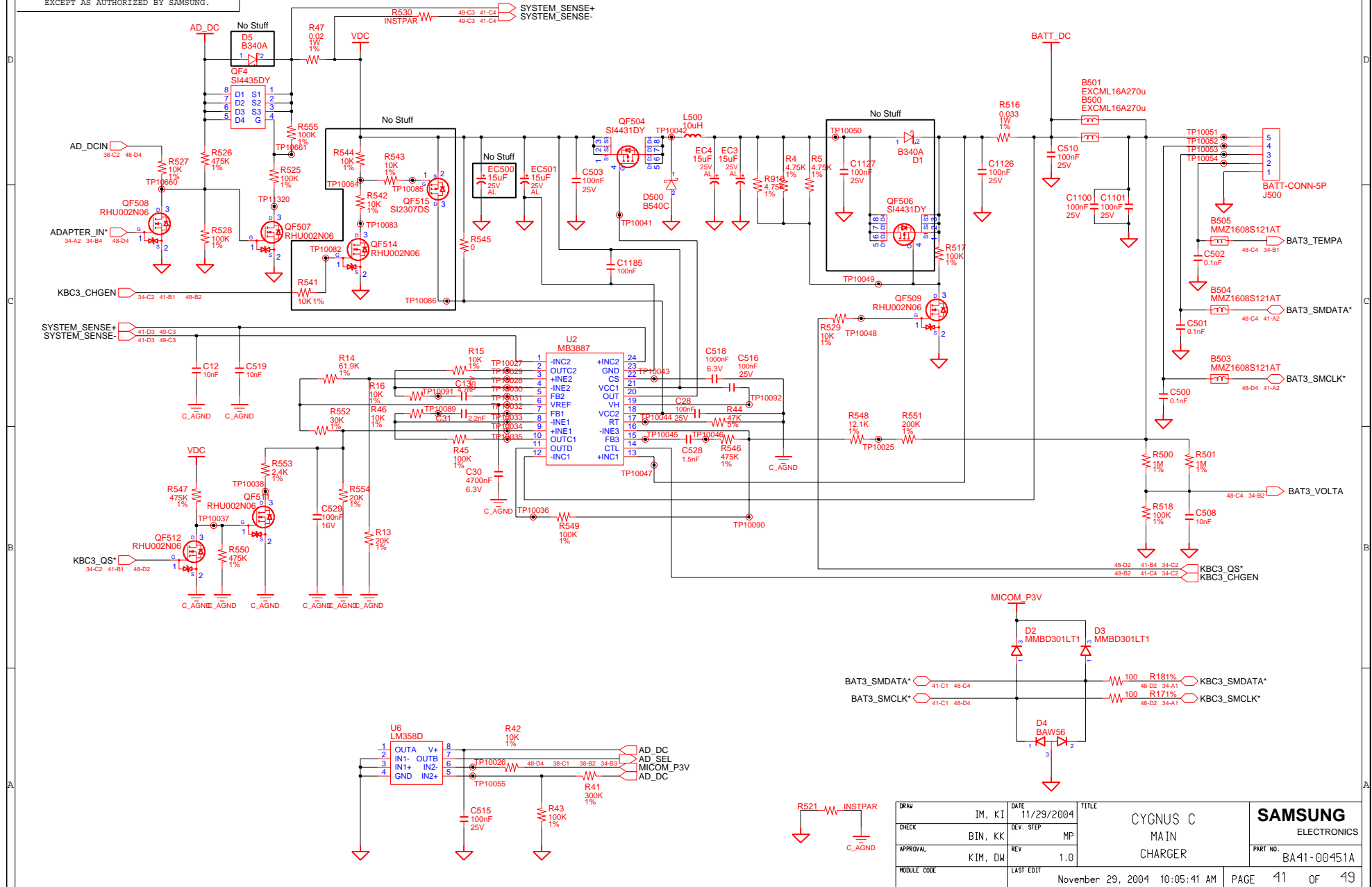
Switched Power On (P1.5V)

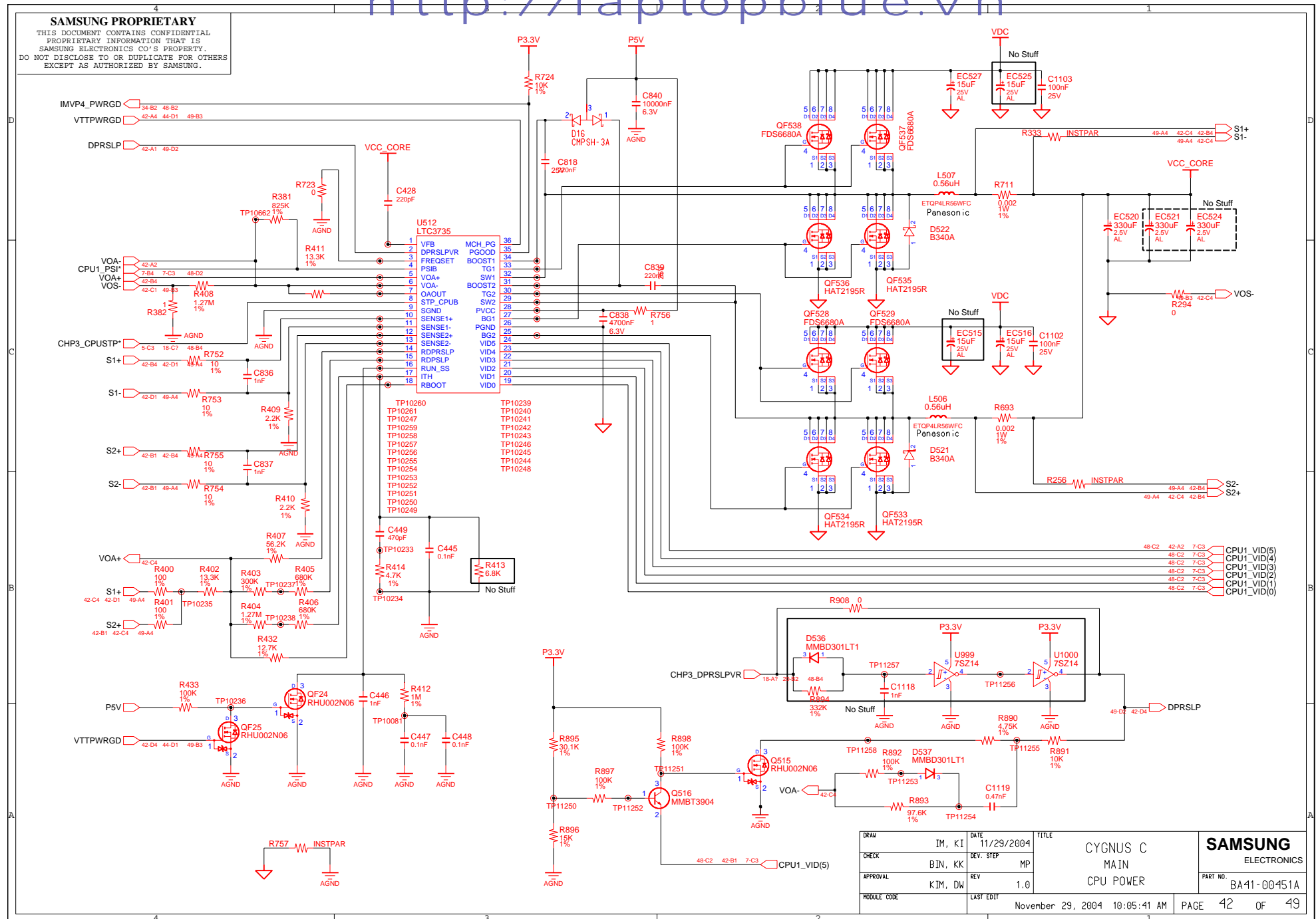


Switched Power On (P1.8V)

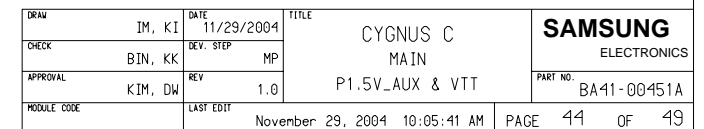


DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP		MAIN	
APPROVAL	KIM, DW	REV	1.0		MICOM & SWITCHED POWER	PART NO.
MODULE CODE		LAST EDIT				BA41-00451A
				November 29, 2004 10:05:41 AM	PAGE	40 OF 49



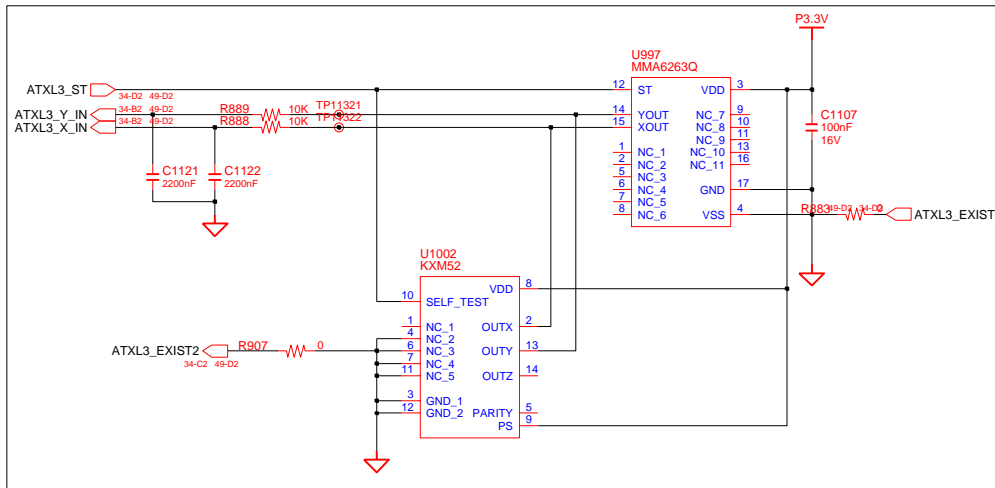


DRAW		DATE	TITLE		SAMSUNG ELECTRONICS
IM, KI		11/29/2004	CYGNUS C		
CHECK	BIN, KK	DEV. STEP	MAIN		
APPROVAL	KIM, DW	REV	P2.5V & P1.2V		
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM		PART NO. BA41-00451A
			PAGE	43	OF 49

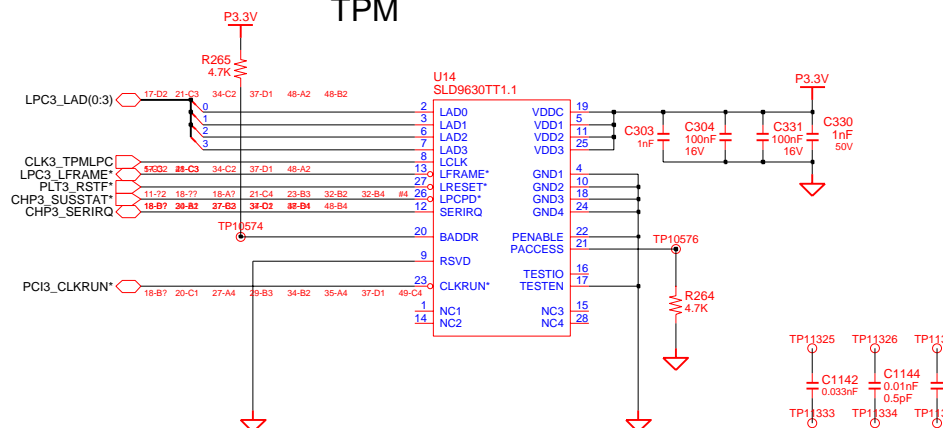


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AIRBAG

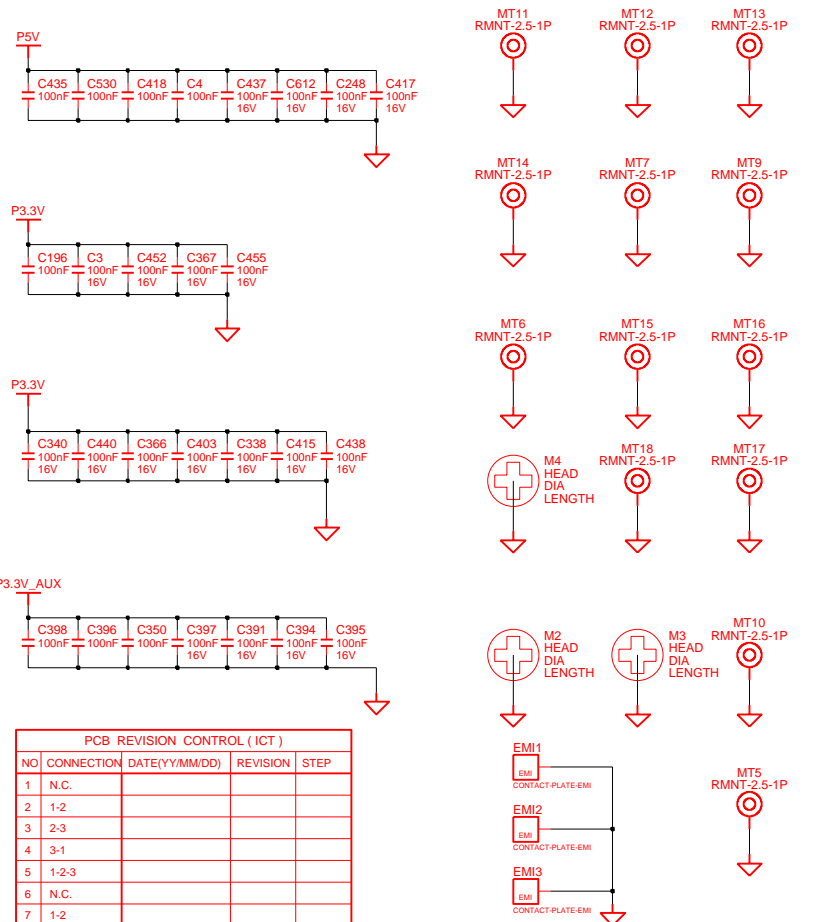


TPM



REV1
1
2 0 0 3

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

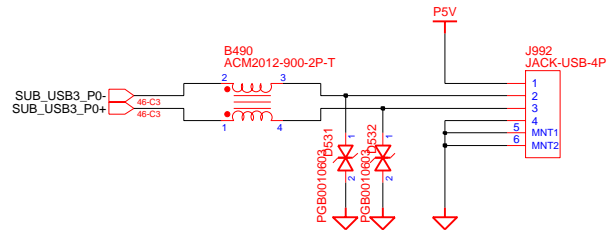


DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAINBD AIRBAG & TPM	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP			PART NO. BA41-00451A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	45 OF 49	

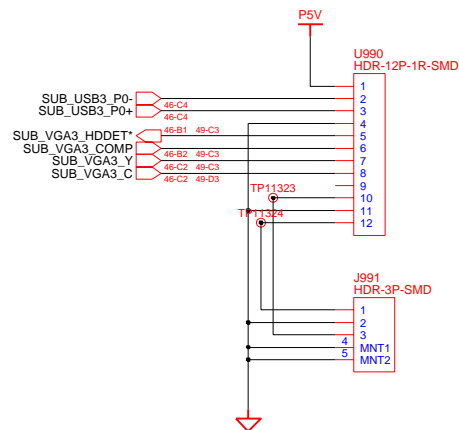
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< USB BOARD >

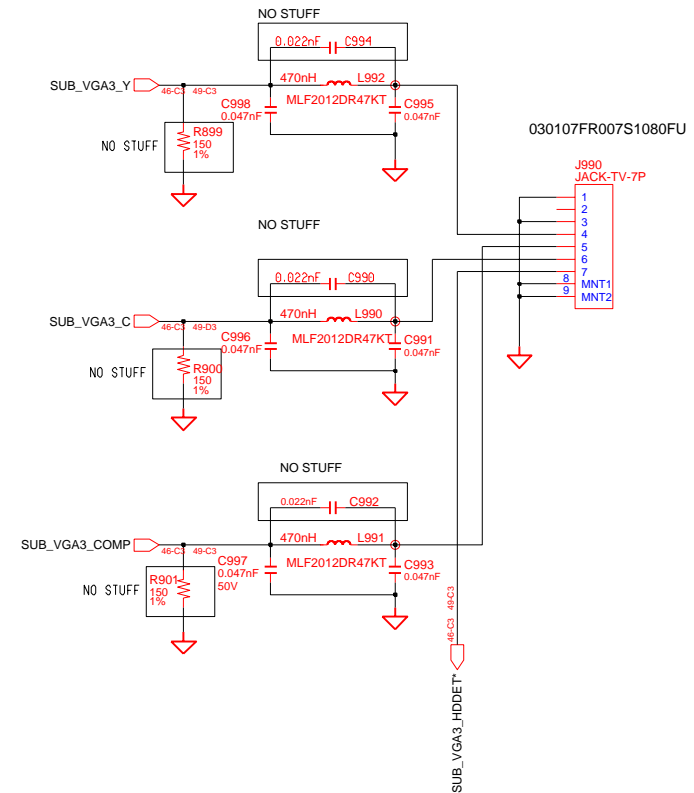
USB Connector



Mother Board I/F



TV OUT JACK



DRAW	IM, KI	DATE	11/29/2004	TITLE	CYGNUS C MAIN MOUNT HOLE	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	MP			PART NO. BA41-00451A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 29, 2004 10:05:41 AM	PAGE	46 OF 49	

4

1

2

3

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Revision History

Page No.

Cause And Actions (Revised Items)

Page No.

Cause And Actions (Revised Items)

DRAWIM, KI

CHECKBIN, KK

APPROVALKIM, DW

MODULE CODE

DATE11/29/2004

DEV. STEPMP

REV1.0

LAST EDIT

TITLE

CYGNUS C
MAIN
REV. HISTORY

November 29, 2004 10:05:41 AM

PAGE47 OF49

SAMSUNG

ELECTRONICS

PART NO.

BA41-00451A

COM-22C-015(1996.6.5) REV. 3

d:/users/mobile20/mentor/cygnus_c/mp1.1/main.mp10_final_20041119

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TP11030MIC5_N01
TP11031MIC5_N02

TP10663OP1.2V_LAN

TP11032OPIC3_AD(0)
TP11033OPIC3_AD(1)
TP11034OPIC3_AD(10)
TP11035OPIC3_AD(11)
TP11036OPIC3_AD(12)
TP11037OPIC3_AD(13)
TP11038OPIC3_AD(14)
TP11039OPIC3_AD(15)
TP11040OPIC3_AD(16)
TP11041OPIC3_AD(17)
TP11042OPIC3_AD(18)
TP11043OPIC3_AD(19)
TP11044OPIC3_AD(2)
TP11045OPIC3_AD(20)
TP11046OPIC3_AD(21)
TP11047OPIC3_AD(22)
TP11048OPIC3_AD(23)
TP11049OPIC3_AD(24)
TP11050OPIC3_AD(25)
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TP11055OPIC3_AD(3)
TP11056OPIC3_AD(30)
TP11057OPIC3_AD(31)
TP11058OPIC3_AD(4)
TP11059OPIC3_AD(5)
TP11060OPIC3_AD(6)
TP11061OPIC3_AD(7)
TP11062OPIC3_AD(8)
TP11063OPIC3_AD(9)
TP11064OPIC3_CBE0*
TP11065OPIC3_CBE1*
TP11066OPIC3_CBE2*
TP11067OPIC3_CBE3*
TP11068OPIC3_CLKRUN*
TP11069OPIC3_DEVSSEL*
TP11070OPIC3_FRAME*
TP11071OPIC3_GNT0*
TP11072OPIC3_GNT1*
TP11073OPIC3_GNT2*
TP11074OPIC3_GNT3*
TP11075OPIC3_INTA*
TP11076OPIC3_INTB*
TP11077OPIC3_INTC*
TP11078OPIC3_INTD*
TP11079OPIC3_INTE*
TP11080OPIC3_INTF*
TP11081OPIC3_INTG*
TP11082OPIC3_INTH*
TP11083OPIC3_IRDY*
TP11084OPIC3_PAR*
TP11085OPIC3_PERR*
TP11086OPIC3_PLCK*
TP11087OPIC3_RE00*
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TP11090OPIC3_RE03*
TP11091OPIC3_RS1*
TP11092OPIC3_SERR*
TP11093OPIC3_STOP*
TP11094OPIC3_TRDY*
TP11096OPICIE3_WAKE*
TP11097OPLT3_RST*
TP11098OPLT3_RSTF*
TP11099OPS25_CLK*
TP11100OPS25_DATA*
TP11101OPS25_NCLK*
TP11102OPS25_MDATA*
TP11103QUICK3_BOOT*
TP11104OS1+
TP11105OS1-
TP11106OS2+
TP11107OS2-

TP11108OSATA3_DET*
TP11109OSMB3_ALERT*
TP11110OSMB3_CLK*
TP11111OSMB3_DATA*
TP11112OSMB3_LINKALERT*
TP11113OSPDIF5_ON*
TP11114OSPDIF5_OUT*
TP11115OSPR0M3_DIN*
TP11116OSPR0M3_DOUT*
TP11117OSUB_VGA3_C*
TP11118OSUB_VGA3_COMP*
TP11119OSUB_VGA3_HDET*
TP11120OSUB_VGA3_Y*
TP11121OSYSTEM_SENSE+*
TP11122OSYSTEM_SENSE-*
TP11123OTPGGLE*
TP11124OVGA2_DDCCLK*
TP11125OVGA2_DDCDATA*
TP11126OVGA3_BKLTON*
TP11127OVGA3_BLUE*
TP11128OVGA3_C*
TP11129OVGA3_CHARGE_POW*
TP11130OVGA3_COMP*
TP11131OVGA3_DVCLK*
TP11132OVGA3_DVDATA*
TP11133OVGA3_GREEN*
TP11134OVGA3_HDET*
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TP11141OVGA5_DDCDATA*
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TP11143OVGA5_DVDATA*
TP11144OVGA5_HSYNC*
TP11145OVGA5_VSYNC*
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TP11148OVTTWRGD*
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TP11176OP0_9V*
TP11177OP0_9V*
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TP11191OP1_5V_AUX*
TP11192OP1_5V_AUX*
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TP11201OP1_8V_AUX*
TP11202OP1_8V_AUX*
TP11203OP1_8V_AUX*
TP11204OP1_8V_AUX*
TP11205OP1_8V_AUX*
TP11206OP2_5V_LAN*
TP11207OP2_5V_LAN*
TP11208OP2_5V_LAN*
TP11209OP2_5V_LAN*
TP11210OP2_5V_LAN*
TP11211OP3_3V_AUX*
TP11212OP3_3V_AUX*
TP11213OP3_3V_AUX*

TP11214OP3_3V_AUX*
TP11215OP3_3V_AUX*
TP11216OP5V*
TP11217OP5V*
TP11218OP5V*
TP11219OP5V*
TP11220OP5V*
TP11221OP5V_AUX*
TP11222OP5V_AUX*
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TP11225OP5V_AUX*
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TP11245OP3_3V_ALWAYS*
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TP11249OP3_3V_ALWAYS*

TP11262OATXL3_EXIST1*
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TP11273OSI03_DRST*

TP11266OVCC_NCTF*
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