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FIRENZE II

CPU : Intel Yonah (533/667MHz)

Chip Set : RC410MD & SB450

Remarks : Mobility Platform

Model Name : FIRENZE II

PBA Name : MAIN

PCB Code : GCE : BA41-00659A
TPT : BA41-00671A

Dev. Step : PRR

Revision : X03

T.R. Date : 2006.03.30

DRAW	CHECK	APPROVAL
TERMI	HJ KIM	SJ PARK

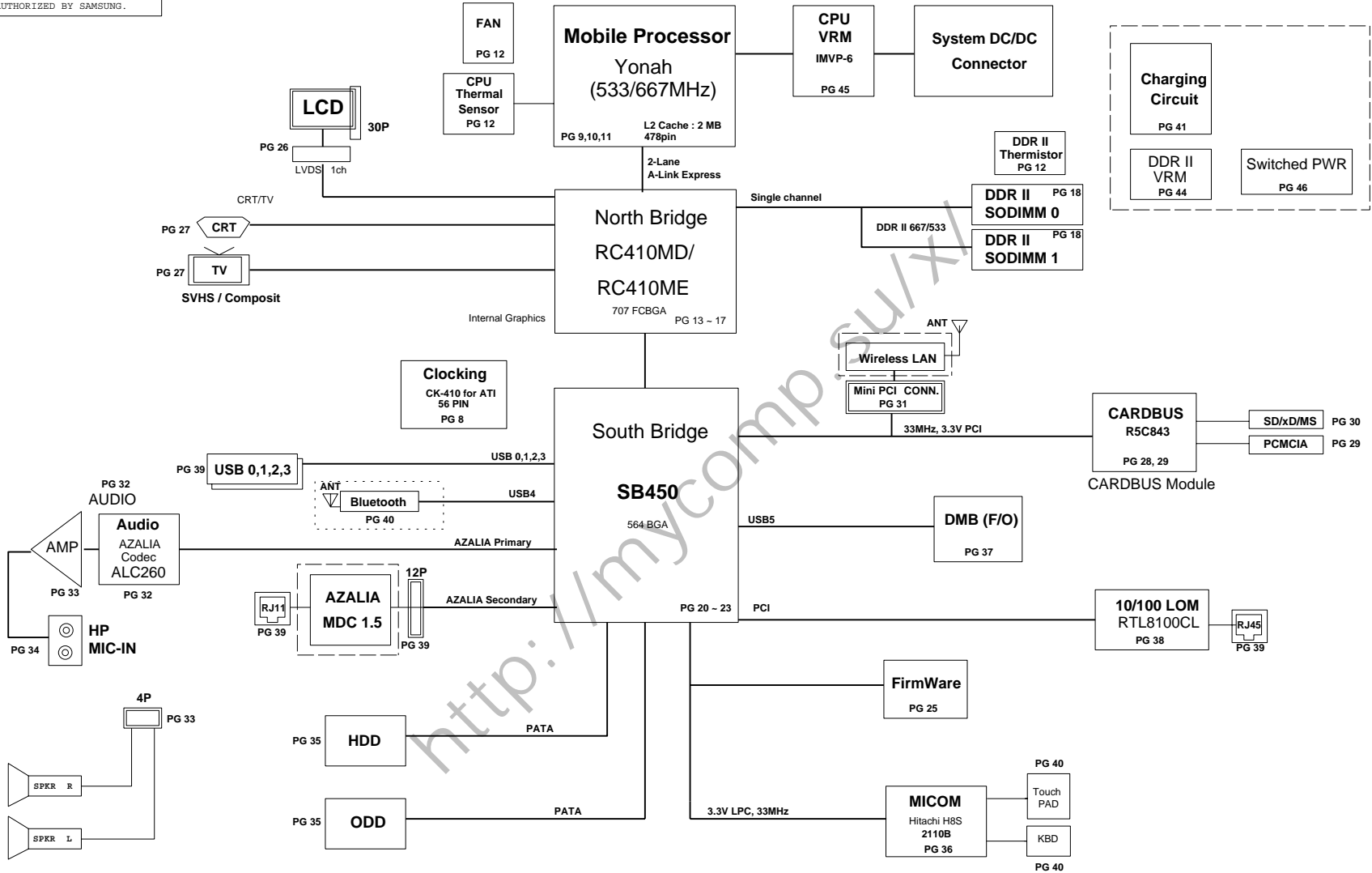
■ Owner : SEC Mobile R & D Signature : X

Table of Contents

Sheet 1. COVER
Sheet 2 - 7. DIAGRAM (Block/Power) & ANNOTATIONS
Sheet 8. CLOCK GENERATOR
Sheet 9 - 11. YONAH
Sheet 12. THERMAL SENSOR / FAN CONTROL
Sheet 13 - 17. RC410MD/RC410ME
Sheet18. DDR II SODIMM
Sheet19. DDR II TERMINATION
Sheet20 - 23. SB450
Sheet24. SB450 STRAPS
Sheet25. FIRMWARE
Sheet26. LCD
Sheet27. CRT AND TV CONN
Sheet28-29. CARDBUS
Sheet30. 6 IN 1
Sheet31. MINIPCI
Sheet32-34. AUDIO
Sheet35. HDD & ODD
Sheet36. MICOM
Sheet37. LID S/W & WLAN ON/OFF S/W & DMB
Sheet38. LOM
Sheet39. LAN & MDC CONN & USB
Sheet40. LED & BLUETOOTH & TOUCHPAD & KEYBOARD
Sheet41. CHARGE
Sheet42. P3.3V_AUX & P5V_AUX
Sheet43. P1.2V & VCCP
Sheet44. DDR2 POWER
Sheet45. CPU VRM
Sheet46. P2.5V/P1.5V POWER & SWITCHED POWER
Sheet47. P1.8V_ALW
Sheet48. POWER STRAPS
Sheet49-50. TP

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR		COVER	
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT				
				April 5, 2006 8:18:08 PM	PAGE	1 OF 52

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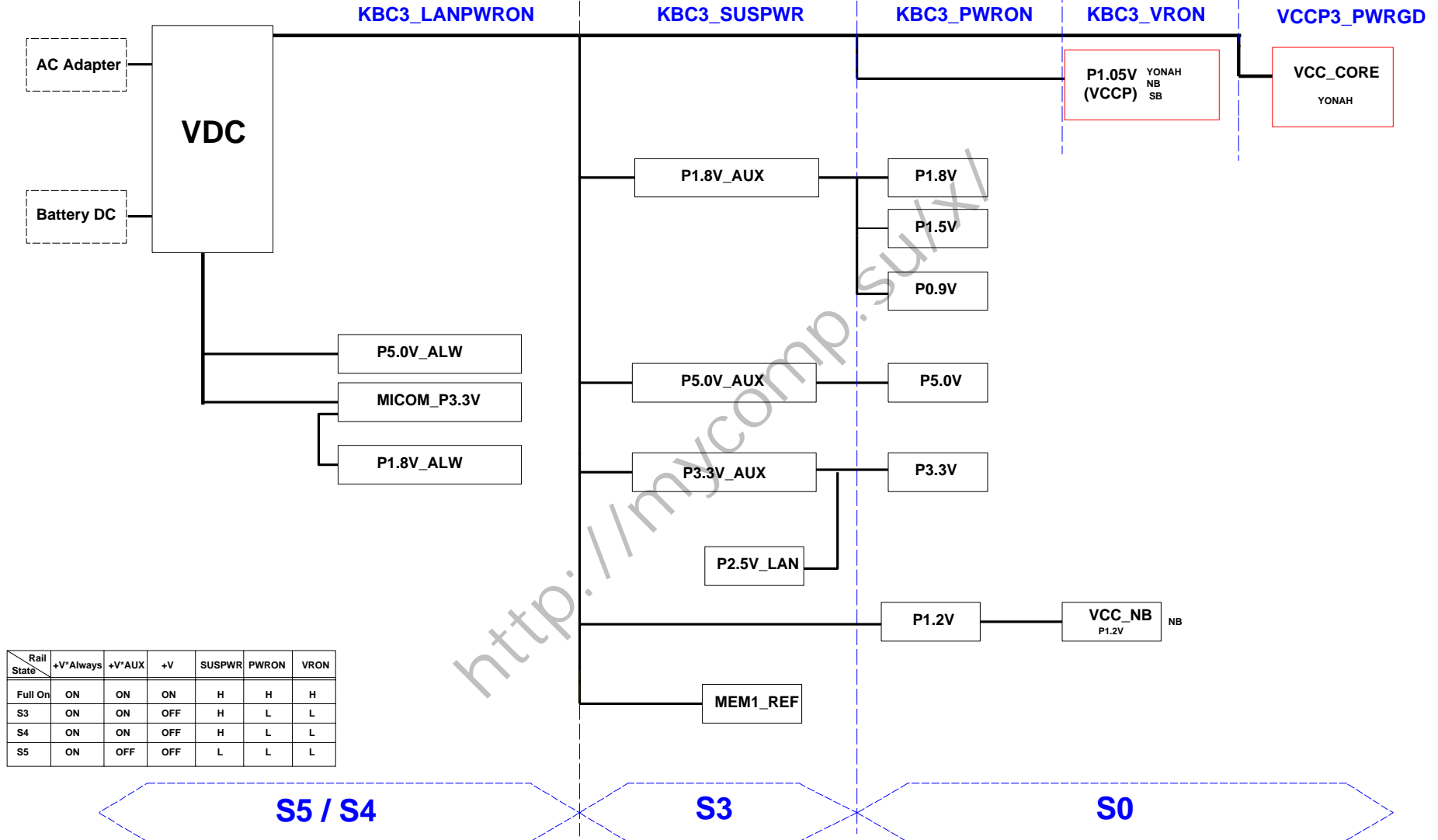


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CHECK	HJ KIM	DEV. STEP	SR	OPERATION BLOCK DIAGRAM		
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Power Diagram

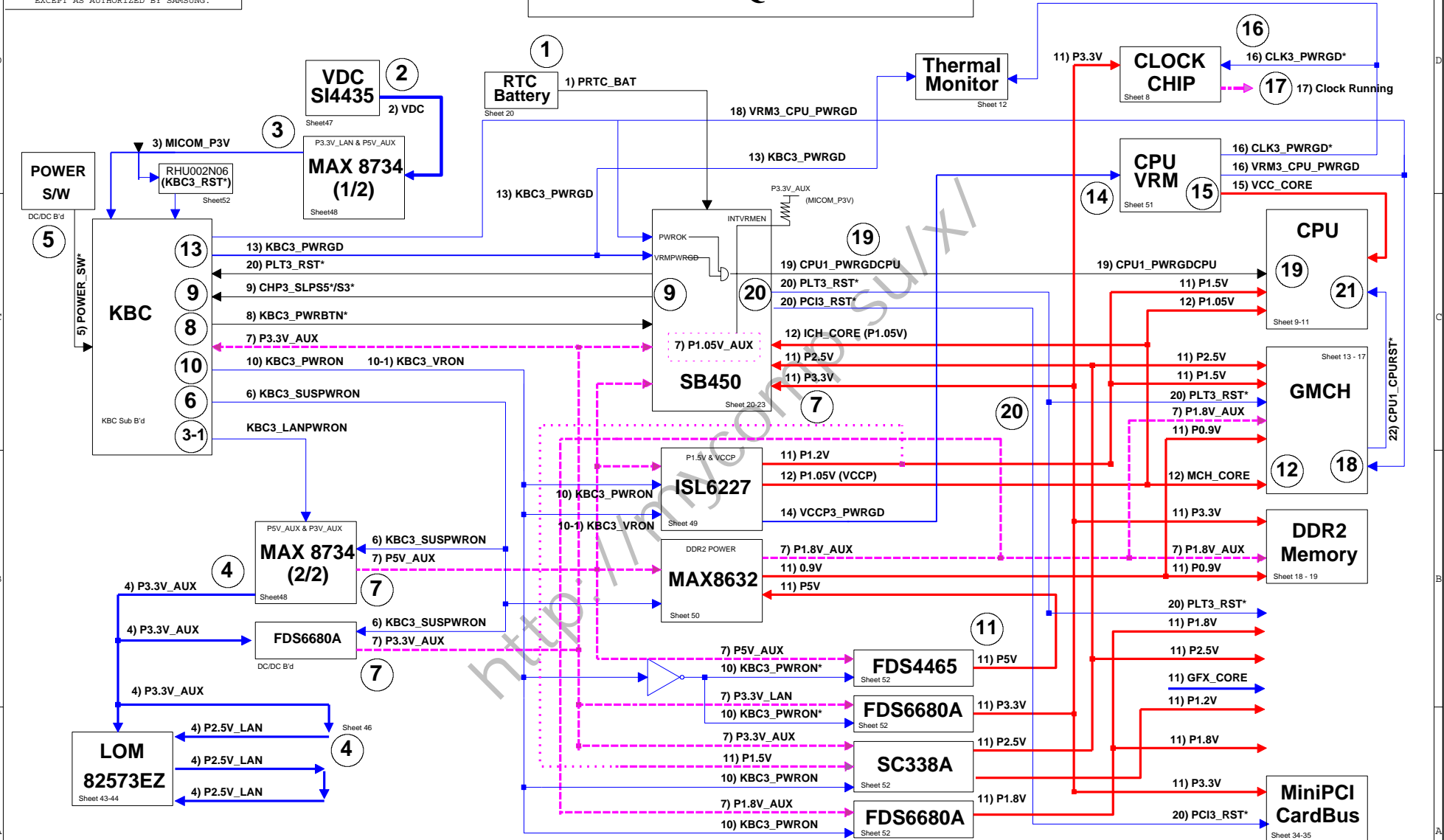


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CHECK	HJ KIM	DEV. STEP	SR	MAIN	POWER DIAGRAM	
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April 5, 2006 8:18:08 PM PAGE 3 OF 52

POWER SEQUENCE Rev. 0.8

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CHECK	HJ KIM	DEV. STEP	SR			ELECTRONICS
APPROVAL	SJ PARK	REV	1.0	POWER SEQUENCE	PART NO.	BA41-00659A
MODULE CODE		LAST EDIT		April 5, 2006 8:18:08 PM	PAGE	4 OF 52

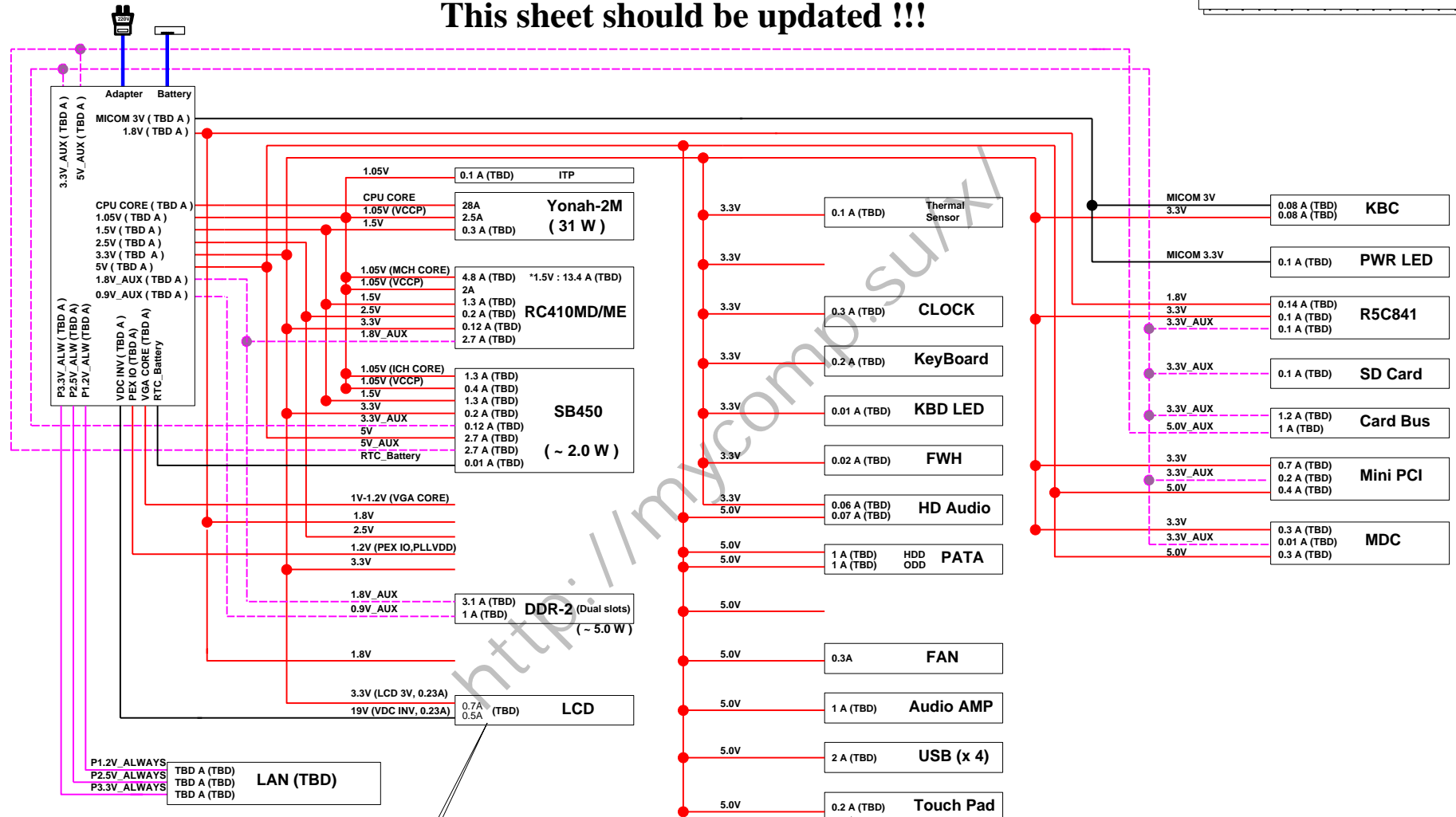
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POWER RAILS ANALYSIS

Rev. 0.8

—— S0 - S5
- - - - S0 - S3
- - - - OFF IN S3 - S5

This sheet should be updated !!!

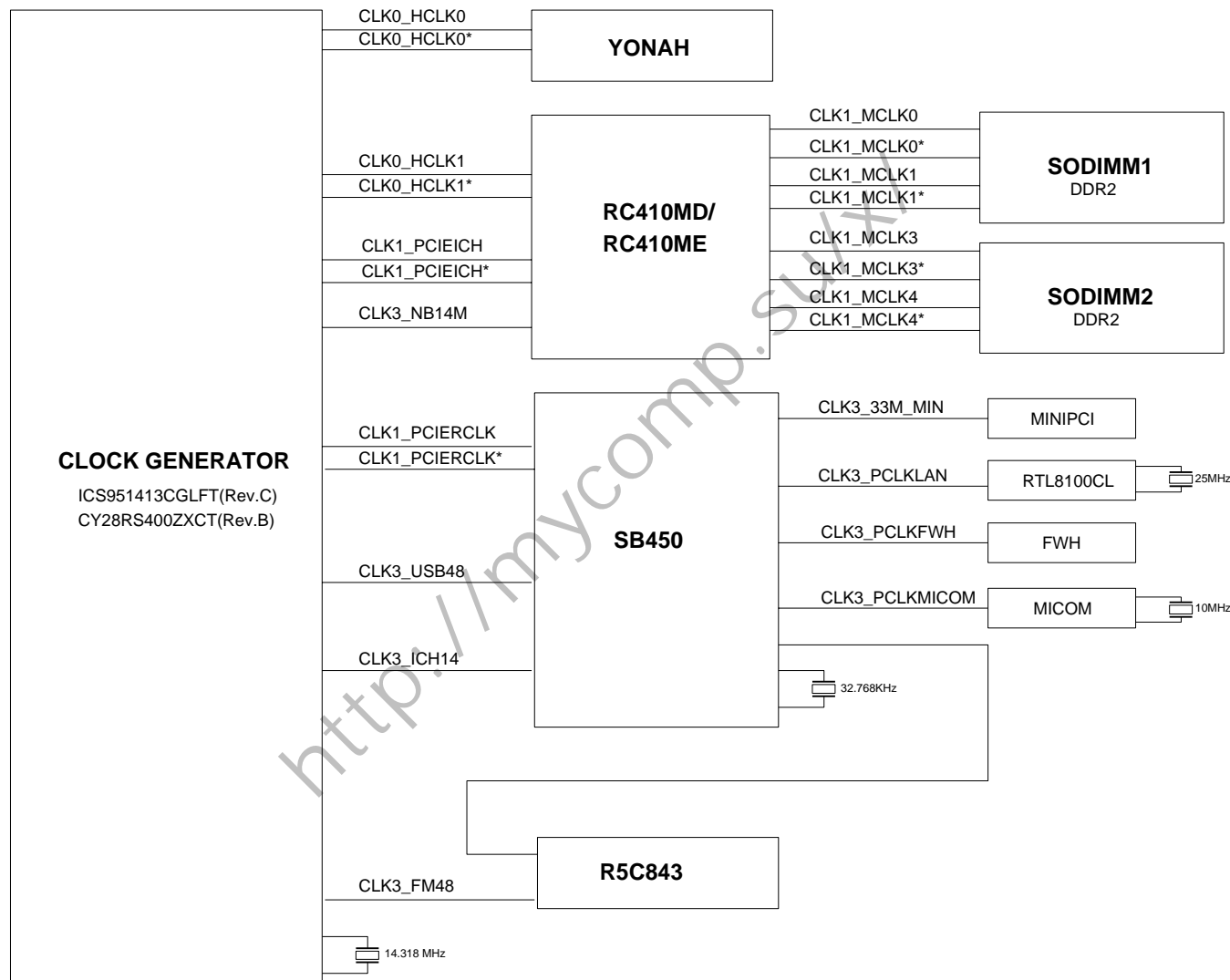


Value by Datasheet/Application notes (Value by measurement)

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II POWER BLOCK	SAMSUNG ELECTRONICS
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April 5, 2006 8:18:08 PM						PAGE 5 OF 52

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DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II CLOCK DIAGRAM	SAMSUNG ELECTRONICS PART NO. BA41-00659A
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	E, F, G
LAN	AD21	1	C
MINIPCI	AD23	2	A, B
USB	AD30(internal)	-	-
Hub to PCI	AD31(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	--
Internal MAC	AD31(internal)	-	-
AC Link	-	-	-

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB450	Real Time Clock
Crystal	10MHz	MICOM	HGS-2110B
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	25MHz	LAN	LOM

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308~1.068V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V) MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P3.3V_DTV	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_ALWS	3.3V power rail (Always On)
P2.5V_ALWS	2.5V power rail (Always On)
P1.2V_ALWS	1.2V power rail (Always On)

CPU Core Voltage Table

VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0 0	1.708 V	1 0 0 0 0 0	1.196 V
0 0 0 0 0 0	1.692 V	1 0 0 0 0 0	1.180 V
0 0 0 0 0 1	1.676 V	1 0 0 0 0 1	1.164 V
0 0 0 0 1 0	1.660 V	1 0 0 0 1 0	1.148 V
0 0 0 0 1 1	1.644 V	1 0 0 1 0 0	1.132 V
0 0 0 1 0 0	1.628 V	1 0 0 1 0 1	1.116 V
0 0 0 1 0 1	1.612 V	1 0 0 1 1 0	1.100 V
0 0 0 1 1 0	1.596 V	1 0 0 1 1 1	1.084 V
0 0 0 1 1 1	1.580 V	1 0 1 0 0 0	1.068 V
0 0 1 0 0 0	1.564 V	1 0 1 0 0 1	1.052 V
0 0 1 0 0 1	1.548 V	1 0 1 0 1 0	1.036 V
0 0 1 0 1 0	1.532 V	1 0 1 0 1 1	1.020 V
0 0 1 0 1 1	1.516 V	1 0 1 1 0 0	1.004 V
0 0 1 1 0 0	1.500 V	1 0 1 1 0 1	0.988 V
0 0 1 1 0 1	1.484 V	1 0 1 1 1 0	0.972 V
0 0 1 1 1 0	1.468 V	1 0 1 1 1 1	0.956 V
0 0 1 0 0 0	1.452 V	1 1 0 0 0 0	0.940 V
0 1 0 0 0 0	1.436 V	1 1 0 0 0 1	0.924 V
0 1 0 0 0 1	1.420 V	1 1 0 0 1 0	0.908 V
0 1 0 0 1 0	1.404 V	1 1 0 0 1 1	0.892 V
0 1 0 1 0 0	1.388 V	1 1 0 1 0 0	0.876 V
0 1 0 1 0 1	1.372 V	1 1 0 1 0 1	0.860 V
0 1 0 1 1 0	1.356 V	1 1 0 1 1 0	0.844 V
0 1 0 1 1 1	1.340 V	1 1 0 1 1 1	0.828 V
0 1 1 0 0 0	1.324 V	1 1 1 0 0 0	0.812 V
0 1 1 0 0 1	1.308 V	1 1 1 0 0 1	0.796 V
0 1 1 0 1 0	1.292 V	1 1 1 0 1 0	0.780 V
0 1 1 0 1 1	1.276 V	1 1 1 0 1 1	0.764 V
0 1 1 1 0 0	1.260 V	1 1 1 1 0 0	0.748 V
0 1 1 1 0 1	1.244 V	1 1 1 1 0 1	0.732 V
0 1 1 1 1 0	1.228 V	1 1 1 1 1 0	0.716 V
0 1 1 1 1 1	1.212 V	1 1 1 1 1 1	0.700 V

HFM Voltage
770:1.26V~1.372V
730,740,750,760:1.26~>1.356V

I C / SMB Address

Devices	Address	Hex	Bus
SB450	Master	-	SMBUS Master
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-410 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0, 1	SYSTEM PORT A
2, 3	SYSTEM PORT B
4	BLUETOOTH
5	DMB

System Power States

CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.
CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is retained, and refreshes continue. All clocks stop except RTC clock.
CHP3_SLPS4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.
CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

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CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0	BOARD INFORMATION	PART NO.	BA41-00659A
MODULE CODE		LAST EDIT		Apr 15, 2006 8:18:08 PM	PAGE	7 OF 52

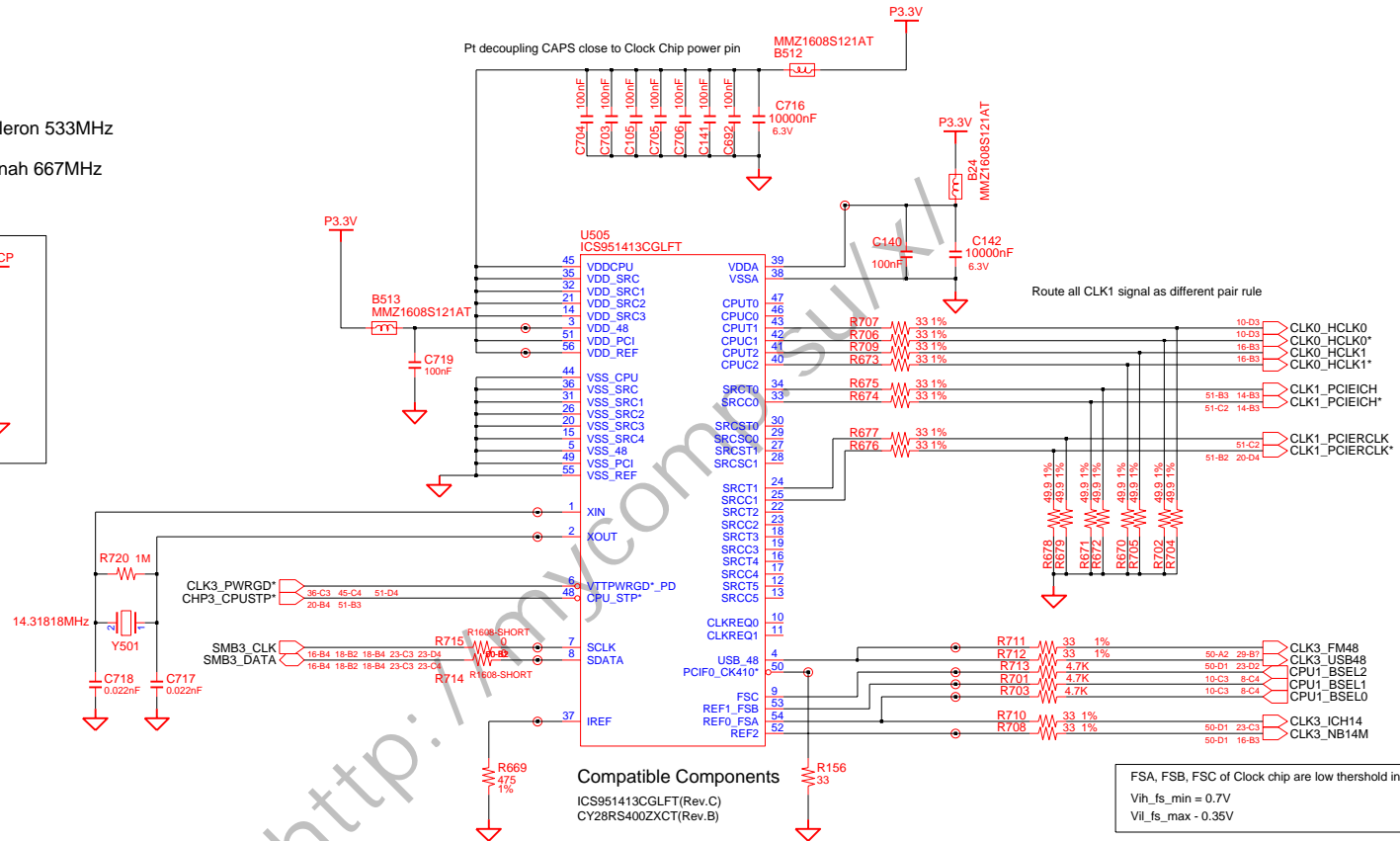
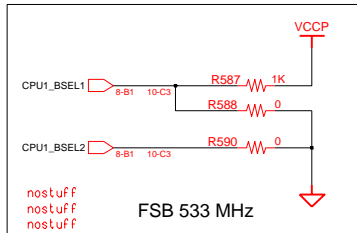
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FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

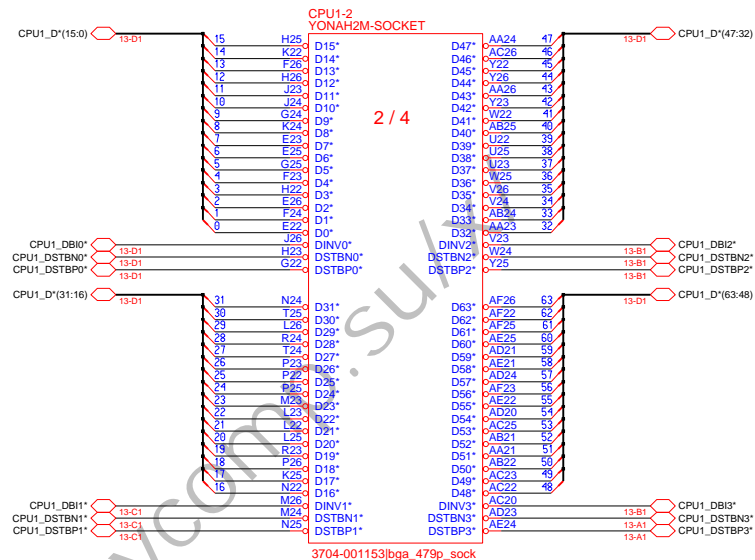
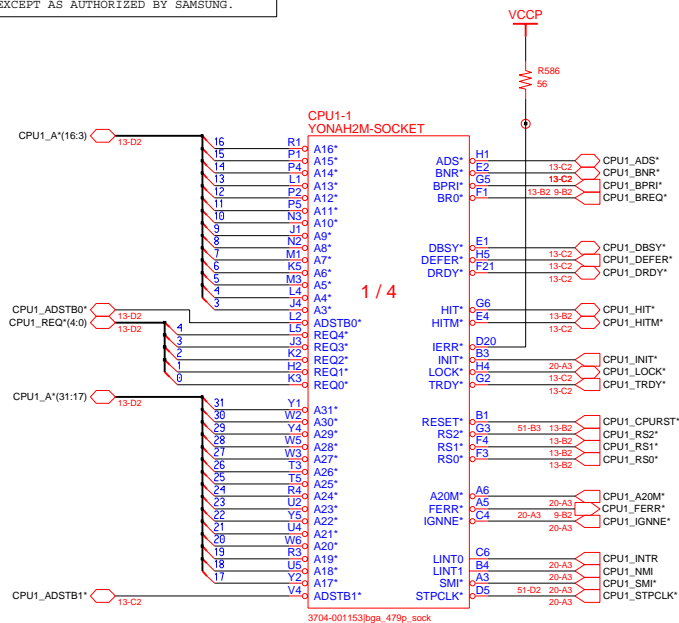
Celeron 533MHz

Yonah 667MHz



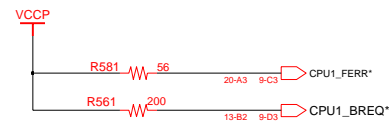
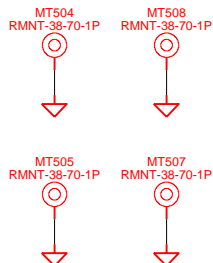
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**NOTE

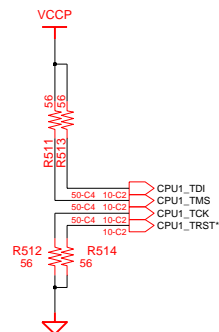
RHE SUPPORTER



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN YONAH CPU (1/3)	SAMSUNG ELECTRONICS
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APPROVAL	SJ PARK	REV	1.0			
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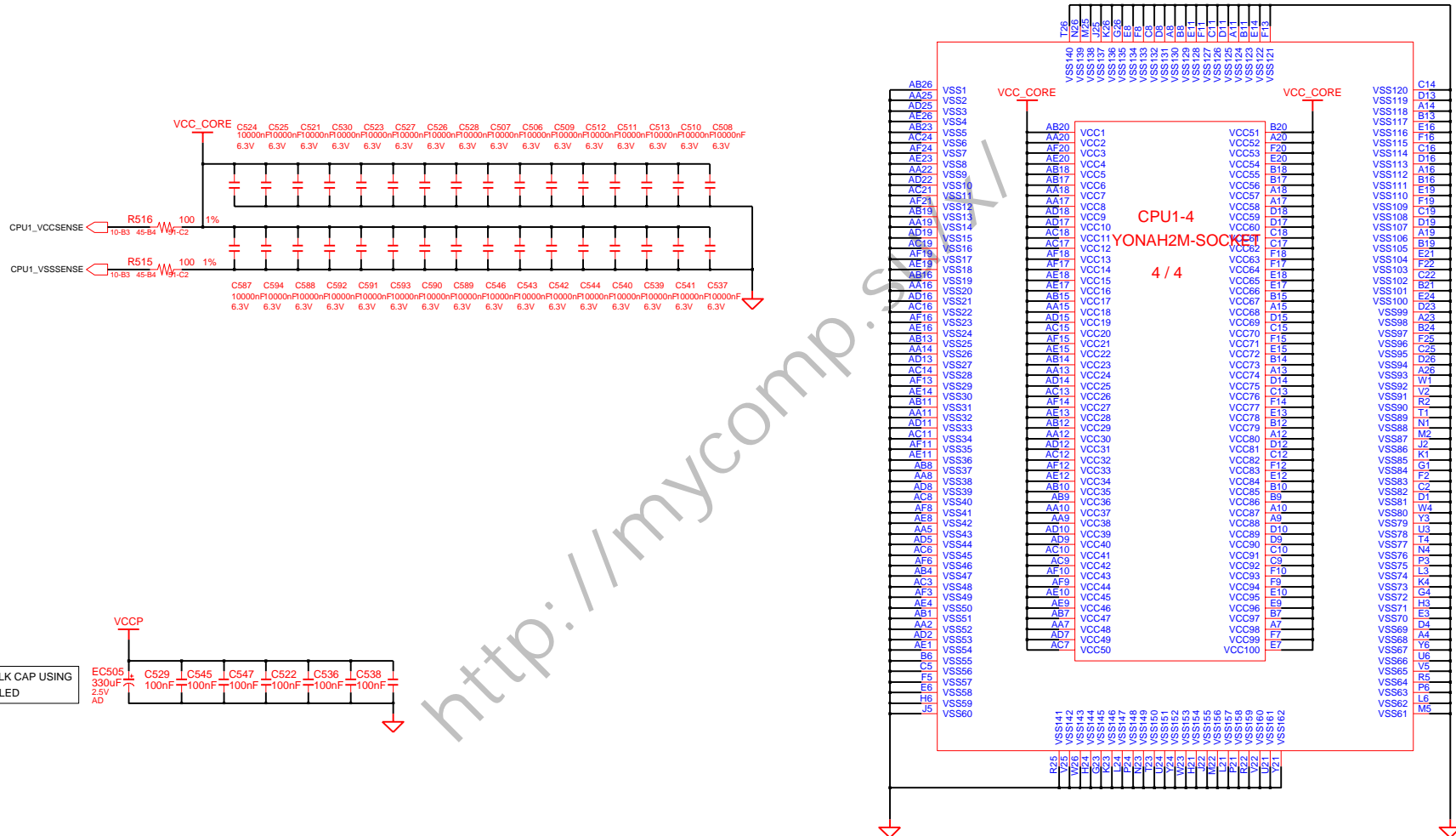
*Yonah Processor (2.33 GHz / 800 MHz : TBD)



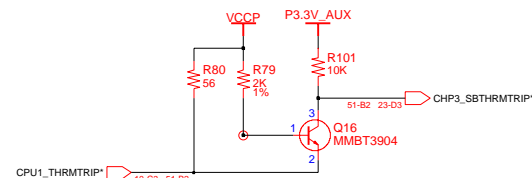
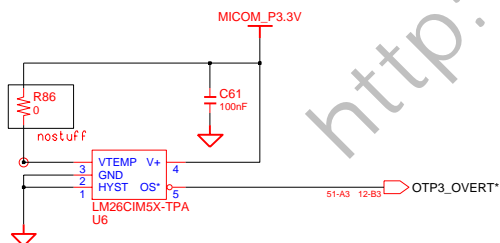
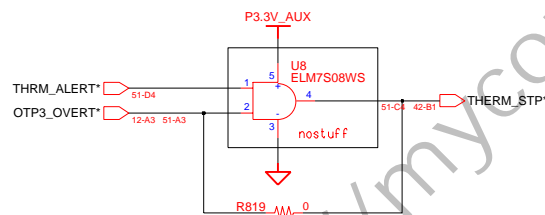
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- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND

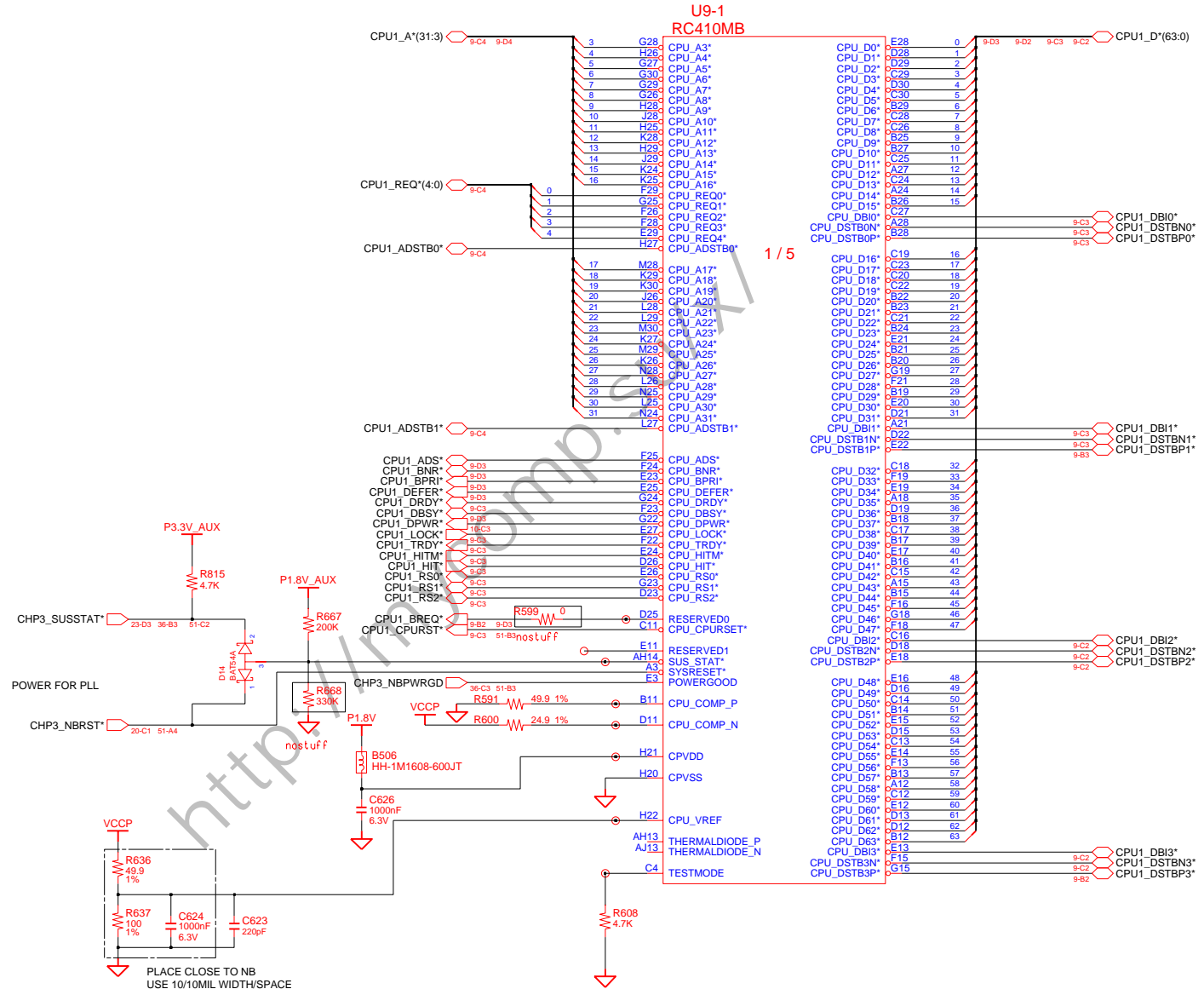


D:/users/mobile62/mentor/firenze2/firenze2_SR1.0_0405

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DUCT + FAN SUPPORTER

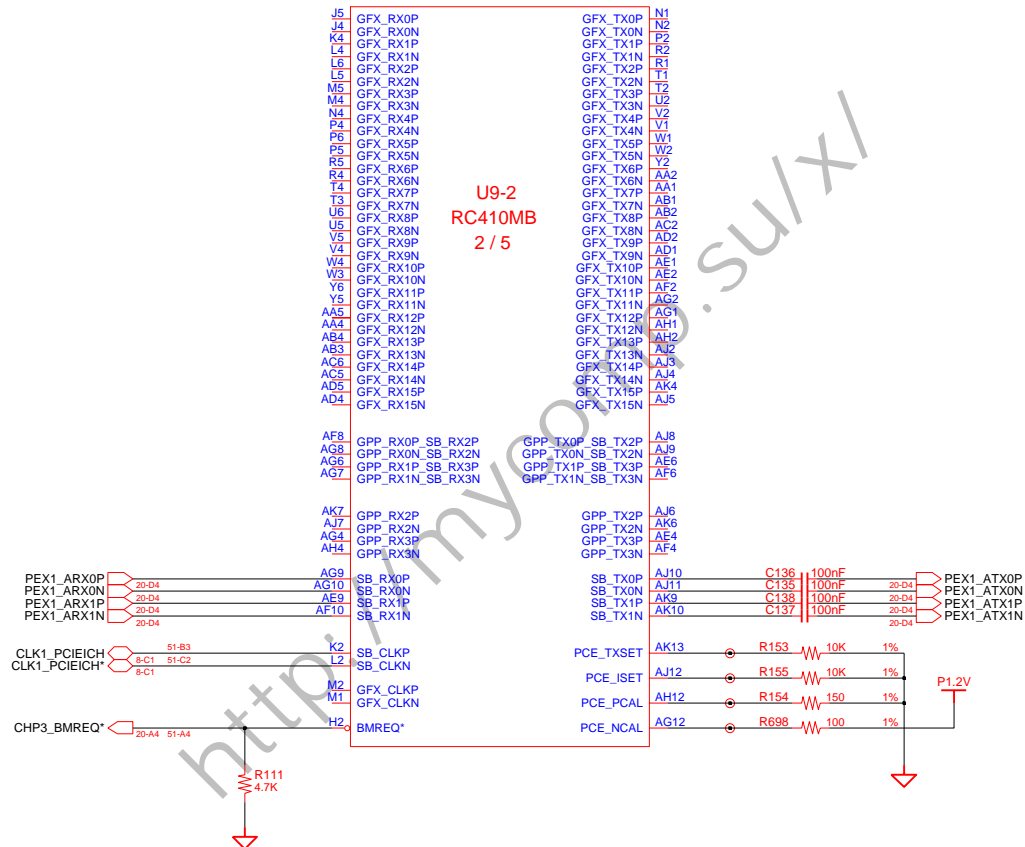


PLACE CLOSE TO NB
USE 10/10MIL WIDTH/SPACE

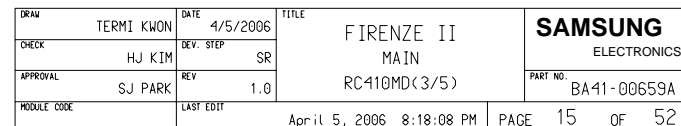
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APPROVAL	SJ PARK	REV	1.0	RC410MD(1/5)		
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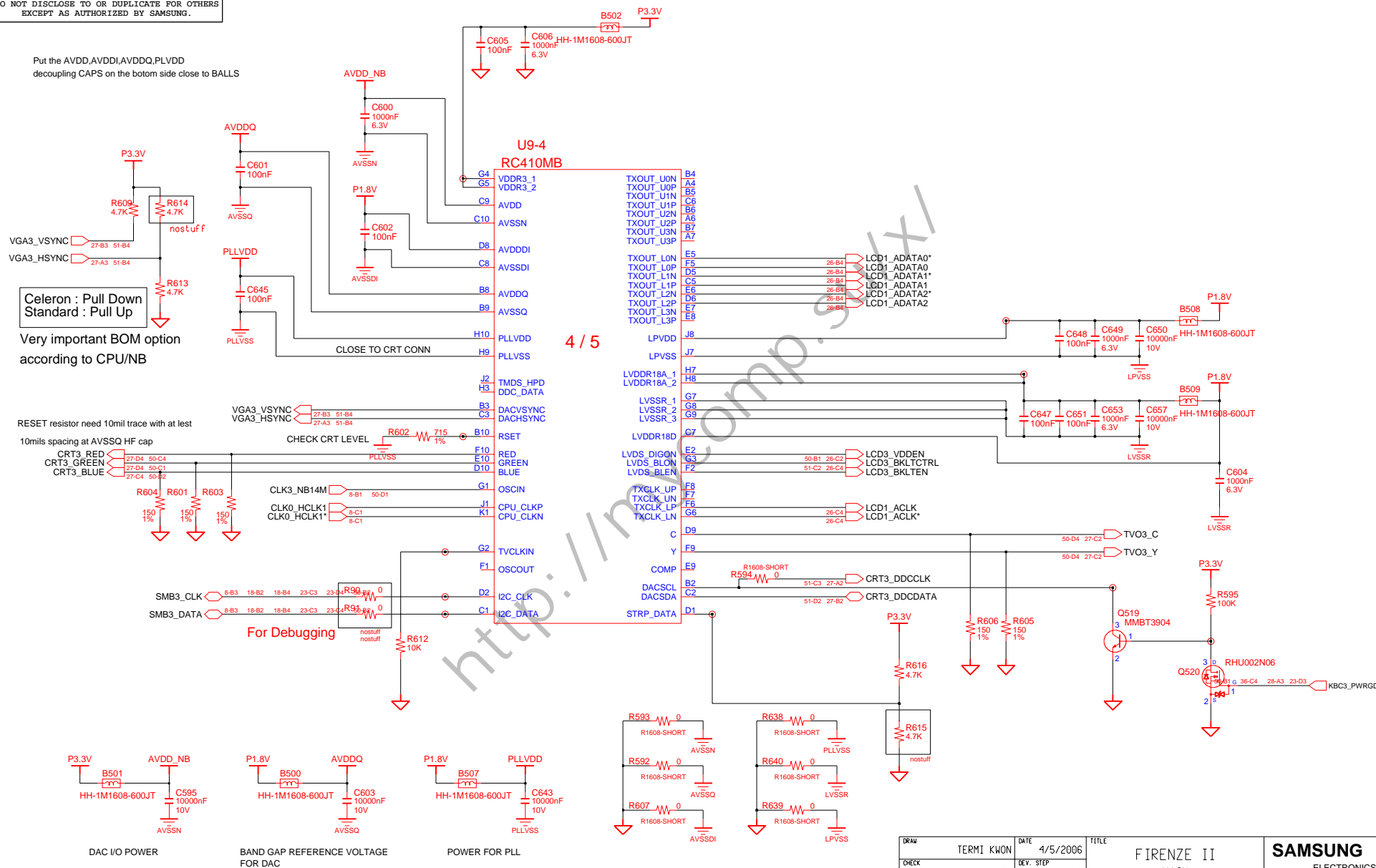
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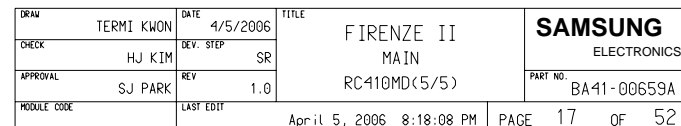
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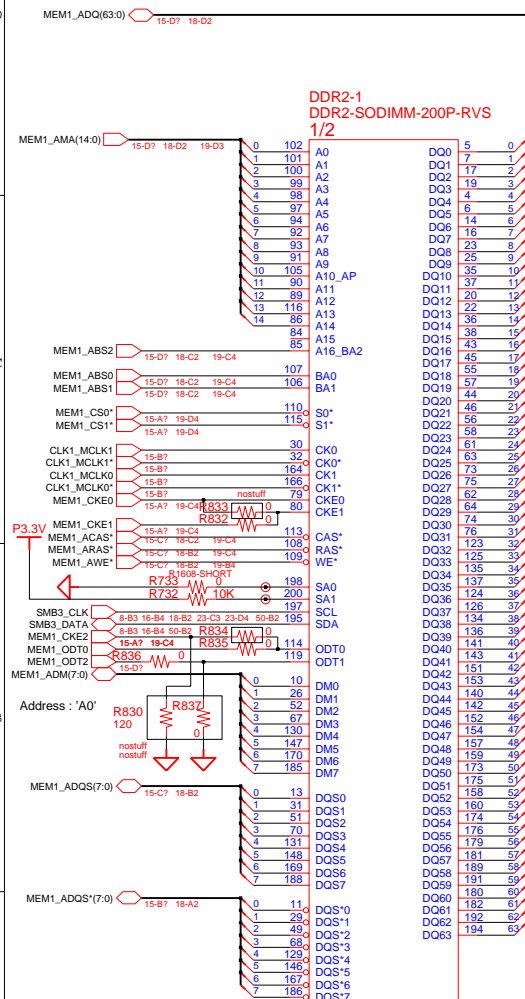


Put the AVDD,AVDDI,AVDDQ,PLVDD
decoupling CAPS on the botom side close to BALLS

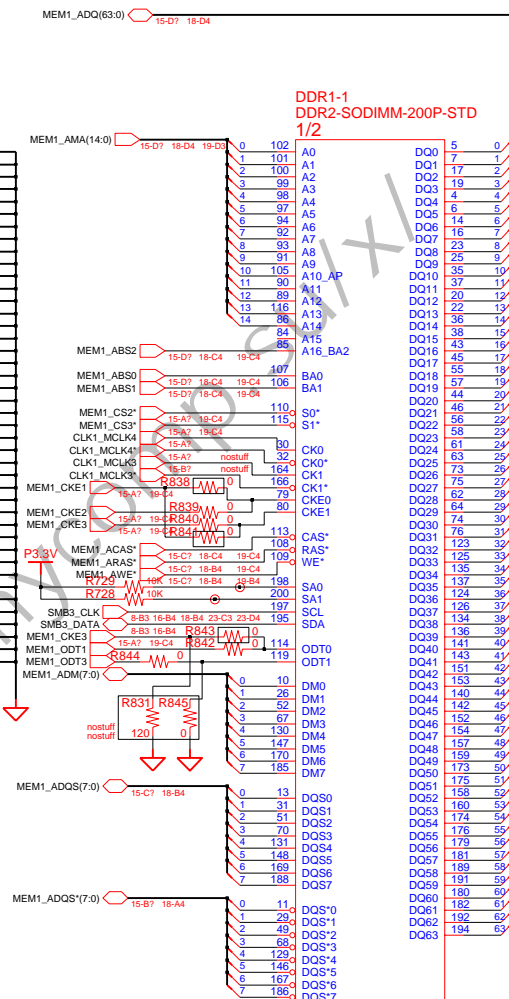


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MODULE CODE	LAST EDIT		April 5, 2006 8:18:08 PM				PAGE	16
						PART NO.	BA41-00659A	



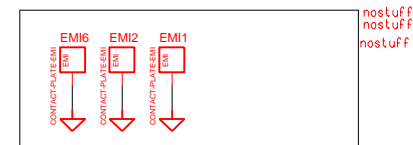
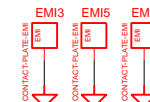
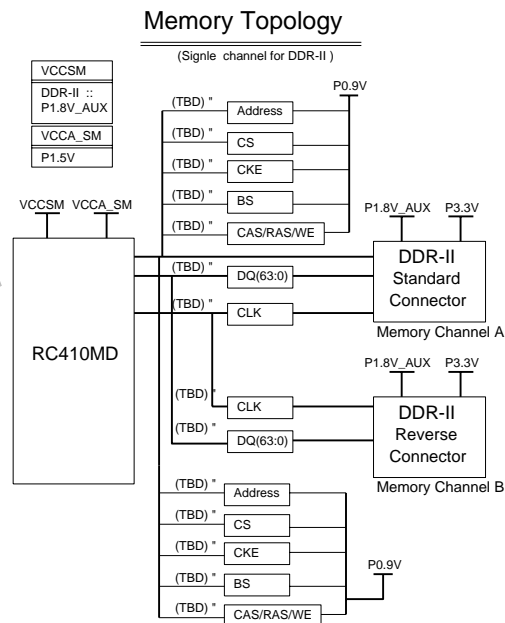


J4 Height : 5.2mm

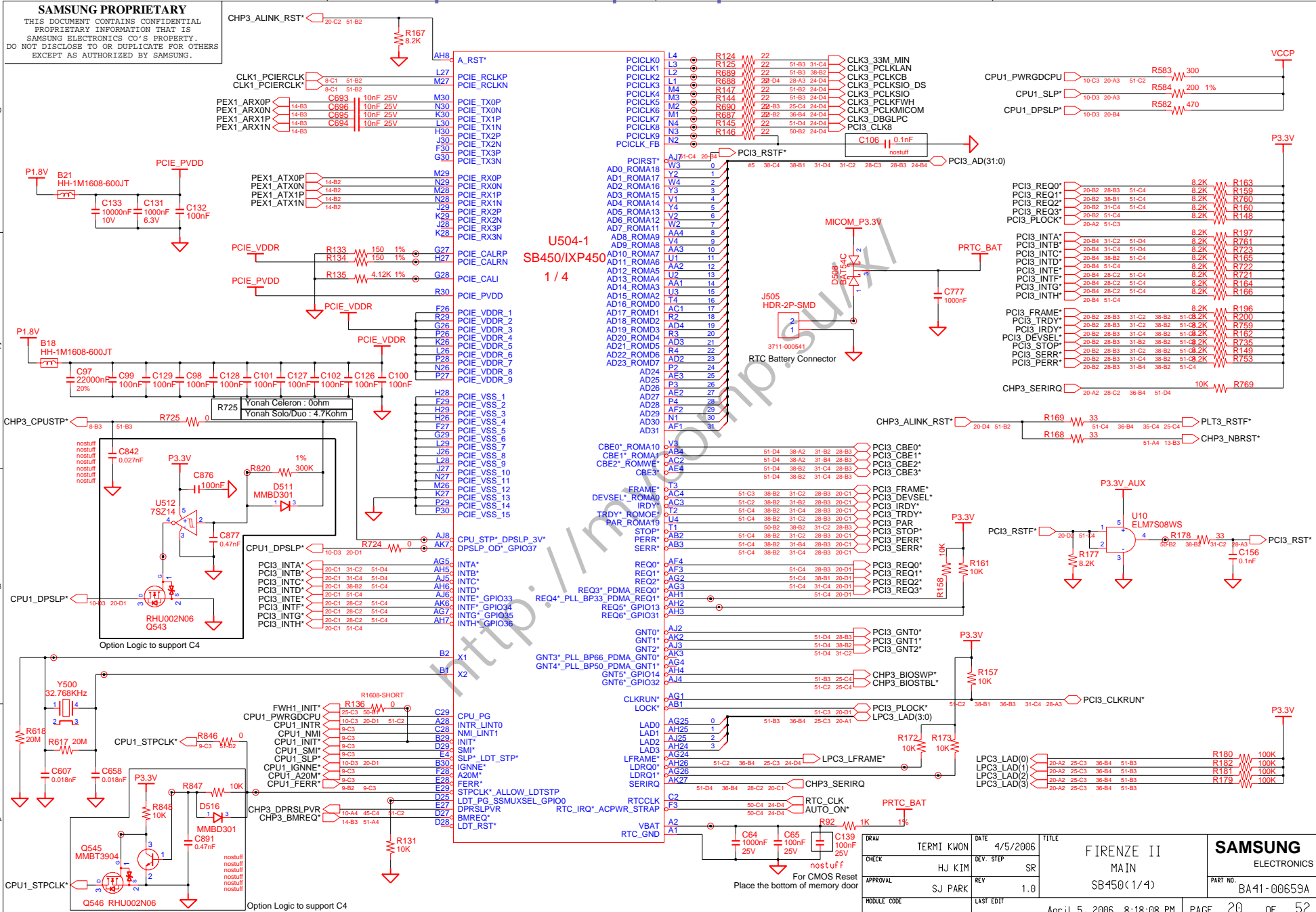


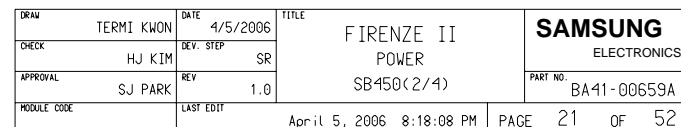
DDR1 Height : 9.2mm

DRAM	TERM1 KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG	
CHECK	HJ KIM	DEV. STEP	SR		MAIN	ELECTRONICS	
APPROVAL	SJ PARK	REV	1.0		DDR2 - SODIMM	PART NO.	BA41-00659A
MODULE CODE		LAST EDIT	April 5, 2006 8:18:08 PM	PAGE	18	OF	52



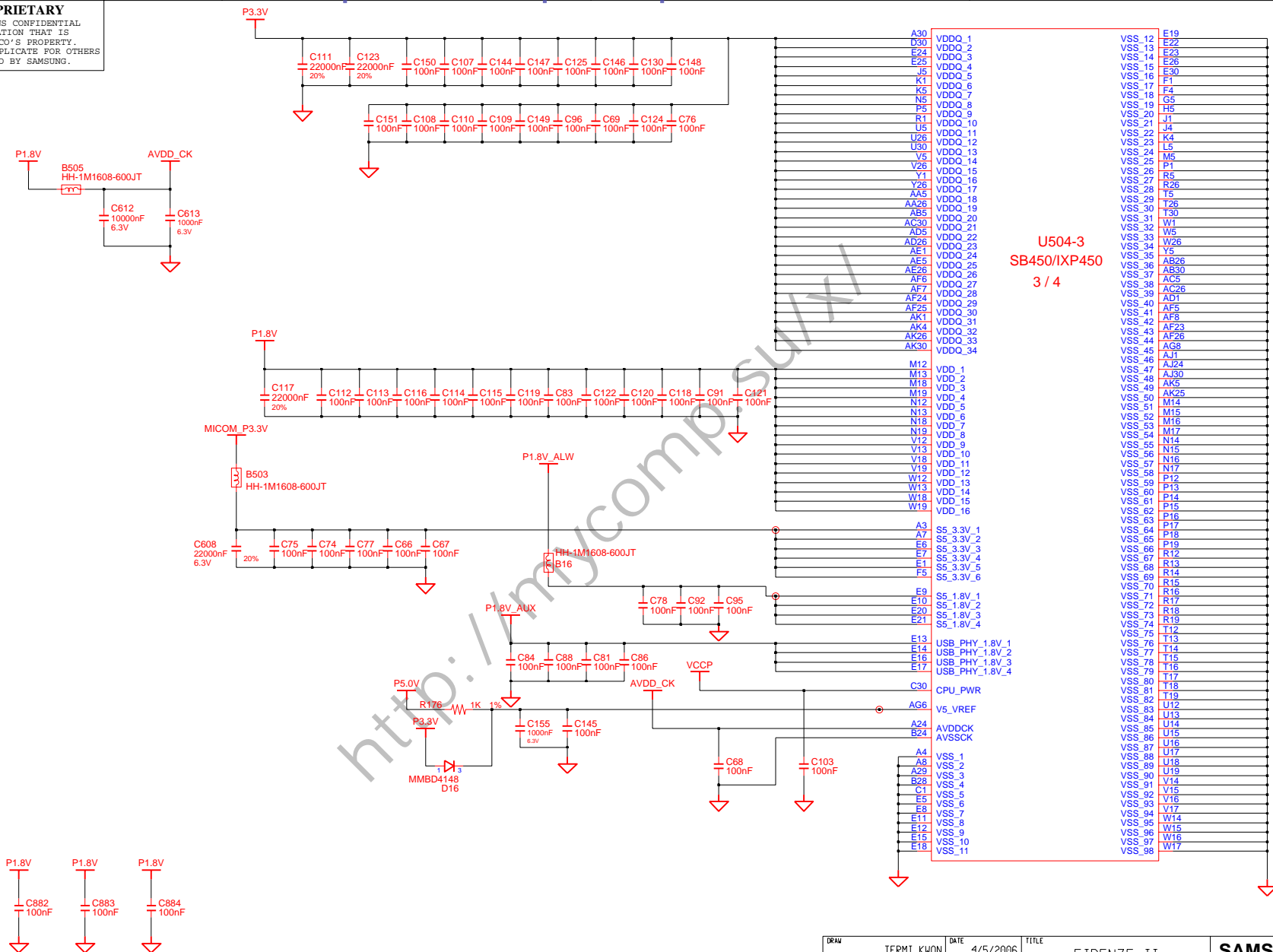
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MODULE CODE	LAST EDIT		April 5, 2006 8:18:08 PM			PAGE	19	OF 52





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April 5, 2006 8:18:08 PM						PAGE 22 OF 52



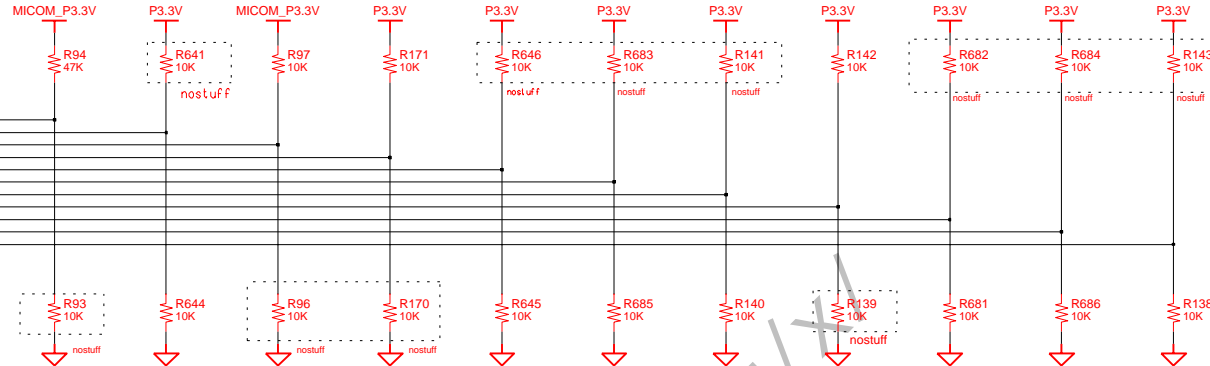
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REQUIRED SYSTE STRAPS

AUTO_ON*
AC_SDOUT
RTC_CLK
LPC3_LFRAME*
CLK3_PCLKCB
CLK3_PCLKSIO_DS
CLK3_PCLKSIO
CLK3_PCLKFWH
CLK3_PCLKMICOM
CLK3_DBG LPC
PCI3_CLK8

20-A2 50-C4
23-B4 50-C4
20-A2 50-C4
20-A2 25-C3 36-B4 51-C2
20-D2 26-A3 51-D4
20-D2 51-B2
20-D2 51-B3
20-D2 25-C4 51-B3
20-D2 36-B4 51-B2
20-D2 51-D4
20-D2 50-B2

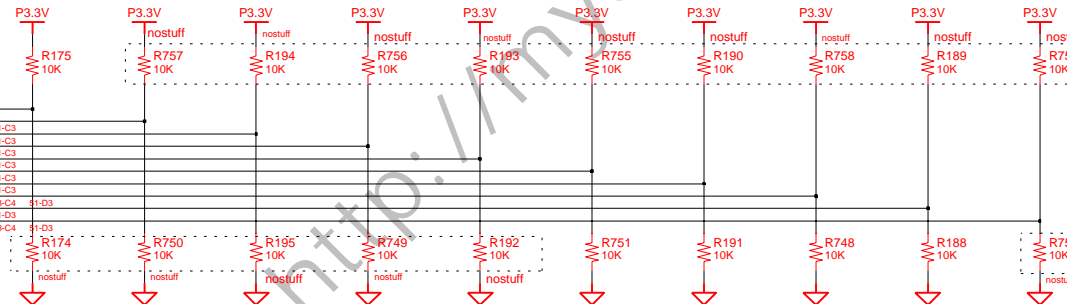


	AUTO_ON	AC_SDOUT	RTC_CLK	LPC3_FRAME	PCI3_CLK2	PCI3_CLK3	PCI3_CLK4	PCI3_CLK5	PCI3_CLK6	PCI3_CLK7, PCI3_CLK8
STRAP HIGH	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	Enable thermtrip* on power up	48MHZ XTAL MODE	USB PHY PWRDOWN DISABLE	USE USB PLL	PCI-E lane auto detect	CPU I/F = KB	ROM TYPE H.H = PCI ROM H.L = LPCROM I LPC ADDRESS MAPPED BELOW 1 M
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	EXRERNAL RTC	Disable thermtrip* on power up	48MHZ OSC MODE	USB PHY PWRDOWN ENABLE	BYPASS USB PLL	Force PCI-E to lane2	CPU I/F = P4	LPC ADDRESS MAPPED TO TOP-4G L.H = LPC ROM II LL = FWH ROM

DEBUS STRAPS

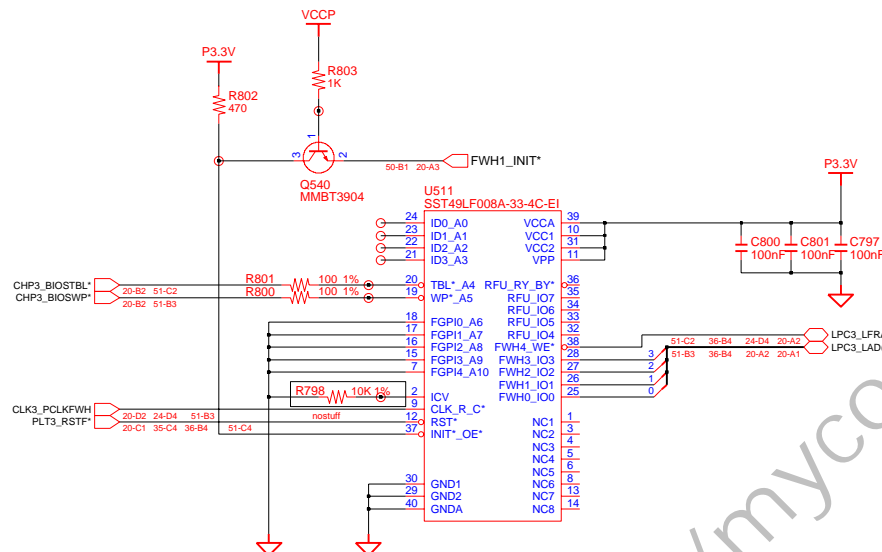
IDE5_DACK*
PCI3_AD(31)
PCI3_AD(30)
PCI3_AD(29)
PCI3_AD(28)
PCI3_AD(27)
PCI3_AD(26)
PCI3_AD(25)
PCI3_AD(24)
PCI3_AD(23)

21-D2 35-C3 50-B1
20-D2 28-C3 31-D4 38-C4 51-C3
20-D2 28-C3 31-D4 38-C4 51-C3
20-D2 28-C3 31-D4 38-C4 51-C3
20-D2 28-C3 31-D4 38-C4 51-C3
20-D2 28-C3 31-D4 38-C4 51-C3
20-D2 28-C3 31-D4 38-C4 51-C3
20-D2 28-C3 31-D4 38-C4 51-C3
20-D2 28-C3 31-D4 38-C4 51-C3
20-D2 28-C3 31-D4 38-C4 51-C3



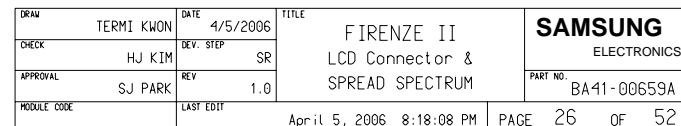
	IDE5_DACK*	PCI3_AD(31)	PCI3_AD(30)	PCI3_AD(29)	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	BYPASS EEPROM PCIE STRAPS	RESERVED
STRAP LOW	USE SHORT RESET					USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0	STRAPS		
MODULE CODE		LAST EDIT				



02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSOR IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT. PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
	WITH INITIAL POST VALUE	88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT.EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT.	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUPT CONTROLLER	9E	ENABLE H/W INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPEMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TEST CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
40	INIT. INTERRUPT VECTOR	BA	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DA	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DC	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	89	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY * PRESS SETUP*	92	JUMP TO USER PATCH 2
5C	TEST RAM BETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

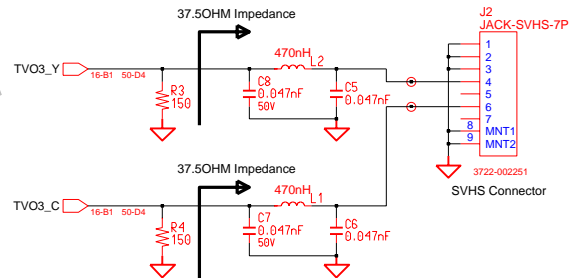
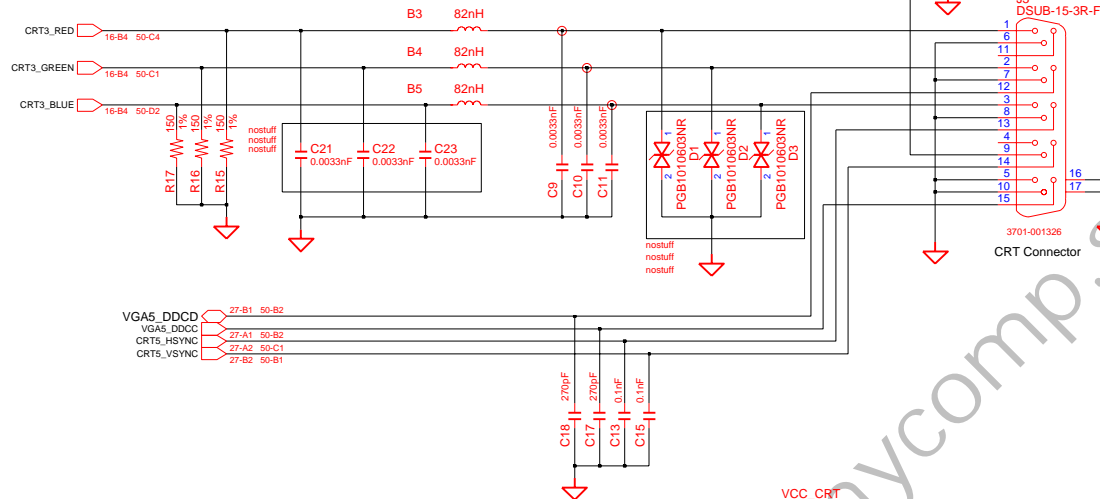
DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN FIRMWARE HUB	SAMSUNG ELECTRONICS	
CHECK	HJ KIM	DEV. STEP	SR				
APPROVAL	SJ PARK	REV	1.0				
MODULE CODE	LAST EDIT		April 5, 2006 8:18:08 PM				PAGE
				PART NO.		BA41-00659A	



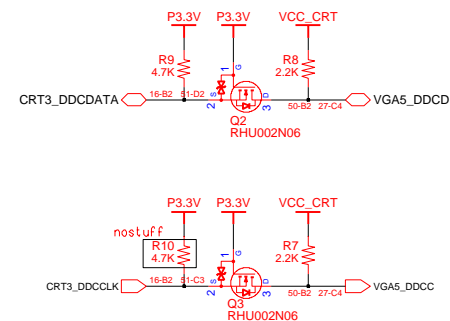
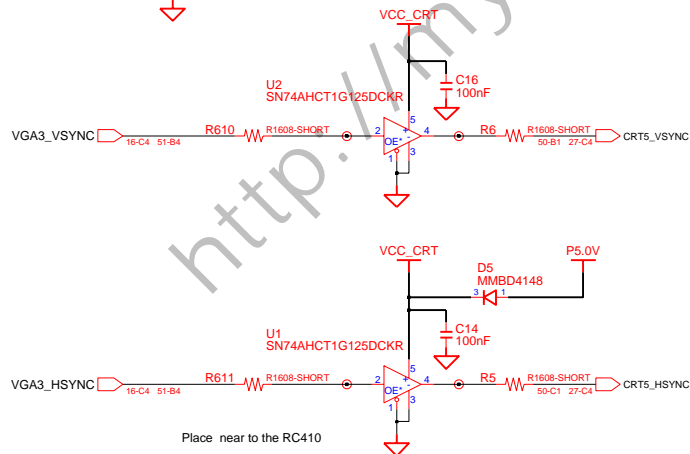
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CRT CONNECTOR

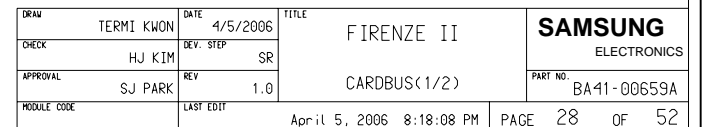


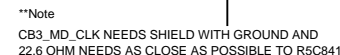
TV-OUT(S-VHS, COMPOSIT)

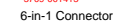


Place near to the RC410

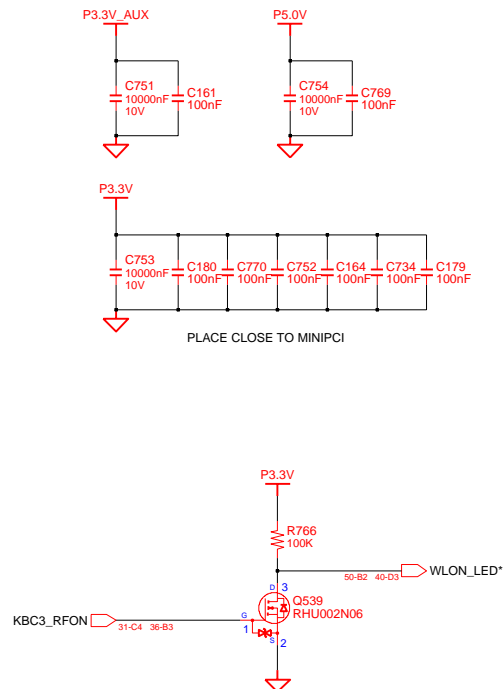
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CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0		CRT AND TV-OUT	
MODULE CODE		LAST EDIT		April 5, 2006 8:18:08 PM	PAGE 27 OF 52	



D:/users/mobile62/mentor/firenze2/firenze2_SR1.0_0405



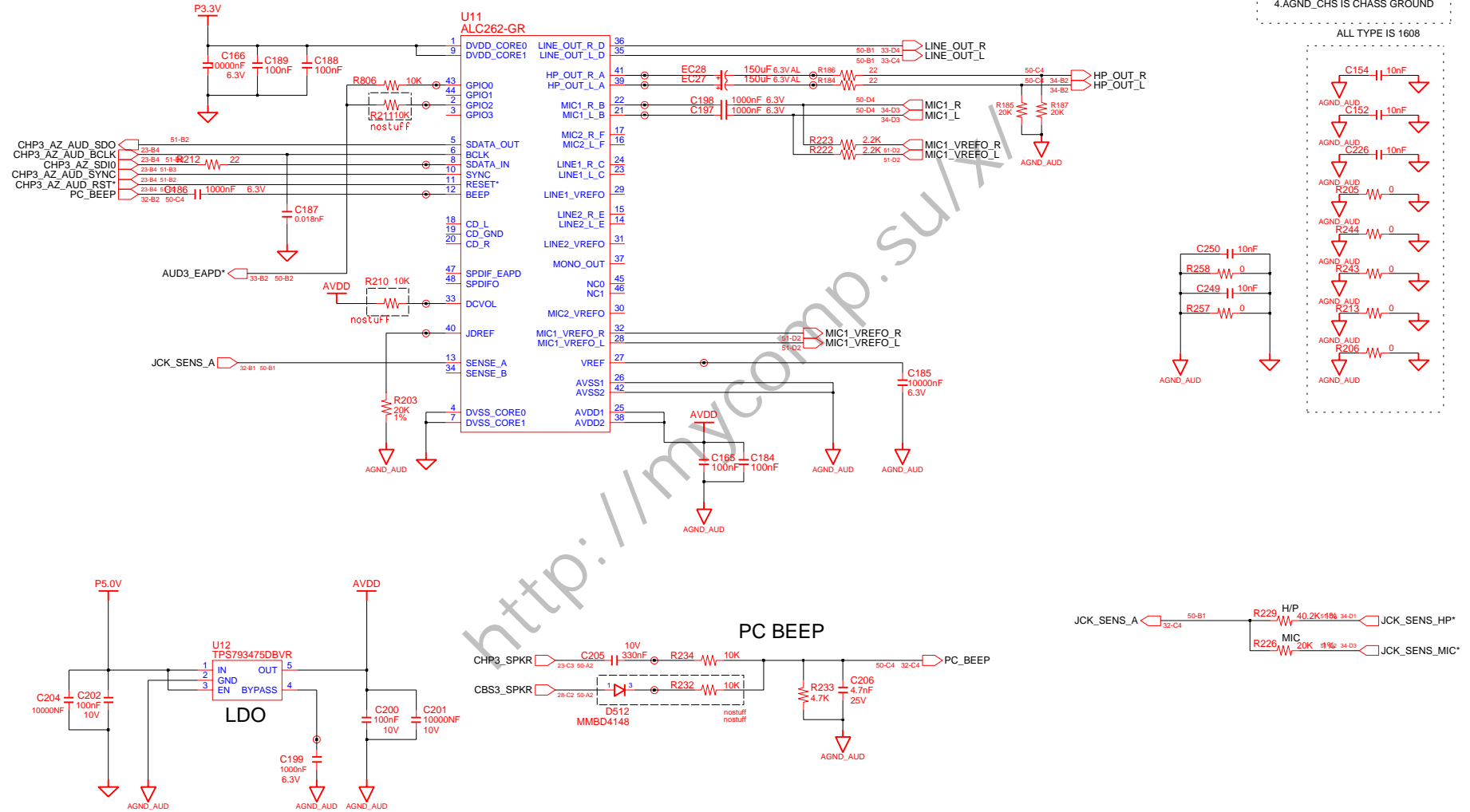
COM-22C-015(1996.6.5) REV. 3



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN MINI PCI	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 5, 2006 8:18:08 PM			
				PAGE	31	OF 52

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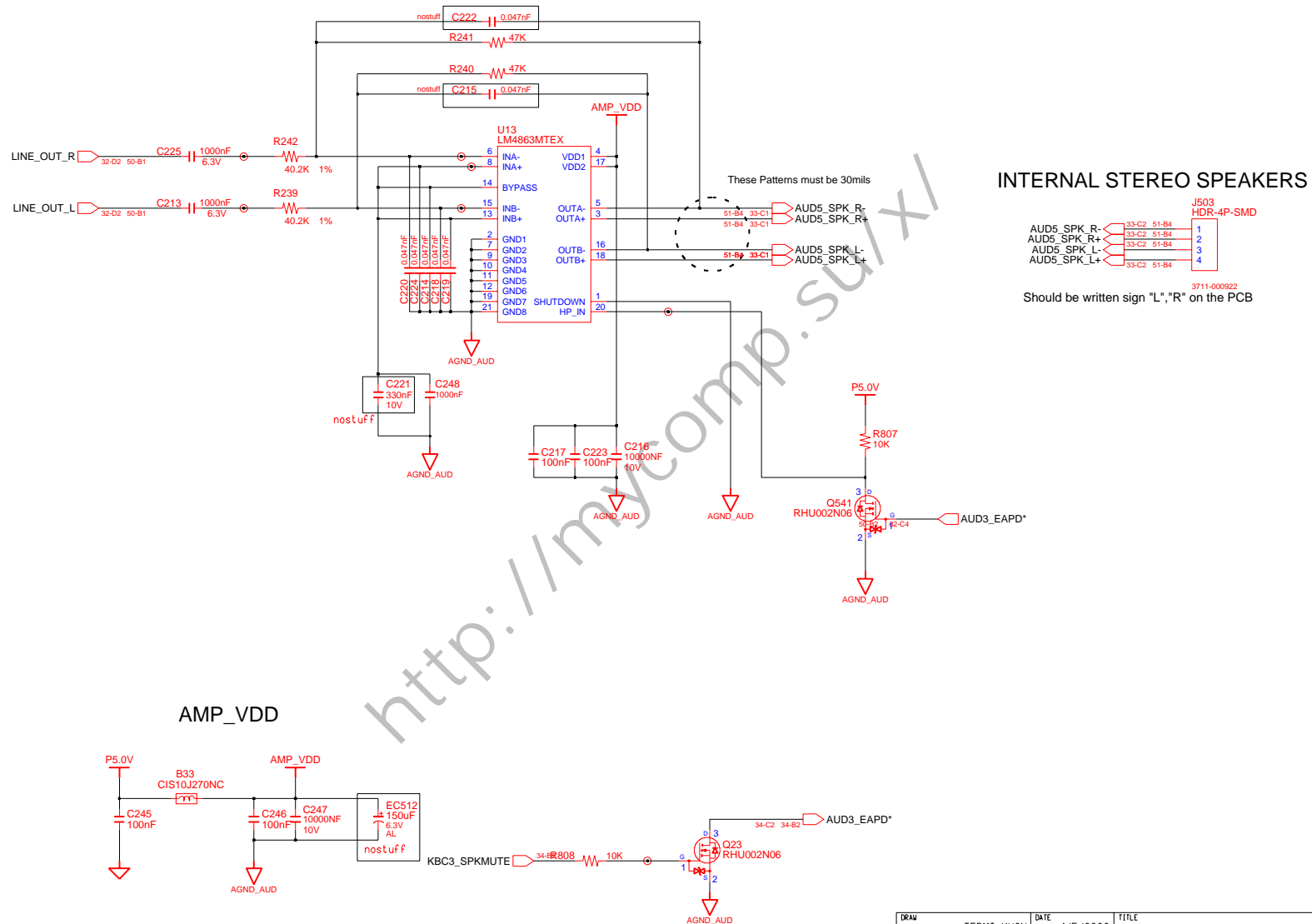
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DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN AUDIO CODEC	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR			PART NO. BA41-00659A
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 5, 2006 8:18:08 PM	PAGE	32	OF 52

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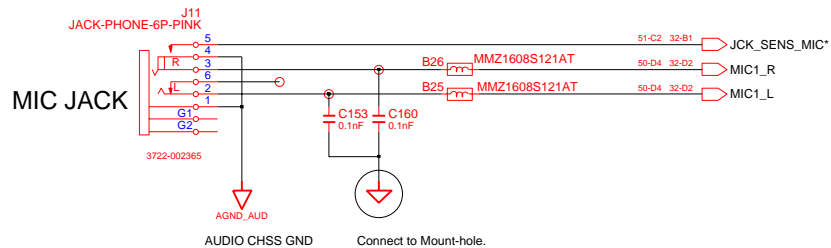
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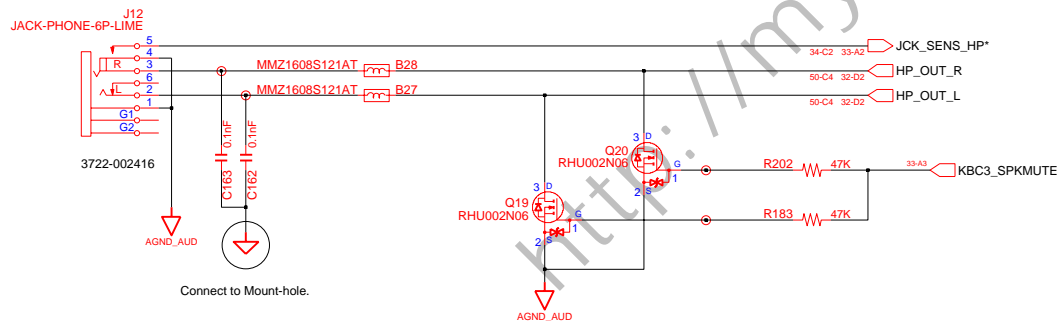
DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN LIMITER & AMP	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR			PART NO. BA41-00659A
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT		April 5, 2006 8:18:08 PM	PAGE 33 OF 52	

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HEADPHONE



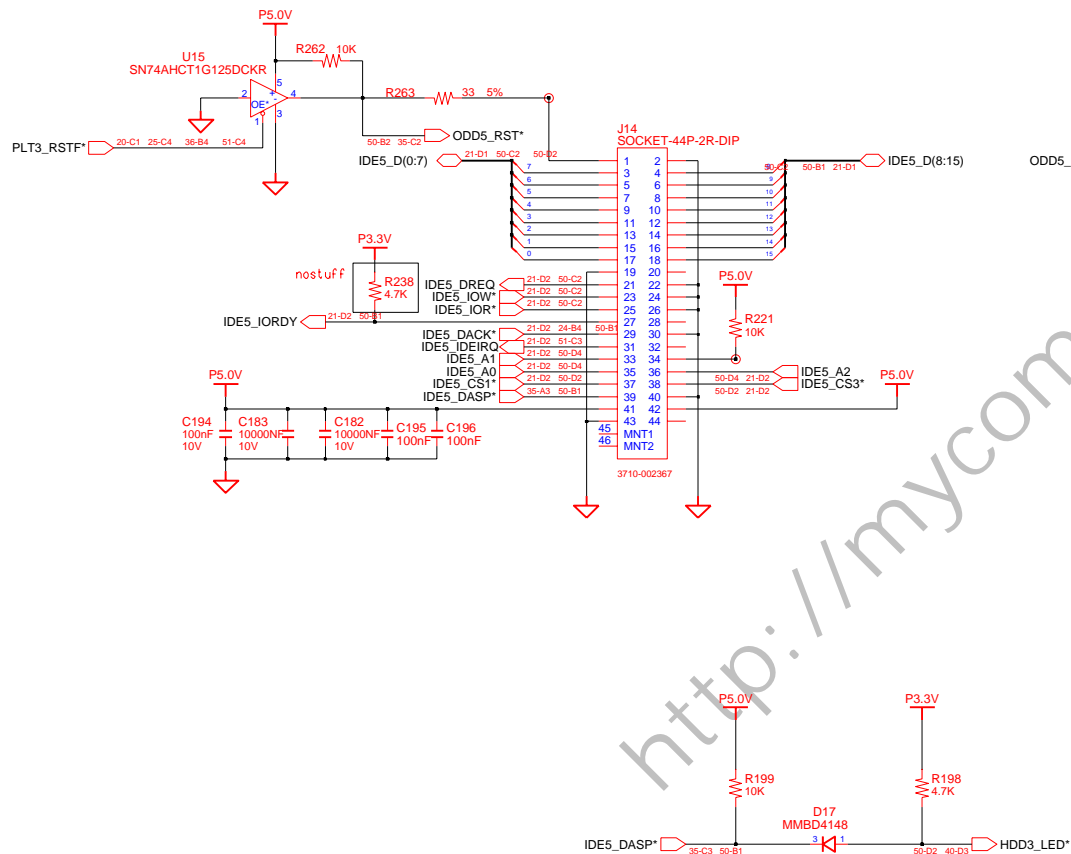
The traces led to Audio Jacks have the width over 10mil

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR		MAIN	
APPROVAL	SJ PARK	REV	1.0		UPPER & AUDIO CONN	
MODULE CODE	undefined	LAST EDIT		April 5, 2006 8:18:08 PM	PAGE 34 OF 52	

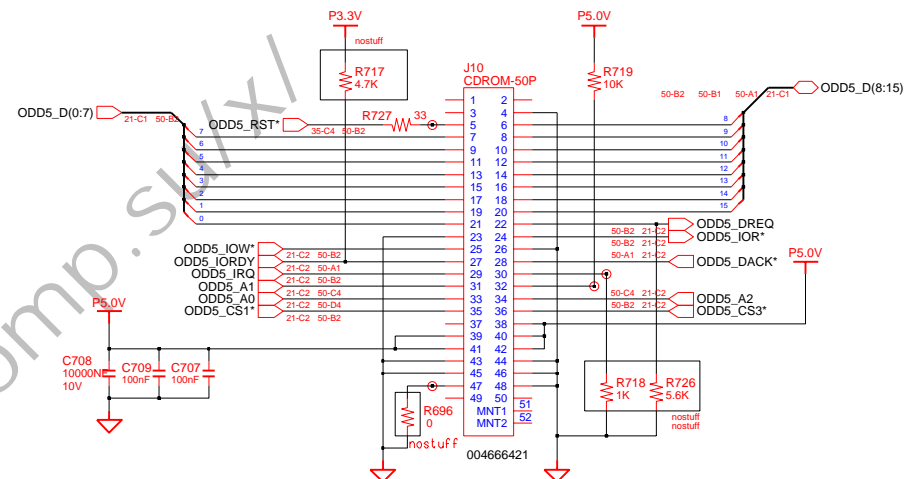
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Main to HDD



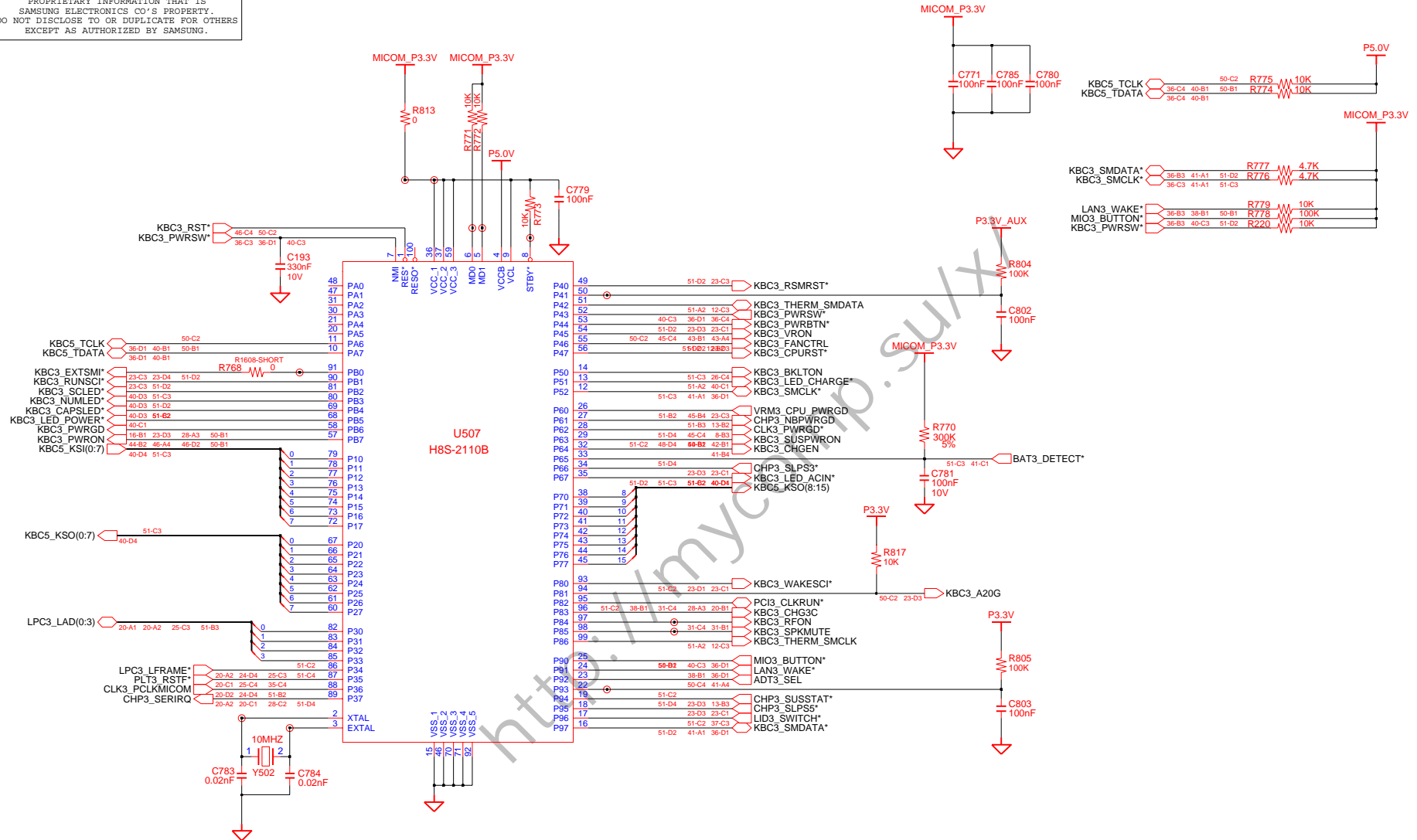
Main to ODD



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II POWER HDD & ODD	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR			PART NO. BA41-00659A
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT		April 5, 2006 8:18:08 PM	PAGE 35 OF 52	

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The removed signal compared from 144pin

KBC5_CAL_THRM*
THRM_ALERT*
LCD3_BKLTON
FAN3_FDBACK*
THERM_STP*

MICOM Crisis Update

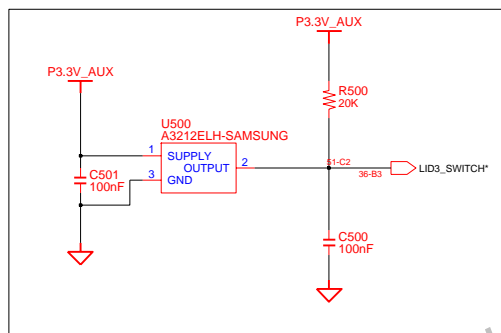
Condition: P90=P91=P92=High(MICOM_P3V)
MD0=MD1=Low(0V)
Serial Port: P84 & P85

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II POWER MICOM	SAMSUNG ELECTRONICS
CHECK	HJ KTM	DEV. STEP	SR			PART NO. BA41-00659A
APPROVAL	SU PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 5, 2006 8:18:08 PM	PAGE	36	OF 52

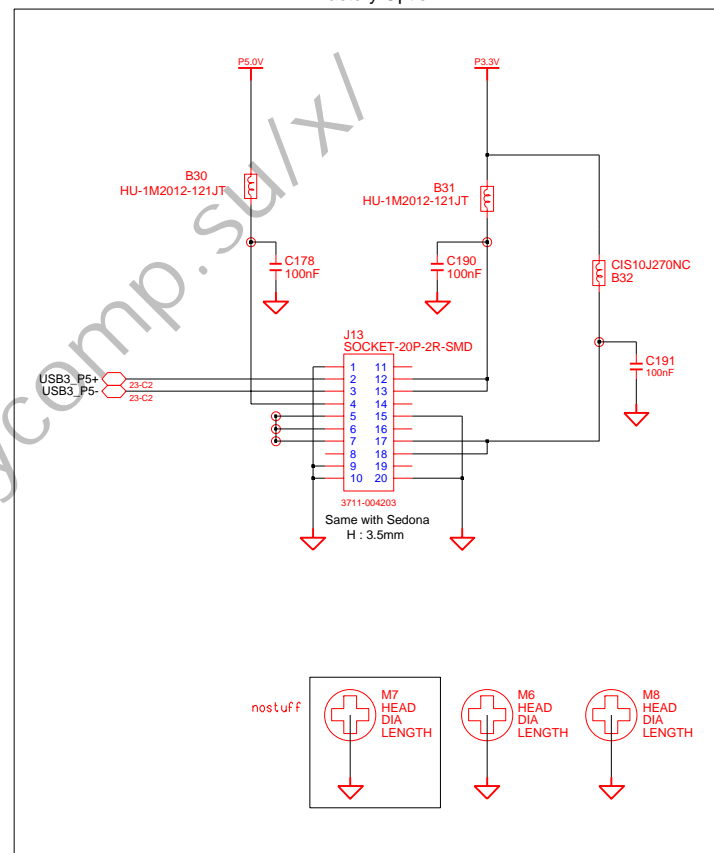
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LID SWITCH



DMB
Factory Option

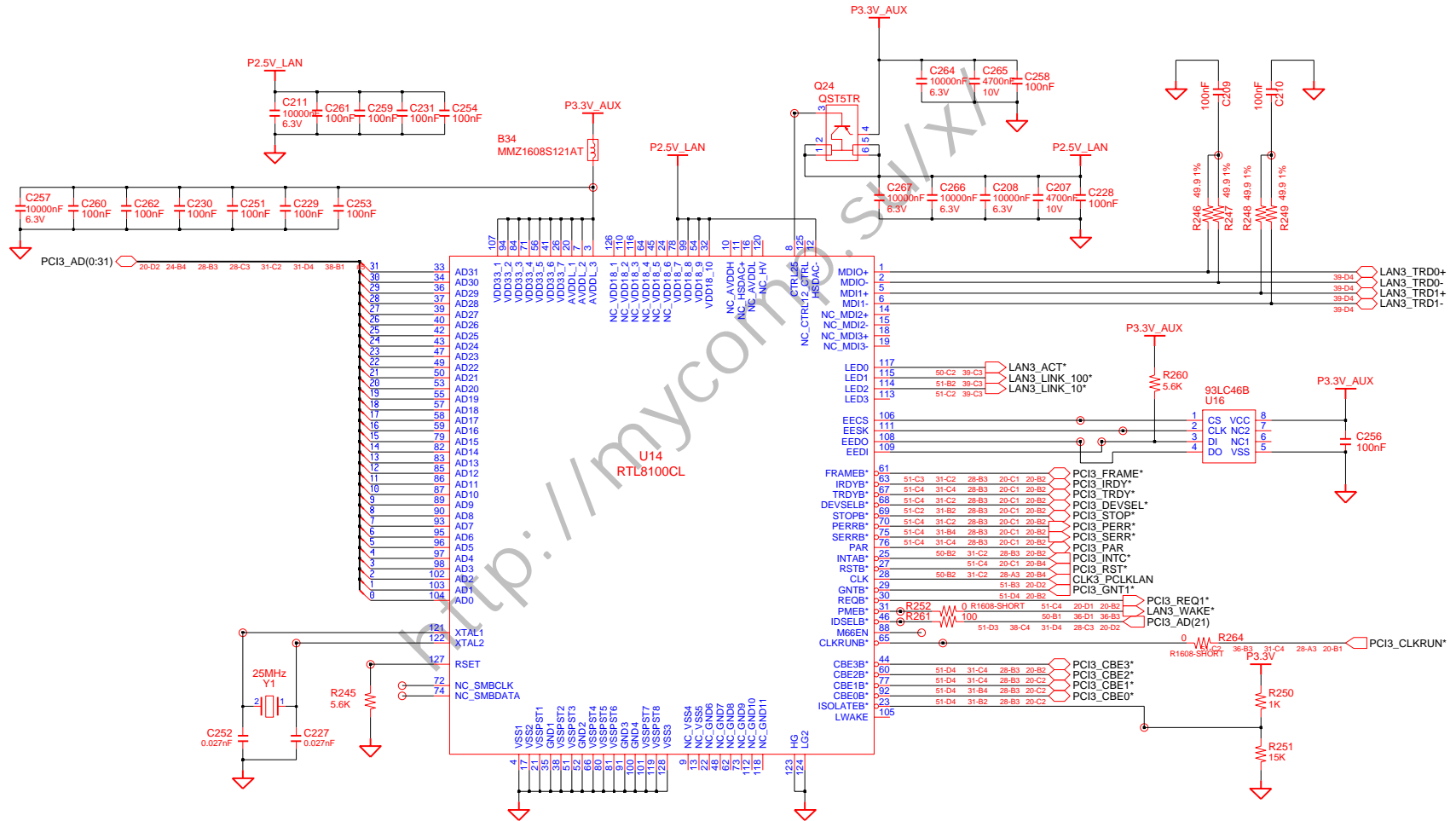


DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR		MAIN	
APPROVAL	SJ PARK	REV	1.0		LPC	
MODULE CODE	undefined	LAST EDIT		April 5, 2006 8:18:08 PM	PAGE 37 OF 52	

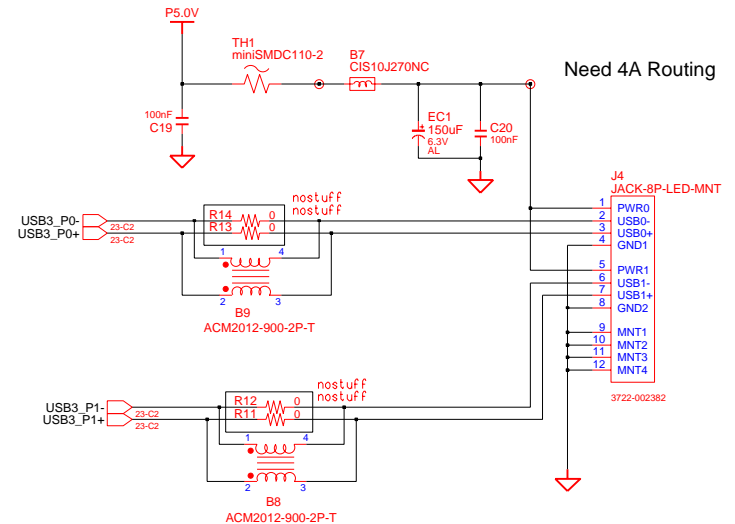
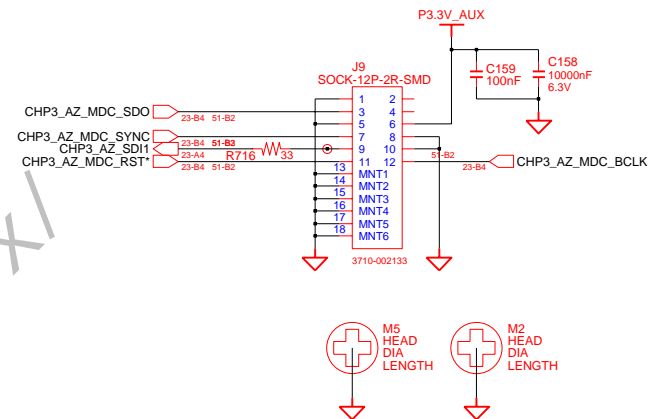
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LAN Controller (Only 10/100M)



MDC Connector

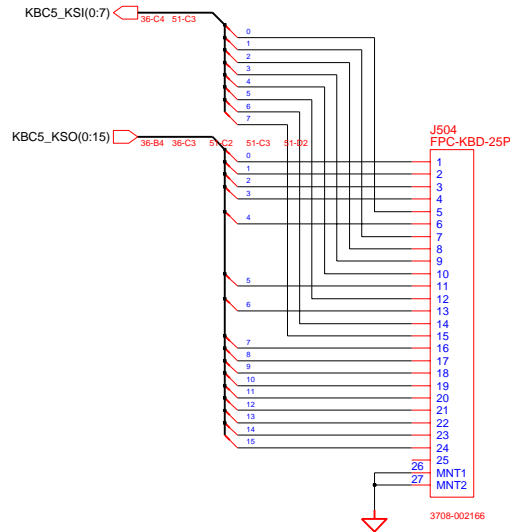


DRAW		TERM1 KWON		DATE		4/5/2006		TITLE		FIRENZE II		SAMSUNG ELECTRONICS	
CHECK		HJ KIM		REV. STEP		SR		MAIN		LAN & USB0 & MODEM Conn.			
APPROVAL		SJ PARK		REV		1.0		PART NO.		BA41-00659A			
MODULE CODE		undefined		LAST EDIT		April 5, 2006 8:18:08 PM				PAGE		39 OF 52	

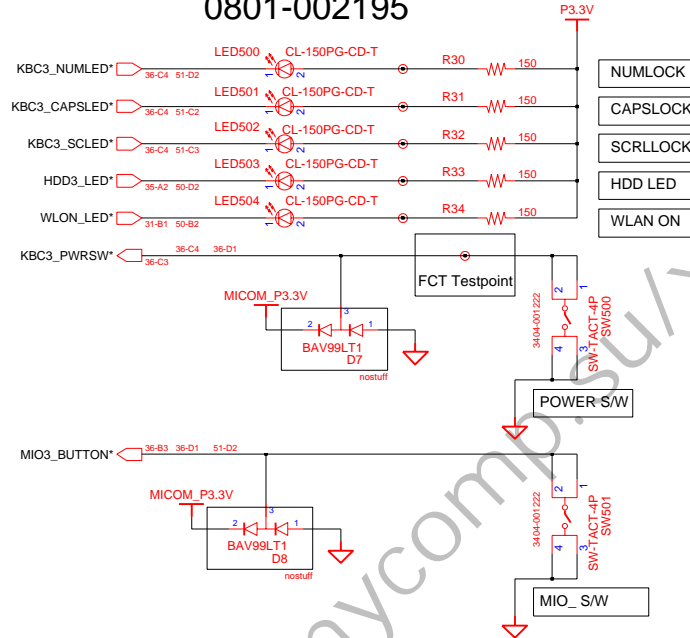
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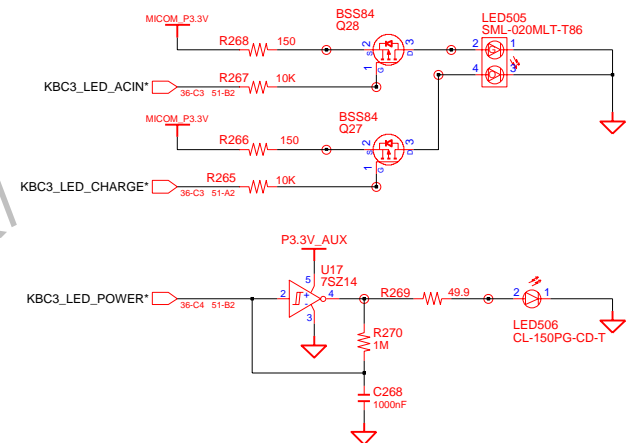
KEYBOARD Same connector with Sedona



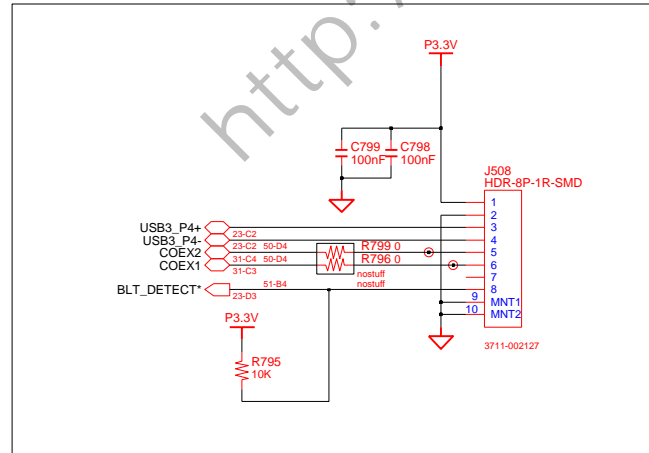
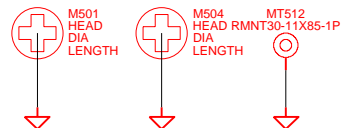
LED 0801-002195



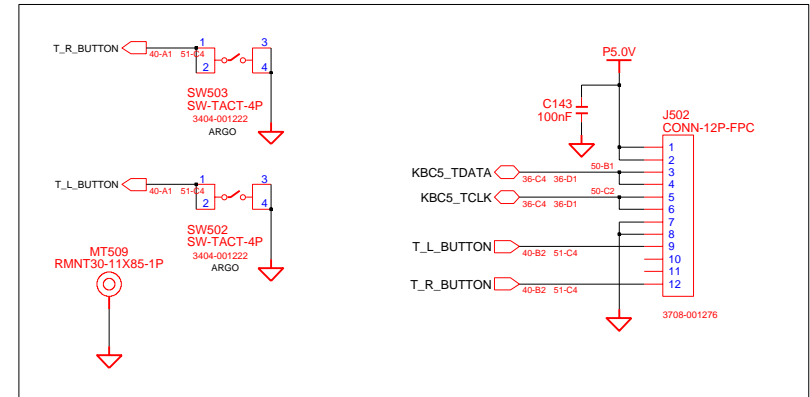
ADAPTERIN/CHARGING LED



Bluetooth Interface Factory Option



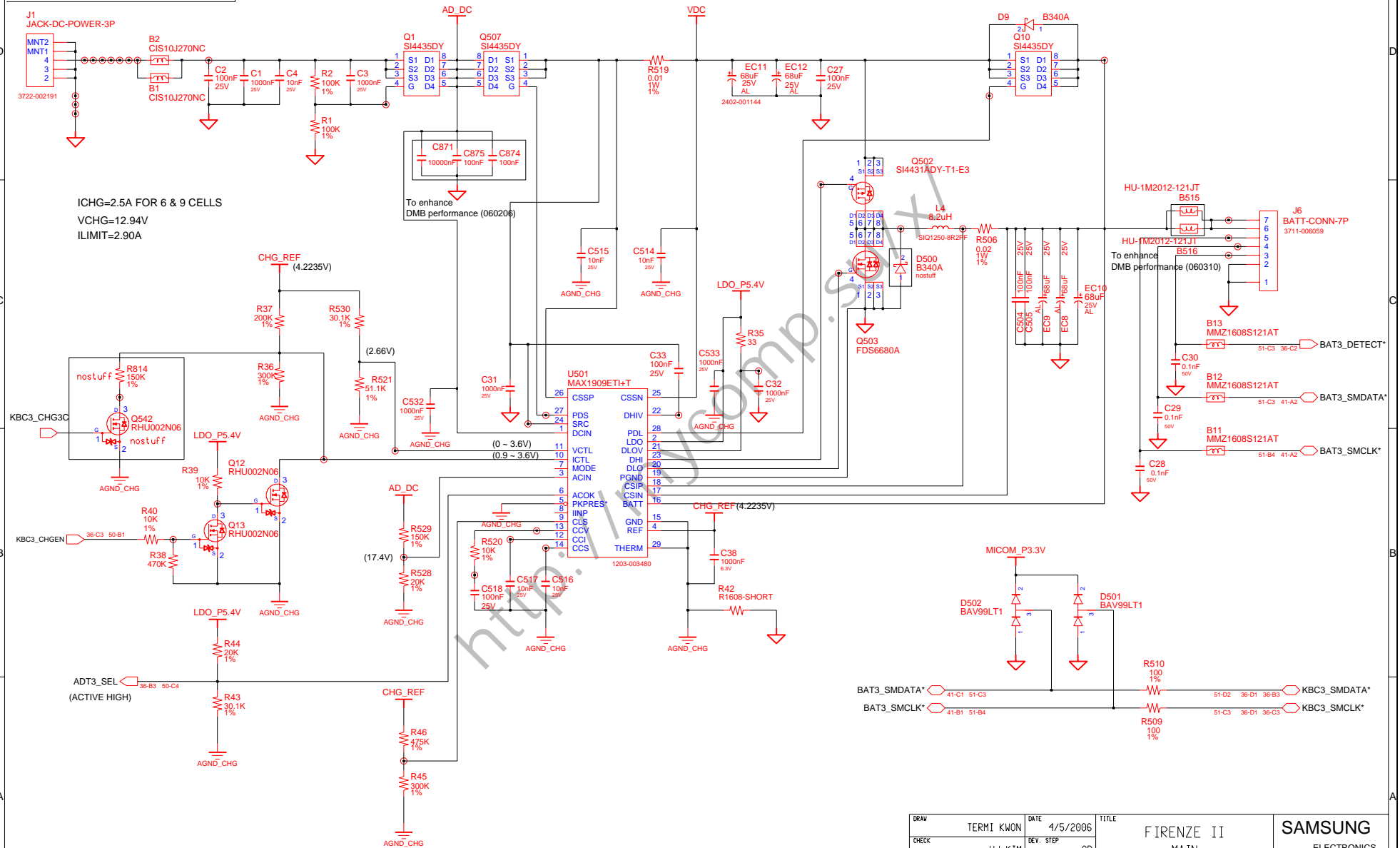
TOUCHPAD



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG
CHECK	HJ KIM	DEV. STEP	SR	MAIN		ELECTRONICS
APPROVAL	SJ PARK	REV	1.0	B'D TO B'D CONNECTOR	PART NO.	BA41-00659A
MODULE CODE	undefined	LAST EDIT	April 5, 2006 8:18:08 PM	PAGE	40	OF 52

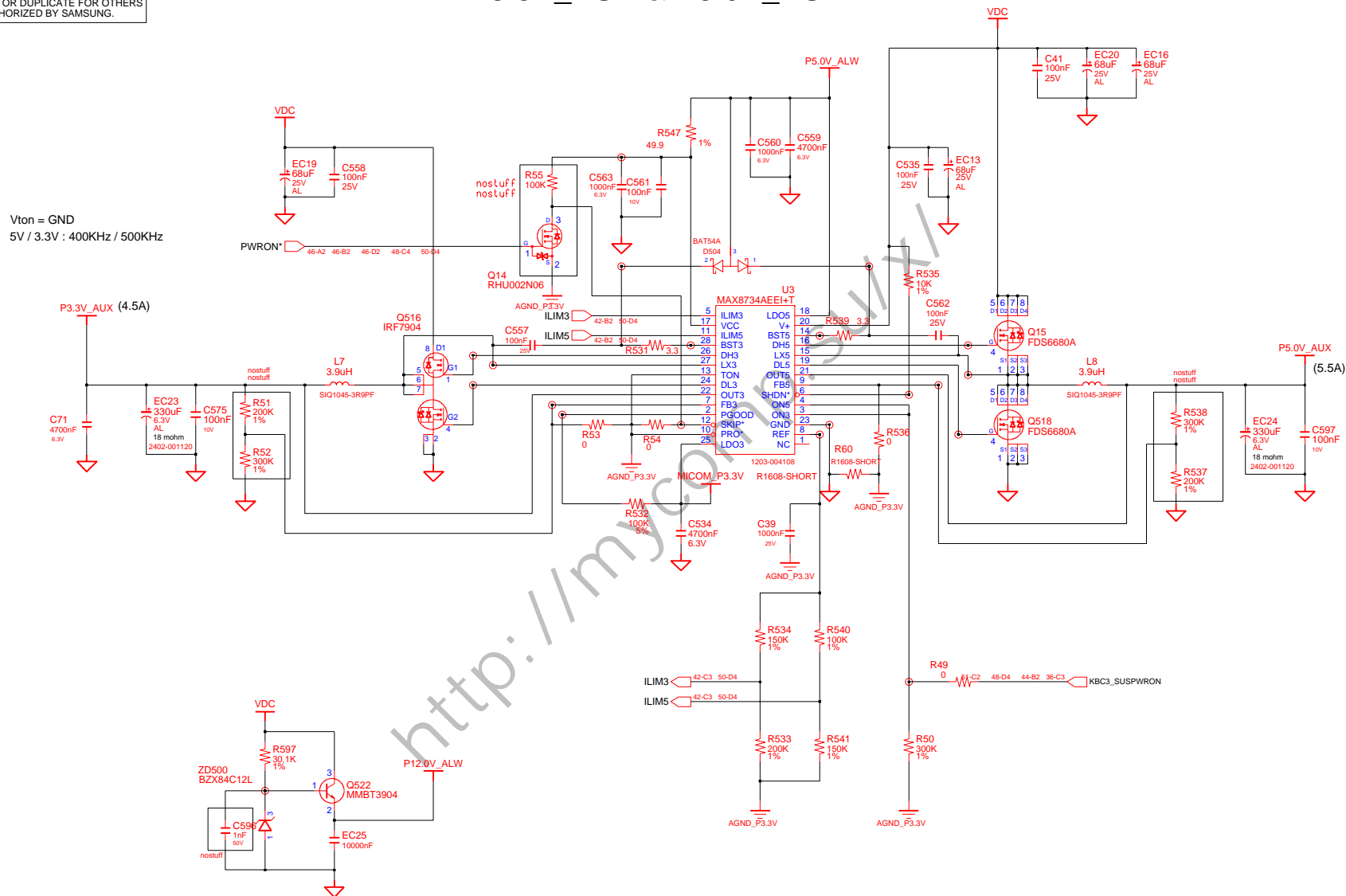
CHARGER & POWER MANAGEMENT

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DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG
CHECK	HJ KIM	DEV. STEP	SR	MAIN	CHARGER	ELECTRONICS
APPROVAL	SJ PARK	REV	1.0			PART NO. BA41-00659A
MODULE CODE	undefined	LAST EDIT	April 5, 2006 8:18:08 PM	PAGE	41	OF 52

Vton = GND
5V / 3.3V : 400KHz / 500KHz



DRAW	TERMI KWON	DATE	4/5/2006	TITLE		FIRENZE II POWER		SAMSUNG ELECTRONICS	
CHECK	HJ KIM	DEV. STEP	SR						
APPROVAL	SJ PARK	REV	1.0	P3.3V ALWAYS & P5V_AUX		PART NO.		BA41-00659A	
MODULE CODE	undefined	LAST EDIT							
				April 5, 2006 8:18:08 PM		PAGE	42	OF	52

P1.2V(VCC_NB) & VCCP (1.05V)

Key components and connections:

- U4 ISL6227CAZ-T**: DC-DC converter with pins for VIN, VCC, UGATE1, UGATE2, ISEN1, ISEN2, LGATE1, LGATE2, VSEN1, VSEN2, PG1, PG2, GND, and OCSET2.
- Q510, Q512 IRF7904**: MOSFETs used for switching the power rails.
- Capacitors**: Various electrolytic and ceramic capacitors for filtering and decoupling, including C889, C827, C830, EC18, EC17, C566, C553, C50, C49, C552, C48, C40, C571, C551, C701, R694, R695, C698, R700, R692, R72, R542, R74, R58, R57, R56, R59, R545, R567, C47, EC21, C863, EC22.
- Resistors**: Various resistors for current sensing, feedback, and gate driving, including R570, C574, R569, C573, L6, SIQ1045-3R99PF, R59, R545, R56, R57, R567, C47, EC21, C863, EC22, R74, R58, R57, R56, R59, R545, R567, C47, EC21, C863, EC22.

TERM	WON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

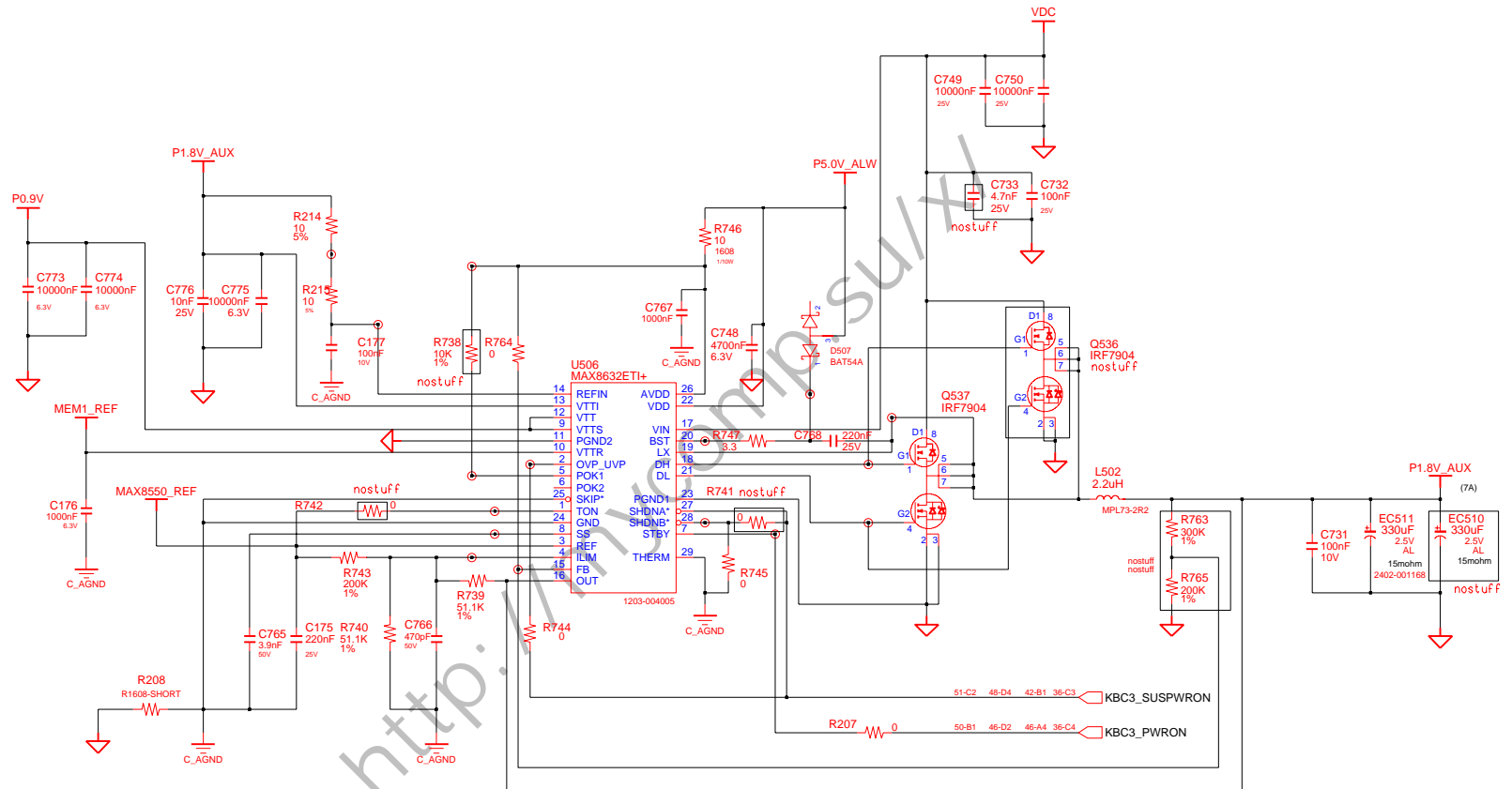
TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

TERMI	KWON	DATE	FILE
4/5/2006	4/5/2006	4/5/2006	4/5/2006
DEV. STEP	SR	SR	SR
REV	1.0	1.0	1.0

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II POWER P1.2V & VCCP	SAMSUNG ELECTRONICS	
CHECK	HJ KIM	DEV. STEP	SR				
APPROVAL	SJ PARK	REV	1.0				
MODULE CODE	undefined	LAST EDIT	April 5, 2006 8:18:08 PM				PAGE
				PART NO.		BA41-00659A	

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DDR2 Power

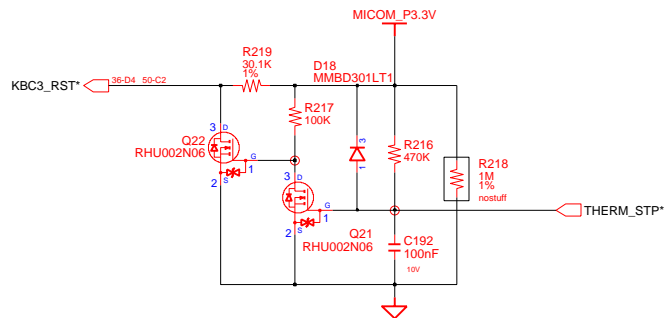


DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN DDR POWER	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			PART NO. BA41-00659A
MODULE CODE	undefined	LAST EDIT		April 5, 2006 8:18:08 PM	PAGE 44	OF 52

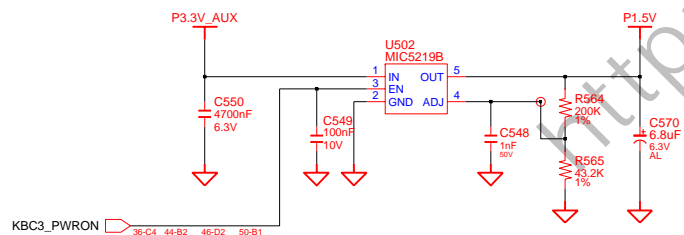
DRAW		TERM1 KWON	DATE	4/5/2006		TITLE		FIRENZE II		SAMSUNG	
CHECK		HJ KIM	REV. STEP	SR		MAIN		ELECTRONICS			
APPROVAL		SJ PARK	REV	1.0		CPU POWER		PART NO.		BA41-00659A	
MODULE CODE		undefined		LAST EDIT		April 5, 2006 8:18:08 PM		PAGE		45	OF 52

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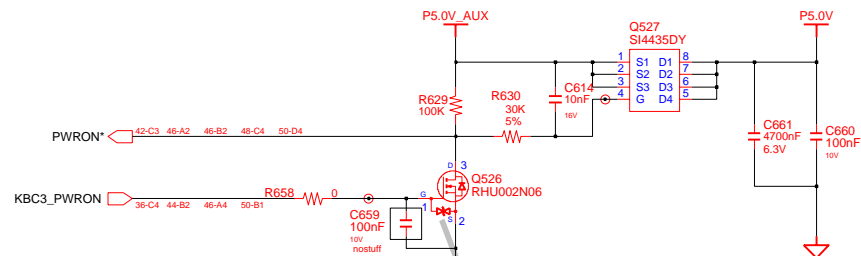
MICOM RESET



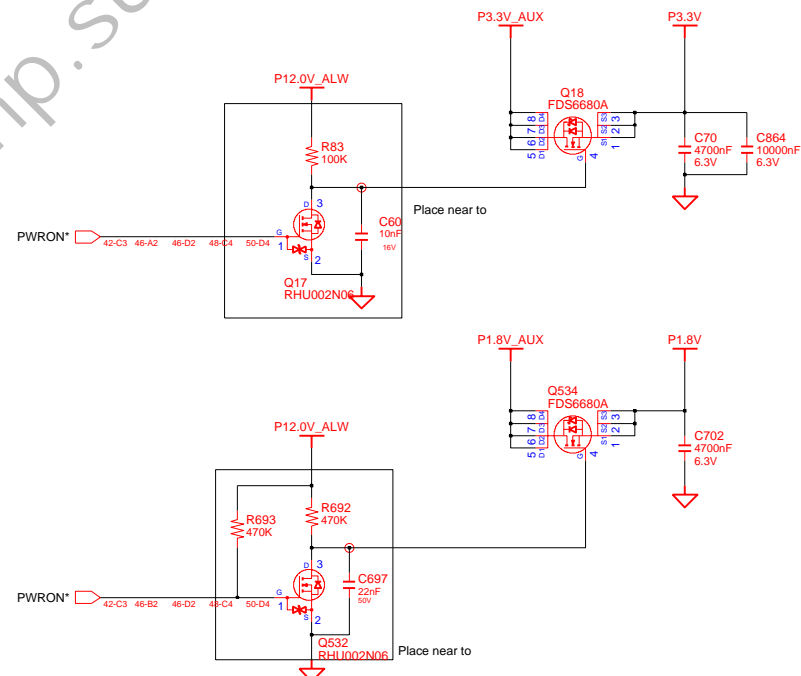
P1.5V POWER



Switched Power On (P5V)

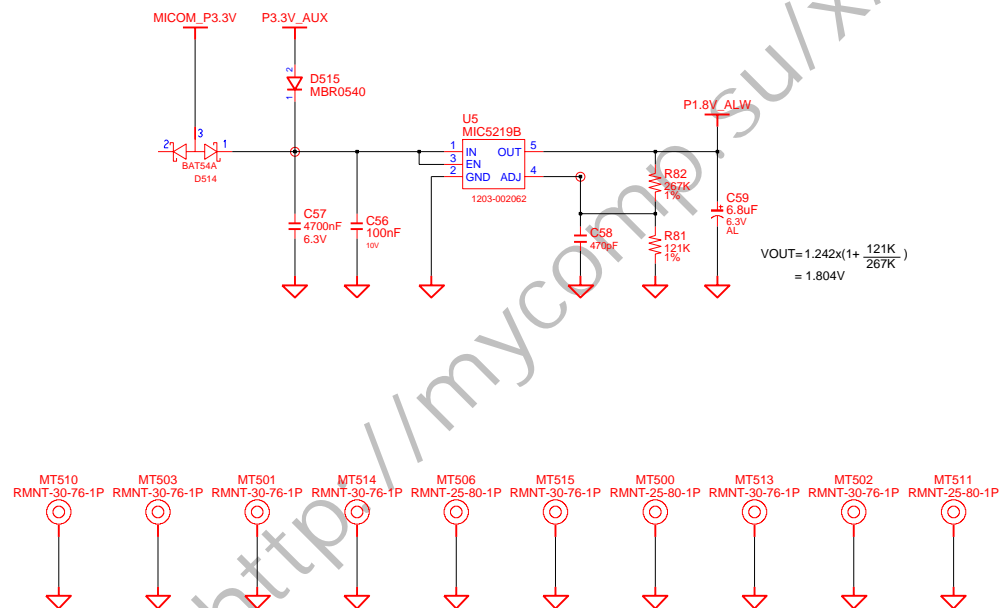


Switched Power On (P3.3V & 1.8V)



DESIGN	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV.	STEP	SR	MAIN	
APPROVAL	SJ PARK	REV	1.0		MICOM & SWITCHED POWER	
MODULE CODE	undefined	LAST EDIT				
				April 5, 2006 8:18:08 PM	PAGE	46 OF 52

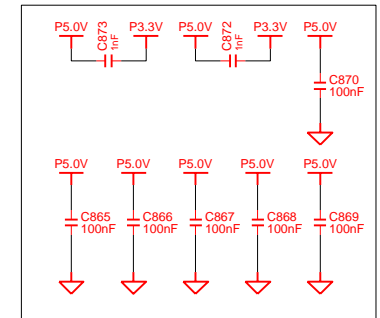
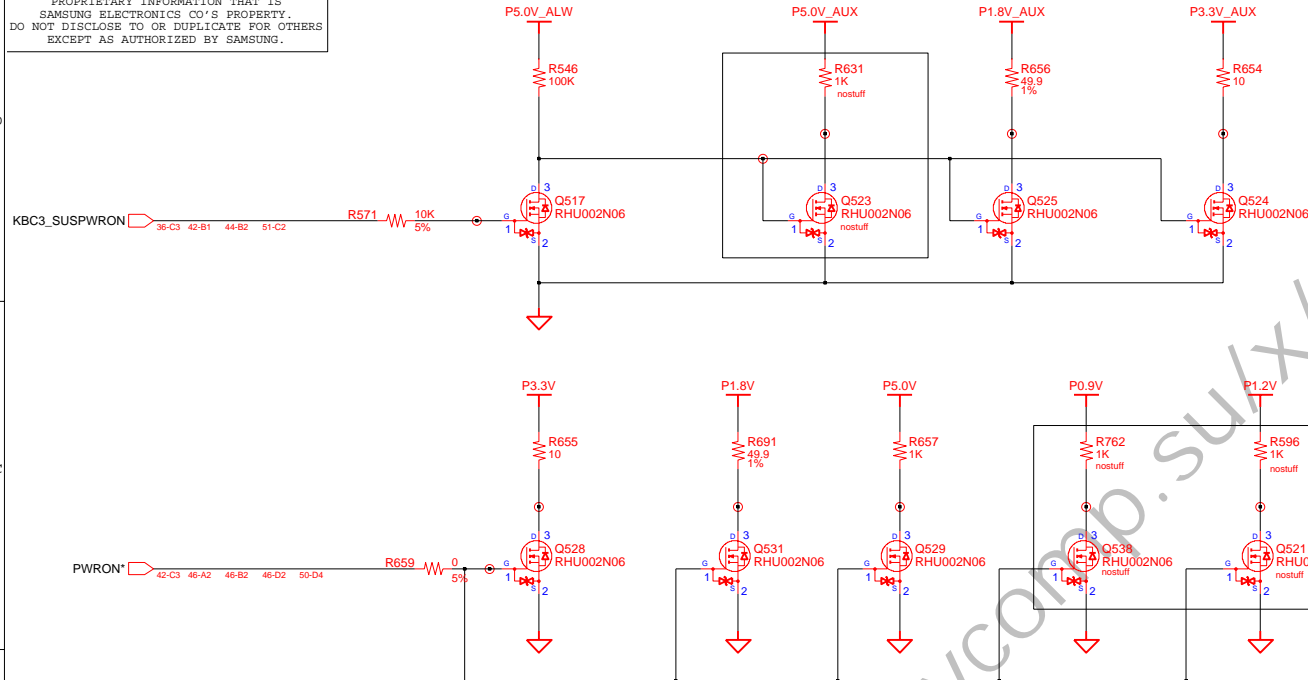
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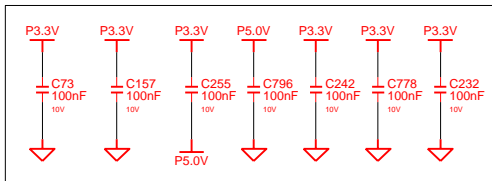
DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG
CHECK	HJ KIM	DEV. STEP	SR			ELECTRONICS
APPROVAL	SJ PARK	REV	1.0	P1.2V & P2.5V AUX POWER	PART NO.	BA41-00659A
MODULE CODE	undefined	LAST EDIT	April 5, 2006 8:18:08 PM	PAGE	47	OF 52

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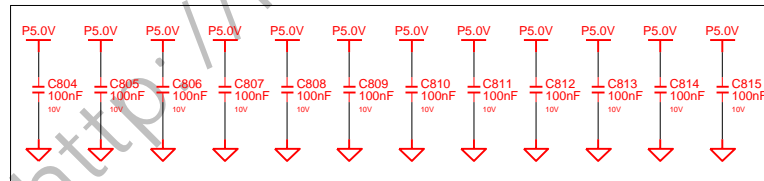
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To enhance DMB performance(060206)

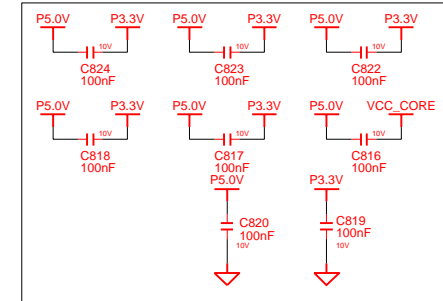


STICHING CAP

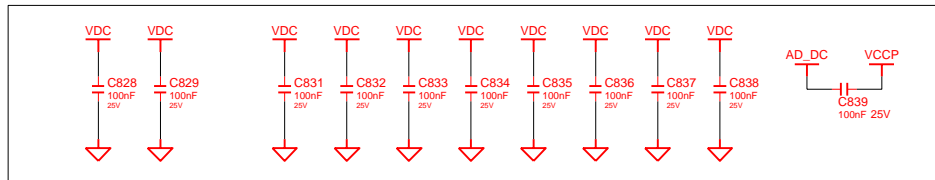


Decap for P5.0V Plane

To reduce BB noise(120 ~ 230MHz) from Power Line (2006/01/24 relate on EMI)



Stitching Cap for Power partition
To reduce BB noise(120 ~ 230MHz) from Power Partition points (2006/01/24 relate on EMI)



Decap for VDC

To reduce BB noise(120 ~ 230MHz) from Power Line (2006/01/24 relate on EMI)

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAINBD POWER ADAPT	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT				
				April 5, 2006 8:18:08 PM	PAGE	48 OF 52

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REV500

1 O

2 O 3

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG ELECTRONICS PART NO. BA41-00659A
CHECK	HJ KIM	DEV. STEP	SR			
APPROVAL	SJ PARK	REV	1.0		TP	
MODULE CODE		LAST EDIT		April 5, 2006 8:18:08 PM	PAGE 49 OF 52	

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OC0EX1
OC0EX2
OILIM3
OILIM5
OMIC1.L
OMIC1.R
OPWRON*
OTV03.C
OTV03.Y
OIDE5.A0
OIDE5.A1
OIDE5.A2
ODDS5.A0
ODDS5.A1
ODDS5.A2
OPC.BEEF
ORTC.CLK
OAC.SDOUT
OAIT3.SEL
OAUTO.ON*

OCPU1.ICK
OCPU1.ID1
OCPU1.TMS
OCRT3.RED

OHPI.OUT.L
OHPI.OUT.R

CLK3_I0H14
CLK3_IN014M
CLK3_USB48

OCRT3.BLUE
OHDD3.LED*
OIDE5_CS1*
OIDE5_CS3*
OIDE5_D(0)
OIDE5_D(1)
OIDE5_D(2)
OIDE5_D(3)
OIDE5_D(4)
OIDE5_D(5)
OIDE5_D(6)
OIDE5_D(7)
OIDE5_D(8)
OIDE5_D(9)
OIDE5_DREQ
OIDE5_IOR*
OIDE5_IOW*
OKBC3_A20G
OKBC3_RST*
OKBC3_VRON
OKBC5_TCLK
OLAN3_ACT*

ODDS5_IRO
OPC13.PAR
OSMB3.CLK

OCBS3_CCLK
OCBS3_CPAR
OCBS3_CVS1
OCBS3_CVS2
OCBS3_SPKR
OHP3_SPKR
CLK3_FM48

ODDS5_CS1*
ODDS5_CS3*
ODDS5_D(0)
ODDS5_D(1)
ODDS5_D(2)
ODDS5_D(3)
ODDS5_D(4)
ODDS5_D(5)
ODDS5_D(6)
ODDS5_D(7)
ODDS5_D(8)
ODDS5_D(9)
ODDS5_DREQ
ODDS5_IOR*
ODDS5_IOW*
ODDS5_RST*
OPC13.CLK8
OPC13_RST*
OSMB3_DATA
OVGA5.DDCC
OVGA5.DDCD
OWLON.LED*
OAUD3.EAPD*
OCBS3_A.D.2
OCBS3_CCD1*
OCBS3_CCD2*
OCBS3_CGNT*
OCBS3_CINT*
OCBS3_CPRQ*
OCBS3_CRST*

OCRT3.GREEN
OCRT5.HSYNC
OCRT5.VSYNC
OFWH1.INIT*
OIDE5_D(10)
OIDE5_D(11)
OIDE5_D(12)
OIDE5_D(13)
OIDE5_D(14)
OIDE5_D(15)
OIDE5_DACK*
OIDE5_DASP*
OIDE5_IORDY
OJCK_SENS.A
OKBC3.CHGEN
OKBC3_PWRON
OKBC3_PWRON
OKBC5_TDATA

OLAN3.WAKE*
QLCD3.VDDEN
QLINE.OUT.L
QLINE.OUT.R

ODDS5_D(10)
ODDS5_D(11)
ODDS5_D(12)
ODDS5_D(13)
ODDS5_D(14)
ODDS5_D(15)
ODDS5_DACK*
OIDE5_IORDY
OPC13_AD(0)
OPC13_AD(1)
OPC13_AD(2)
OPC13_AD(3)

DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II	SAMSUNG
CHECK	HJ KIM	DEV. STEP	SR			ELECTRONICS
APPROVAL	SJ PARK	REV	1.0	TP		PART NO. BA41-00659A
MODULE CODE		LAST EDIT	April 5, 2006 8:18:08 PM	PAGE	50	OF 52

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- P3.3V
- P3.3V
- P3.3V
- P3.3V
- P5.0V
- P5.0V
- P5.0V
- P5.0V
- P5.0V
- PLL VDD

OPLL VSS

OPRTC_BAT

OP1.8V_ALW

- P1.8V_AUX
- P1.8V_AUX
- P1.8V_AUX
- P1.8V_AUX
- P2.5V_LAN
- P2.5V_LAN
- P2.5V_LAN
- P2.5V_LAN
- P3.3V_AUX
- P3.3V_AUX
- P3.3V_AUX
- P3.3V_AUX
- P5.0V_ALW
- P5.0V_ALW
- P5.0V_ALW
- P5.0V_AUX
- P5.0V_AUX
- P5.0V_AUX
- PCIE_PVDD

○PCIE_VDDR

- ☐ P12_0V_ALW
- ☐ P12_0V_ALW
- ☐ P12_0V_ALW
- ☐ P12_0V_ALW
- ☐ P12_0V_ALW
- ☐ VDC
- ☐ VDC
- ☐ VDC
- ☐ VDC
- ☐ VDC
- ☐ VCCP
- ☐ VCCP
- ☐ VCCP
- ☐ VCCP
- ☐ VCCP
- ☐ VCC_NB

○VCC_NB
○VCC_NB
○VCC_NB
○VCC_NB

VCC_CRT

○VCC_CORE
○VCC_CORE
○VCC_CORE
○VCC_CORE
○VCC_CORE

