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DRESDEN-INT

PCB Thickness:1.1mm

CPU : AMD GRIFFIN
Chip Set : AMD RS780MN + SB700
Remarks : AMD PUMA Platform w/ IGP
2 SODIMMs DDR2

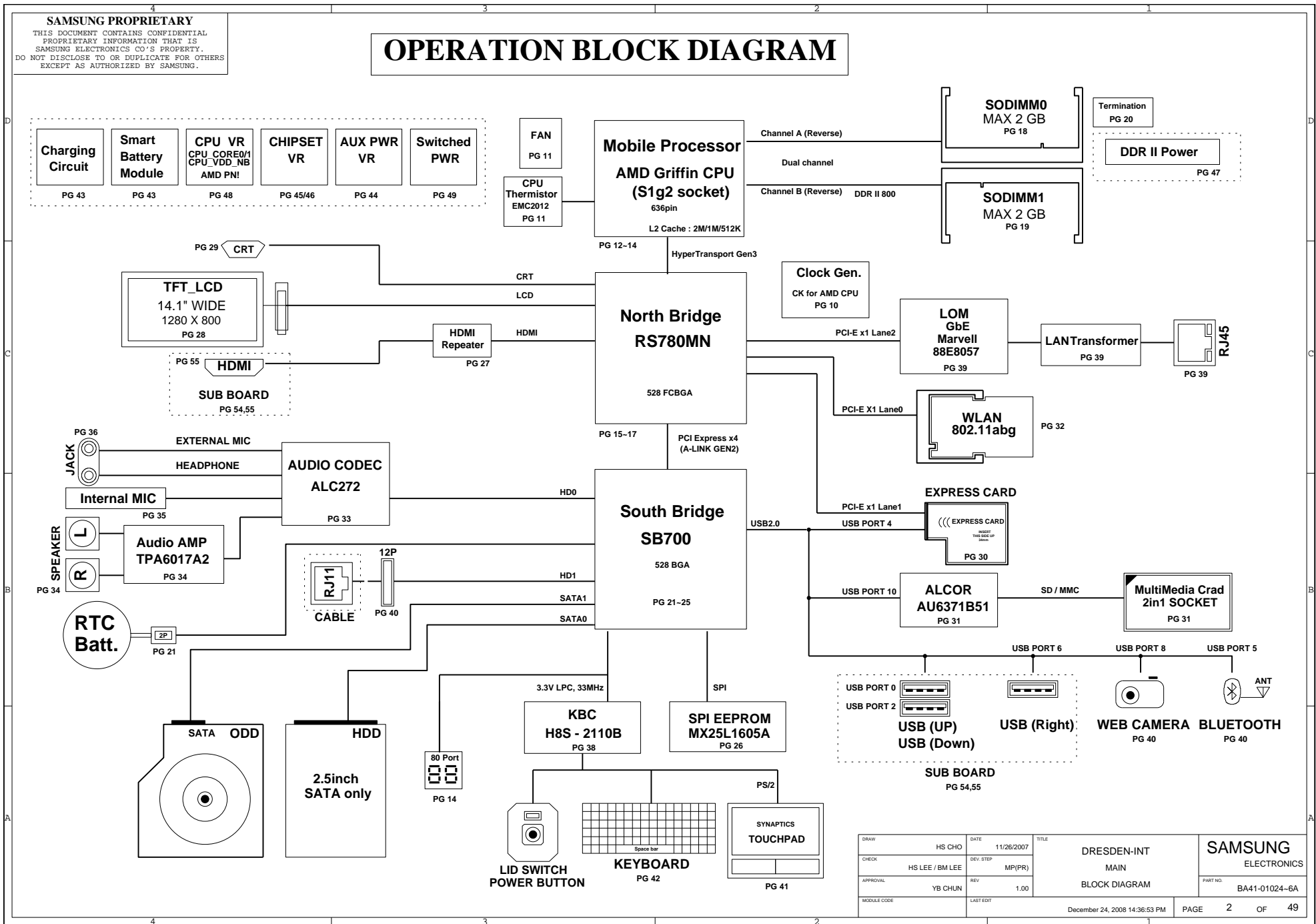
Model Name : DRESDEN-INT
PBA Name : MAIN
PCB Code : BA41-01024A (GCE)
BA41-01025A (NY)
BA41-01026A (HST)
Dev. Step : MP (PR)
Revision : 1.00
T.R. Date : 2008.12.24

DRAW	CHECK	APPROVAL
-	-	-

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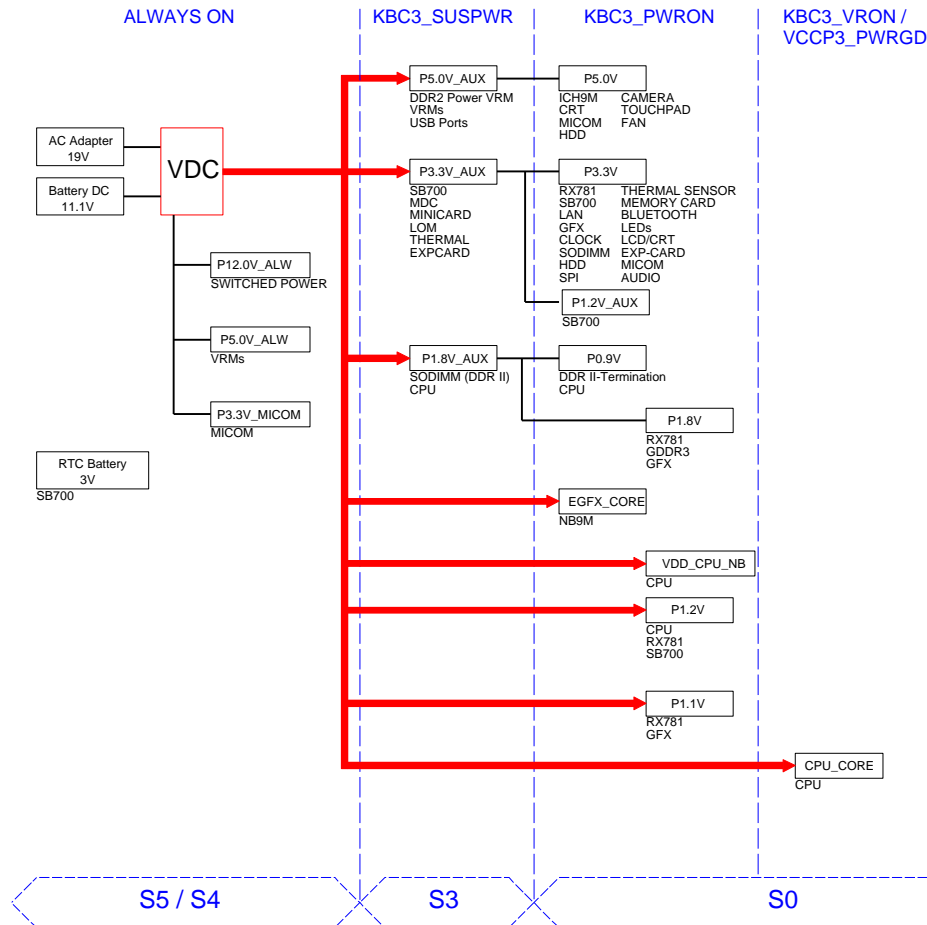
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CHECK	HS LEE / BM LEE	DEV. STEP	MP (PR)		COVER	ELECTRONICS
APPROVAL	YB CHUN	REV	1.00		CONTENTS	PART NO.
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POWER DIAGRAM

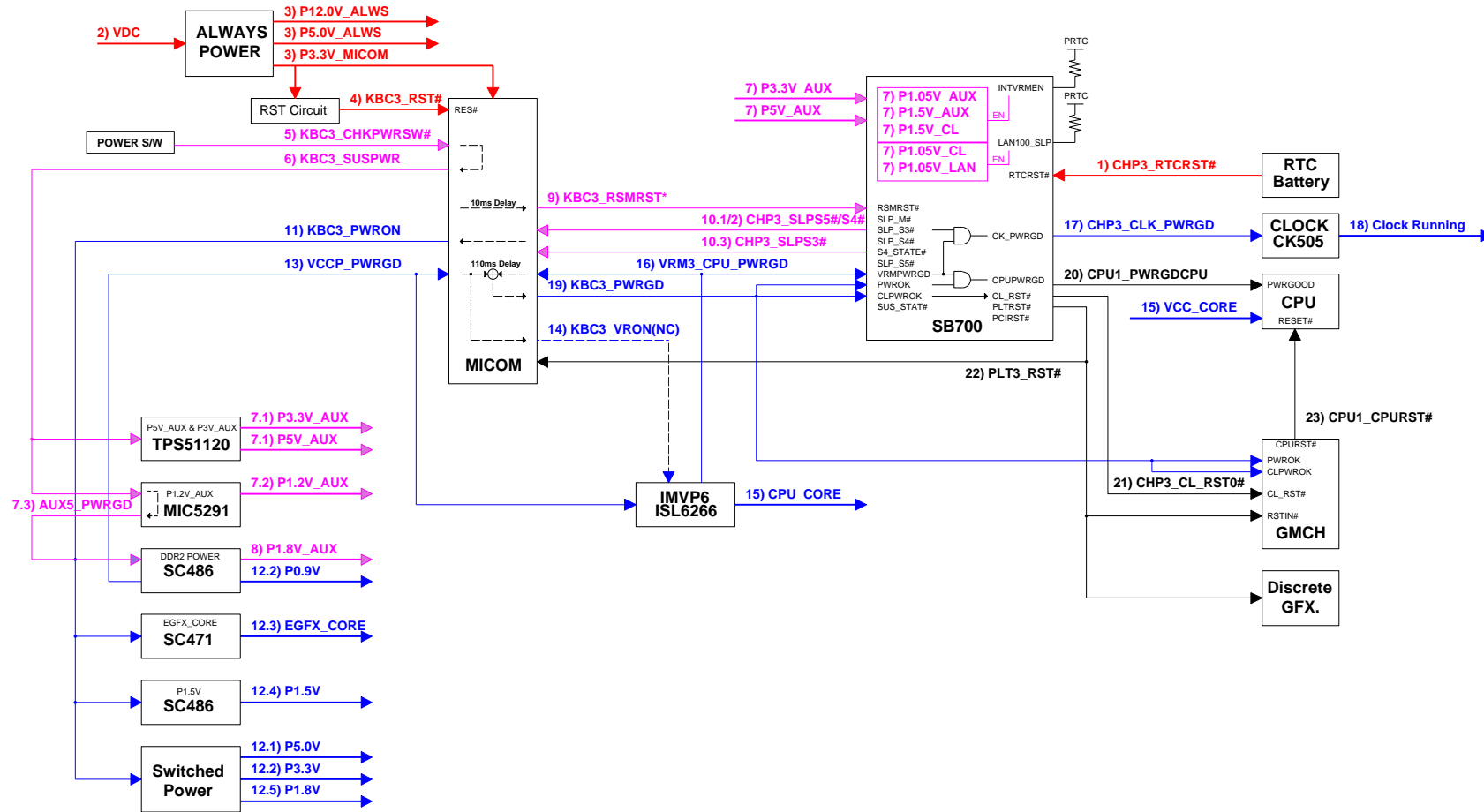


Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	OFF	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L

DRAW	HS CHO	DATE	11/26/2007	TITLE	DRESDEN-INT MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS
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POWER SEQUENCE Rev. 0.1

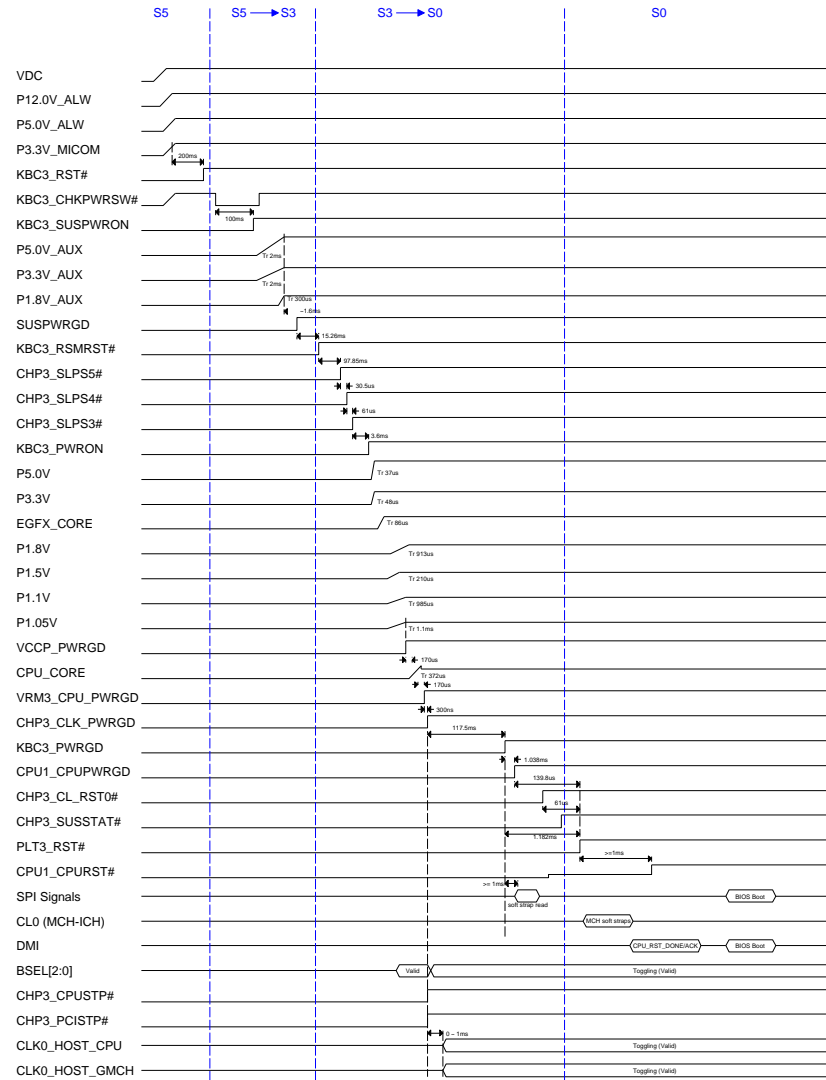


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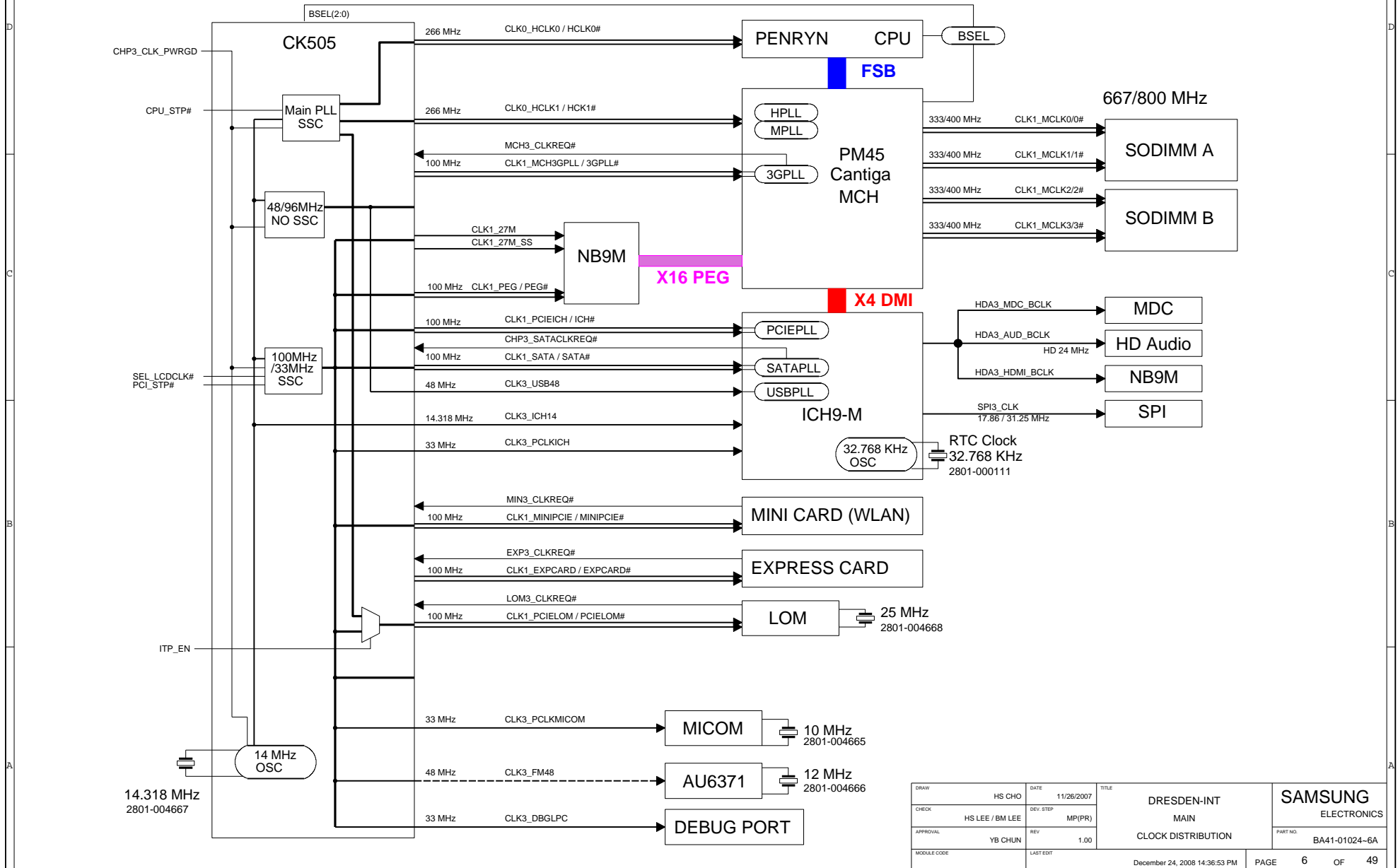
Timing Diagram, Power ON Rev. 0.1 Phil 2008-04-15



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CLOCK DISTRIBUTION Rev. 0.1



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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
---------	--------	----------	------------

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH	Real Time Clock
Crystal	10MHz	MICOM	H8S/2110BV
Crystal	14.318MHz	CLOCK-GENERATOR	ICS951461
Crystal	12MHz	MEMORY CARD	MEMORY CARD
Crystal	25MHz	LAN	LAN

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for Processor (1.308~1.068V)
P1.05V	Processor System Bus(PSB) Termination (1.05V) GMCH & ICH8 Core Voltage
P1.8V_AUX	1.8V power rail for DDR2 (off in S4-S5)
P0.9V	0.9V switched power rail (off in S3-S5)
P1.8V	1.8V power rail for GDDR3 (off in S3-S5)
P1.1V	1.1V power rail for GFX (off in S3-S5)
P1.5V	1.5V power rail for ICH (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
PRTC_BAT	3.0V power rail (ALWAYS ON)
P3.3V_MICOM	3.3V always on power rail for MICOM
P5.0V_ALW	5V power rail (Always On)
P12.0V_ALW	12V power rail (Always On)

CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 1 0 0	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 1	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 0 1	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 0	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 1 0 0 0 0	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 1 0 0 0 1	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
				**11111111* : 0V power good asserted.	

I²C / SMB Address

Devices	Address	Hex	Bus
ICH	Master	-	SMBUS Master
SODIMM0	1010 000X	A0h	-
SODIMM1	1010 010X	A4h	-
CK-505 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
MICOM	Master	-	SMBUS Master
BATTERY	0001 011X	16h	-
EMC2102 (Thermal Sensor)	0111 101X	7Ah	Thermal Sensor

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1	SYSTEM PORT B
4	EXPRESS CARD
5	BLUETOOTH
6	SYSTEM PORT C
8	CAMERA
9	MINI PCIE (WLAN)
10	MEMORY CARD

System Power States

CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.

CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is retained, and refreshes continue. All clocks stop except RTC clock.

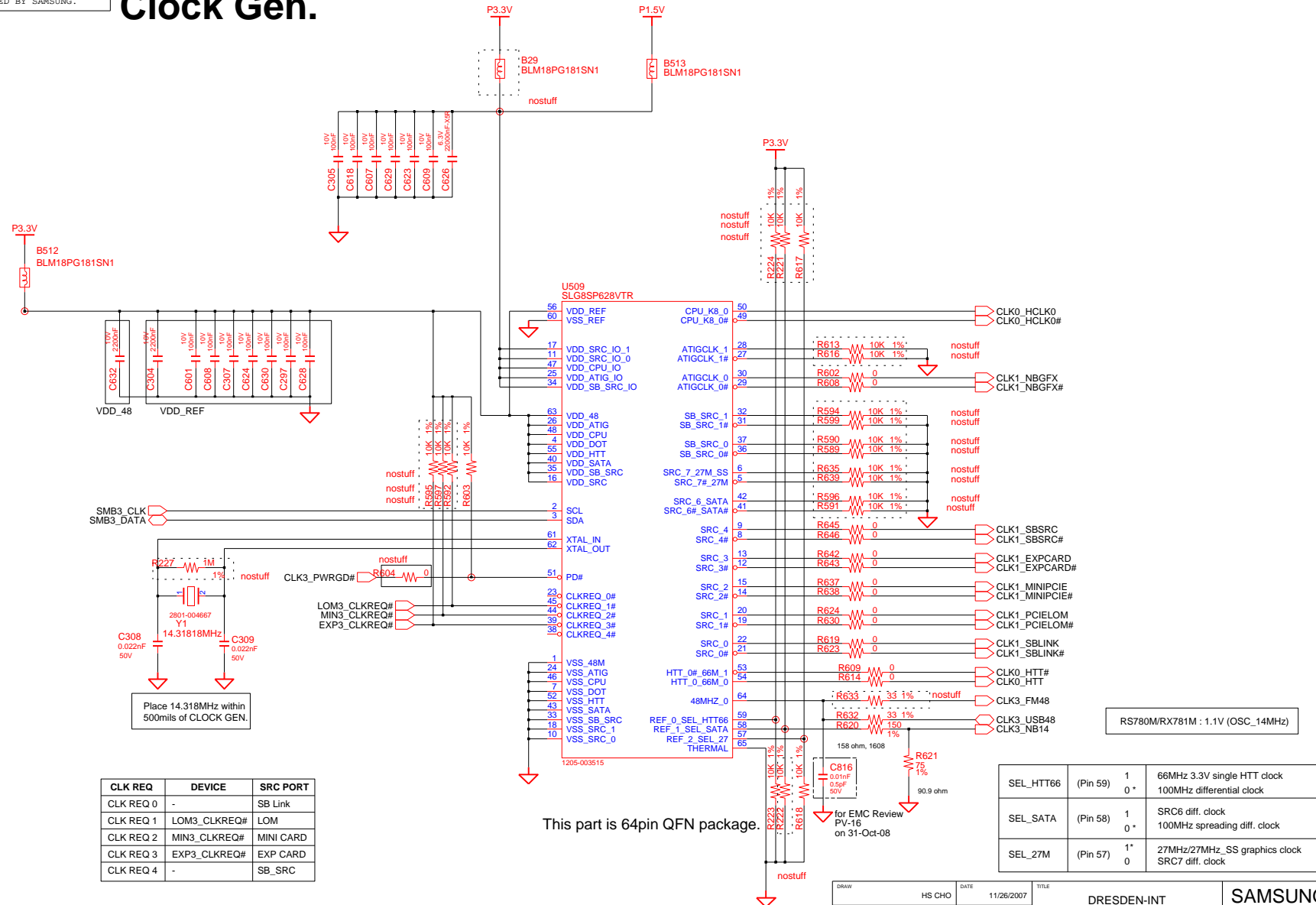
CHP3_SLPS4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.

CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

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CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)		MAIN	ELECTRONICS
APPROVAL	YB CHUN	REV	1.00		BOARD INFORMATION	PART NO.
MODULE CODE		LAST EDIT			December 24, 2008 14:36:53 PM	BA41-01024-6A
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Clock Gen.



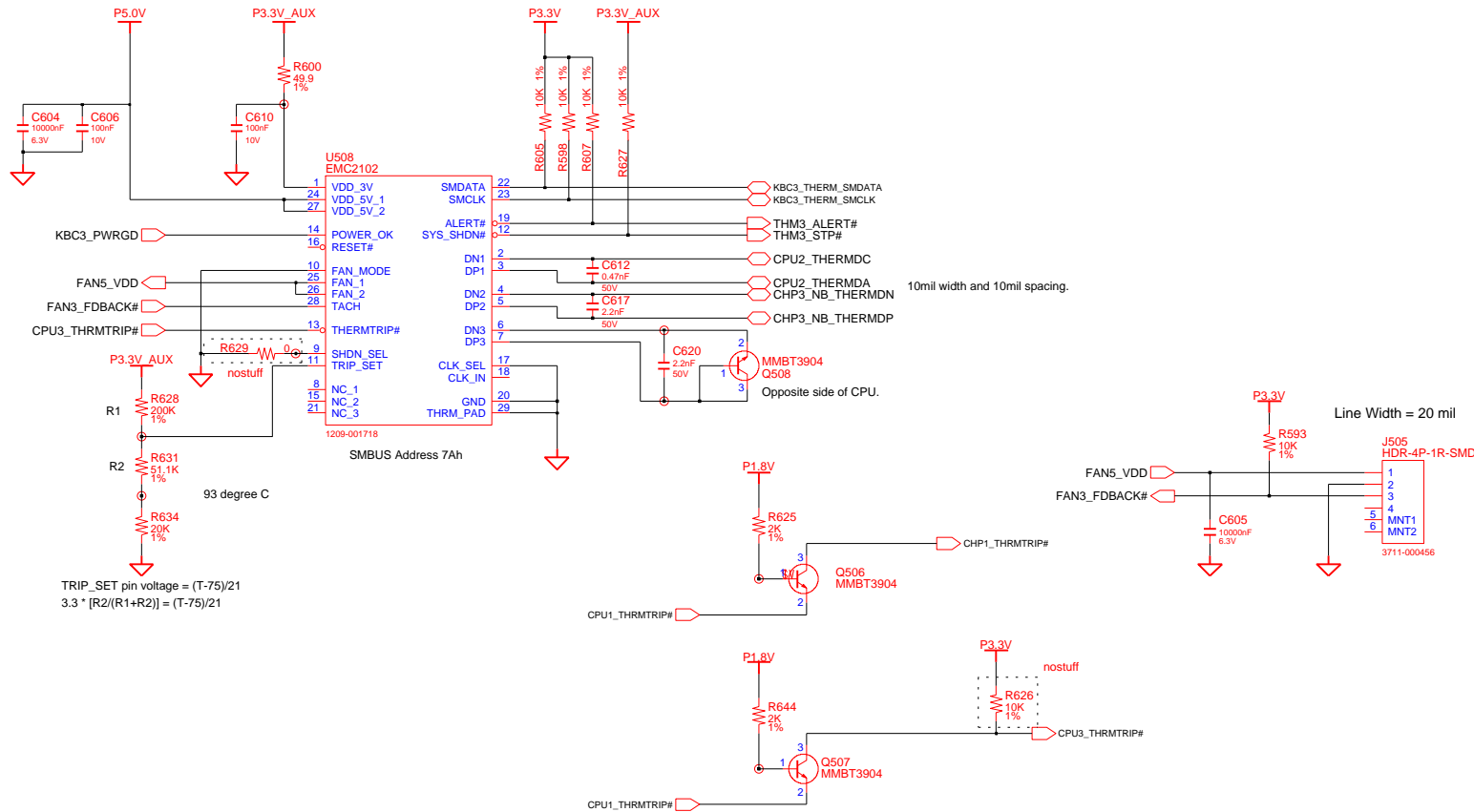
This part is 64pin QFN package.

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APPROVAL	YB CHUN	REV	1.00		CLOCK GEN	PART NO.
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THERMAL SENSOR & FAN CONTROL



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APPROVAL	YB CHUN	REV	1.00		THERMAL SENSOR&FAN CONTROL	PART NO. BA41-01024-6A
MODULE CODE		LAST ENT		December 24, 2008 14:36:53 PM	PAGE 11 OF 49	

Pin 1/2V

CPU500-1 S1G2

Pin 1/5

HT LINK

CPU1_HTTIN(15:0)

CPU1_HTTOUT(15:0)

CPU1_CLKIN_0

CPU1_CLKIN_1

CPU1_CLKIN_0#

CPU1_CLKIN_1#

CPU1_CTLIN_0

CPU1_CTLIN_1

CPU1_CTLIN_0#

CPU1_CTLIN_1#

CPU1_CLKOUT_0

CPU1_CLKOUT_1

CPU1_CLKOUT_0#

CPU1_CLKOUT_1#

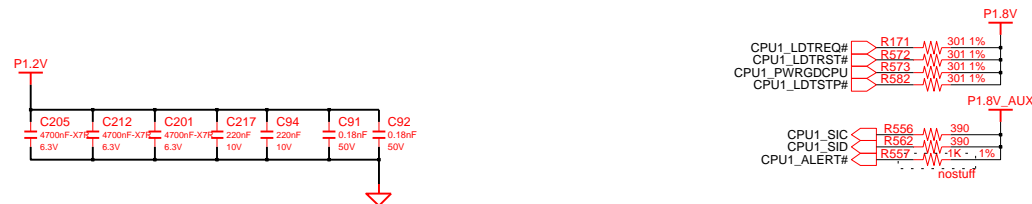
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CPU1_CTLOUT_1

CPU1_CTLOUT_0#

CPU1_CTLOUT_1#

0185482000

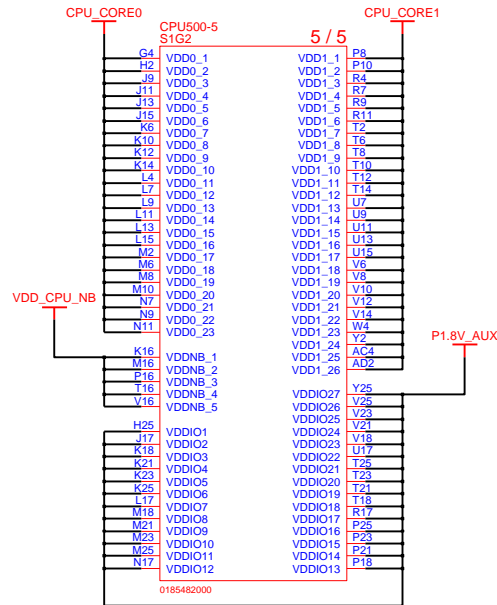
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MODULE CODE	LAST EDIT					December 24, 2008 14:36:53 PM

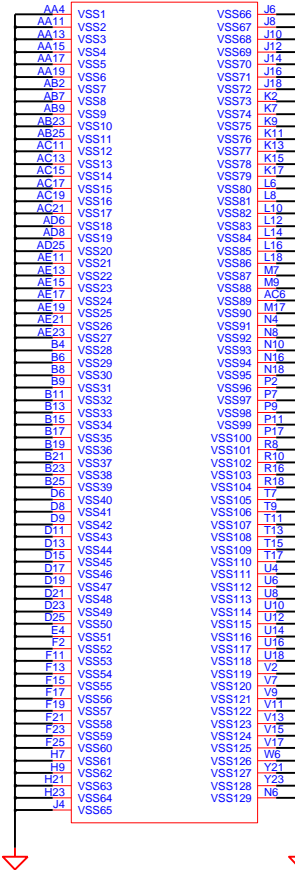
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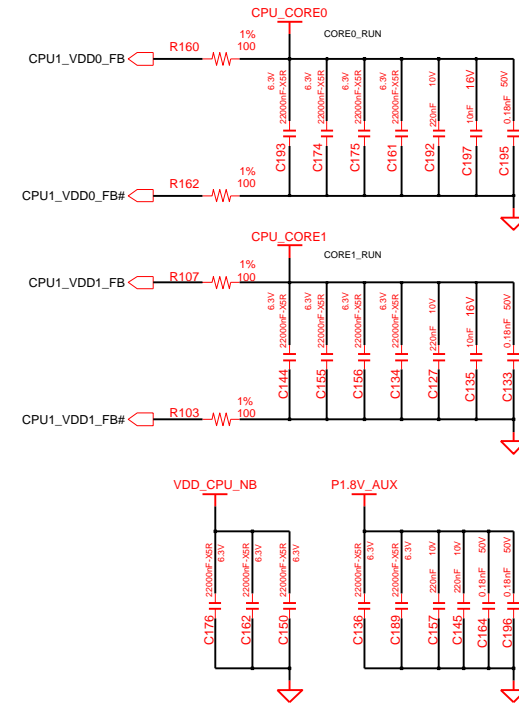
S1g2 CPU (3/3)



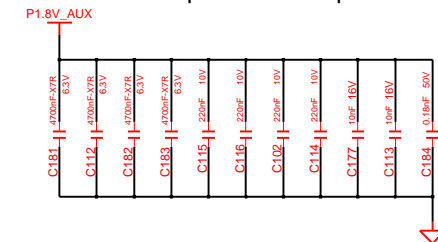
CPU Socket : 0185482000



Bottom side decoupling




Decoupling between processor and Memory Place close to processor as possible




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MODULE CODE		LAST EDIT December 24, 2008 14:36:53 PM			PAGE 15	OF 49

The schematic diagram illustrates the electrical connections for the RS780MN 2/3 board. It features several functional blocks and components:

- Power Management:** Includes regulators like B27, B28, B18, and B21, along with decoupling capacitors (C224, C225, C226, C227, C228, C229, C230, C231, C232, C233, C234, C235, C236, C237, C238, C239, C240, C241, C242, C243, C244, C245, C246, C247, C248, C249, C250, C251, C252, C253, C254, C255, C256, C257, C258, C259, C260, C261, C262, C263, C264, C265, C266, C267, C268, C269, C270, C271, C272, C273, C274, C275, C276, C277, C278, C279, C280, C281, C282, C283, C284, C285, C286, C287, C288, C289, C290, C291, C292, C293, C294, C295, C296, C297, C298, C299, C300, C301, C302, C303, C304, C305, C306, C307, C308, C309, C310, C311, C312, C313, C314, C315, C316, C317, C318, C319, C320, C321, C322, C323, C324, C325, C326, C327, C328, C329, C330, C331, C332, C333, C334, C335, C336, C337, C338, C339, C340, C341, C342, C343, C344, C345, C346, C347, C348, C349, C350, C351, C352, C353, C354, C355, C356, C357, C358, C359, C360, C361, C362, C363, C364, C365, C366, C367, C368, C369, C370, C371, C372, C373, C374, C375, C376, C377, C378, C379, C380, C381, C382, C383, C384, C385, C386, C387, C388, C389, C390, C391, C392, C393, C394, C395, C396, C397, C398, C399, C400, C401, C402, C403, C404, C405, C406, C407, C408, C409, C410, C411, C412, C413, C414, C415, C416, C417, C418, C419, C420, C421, C422, C423, C424, C425, C426, C427, C428, C429, C430, C431, C432, C433, C434, C435, C436, C437, C438, C439, C440, C441, C442, C443, C444, C445, C446, C447, C448, C449, C450, C451, C452, C453, C454, C455, C456, C457, C458, C459, C460, C461, C462, C463, C464, C465, C466, C467, C468, C469, C470, C471, C472, C473, C474, C475, C476, C477, C478, C479, C480, C481, C482, C483, C484, C485, C486, C487, C488, C489, C490, C491, C492, C493, C494, C495, C496, C497, C498, C499, C500, C501, C502, C503, C504, C505, C506, C507, C508, C509, C510, C511, C512, C513, C514, C515, C516, C517, C518, C519, C520, C521, C522, C523, C524, C525, C526, C527, C528, C529, C530, C531, C532, C533, C534, C535, C536, C537, C538, C539, C540, C541, C542, C543, C544, C545, C546, C547, C548, C549, C550, C551, C552, C553, C554, C555, C556, C557, C558, C559, C560, C561, C562, C563, C564, C565, C566, C567, C568, C569, C570, C571, C572, C573, C574, C575, C576, C577, C578, C579, C580, C581, C582, C583, C584, C585, C586, C587, C588, C589, C590, C591, C592, C593, C594, C595, C596, C597, C598, C599, C600, C601, C602, C603, C604, C605, C606, C607, C608, C609, C610, C611, C612, C613, C614, C615, C616, C617, C618, C619, C620, C621, C622, C623, C624, C625, C626, C627, C628, C629, C630, C631, C632, C633, C634, C635, C636, C637, C638, C639, C640, C641, C642, C643, C644, C645, C646, C647, C648, C649, C650, C651, C652, C653, C654, C655, C656, C657, C658, C659, C660, C661, C662, C663, C664, C665, C666, C667, C668, C669, C670, C671, C672, C673, C674, C675, C676, C677, C678, C679, C680, C681, C682, C683, C684, C685, C686, C687, C688, C689, C690, C691, C692, C693, C694, C695, C696, C697, C698, C699, C700, C701, C702, C703, C704, C705, C706, C707, C708, C709, C710, C711, C712, C713, C714, C715, C716, C717, C718, C719, C720, C721, C722, C723, C724, C725, C726, C727, C728, C729, C730, C731, C732, C733, C734, C735, C736, C737, C738, C739, C740, C741, C742, C743, C744, C745, C746, C747, C748, C749, C750, C751, C752, C753, C754, C755, C756, C757, C758, C759, C760, C761, C762, C763, C764, C765, C766, C767, C768, C769, C770, C771, C772, C773, C774, C775, C776, C777, C778, C779, C780, C781, C782, C783, C784, C785, C786, C787, C788, C789, C790, C791, C792, C793, C794, C795, C796, C797, C798, C799, C800, C801, C802, C803, C804, C805, C806, C807, C808, C809, C810, C811, C812, C813, C814, C815, C816, C817, C818, C819, C820, C821, C822, C823, C824, C825, C826, C827, C828, C829, C830, C831, C832, C833, C834, C835, C836, C837, C838, C839, C840, C841, C842, C843, C844, C845, C846, C847, C848, C849, C850, C851, C852, C853, C854, C855, C856, C857, C858, C859, C860, C861, C862, C863, C864, C865, C866, C867, C868, C869, C870, C871, C872, C873, C874, C875, C876, C877, C878, C879, C880, C881, C882, C883, C884, C885, C886, C887, C888, C889, C890, C891, C892, C893, C894, C895, C896, C897, C898, C899, C900, C901, C902, C903, C904, C905, C906, C907, C908, C909, C910, C911, C912, C913, C914, C915, C916, C917, C918, C919, C920, C921, C922, C923, C924, C925, C926, C927, C928, C929, C930, C931, C932, C933, C934, C935, C936, C937, C938, C939, C940, C941, C942, C943, C944, C945, C946, C947, C948, C949, C950, C951, C952, C953, C954, C955, C956, C957, C958, C959, C960, C961, C962, C963, C964, C965, C966, C967, C968, C969, C970, C971, C972, C973, C974, C975, C976, C977, C978, C979, C980, C981, C982, C983, C984, C985, C986, C987, C988, C989, C990, C991, C992, C993, C994, C995, C996, C997, C998, C999, C1000, C1001, C1002, C1003, C1004, C1005, C1006, C1007, C1008, C1009, C1010, C1011, C1012, C1013, C1014, C1015, C101

DRAW HS CHO		DATE 11/26/2007	TITLE DRESDEN-INT MAIN RS780MN 2/3			
CHECK HS LEE / BM LEE		DEV. STEP MP(PR)				
APPROVAL YB CHUN		REV 1.00				
MODULE CODE			LAST EDIT December 24, 2008 14:36:53 PM		PAGE 16	OF 49
					PART NO. BA41-01024-6A	

U507-5
216-0674026

P1.1V

R838
0

C202 4700nF-X7R 6.3V

C228 100nF 10V

C235 100nF 10V

C229 100nF 10V

J17
K16
L16
M16
P16
R16
T16

VDDHT_1
VDDHT_2
VDDHT_3
VDDHT_4
VDDHT_5
VDDHT_6
VDDHT_7

P1.2V

R839
0

C204 1000nF 6.3V

C209 100nF 10V

C208 100nF 10V

C207 100nF 10V

H18
G19
F20
E21
D22
B23
A23

VDDHTRX_1
VDDHTRX_2
VDDHTRX_3
VDDHTRX_4
VDDHTRX_5
VDDHTRX_6
VDDHTRX_7

C200 4700nF-X7R 6.3V

C211 100nF 10V

C213 100nF 10V

C203 100nF 10V

C223 100nF 10V

AE25
AD24
AC23
AB22
AA21
Y20
W19
V18
U17
T17
R17
P17
M17

VDDHTTX_1
VDDHTTX_2
VDDHTTX_3
VDDHTTX_4
VDDHTTX_5
VDDHTTX_6
VDDHTTX_7
VDDHTTX_8
VDDHTTX_9
VDDHTTX_10
VDDHTTX_11
VDDHTTX_12
VDDHTTX_13

P1.8V

B23
CIC21J601NE

C278 22000nF-X5R 20% 6.3V

C257 4700nF-X7R 6.3V

C277 4700nF-X7R 6.3V

C256 100nF 10V

C264 100nF 10V

C262 100nF 10V

C263 100nF 10V

J10
P10
K10
M10
L10
W9
H9
R10
Y9
A9
AB9
AD9
AE9
U10

VDDA18PCIE_1
VDDA18PCIE_2
VDDA18PCIE_3
VDDA18PCIE_4
VDDA18PCIE_5
VDDA18PCIE_6
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VDDA18PCIE_13

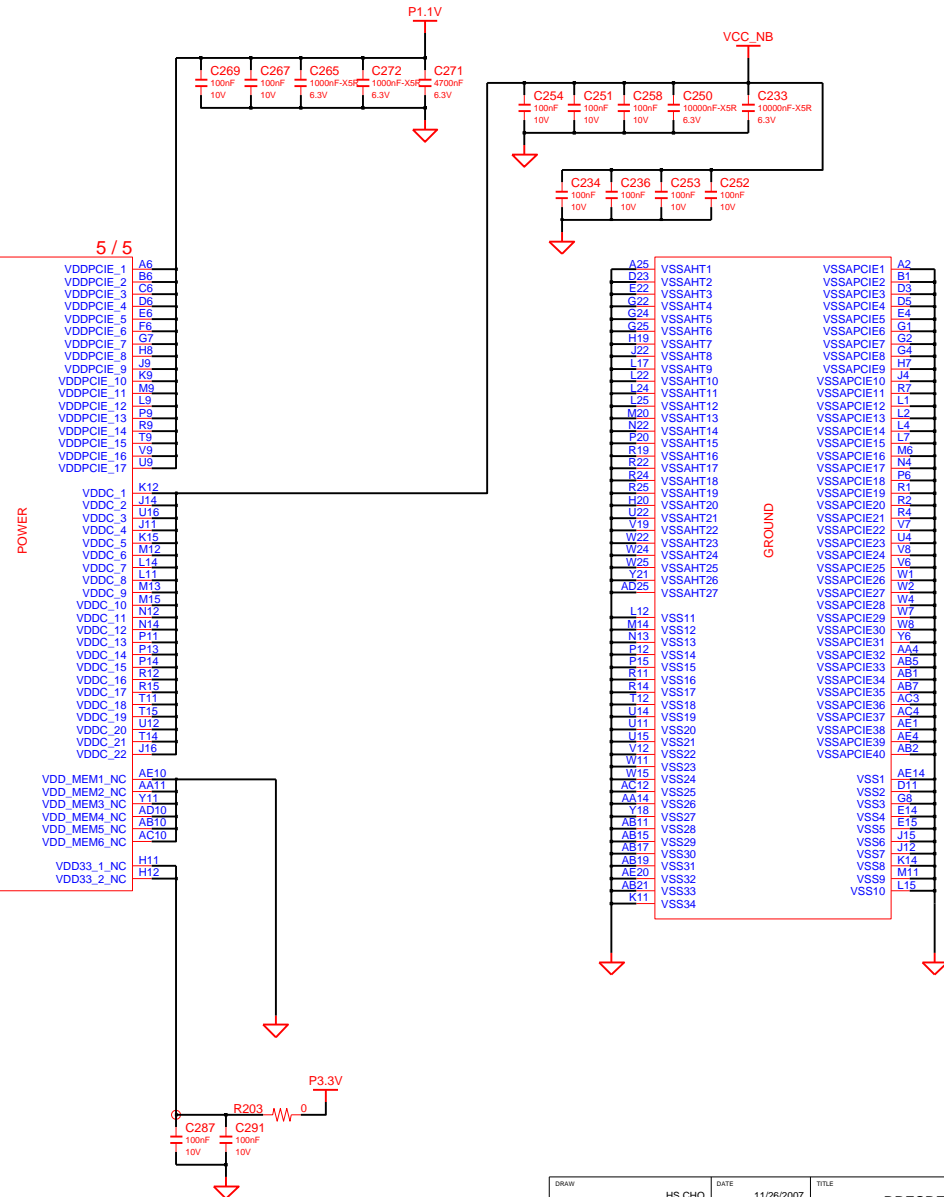
P1.8V

C266 1000nF-X5R 6.3V

F9
G9
AE11
AD11

VDD18_1
VDD18_2
VDD18_MEM
VDD18_3

0904-002431



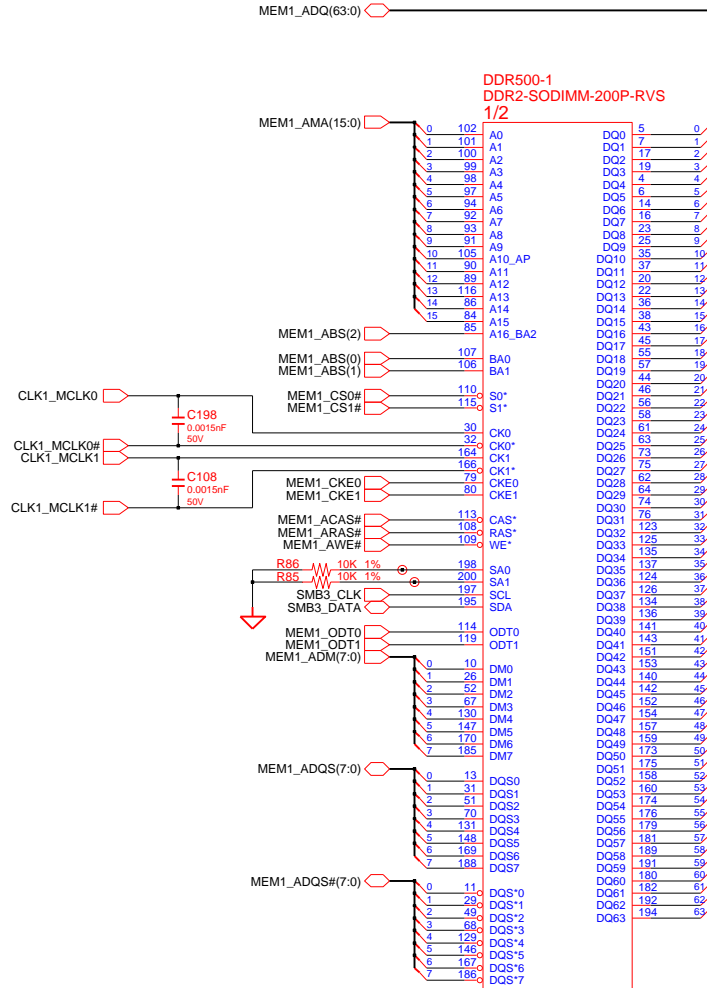
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CHECK HS LEE / BM LEE		DEV. STEP MP(PR)				
APPROVAL YB CHUN		REV 1.00				
MODULE CODE		LAST EDIT December 24, 2008 14:36:53 PM	PAGE	17	OF	49

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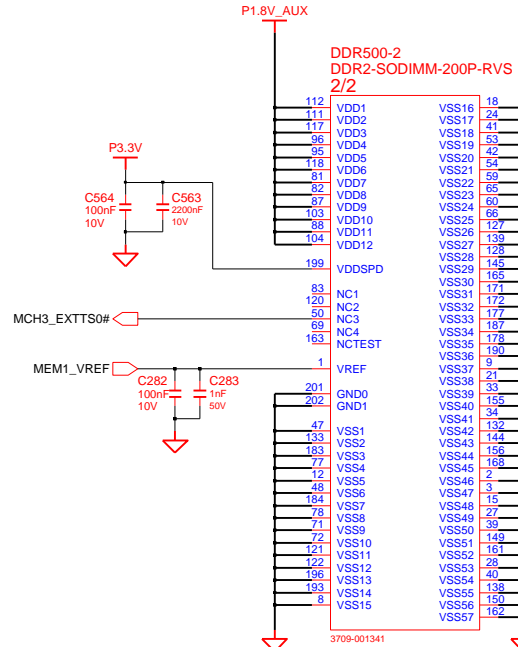
DDR SO-DIMM #0

Height : 5.2mm (Reverse)



DDR500-1
DDR2-SODIMM-200P-RVS
1/2

ME POWER RAIL UNDER ME ENABLE



3709-001341

Tyco/Foxconn : 3709-001341
Suyin : 3709-001502

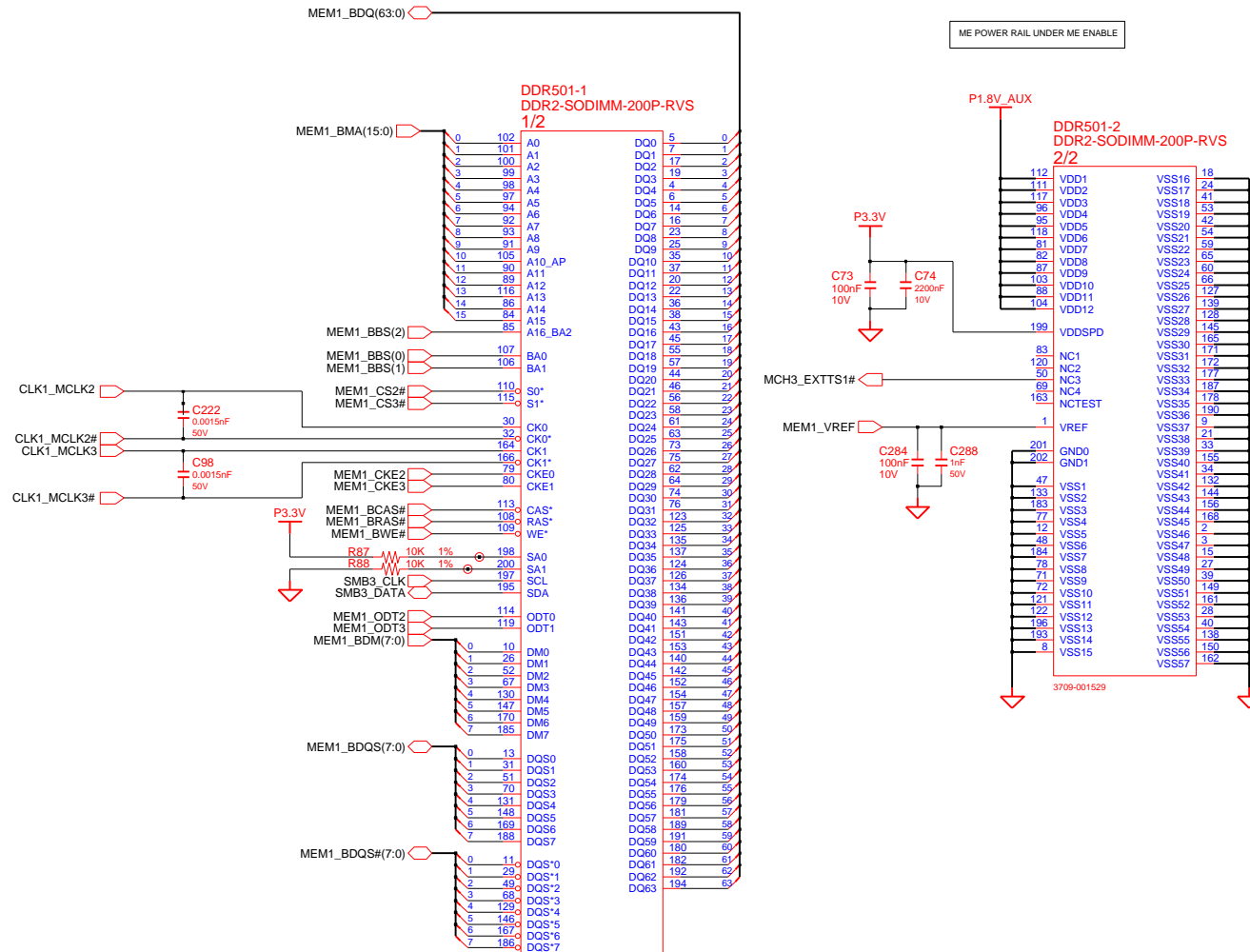
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CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)			PART NO. BA41-01024*6A
APPROVAL	YB CHUN	REV	1.00		SODIMM DDR2	
MODULE CODE		LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	18	OF 49

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DDR SO-DIMM #1

Height : 9.2mm (Reverse)

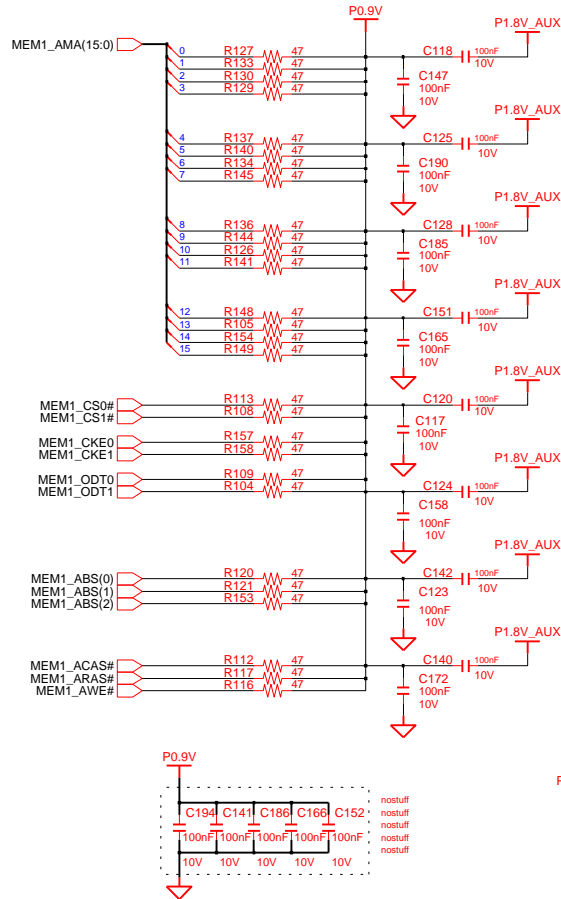


Foxcon : 3709-001390
Suyin : 3709-001503

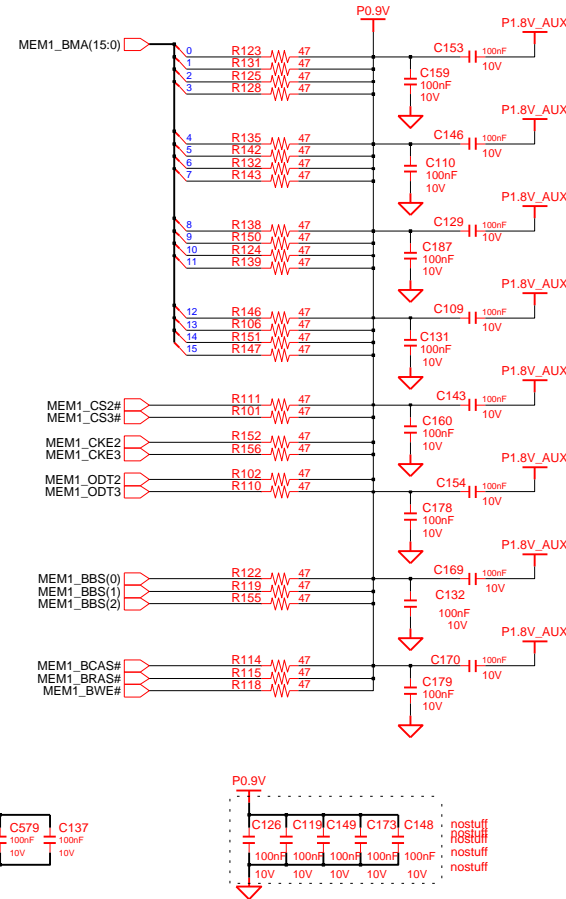
DESIGN	HS CHO	DATE	9/1/2008	TITLE	DRESDEN-INT MAIN	SAMSUNG ELECTRONICS
CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)			
APPROVAL	YB CHUN	REV	1.00		SODIMM DDR2	PART NO. BA41-01024*6A
MODULE CODE		LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	19	OF 49

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SODIMM TERMINATION



Place near SO-DIMM0



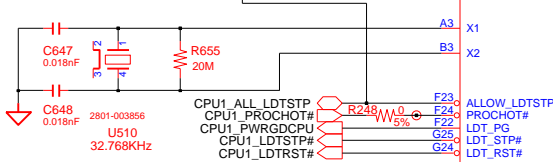
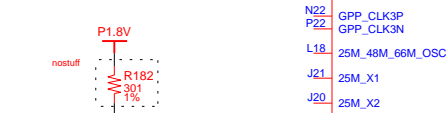
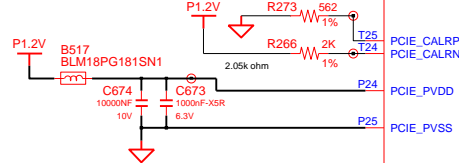
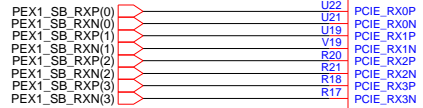
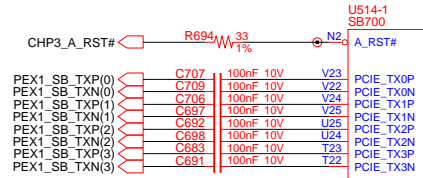
Place near SO-DIMM1

DRAW	HS CHO	DATE	5/28/2007	TITLE	DRESDEN-INT	SAMSUNG
CHECK	HS LEE / BM LEE	DEV. STEP	MP<PR>			ELECTRONICS
APPROVAL	YB CHUN	REV	1.00		SODIMM TERMINATION	PART NO.
MODULE CODE	undefined	LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	20	OF 49
						BA41-01024*6A

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SB700(1/4)



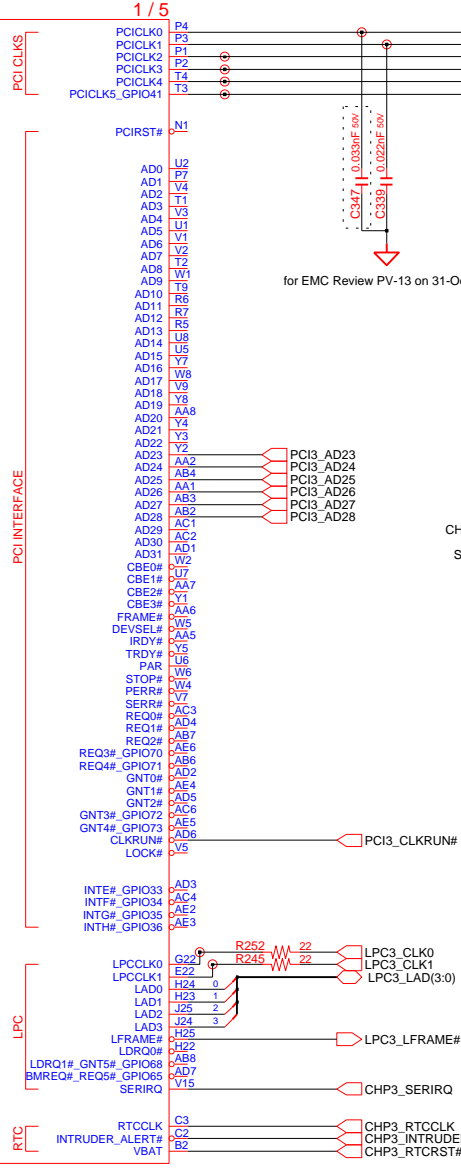
PCI EXPRESS INTERFACE

CLOCK GENERATOR

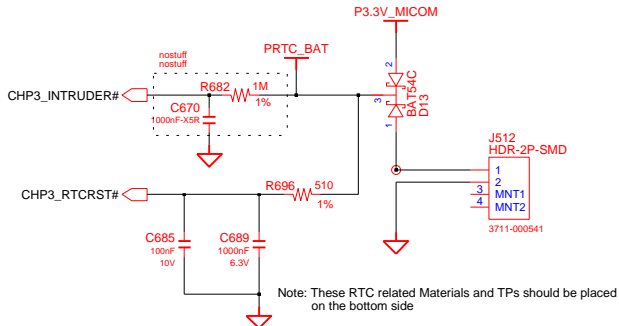
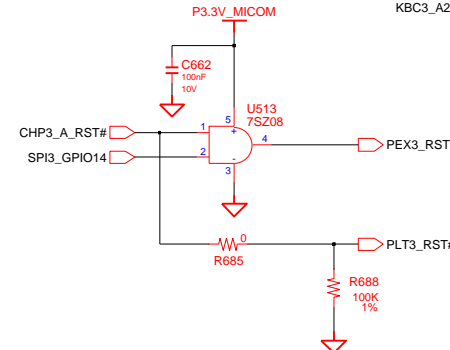
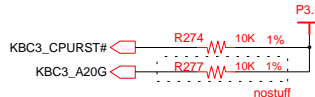
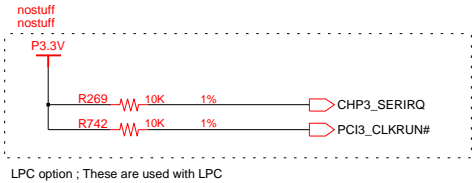
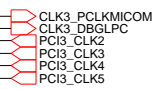
RTC XTAL

CPU

RTC



for EMC Review PV-13 on 31-Oct-08



DESIGN	HS CHO	DATE	3/19/2008	TITLE	DRESDEN-INT MAIN SB700 1/4	SAMSUNG ELECTRONICS
CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)			PART NO. BA41-01024-6A
APPROVAL	YB CHUN	REV	1.00			
MODULE CODE	undefined	LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	21	OF 49

DRAW		HS CH0	DATE	1/10/2008		DRESDEN-INT MAIN SB700 3/4		SAMSUNG ELECTRONICS	
CHECK		HS LEE / BM LEE	REV.	STEP	MP(PR)				
APPROVAL		YB CHUN	REV	1.00					
MODULE CODE		undefined		LAST EDIT		December 24, 2008 14:36:53 PM		PAGE	23 OF 49

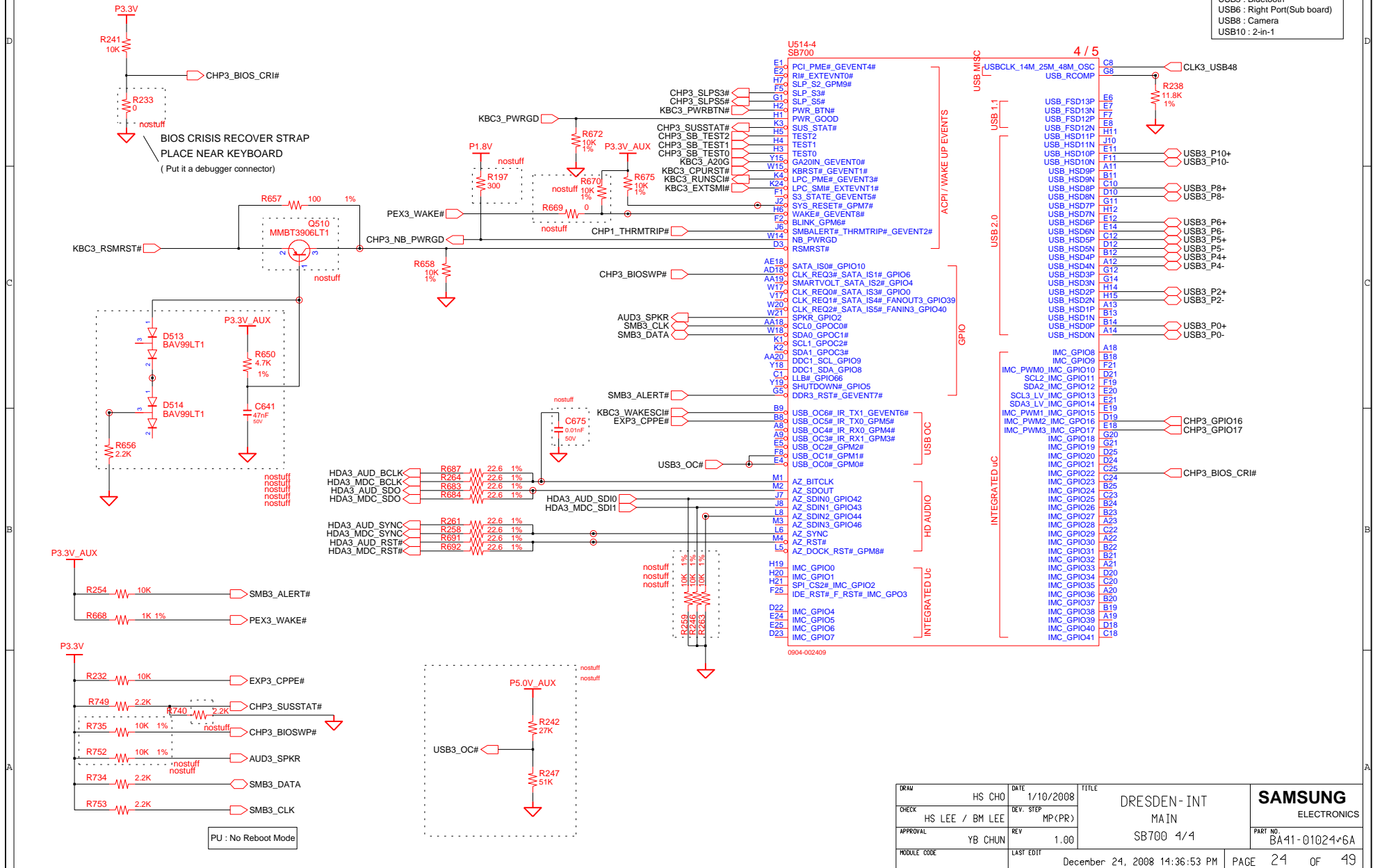
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SB700(4/4)

USB0 and 6 ports should be
connected with external ports

USB0 : 2 : Rear Port(Sub board)
USB4 : Express USB
USB5 : Bluetooth
USB6 : Right Port(Sub board)
USB8 : Camera
USB10 : 2-in-1

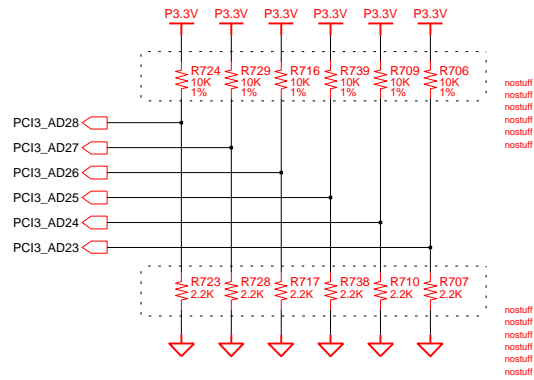


DRAW	HS CHO	DATE	1/10/2008	TITLE	DRESDEN-INT MAIN SB700 4/4	SAMSUNG ELECTRONICS
CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)			PART NO. BA11-01024*6A
APPROVAL	YB CHUN	REV	1.00			
MODULE CODE		LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	24	OF 49

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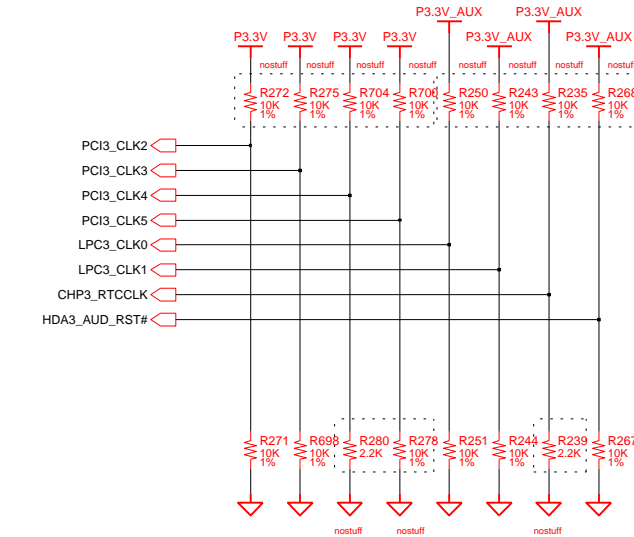
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SB700 HW STRAP

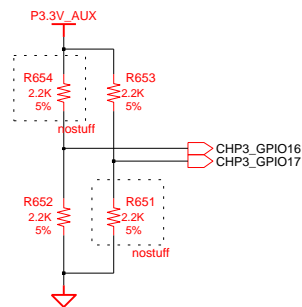
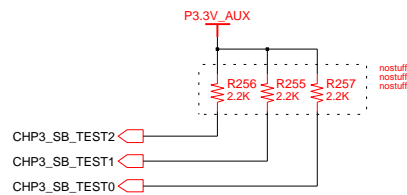


DEBUG STRAPS

STRAP	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED



STRAP	PCI3_CLK2	PCI3_CLK3	PCI3_CLK4	PCI3_CLK5	LPC3_CLK0	LPC3_CLK1	RTC_CLK	AUD_RST#
HIGH	BOOTFAIL TIMER ENABLED	USER DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC	ENABLE PCI MEM BOOT
LOW	BOOTFAIL TIMER DISABLED	IGNORE DEBUG STRAPS	RESERVED	RESERVED	EC DISABLED	CLKGEN DISABLED	EXRERNAL RTC (PD on X1. Apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT



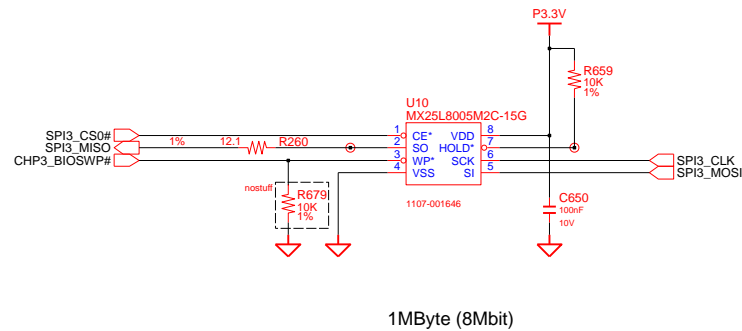
GPIO17	GPIO16
ROM TYPE	
H, H = PCI ROM	
H, L = SPI ROM	
L, H = LPC ROM	
L, L = FWH ROM	

DRAW	HS CHO	DATE	1/10/2008	TITLE	DRESDEN-INT	SAMSUNG ELECTRONICS
CHECK	HS LEE / BM LEE	DEV. STEP	MP<PR>			
APPROVAL	YB CHUN	REV	1.00		SB700 HW STRAP	PART NO. BA41-01024-6A
MODULE CODE		LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	25	OF 49

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BIOS ROM



- | | | | |
|----|---|----|---------------------------------|
| 02 | VERIFY REAL MODE | 66 | CONFIGURE ADVANCE CACHE REG. |
| 03 | DISABLE NMI | 6A | DISPLAY EXTERNAL CACHE SIZE |
| 04 | GET CPU TYPE | 6C | DISPLAY SHADOW MESSAGE |
| 06 | INIT. SYSTEM H/W | 6E | DISPLAY NON-DISPOSABLE SEGMENT |
| 08 | INIT. CHIPSET REG. | 70 | DISPLAY ERROR MESSAGE |
| 09 | SET IN POST FLAG | 72 | CHECK FOR CONFIGURATION ERROR |
| 0A | INIT CPU.REG | 74 | TEST REAL-TIME CLOCK |
| 0B | CPU CACHE ON | 76 | CHECK FOR KEYBOARD ERROR |
| 0C | INIT.CACHE TO POST | 7C | SETUP HARDWARE INTERRUPT VECTOR |
| 0E | INIT. I/O VALUE | 7E | TEST COPROCESSER IF PRESENT |
| 0F | ENABLE THE L-BUS IDE | 80 | DISABLE ON-BOARD I/O PORT |
| 10 | INIT. POWER MANAGER | 82 | DETECT AND INSTALL EXT.RS232C |
| 11 | LOAD ALTERNATE REG. | 84 | DETECT AND INSTALL EXT.PARALLEL |
| 13 | PCI BUS MASTER RESET
WITH INITIAL POST VALUE | 86 | RE-INIT. ON-BOARD I/O PORT |
| 14 | INIT. KEYBOARD CONTROLLER | 88 | INIT. BIOS DATA ROM |
| 16 | CHECK CHECKSUM | 8A | INIT.EXTENDED BIOS DATA AREA |
| 18 | 8254 TIMER INIT. | 8C | INIT. FDD CONTROLLER |
| 1A | 8237 DMA CONTROLLER INIT. | 9A | SHADOW OPTION ROMS |
| 1C | RESET INTERRUPT CONTROLLER | 9C | SETUP POWER MANAGEMENT |
| 20 | TEST DRAM REFRESH | 9E | ENABLE H/W INTERRUPT |
| 22 | TEST 8742 KEYBOARD CONTROLLER | A0 | SET TIME OF DAY |
| 24 | SET ES SEGMENT REG. TO 4GB | A4 | INIT. TYPOMATIC RATE |
| 26 | ENABLE A20 | A8 | ERASE F2 PROMPT |
| 28 | AUTO SIZING DRAM | AA | SCAN FOR F2 KEY STROKE |
| 32 | COMPUTE THE CPU SPEED | AC | ENTER SETUP |
| 34 | TESET CMOS RAM | AE | CLEAR IN POST FLAG |
| 38 | SHADOW SYSTEM BIOS ROM | B0 | CHECK FOR ERRORS |
| 3A | AUTO SIZING CACHE | B2 | POST DONE-PREPARE TO BOOT O/S |
| 3C | CONFIGURE ADVANCED CHIPSET REG. | B4 | ONE BEEP |
| 3D | LOAD ALTER REG. WITH CMOS VALUE | B6 | CHECK PASSWORD (OPTION) |
| 42 | INIT. INTERRUPT VECTOR | B7 | ACPI INIT |
| 44 | INIT. BIOS INTERRUPT | BA | DMI INIT |
| 46 | CHECK ROM COPYRIGHT NOTICE | BE | CLEAR SCREEN |
| 47 | INIT. I20 SUPPORT IF INSTALLED | C0 | TRY BOOT WITH INT19 |
| 48 | CHECK VIDEO CONFIGURE AGAINST CMOS | D0 | INTERRUPT HANDLER ERROR |
| 49 | INIT. PCI BUS AND DEVICE | D2 | UNKNOWN INTERRUPT ERROR |
| 4A | INIT. ALL VIDEO BIOS ROM | D4 | PENDING INTERRUPT ERROR |
| 4C | SHADOW VIDEO BIOS ROM | D6 | SHUTDOWN 5 |
| 50 | DISPLAY CPU TYPE AND SPEED | D8 | SHUTDOWN ERROR |
| 52 | TEST KEYBOARD | DA | EXTENDED BLOCK MOVE |
| 54 | SET KEYCLICK IF ENABLED | DC | SHUTDOWN 10 |
| 56 | ENABLE KEYBOARD | 89 | ENABLE NMI |
| 58 | TEST FOR UNEXPECTED INTERRUPTS | 90 | INIT. HDD CONTROLLER |
| 5A | DISPLAY "PRESS SETUP" | 91 | INIT. LOCAL BUS HDD CONTROLLER |
| 5C | TEST RAM BETWEEN 512K AND 640K | 92 | JUMP TO USER PATCH 2 |
| 60 | TEST EXTENDED MEMORY | 94 | DISABLE A20 ADDRESS LINE |
| 62 | TEST EXTENDED MEMORY ADDRESS LINE | 96 | CLEAR HUGE ES SEGMENT REG. |
| 64 | JUMP TO USER PATCH 1 | 98 | SEARCH FOR OPTION ROMS |

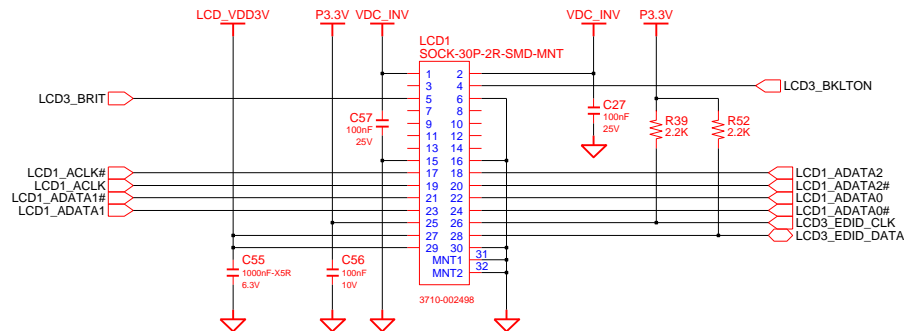
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CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)		SPI_BIOS_ROM	ELECTRONICS
APPROVAL	YB CHUN	REV	1.00		BIOS_ROM (1M)	PART NO.
MODULE CODE		LAST EDIT				BA41-01024-6A
				December 24, 2008 14:36:53 PM	PAGE	32 OF 60

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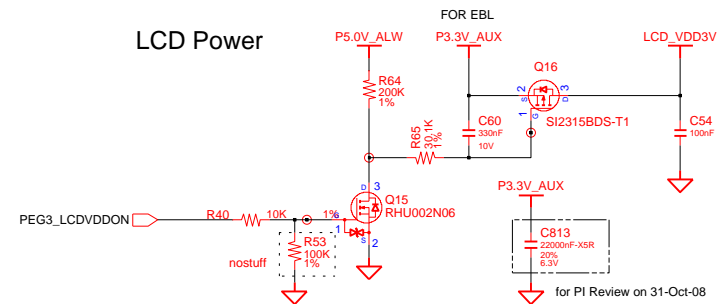
LVDS

1CH WXGA LCD CONNECTOR

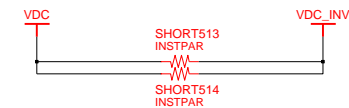


Signals : #40AWG
LCD Vdd : #36AWG
Inverter Vdd : #36AWG
GND : #36AWG

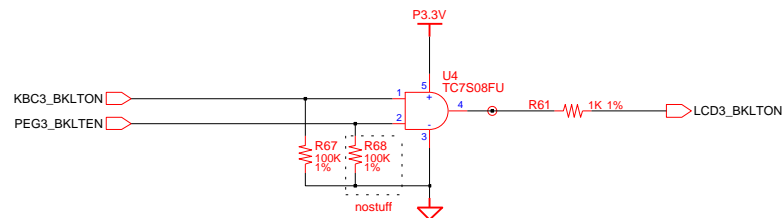
LCD Power



Inverter Power



Backlight ON



DRAW	HS CHO	DATE	8/12/2006	TITLE	DRESDEN-INT	SAMSUNG
CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)	LCD_IF	ELECTRONICS	
APPROVAL	YB CHUN	REV	1.00	LVDS	PART NO.	BA41-01024-6A
MODULE CODE	undefined	LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	34	OF 63

CRT CONNECTOR

The schematic diagram illustrates the internal circuitry of a CRT connector. It shows the following components and connections:

- Input Signals:** CRT3_RED, CRT3_GREEN, CRT3_BLUE, CRT3_HSYNC, CRT3_VSYNC, CRT5_DDCDATA, CRT5_DDCCLK.
- Power Supply:** P3.3V, VCC_CRT, P5.0V.
- Resistors:** R168, R174, R215, R208, R193, R180, R198, R183, R598, R587, R586, R213, R207.
- Capacitors:** C286, C280, C276, C289, C285, C279, C251, C245, C275, C280, C261, C246, C268.
- Inductors:** L1, L2, L3.
- Diodes:** D511, D510, D509, D506, D507, D508, D509, D510, D511, BAV99LT1.
- Transistors:** U7, U6 (SN74AHC1G125DCKR).
- Connectors:** 3701-001403.

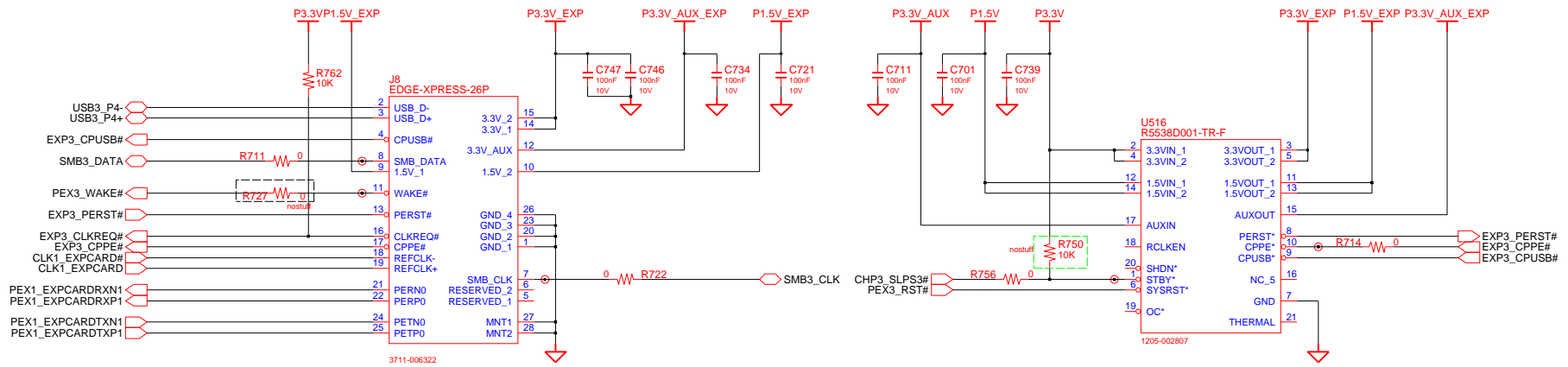
The circuit is designed to interface the CRT connector with the system's power and signal lines. It includes a 3701-001403 connector for the CRT signal lines. The diagram also shows the internal connections of the CRT connector, including the 3701-001403 connector and the 3701-001403 connector.

DRAW		DATE	8/12/2006	DRESDEN-INT CRT_IF CRT		SAMSUNG ELECTRONICS	
CHECK		DEV. STEP	MP(P/R)				
APPROVAL		REV	1.00				
YB CHUN						PART NO. BA41-01024-6A	
MODULE CODE		LAST EDIT		December 24, 2008 14:36:53 PM		PAGE	35 OF 63

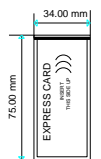
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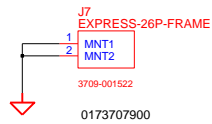
EXPRESS CARD



EXPRESS CARD
Type 1 module



34.00 mm W
X
75.00 mm L
X
5.00 mm H



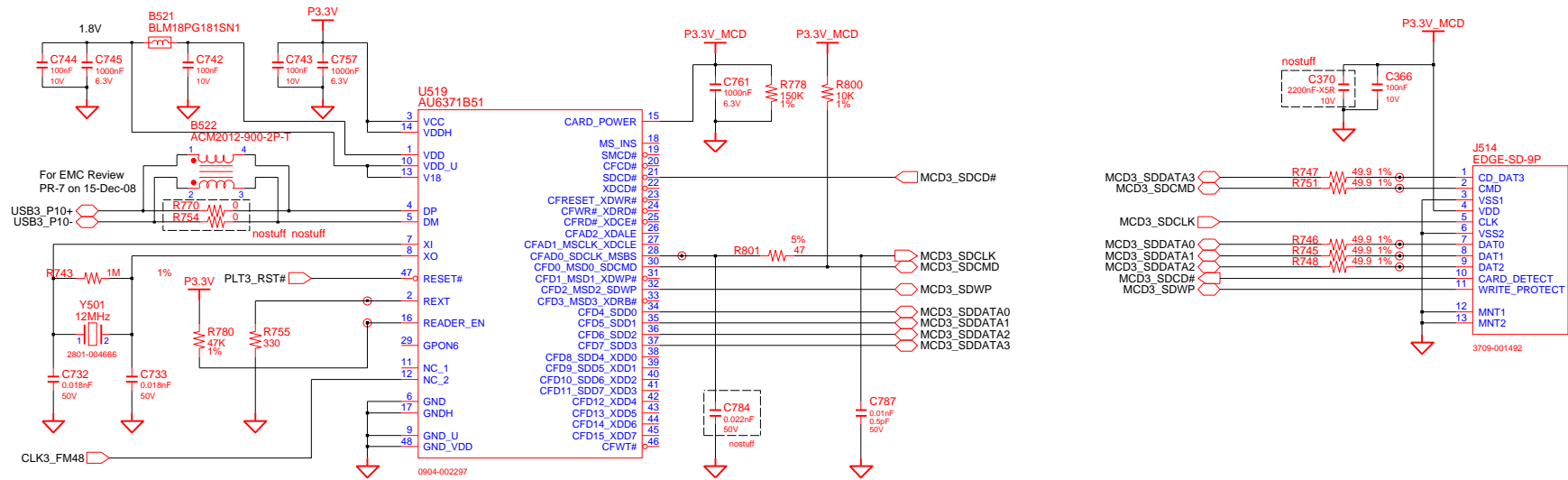
0173707900

DRAW	HS CHO	DATE	8/17/2007	TITLE	DRESDEN-INT EXPRESS_CARD	SAMSUNG ELECTRONICS
CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)			
APPROVAL	YB CHUN	REV	1.00		EXPRESS_CARD (34mm)	PART NO. BA41-01024-6A
MODULE CODE		LAST EDIT				
				December 24, 2008 14:36:53 PM	PAGE	42 OF 60

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MEMORY CARD (2 IN 1)

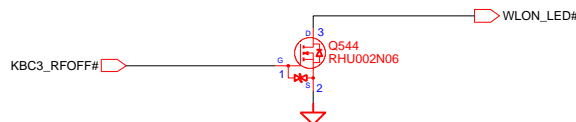
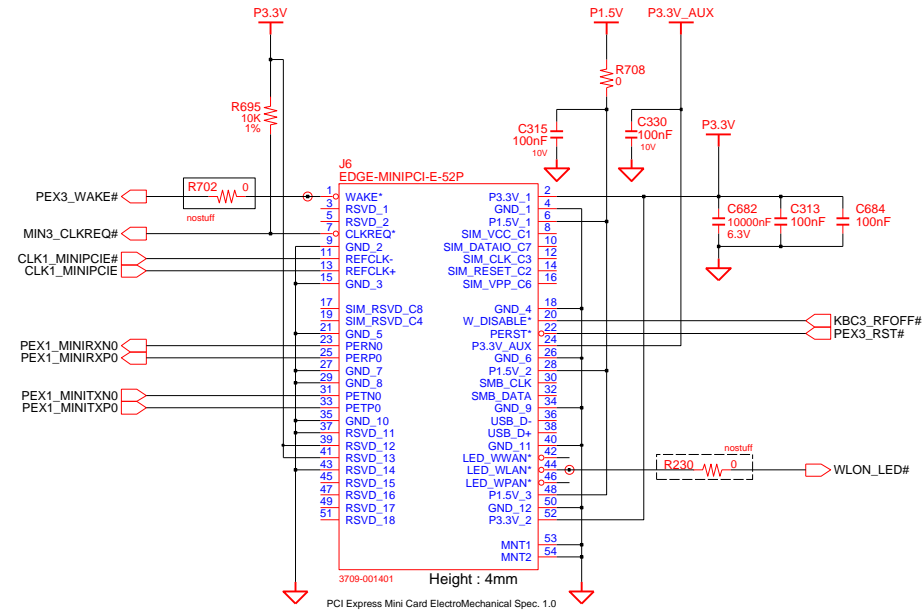


DRAW	HS CHO	DATE	8/17/2007	TITLE	DRESDEN-INT	SAMSUNG
CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)		MEMORY CARD	ELECTRONICS
APPROVAL	YB CHUN	REV	1.00		MMC (2-IN-1)	PART NO.
MODULE CODE		LAST EDIT				BA41-01024-6A
				December 24, 2008 14:36:53 PM	PAGE	41 OF 60

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Mini PCI-E Card (WLAN)



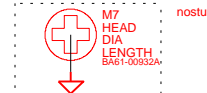
WLAN MINICARD NUT
Height : 4mm



For Full size minicard

(Top)

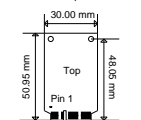
WLAN MINICARD NUT
Height : 4mm



For half size minicard

(Top)

Mini PCI Express Card



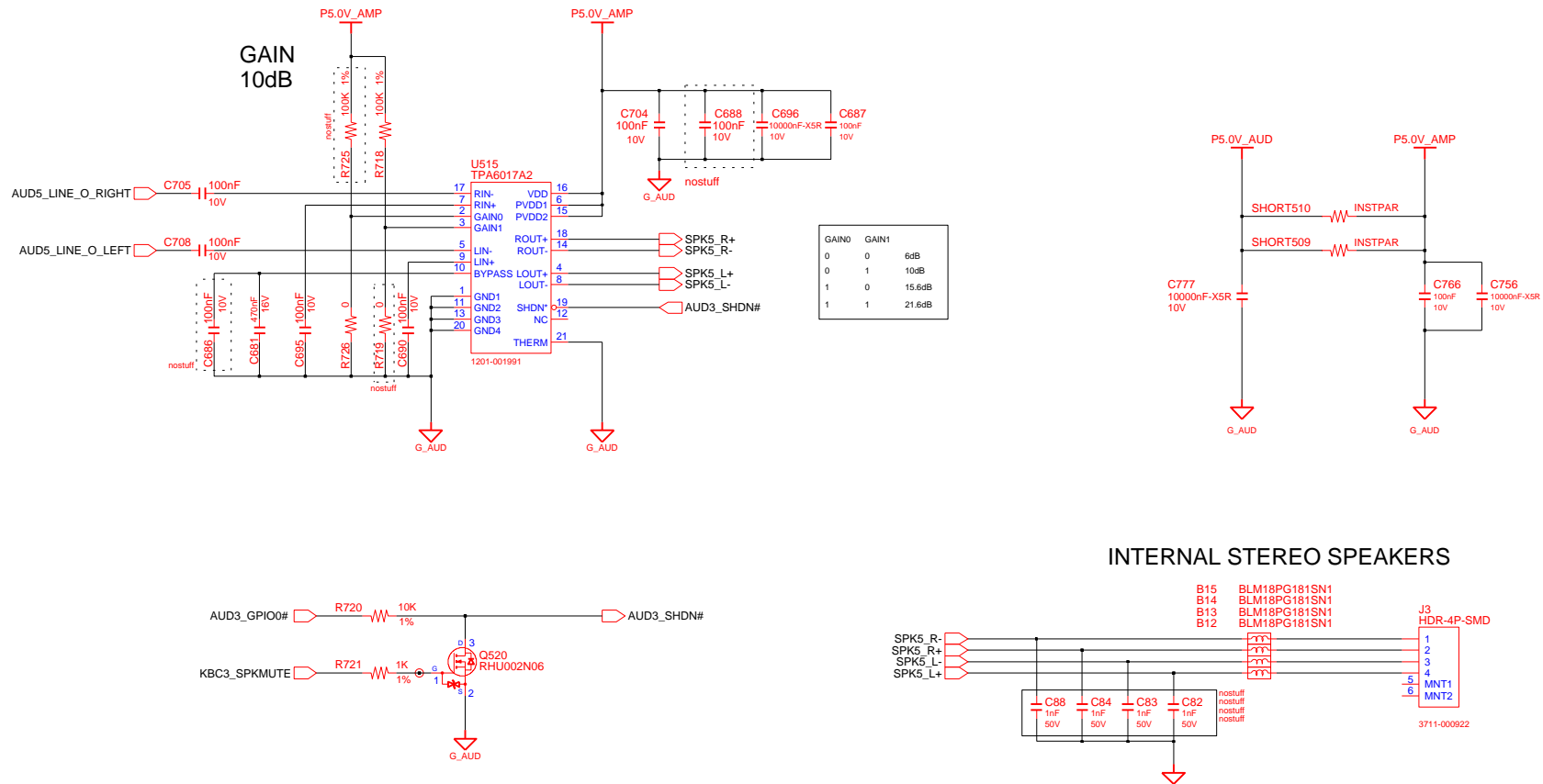
Odd Pins : Top side
Even Pins : Bottom Side

DRAWN	HS CHO	DATE	8/12/2006	TITLE	DRESDEN-INT	SAMSUNG
CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)		PCIE_MINICARD	ELECTRONICS
APPROVAL	YB CHUN	REV	1.00		WLAN	PART NO.
MODULE CODE	undefined	LAST EDIT				BA41-01024-6A
				December 24, 2008 14:36:53 PM	PAGE	40 OF 60

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AUDIO AMP & INT. SPEAKER

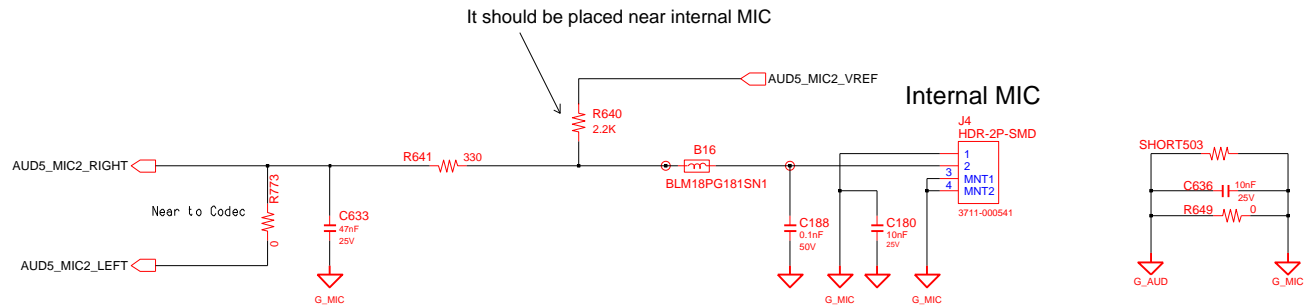


DRAW	HS CHO	DATE	10/25/2006	TITLE	DRESDEN-INT MAIN	SAMSUNG ELECTRONICS PART NO. BA41-01024-6A
CHECK	HS LEE / BM LEE	DEV. STEP	MP<PR>			
APPROVAL	YB CHUN	REV	1.00	AUDIO AMP & INT. SPEAKER		
MODULE CODE		LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	28 OF 49	

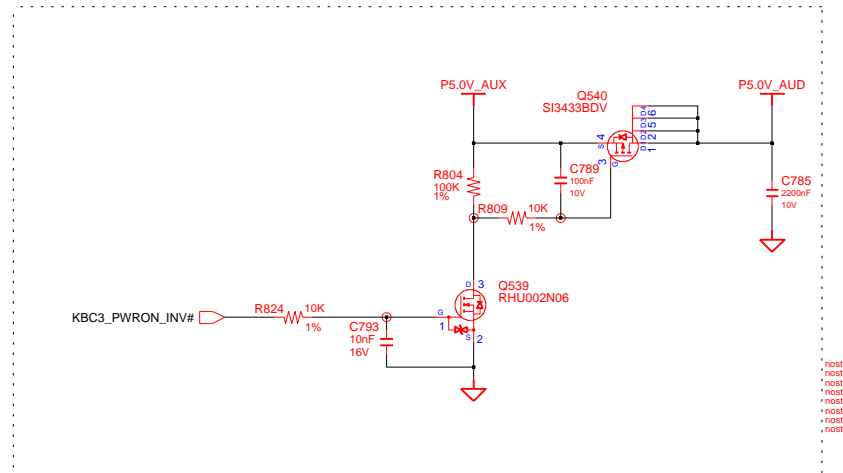
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AUDIO POWER & INT. MIC



Audio Power (nostuff)

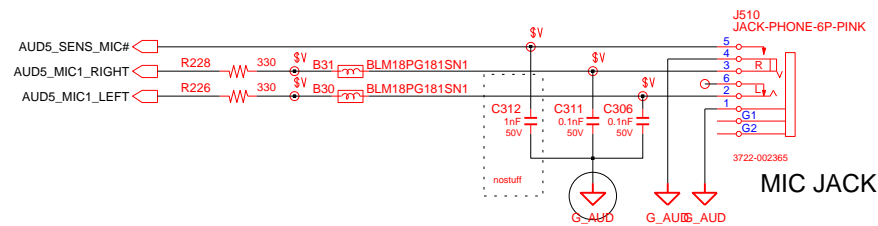
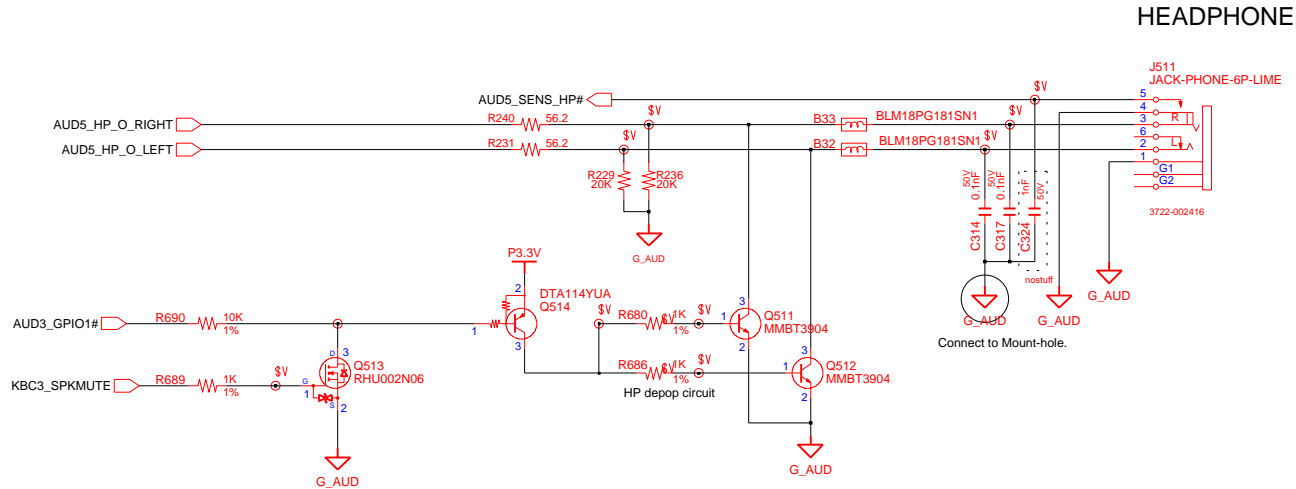


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CHECK	HS LEE / BM LEE	DEV. STEP	MP<PR>	REV	1.00	
APPROVAL	YB CHUN	LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	29	OF 49
MODULE CODE						

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HEADPHONE & EXT. MIC



The traces led to Audio Jacks have the width over 10mil

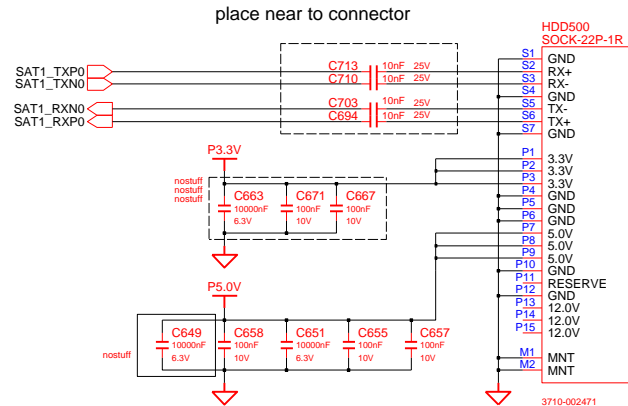
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CHECK	HS LEE / BM LEE	DEV. STEP	MP<PR>			
APPROVAL	YB CHUN	REV	1.00		HEADPHONE&EXT.MIC	PART NO. BA41-01024x6A
MODULE CODE		LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	30	OF 49

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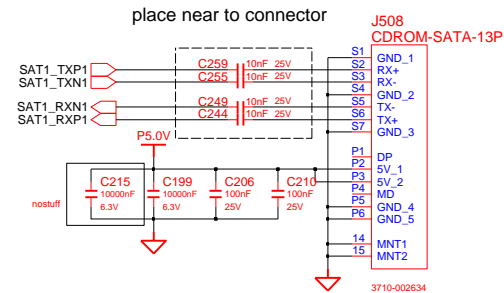
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SATA IF CONNECTOR

Main to HDD



Main to ODD

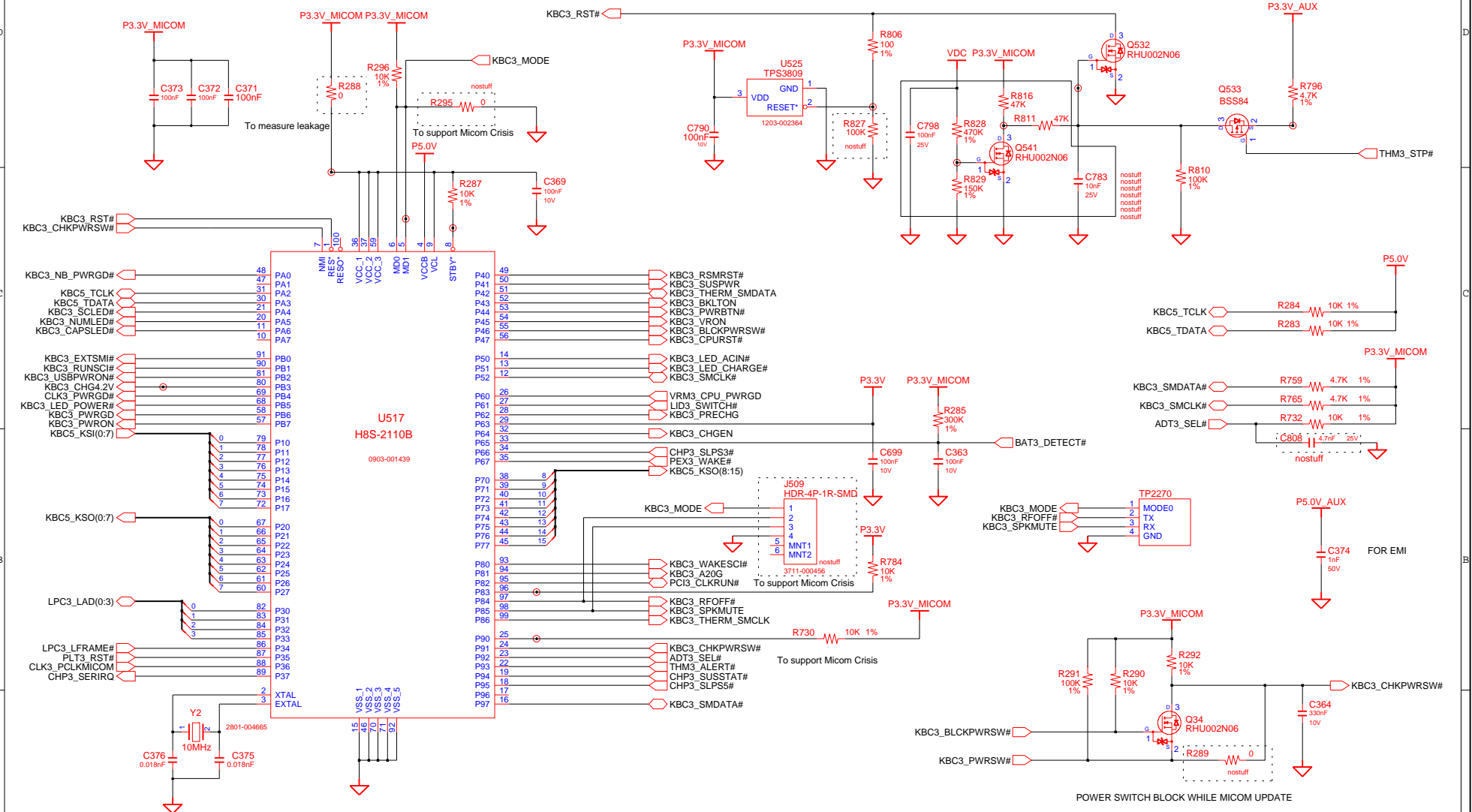


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MODULE CODE		LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	31	OF 49

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MICOM

MICOM RESET

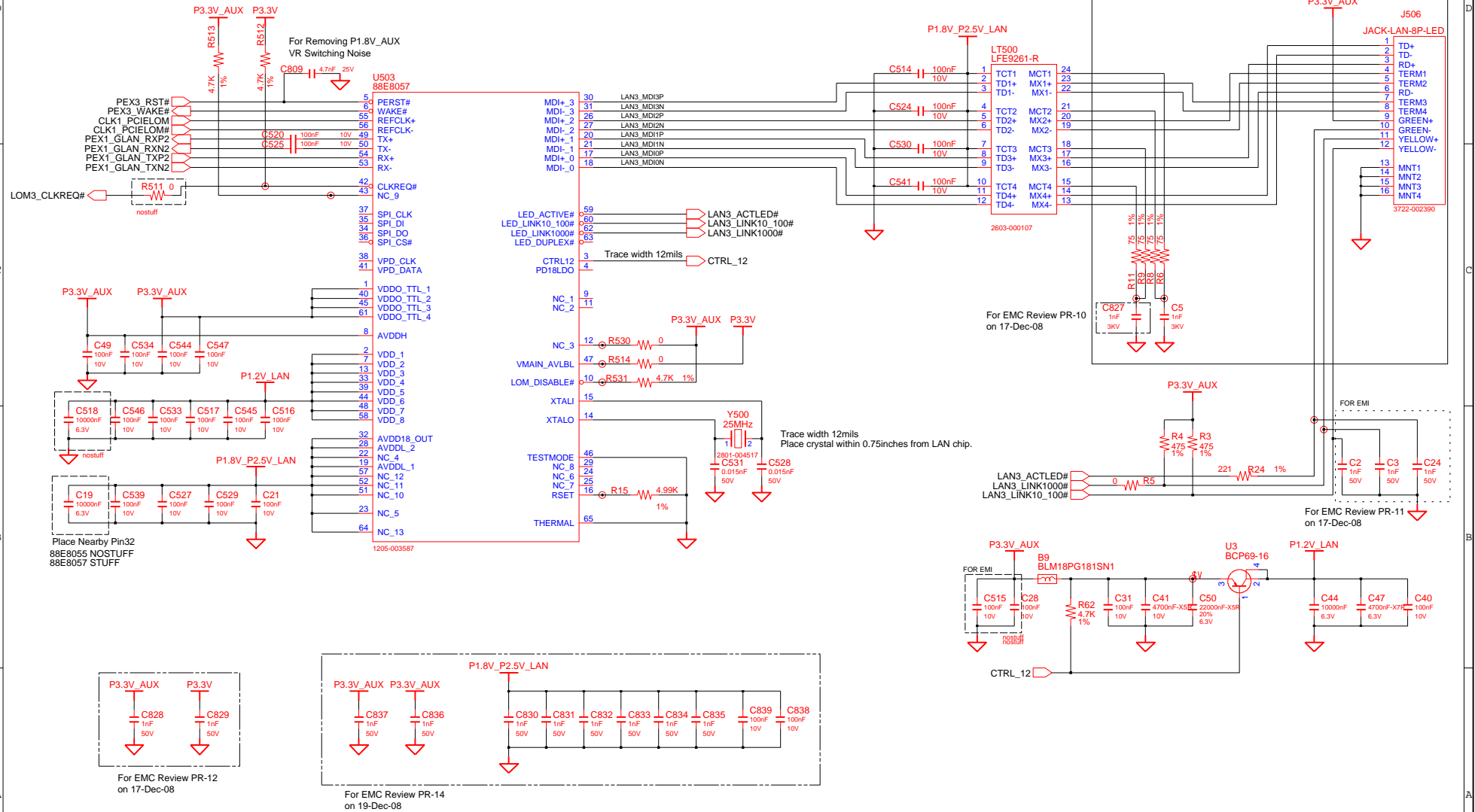


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APPROVAL	YB CHUN	REV	1.00		MICOM	
MODULE CODE		LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	32	OF 49

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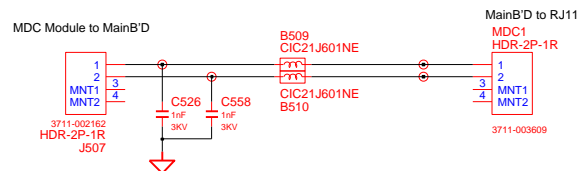
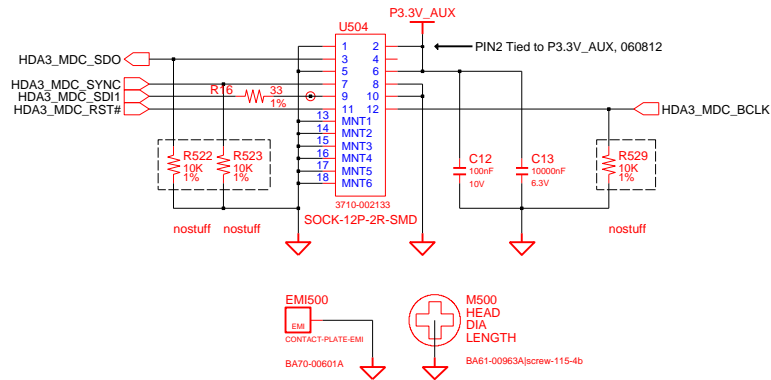
LAN (88E5057)



DRAW	HS CHO	DATE	11/8/2006	TITLE	DRESDEN-INT MAIN LAN (88E5057)	SAMSUNG ELECTRONICS
CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)			PART NO. BA41-01024*6A
APPROVAL	YB CHUN	REV	1.00			
MODULE CODE	undefined	LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	33	OF 49

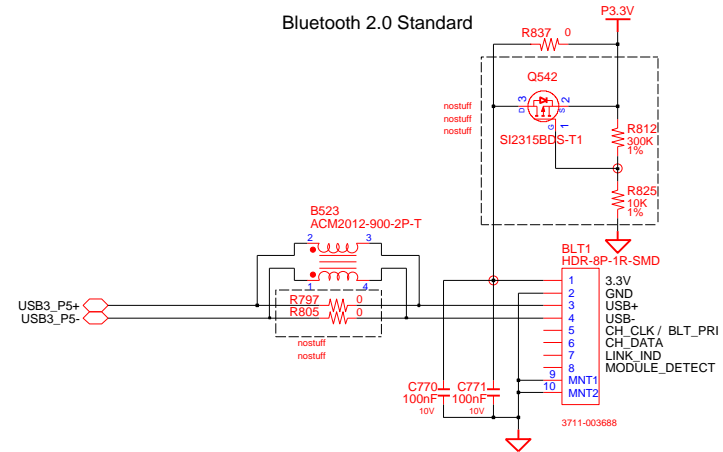
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MDC connector

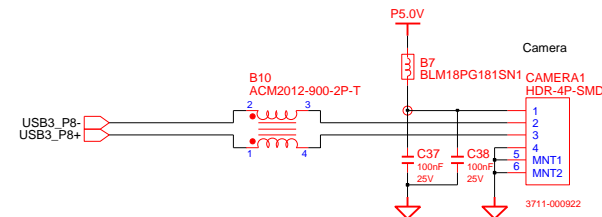


BLUETOOTH

Bluetooth 2.0 Standard



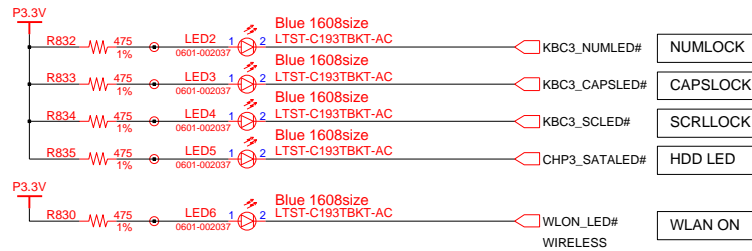
CAMERA



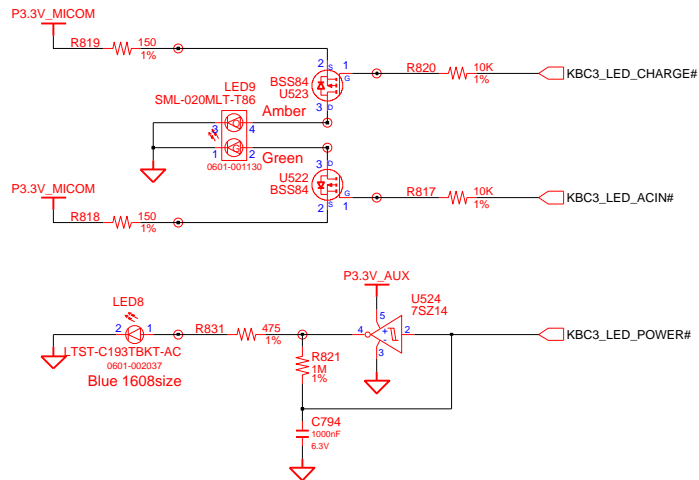
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CHECK	HS LEE / BM LEE	DEV. STEP	MP<PR>			PART NO. BA41-01024v6A
APPROVAL	YB CHUN	REV	1.00		CAMERA/BLUETOOTH/MDC	
MODULE CODE	undefined	LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	34	OF 49

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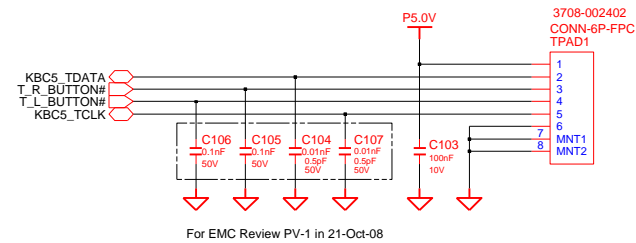
LEDS



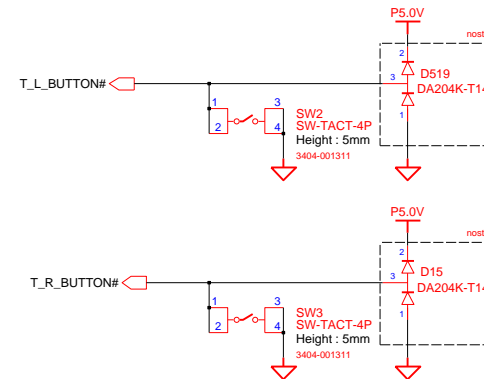
Adaptor-In / Charging LED



TOUCH PAD



TP_SWITCH

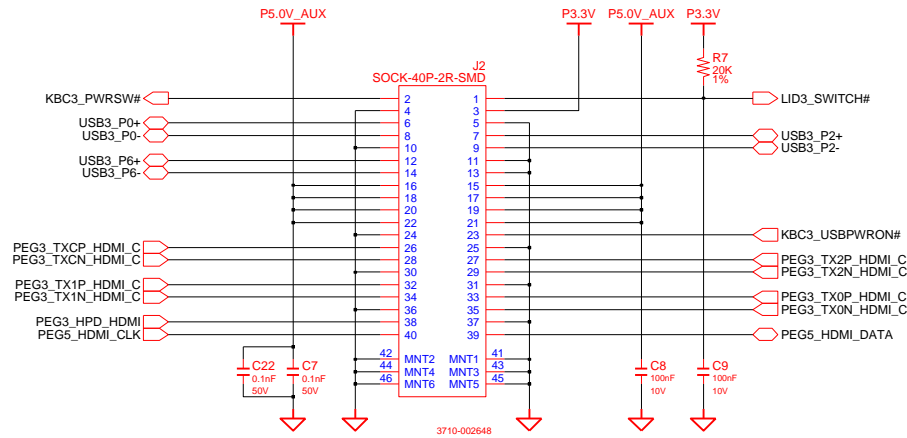


DRAW	HS CHO	DATE	8/14/2007	TITLE	DRESDEN-INT MAIN	SAMSUNG ELECTRONICS
CHECK	HS LEE / BM LEE	DEV. STEP	MP<PR>			PART NO. BA41-01024*6A
APPROVAL	YB CHUN	REV	1.00		LED/TOUCH PAD	
MODULE CODE	undefined	LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	35	OF 49

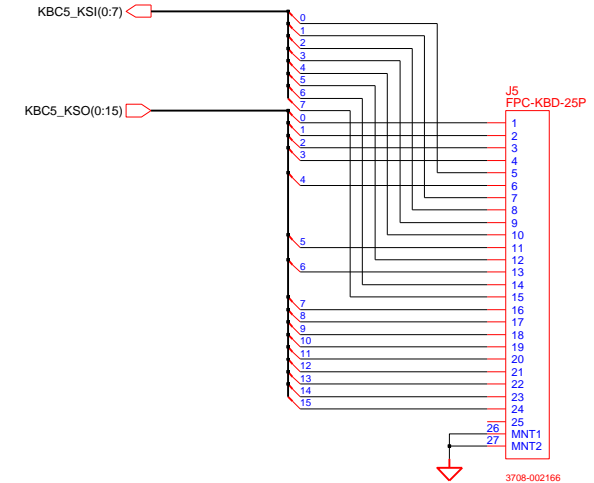
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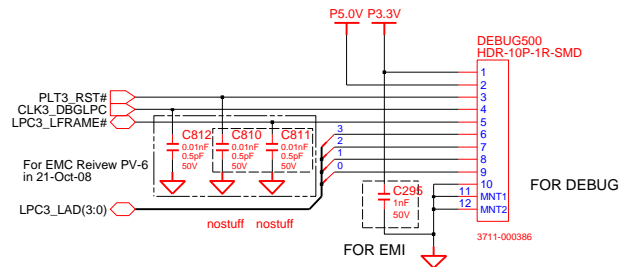
Main to SUB Connector



KEYBOARD



DEBUG PORT



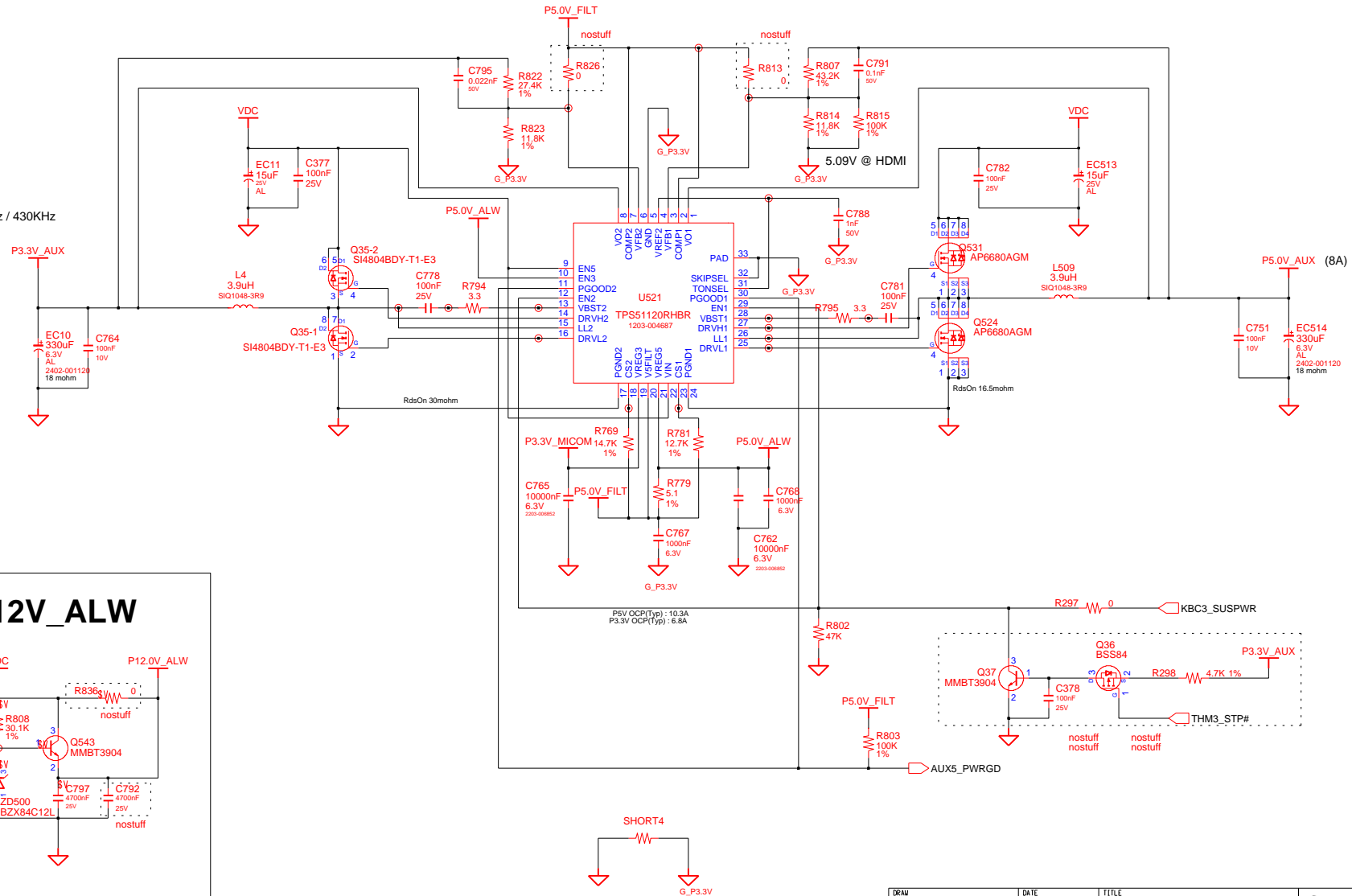
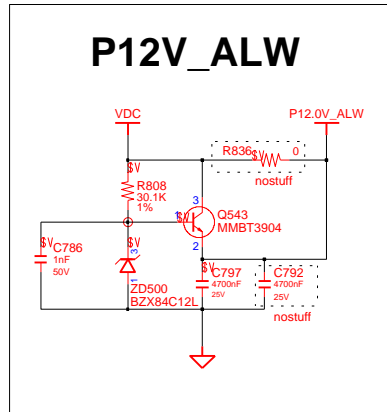
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CHECK	HS LEE / BM LEE	DEV. STEP	MP (PR)			PART NO. BA41-01024x6A
APPROVAL	YB CHUN	REV	1.00		SUB/DEBUG/KBD	
MODULE CODE	undefined	LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	36	OF 49

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P3.3V_AUX & P5.0V_AUX

TONSEL VREF2
5V / 3.3V : 280KHz / 430KHz
(4A)



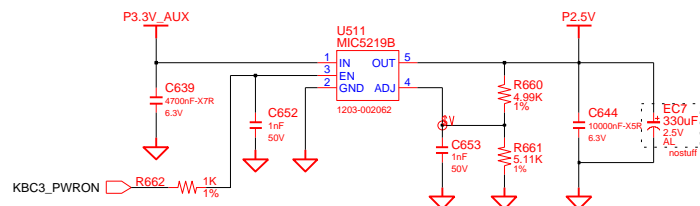
DRAW	HS CHO	DATE	2/13/2008	TITLE	DRESDEN-INT MAIN AUX POWER	SAMSUNG ELECTRONICS
CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)			PART NO. BA41-01024x6A
APPROVAL	YB CHUN	REV	1.00			
MODULE CODE		LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	38	OF 49

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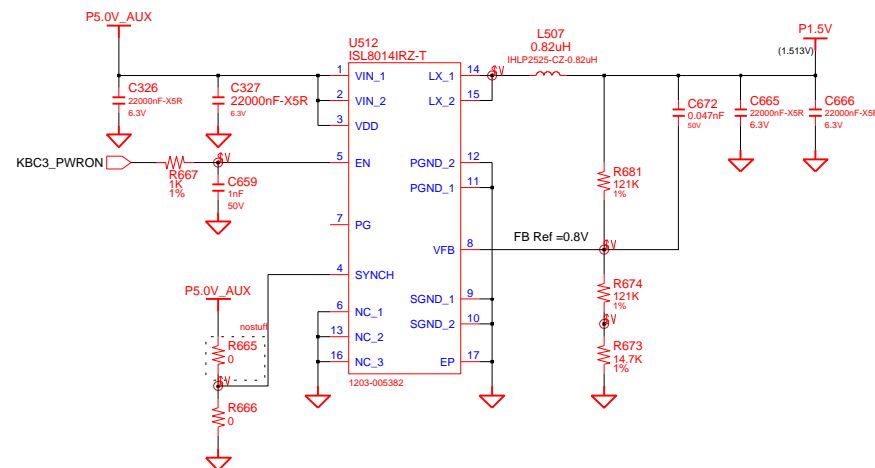
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CHIPSET POWER(P2.5V & P1.5V & P1.1V & P1.2V_AUX)

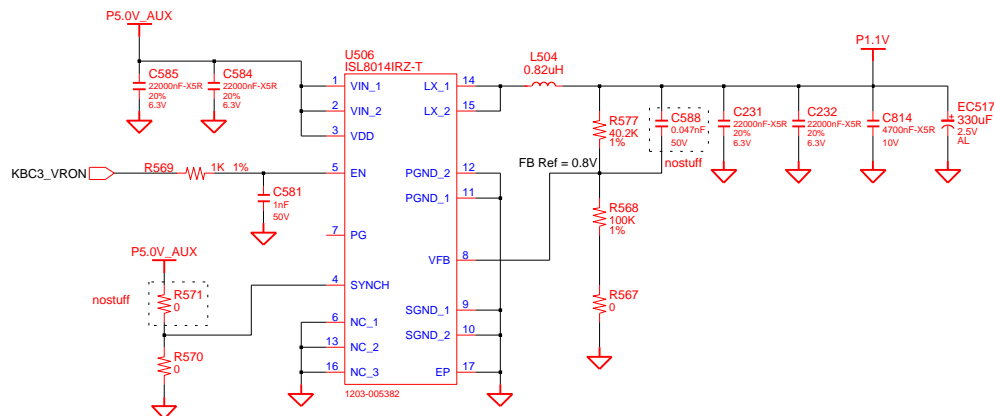
P2.5V



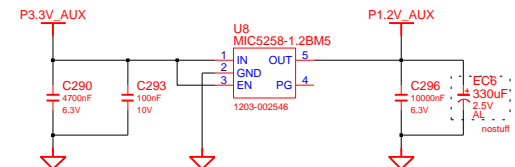
P1.5V



P1.1V



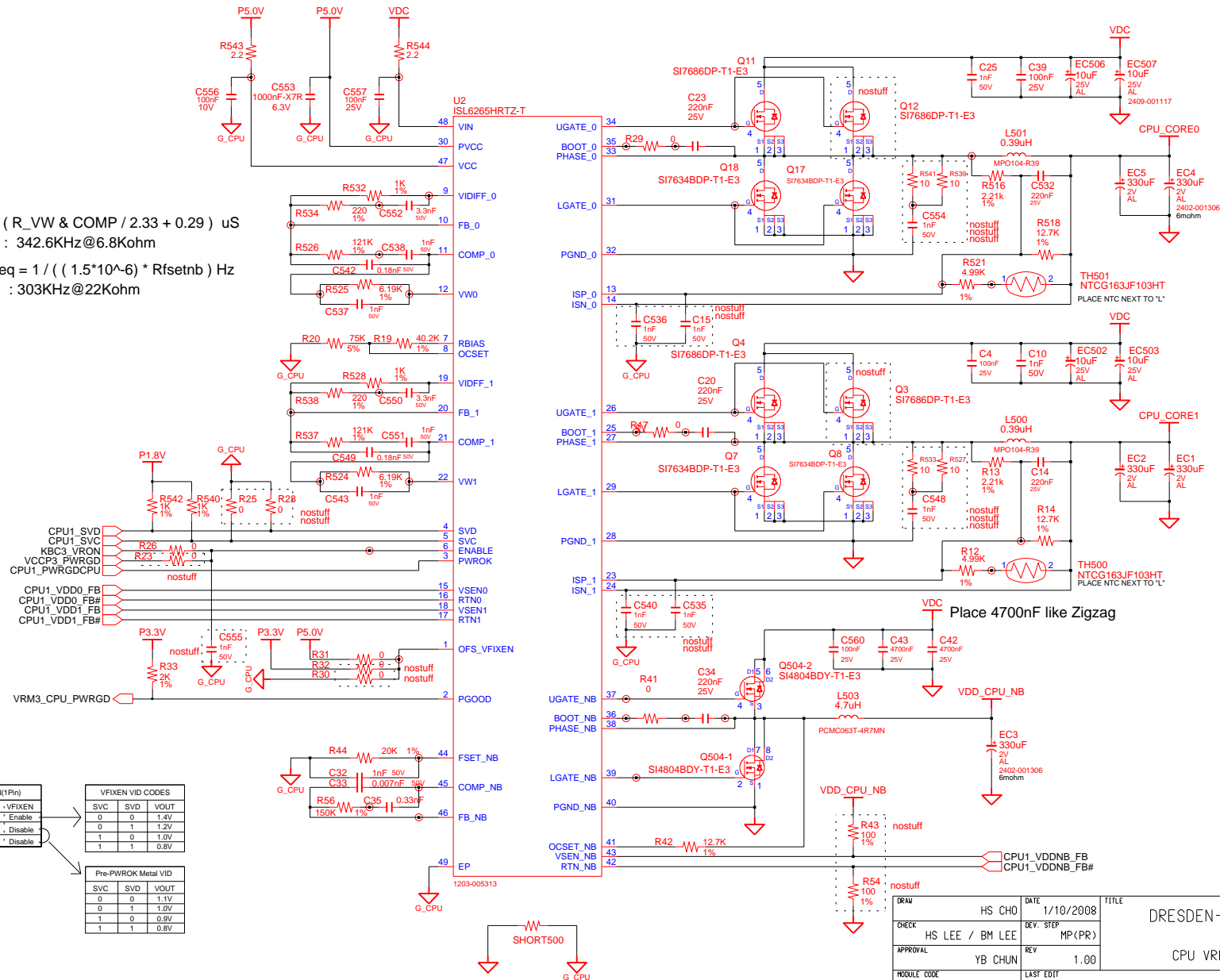
P1.2V_AUX



DRAW	HS CHO	DATE	1/10/2008	TITLE	DRESDEN-INT	SAMSUNG
CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)			ELECTRONICS
APPROVAL	YB CHUN	REV	1.00	CHIPSET POWER(2/2)	PART NO.	BA41-01024-6A
MODULE CODE		LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	40	OF 49

VDD Freq = (R_VW & COMP / 2.33 + 0.29) uS
: 342.6KHz@6.8Kohm

VDD_NB Freq = 1 / ((1.5*10⁻⁶) * Rfsetnb) Hz
: 303KHz@22Kohm



The diagram illustrates the relationship between the OFS/VFIXEN(1Pin) settings, the VFIXEN VID CODES, and the Pre-PWROK Metal VID settings.

OFS/VFIXEN(1Pin)

	OFS	VFIXEN
3.3V	Disable	Enable
GND	Enable	Disable
5V	Disable	Disable

Arrows indicate that the 3.3V and 5V settings of OFS/VFIXEN(1Pin) correspond to the VFIXEN VID CODES, and the 5V setting corresponds to the Pre-PWROK Metal VID.

VFIXEN VID CODES

SVC	SVD	VOUT
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

Pre-PWROK Metal VID

SVC	SVD	VOUT
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

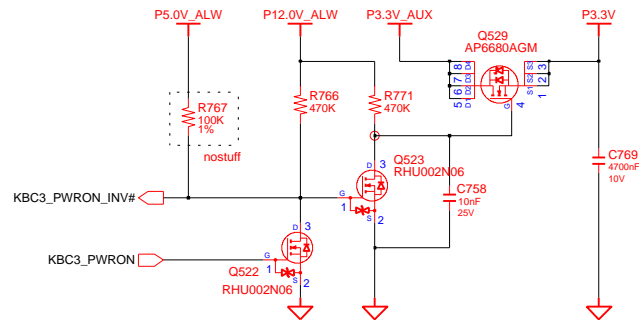
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CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)		
APPROVAL	YB CHUN	REV	1.00		
MODULE CODE	LAST EDIT				
			December 24, 2008 14:36:53 PM	PAGE	42 OF 49

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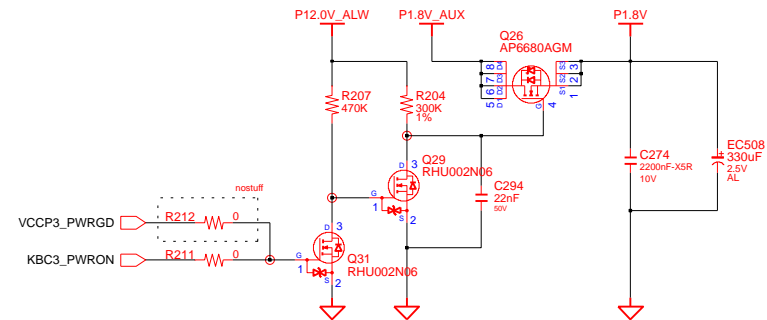
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Switched Power

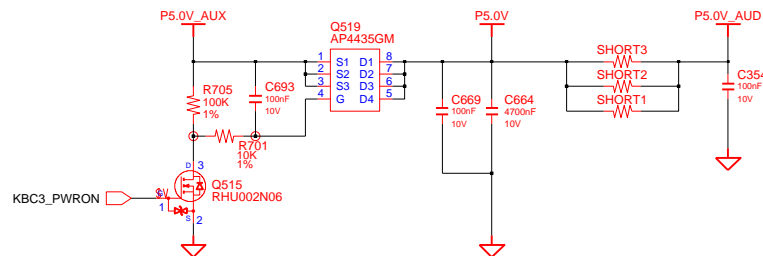
Switched Power On (P3.3V)



Switched Power On (P1.8V)



Switched Power On (P5.0V)

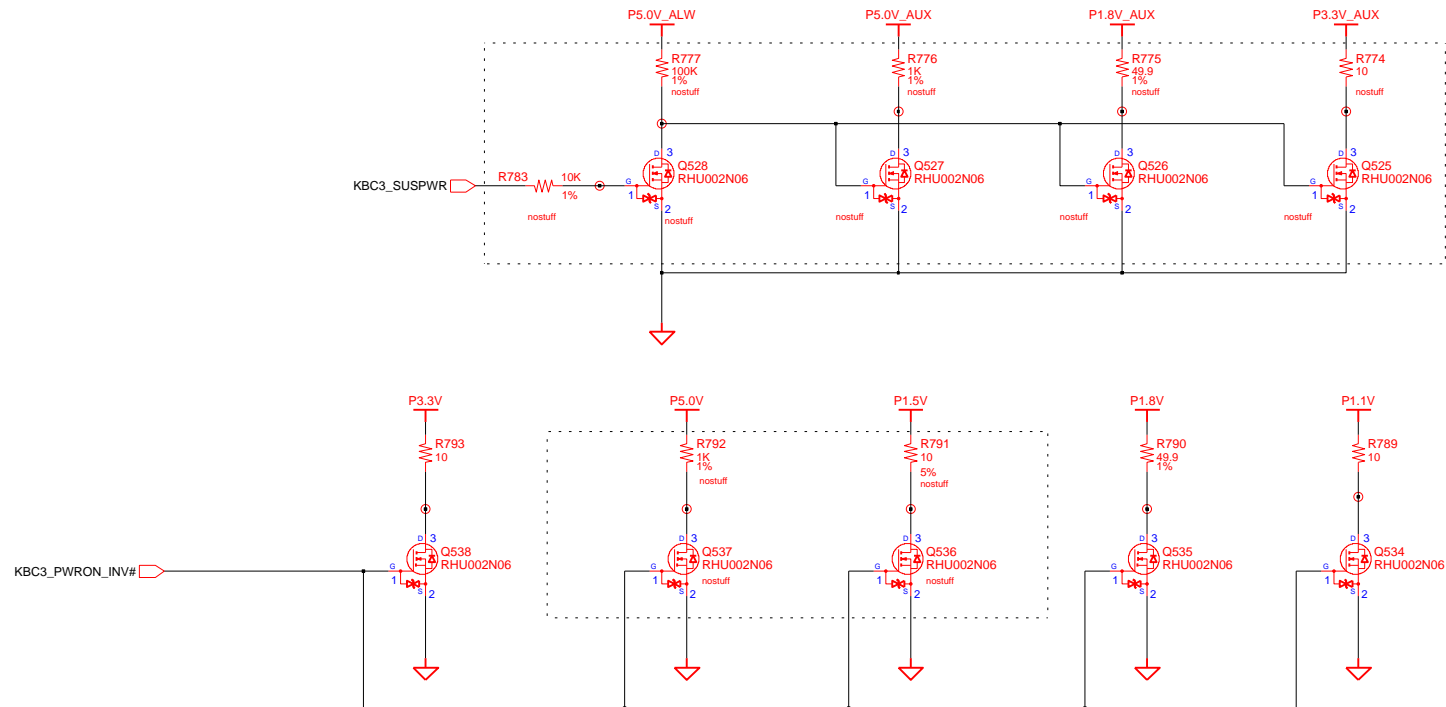


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CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)			
APPROVAL	YB CHUN	REV	1.00		Switched Power	PART NO. BA41-01024v6A
MODULE CODE	undefined	LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	43	OF 49

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POWER DISCHARGER

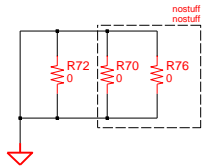
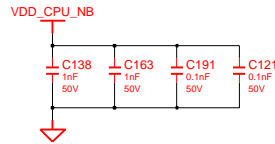
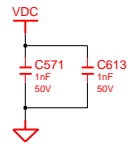
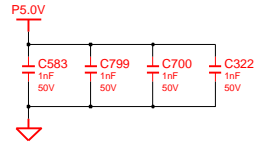
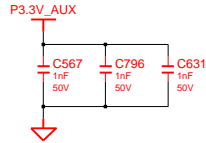


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MODULE CODE		LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	44	OF 49

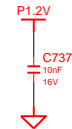
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EMC

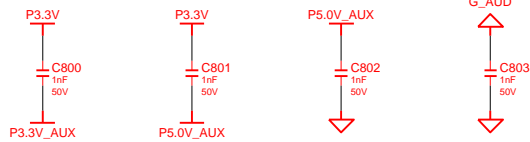


Added on 18-Sep-08

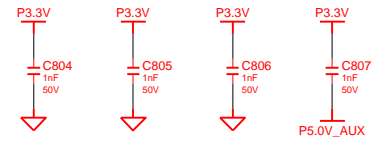


For EMC Review ADV1-16

Added on 21-Oct-08

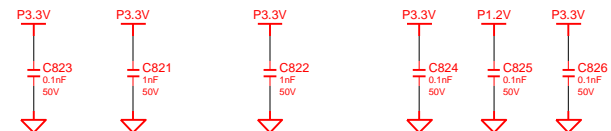


For EMC Review PV-2 For EMC Review PV-3 For EMC Review PV-4 For EMC Review PV-5



For EMC Review PV-9

Added on 15-Dec-08



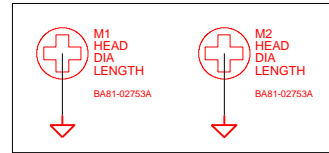
For EMC Review PR-5 For EMC Review PR-6 For EMC Review PR-8

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CHECK	HS LEE / BM LEE	DEV. STEP	MP<PR>			ELECTRONICS
APPROVAL	YB CHUN	REV	1.00		EMC	PART NO.
MODULE CODE	undefined	LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	45	BA41-01024-6A
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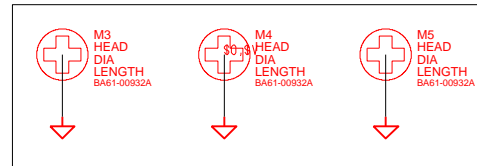
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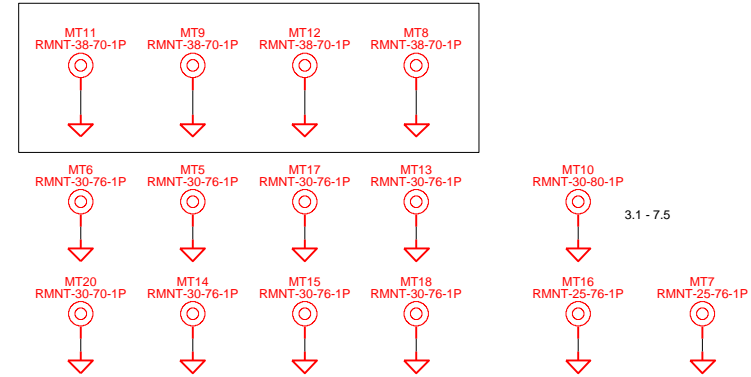
FAN-NUT



THERMAL-NUT

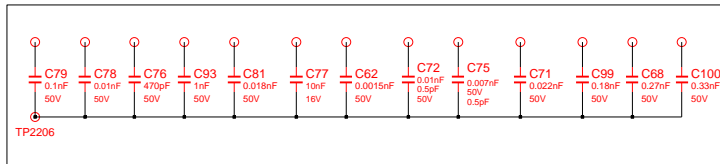


CPU RHE

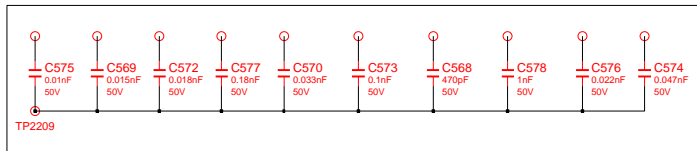


ICT Cap : need to change with last BOM

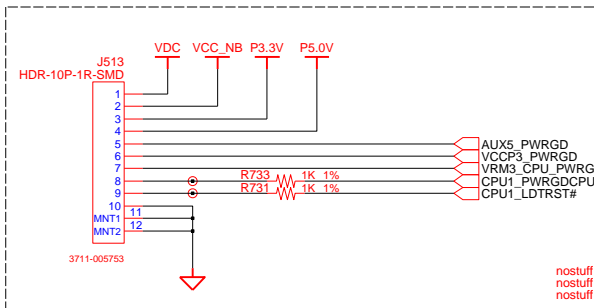
1 - 499 SIDE



500 - SIDE



ICT PORT



REV500
1
2 3

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP
1	N.C.			ADV1
2	1-2			PV
3	2-3		1.0	MP(PR)
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW	HS CHO	DATE	1/10/2008	TITLE	DRESDEN-INT	SAMSUNG
CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)			ELECTRONICS
APPROVAL	YB CHUN	REV	1.00		MTH/ICT	PART NO.
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○MCD3_SDWP
○MEM1_VREF
○PCI3_AD23
○PCI3_AD24
○PCI3_AD25
○PCI3_AD26
○PCI3_AD27
○PCI3_AD28
○PEX3_WAKE#
○PEX3_RST#
○AUD3_GPIO0#
○AUD3_GPIO1#
○BAT3_SMCLK#
○CHP3_A_RST#
○CHP3_GPIO16
○CHP3_GPIO17
○CHP3_SERIRQ
○CHP3_SLP5S#
○CHP3_SLP5S#
○CLK3_DBG LPC
○CLK3_PWRGD#
○CPU1_ALERT#
○CRT3_DDCCLK
○CRT5_DDCCLK
○CRT3_DDCDATA
○CRT5_DDCDATA
○EXP3_CPURST#
○EXP3_PERST#
○SMB3_DATA
○SPI3_CS0#
○SPI3_MISO
○SPI3_MOSI
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○MCD3_SDCMD
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○LPC3_LAD(2)
○LPC3_LAD(3)
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○CPU2_THERMDC

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○CHP3_NB_THERMDP
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○HDA3_MDC_SDO
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○KBC3_EXTSMI#

○KBC3_NUMLED#
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○KBC3_SMDATA#
○KBC3_SPKMUTE
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○CHP3_SB_TEST2
○CHP3_SUSSTAT#
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○PEG5_HDMI_CLK
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○AUD5_HP_O_RIGHT
○AUD5_MIC1_RIGHT
○AUD5_MIC2_RIGHT
○AUD5_HP_O_LEFT
○AUD5_MIC1_LEFT
○AUD5_MIC2_LEFT
○AUD5_MIC2_VREF
○CHP1_THRMTRIP#
○CHP3_BIOS_CRI#
○CHP3_INTRUDER#

○CPU1_PROCHOT#

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○HDA3_MDC_SYNC
○KBC3_CAPSLED#
○KBC3_NB_PWRGD#
○VRM3_CPU_PWRGD#
○CPU1_ALL_LDTSTP
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○KBC3_LED_POWER#
○KBC3_PWRON_INV#
○USB3_SUB_PWRON#
○CHP3_STRAP#
○KBC3_LED_CHARGE#
○KBC3_THERM_SMCLK
○LAN3_LINK10_100#
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○CPU1_VDDIO_FB#
○CPU1_VDDNB_FB#
○CPU3_THRMTRIP#
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○PEG5_HDMI_SUB_CLK
○PEG3_HDMI_SUB_DATA

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○KBC3_VRON
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○SPK5_L-
○SPK5_R+
○SPK5_R-
○FAN5_VDD

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○T_R_BUTTON#
○KBC3_BKLTON
○KBC3_RST#
○KBC5_TCLK
○KBC5_TDATA
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○P1.8V_P2.5V_LAN
○VDC-
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○VDC_ADPT
○VDD_CPU_NB
○P1.1V
○P3.3V_MCD
○P5.0V_ALW
○P5.0V_AMP
○P5.0V_AUD
○P5.0V_AUX
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○G_AUD
○G_CHG
○G_CPU
○G_DDR
○G_MIC

○G_P1.2V
○G_P3.3V
○LCD_VDD3V
○P0.9V
○P1.2V
○P1.5V
○P1.8V
○P2.5V
○P5.0V_SUB
○P12.0V_ALW
○P3.3V_HDMI
○P4.75V_AUD
○P5.0V_FILTER
○P3.3V_MICOM
○P3.3V
○PRTC_BAT
○P1.2V_AUX
○P1.2V_LAN
○P1.5V_EXP
○P1.8V_AUX
○P3.3V_AUX
○P3.3V_EXP
○VCC_NB
○P5.0V
○VCC_CRT

DRAW	HS CHO	DATE	1/10/2008	TITLE	DRESDEN-INT	SAMSUNG
CHECK	HS LEE / BM LEE	DEV. STEP	MP (PR)			ELECTRONICS
APPROVAL	YB CHUN	REV	1.00	TP		PART NO.
MODULE CODE	undefined	LAST EDIT	December 24, 2008 14:36:53 PM	PAGE	47	OF 49

The schematic illustrates the electrical design of a USB board. Key components and sections include:

- Power Regulation:** Features two TPS2062 ICs (U501, U502) for USB power management, each with associated capacitors (C503-C507, C511) and diodes (PGB1010603NR).
- USB Ports:** Shows two USB ports (J501, J503) with their respective pin connections and associated components like BSS84 MOSFETs and resistors (R508, R510).
- Discharge Circuit:** Includes a MOSFET (Q2, RHU002N06) and resistors (R1, R2) for USB discharge control, triggered by USB3_SUB_PWRON#.
- Connectors and Switches:** Details various connectors (J1, J501, J503) and a switch (SW1) for power control.
- Passive Components:** Numerous capacitors (C501-C507, C511) and resistors (R508, R510) are specified with their values and tolerances.

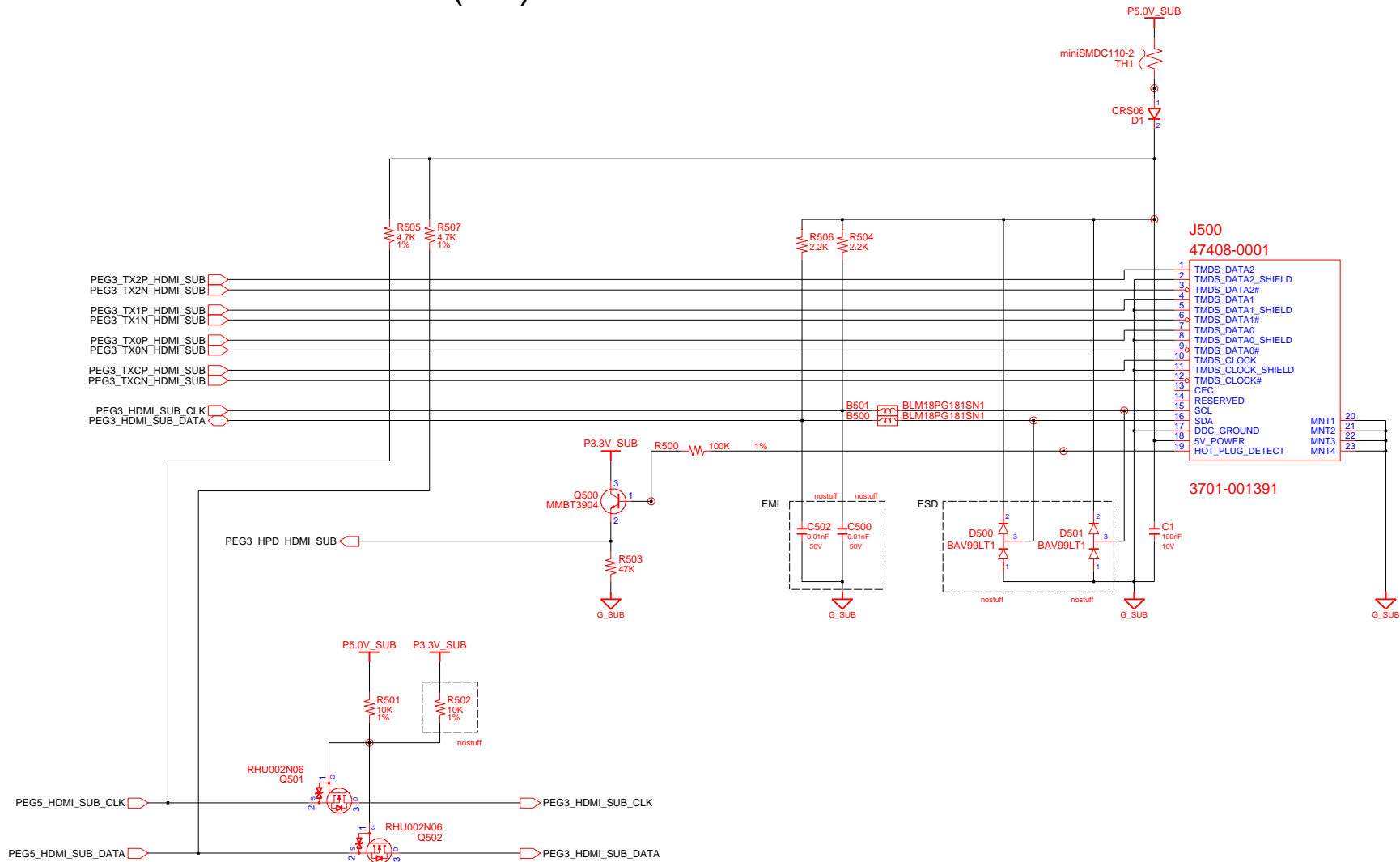
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CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)			
APPROVAL	YB CHUN	REV	1.00			
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Sub Board (2/2)



Note: These FETs should be placed near HDMI Connector

DRAW	HS CHO	DATE	11/26/2007	TITLE	DRESDEN-INT SUB SUB BOARD (2/2)	SAMSUNG ELECTRONICS
CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)			PART NO. BA41-01024-6A
APPROVAL	YB CHUN	REV	1.00			
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