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FIRENZE

CPU : Dothan533
 Chip Set : ALVISO & ICH6-M
 Remarks : EXTERNAL GFX

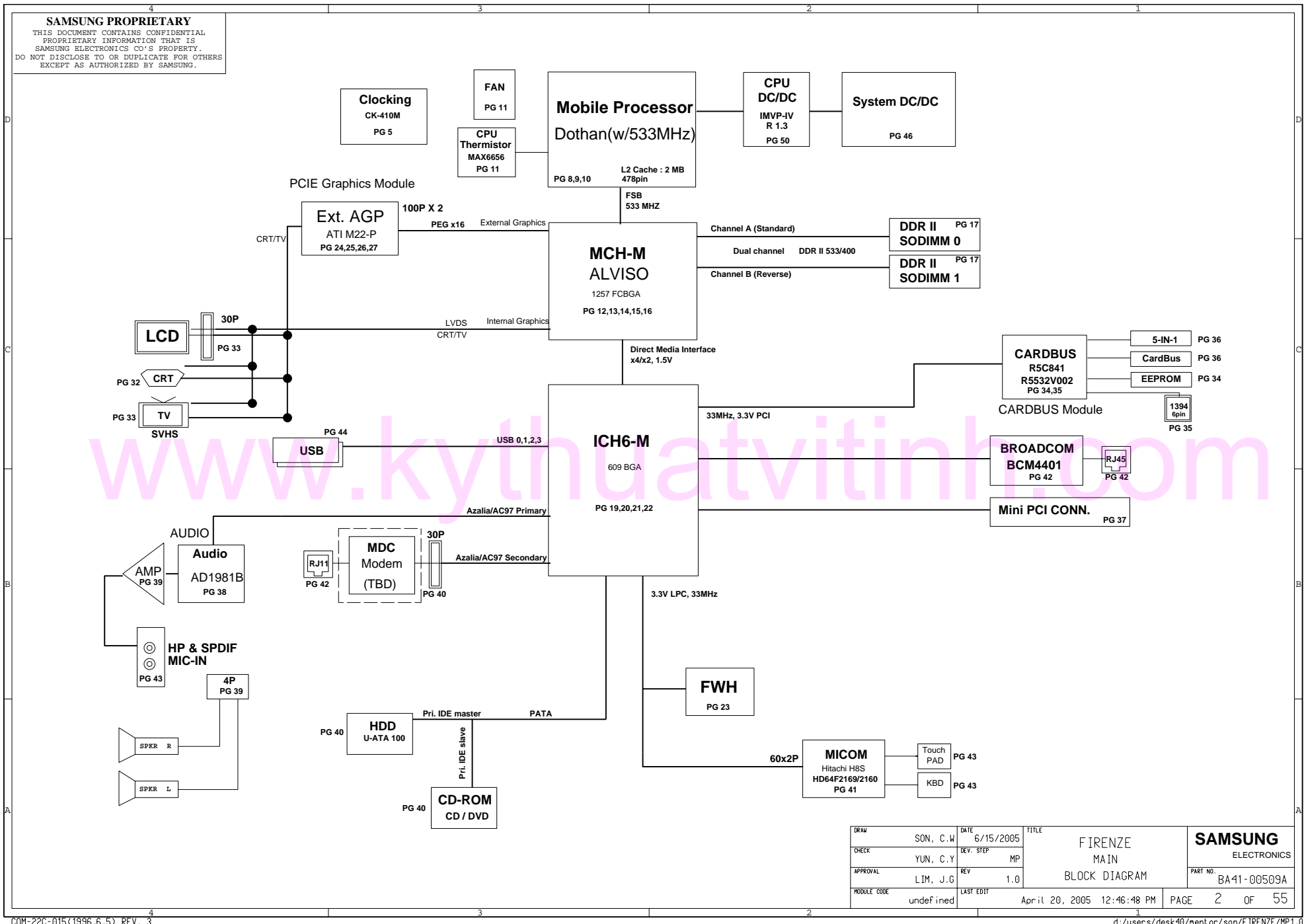
Model Name : FIRENZE
 PBA Name : MAIN
 PCB Code : BA41-00509A
 Dev. Step : MP
 Revision : 1.0
 T.R. Date : 2005.06.07

DRAW	CHECK	APPROVAL
SON, C.W	YUN, C.Y	LIM, J.G

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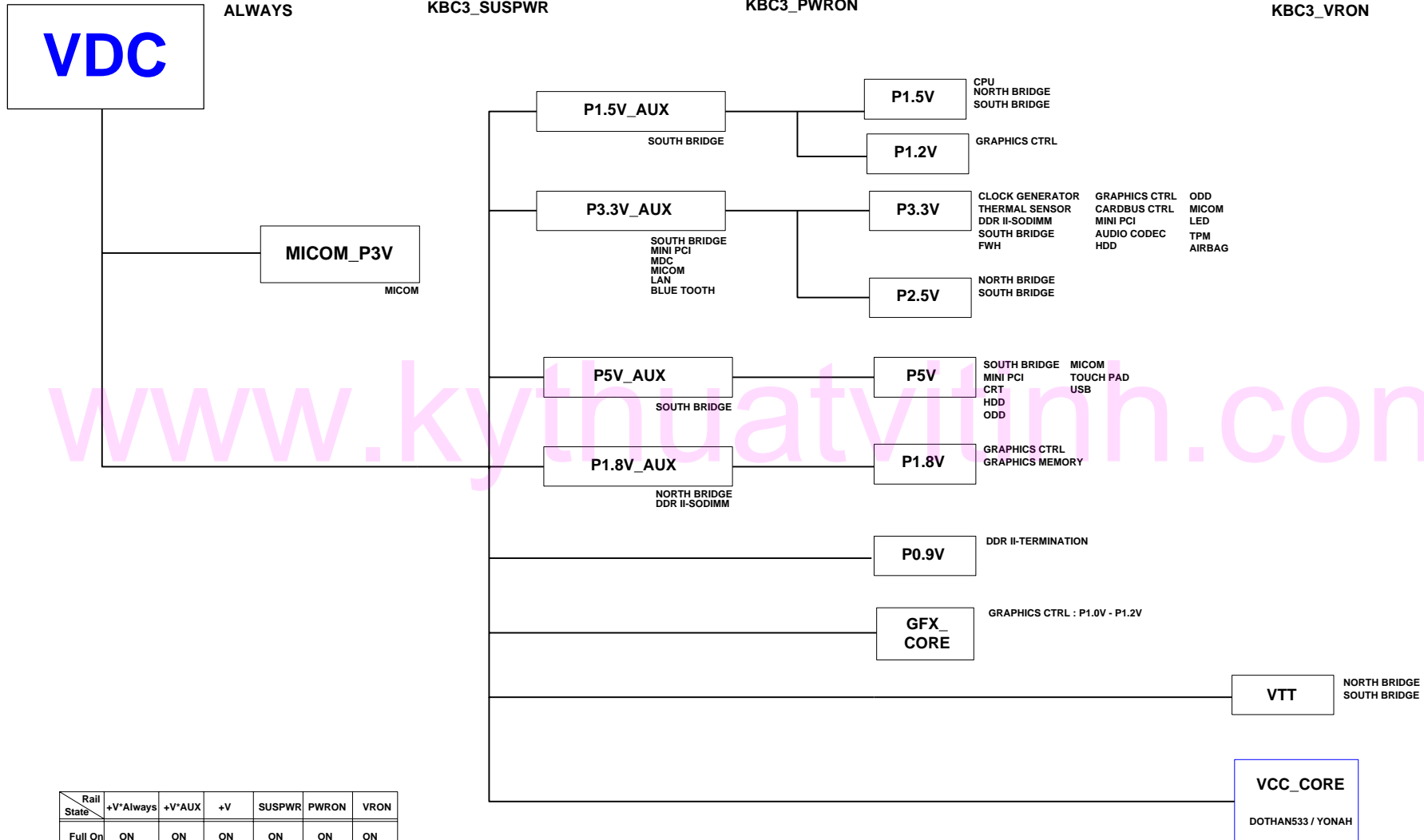
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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0		BOARD INFORMATION	PART NO. BA41-00509A
MODULE CODE	undefined	LAST EDIT	June 15, 2005 4:12:30 PM	PAGE	1	OF 55



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Power Diagram



Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF	OFF
S4	ON	OFF	OFF	OFF	OFF	OFF
S5	ON	OFF	OFF	OFF	OFF	OFF

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APPROVAL	LIM, J.G	REV	1.0			
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION**PCI Devices**

DEVICES	IDSEL#	REQ/GNT#	INTERRUPTS
CARDBUS CONTROLLER	AD25	0	A,B,C
MINIPCI	AD23	1	E,F
LAN CONTROLLER	AD21	2	G

Voltage Rails

VDC	Primary DC system power supply (9 to 20V)
VCC_CORE	Core voltage for DOTHAN (0.7~1.708V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V)
GFX_CORE	MCH-M Core Voltage (off in S3-S5) ATI M24-P Core Voltage (1.0~1.2V) (off in S3-S5)
P0.9V	0.9V power rail (off in S3-S5)
P1.2V	1.2V power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)

CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V
0	0	0	0	1	1	1.660 V	1	0	0	0	1	1	1.148 V
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V
0	0	0	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V
0	0	1	1	0	1	1.500 V	1	0	1	1	0	1	0.988 V
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V
0	1	0	1	1	0	1.356 V	1	1	0	1	1	0	0.844 V
0	1	0	1	1	1	1.340 V	1	1	0	1	1	1	0.828 V
0	1	1	0	0	0	1.324 V	1	1	1	0	0	0	0.812 V
0	1	1	0	0	1	1.308 V	1	1	1	0	0	1	0.796 V
0	1	1	0	1	0	1.292 V	1	1	1	0	1	0	0.780 V
0	1	1	0	1	1	1.276 V	1	1	1	0	1	1	0.764 V
0	1	1	1	0	0	1.260 V	1	1	1	1	0	0	0.748 V
0	1	1	1	0	1	1.244 V	1	1	1	1	0	1	0.732 V
0	1	1	1	1	0	1.228 V	1	1	1	1	1	0	0.716 V
0	1	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V

IC / SMB Address

Devices	Address	Hex	Bus
SOUTH BRIDGE	Master	-	SMBUS Master
ADM1032(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
1,3	SYSTEM PORT A
0,2	SYSTEM PORT B

System Power States

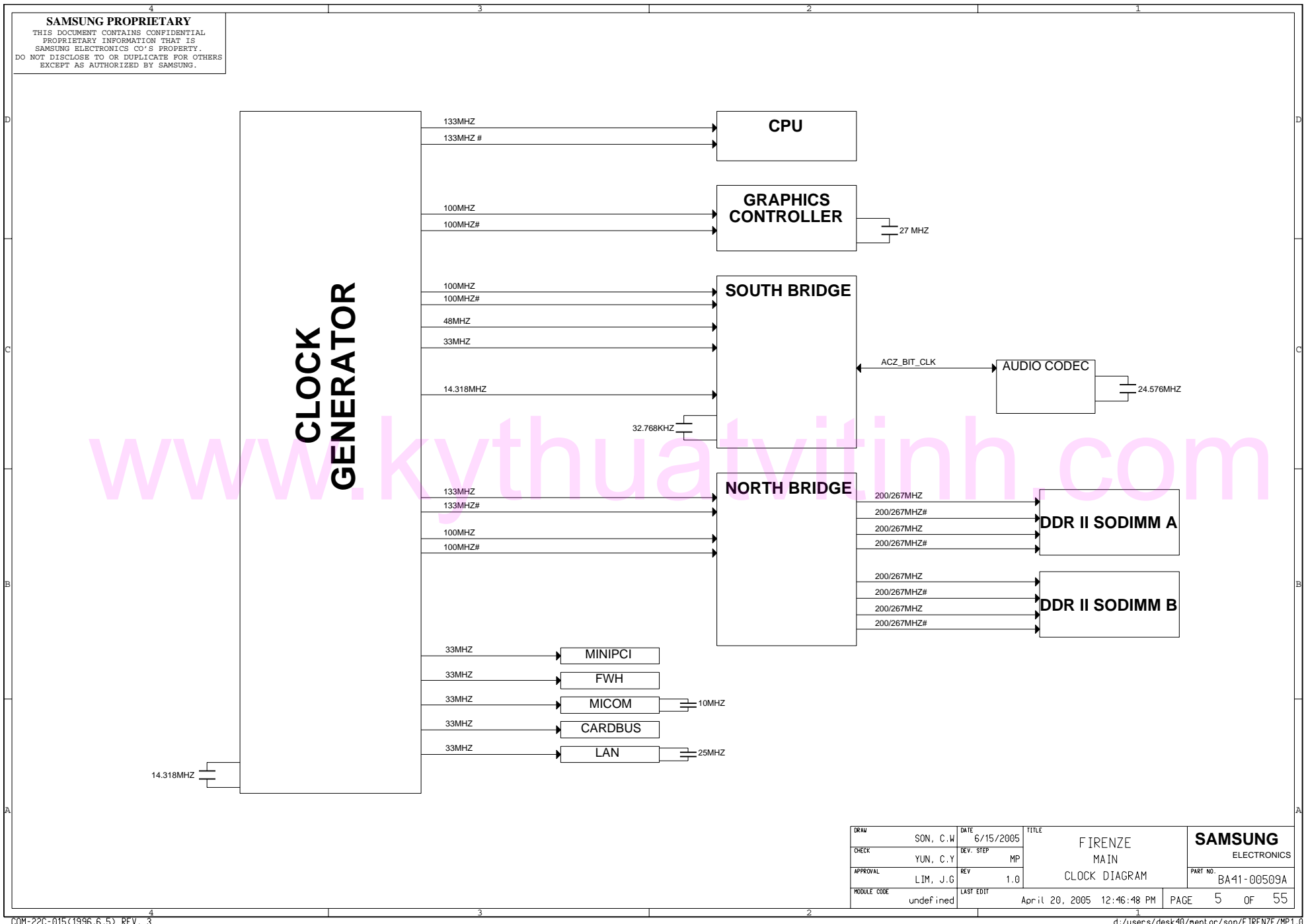
- CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.
- CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3_SLPS4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.
- CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

REVISION HISTORY

See rev notes in the changes file for more information.

MiniPCI SLOT1

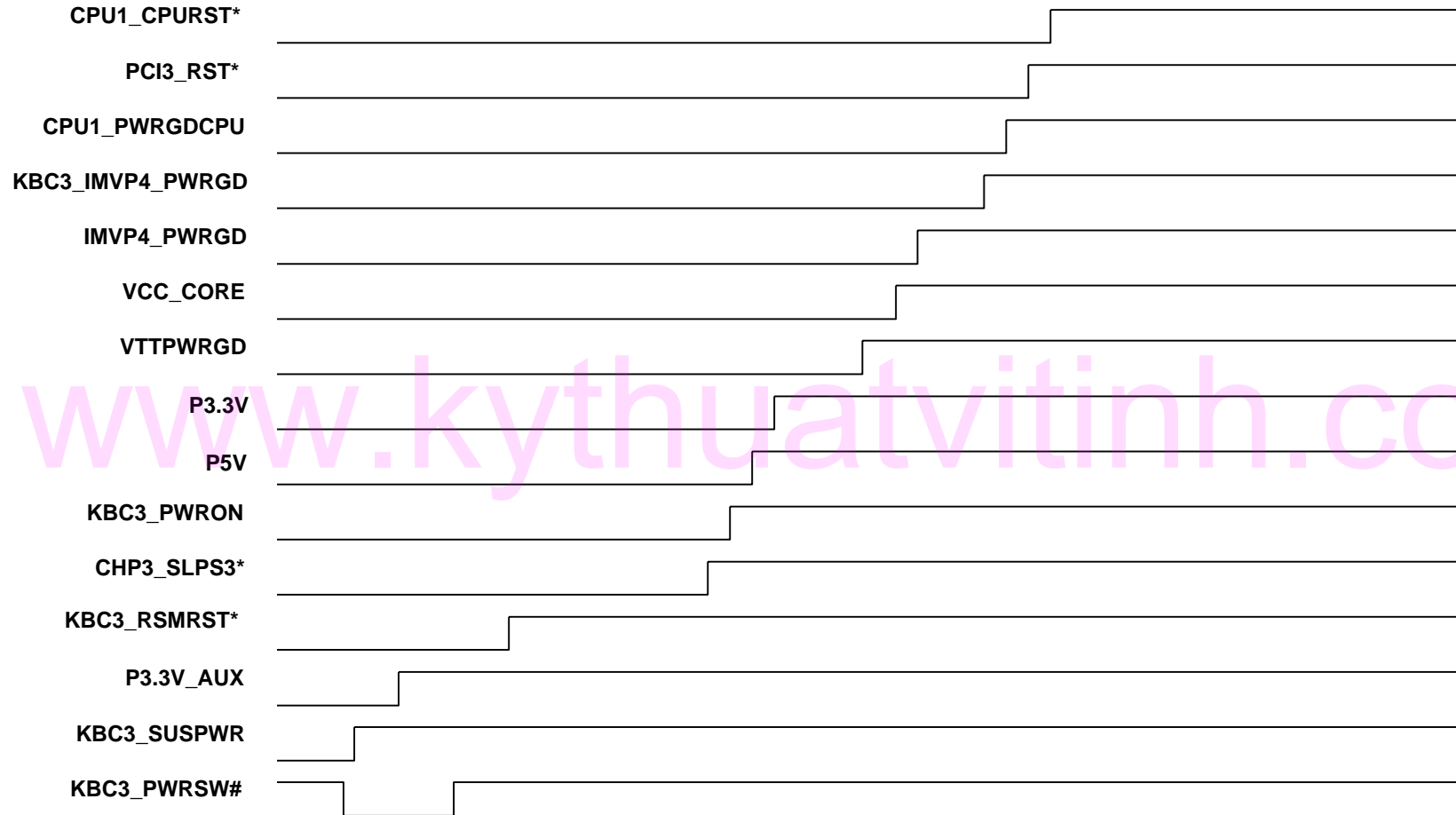
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APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	4	OF 55



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RESET DIAGRAM

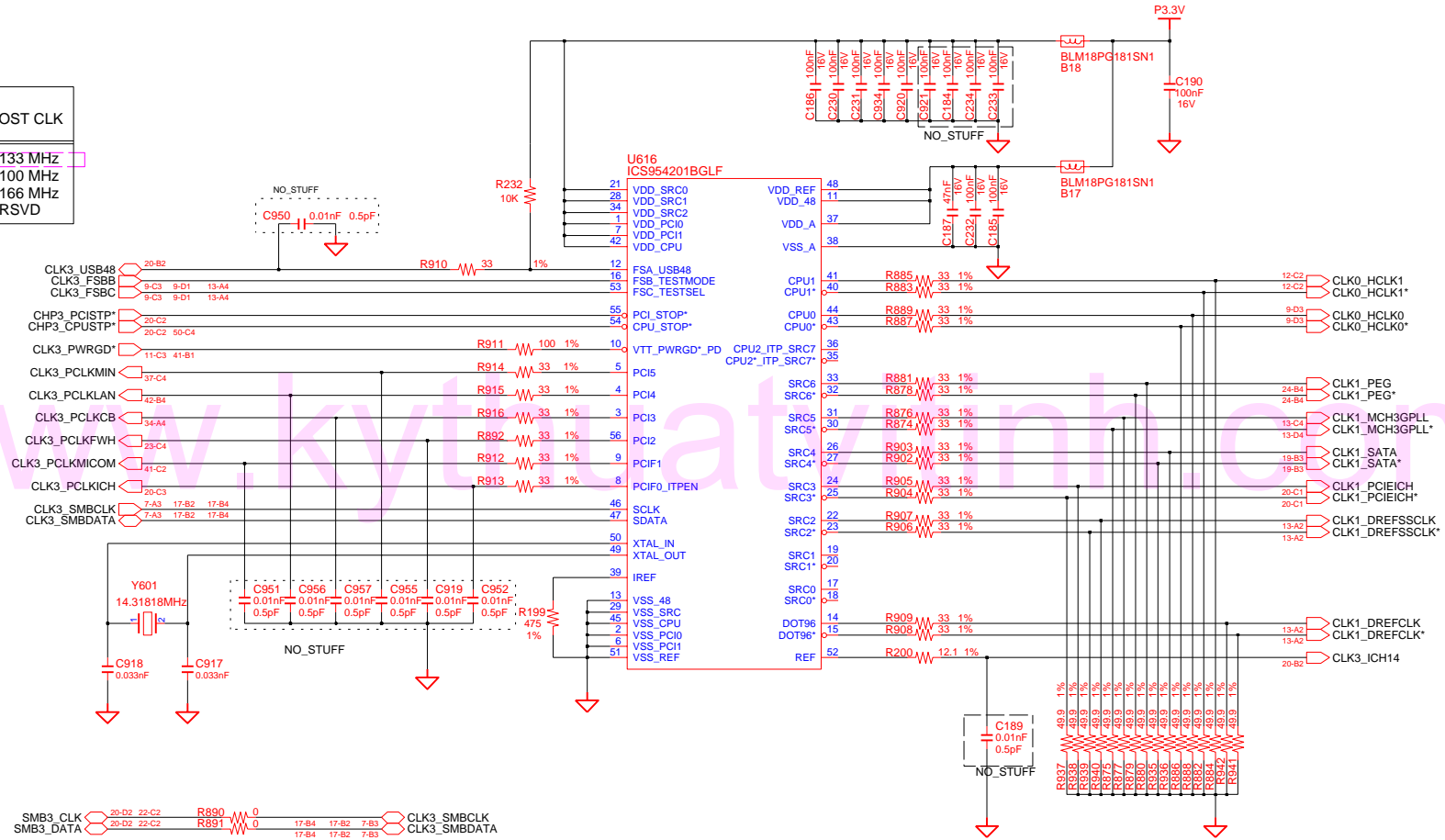


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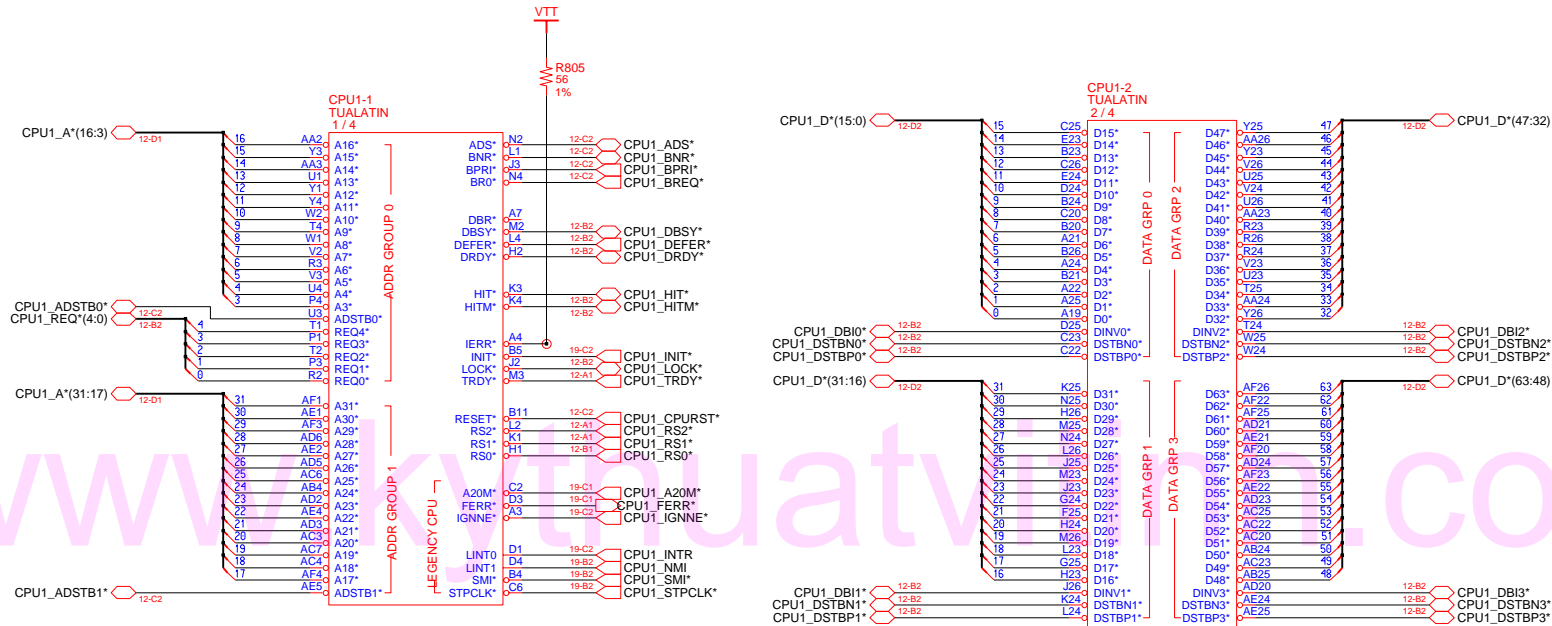
FSA	FSB	FSC	HOST CLK
BSEL2	BSEL1	BSEL0	
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS
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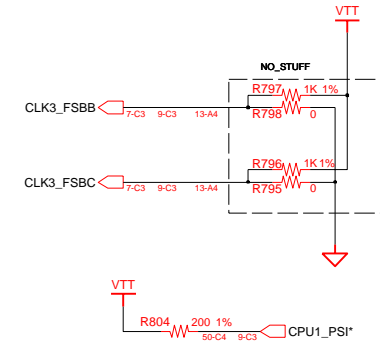
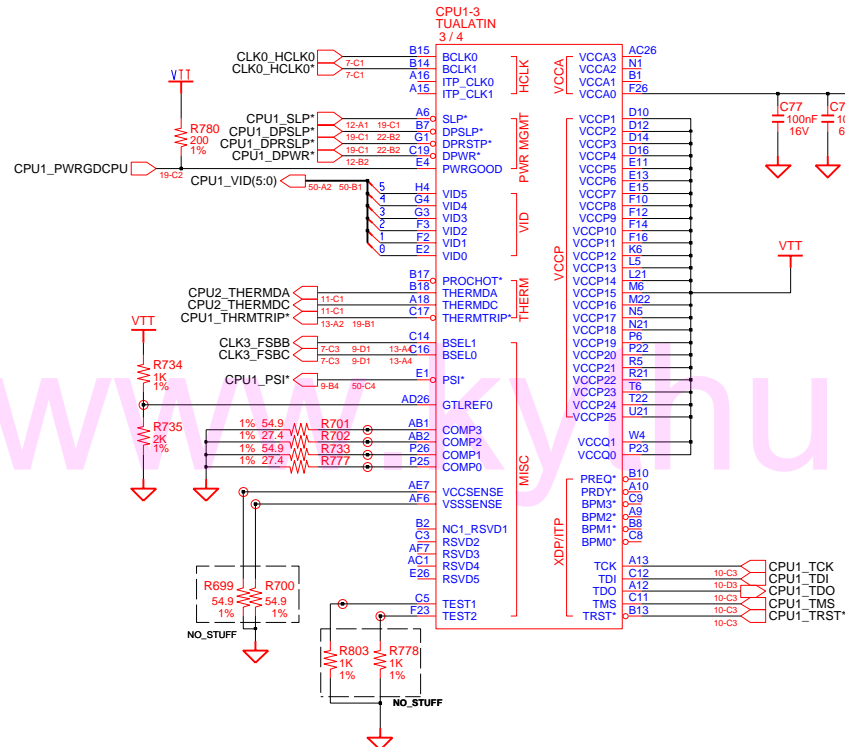
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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN CPU(1/3)	SAMSUNG ELECTRONICS
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CPU Core Voltage Table

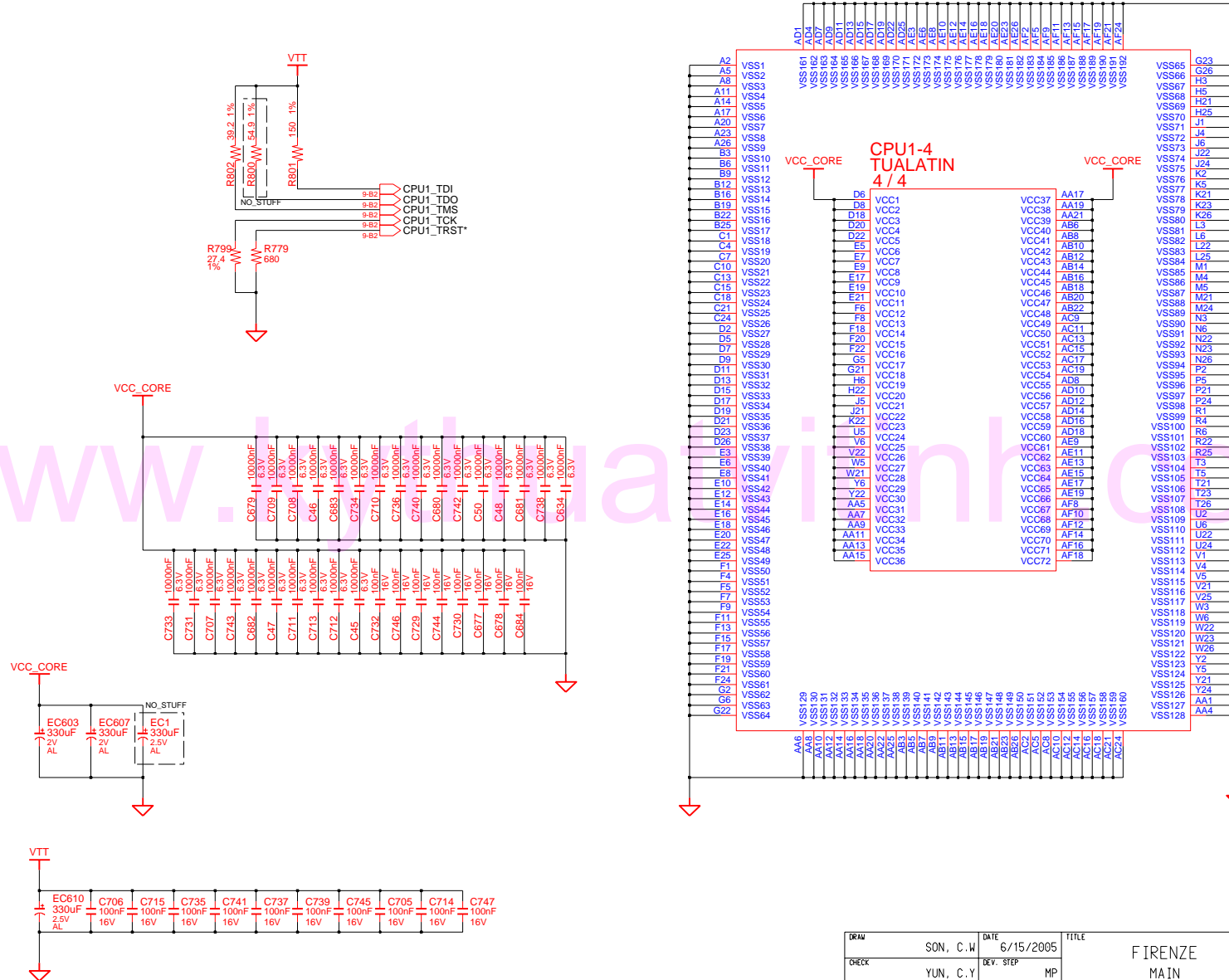
VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0 0	1.708 V	1 0 0 0 0 0	1.196 V
0 0 0 0 0 1	1.692 V	1 0 0 0 0 1	1.180 V
0 0 0 0 1 0	1.676 V	1 0 0 0 1 0	1.164 V
0 0 0 0 1 1	1.660 V	1 0 0 0 1 1	1.148 V
0 0 0 1 0 0	1.644 V	1 0 0 1 0 0	1.132 V
0 0 0 1 0 1	1.628 V	1 0 0 1 0 1	1.116 V
0 0 0 1 1 0	1.612 V	1 0 0 1 1 0	1.100 V
0 0 0 1 1 1	1.596 V	1 0 0 1 1 1	1.084 V
0 0 1 0 0 0	1.580 V	1 0 1 0 0 0	1.068 V
0 0 1 0 0 1	1.564 V	1 0 1 0 0 1	1.052 V
0 0 1 0 1 0	1.548 V	1 0 1 0 1 0	1.036 V
0 0 1 0 1 1	1.532 V	1 0 1 0 1 1	1.020 V
0 0 1 1 0 0	1.516 V	1 0 1 1 0 0	1.004 V
0 0 1 1 0 1	1.500 V	1 0 1 1 0 1	0.988 V
0 0 1 1 1 0	1.484 V	1 0 1 1 1 0	0.972 V
0 0 1 1 1 1	1.468 V	1 0 1 1 1 1	0.956 V
0 1 0 0 0 0	1.452 V	1 1 0 0 0 0	0.940 V
0 1 0 0 0 1	1.436 V	1 1 0 0 0 1	0.924 V
0 1 0 0 1 0	1.420 V	1 1 0 0 1 0	0.908 V
0 1 0 0 1 1	1.404 V	1 1 0 0 1 1	0.892 V
0 1 0 1 0 0	1.388 V	1 1 0 1 0 0	0.876 V
0 1 0 1 0 1	1.372 V	1 1 0 1 0 1	0.860 V
0 1 0 1 1 0	1.356 V	1 1 0 1 1 0	0.844 V
0 1 0 1 1 1	1.340 V	1 1 0 1 1 1	0.828 V
0 1 1 0 0 0	1.324 V	1 1 1 0 0 0	0.812 V
0 1 1 0 0 1	1.308 V	1 1 1 0 0 1	0.796 V
0 1 1 0 1 0	1.292 V	1 1 1 0 1 0	0.780 V
0 1 1 0 1 1	1.276 V	1 1 1 0 1 1	0.764 V
0 1 1 1 0 0	1.260 V	1 1 1 1 0 0	0.748 V
0 1 1 1 0 1	1.244 V	1 1 1 1 0 1	0.732 V
0 1 1 1 1 0	1.228 V	1 1 1 1 1 0	0.716 V
0 1 1 1 1 1	1.212 V	1 1 1 1 1 1	0.700 V

Highest Freq. of Dothan400(1.8GHz)
* Highest Freq. of Dothan533(?? GHz : TBD)

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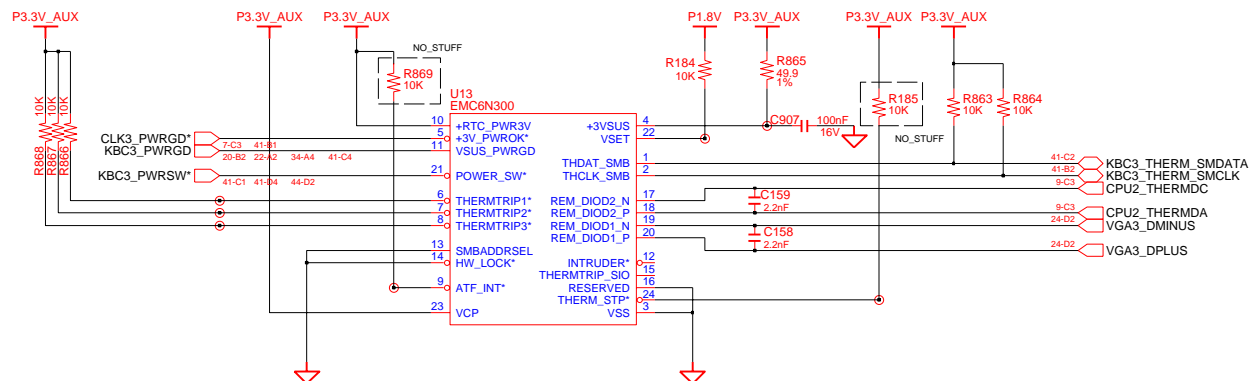
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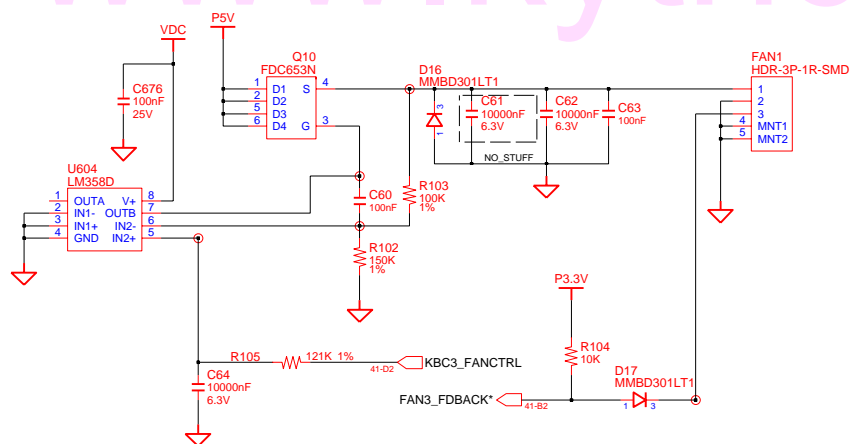


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APPROVAL	LIM, J. G	REV	1.0	CPU(3/3)		
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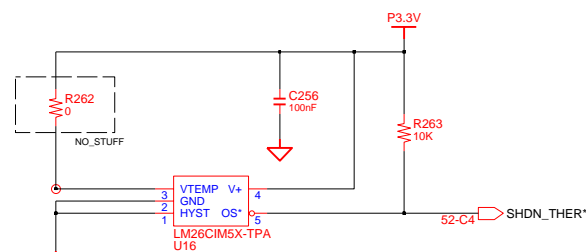
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FAN CONTROL



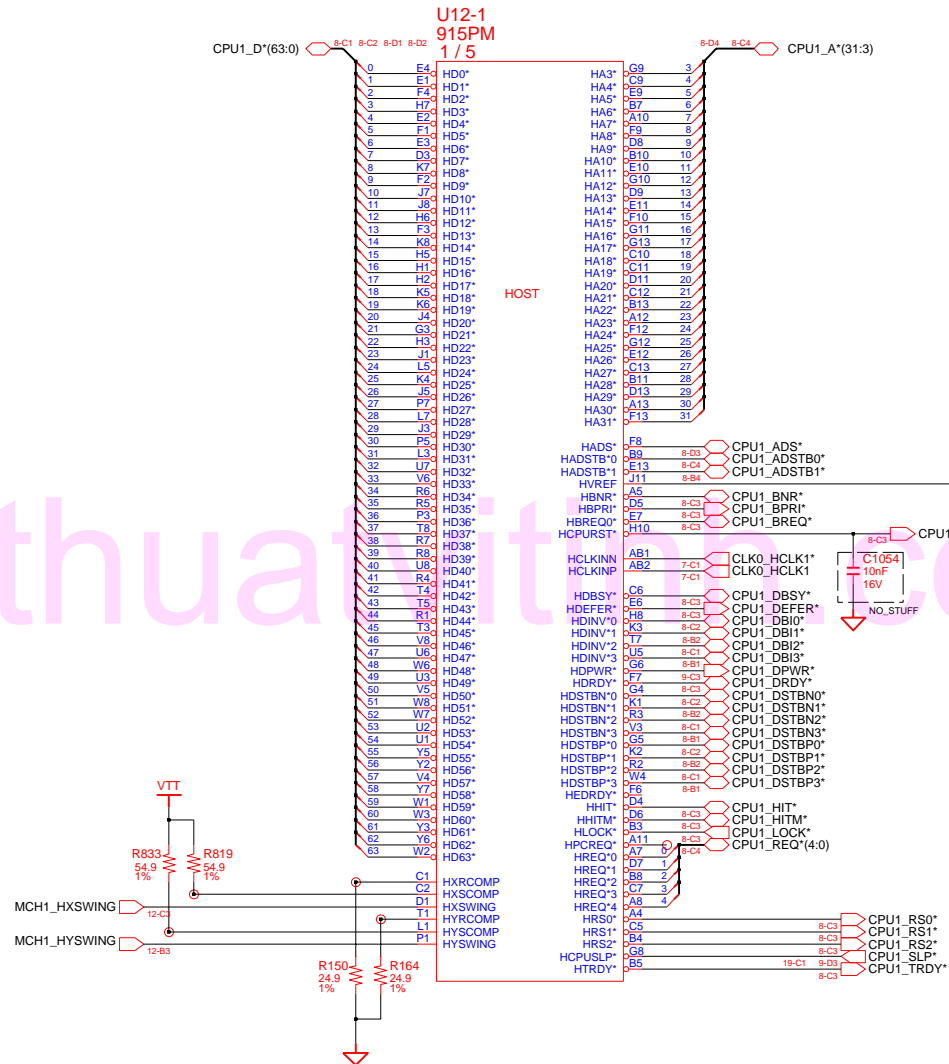
OPT CIRCUIT



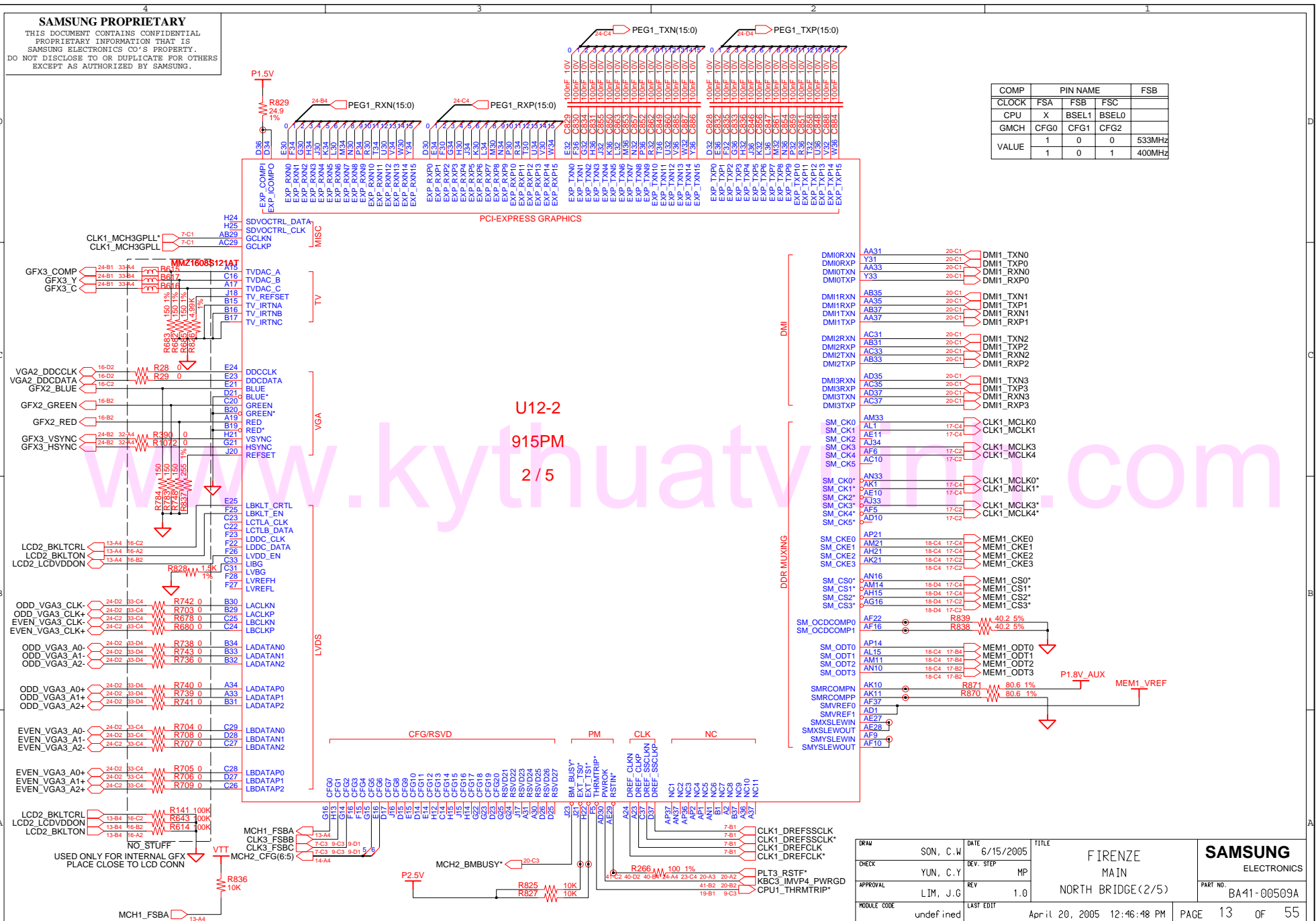
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CHECK	YUN, C.Y.	DEV. STEP	MP		
APPROVAL	LIM, J.G.	REV	1.0		
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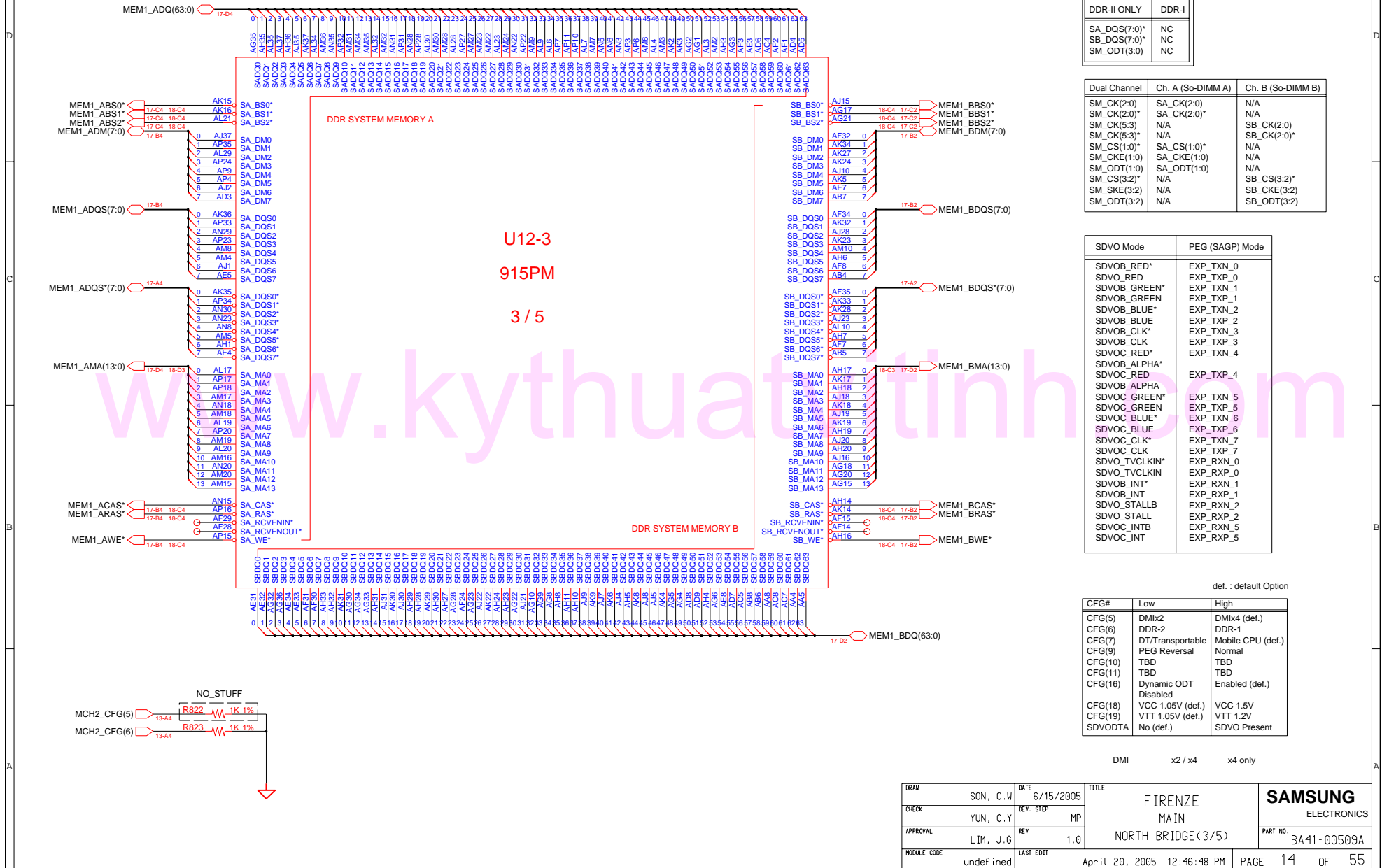


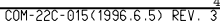
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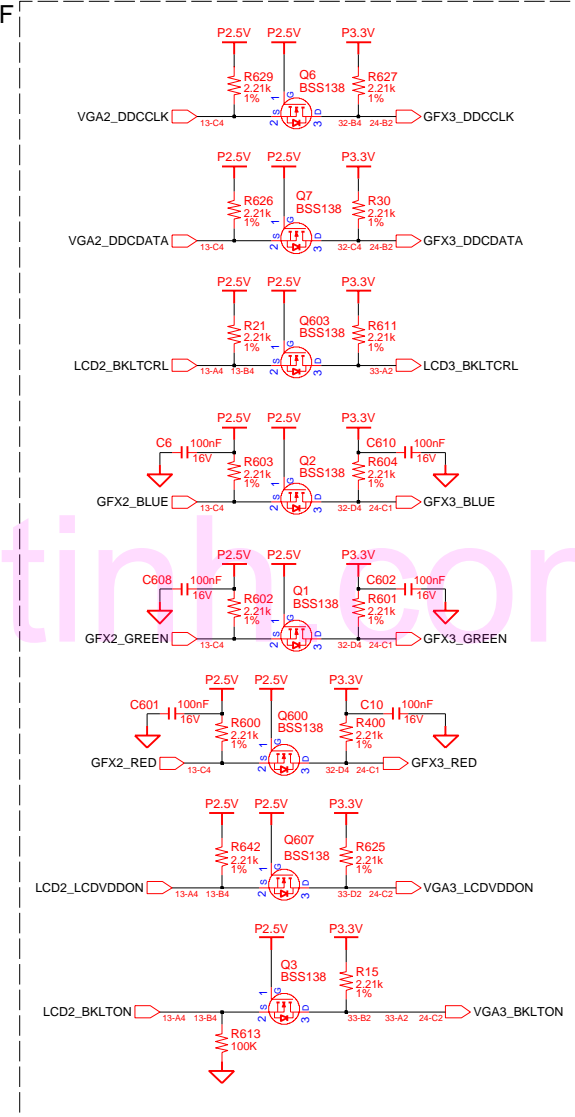
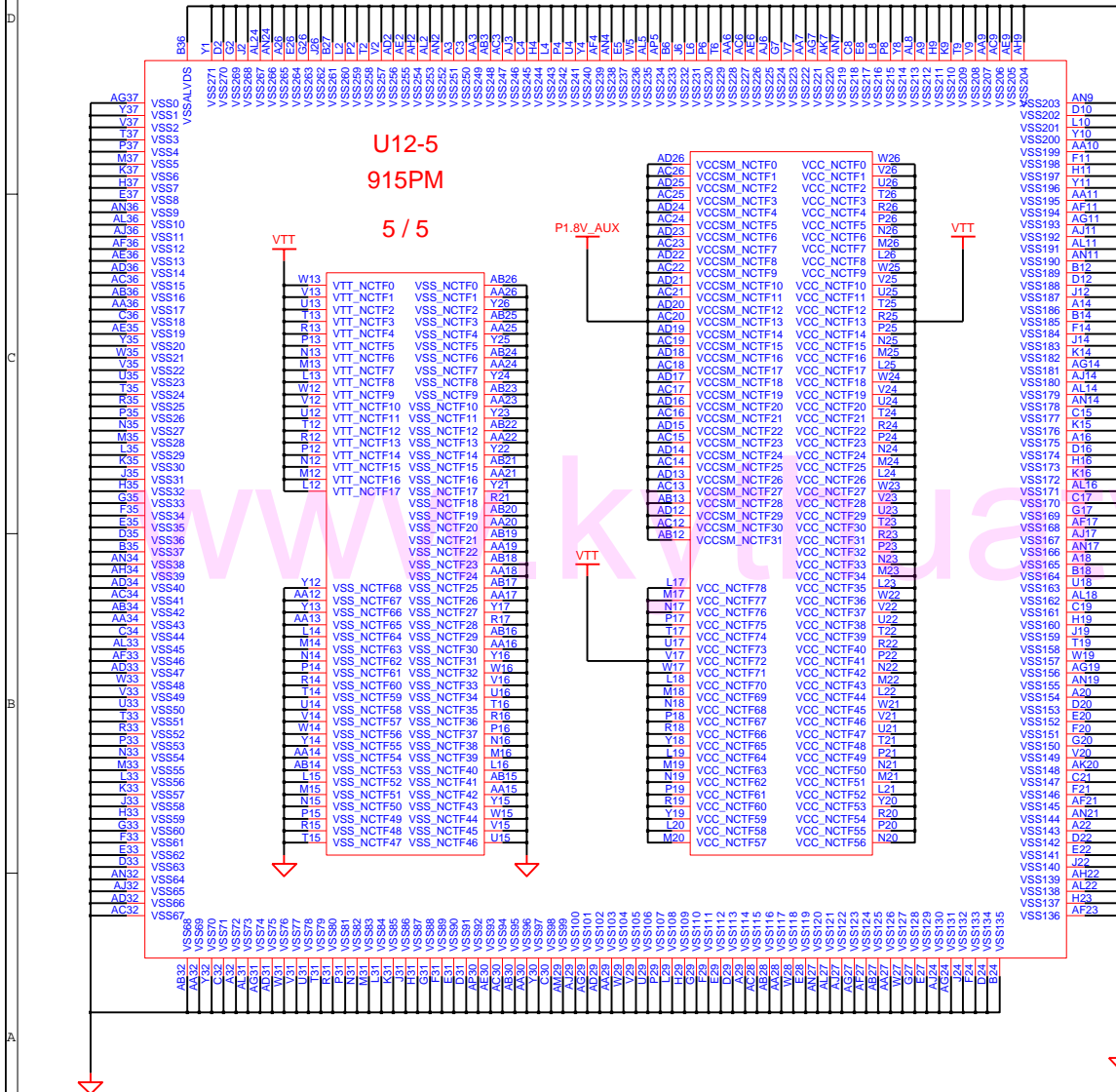


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LVDS Voltage Translation Logic (2.5V -> 3.3V) INTERNAL GFX ONLY

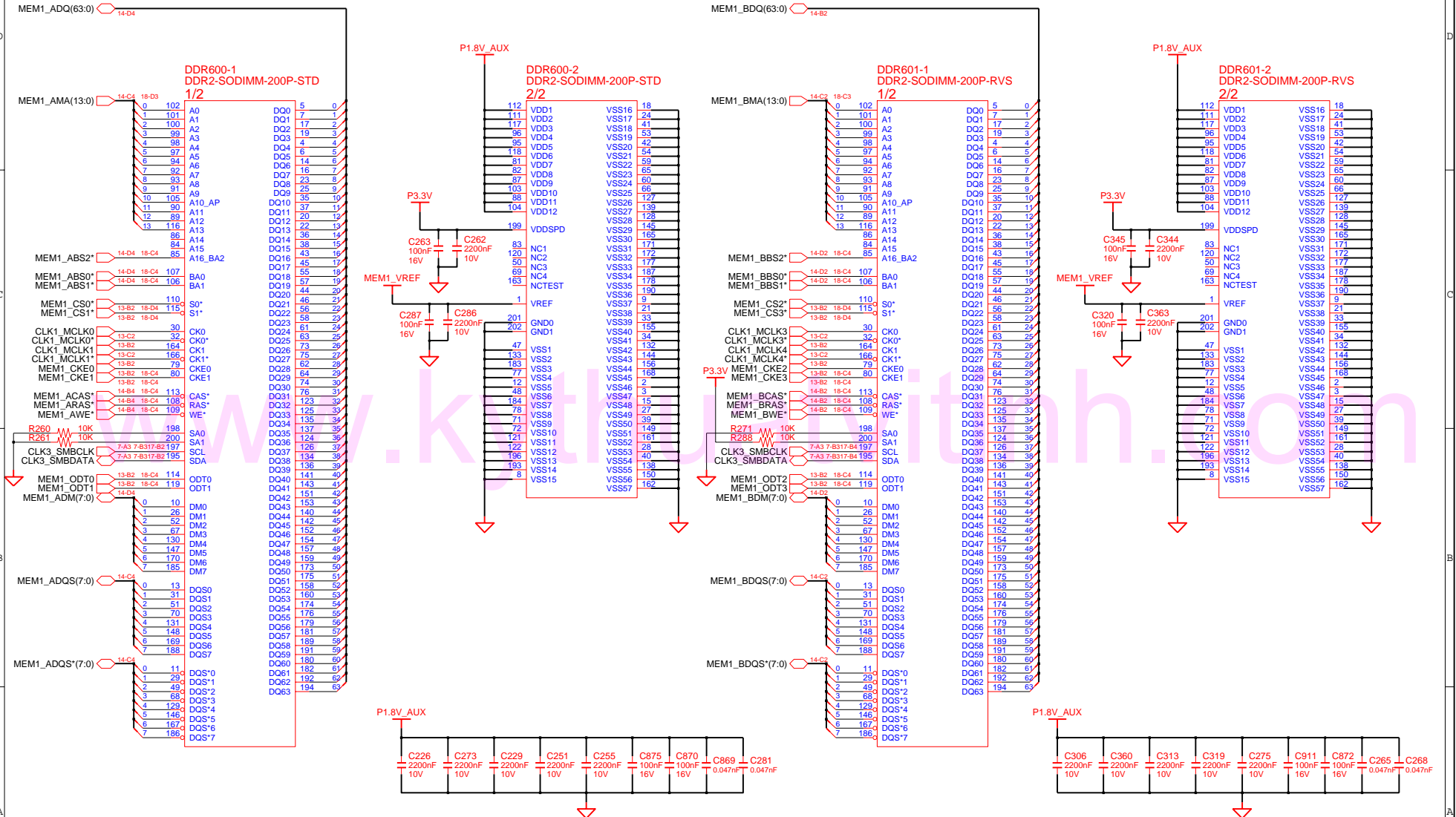
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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP		MAIN	
APPROVAL	LIM, J.G	REV	1.0		NORTH BRIDGE(5/5)	PART NO. BA41-00509A
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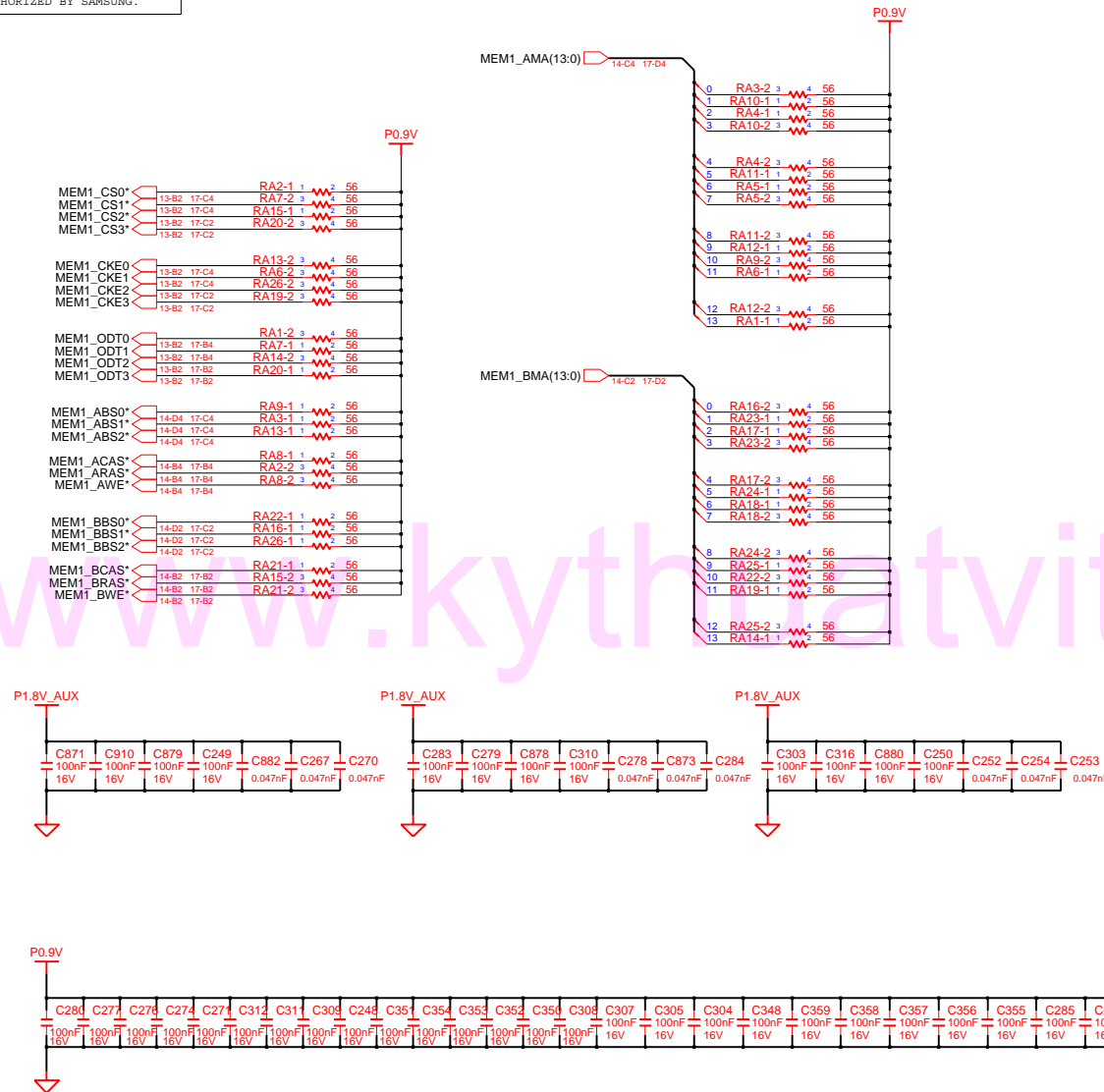
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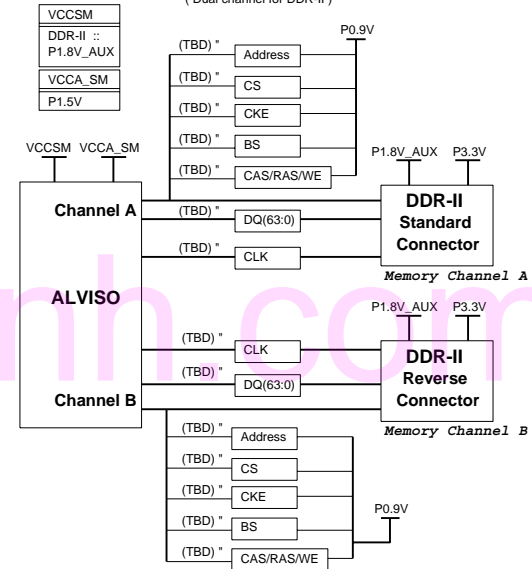
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APPROVAL	LIM, J.G	REV	1.0	DDR2-SODIMM		
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	17 OF 55	

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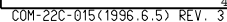


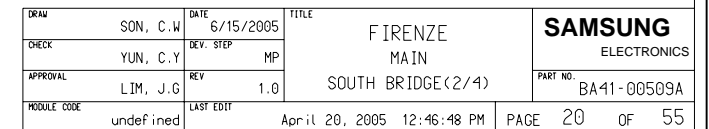
Memory Topology

(Dual channel for DDR-II)



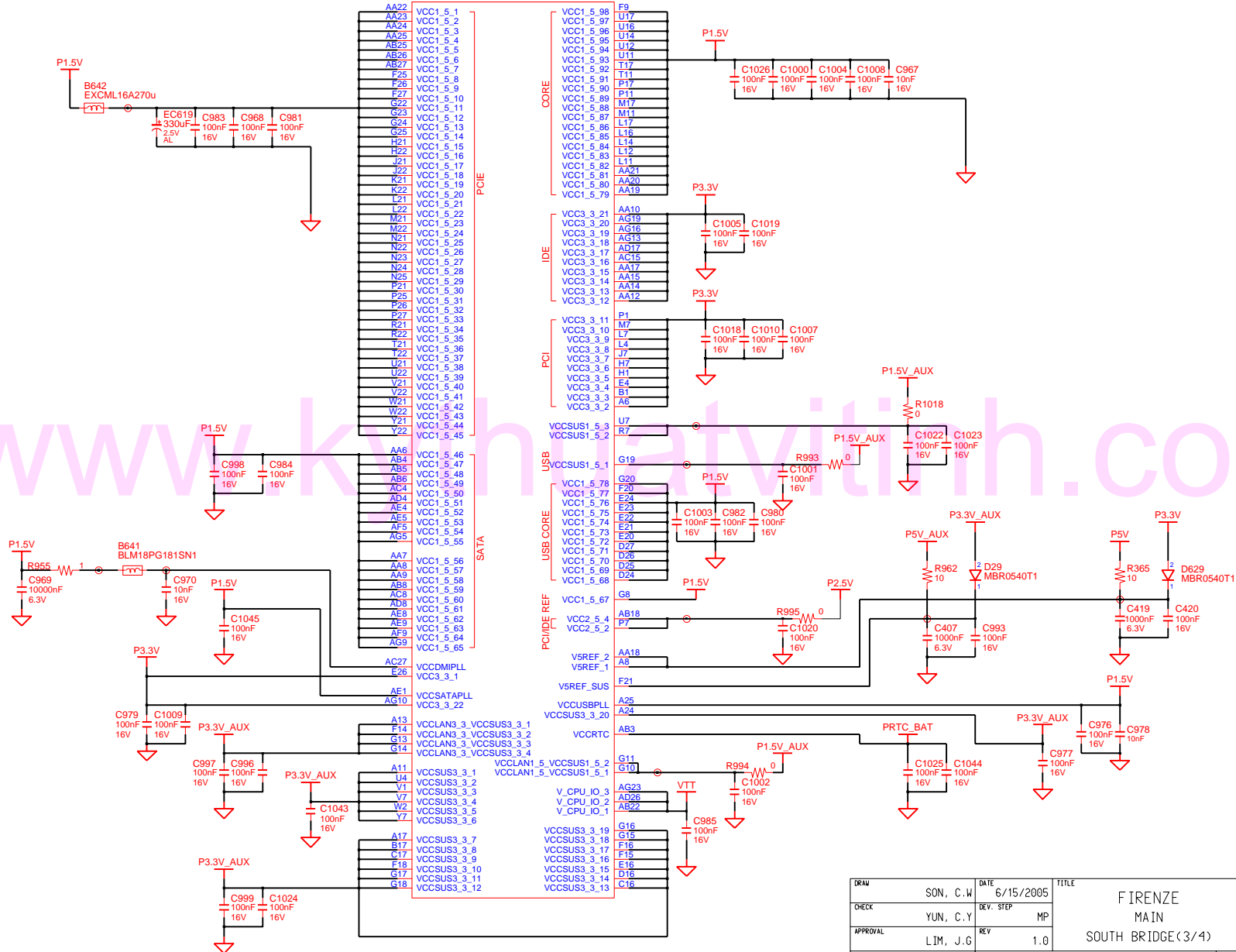
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CHECK	YUN, C.Y	DEV. STEP	MP			PART NO. BA41-00509A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	18	OF 55





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U23-4
82801FBM
4/5



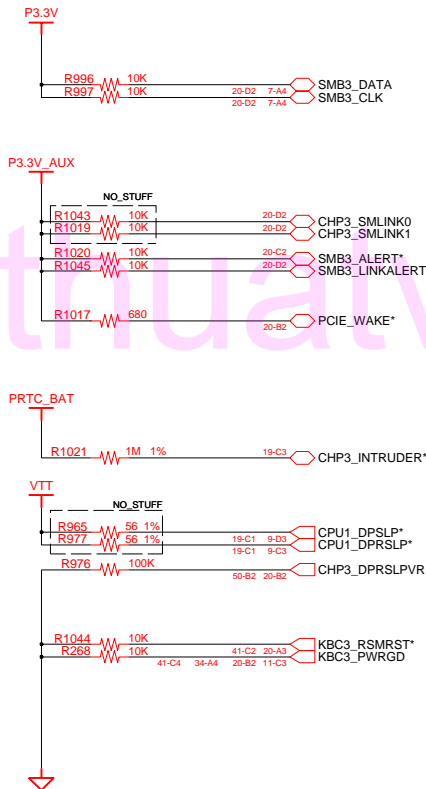
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CHECK	YUN, C.Y	DEV. STEP	MP	MAIN	BA41-00509A	
APPROVAL	LIM, J.G	REV	1.0	SOUTH BRIDGE(3/4)	PAGE	21 OF 55
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM			

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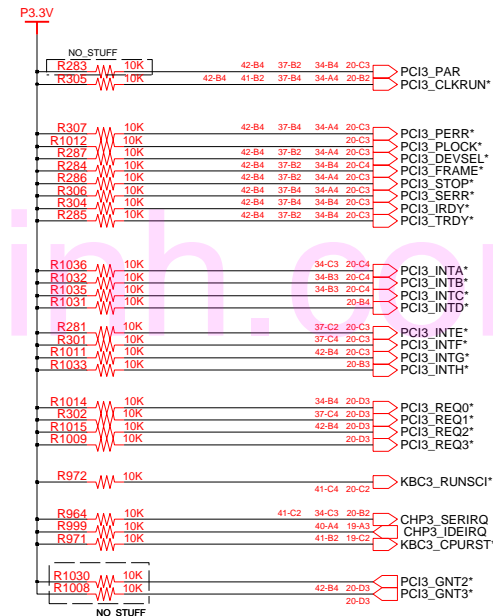
U23-5
82801FBM
5 / 5

AG22	VSS_172	VSS_86	P22
AG20	VSS_171	VSS_85	P16
AG17	VSS_170	VSS_84	P15
AG14	VSS_169	VSS_83	P14
AG12	VSS_168	VSS_82	P13
AG7	VSS_167	VSS_81	P12
AG3	VSS_166	VSS_80	N17
AG1	VSS_165	VSS_79	N16
AF26	VSS_164	VSS_78	N15
AF12	VSS_163	VSS_77	N14
AF10	VSS_162	VSS_76	N13
AF7	VSS_161	VSS_75	N12
AF3	VSS_160	VSS_74	N11
AF1	VSS_159	VSS_73	N7
AE25	VSS_158	VSS_72	N1
AE21	VSS_157	VSS_71	M27
AE12	VSS_156	VSS_70	M26
AE11	VSS_155	VSS_69	M23
AE10	VSS_154	VSS_68	M18
AE7	VSS_153	VSS_67	M16
AE6	VSS_152	VSS_66	M15
AE2	VSS_151	VSS_65	M14
AD24	VSS_150	VSS_64	M13
AD18	VSS_149	VSS_63	M12
AD15	VSS_148	VSS_62	L25
AD10	VSS_147	VSS_61	L24
AD6	VSS_146	VSS_60	L23
AD2	VSS_145	VSS_59	L13
AD1	VSS_144	VSS_58	K27
AC26	VSS_143	VSS_57	K26
AC24	VSS_142	VSS_56	K23
AC23	VSS_141	VSS_55	K22
AC22	VSS_140	VSS_54	K1
AC12	VSS_139	VSS_53	J25
AC10	VSS_138	VSS_52	J24
AC6	VSS_137	VSS_51	J23
AC3	VSS_136	VSS_50	J22
AB19	VSS_135	VSS_49	H27
AB10	VSS_134	VSS_48	H26
AB9	VSS_133	VSS_47	H23
AB7	VSS_132	VSS_46	G27
AB2	VSS_131	VSS_45	G12
AB1	VSS_130	VSS_44	G9
AA16	VSS_129	VSS_43	G7
AA13	VSS_128	VSS_42	G1
AA11	VSS_127	VSS_41	F22
AA4	VSS_126	VSS_40	F19
Y27	VSS_125	VSS_39	F17
Y26	VSS_124	VSS_38	E27
Y23	VSS_123	VSS_37	E27
Y6	VSS_122	VSS_36	E25
W25	VSS_121	VSS_35	E19
W24	VSS_120	VSS_34	E18
W23	VSS_119	VSS_33	E15
W7	VSS_118	VSS_32	E14
W1	VSS_117	VSS_31	D22
V27	VSS_116	VSS_30	D20
V26	VSS_115	VSS_29	D18
V23	VSS_114	VSS_28	D14
V4	VSS_113	VSS_27	D13
U25	VSS_112	VSS_26	D10
U24	VSS_111	VSS_25	D7
U23	VSS_110	VSS_24	D1
U15	VSS_109	VSS_23	C22
U13	VSS_108	VSS_22	C20
T27	VSS_107	VSS_21	C18
T26	VSS_106	VSS_20	C14
T23	VSS_105	VSS_19	C4
T16	VSS_104	VSS_18	B25
T15	VSS_103	VSS_17	B24
T14	VSS_102	VSS_16	B23
T13	VSS_101	VSS_15	B19
T12	VSS_100	VSS_14	B15
T7	VSS_99	VSS_13	B13
T1	VSS_98	VSS_12	A26
R25	VSS_97	VSS_11	A23
R24	VSS_96	VSS_10	A21
R17	VSS_95	VSS_9	A19
R16	VSS_94	VSS_8	A15
R15	VSS_93	VSS_7	A12
R14	VSS_92	VSS_6	A9
R13	VSS_91	VSS_5	A7
R12	VSS_90	VSS_4	A4
R11	VSS_89	VSS_3	A1
R4	VSS_88	VSS_2	
	VSS_87	VSS_1	

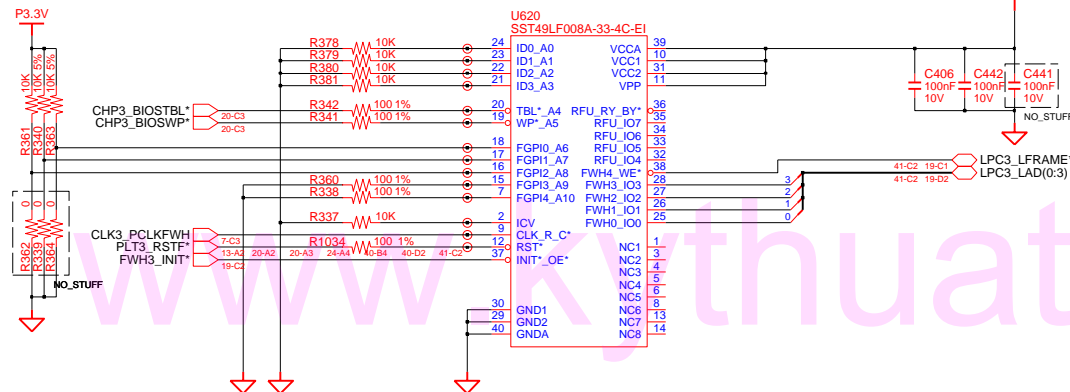


ICH6-m Strapping Options

	Function	Default
CHP3_SPKR	No Reboot	No Stuff
CHP3_BIOSWP*	Boot BIOS	No Stuff
PC/PCI_GNTA*	A16 swap override	No Stuff
AC97_SDOUT	Safe Mode	TBD
EEP_DOUT		TBD

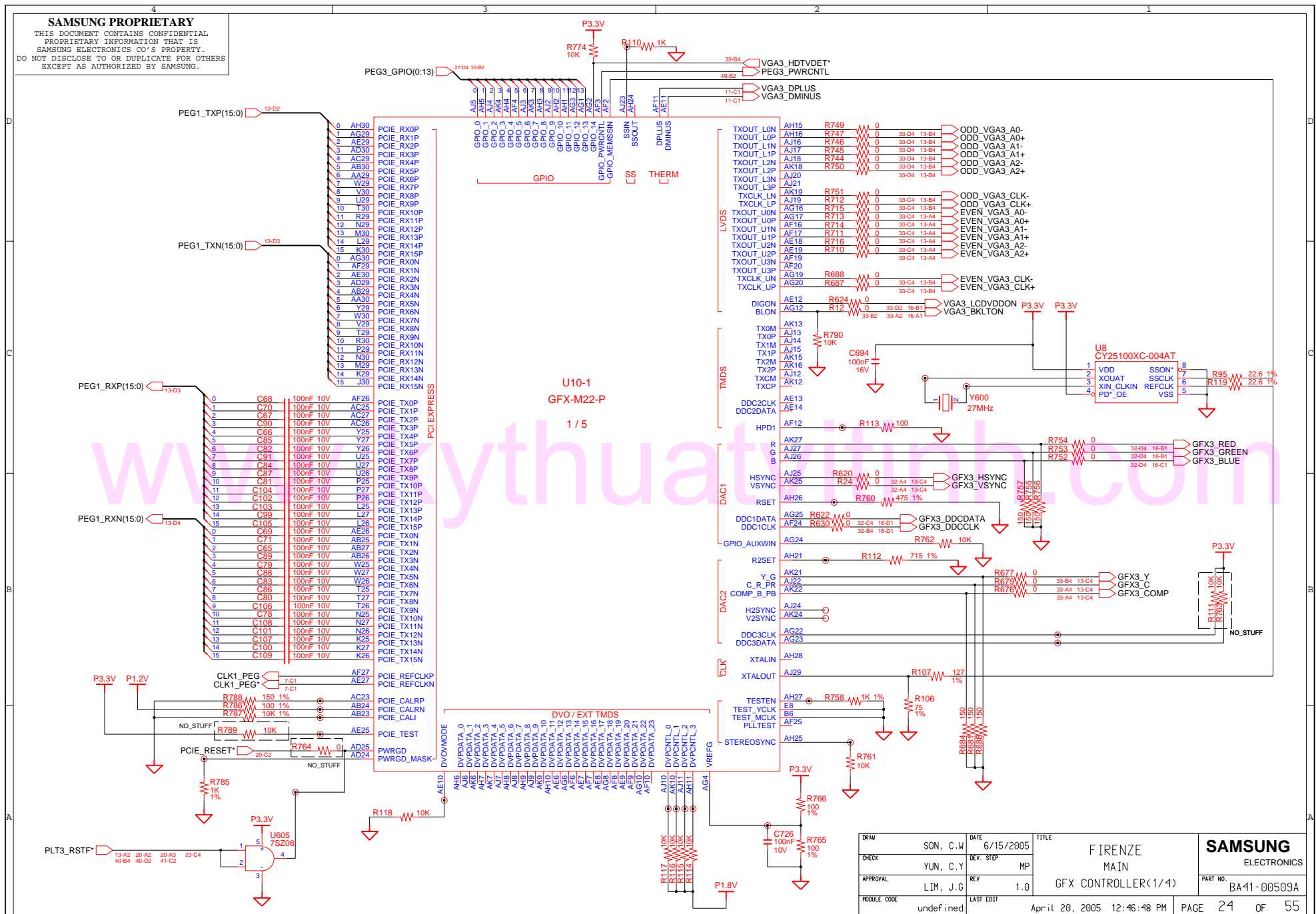


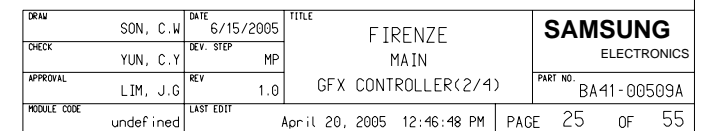
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CHECK	YUN, C.Y	DEV. STEP	MP	MAIN	BA41-00509A	
APPROVAL	LIM, J.G	REV	1.0	SOUTH BRIDGE(4/4)		
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	22	OF 55

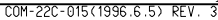


- | | | | |
|----|------------------------------------|----|---------------------------------|
| 02 | VERIFY REAL TIME | 66 | CONFIGURE ADVANCED CACHE REG. |
| 03 | DISABLE NMI | 6A | DISPLAY EXTERNAL CACHE SIZE |
| 04 | GET CPU TYPE | 6C | DISPLAY SHADOW MESSAGE |
| 06 | INIT. SYSTEM H/W | 6E | DISPLAY NON-DISPOSABLE SEGMENT |
| 08 | INIT. CHIPSET REG. | 70 | DISPLAY ERROR MESSAGE |
| 09 | SET IN POST FLAG | 72 | INIT. FOR CONFIGURATION ERROR |
| 0A | INIT CPU.REG | 74 | TEST REAL-TIME CLOCK |
| 0B | CPU CACHE ON | 76 | CHECK FOR KEYBOARD ERROR |
| 0C | INIT.CACHE TO POST | 7C | SETUP HARDWARE INTERRUPT VECTOR |
| 0E | INIT. I/O VALUE | 7E | TEST COPROCESSER IF PRESENT |
| 0F | ENABLE THE L-BUS IDE | 80 | DISABLE ON-BOARD I/O PORT |
| 10 | INIT. POWER MANAGER | 82 | DETECT AND INSTALL EXT.RS232C |
| 11 | LOAD ALTERNATE REG. | 84 | DETECT AND INSTALL EXT.PARALLEL |
| 13 | PCI BUS MASTER RESET | 86 | RE-INIT. ON-BOARD I/O PORT |
| | WITH INITIAL POST VALUE | 88 | INIT. BIOS DATA ROM |
| 14 | INIT. KEYBOARD CONTROLLER | 8A | INIT.EXTENDED BIOS DATA AREA |
| 16 | CHECK CHECKSUM | 8C | INIT. FDD CONTROLLER |
| 18 | 8254 TIMER INIT. | 9A | SHADOW OPTION ROMS |
| 1A | 8237 DMA CONTROLLER INIT. | 9C | SETUP POWER MANAGEMENT |
| 1C | RESET INTERRUPT CONTROLLER | 9E | ENABLE H/W INTERRUPT |
| 20 | TEST DRAM REFRESH | A0 | SET TIME OF DAY |
| 22 | TEST 8742 KEYBOARD CONTROLLER | A4 | INIT. TYPEMATIC RATE |
| 24 | SET ES SEGMENT REG. TO 4GB | A8 | ERASE F2 PROMPT |
| 26 | ENABLE A20 | AA | SCAN FOR F2 KEY STROKE |
| 28 | AUTO SIZING DRAM | AC | ENTER SETUP |
| 32 | COMPUTE THE CPU SPEED | AE | CLEAR IN POST FLAG |
| 34 | TEST CMOS RAM | B0 | CHECK FOR ERRORS |
| 38 | SHADOW SYSTEM BIOS ROM | B2 | POST DONE-PREPARE TO BOOT O/S |
| 3A | AUTO SIZING CACHE | B4 | ONE BEEP |
| 3C | CONFIGURE ADVANCED CHIPSET REG. | B6 | CHECK PASSWORD (OPTION) |
| 3D | LOAD ALTER REG. WITH CMOS VALUE | B7 | ACPI INIT |
| 42 | INIT. INTERRUPT VECTOR | BA | DMI INIT |
| 44 | INIT. BIOS INTERRUPT | BE | CLEAR SCREEN |
| 46 | CHECK ROM COPYRIGHT NOTICE | C0 | TRY BOOT WITH INT19 |
| 47 | INIT. I20 SUPPORT IF INSTALLED | D0 | INTERRUPT HANDLER ERROR |
| 48 | CHECK VIDEO CONFIGURE AGAINST CMOS | D2 | UNKNOWN INTERRUPT ERROR |
| 49 | INIT. PCI BUS AND DEVICE | D4 | PENDING INTERRUPT ERROR |
| 4A | INIT. ALL VIDEO BIOS ROM | D6 | SHUTDOWN 5 |
| 4C | SHADOW VIDEO BIOS ROM | D8 | SHUTDOWN ERROR |
| 50 | DISPLAY CPU TYPE AND SPEED | DA | EXTENDED BLOCK MOVE |
| 52 | TEST KEYBOARD | DC | SHUTDOWN 10 |
| 54 | SET KEYCLICK IF ENABLED | 89 | ENABLE NMI |
| 56 | ENABLE KEYBOARD | 90 | INIT. HDD CONTROLLER |
| 58 | TEST FOR UNEXPECTED INTERRUPTS | 91 | INIT. LOCAL BUS HDD CONTROLLER |
| 5A | DISPLAY "PRESS SETUP" | 92 | JUMP TO USER PATCH 2 |
| 5C | TEST RAM BETWEEN 512K AND 640K | 94 | DISABLE A20 ADDRESS LINE |
| 60 | TEST EXTENDED MEMORY | 96 | CLEAR HUGE ES SEGMENT REG. |
| 62 | TEST EXTENDED MEMORY ADDRESS LINE | 98 | SEARCH FOR OPTION ROMS |
| 64 | JUMP TO USER PATCH 1 | | |

DRAM	SON, C. W	DATE	6/15/2005	TITLE			FIRENZE		SAMSUNG ELECTRONICS	
CHECK	YUN, C. Y	DEV. STEP	MP							
APPROVAL	LIM, J. G	REV	1.0							
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM							
							PART NO.		BA41-00509A	

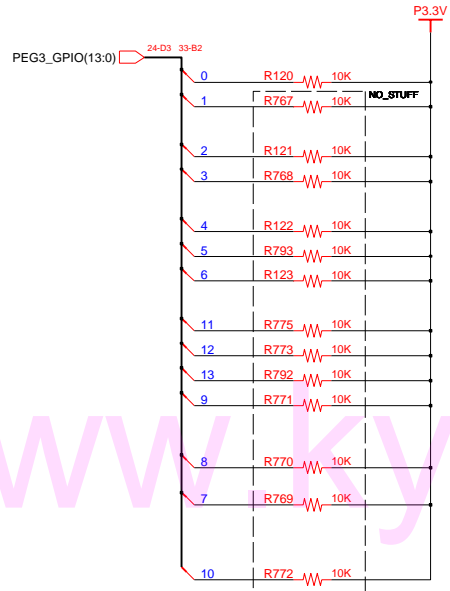






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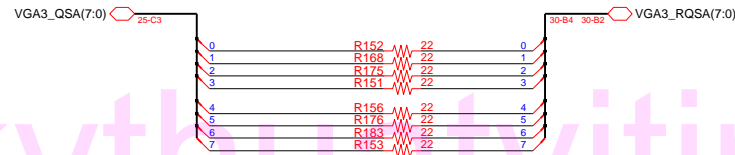


Straps	Pin Number	Descriptions
CAL_BG_BACKUP	GPIO0	PCI-Express Current Calibration Bandgap Backup 0 : use reference voltage from bandgap (Default) 1 : use reference voltage from resistor divider
PLL_CAL_FORCE_EN	GPIO1	PCI-Express PLL Calibration Force Enable 0 : Disable PLL force calibration (Default) 1 : Enable PLL force calibration
PCIE Mode(1:0)	GPIO(3:2)	PCI-Express Mode 00 : PCI Express 1.0A mode (Default) 01 : Reserved 10 : PCI Express 1.0 mode 11 : Reserved
CAL_OFF	GPIO4	Turn-Off PCI-Express Impedance / Strength Calibration 0 : Enable (Default) 1 : Disable Also, used to demux VCoreF / CALREF
BYPASS_PLL	GPIO5	Bypass PCI-Express PLL 0 : - (Default) 1 : -
ICOMP	GPIO6	PCI-Express Transmitter Current Compensation 0 : Normal (Default) 1 : Inject extra current for output buffer switching
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDs. 0000 : No ROM, CHG_ID = 0 0001 : No ROM, CHG_ID = 1 0100 : Reserved 0110 : Reserved Others : ROM (Third party vendors)
DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.

DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0		GFX CONTROLLER(4/4)	PART NO. BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	27	OF 55

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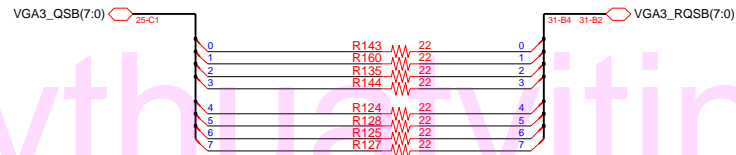


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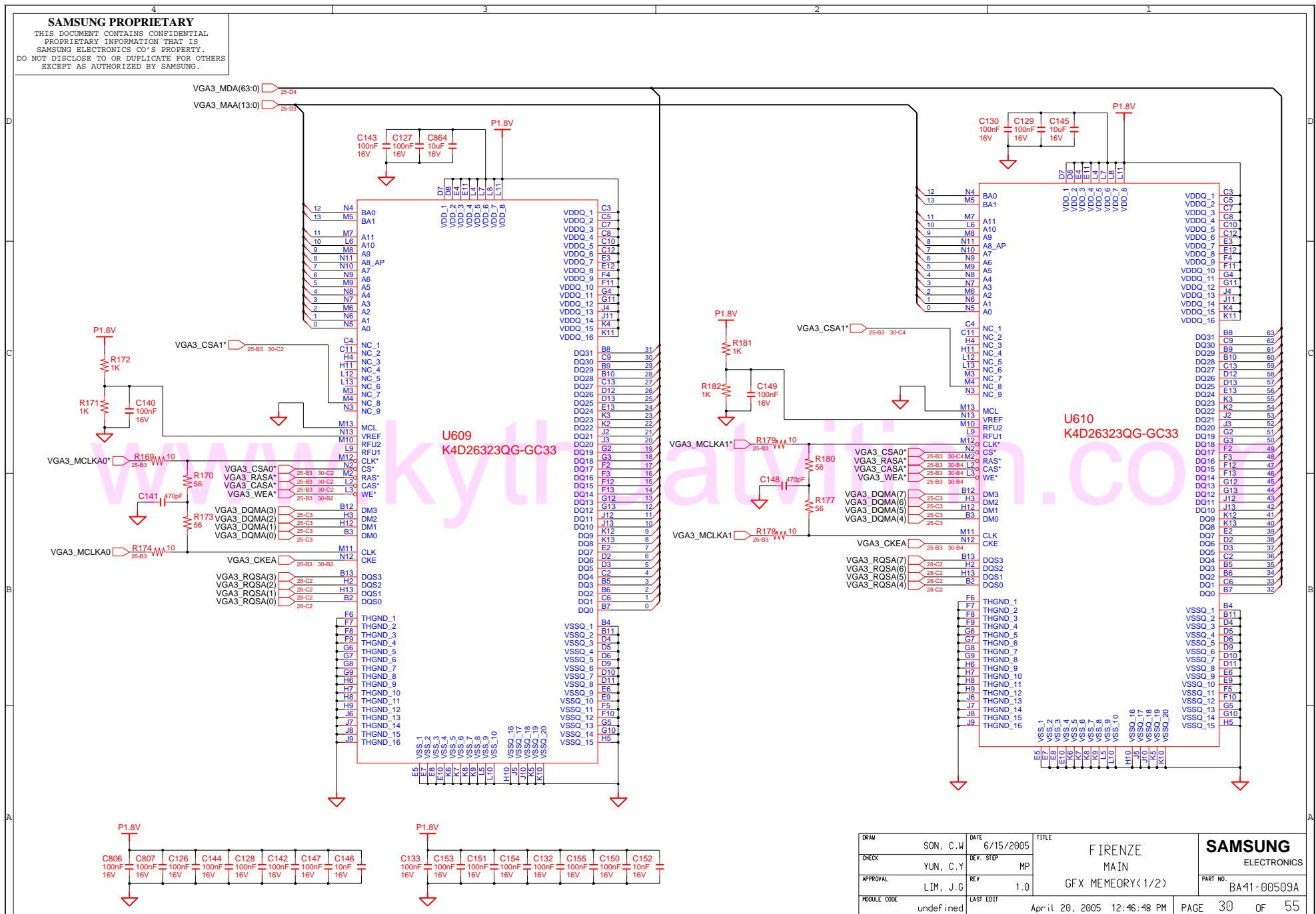
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CHECK	YUN, C.Y	DEV. STEP	MP	MAIN		
APPROVAL	LIM, J.G	REV	1.0	GFX MEMORY TERM(1/2)	PART NO.	BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	28	OF 55

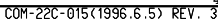
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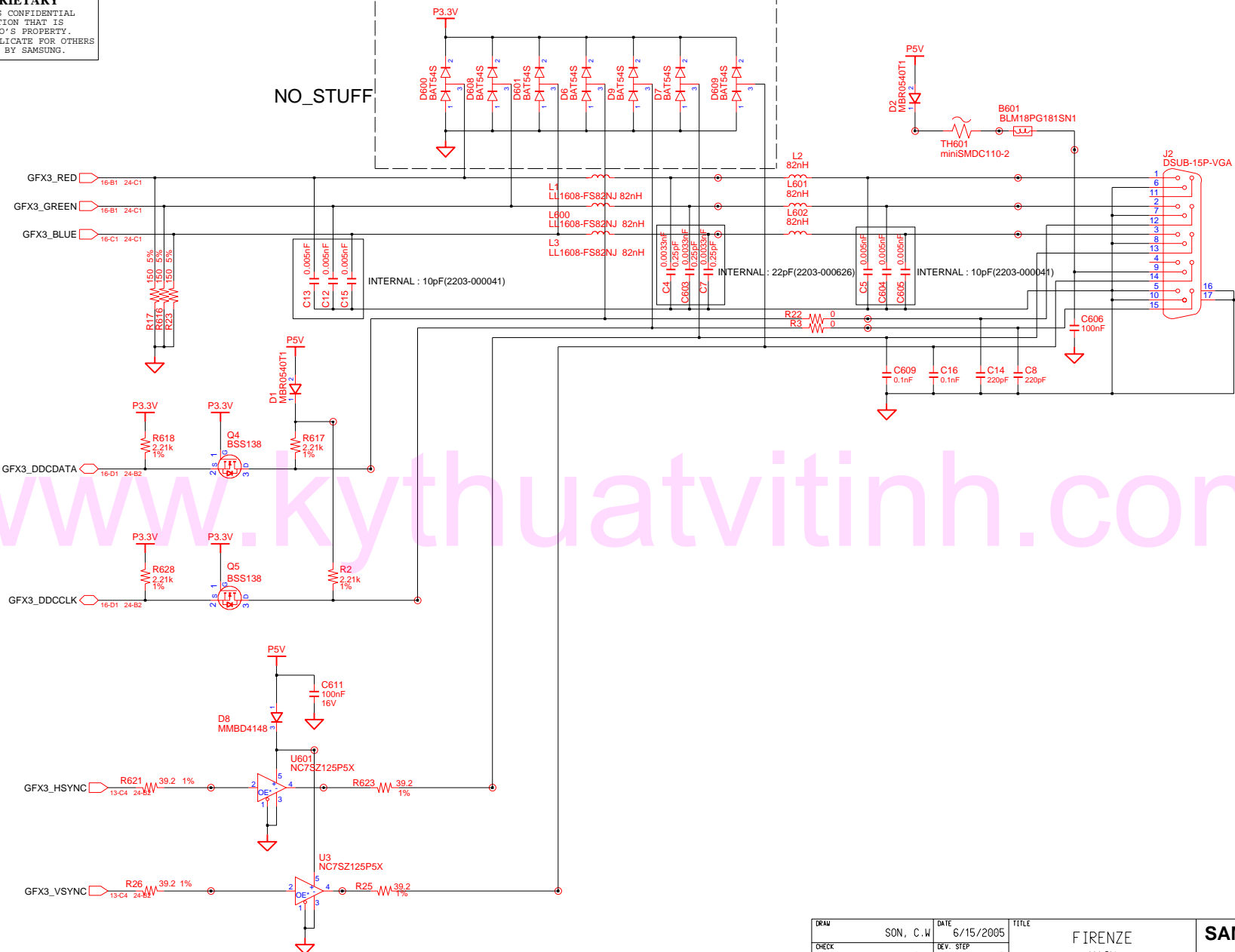
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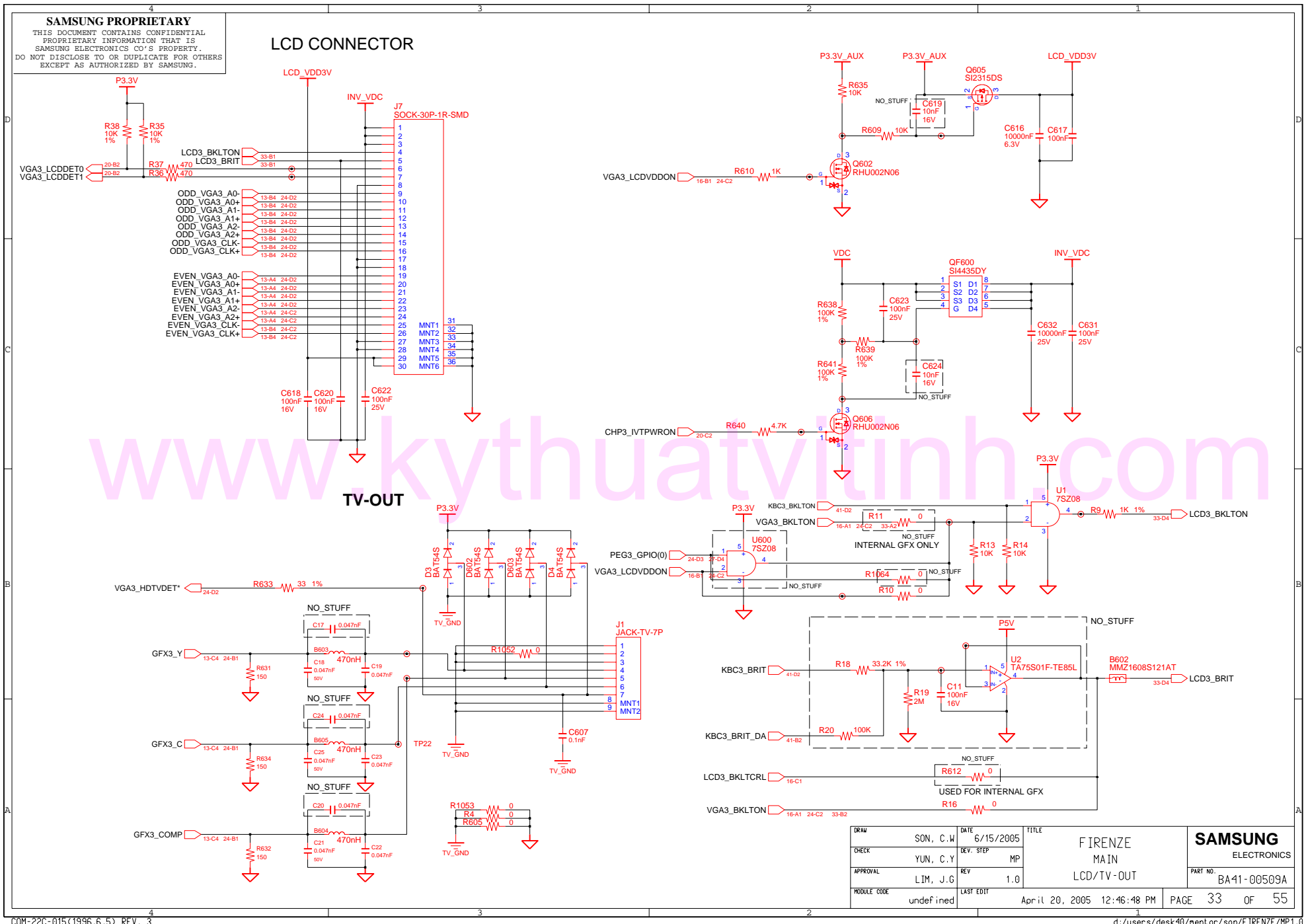
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CHECK	YUN, C.Y	DEV. STEP	MP			
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MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	29	OF 55

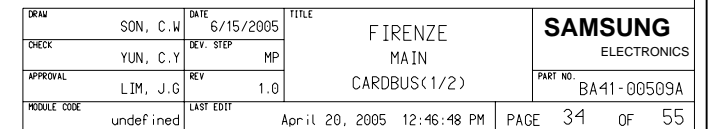


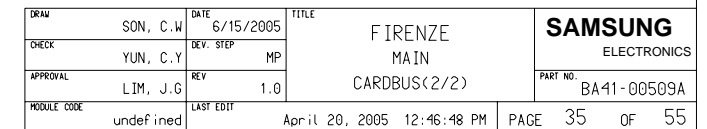


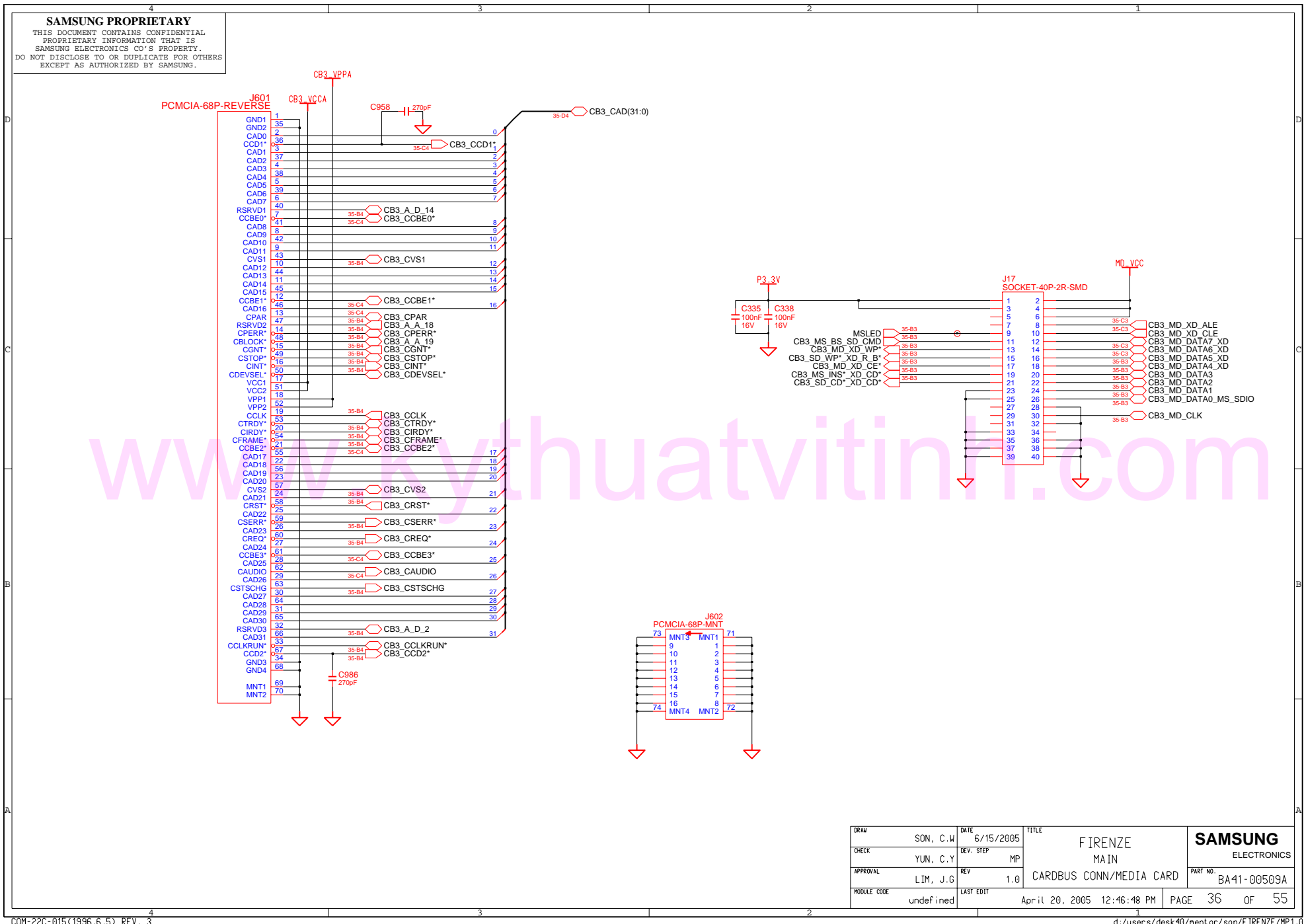


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CHECK	YUN, C.Y	DEV. STEP	MP				
APPROVAL	LIM, J.G	REV	1.0				
MODULE CODE		LAST EDIT		PART NO.		BA41-00509A	
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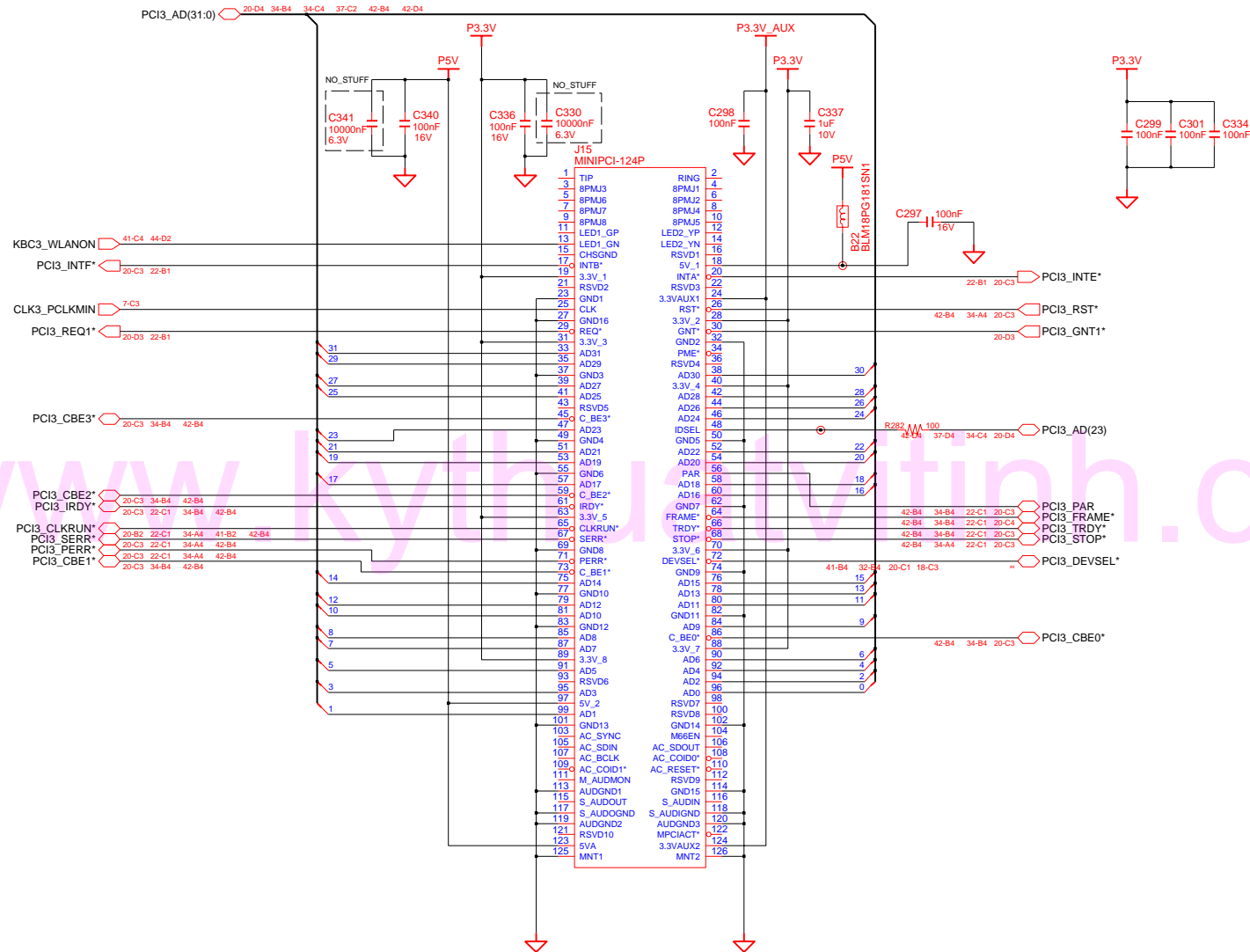




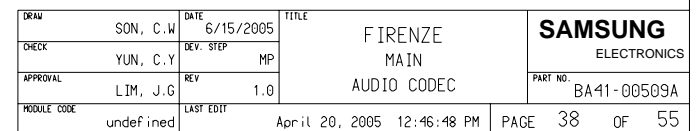
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MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	36	OF 55

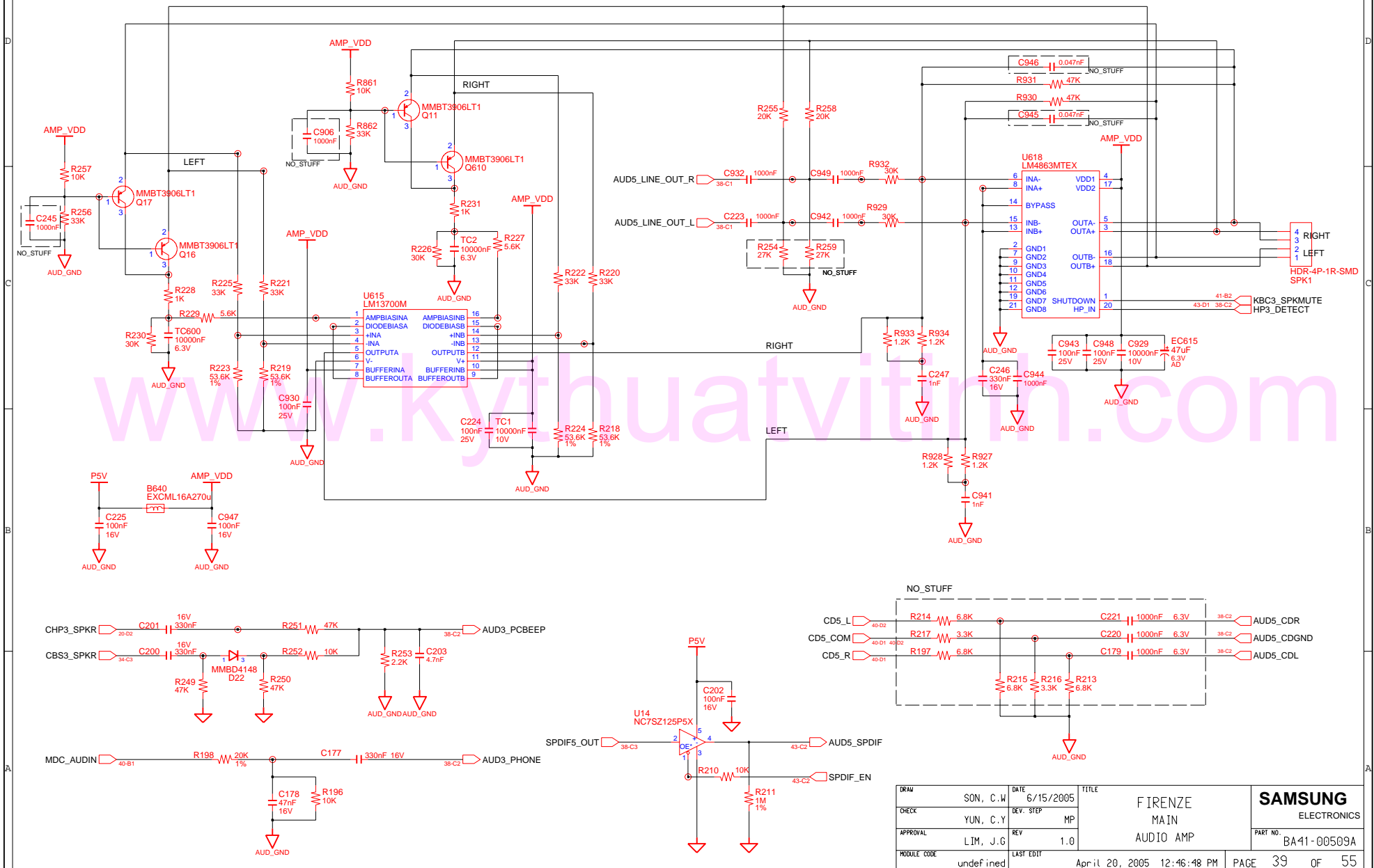
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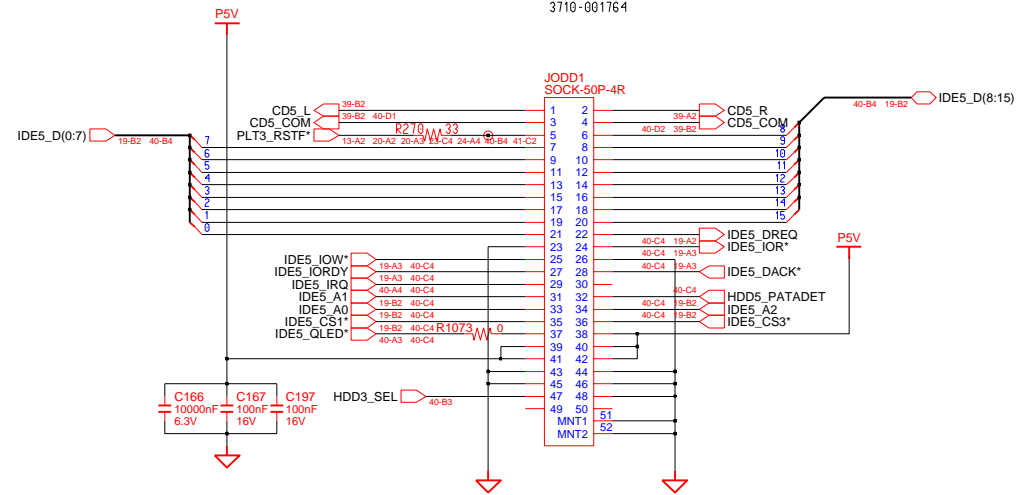
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APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	37	OF 55



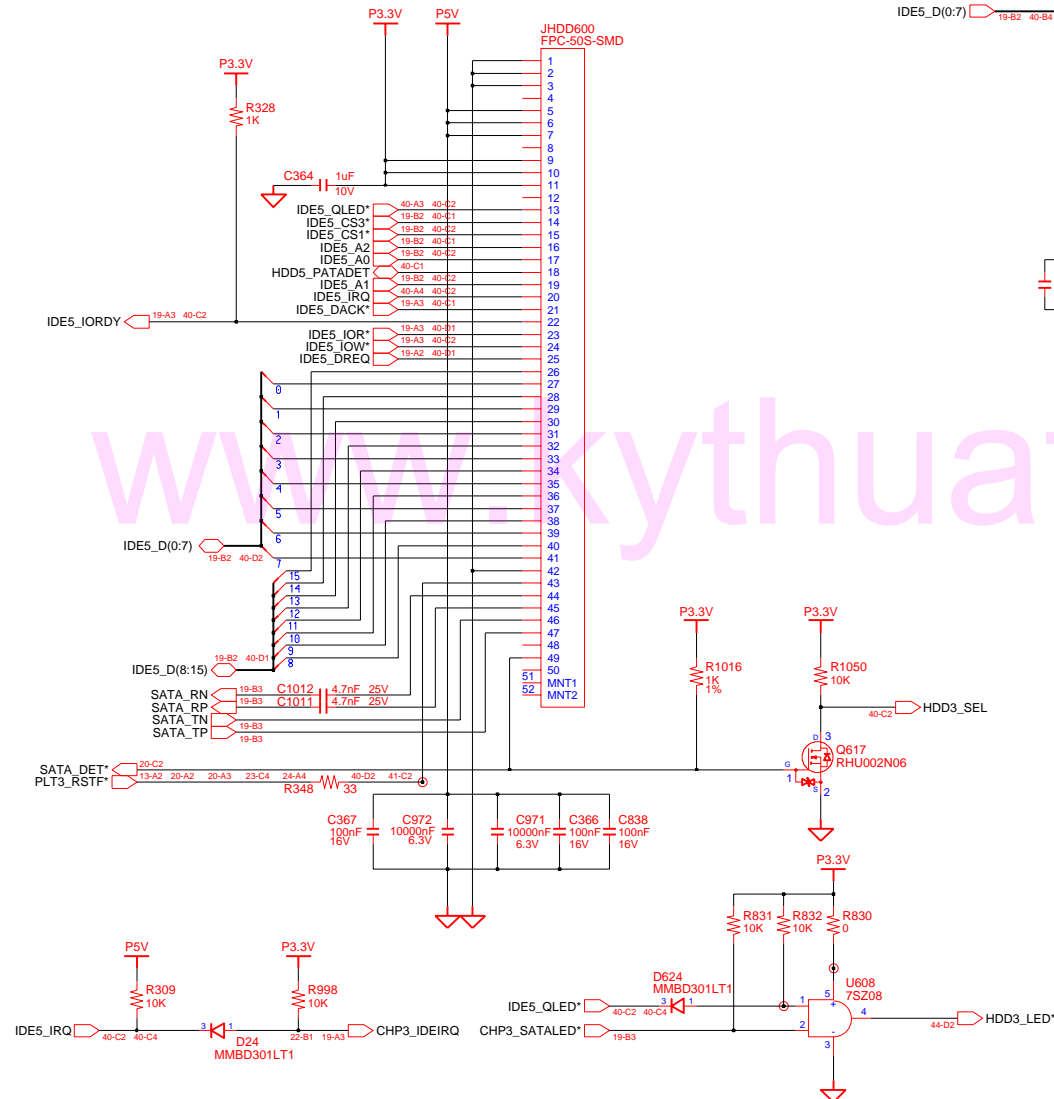
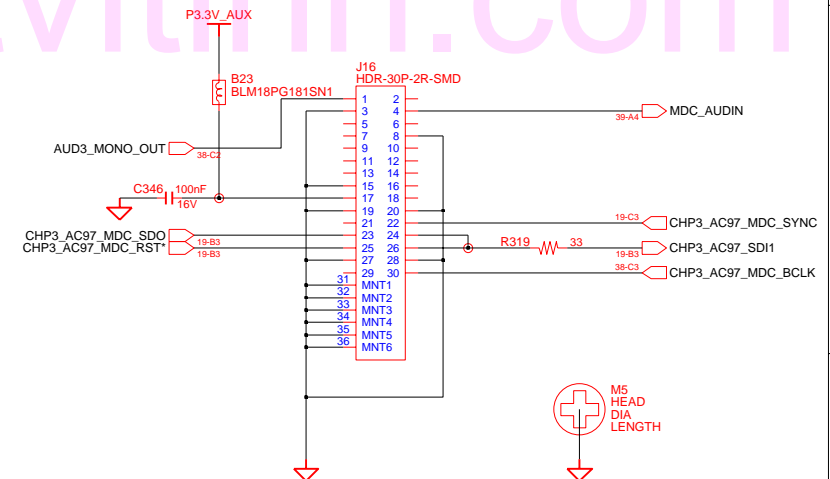



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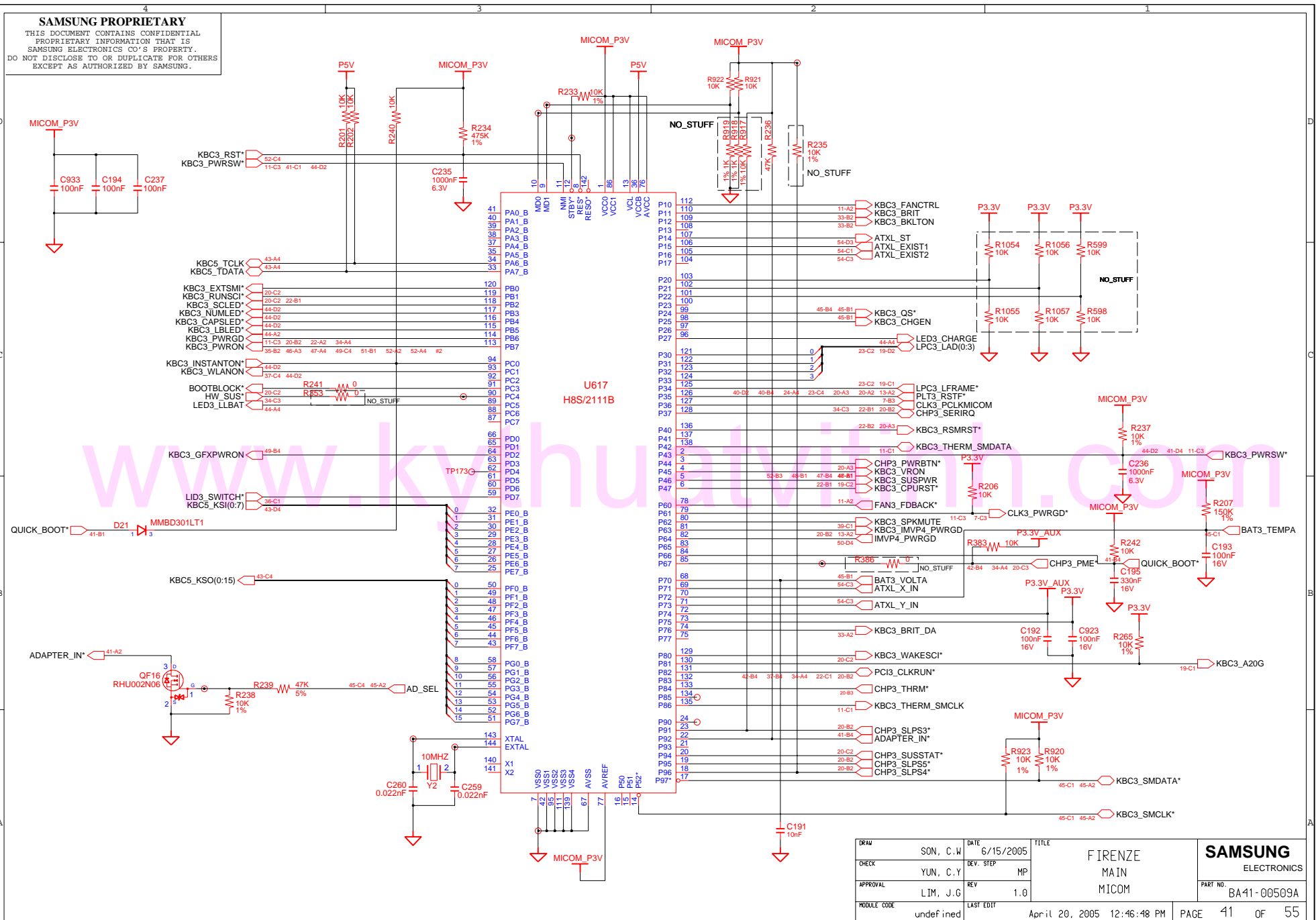
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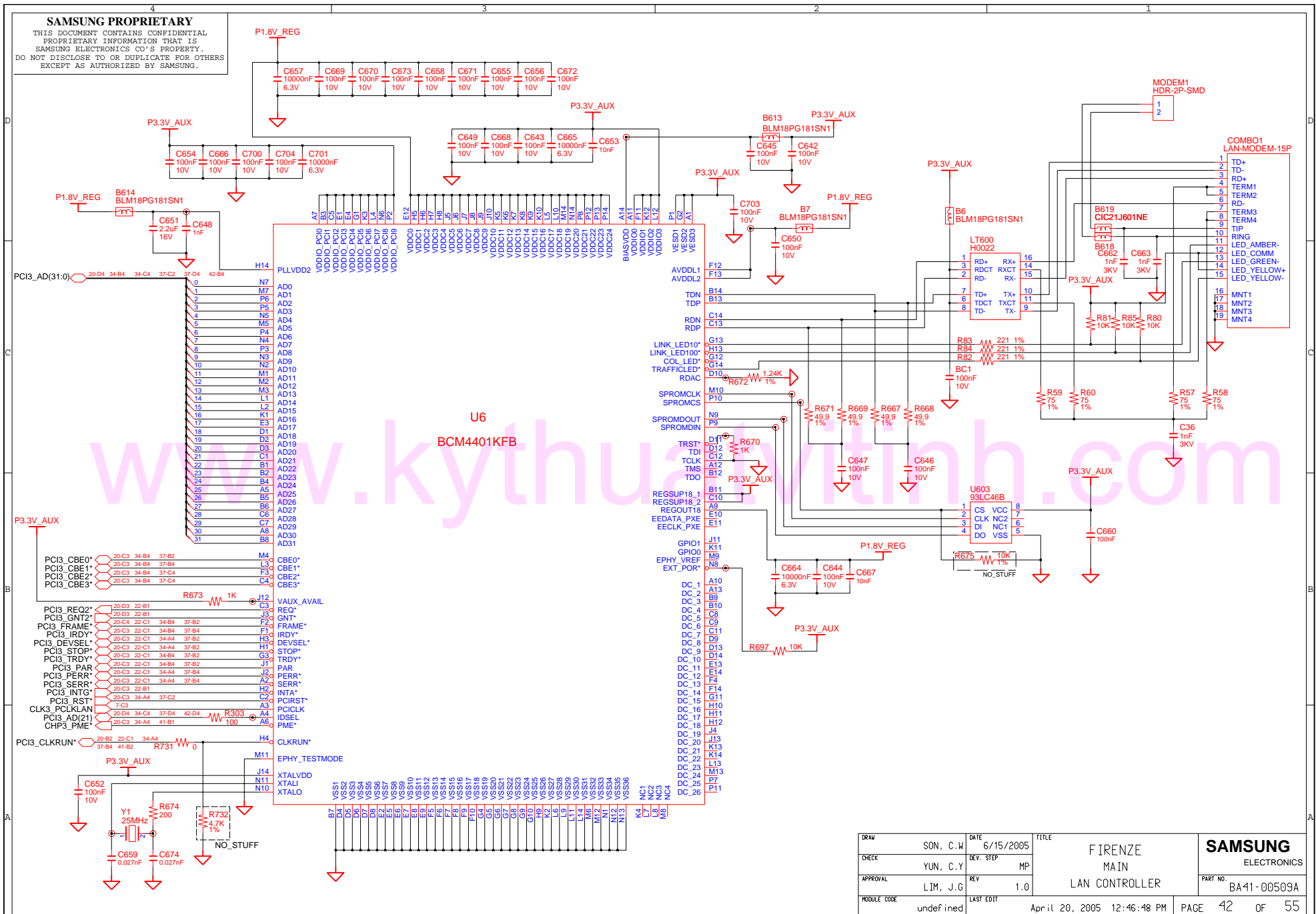


MDC Connector



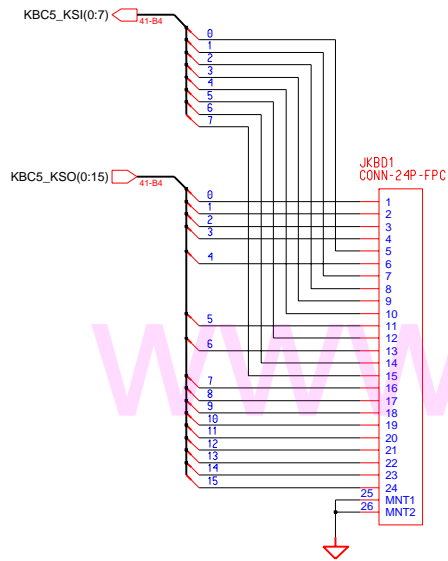
DRAW	SON, C.W	DATE	6/15/2005	TITLE FIRENZE MAIN HDD/ODD/MDC CONN			
CHECK	YUN, C.Y	DEV. STEP	MP				
APPROVAL	LIM, J.G	REV	1.0				
MODULE CODE		LAST EDIT		April 20, 2005 12:46:48 PM		PAGE	40 OF 55



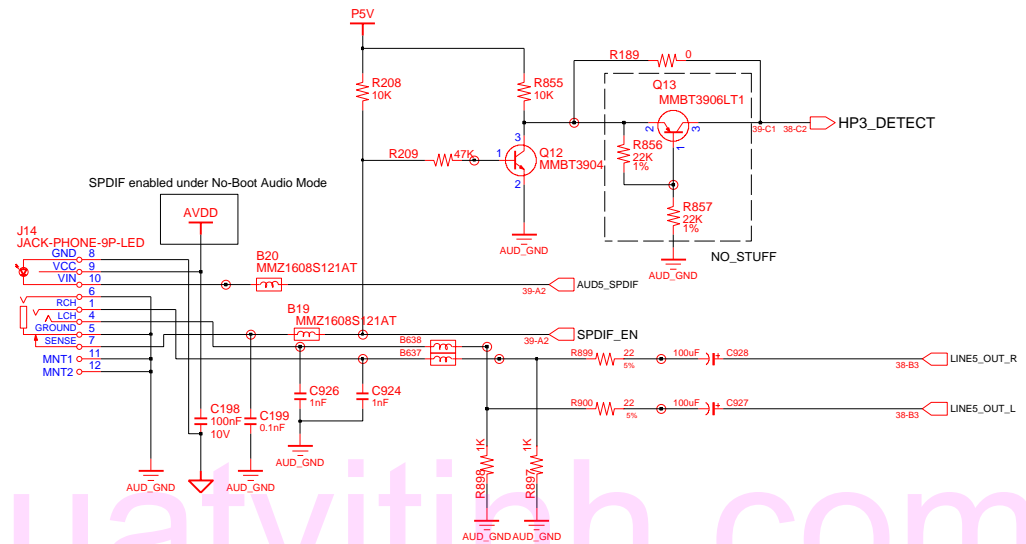
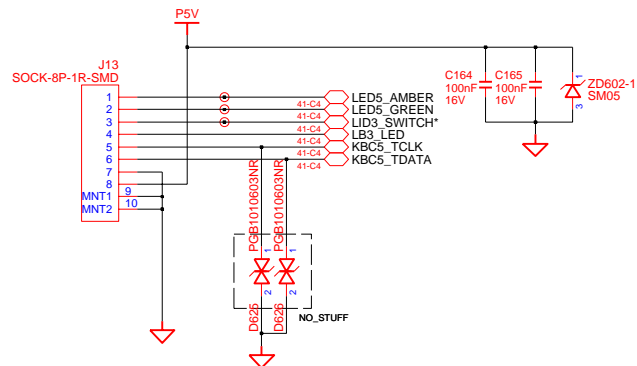


DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG ELECTRONICS PART NO. BA41-00509A
CHECK	YUN, C.Y	DEV. STEP	MP	MAIN	LAN CONTROLLER	
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	42 OF 55	

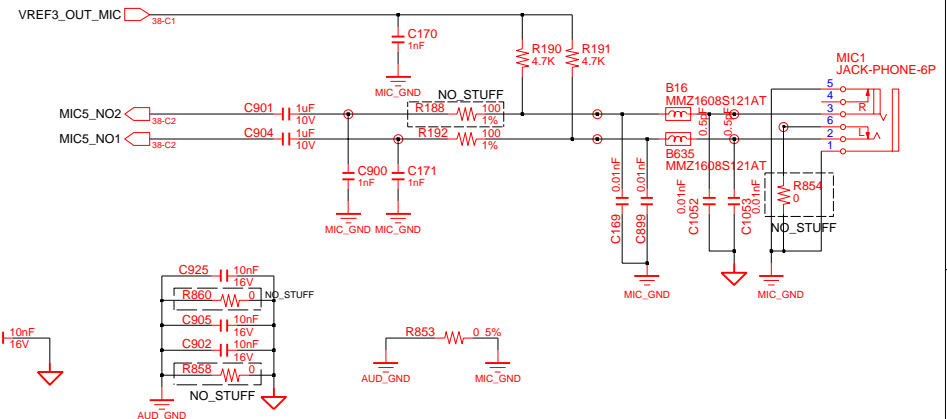
KEYBOARD



TOUCH PAD



MICROPHONE

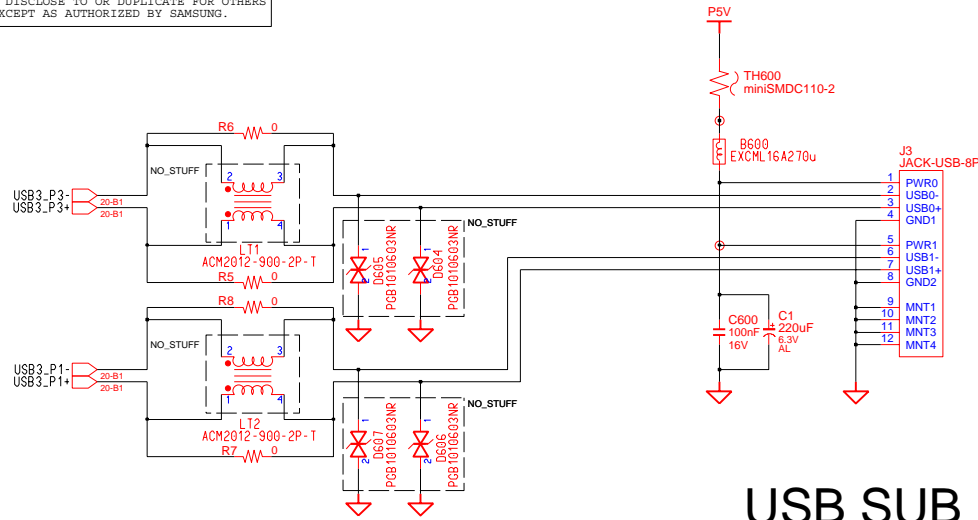


DRAM	SON, C.W	DATE	6/15/2005	TITLE	F IRENZE MAIN KBD/TPAD/HP/MIC	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM			
				PART NO.	BA11-00509A	

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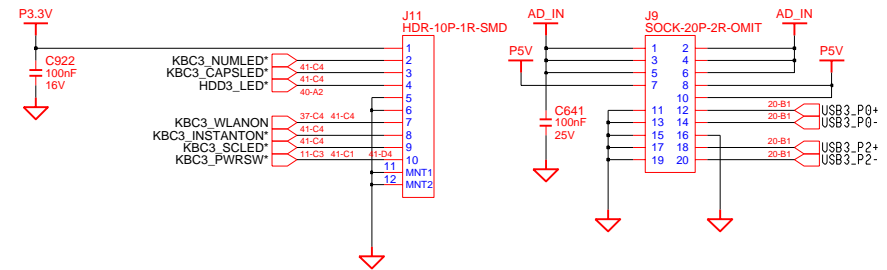
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USB PORT

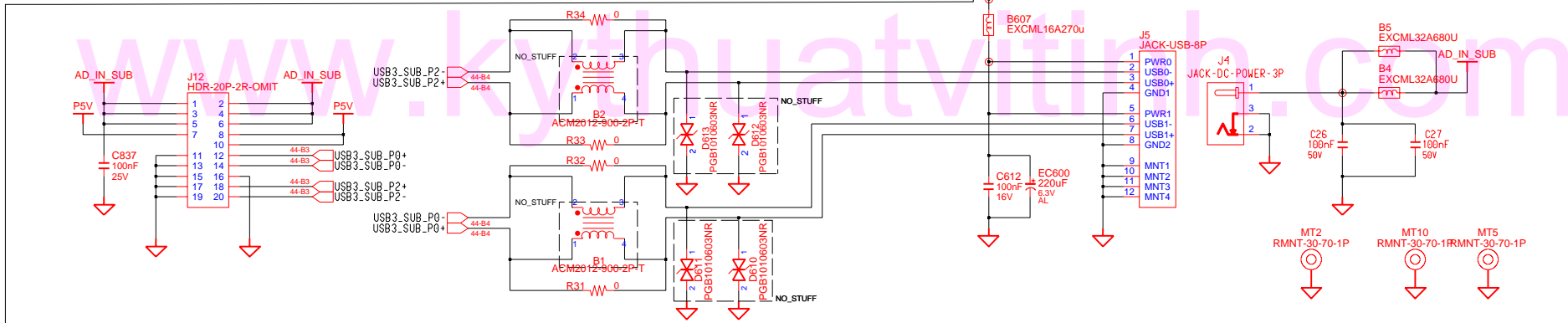


MAIN TO ON-TOP

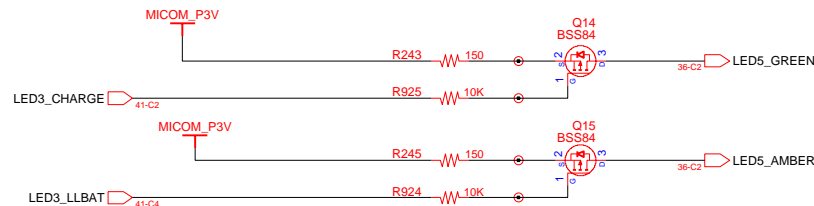
MAIN TO USB



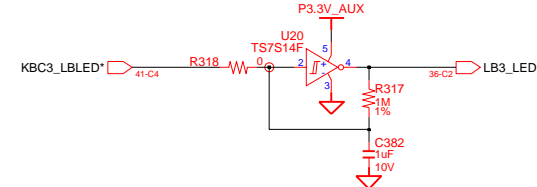
USB SUB B'D



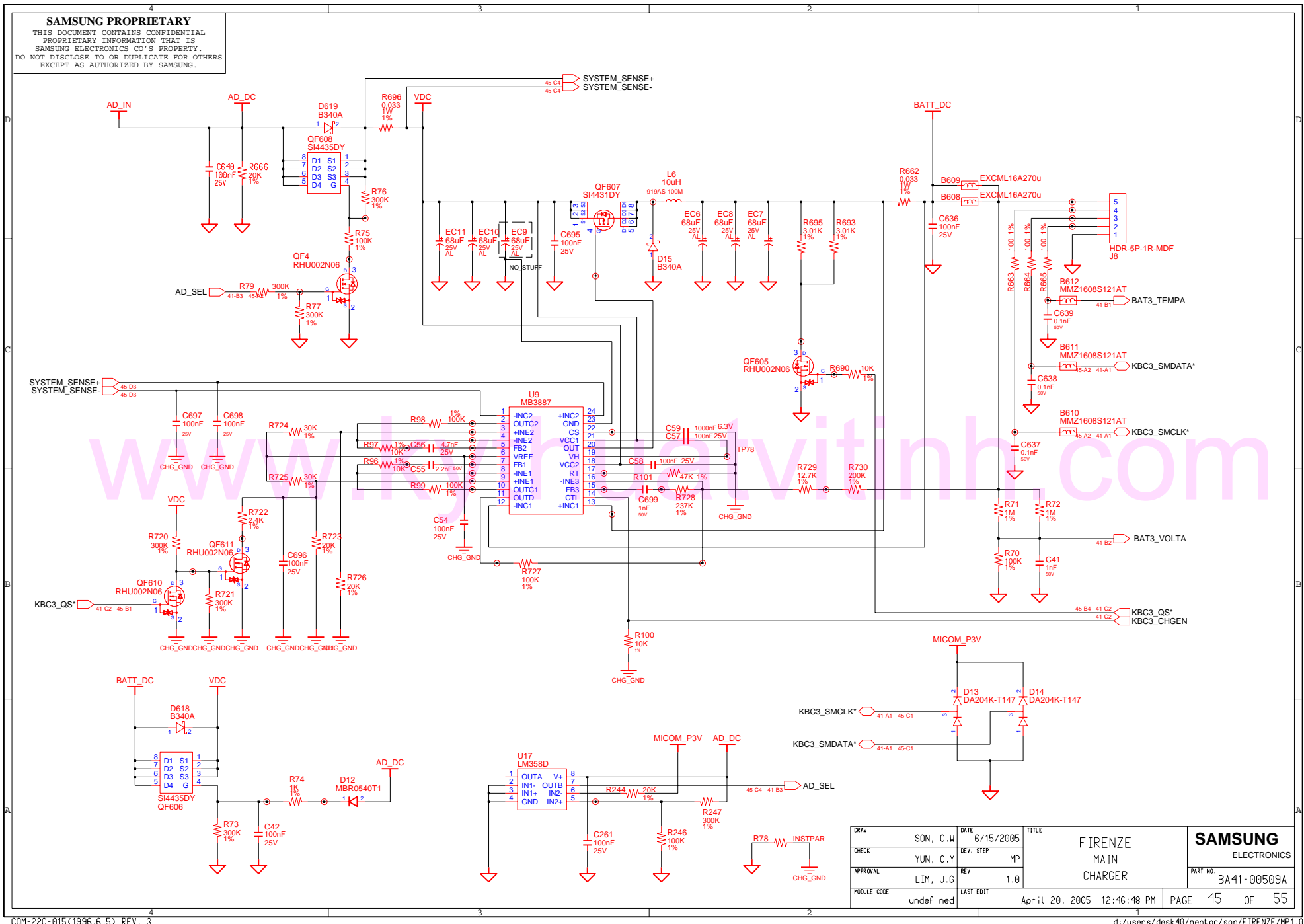
ADAPTER IN / CHARGER LED



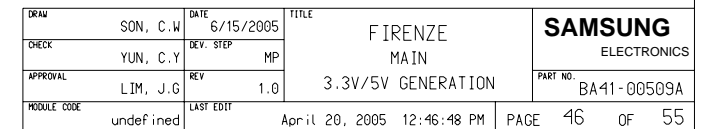
POWER ON / LB LED



DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE	SAMSUNG
CHECK	YUN, C.Y	DEV. STEP	MP		MAIN	ELECTRONICS
APPROVAL	LIM, J.G	REV	1.0		USB PORT/LED/ON-TOP	PART NO. BA41-00509A
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	44	OF 55

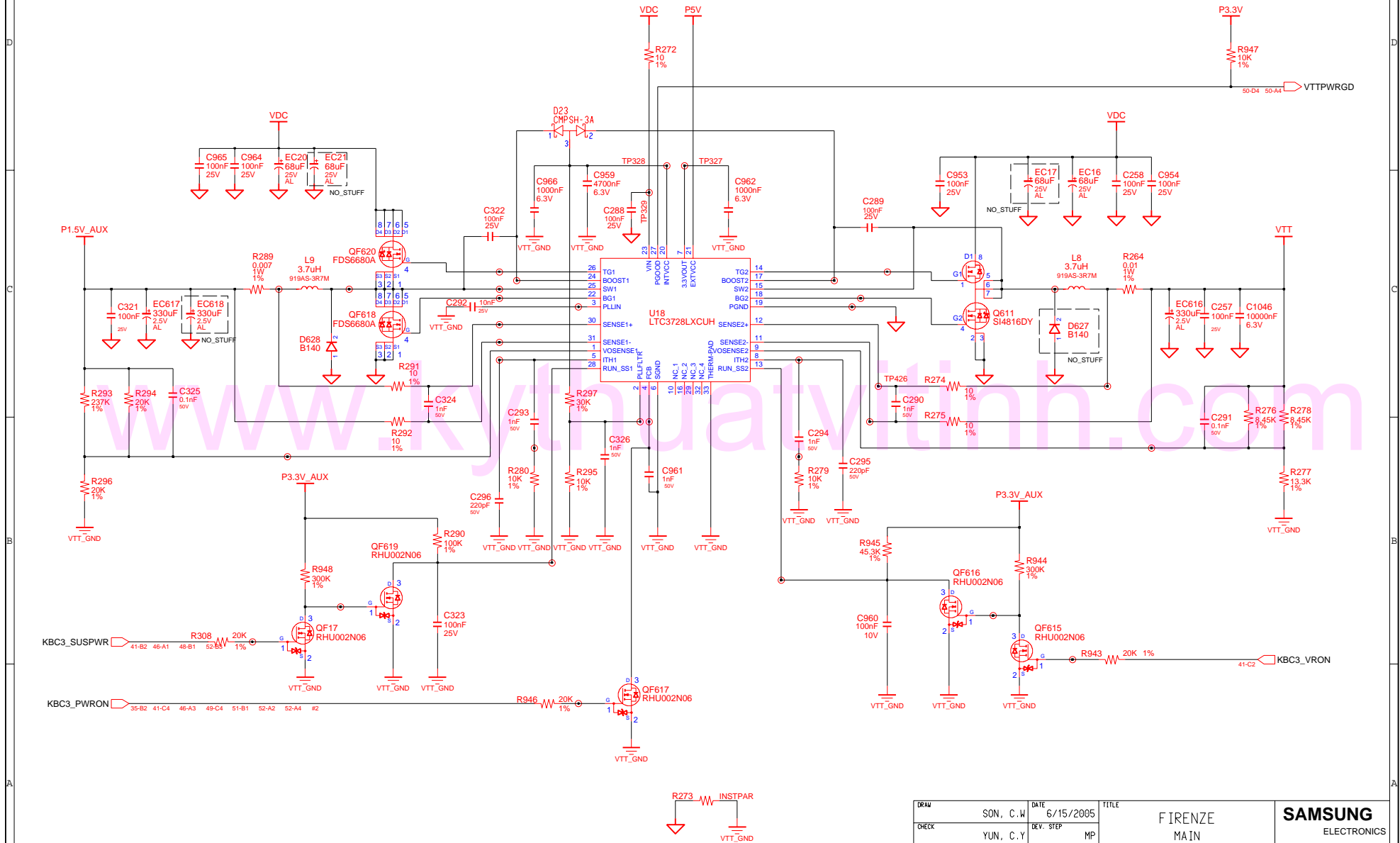


DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN CHARGER	SAMSUNG ELECTRONICS PART NO. BA41-00509A
CHECK	YUN, C.Y	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	45 OF 55	



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DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN 1.5V_AUX/VTT	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			PART NO. BA41-00509A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	47	OF 55

The schematic diagram illustrates the electrical connections for the SC1486AITSTR microcontroller. Key components include:

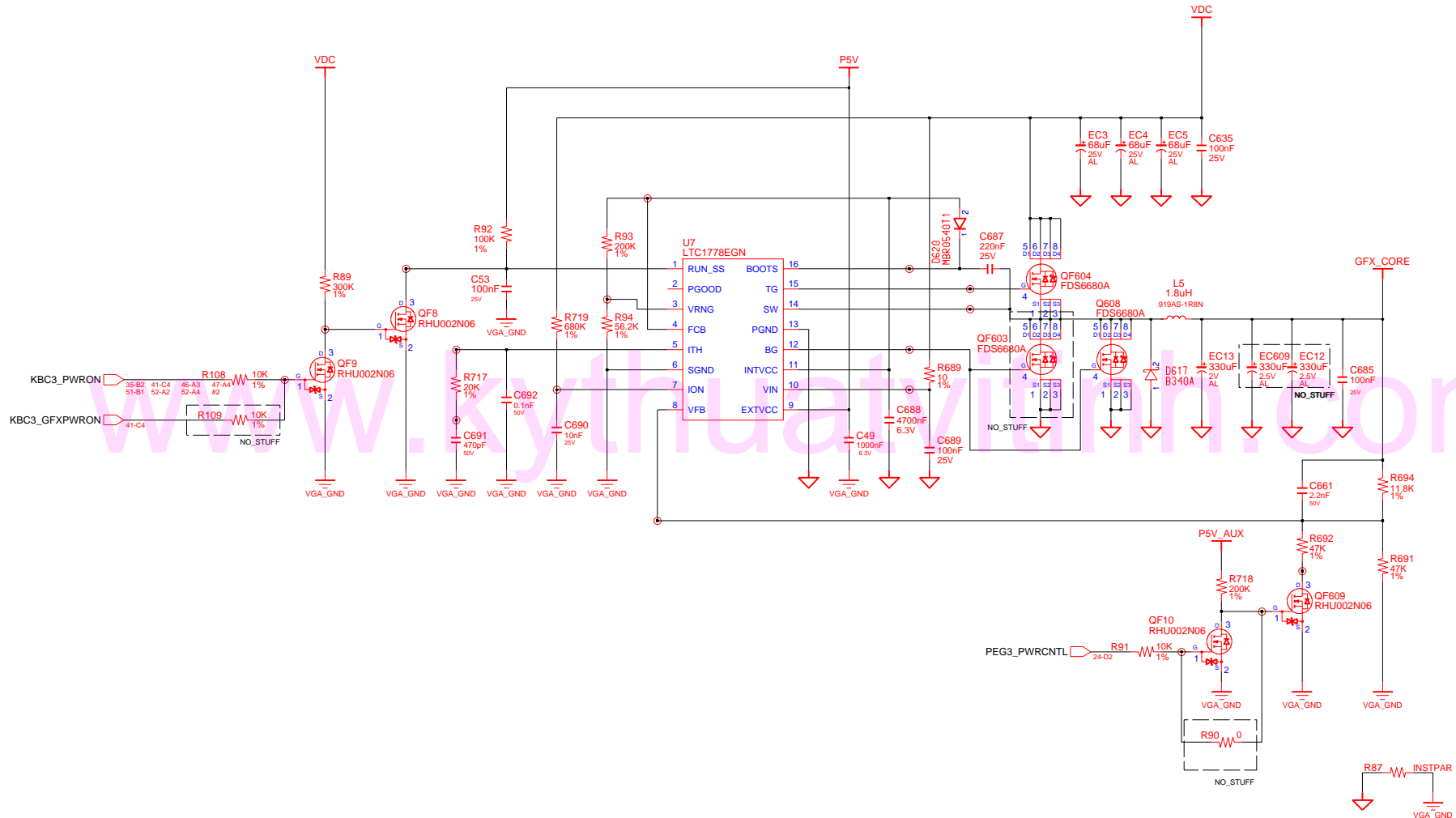
- Microcontroller (U22):** SC1486AITSTR, a 28-pin device with pins labeled PGND1, DL1, VDDP1, ILIM1, LX1, DH1, BST1, REFIN, TON2, REFOUT, VCCA2, FBK2, PGOOD2, AGND2, AGND1, PGOOD1, FBK1, VCCA1, VOUT1, TON1, EN, PSV1, BST2, DH2, LX2, ILIM2, VDDP2, DL2, and PGND2.
- Power Supply:** P1.8V_AUX (253 ~ 272KHz), MEM1_VREF, P5V_AUX, P1.8V_AUX, P5V, P1.8V_AUX, and VDC.
- Resistors:** R957, R960, R958, R959, C991, R984, R985, R986, R987, R988, R989, R990, R991, R992, R993, R994, R995, R996, R997, R998, R999, R1000, R1001, R1002, R1003, R1004, R1005, R1006, R1007, R1008, R1009, R1010, R1011, R1012, R1013, R1014, R1015, R1016, R1017, R1018, R1019, R1020, R1021, R1022, R1023, R1024, R1025, R1026, R1027, R1028, R1029, R1030, R1031, R1032, R1033, R1034, R1035, R1036, R1037, R1038, R1039, R1040, R1041, R1042, R1043, R1044, R1045, R1046, R1047, R1048, R1049, R1050, R1051, R1052, R1053, R1054, R1055, R1056, R1057, R1058, R1059, R1060, R1061, R1062, R1063, R1064, R1065, R1066, R1067, R1068, R1069, R1070, R1071, R1072, R1073, R1074, R1075, R1076, R1077, R1078, R1079, R1080, R1081, R1082, R1083, R1084, R1085, R1086, R1087, R1088, R1089, R1090, R1091, R1092, R1093, R1094, R1095, R1096, R1097, R1098, R1099, R1100, R1101, R1102, R1103, R1104, R1105, R1106, R1107, R1108, R1109, R1110, R1111, R1112, R1113, R1114, R1115, R1116, R1117, R1118, R1119, R1120, R1121, R1122, R1123, R1124, R1125, R1126, R1127, R1128, R1129, R1130, R1131, R1132, R1133, R1134, R1135, R1136, R1137, R1138, R1139, R1140, R1141, R1142, R1143, R1144, R1145, R1146, R1147, R1148, R1149, R1150, R1151, R1152, R1153, R1154, R1155, R1156, R1157, R1158, R1159, R1160, R1161, R1162, R1163, R1164, R1165, R1166, R1167, R1168, R1169, R1170, R1171, R1172, R1173, R1174, R1175, R1176, R1177, R1178, R1179, R1180, R1181, R1182, R1183, R1184, R1185, R1186, R1187, R1188, R1189, R1190, R1191, R1192, R1193, R1194, R1195, R1196, R1197, R1198, R1199, R1200, R1201, R1202, R1203, R1204, R1205, R1206, R1207, R1208, R1209, R1210, R1211, R1212, R1213, R1214, R1215, R1216, R1217, R1218, R1219, R1220, R1221, R1222, R1223, R1224, R1225, R1226, R1227, R1228, R1229, R1230, R1231, R1232, R1233, R1234, R1235, R1236, R1237, R1238, R1239, R1240, R1241, R1242, R1243, R1244, R1245, R1246, R1247, R1248, R1249, R1250, R1251, R1252, R1253, R1254, R1255, R1256, R1257, R1258, R1259, R1260, R1261, R1262, R1263, R1264, R1265, R1266, R1267, R1268, R1269, R1270, R1271, R1272, R1273, R1274, R1275, R1276, R1277, R1278, R1279, R1280, R1281, R1282, R1283, R1284, R1285, R1286, R1287, R1288, R1289, R1290, R1291, R1292, R1293, R1294, R1295, R1296, R1297, R1298, R1299, R1300, R1301, R1302, R1303, R1304, R1305, R1306, R1307, R1308, R1309, R1310, R1311, R1312, R1313, R1314, R1315, R1316, R1317, R1318, R1319, R1320, R1321, R1322, R1323, R1324, R1325, R1326, R1327, R1328, R1329, R1330, R1331, R1332, R1333, R1334, R1335, R1336, R1337, R1338, R1339, R1340, R1341, R1342, R1343, R1344, R1345, R1346, R1347, R1348, R1349, R1350, R1351, R1352, R1353, R1354, R1355, R1356, R1357, R1358, R1359, R1360, R1361, R1362, R1363, R1364, R1365, R1366, R1367, R1368, R1369, R1370, R1371, R1372, R1373, R1374, R1375, R1376, R1377, R1378, R1379, R1380, R1381, R1382, R1383, R1384, R1385, R1386, R1387, R1388, R1389, R1390, R1391, R1392, R1393, R1394, R1395, R1396, R1397, R1398, R1399, R1400, R1401, R1402, R1403, R1404, R1405, R1406, R1407, R1408, R1409, R1410, R1411, R1412, R1413, R1414, R1415, R1416, R1417, R1418, R1419, R1420, R1421, R1422, R1423, R1424, R1425, R1426, R1427, R1428, R1429, R1430, R1431, R1432, R1433, R1434, R1435, R1436, R1437, R1438, R1439, R1440, R1441, R1442, R1443, R1444, R1445, R1446, R1447, R1448, R1449, R1450, R1451, R1452, R1453, R1454, R1455, R1456, R1457, R1458, R1459, R1460, R1461, R1462, R1463, R1464, R1465, R1466, R1467, R1468, R1469, R1470, R1471, R1472, R1473, R1474, R1475, R1476, R1477, R1478, R1479, R1480, R1481, R1482, R1483, R1484, R1485, R1486, R1487, R1488, R1489, R1490, R1491, R1492, R1493, R1494, R1495, R1496, R1497, R1498, R1499, R1500, R1501, R1502, R1503, R1504, R1505, R1506, R1507, R1508, R1509, R1510, R1511, R1512, R1513, R1514, R1515, R1516, R1517, R1518, R1519, R1520, R1521, R1522, R1523, R1524, R1525, R1526, R1527, R1528, R1529, R1530, R1531, R1532, R1533, R1534, R1535, R1536, R1537, R1538, R1539, R1540, R1541, R1542, R1543, R1544, R1545, R1546, R1547, R1548, R1549, R1550, R1551, R1552, R1553, R1554, R1555, R1556, R1557, R1558, R1559, R1560, R1561, R1562, R1563, R1564, R1565, R1566, R1567, R1568, R1569, R1570, R1571, R1572, R1573, R1574, R1575, R1576, R1577, R1578, R1579, R1580, R1581, R1582, R1583, R1584, R1585, R1586, R1587, R1588, R1589, R1590, R1591, R1592, R1593, R1594, R1595, R1596, R1597, R1598, R1599, R1600, R1601, R1602, R1603, R1604, R1605, R1606, R1607, R1608, R1609, R1610, R1611, R1612, R1613, R1614, R1615, R1616, R1617, R1618, R1619, R1620, R

d:/users/desk40/mentor/son/FIRENZE/MP1.0

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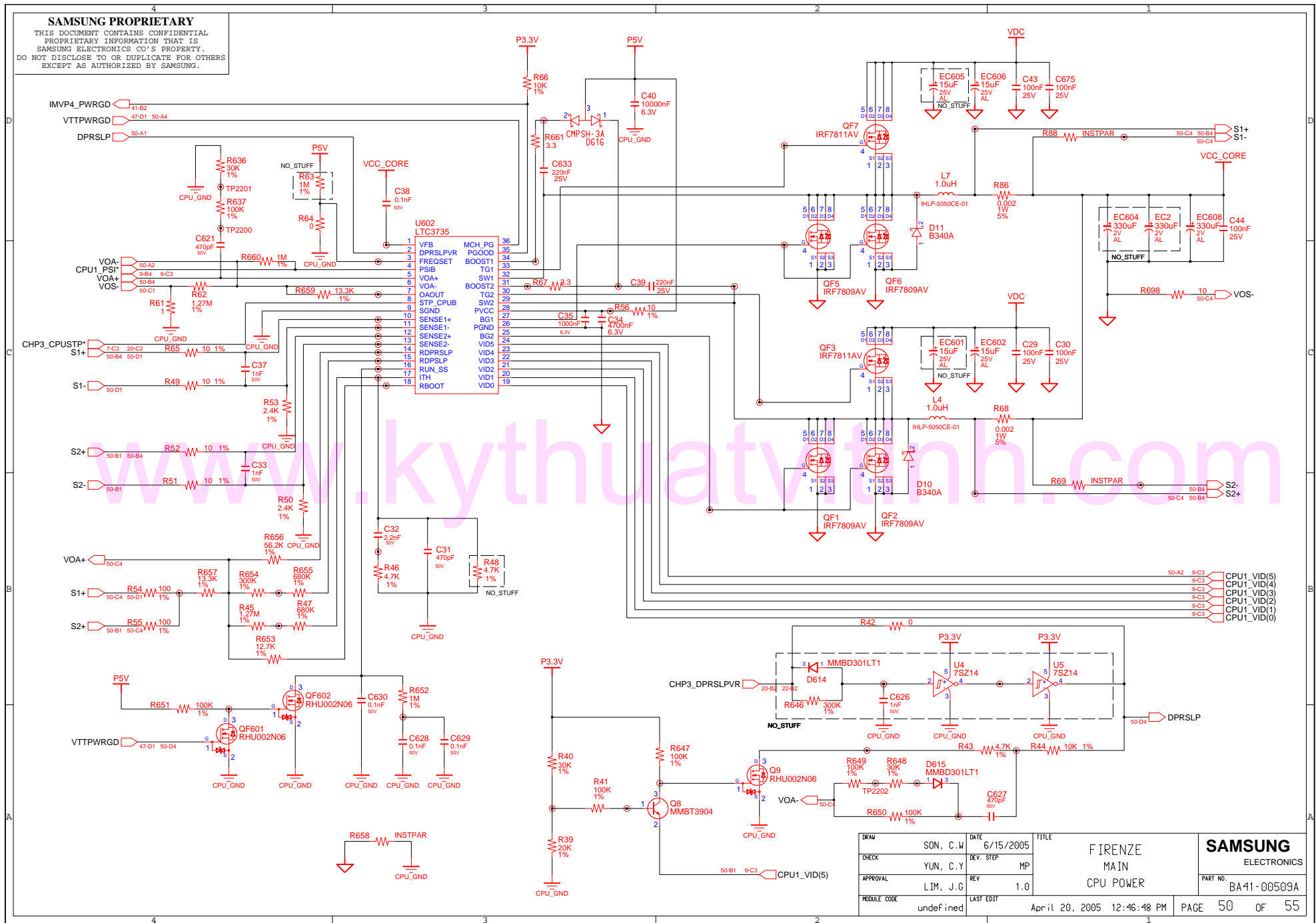
Graphic Core Power



DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN GRAPHIC CORE POWER	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			PART NO. BA41-00509A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	49	OF 55

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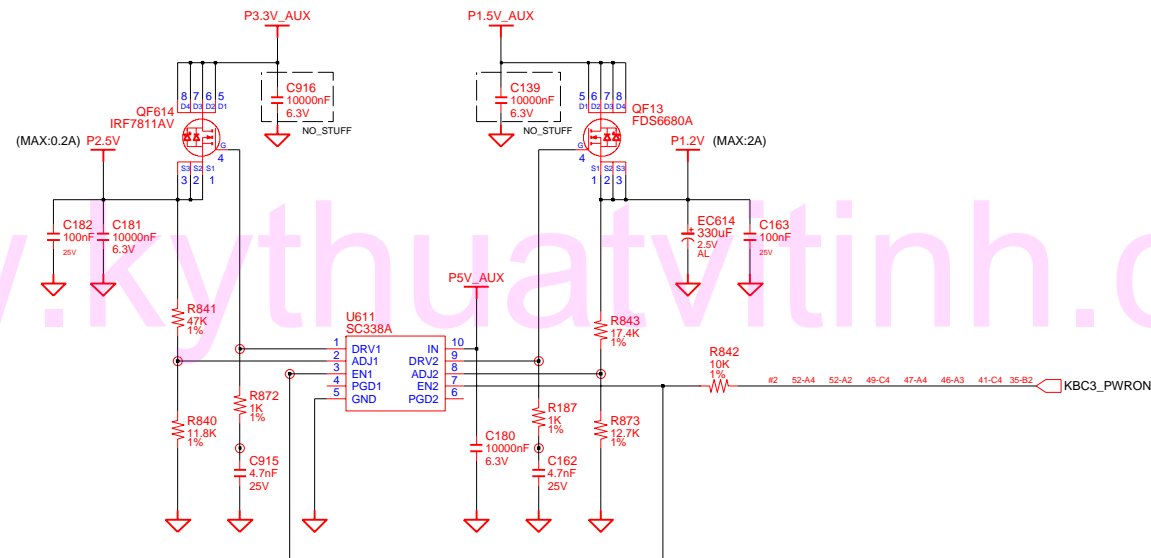


DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN CPU POWER	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			PART NO. BA41-00509A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	50	OF 55

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P1.2V / P2.5V POWER

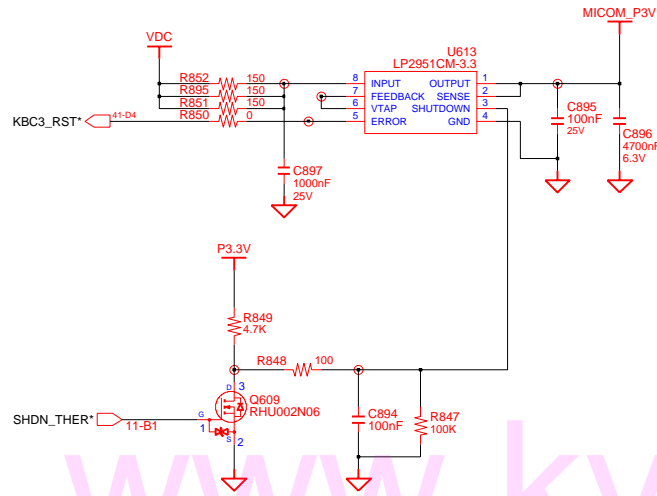


DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			PART NO. BA41-00509A
APPROVAL	LIM, J.G	REV	1.0		1.2V/2.5V POWER	
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	51	OF 55

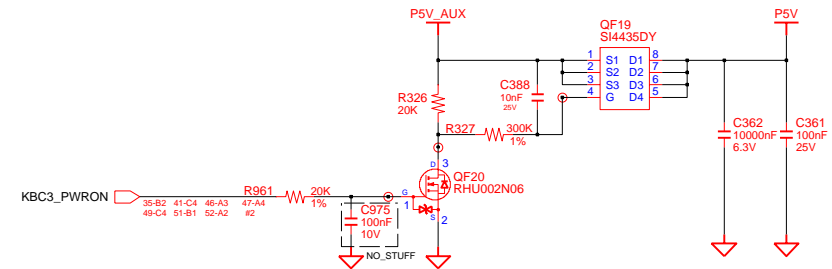
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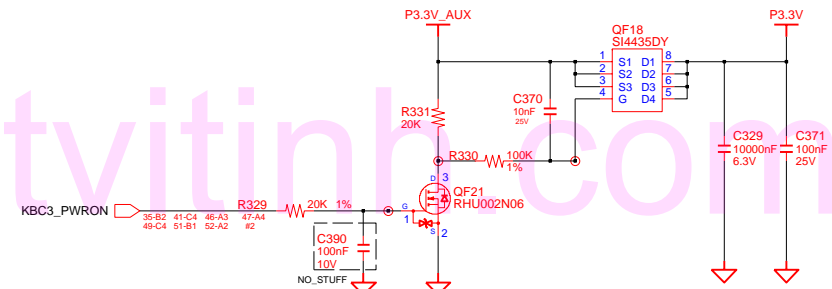
MICOM_P3V Power



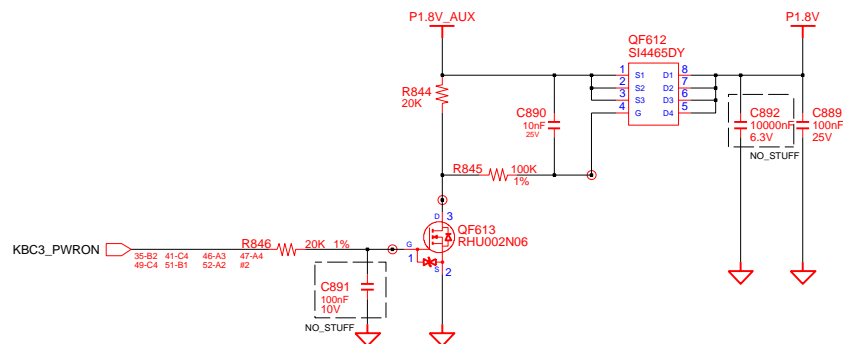
Switched Power On (P5V)



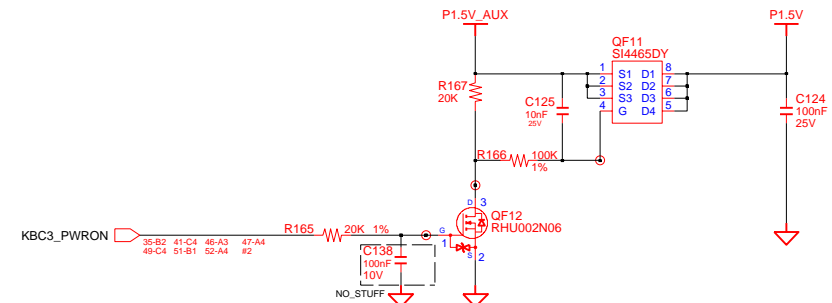
Switched Power On (P3.3V)



Switched Power On (P1.8V)



Switched Power On (P1.5V)

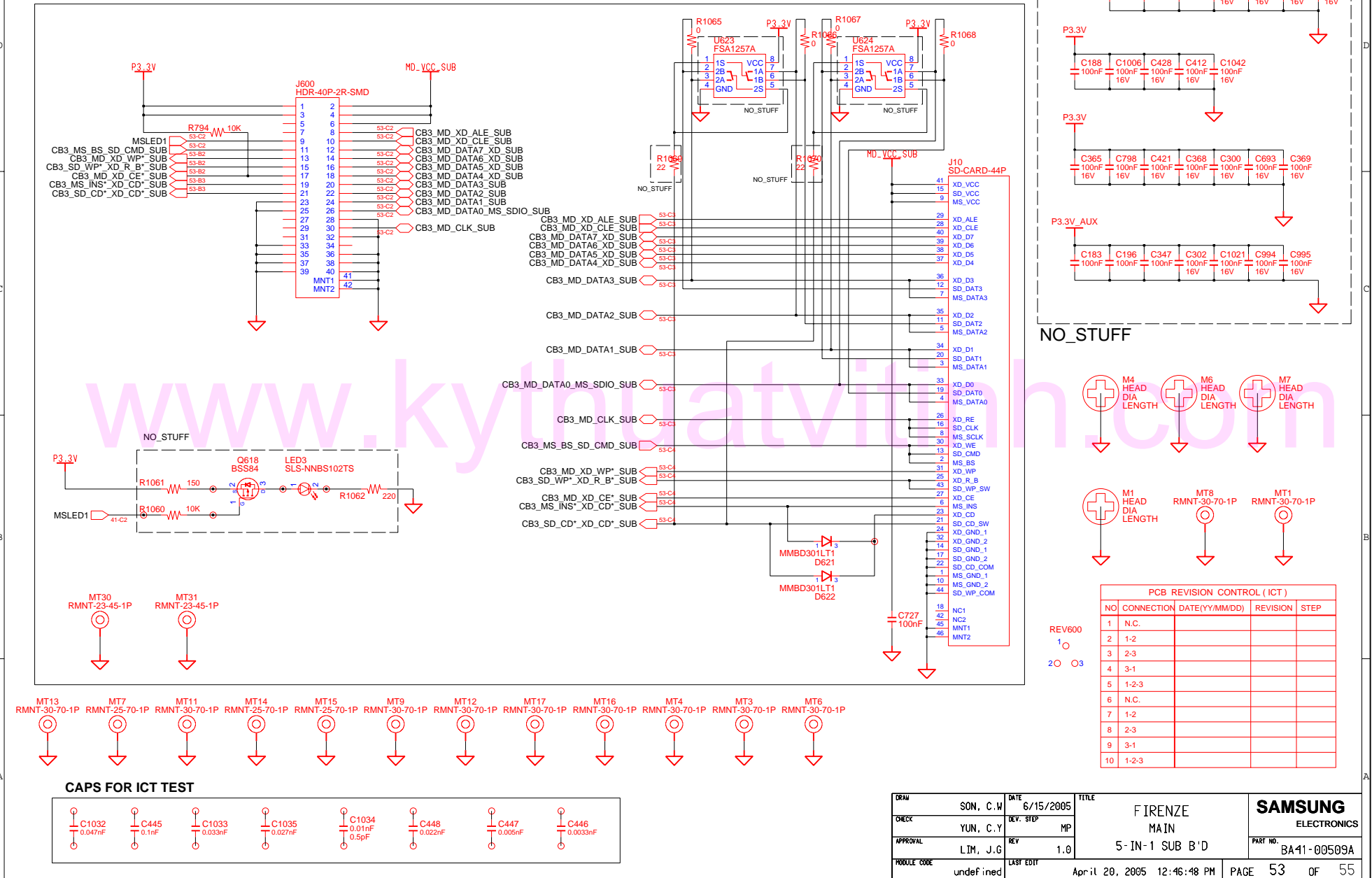


DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			PART NO. BA41-00509A
APPROVAL	LIM, J.G	REV	1.0		MICOM&SWITCHED POWER	
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	52	OF 55

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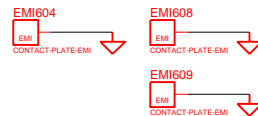
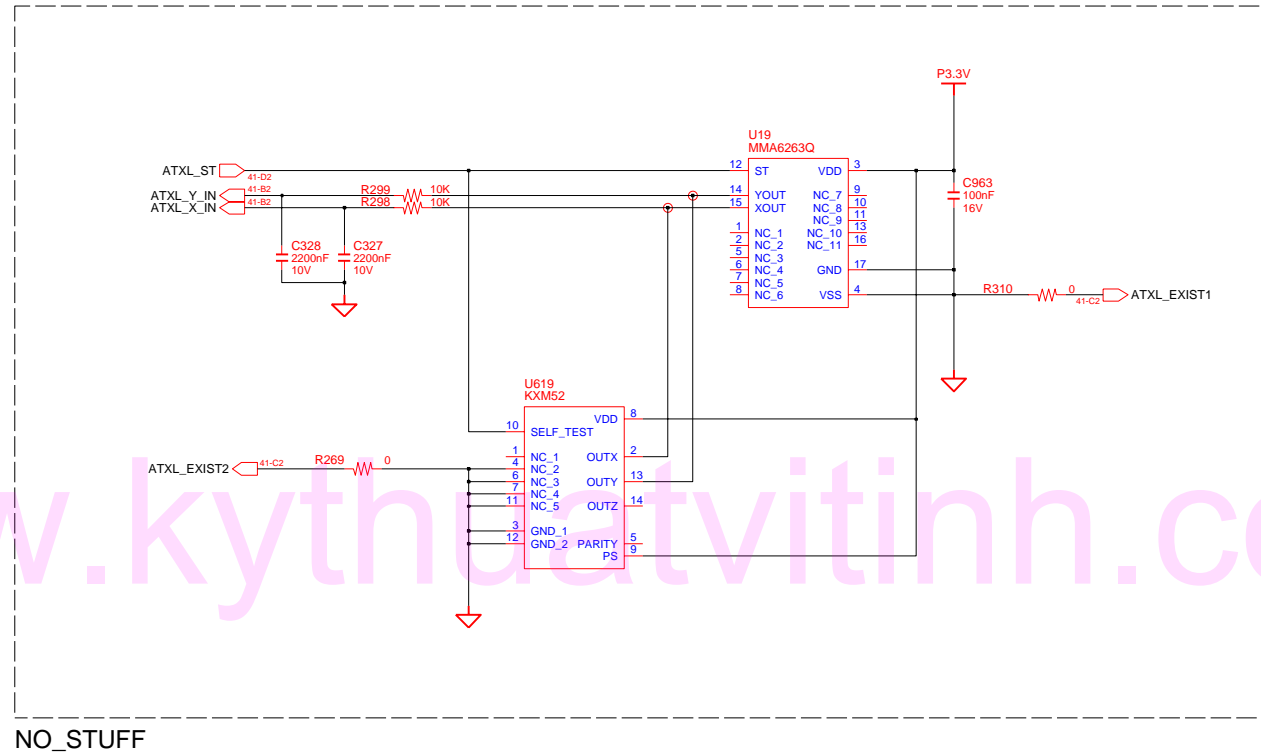
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5-IN-1 SUB B'D

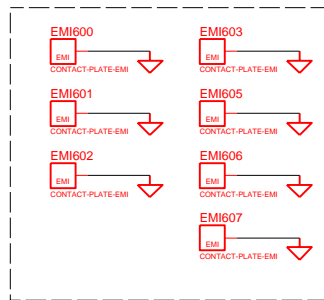


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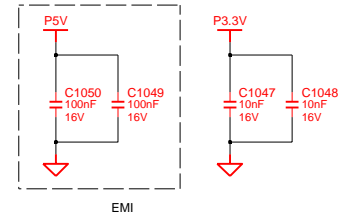
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NO_STUFF



NO_STUFF



DRAW	SON, C.W	DATE	6/15/2005	TITLE	FIRENZE MAIN AIR BAG	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	MP			PART NO. BA41-00509A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April 20, 2005 12:46:48 PM	PAGE	54	OF 55

