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OSLO2

CPU : Intel Penryn-6M (1067/800) MHz
 Chip Set : Intel Cantiga & ICH9M
 Remarks : Montevina Platform

Model Name : Oslo2_DDR3
 PBA Name : MAIN
 PCB Code : BA41-00866A
 BA41-00867A
 Dev. Step : MP
 Revision : 1.1
 T.R. Date : 2008. 05.15

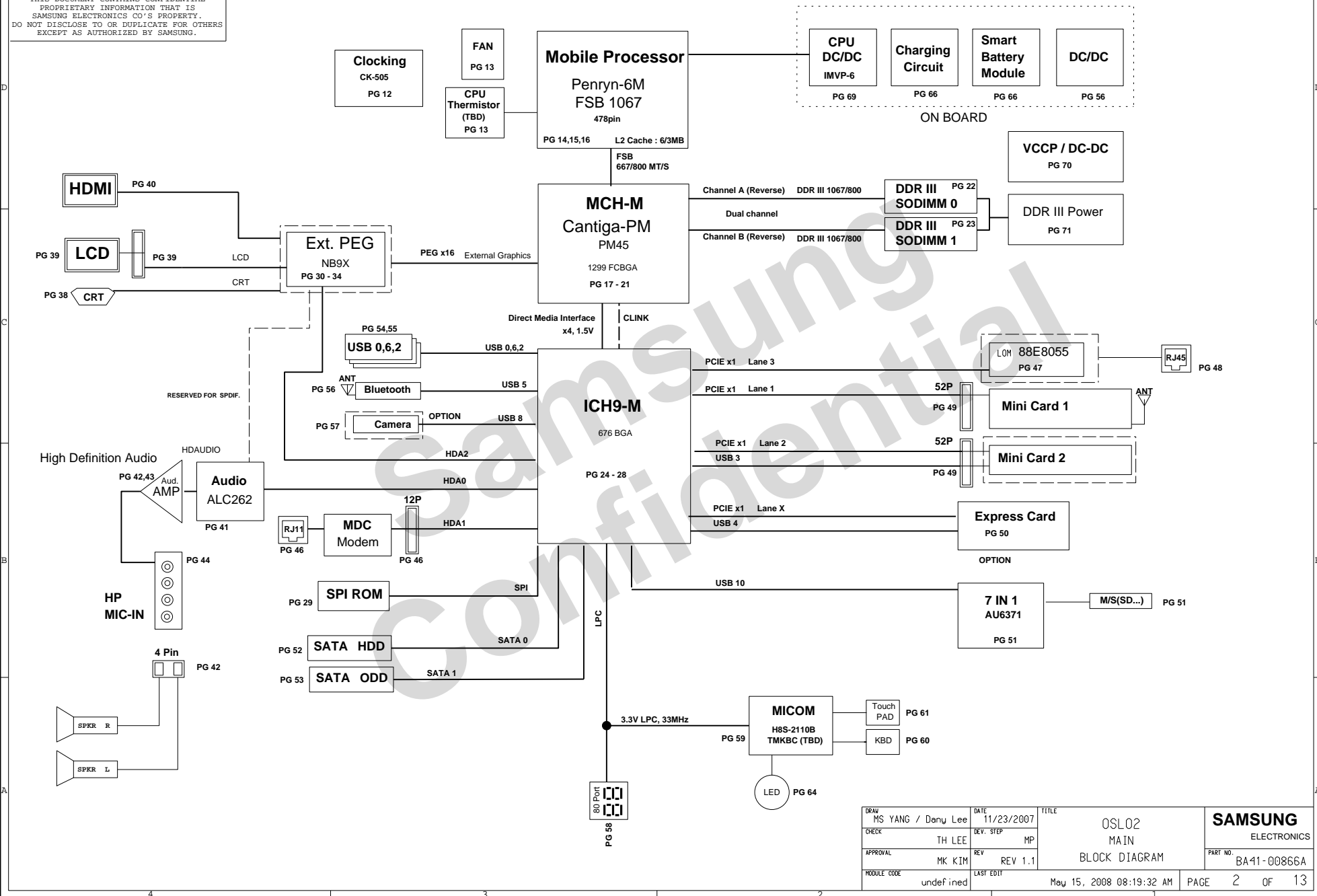
DRAW	CHECK	APPROVAL
MS YANG TH LEE	TH LEE	MK KIM

■ Owner : SEC Mobile R & D Signature : X

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 Sheet 71. PWR_MV_Memory
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DRAW MS YANG / Dany Lee	DATE 11/23/2007	TITLE OSLO2 MAIN COVER	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP		PART NO. BA41-00866A
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT May 15, 2008 08:19:32 AM	PAGE 1 OF 13	

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DRAW MS YANG / Dany Lee	DATE 11/23/2007	TITLE OSLO2 MAIN BLOCK DIAGRAM	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP		
APPROVAL MK KIM	REV REV 1.1		
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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Marvell LAN (88E8850)
Crystal	12MHz	Multi Card Reader	Alkor AU6371

LCD Pannel Detect (EDID)

Devices	Resolution	PANNEL_DETECT_0
---------	------------	-----------------

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
GFX_CORE	Core Voltage for GPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH9-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail for DDR (off in S4-S5)
P0.75V	0.75V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9-m	Master	-	SMBUS Master
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
MICOM	Master	-	SMBUS Master
Battery	0001011x	16h	Battery
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor (EMC2012)

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 2
1	NC
2	SYSTEM PORT 1
3	Mini Card
4	Express Card
5	Bluetooth
6	SYSTEM PORT 2
7	NC
8	Camera
9	NC
10	Multi Card Reader (7-in-1)
11	NC

PCI Express Assign

PORT #	ASSIGNED TO
1	Mini Card 1 (WLAN)
2	Mini Card 2 (ROBSON or DVB-T)
3	Express Card
4	LOM
5	NC
6	NC

REVISION HISTORY

See rev notes for more information.

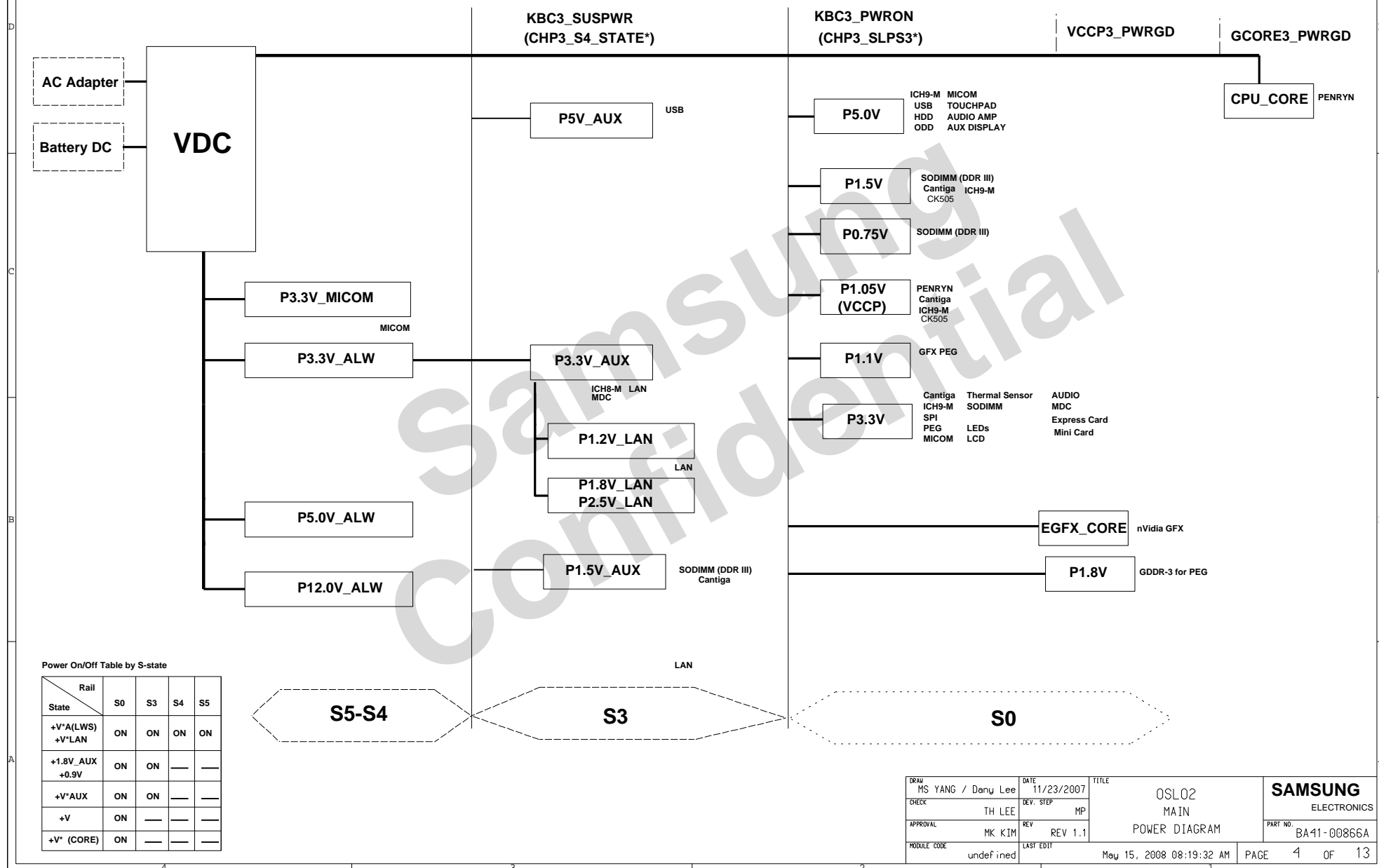
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CHECK TH LEE	DEV. STEP MP	REV REV 1.1	
APPROVAL MK KIM	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 3 OF 13
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POWER DIAGRAM

Rev 0.1

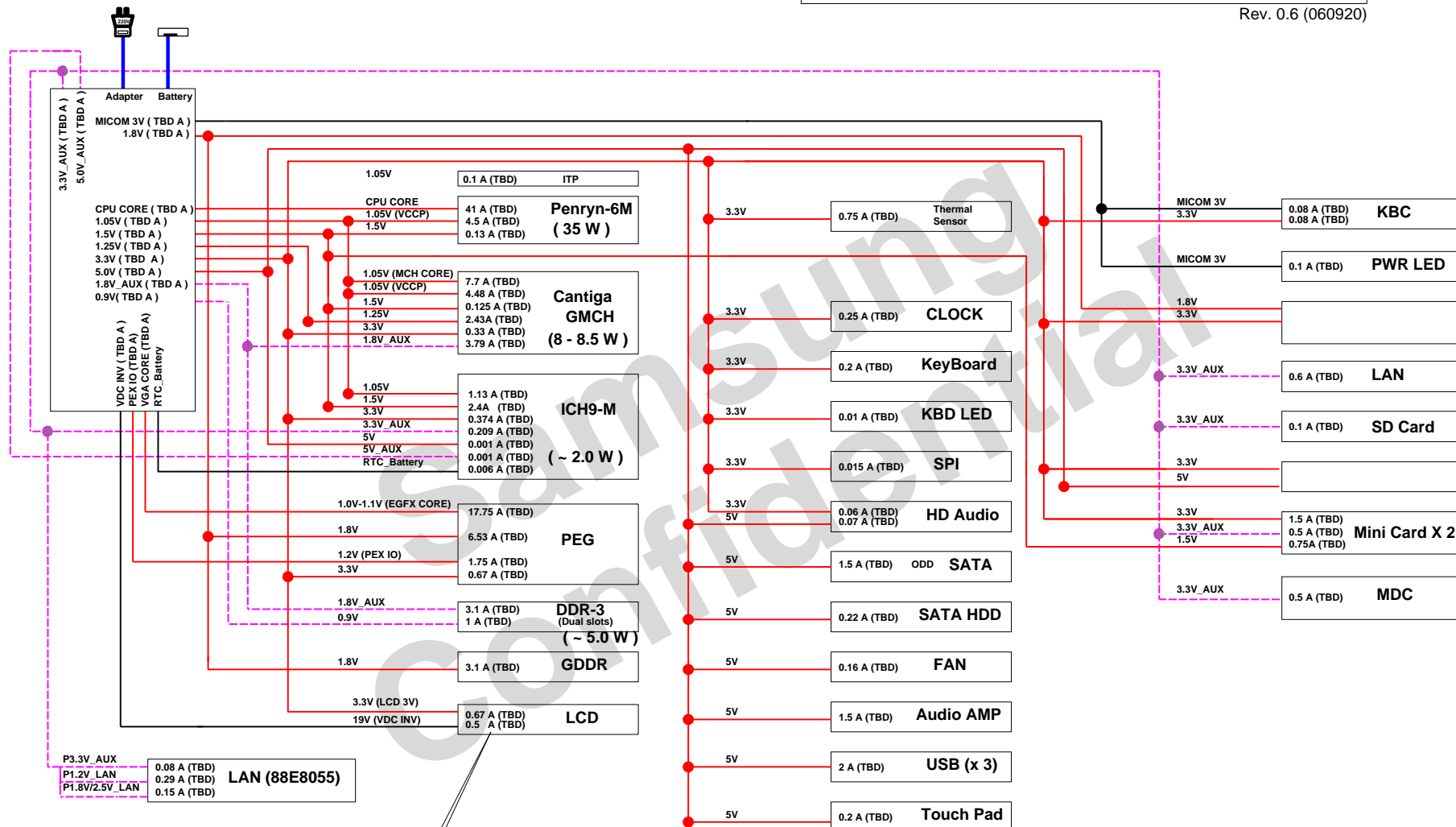


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POWER RAILS ANALYSIS

Rev. 0.6 (060920)



Value by Datasheet/Application notes (Value by measurement)

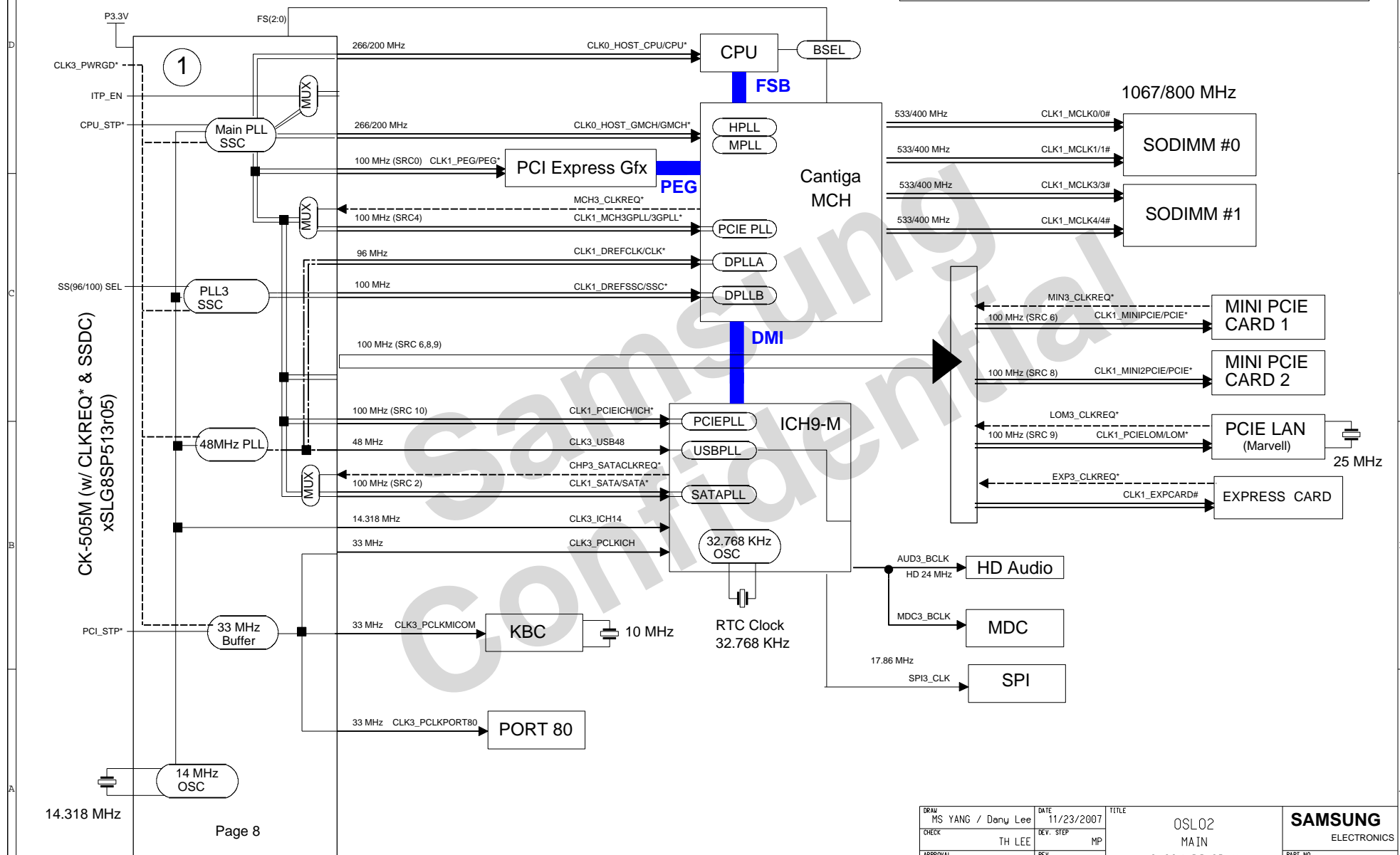
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MODULE CODE	undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	5	OF 13

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CLOCK DISTRIBUTION

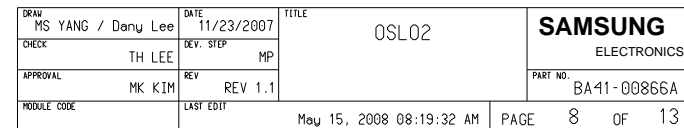
Rev. 0.1



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DRAW MS YANG / Dany Lee	DATE 11/23/2007	TITLE OSL02 MAIN CLOCK DIAGRAM	SAMSUNG ELECTRONICS
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APPROVAL MK KIM	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 7 OF 13
MODULE CODE undefined			

A



Express_card

84
#1

Multi_MV_Au6372

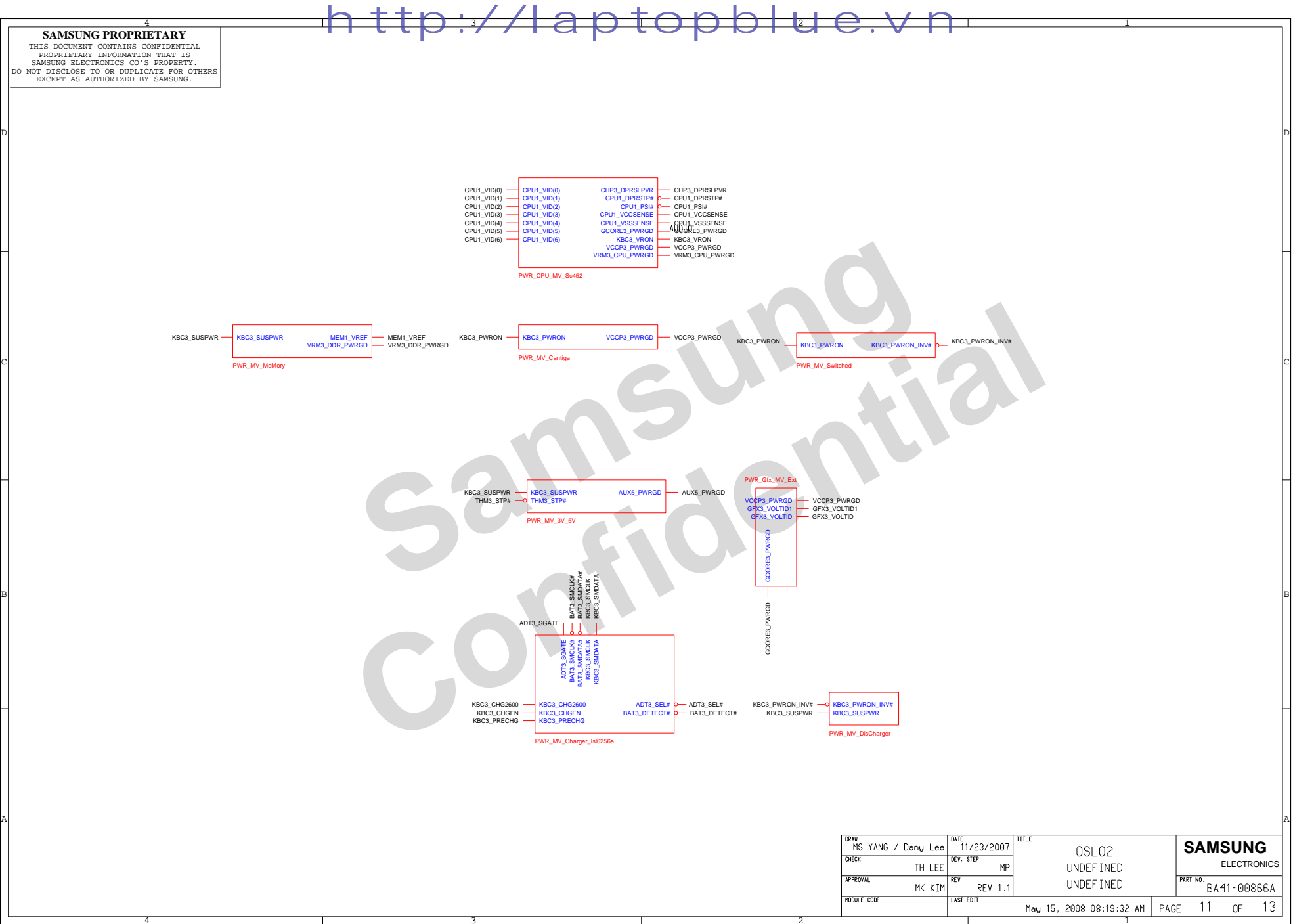
MICOM_Renesas2110_100p

SPI BIOS_ROM

Other_Debug_80

ICH_9M_B

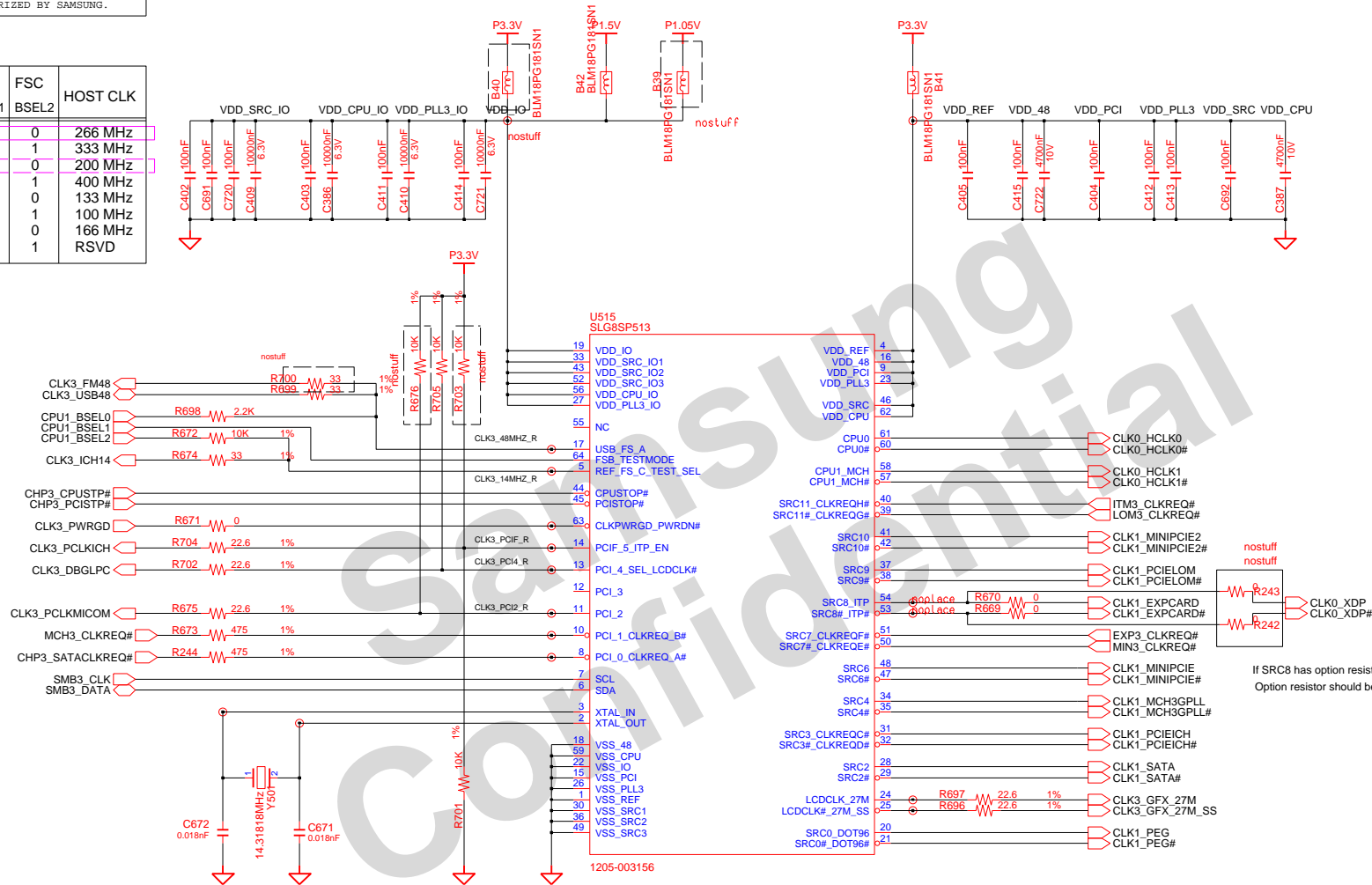
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CHECK TH LEE		REV: STEP MP					
APPROVAL MK KIM		REV REV 1.1					
MODULE CODE		LAST EDIT		May 15, 2008 08:19:32 AM		PAGE 9 OF 13	



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FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATACLKREQ#	SRC2
CLK REQ B	MCH3_CLKREQ#	SRC4
CLK REQ E	MIN3_CLKREQ#	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8
CLK REQ G	LOM3_CLKREQ#	SRC9

SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

Place 14.318MHz within
 500mils of CK-505

2nd source IDT, 1205-003159

This part is 64pin QFN package.

DRAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSLO2	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP		Main_Clock_Circuit	
APPROVAL	MK KIM	REV	1.1		CK_Clock_505M	PART NO. BA11-00866A
MODULE CODE	undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	1	OF 1

The schematic diagram illustrates the connection of the CPU to the board. The CPU pinout is shown on the left, with pins 1 through 29. The board components are shown on the right, including the CPU pin connections, the CPU pinout, and the board components. The diagram includes the CPU pinout, board components, and a detailed view of the CPU pin connections.

Pin Connections:

- Pin 1:** FAN_MODE
- Pin 2:** FAN_1
- Pin 3:** FAN_2
- Pin 4:** TACH
- Pin 5:** THERMTRIP#
- Pin 6:** SHDN_SEL
- Pin 7:** TRIP_SET
- Pin 8:** CLK_SEL
- Pin 9:** CLK_IN
- Pin 10:** NC_1
- Pin 11:** NC_2
- Pin 12:** NC_3
- Pin 13:** GND
- Pin 14:** THRM_PAD
- Pin 15:** SMDATA
- Pin 16:** SMCLK
- Pin 17:** ALERT#
- Pin 18:** SYS_SHDN#
- Pin 19:** DN1
- Pin 20:** DP1
- Pin 21:** DN2
- Pin 22:** DP2
- Pin 23:** DN3
- Pin 24:** DP3
- Pin 25:** KBC3_THERM_SMDATA
- Pin 26:** KBC3_THERM_SMCLK
- Pin 27:** THM3_ALERT#
- Pin 28:** THM3_STP#
- Pin 29:** CPU2_THERMDC
- Pin 30:** CPU2_THERMDA
- Pin 31:** GFX3_THERMDN
- Pin 32:** GFX3_THERMDP

Board Components:

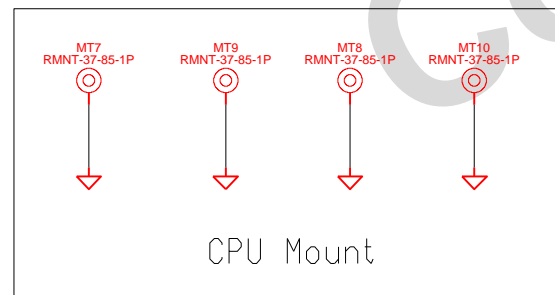
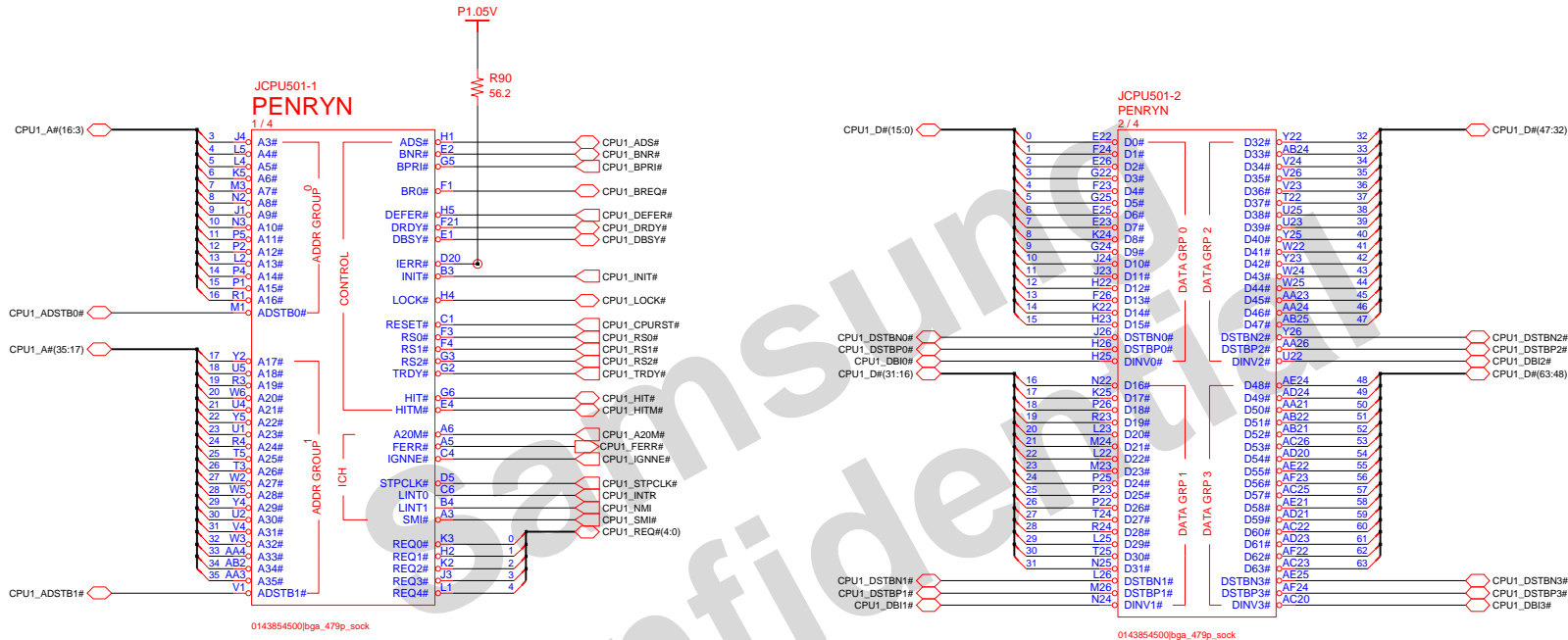
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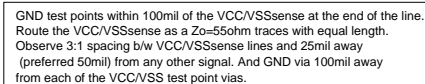
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479P CPU socket is 3704-001153



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CHECK	TH LEE	DEV. STEP	MP		CPU	
APPROVAL	MK KIM	REV	REV 1.1		PENRYN (1/3)	PART NO.
MODULE CODE	undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	1	BA11-00866A
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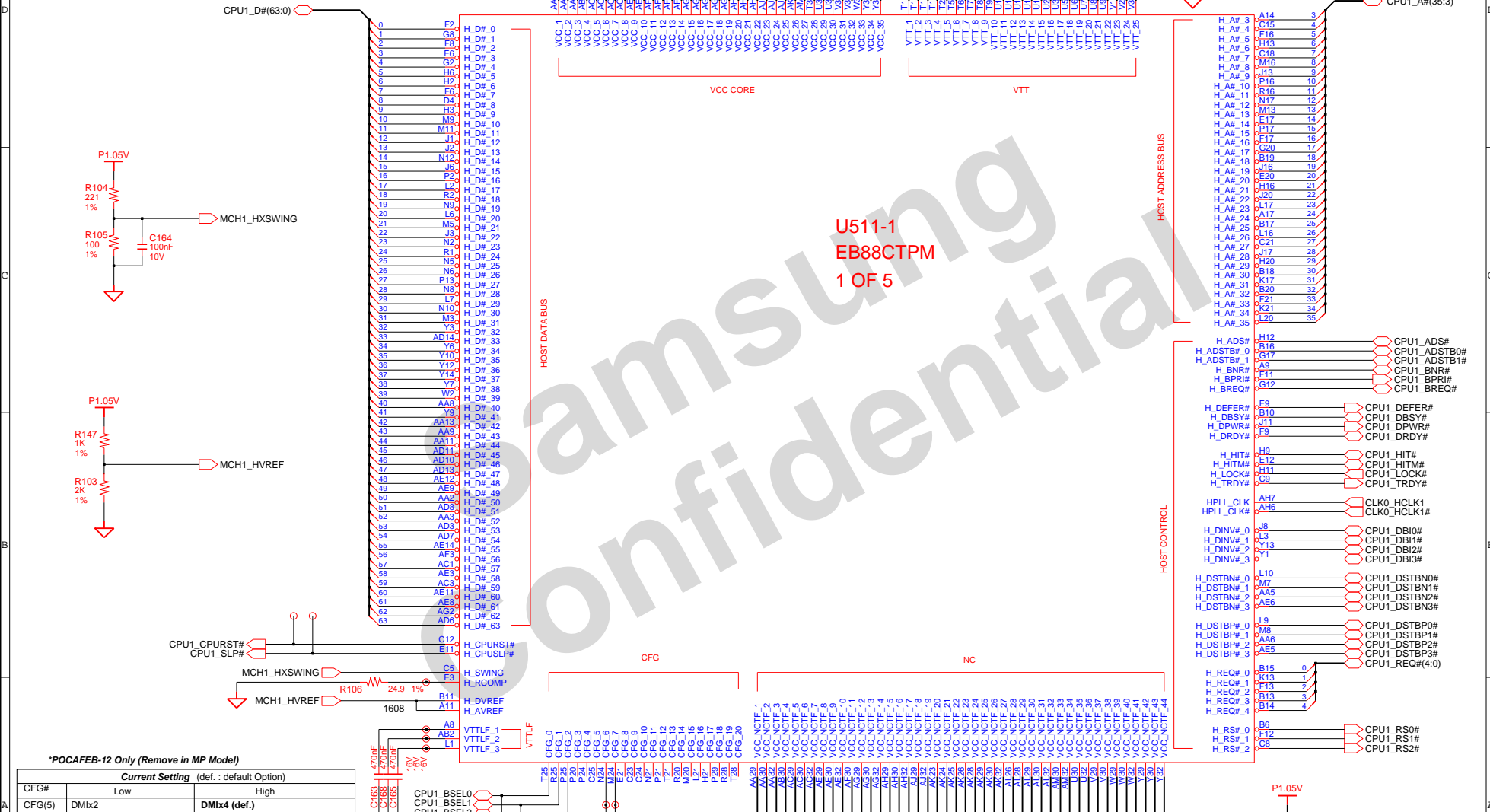


	Pull-up	Pull-down
FSB 1067 MHz FSB 800 MHz	BSEL1	BSEL0, BSEL1, BSEL2 BSEL0, BSEL2

SRP Sheet Number: 15 of 76

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*POCAFEB-12 Only (Remove in MP Model)

CFG#	Low	High
CFG(5)	DMIx2	DMIx4 (def.)
CFG(6)	ITPM Host Interface Enable	ITPM Host Interface Disable (def.)
CFG(7)	ME Crypto no confidentiality	ME Crypto confidentiality (def.)
CFG(9)	PEG Reversal (def.)	Normal
CFG(10)	PCIe Loop Back Enable	PCIe Loop Back Disable(def)
CFG(16)	Dynamic ODT Disabled	Dynamic ODT Enabled (def.)
CFG(19)	DMI Lane Normal (def.)	DMI Lane Reversal
CFG(20)	SDVO or PCIe X1 Only(def.)	SDVO and PCIe X1 Simultaneously

DRAW MS YANG / Dany Lee CHECK TH LEE APPROVAL MK KIM MODULE CODE undefined	DATE 11/8/2006 DEV. STEP MP REV REV 1.1 LAST EDIT	TITLE OSLO2 MCH_CANTIGA_PM_DDR3 CANTIGA (1/5)	SAMSUNG ELECTRONICS PART NO. BA11-00866A
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NC FOR DDR2 BD??

U511-4
88CTPM
4 OF 5

ORAM	MS YANG / Dany Lee	DATE	11/8/2006	TITLE OSLO2 MCH_CANTIGA_PM_DDR3 CANTIGA (4/5)	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP		
APPROVAL	MK KIM	REV	REV 1.1		
MODULE CODE		LAST EDIT			
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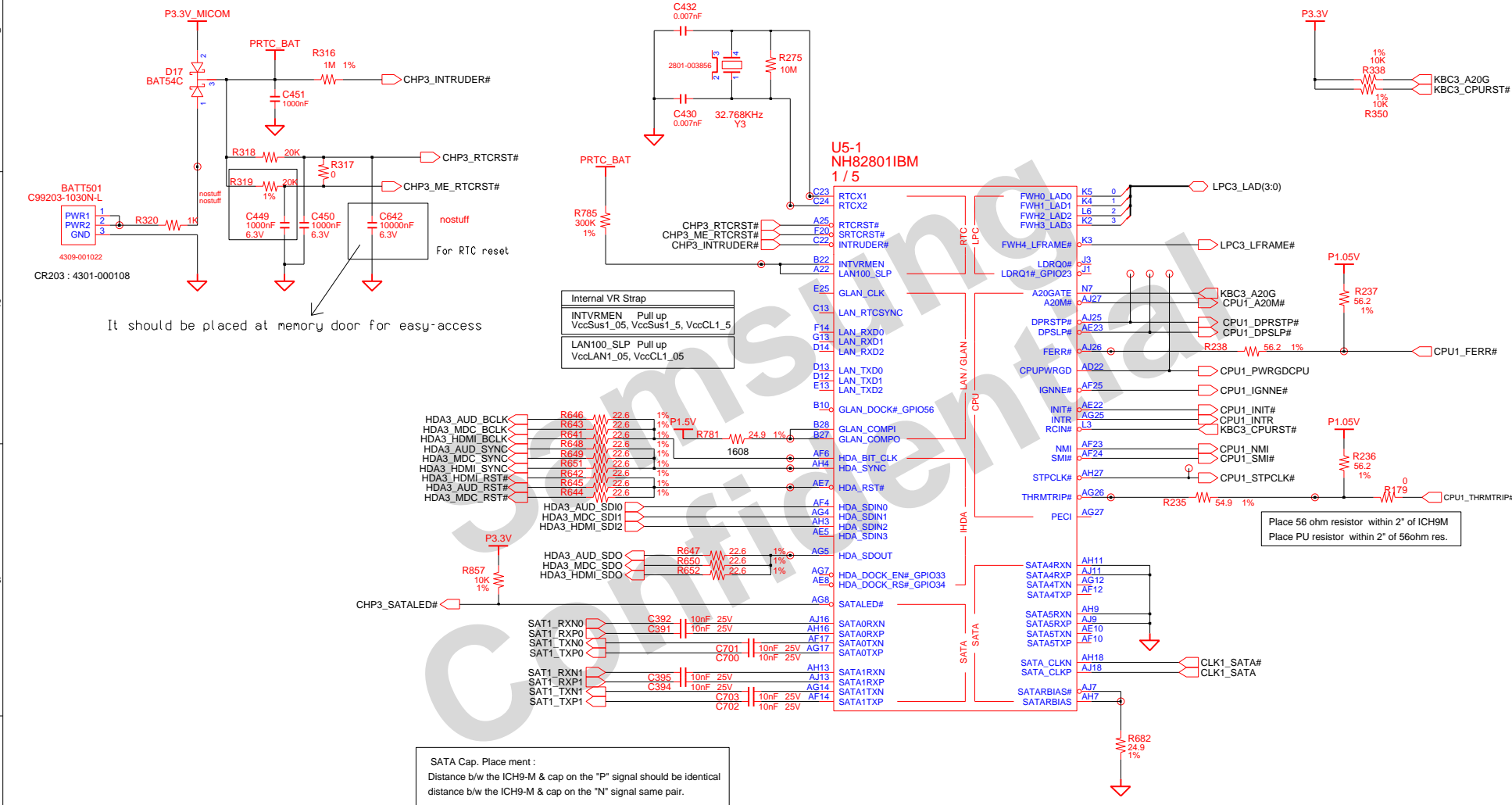
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SRP Sheet Number: 21 of 76

Height : 9.2mm (Reverse)



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DRAW	MS YANG / Dany Lee	DATE	11/8/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP		ICH_9M_B	
APPROVAL	MK KIM	REV	1.1		ICH9-M (1/5)	PART NO. BA11-00866A
MODULE CODE		LAST EDIT				

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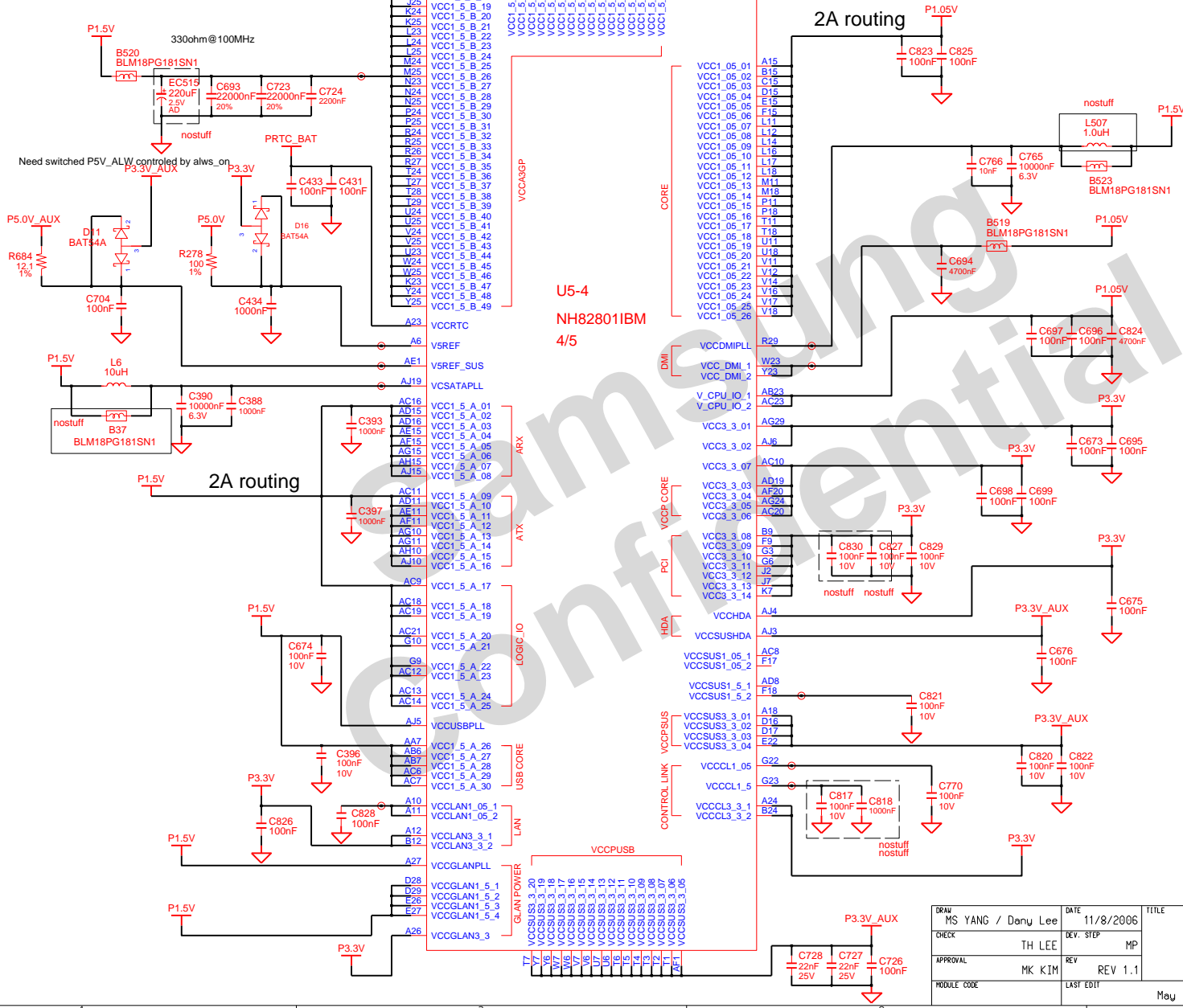
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DRAW	MS YANG / Dany Lee	DATE	11/8/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	REV. STEP	MP		ICH9_M.B	
APPROVAL	MK KIM	REV	1.1		ICH9-M (3/5)	PART NO. BA11-00866A
MODULE CODE		LAST EDIT				

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AA26	VSS_001	VSS_106	N14
AA27	VSS_002	VSS_107	N15
AA3	VSS_003	VSS_108	N16
AA4	VSS_004	VSS_109	N17
AB1	VSS_005	VSS_110	N18
AA23	VSS_006	VSS_111	N26
AB28	VSS_007	VSS_112	N27
AB4	VSS_008	VSS_113	P12
AB5	VSS_009	VSS_114	P13
AC17	VSS_010	VSS_115	P14
AC26	VSS_011	VSS_116	P15
AC3	VSS_012	VSS_117	P16
AD1	VSS_013	VSS_118	P17
AD10	VSS_014	VSS_119	P23
AD12	VSS_015	VSS_120	P28
AD13	VSS_016	VSS_121	P4
AD14	VSS_017	VSS_122	P7
AD17	VSS_018	VSS_123	R11
AD18	VSS_019	VSS_124	R12
AD21	VSS_020	VSS_125	R13
AD28	VSS_021	VSS_126	R14
AD29	VSS_022	VSS_127	R15
AD4	VSS_023	VSS_128	R16
AD5	VSS_024	VSS_129	R18
AD6	VSS_025	VSS_130	R28
AD7	VSS_026	VSS_131	T12
AE12	VSS_027	VSS_132	T13
AE13	VSS_028	VSS_133	T14
AE14	VSS_029	VSS_134	T15
AE16	VSS_030	VSS_135	T16
AE17	VSS_031	VSS_136	T17
AE2	VSS_032	VSS_137	T23
AE20	VSS_033	VSS_138	B26
AE24	VSS_034	VSS_139	U12
AE3	VSS_035	VSS_140	U13
AE4	VSS_036	VSS_141	U14
AE6	VSS_037	VSS_142	U15
AE9	VSS_038	VSS_143	U16
AF13	VSS_039	VSS_144	U17
AF16	VSS_040	VSS_145	AD23
AF18	VSS_041	VSS_146	U26
AF22	VSS_042	VSS_147	U27
AF26	VSS_043	VSS_148	U3
AF27	VSS_044	VSS_149	V13
AF5	VSS_045	VSS_150	V15
AF7	VSS_046	VSS_151	V23
AF9	VSS_047	VSS_152	V28
AG13	VSS_048	VSS_153	V29
AG16	VSS_049	VSS_154	V4
AG18	VSS_050	VSS_155	V5
AG20	VSS_051	VSS_156	W26
AG23	VSS_052	VSS_157	W27
AG3	VSS_053	VSS_158	W3
AG6	VSS_054	VSS_159	Y1
AG9	VSS_055	VSS_160	Y28
AH12	VSS_056	VSS_161	Y29
AH14	VSS_057	VSS_162	Y4
AH17	VSS_058	VSS_163	Y5
AH2	VSS_059	VSS_164	AG28
AH22	VSS_060	VSS_165	AH6
AH25	VSS_061	VSS_166	AF2
AH28	VSS_062	VSS_167	B25
AH5	VSS_063	VSS_168	A1
AH8	VSS_064	VSS_169	A2
AJ12	VSS_065	VSS_170	A28
AJ14	VSS_066	VSS_171	A29
AJ17	VSS_067	VSS_172	AH1
AJ8	VSS_068	VSS_173	AH29
B11	VSS_069	VSS_174	AJ1
B14	VSS_070	VSS_175	AJ2
B17	VSS_071	VSS_176	AJ28
B2	VSS_072	VSS_177	AJ29
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	VSS_365	VSS_470	
	VSS_366	VSS_471	

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- SPI ROM LIST (8M)-

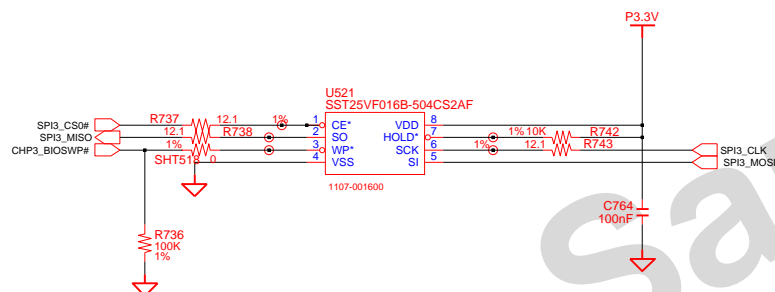
Macronix - MX25L8005M2C-15G
-> 1107-001646

STM - M25PE80
-> 1107-001674

- SPI ROM LIST (16M)-

Macronix - MX25L1605A
-> 1107-001600

SST - SST25VF016B
-> 1107-001600

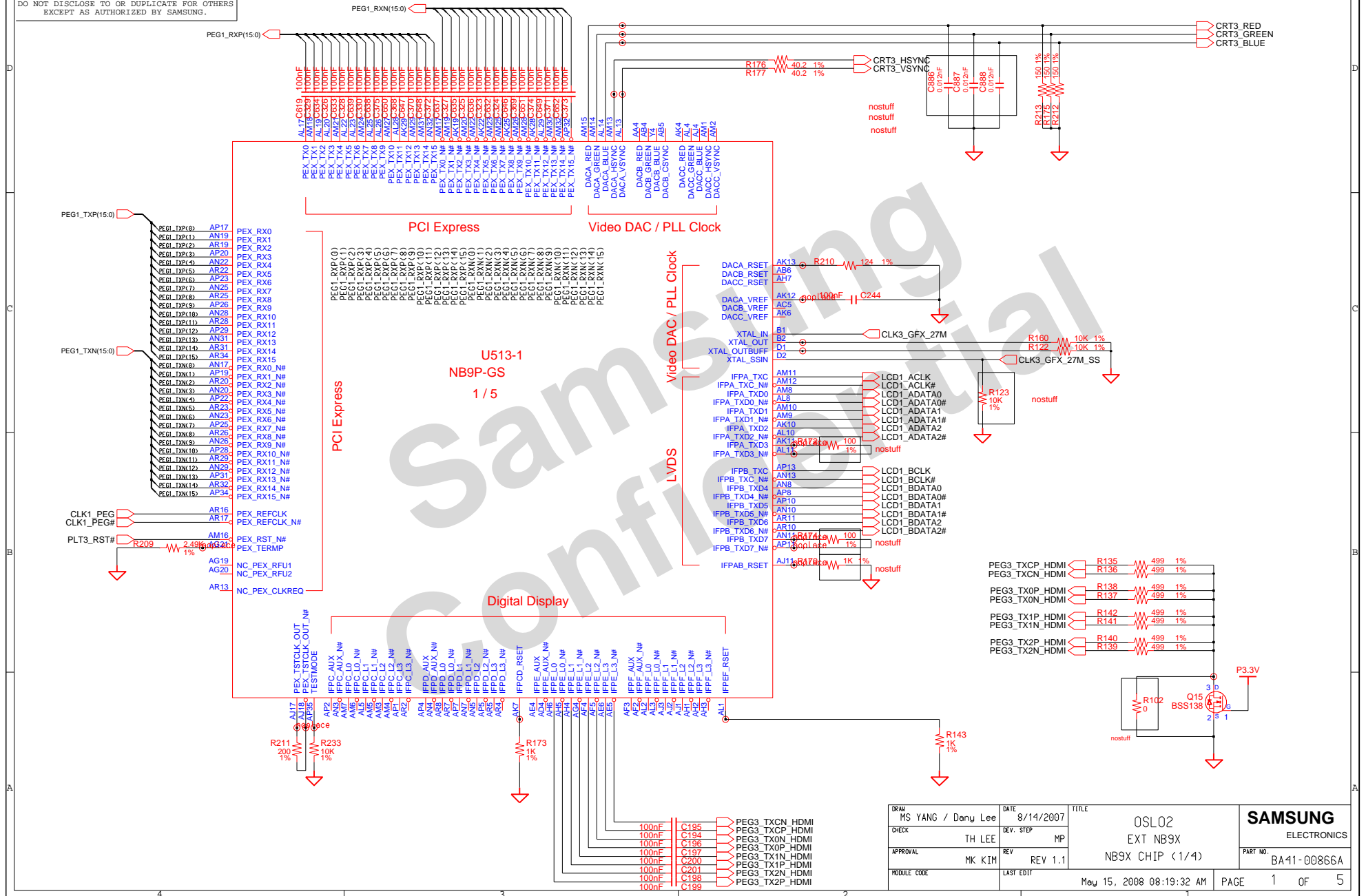


02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD EERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
OE	INIT. I/O VALUE	7E	TEST COPROCESSOR IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
	WITH INITIAL POST VALUE	88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT.EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT.	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUPT CONTROLLER	9E	ENABLE H/W INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPOMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TESET CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
42	INIT. INTERRUPT VECTOR	BA	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DA	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DC	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	89	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY "PRESS SETUP"	92	JUMP TO USER PATCH 2
5C	TEST RAM BETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS PART NO. BA41-00866A
CHECK TH LEE	DEV. STEP MP	SPI_BIOS_ROM	
APPROVAL MK KIM	REV REV 1.1	SPI_BIOS_ROM	
MODULE CODE	LAST EDIT		
May 15, 2008 08:19:32 AM			PAGE 1 OF 1

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DRAW	MS YANG / Dany Lee	DATE	8/14/2007	TITLE	OSL02 EXT NB9X NB9X CHIP (1/4)	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK	TH LEE	REV. STEP	MP			
APPROVAL	MK KIM	REV	REV 1.1			
MODULE CODE		LAST EDIT				

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PAGE 1 OF 5

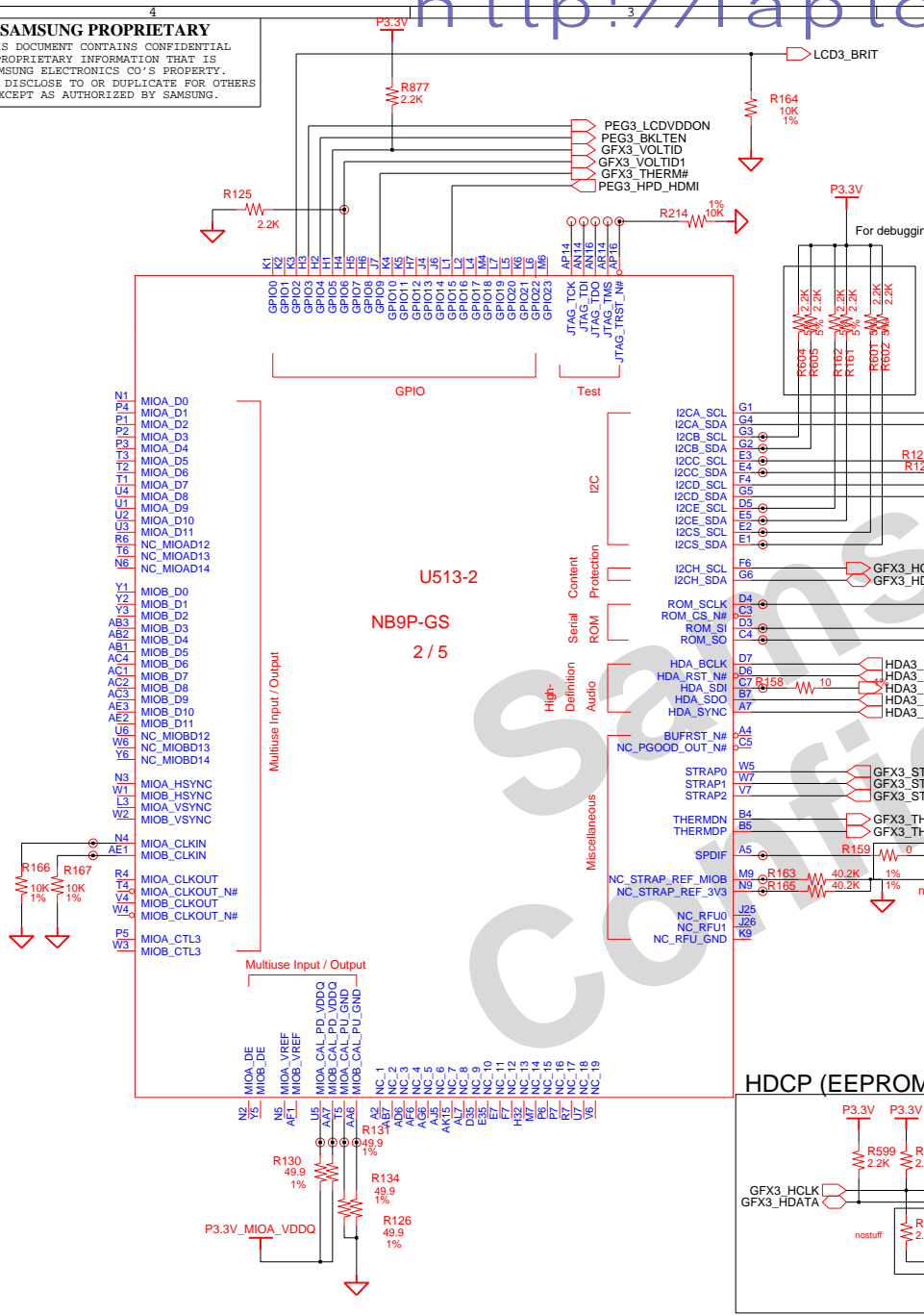
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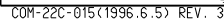
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Pin	Description	Activate
GPIO(0)	DVI detect	High
GPIO(1)	TV detect	Low
GPIO(2)	PWM Brightness control	High
GPIO(3)	LCD VDD on enable	High
GPIO(4)	Backlight on/off	High
GPIO(5)	GPU VDD	00 = 0.89V, 01 = 1.0V
GPIO(6)	GPU VID1	10 = 1.05V, 11 = Reserved
GPIO(7)	GPU VID2 or Mem VID	NC
GPIO(8)	Thermal diode Alert	LOW
GPIO(9)	Fan control	NC
GPIO(10)	Memory VREF switch	NC
GPIO(11)	SU Rater sync	HIGH
GPIO(12)	AC Power dection input	NC
GPIO(13)	Power supply control	NC
GPIO(14)	Power supply control	NC
GPIO(15)	HDMI Detect	High
GPIO(16)	DP Detect	High

Strap option	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_27	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	DEVID[4]	VENID	CLK_CFG	PLL_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	DEVID[3]	DEVID[2]	DEVID[1]	DEVID[0]
STRAP1	PADCFG[3]	PADCFG[2]	PADCFG[1]	PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

Resistor value	PU to VDD	PD to GND	XCLK27 = 1.27MHz
5K ohm	1000	0000	RAM CFG (SEC)
10 Kohm	1001	0001	0011 512Mbit 0111 1Gbit
15K ohm	1010	0010	USER[3:0]=1111 for EDID
20K ohm	1011	0011	PADCFG[3:0]=0001 of NP
25K ohm	1100	0100	NB9M-GS:0x06E9 (01001)
30K ohm	1101	0101	NB9M-GS:0x06E8 (01000)
35K ohm	1110	0110	NB9P-GS:0x0406 (00110)
45K ohm	1111	0111	NB9P-GS:0x0649 (01001)
			NB9P-GS:0x0648 (01000)

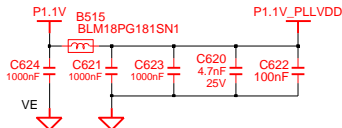




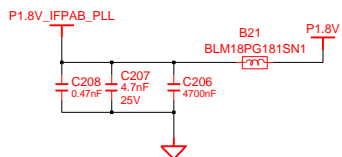
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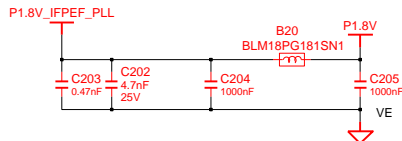
PLL_VDD



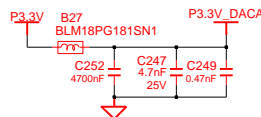
IFPAB_PLLVDD



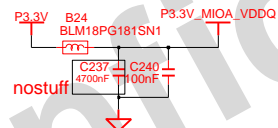
IFPEF_PLLVDD



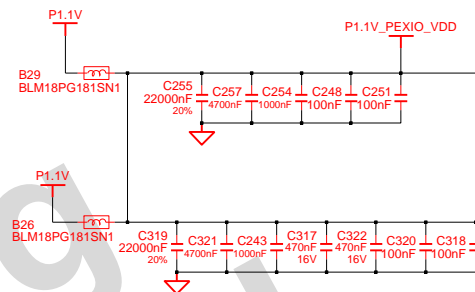
DACA/B/C



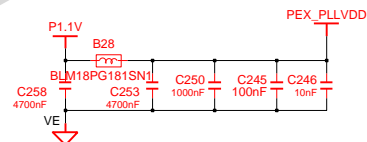
MIOA/B_VDDQ



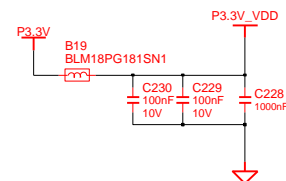
PEX_IOVDD (w PEX_IOVDDQ)



PEX_PLL_VDD



3.3V_VDD

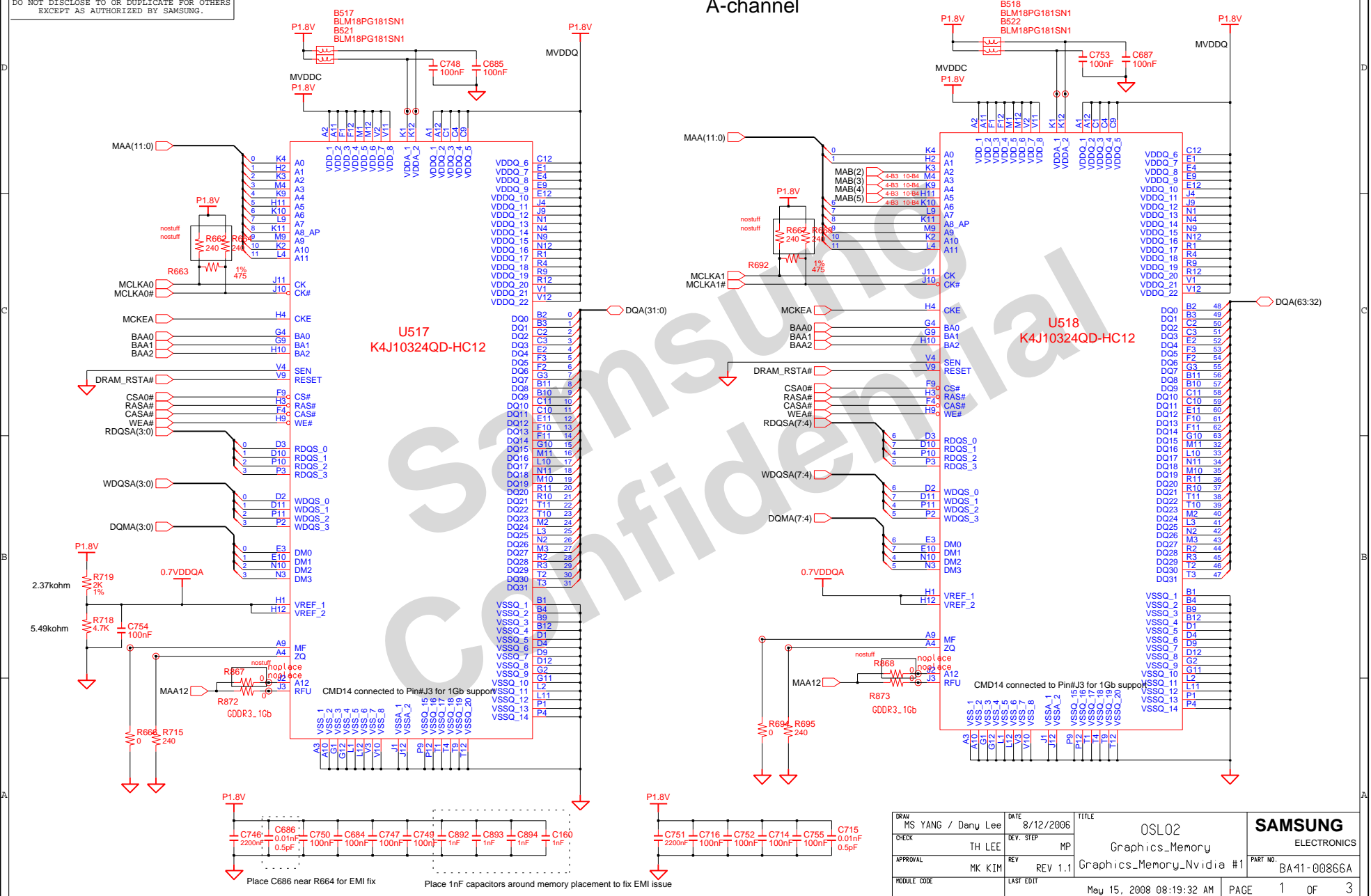


DRAW	MS YANG / Dany Lee	DATE	8/14/2007	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP		EXT NB9X	
APPROVAL	MK KIM	REV	REV 1.1		NB9X POWER RAIL	PART NO. BA11-00866A
MODULE CODE		LAST EDIT				

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A-channel

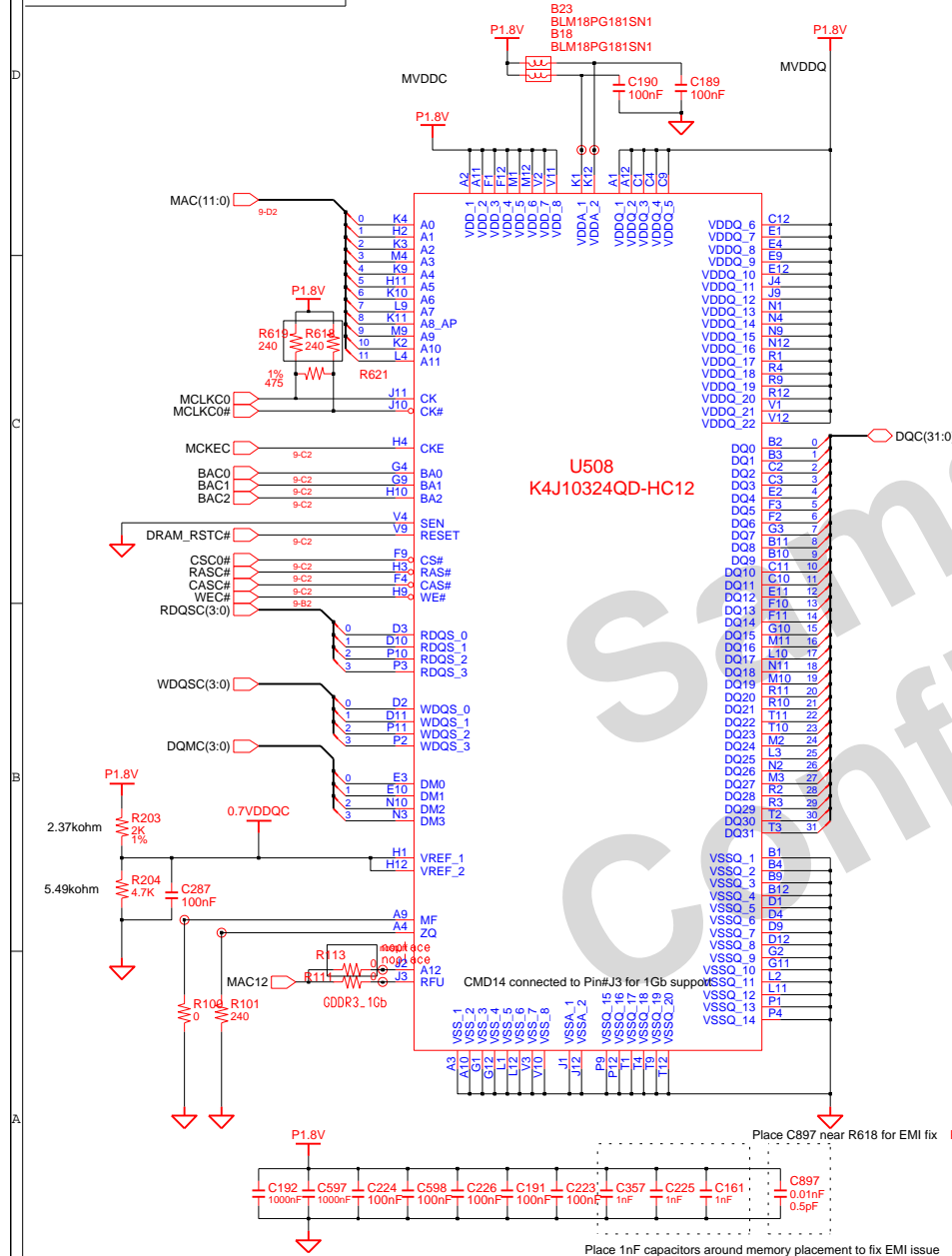


ORAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02 Graphics_Memory	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP			
APPROVAL	MK KIM	REV	REV 1.1			
MODULE CODE		LAST EDIT				
				May 15, 2008 08:19:32 AM	PAGE	1 OF 3

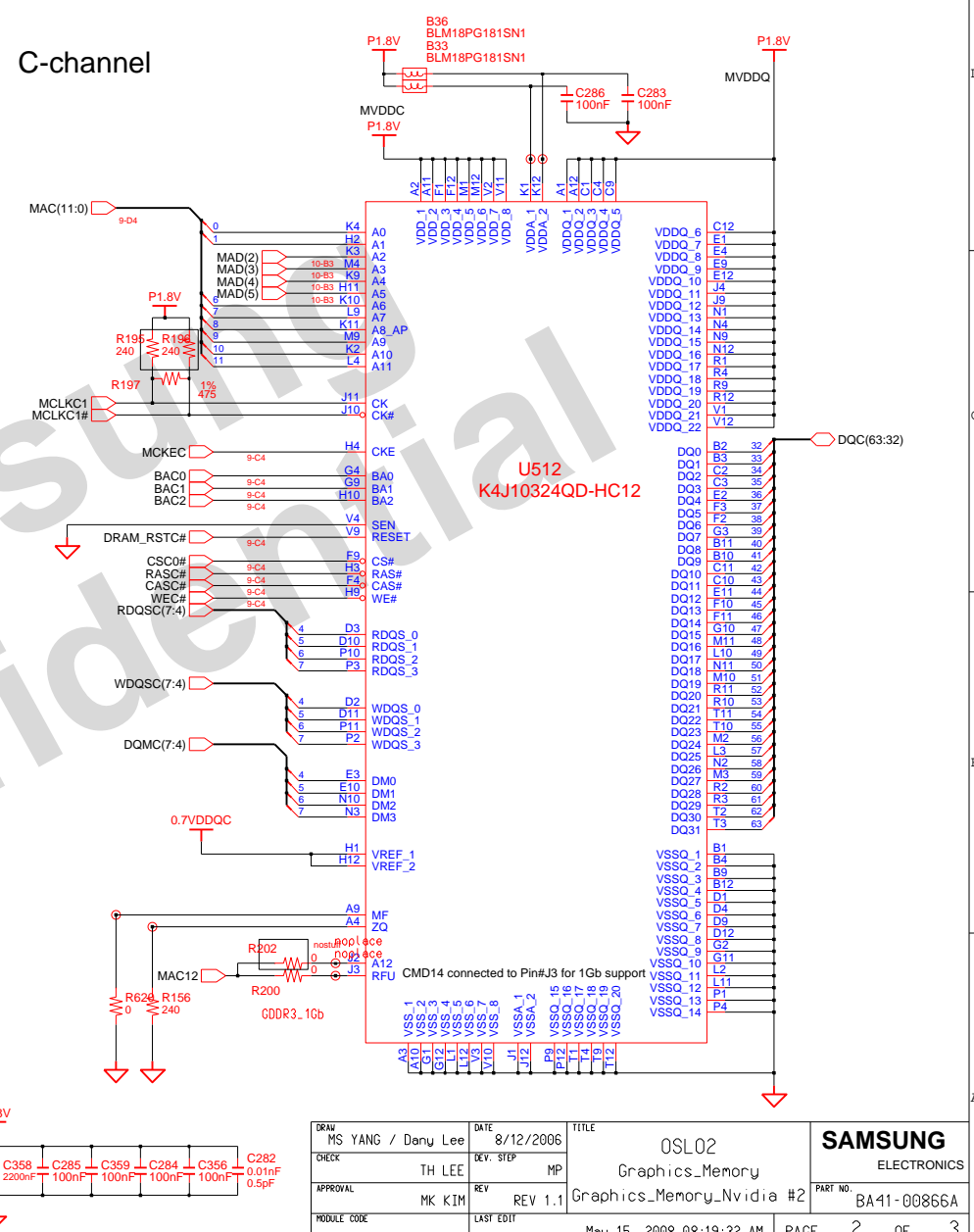
This page is for "2channel-model".

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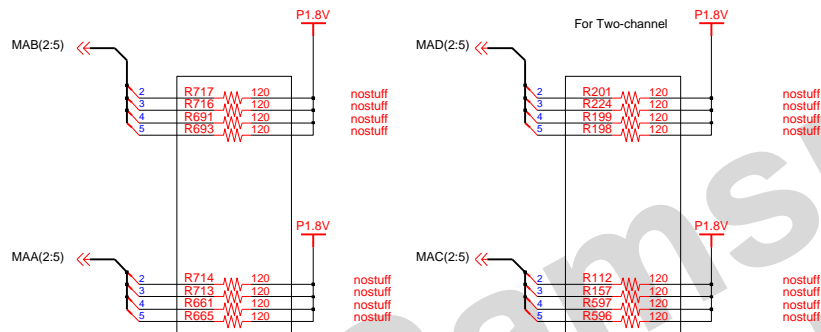
C-channel



DRAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP		Graphics_Memory	
APPROVAL	MK KIM	REV	REV 1.1		Graphics_Memory_Nvidia #2	PART NO.
MODULE CODE		LAST EDIT				BA41-00866A
May 15, 2008 08:19:32 AM						PAGE 2 OF 3

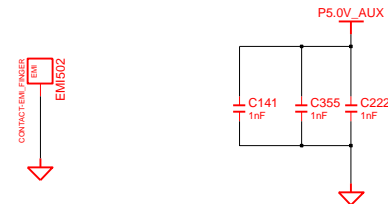
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EMI solution @ OSLO2

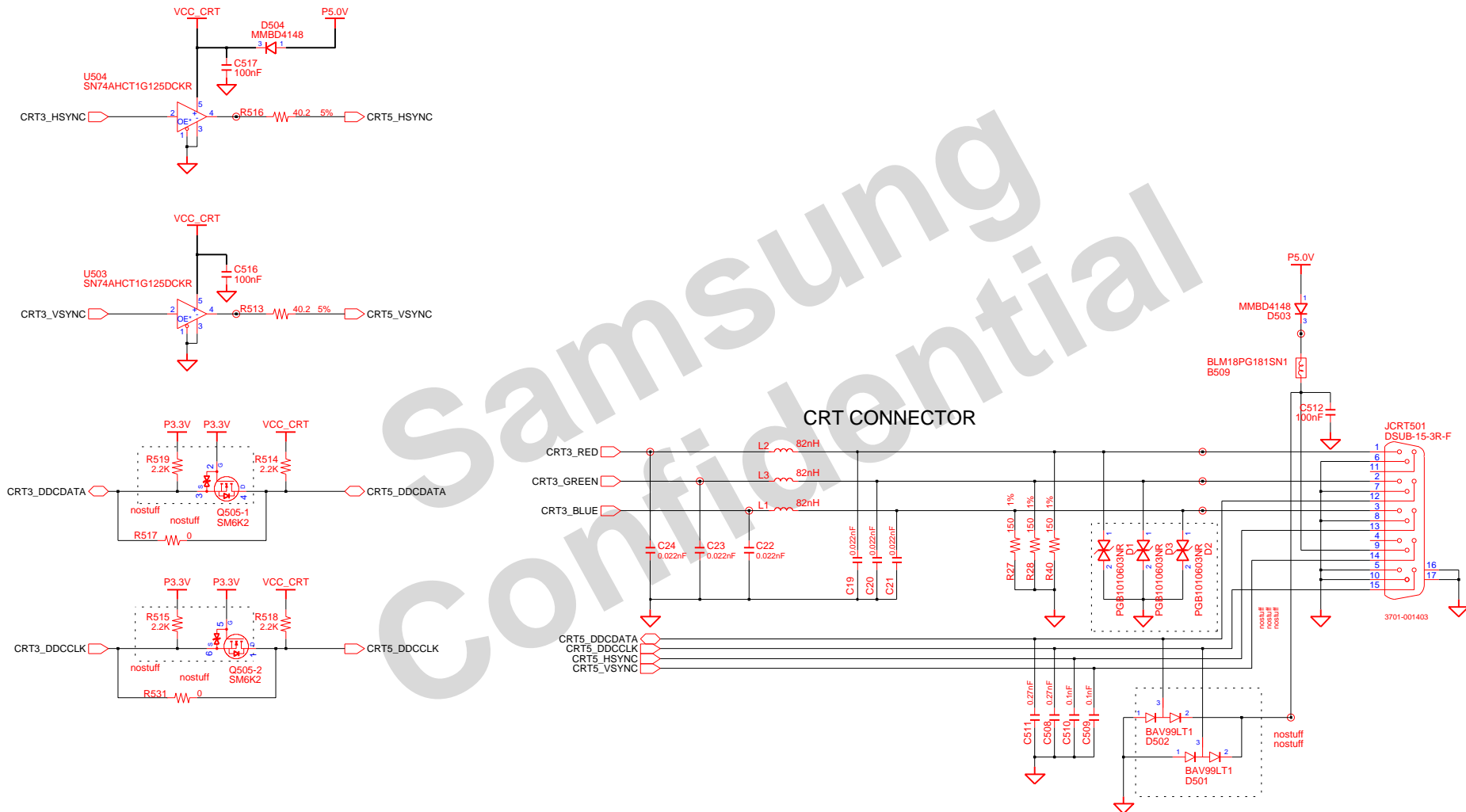
Place three 1nF capacitor around C-channel component



DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSLO2	SAMSUNG ELECTRONICS PART NO. BA41-00866A
CHECK TH LEE	DEV. STEP MP	Graphics_Memory	
APPROVAL MK KIM	REV REV 1.1	Graphics_Memory_Nvidia #3	
MODULE CODE	LAST EDIT	May 15, 2008 08:19:32 AM	
			PAGE 3 OF 3

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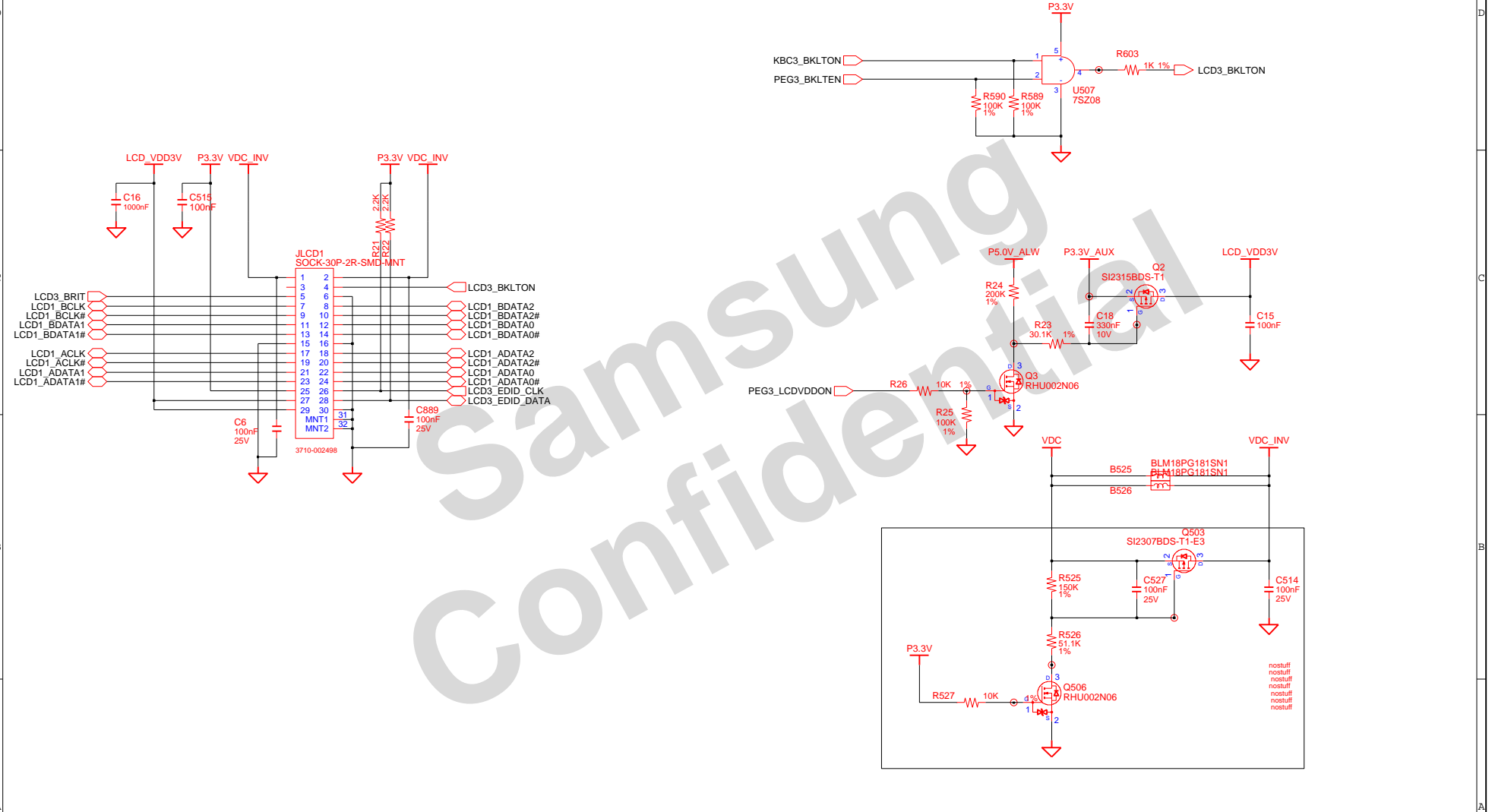
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DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP	Interface_Circuit	
APPROVAL MK KIM	REV REV 1.1	Graphics_IF_CRT	
MODULE CODE	LAST EDIT		
		May 15, 2008 08:19:32 AM	

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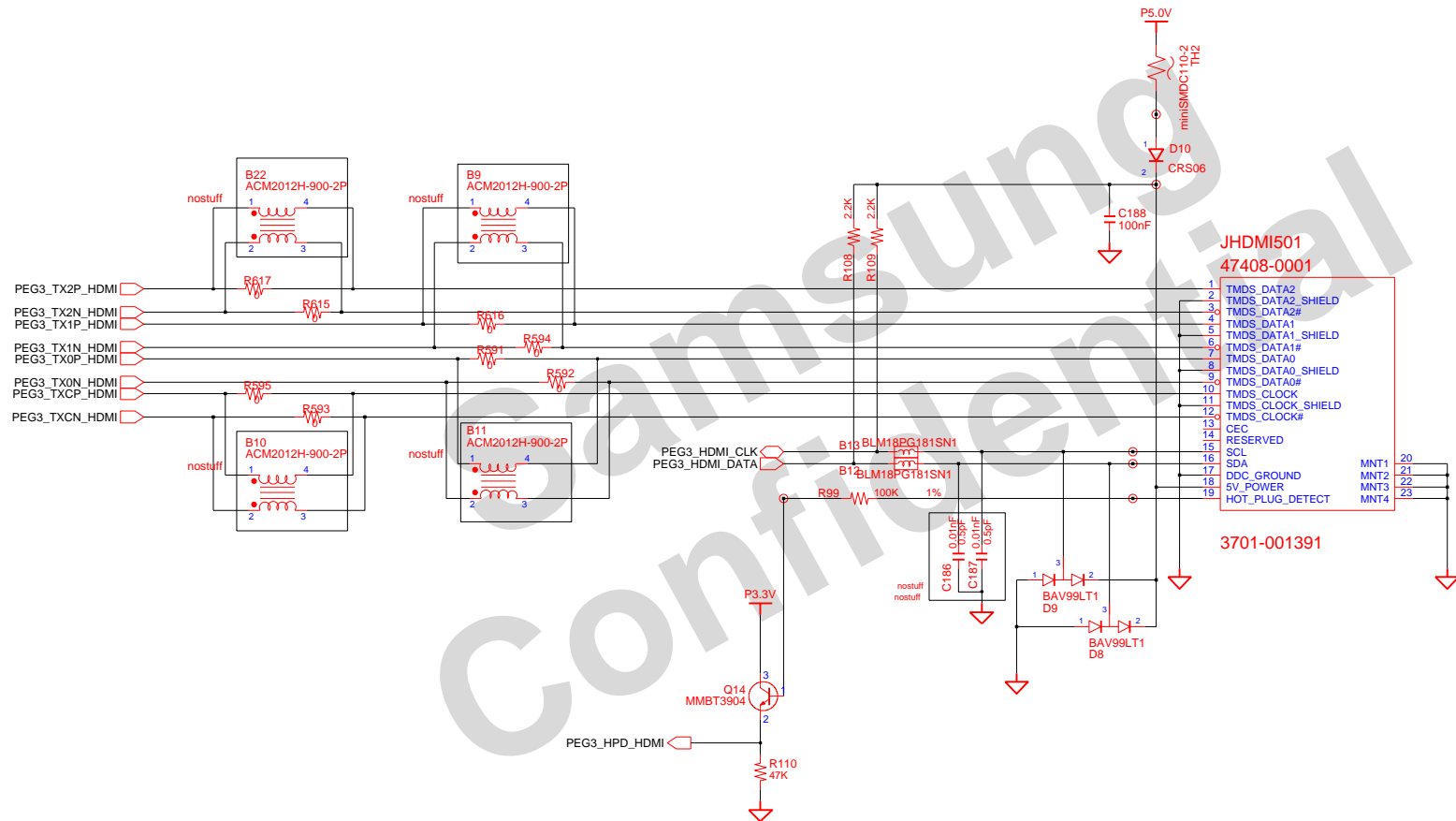
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DRAW	MS YANG / Dany Lee	DATE	8/17/2007	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP		UNDEF INED	
APPROVAL	MK KIM	REV	1.1			PART NO. BA11-00866A
MODULE CODE		LAST EDIT				

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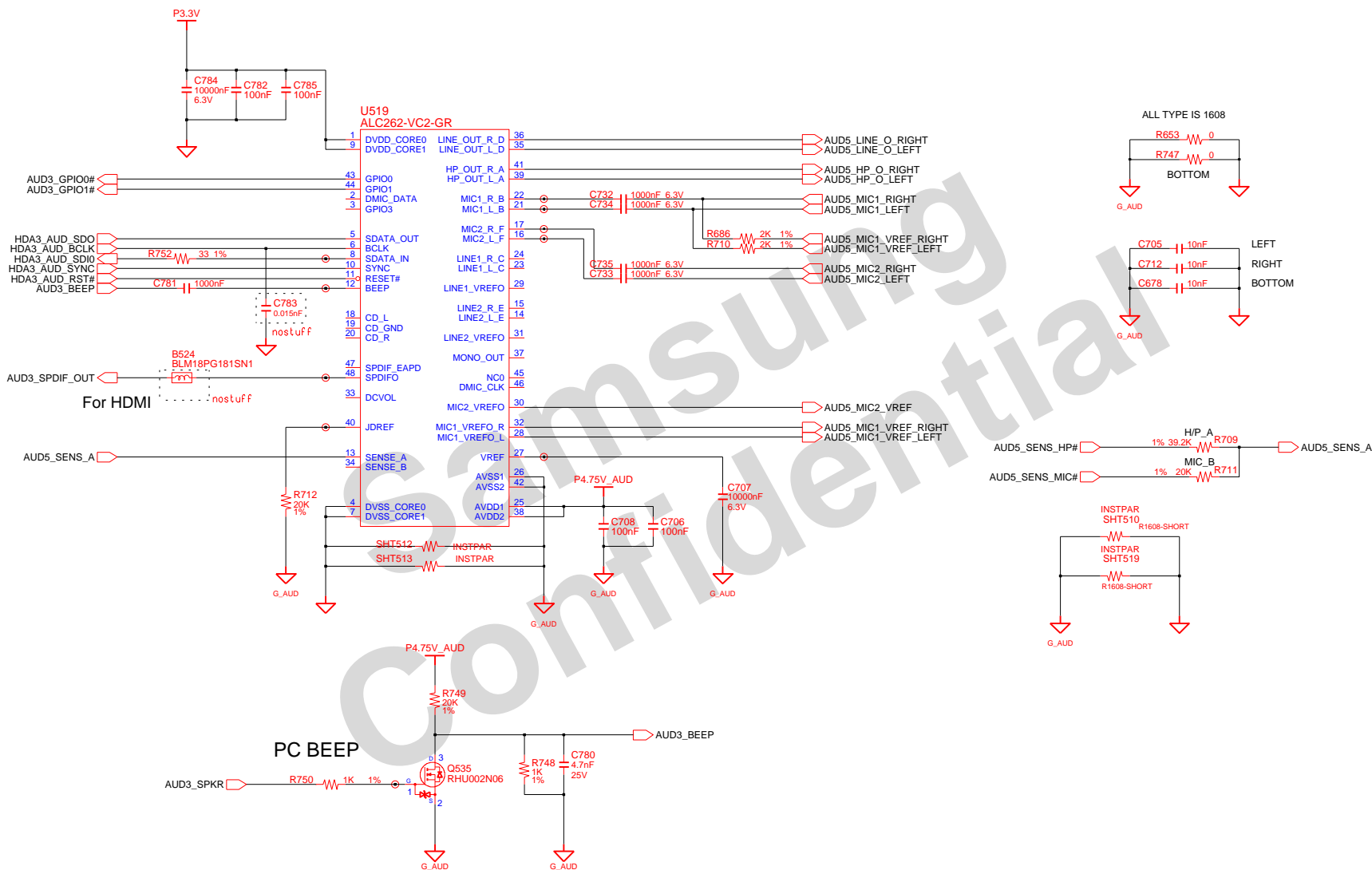
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DRAW MS YANG / Dany Lee	DATE 8/17/2007	TITLE OSL02 UNDEFINED	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP		
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MODULE CODE	LAST EDIT		
May 15, 2008 08:19:32 AM			PAGE 13 of 13

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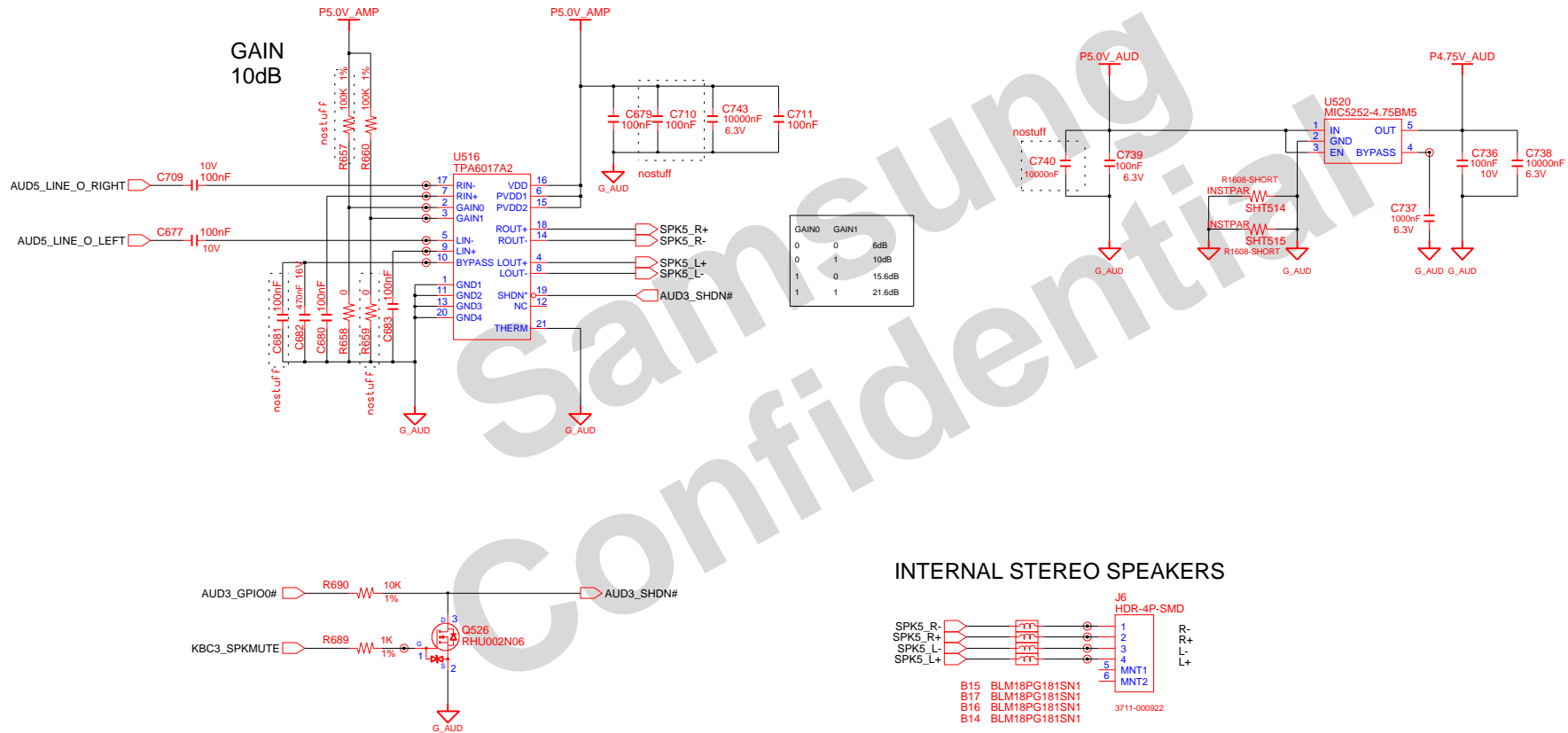
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DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS PART NO. BA41-00866A
CHECK TH LEE	DEV. STEP MP	HDA_Codemc_Alc262	
APPROVAL MK KIM	REV 1.1	HDA_Codemc_Alc262 #1	
MODULE CODE undefined	LAST EDIT		
	May 15, 2008 08:19:32 AM	PAGE 1 OF 5	

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DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS PART NO. BA41-00866A
CHECK TH LEE	DEV. STEP MP	HDA_Codec_Alc262	
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MODULE CODE	LAST EDIT		

May 15, 2008 08:19:32 AM PAGE 2 OF 5

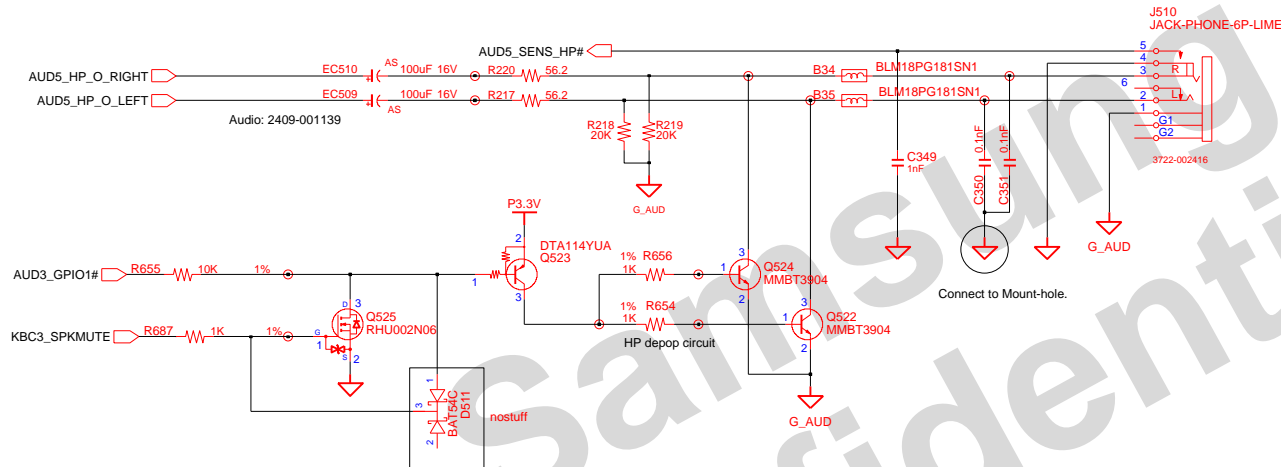


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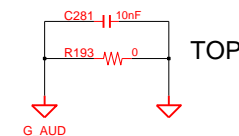
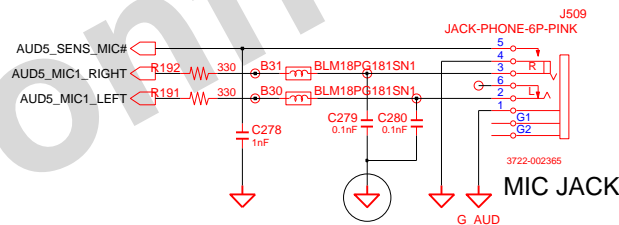
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HEADPHONE



Connect to Mount-hole.



The traces led to Audio Jacks have the width over 10mil

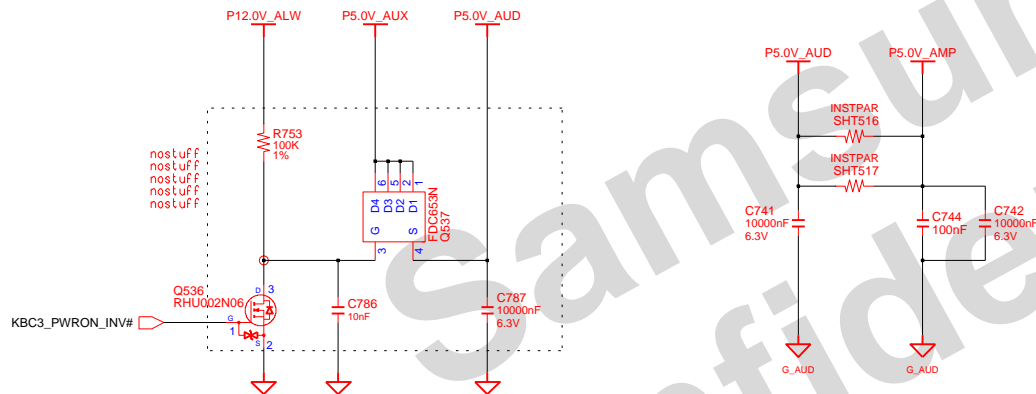
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APPROVAL MK KIM	REV REV 1.1	HDA_Codec_Alc262 #4	
MODULE CODE	LAST EDIT		

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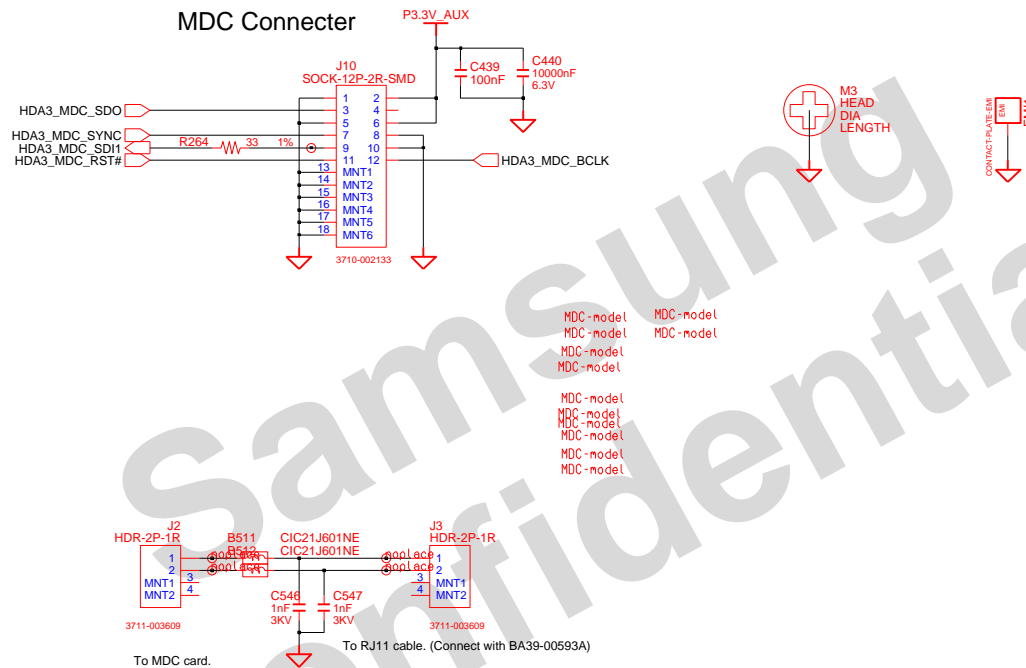
AUDIO POWER



DRAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS PART NO. BA41-00866A
CHECK	TH LEE	DEV. STEP	MP		HDA_Codec_Alc262	
APPROVAL	MK KIM	REV	REV 1.1		HDA_Codec_Alc262 #5	
MODULE CODE	undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	5 OF 5	

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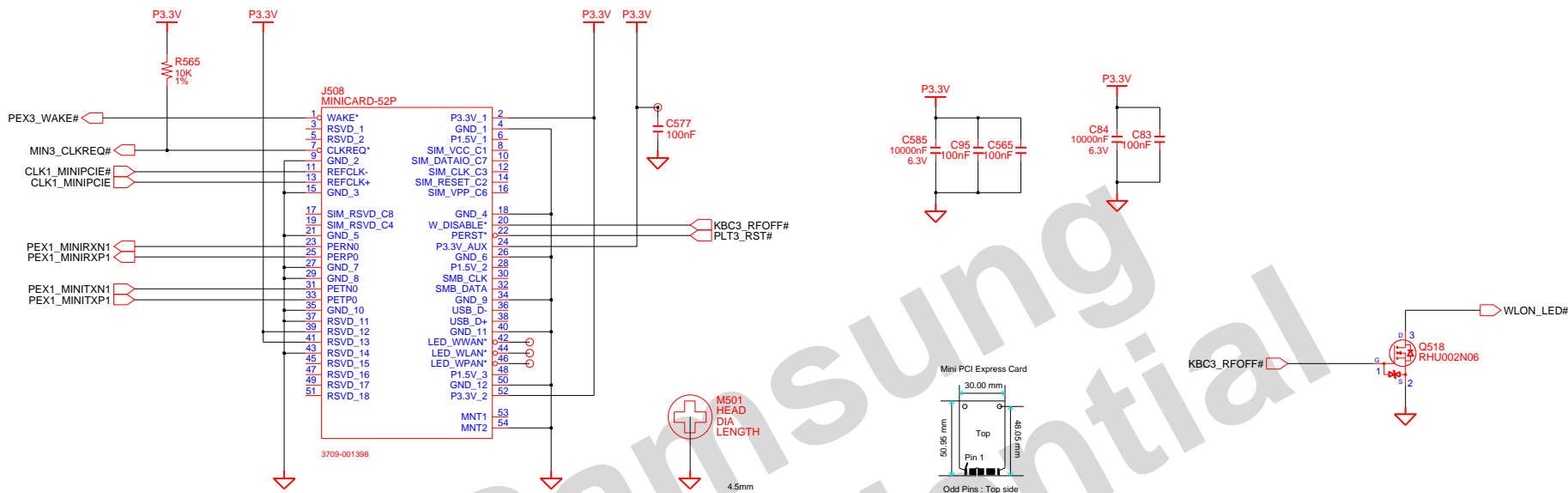


DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 HDA_Modem HDA_Modem	SAMSUNG ELECTRONICS PART NO. BA411-00866A
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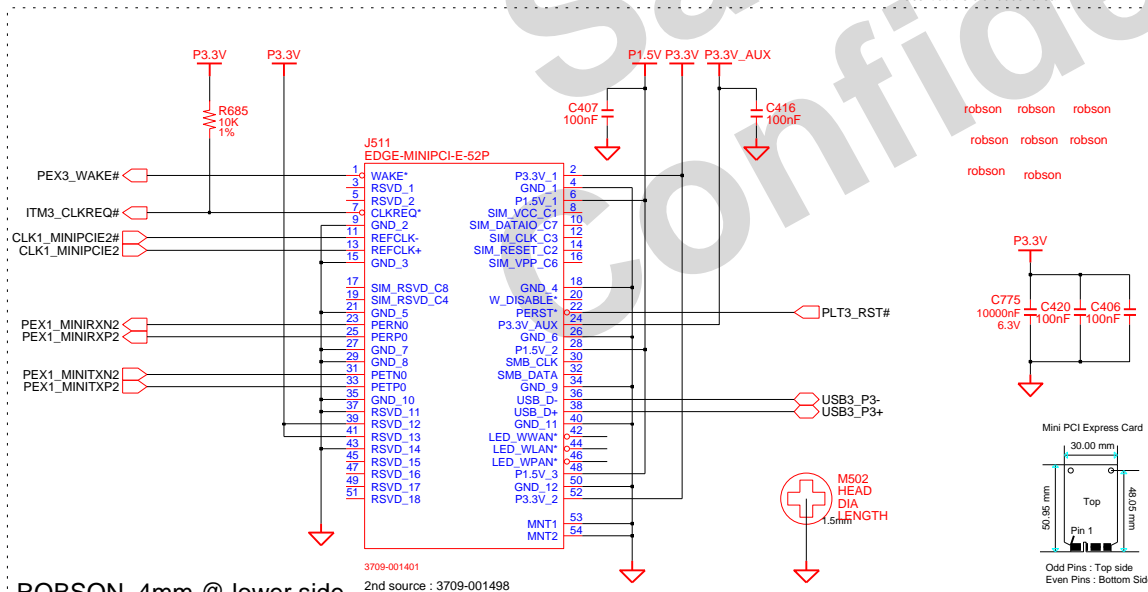
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WLAN, 7mm @ Upper side



To fix Shirley Peak EMI issue
Place it at the old rubber area



ROBSON, 4mm @ lower side

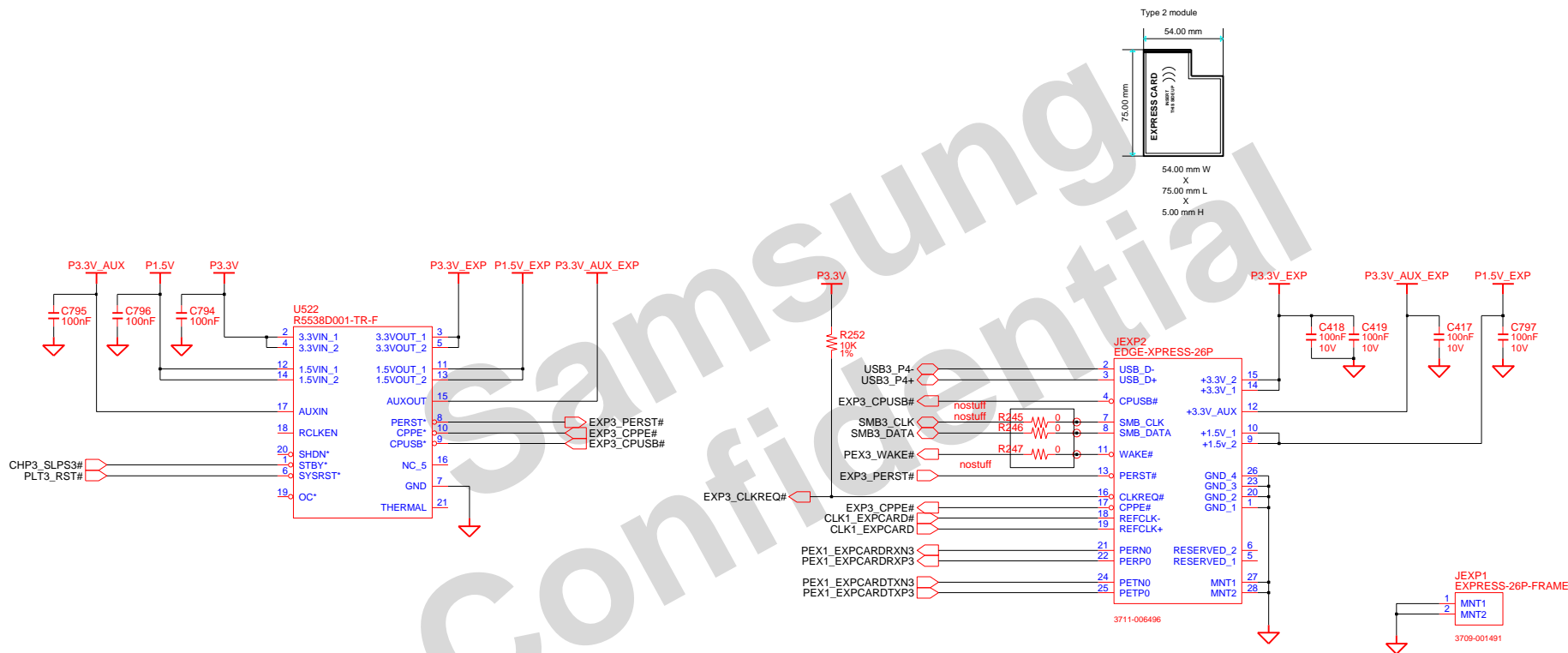
3709-001401
2nd source : 3709-001498

DRAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP		PCIE_Minicard_Slot	
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MODULE CODE	undefined	LAST EDIT				

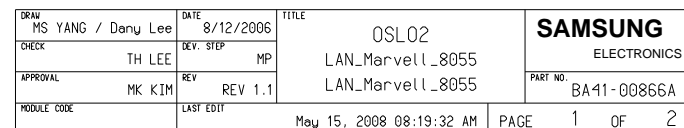
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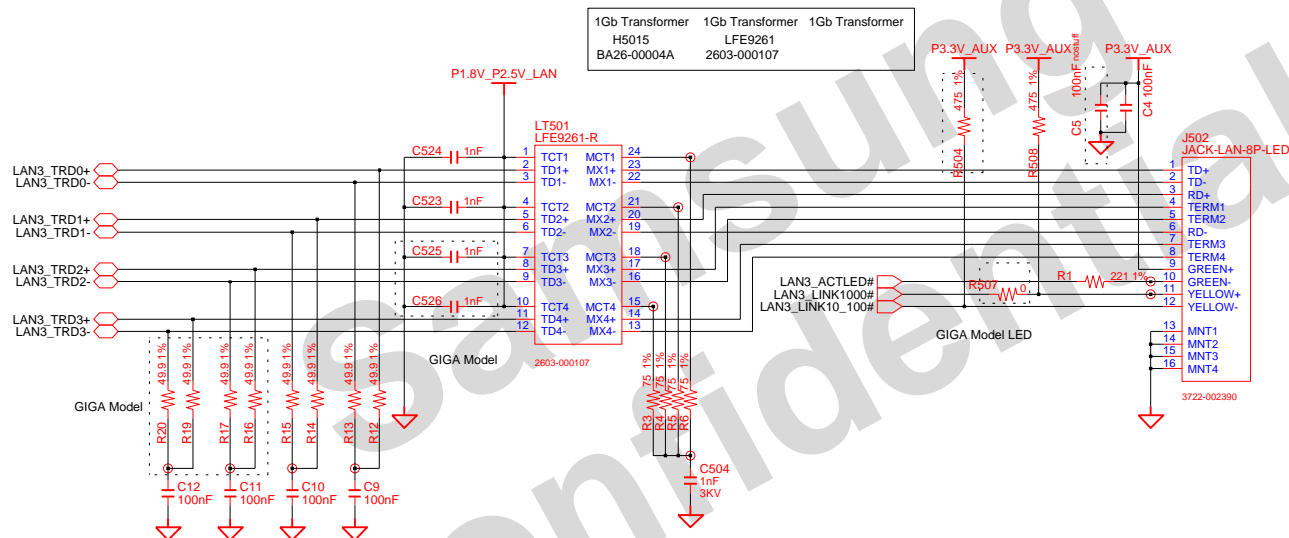
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CHECK	TH LEE	DEV. STEP	MP			
APPROVAL	MK KIM	REV	REV 1.1			
MODULE CODE	undefined	LAST EDIT		May 15, 2008 08:19:32 AM	PAGE 0F	



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The distance between LAN controller
and transformer is designed to extend less than two inches.



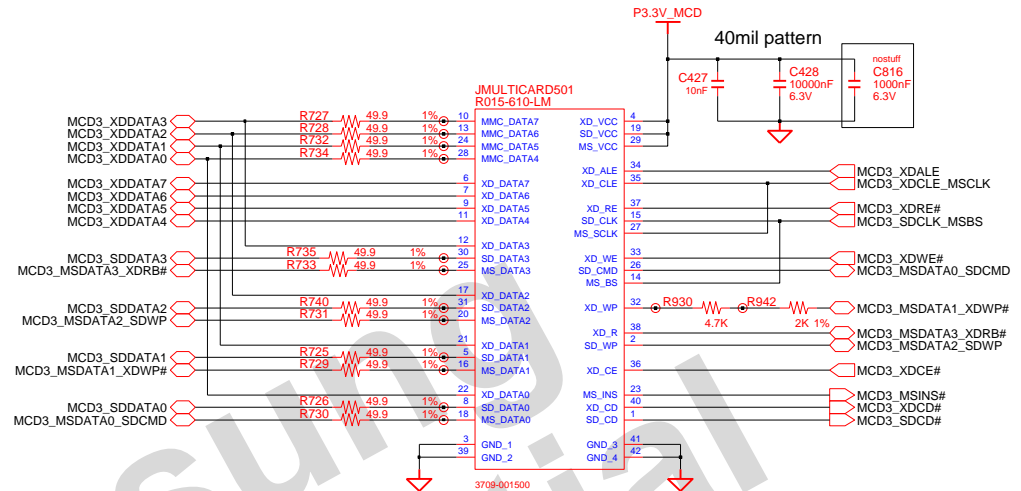
Place near to the Marvell chip.

DRW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS PART NO. BA41-00866A
CHECK TH LEE	DEV. STEP MP	LAN_Marvell_8055	
APPROVAL MK KIM	REV REV 1.1	LAN_Marvell_8055	
MODULE CODE	LAST EDIT		
May 15, 2008 08:19:32 AM			PAGE 2 OF 2

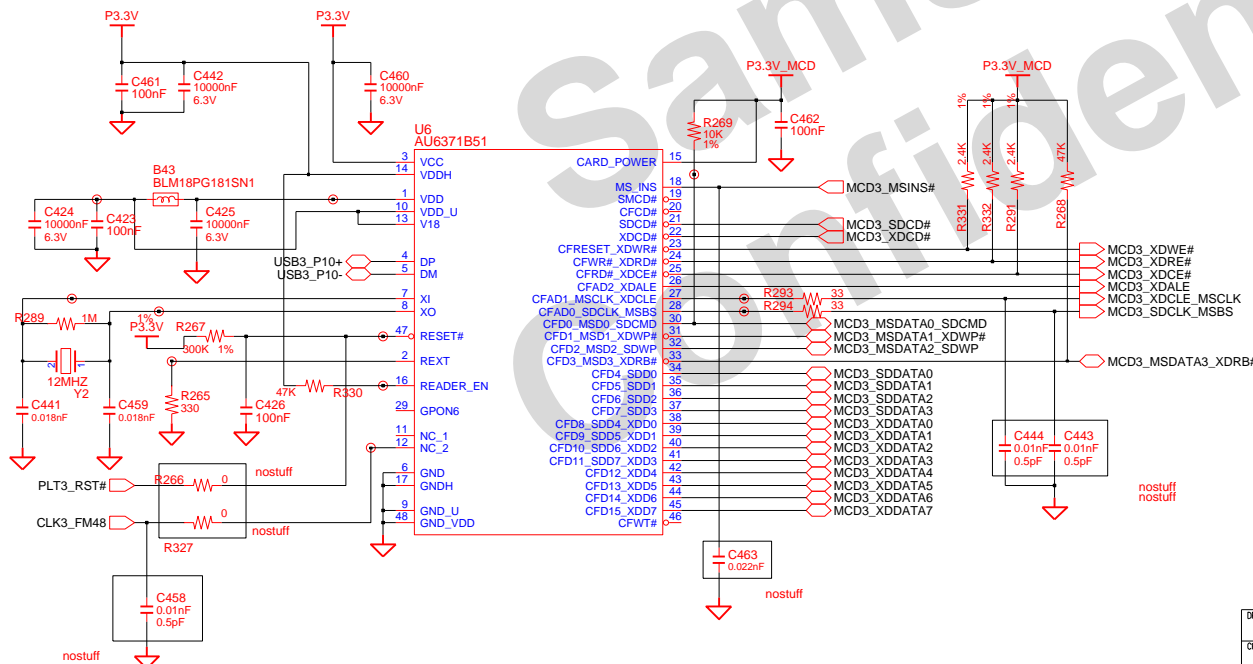
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P3.3V_MCD distance between Controller and socket should be less than 2 inches



40 mil trace for medica card socket ground

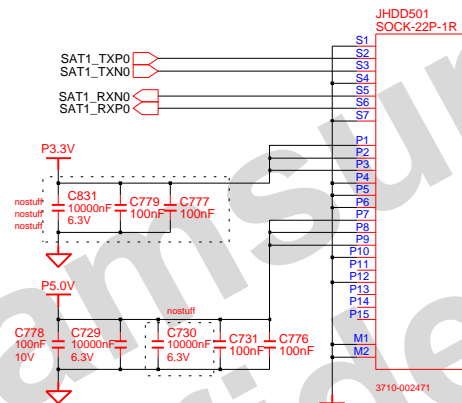


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APPROVAL	MK KIM	REV	REV 1.1	PART NO.	
MODULE CODE		LAST EDIT	Mon 15, 2008 08:19:32 AM	PAGE 15	

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FOR SATA HDD

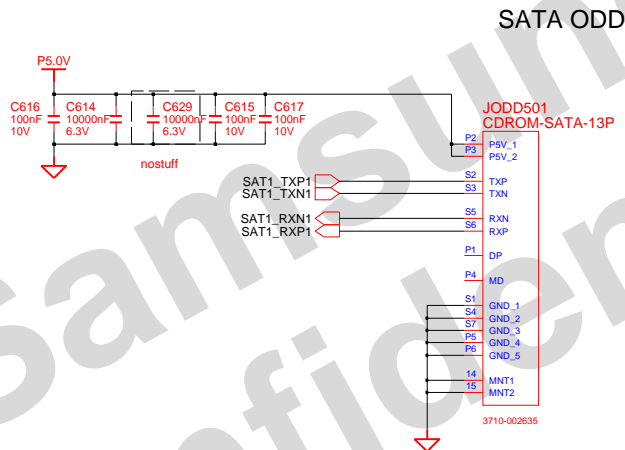


DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP	HDD_IF_Conn	
APPROVAL MK KIM	REV REV 1.1	HDD_IF_Conn	
MODULE CODE	LAST EDIT		

May 15, 2008 08:19:32 AM PAGE 1 OF 1

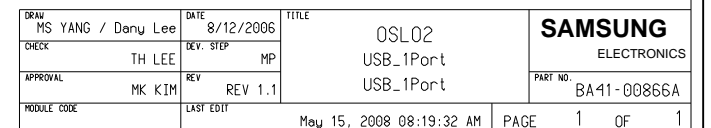
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DRAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP	ODD_IF_Conn	ODD_IF_Conn	
APPROVAL	MK KIM	REV	REV 1.1			PART NO. BA41-00866A
MODULE CODE		LAST EDIT				

May 15, 2008 08:19:32 AM PAGE 1 OF 1



The schematic diagram illustrates the USB3-P0 and USB3-P6 ports and their internal components. Key elements include:

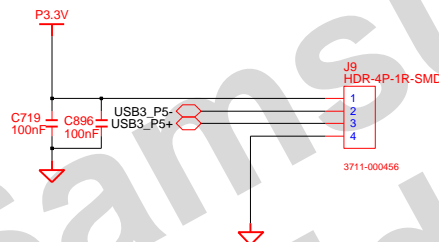
- Power Input:** P5.0V_AUX is connected to a 100nF capacitor (C528) and the IN pin of the U502 TPS2062 USB-to-UART bridge.
- USB3-P0 Port:**
 - USB3_P0- and USB3_P0+ are connected to the PWR0 and USB0 pins of J504.
 - USB3_P0- and USB3_P0+ are connected to the PWR1 and USB1 pins of J504.
 - USB3_P6- and USB3_P6+ are connected to the MNT1 and MNT2 pins of J504.
 - USB3_P6- and USB3_P6+ are connected to the MNT3 and MNT4 pins of J504.
- Internal Components:**
 - U502 TPS2062:** A USB-to-UART bridge with pins IN, OUT1, OC1*, OC2*, EN1*, EN2*, and GND.
 - J504 JAKC-8P-LED-MNT:** An 8-pin connector with pins PWR0, USB0, USB0+, GND1, PWR1, USB1, USB1+, and GND2.
 - B505 ACM2012-900-2P-T:** A 2-pin connector with pins 1 and 2.
 - B507 ACM2012-900-2P-T:** A 2-pin connector with pins 1 and 2.
 - R8, R7, R9, R10:** Resistors connected to the USB3_P0- and USB3_P6- pins.
 - C506, EC502, EC503, C505:** Capacitors connected to the USB3_P0- and USB3_P6- pins.
 - BSS84 Q507:** A MOSFET connected to the USB3_P0- and USB3_P6- pins.
 - R511, R512:** Resistors connected to the USB3_P0- and USB3_P6- pins.
 - Q504 RHU002N06:** A MOSFET connected to the USB3_P0- and USB3_P6- pins.

D:/users/mobile16/mentor/oslo2/oslo2_pr/design_blocks/USB_2Port
SRP Sheet Number: 55 of 76

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Bluetooth Interface

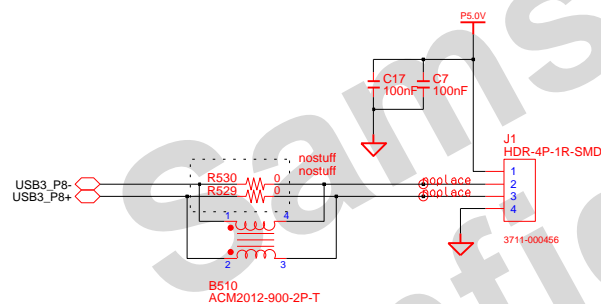


DRAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP	Bluetooth_IF_Conn	Bluetooth_IF_Conn	
APPROVAL	MK KIM	REV	REV 1.1			PART NO. BA41-00866A
MODULE CODE		LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	1 OF 1	

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CAMERA

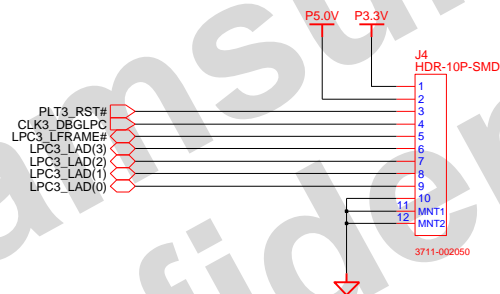


DRW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 Camera_IF_Conn Camera_IF_Conn	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP		PART NO. BA41-00866A
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 1 OF 1

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80H DECODER CONNECTOR

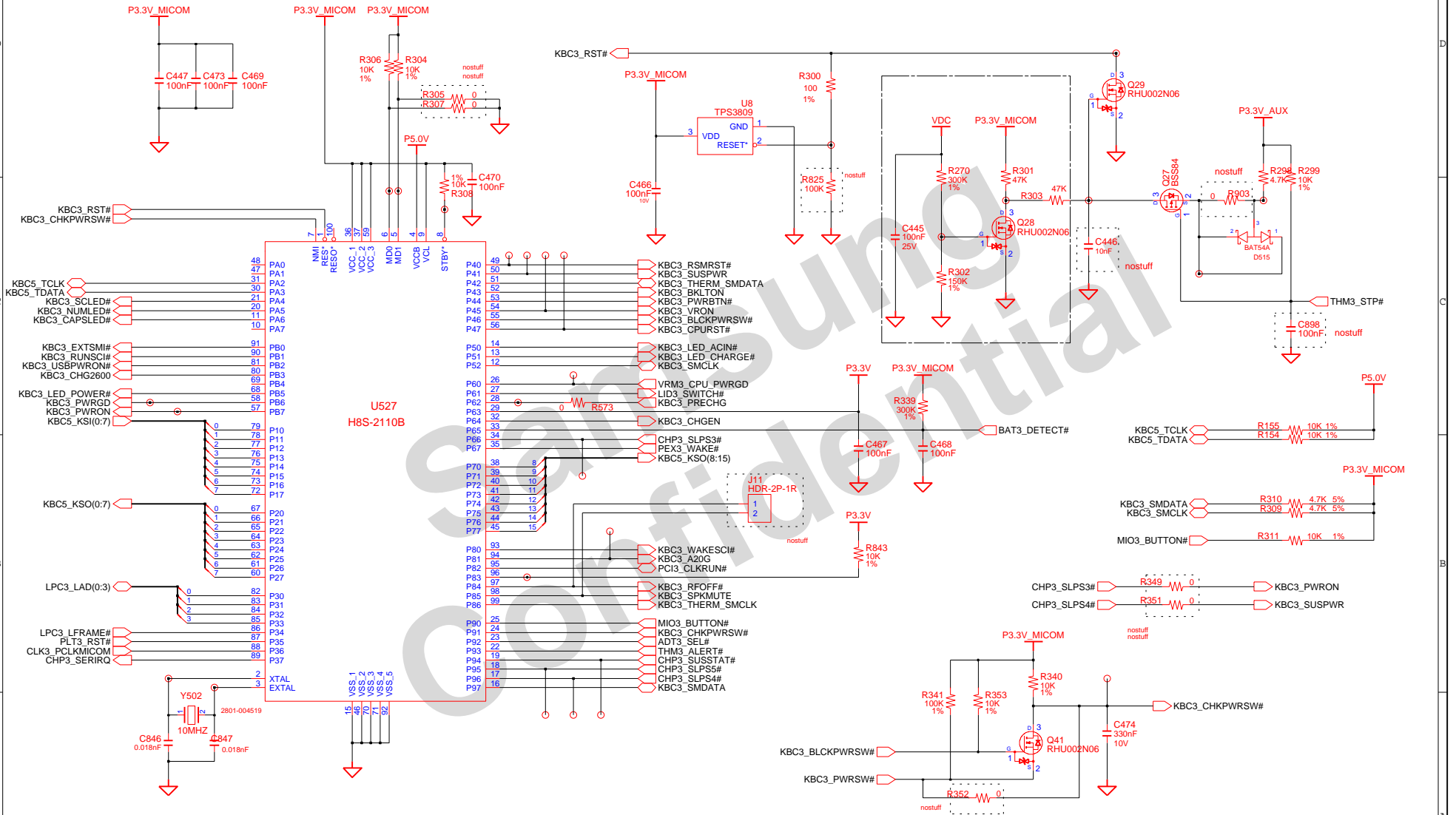


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APPROVAL	MK KIM	REV	REV 1.1			PART NO. BA41-00866A
MODULE CODE		LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	1	OF 1

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MICOM RESET



POWER SWITCH BLOCK WHILE MICOM UPDATE

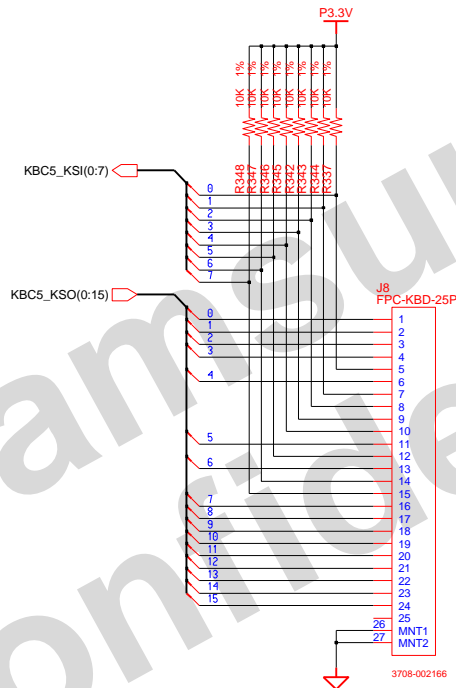
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CHECK	TH LEE	DEV. STEP	MP	MICOM_Renesas2110-100p		
APPROVAL	MK KIM	REV	1.1	MICOM_Renesas2110-100p		
MODULE CODE		LAST EDIT				

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KEYBOARD

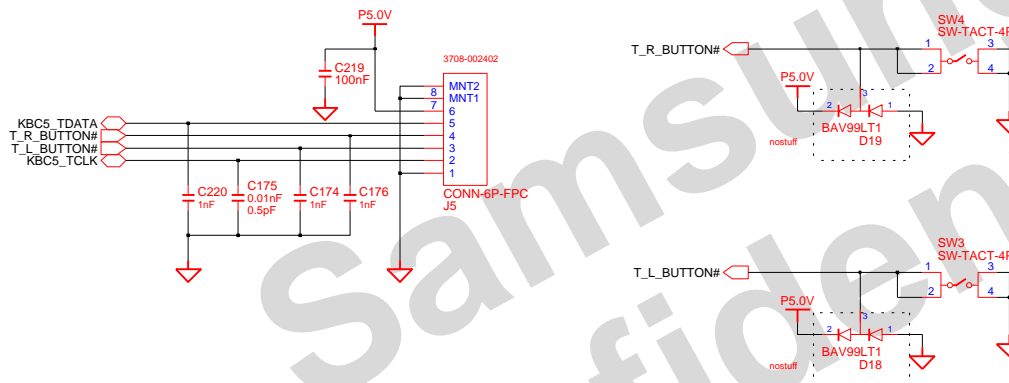


DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 KBD_IF_Conn KBD_IF_Conn	SAMSUNG ELECTRONICS PART NO. BA41-00866A
CHECK TH LEE	DEV. STEP MP	REV REV 1.1	
APPROVAL MK KIM	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 1 OF 1
MODULE CODE			

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TOUCHPAD

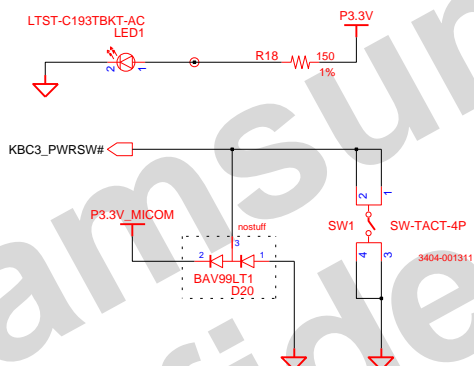


DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 Touchpad_IF_Conn Touchpad_IF_Conn	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP		PART NO. BA41-00866A
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

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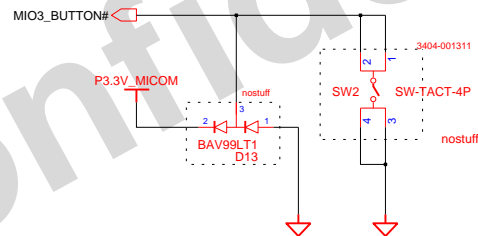
Put this LED located near PWRSW from ME recommendation
Power LED, Blue color



DRAW	MS YANG / Dany Lee	DATE	8/12/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP	PWR_Switchbutton	PWR_Switchbutton	
APPROVAL	MK KIM	REV	REV 1.1			PART NO. BA41-00866A
MODULE CODE		LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	1 OF 1	

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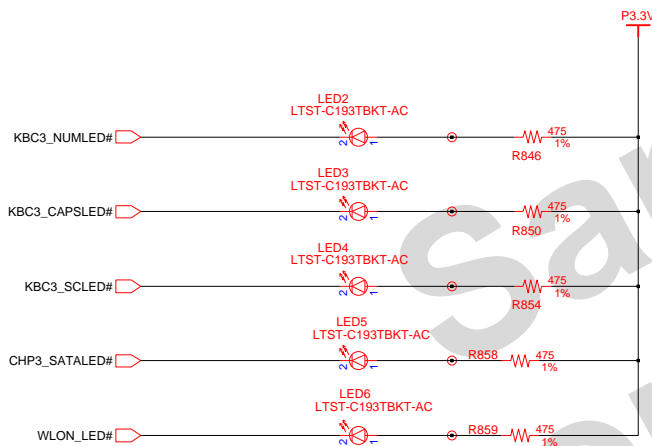
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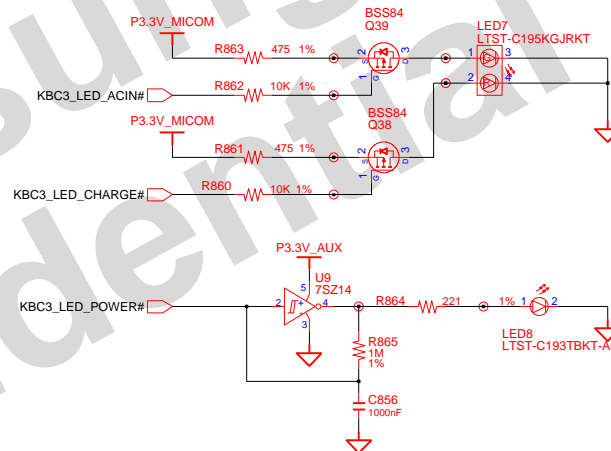
DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 MIO_Switch MIO_Switch	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP		PART NO. BA41-00866A
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 1 OF 1

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ADAPTERIN/CHARGING LED

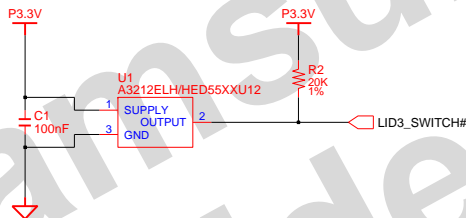


DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 LED_Switch LED_Switch	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP		PART NO. BA41-00866A
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 1 OF 1

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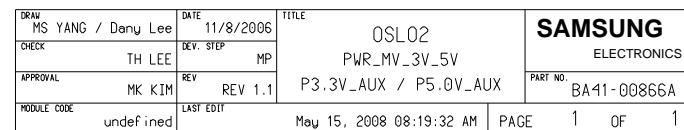
LID_SWITCH



DRAW MS YANG / Dany Lee	DATE 8/12/2006	TITLE OSL02 LID_Switch LID_Switch	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP		PART NO. BA41-00866A
APPROVAL MK KIM	REV REV 1.1		
MODULE CODE	LAST EDIT May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

[illegible]

TONSEL VREF2
5V / 3.3V : 280KHz / 430KHz
(4.5A)

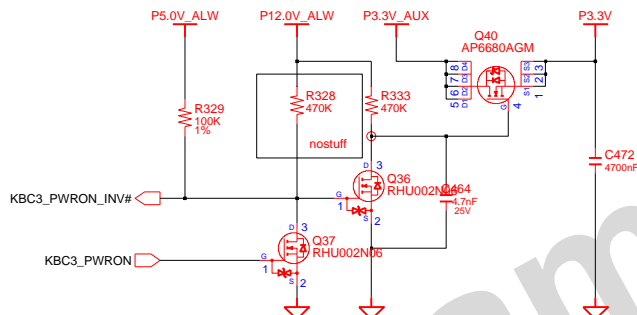


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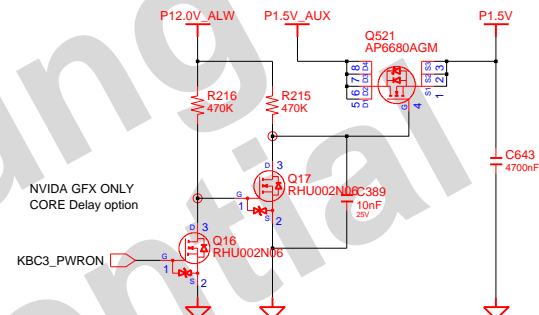
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Switched Power

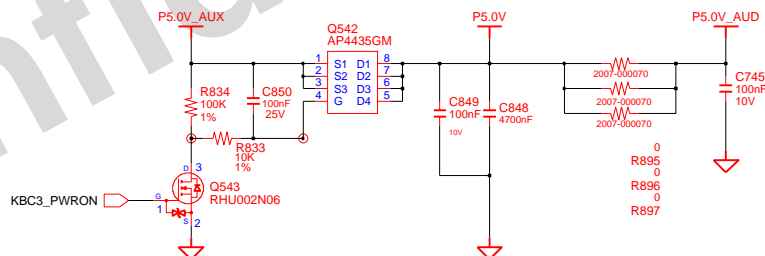
Switched Power On (P3.3V)



Switched Power On (P1.5V)



Switched Power On (P5.0V)

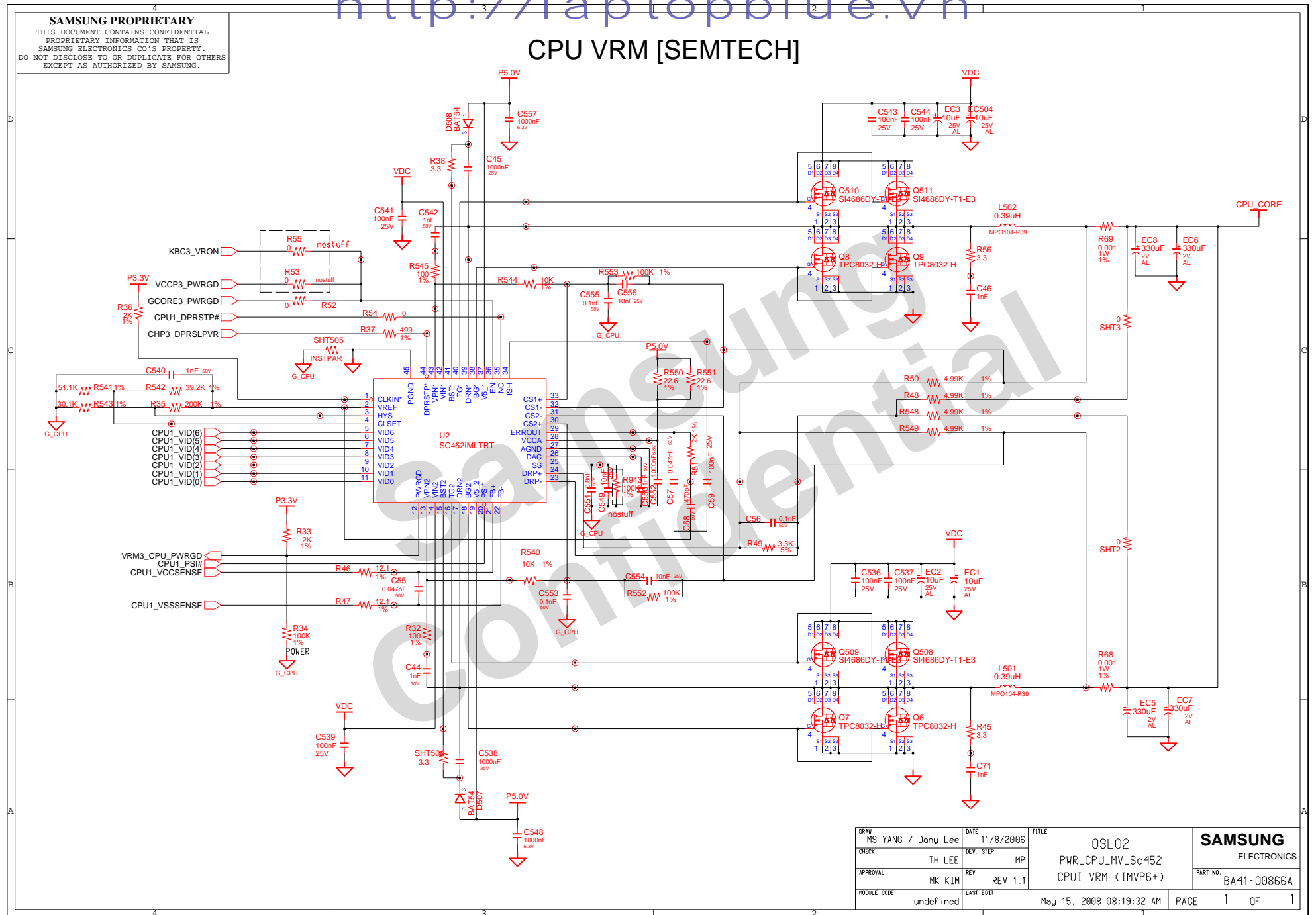


DRAW MS YANG / Dany Lee	DATE 01/09/2008	TITLE OSLO2 PWR_MV_Switched SWITCHED POWER	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP	REV 1.1	
APPROVAL MK KIM	REV 1.1	LAST EDIT	
MODULE CODE			

CPU VRM [SEMTECH]

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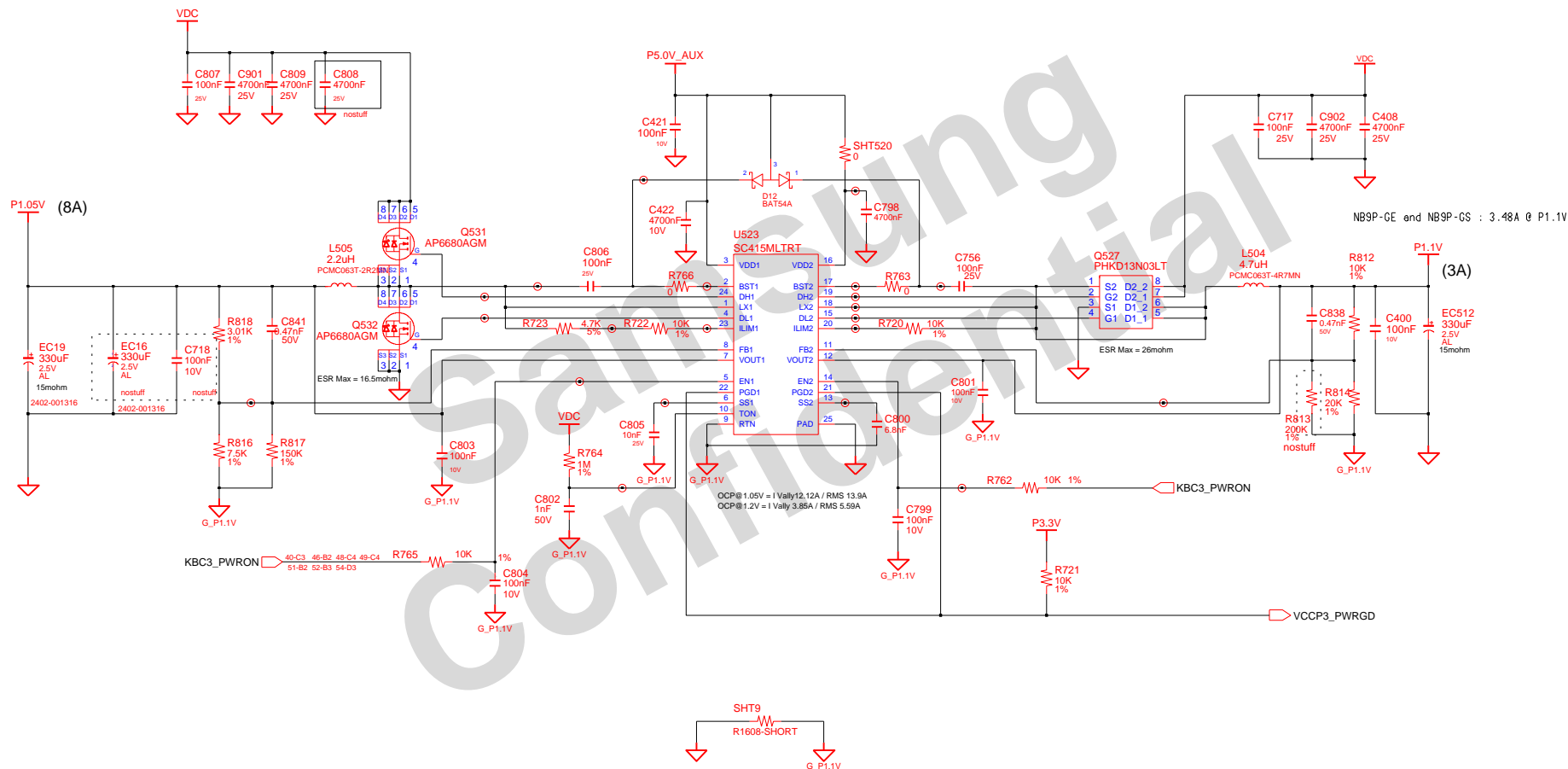
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DRAW	MS YANG / Dany Lee	DATE	11/8/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP		PWR_CPU_MV_Sc452	
APPROVAL	MK KIM	REV	1.1		CPU1 VRM (IMVP6+)	PART NO.
MODULE CODE	undefined	LAST EDIT				BA11-00866A
				May 15, 2008 08:19:32 AM	PAGE	1 OF 1

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CHIPSET POWER(P1.05V & P1.1V)

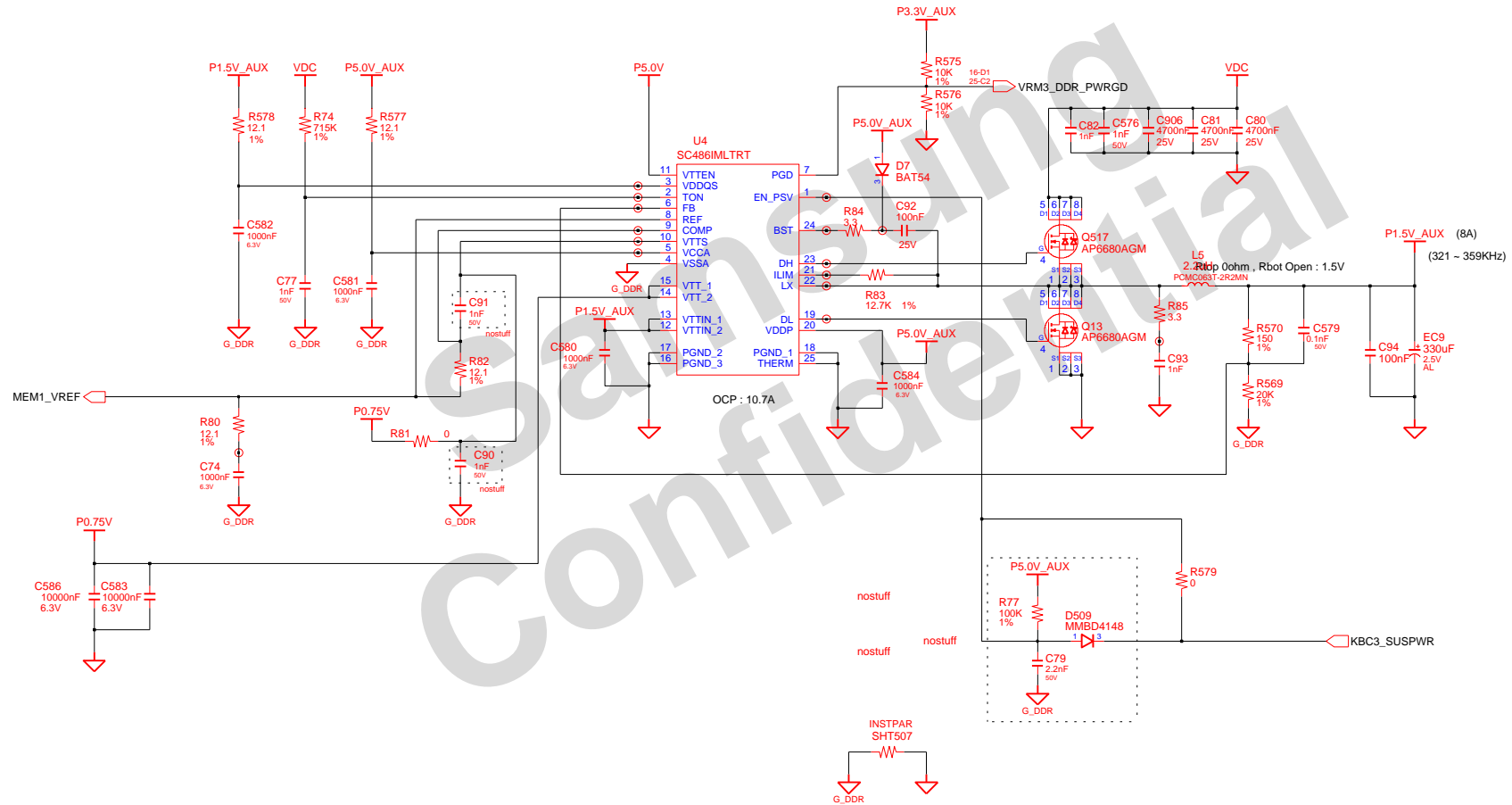


DRAW	MS YANG / Dany Lee	DATE	8/14/2007	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	REV.	STEP	MP	PWR_MV_Cantiga	
APPROVAL	MK KIM	REV	1	Chipset Power (P1.05V, P1.1V)	PART NO.	BA41-00866A
MODULE CODE	undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	1	OF 1

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DDR3 Power

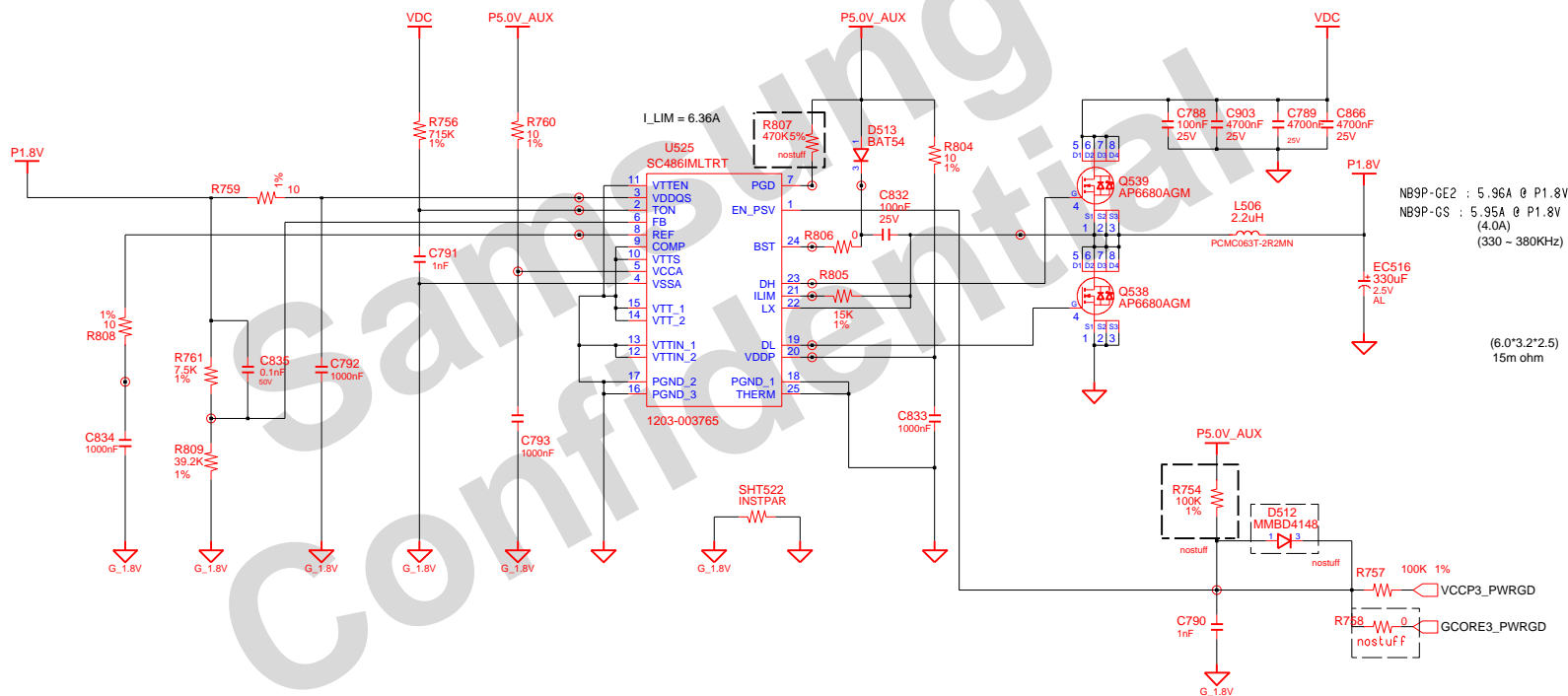


DRAW	MS YANG / Dany Lee	DATE	11/8/2006	TITLE	OSL02	SAMSUNG ELECTRONICS
CHECK	TH LEE	DEV. STEP	MP	PWR_MV_Memory		
APPROVAL	MK KIM	REV	REV 1.1	DDR3 POWER (P1.5V_AUX)	PART NO.	BA11-00866A
MODULE CODE	undefined	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE	1	OF 1

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P1.8V (External Gfx Memory)



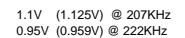
NB9P-GE2 : 5.96A @ P1.8V
NB9P-GS : 5.95A @ P1.8V
(4.0A)
(330 ~ 380KHz)

(6.0*3.2*2.5)
15m ohm

DRAW MS YANG / Dany Lee	DATE 8/14/2007	TITLE OSL02 PWR_Gfx_MV_Ext Ext Gfx Memory(SC486)	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK TH LEE	DEV. STEP MP	REV 1.1	
APPROVAL MK KIM	REV 1.1	LAST EDIT May 15, 2008 08:19:32 AM	
MODULE CODE	LAST EDIT	PAGE 1 OF 2	

Location	Value	VID0	VID1	SPEC	RESULT
R770	2 K	0	0	0.89 V	0.9000
R778	11.8K	1	0	1.00 V	1.0013
R777	3.01 K	0	1	1.05 V	1.0500
R773	10 K	1	1	Reserved	1.1027
R775	6.99 K				

Location	Value	VID0	VID1	SPEC	RESULT
R770		0	0		
R778		1	0		
R777		0	1		
R773		1	1		
R779					

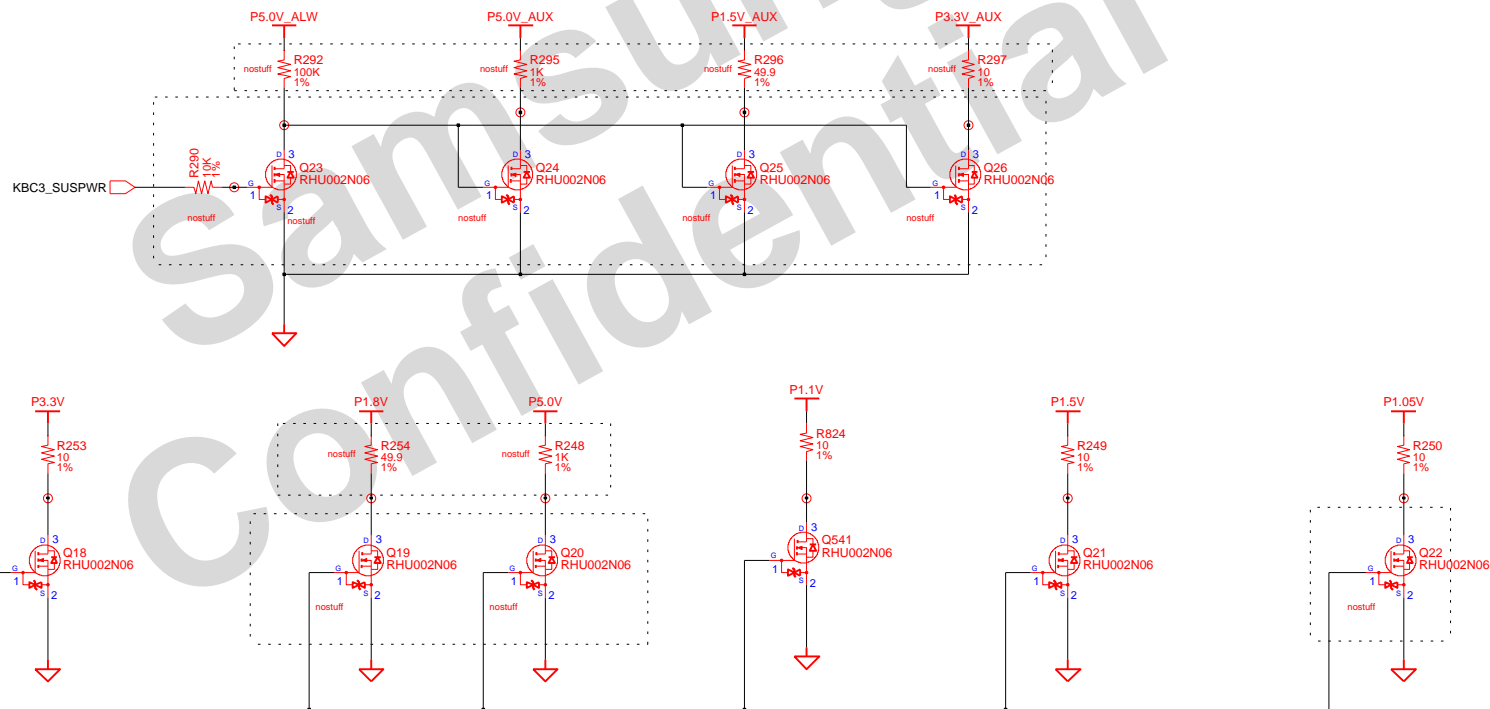


D:/users/mobile16/mentor/oslo2/oslo2_pr/design_blocks/PWR_Gfx_MV_Ext
SRP Sheet Number: 73 of 76

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POWER DISCHARGER

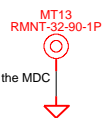
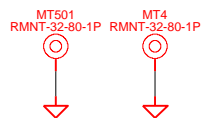
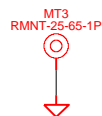
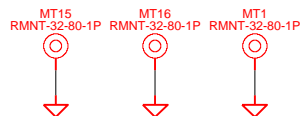


DRAW	MS YANG / Dany Lee	DATE	8/14/2007	TITLE	OSL02	SAMSUNG ELECTRONICS PART NO. BA11-00866A
CHECK	TH LEE	DEV. STEP	MP		PWR_MV_DisCharger	
APPROVAL	MK KIM	REV	REV 1.1		DISCHARGING LOGIC	
MODULE CODE	undefined	LAST EDIT				
				May 15, 2008 08:19:32 AM	PAGE	1 OF 1

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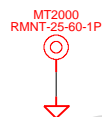
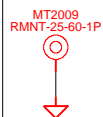
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For KBD support

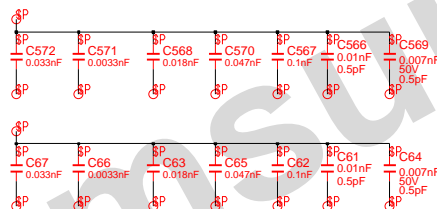
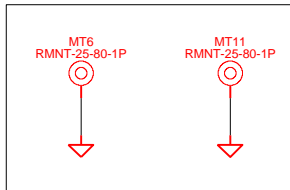
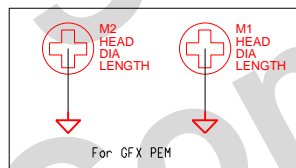
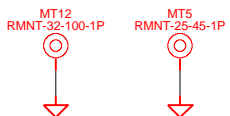
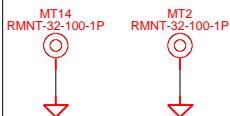


Place it near the MDC 32,90

25,60

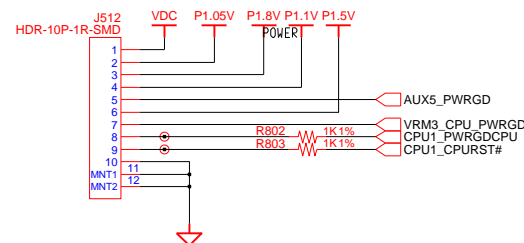


32,100

REV1
1 O no place
2 O O3

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

ICT PORT



DRAW MS YANG / Dany Lee	DATE 11/23/2007	TITLE OSL02 UNDEFINED	SAMSUNG ELECTRONICS
CHECK TH LEE	DEV. STEP MP	REV REV 1.1	PART NO. BA11-00866A
APPROVAL MK KIM	LAST EDIT	May 15, 2008 08:19:32 AM	PAGE 12 OF 13

Sheet1 ----- Root[sheet1]
Sheet2 ----- Root[sheet2]
Sheet3 ----- Root[sheet3]
Sheet4 ----- Root[sheet4]
Sheet5 ----- Root[sheet5]
Sheet6 ----- Root[sheet6]
Sheet7 ----- Root[sheet7]
Sheet8 ----- Root[sheet8]
Sheet9 ----- Root[sheet9]
Sheet10 ----- Root[sheet10]
Sheet11 ----- Root[sheet11]
Sheet12 ----- CK_Clock_505M[sheet1]
Sheet13 ----- Thermal_Sensor_SMSC_Emc2102[sheet1]
Sheet14 ----- CPU_Penryn_MV_SV[sheet1]
Sheet15 ----- CPU_Penryn_MV_SV[sheet2]
Sheet16 ----- CPU_Penryn_MV_SV[sheet3]
Sheet17 ----- MCH_CANTIGA_PM_DDR3[sheet1]
Sheet18 ----- MCH_CANTIGA_PM_DDR3[sheet2]
Sheet19 ----- MCH_CANTIGA_PM_DDR3[sheet3]
Sheet20 ----- MCH_CANTIGA_PM_DDR3[sheet4]
Sheet21 ----- MCH_CANTIGA_PM_DDR3[sheet5]
Sheet22 ----- SODIMM_DDR3[sheet1]
Sheet23 ----- SODIMM_DDR3[sheet2]
Sheet24 ----- ICH_9M_B[sheet1]
Sheet25 ----- ICH_9M_B[sheet2]
Sheet26 ----- ICH_9M_B[sheet3]
Sheet27 ----- ICH_9M_B[sheet4]
Sheet28 ----- ICH_9M_B[sheet5]
Sheet29 ----- SPI_BIOS_ROM[sheet1]
Sheet30 ----- Gfx_External_Nvidia_Nb9x[sheet1]
Sheet31 ----- Gfx_External_Nvidia_Nb9x[sheet2]
Sheet32 ----- Gfx_External_Nvidia_Nb9x[sheet3]
Sheet33 ----- Gfx_External_Nvidia_Nb9x[sheet4]
Sheet34 ----- Gfx_External_Nvidia_Nb9x[sheet5]
Sheet35 ----- Graphics_Memory_Nvidia[sheet1]
Sheet36 ----- Graphics_Memory_Nvidia[sheet2]
Sheet37 ----- Graphics_Memory_Nvidia[sheet3]
Sheet38 ----- Graphics_IF_CRT[sheet1]
Sheet39 ----- Graphics_IF_CRT[sheet2]
Sheet40 ----- Graphics_IF_CRT[sheet3]
Sheet41 ----- HDA_Codec_Alc262[sheet1]
Sheet42 ----- HDA_Codec_Alc262[sheet2]
Sheet43 ----- HDA_Codec_Alc262[sheet3]
Sheet44 ----- HDA_Codec_Alc262[sheet4]
Sheet45 ----- HDA_Codec_Alc262[sheet5]
Sheet46 ----- HDA_Modem[sheet1]
Sheet47 ----- PCIE_Minicard_Slot[sheet1]
Sheet48 ----- Express_card[sheet1]
Sheet49 ----- LAN_Marvell_8055[sheet1]
Sheet50 ----- LAN_Marvell_8055[sheet2]

Sheet51 ----- Multi_MV_Au6372[sheet1]
Sheet52 ----- HDD_IF_Conn[sheet1]
Sheet53 ----- ODD_IF_Conn[sheet1]
Sheet54 ----- USB_1Port[sheet1]
Sheet55 ----- USB_2Port[sheet1]
Sheet56 ----- Bluetooth_IF_Conn[sheet1]
Sheet57 ----- Camera_IF_Conn[sheet1]
Sheet58 ----- Other_Debug_80[sheet1]
Sheet59 ----- MICOM_Renesas2110_100p[sheet1]
Sheet60 ----- KBD_IF_Conn[sheet1]
Sheet61 ----- Touchpad_IF_Conn[sheet1]
Sheet62 ----- PWR_Switchbutton[sheet1]
Sheet63 ----- MIO_Switch[sheet1]
Sheet64 ----- LED_Switch[sheet1]
Sheet65 ----- LID_Switch[sheet1]
Sheet66 ----- PWR_MV_Charger_Isl6256a[sheet1]
Sheet67 ----- PWR_MV_3V_5V[sheet1]
Sheet68 ----- PWR_MV_Switched[sheet1]
Sheet69 ----- PWR_CPU_MV_Sc452[sheet1]
Sheet70 ----- PWR_MV_Cantiga[sheet1]
Sheet71 ----- PWR_MV_Memory[sheet1]
Sheet72 ----- PWR_Gfx_MV_Ext[sheet1]
Sheet73 ----- PWR_Gfx_MV_Ext[sheet2]
Sheet74 ----- PWR_MV_DisCharger[sheet1]
Sheet75 ----- Root[sheet12]
Sheet76 ----- Root[sheet13]