

# CICHLID

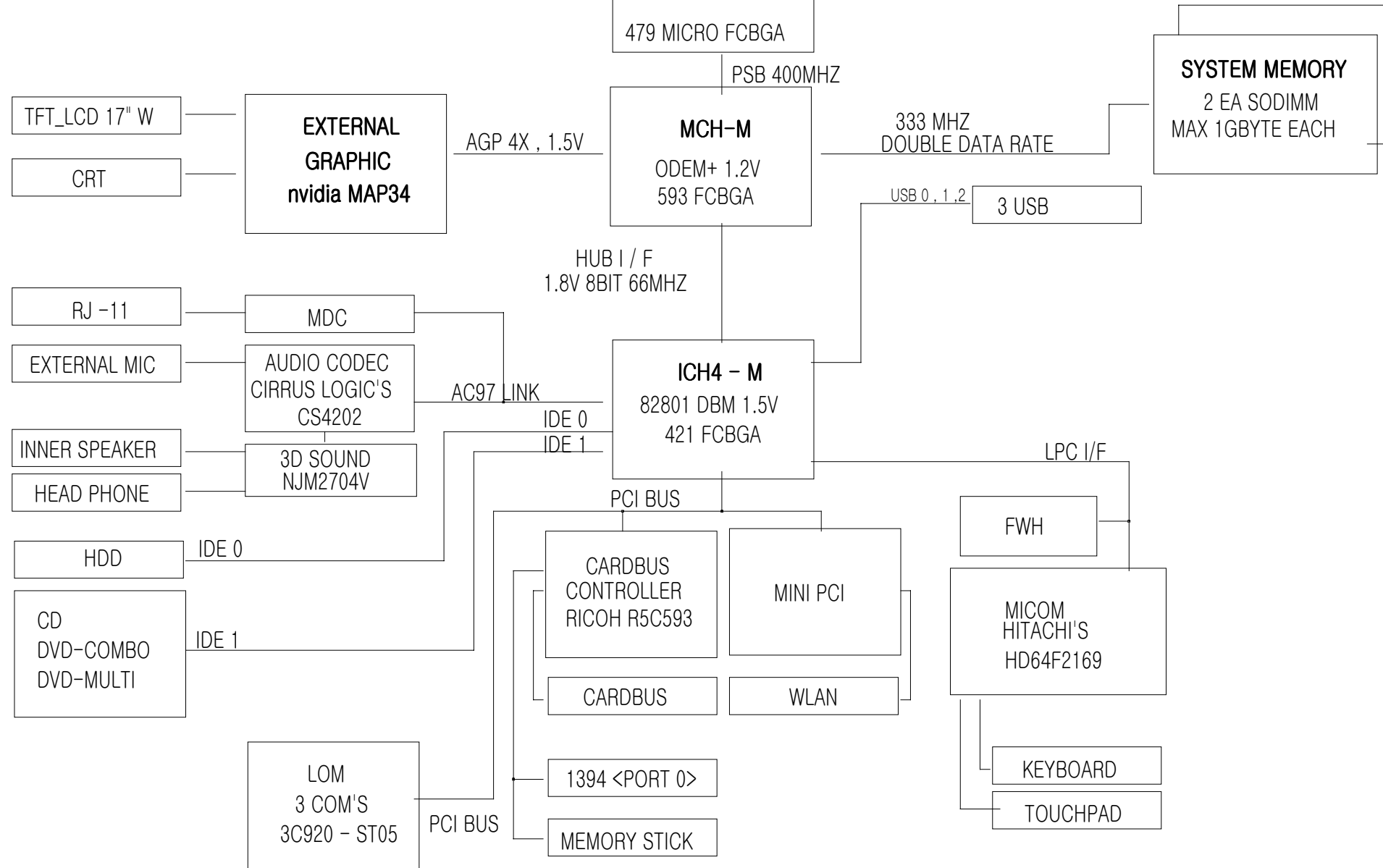
CPU : BANIAS/DOTHAN  
Chip Set : MCH-M ODEM+  
Remarks : TEMP

Model Name : CICHLID MAIN  
PBA Name : BA92-02649A  
PCB Code : BA41-00392A  
Dev. Step : MP  
Revision : 1.0

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3. BOARD INFORMATION --(SHEET3)  
4. CLOCK GENERATOR --(SHEET4)  
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DRAW	CHECK	APPROVAL

DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHLID	SAMSUNG
CHECK	H.S, OH	DEV. STEP	MP			ELECTRONICS
APPROVAL	H.S, KIM	REV	1.0	COVER		PART NO. BA41-00392A
MODULE CODE		LAST EDIT	March, 30, 2004 10:12:30 AM	PAGE	1 OF	41



DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHLID	SAMSUNG
CHECK	H.S., OH	DEV. STEP	MP			ELECTRONICS
APPROVAL	H.S., KIM	REV	1.0		BLOCK DIAGRAM	PART NO. BA41-00392A
MODULE CODE		LAST EDIT	March, 30, 2004 10:13:05 AM	PAGE	2 OF 41	

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD19	0	A,B,C
LAN	AD21	3	D
MiniPCI SLOT1	AD23	2	E,F
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
AGP	AD17(internal)	-	A,B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
PCI SLOT	AD20	-	A,B,C,D

CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V
0	0	0	0	0	1	1.676 V	1	0	0	0	1	0	1.164 V
0	0	0	0	0	1	1.660 V	1	0	0	0	1	1	1.148 V
0	0	0	0	1	0	1.644 V	1	0	0	1	0	0	1.132 V
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V
0	0	1	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V
0	0	1	1	1	0	1.500 V	1	0	1	1	0	1	0.988 V
0	0	1	1	1	1	1.484 V	1	0	1	1	1	0	0.972 V
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V
0	1	0	1	1	0	1.372 V	1	1	0	1	1	0	0.860 V
0	1	0	1	1	1	1.356 V	1	1	0	1	1	1	0.844 V
0	1	0	1	1	1	1.340 V	1	1	0	1	1	1	0.828 V
0	1	0	1	1	1	1.324 V	1	1	1	0	0	0	0.812 V
0	1	0	1	1	1	1.308 V	1	1	1	0	0	1	0.796 V
0	1	1	0	0	0	1.292 V	1	1	1	0	1	0	0.780 V
0	1	1	0	0	1	1.276 V	1	1	1	0	1	1	0.764 V
0	1	1	0	1	0	1.260 V	1	1	1	0	1	1	0.748 V
0	1	1	1	0	0	1.244 V	1	1	1	1	0	0	0.732 V
0	1	1	1	0	1	1.228 V	1	1	1	1	1	0	0.716 V
0	1	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for BANIAS CPU (1.356 - 0.844V)
VCCP	BANIAS/ODEM Processor System Bus(PSB) Termination (1.05V)
VCC_MCH	MCH-M Core Voltage (1.2V)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
P2.5V_AUX	2.5V power rail (off in S4-S5)
P1.25V_AUX	1.25V power rail (off in S4-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P3.3V_ALWAYS	3.3V always on Power Rail
P5V	5.0V switched power rail (off in S3-S5)
P5V_ALWAYS	5.0V always on power
P12V	12.0V switched power rail (off in S3-S5)

IC / SMB Address

Devices	Address	Hex	Bus
ICH4	-	-	-
ADM1032(CPU Thermal Sensor)	1001 110x	9Ch	SMBUS Master Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001x	A2h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1	SYSTEM PORT B
2	SYSTEM PORT C
3	FINGER PRINT
4	BLUETOOTH

System Power States

CHP3\_SLPS1\* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.

CHP3\_SLPS3\* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.

CHP3\_SLPS4\* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.

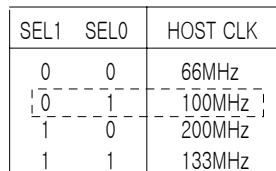
CHP3\_SLPS5\* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

REVISION HISTORY

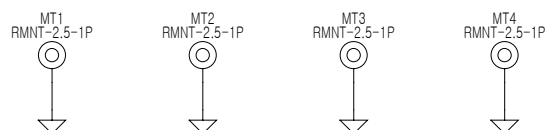
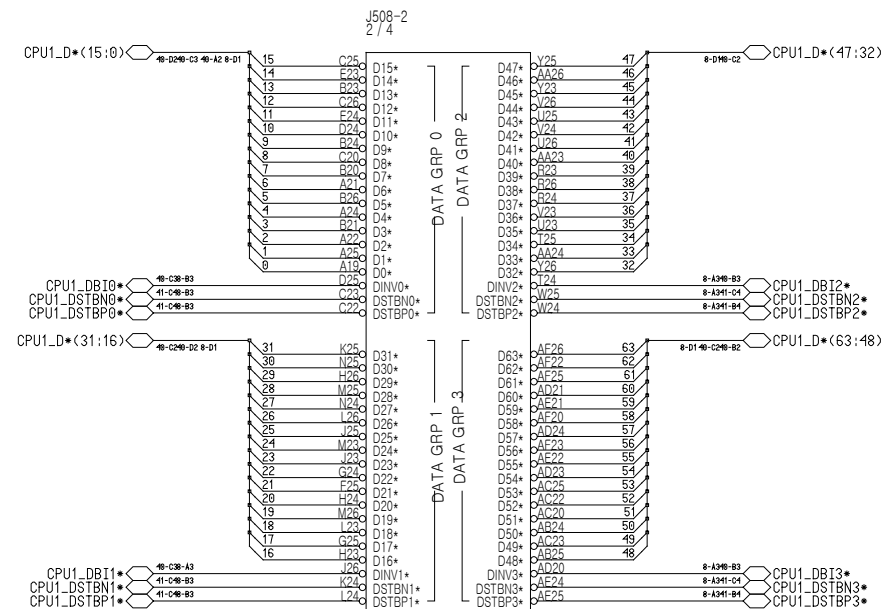
See rev notes in the changes file for more information.

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APPROVAL		H.S, KIM		REV	1.0				BOARD INFORMATION	PART NO.	BA41-00392A		
MODULE CODE				LAST EDIT				March, 30, 2004 10:13:36 AM		PAGE	3	OF	41

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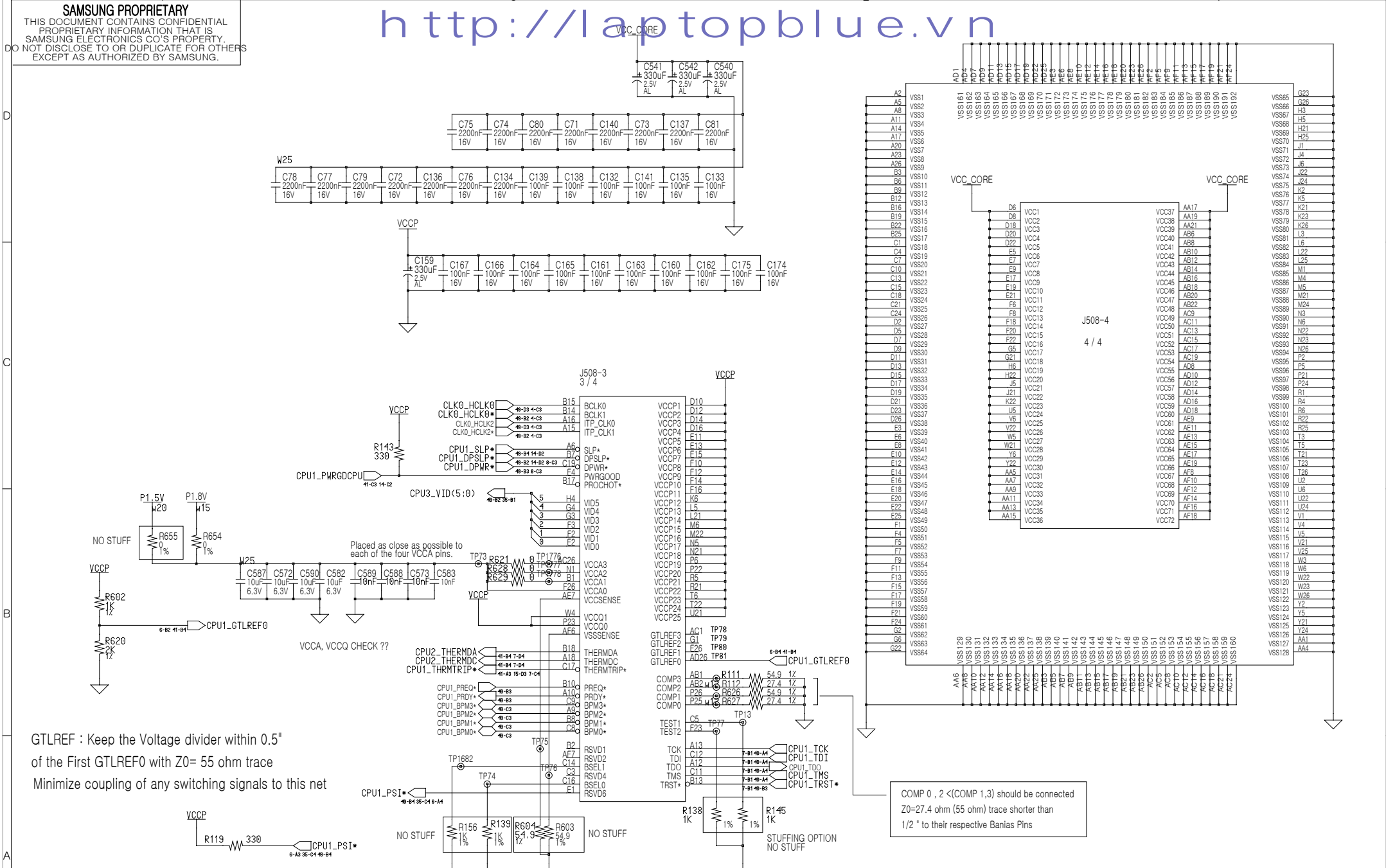
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d:/users/mobile15/mentor/cichlid_or/main11
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COM-22C-015(1996.6.5) REV. 3

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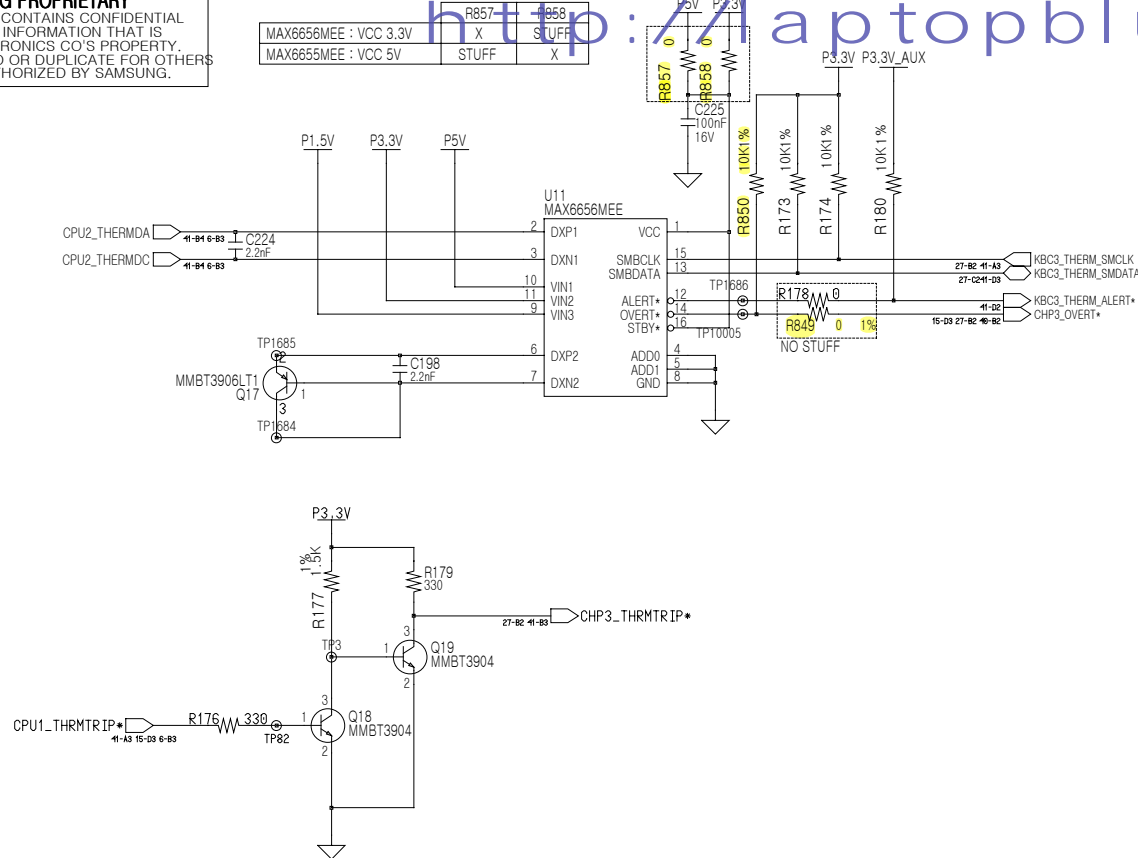


GTLREF : Keep the Voltage divider within 0.5"  
of the First GTLREF0 with Z0= 55 ohm trace  
Minimize coupling of any switching signals to this net

COMP 0 , 2 <(COMP 1,3) should be connected  
Z0=27.4 ohm (55 ohm) trace shorter than  
1/2 " to their respective Banias Pins

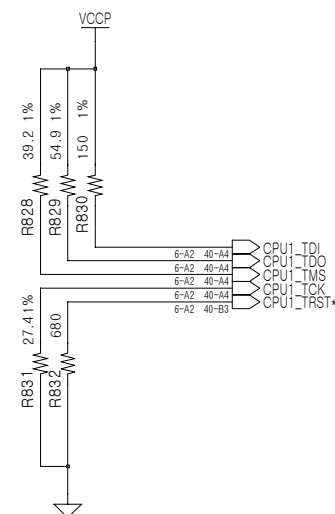
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MODULE CODE		LAST EDIT		March, 30, 2004 10:14:48 AM	PAGE	6 OF 41


MAX6656MEE : VCC 3.3V	R857 X	R858 STUFF
MAX6655MEE : VCC 5V	STUFF	X



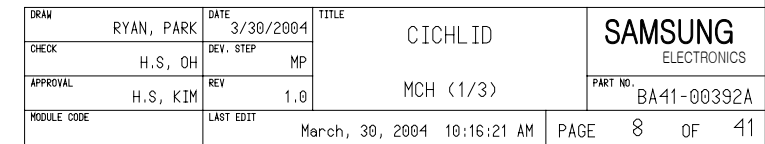
VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V
0	0	0	0	0	1	1.676 V	1	0	0	0	1	0	1.164 V
0	0	0	0	0	1	1.660 V	1	0	0	0	1	1	1.148 V
0	0	0	0	1	0	1.644 V	1	0	0	1	0	0	1.132 V
0	0	0	0	1	0	1.628 V	1	0	0	1	0	1	1.116 V
0	0	0	0	1	0	1.612 V	1	0	0	1	1	0	1.100 V
0	0	0	1	1	1	1.596 V	1	0	1	1	1	1	1.084 V
0	0	0	1	0	0	1.580 V	1	0	1	0	0	0	1.068 V
0	0	0	1	0	0	1.564 V	1	0	1	0	0	1	1.052 V
0	0	0	1	0	1	1.548 V	1	0	1	0	1	0	1.036 V
0	0	0	1	0	1	1.532 V	1	0	1	0	1	1	1.020 V
0	0	0	1	1	0	1.516 V	1	0	1	1	0	0	1.004 V
0	0	0	1	1	0	1.500 V	1	0	1	1	0	0	0.988 V
0	0	0	1	1	1	1.484 V	1	0	1	1	1	0	0.972 V
0	0	0	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V
0	0	1	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V
0	0	1	0	0	0	1.436 V	1	1	0	0	0	1	0.924 V
0	0	1	0	0	1	1.420 V	1	1	0	0	1	0	0.908 V
0	0	1	0	0	1	1.404 V	1	1	0	0	1	1	0.892 V
0	0	1	0	1	0	1.388 V	1	1	0	0	1	0	0.876 V
0	0	1	0	1	0	1.372 V	1	1	0	0	1	0	0.860 V
0	0	1	0	1	1	1.356 V	1	1	0	0	1	1	0.844 V
0	0	1	0	1	1	1.340 V	1	1	0	0	1	1	0.828 V
0	0	1	1	0	0	1.324 V	1	1	1	0	0	0	0.812 V
0	0	1	1	0	0	1.308 V	1	1	1	0	0	1	0.796 V
0	0	1	1	0	1	1.292 V	1	1	1	0	1	0	0.780 V
0	0	1	1	0	1	1.276 V	1	1	1	0	1	1	0.764 V
0	0	1	1	1	0	1.260 V	1	1	1	0	1	1	0.748 V
0	0	1	1	1	0	1.244 V	1	1	1	1	0	0	0.732 V
0	0	1	1	1	1	1.228 V	1	1	1	1	1	0	0.716 V
0	0	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND

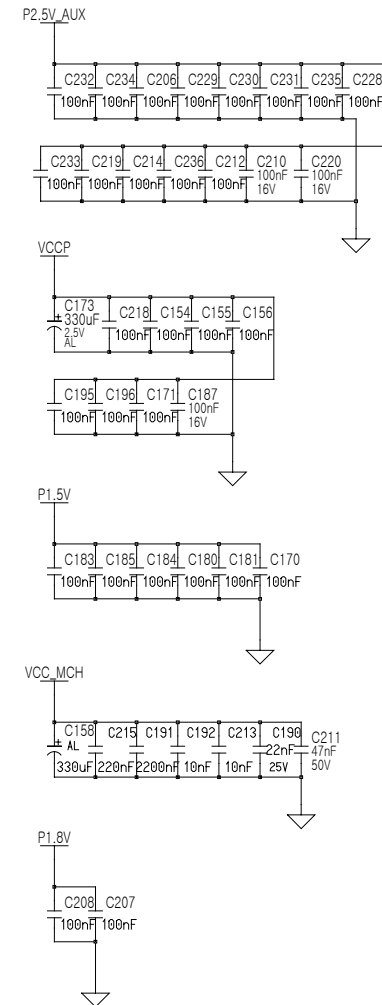


DRAW	KI. 1M	DATE	4/7/2003	TITLE  AQUILA W MAIN THERMAL SENSOR & VID			
CHECK	KK. BIN	DEV. STEP	DV				
APPROVAL	DW. KIM	REV	1.0				
MODULE CODE		LAST EDIT	April 7, 2003 8:36:31 AM			PAGE	7
				PART NO.		BA41-#####	

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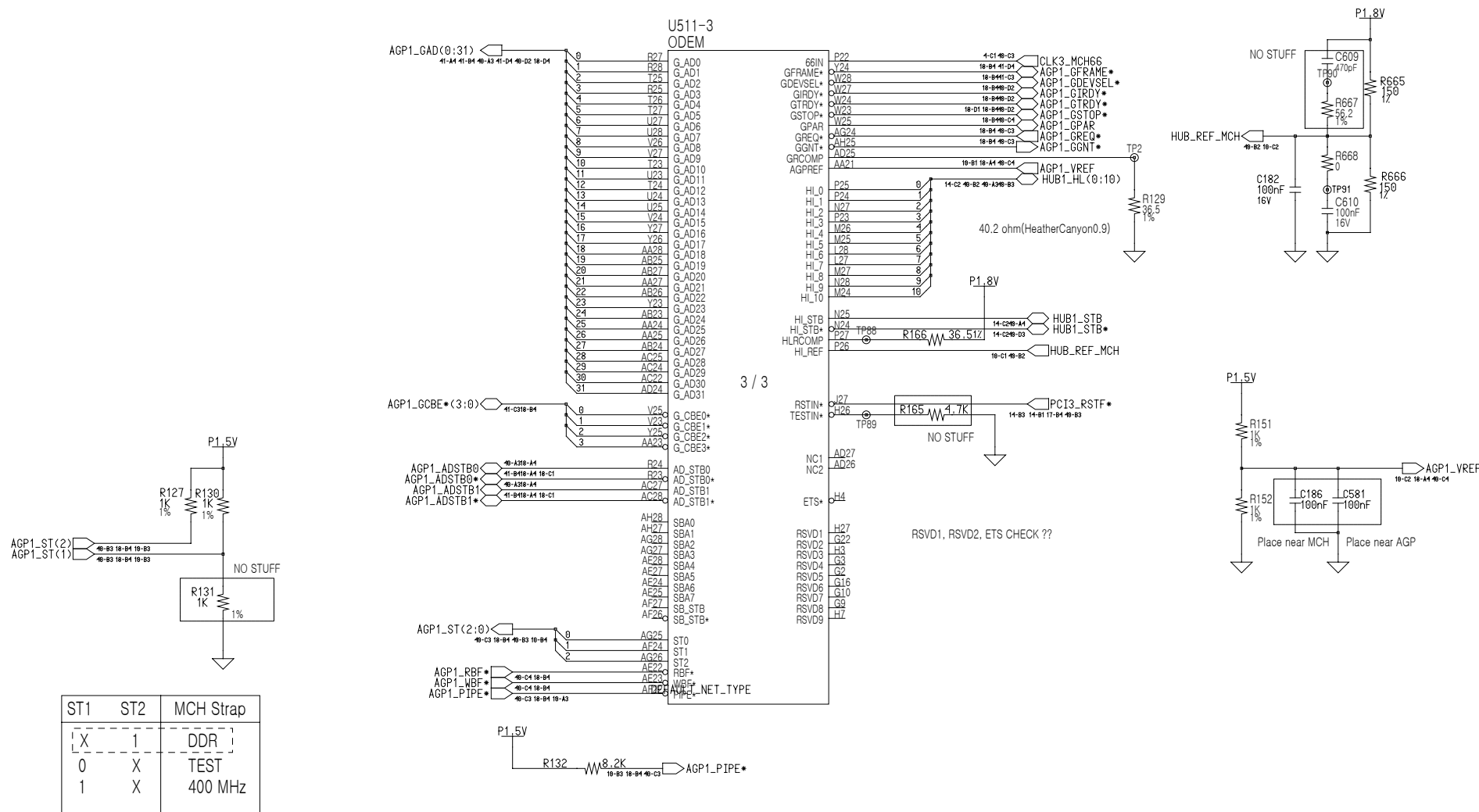





MCH signal ball to signal Via = Max 40 mil  
MCH output signal via to input signal via = 95mil ~ 105 mil  
RCVEN Sinal must be routed on the same layer as the memory clocks.

```
d:/users/mobile15/mentor/cichlid_or/main11
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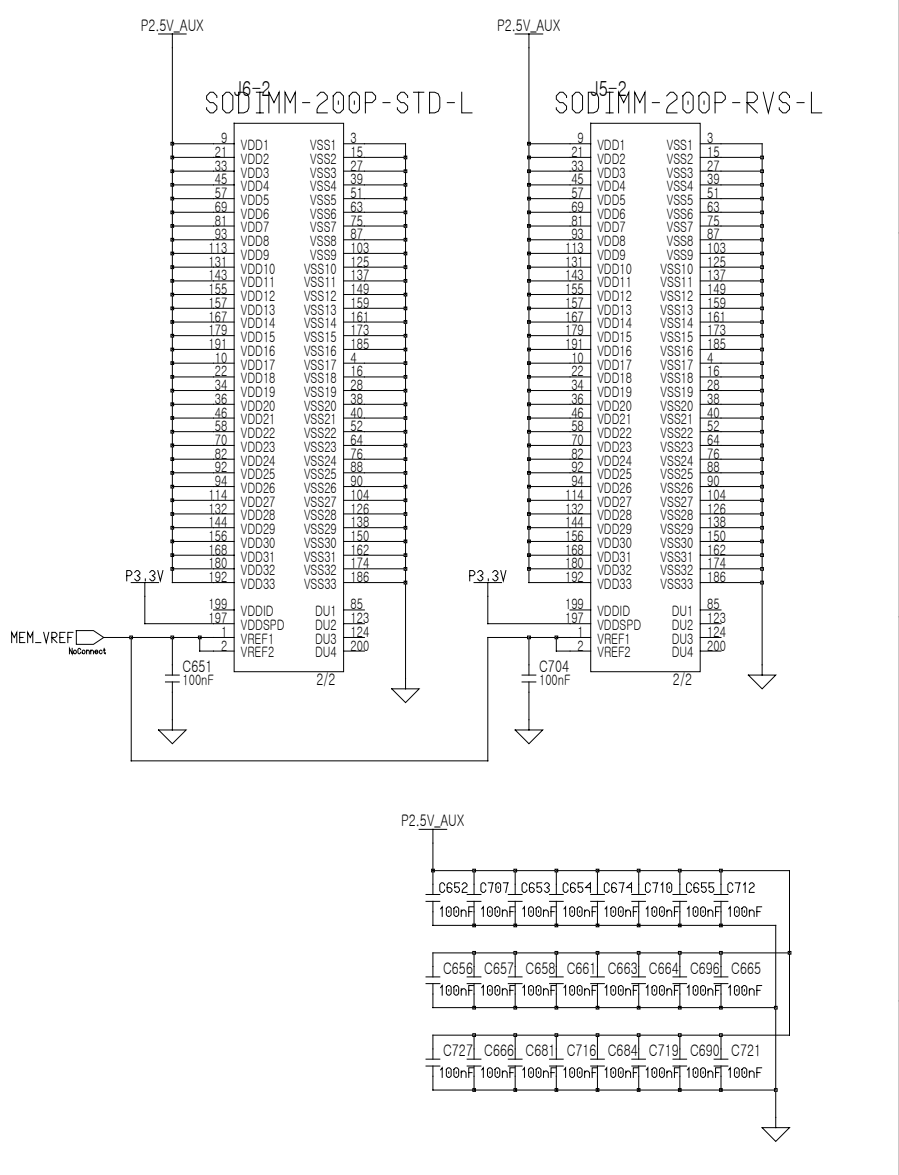
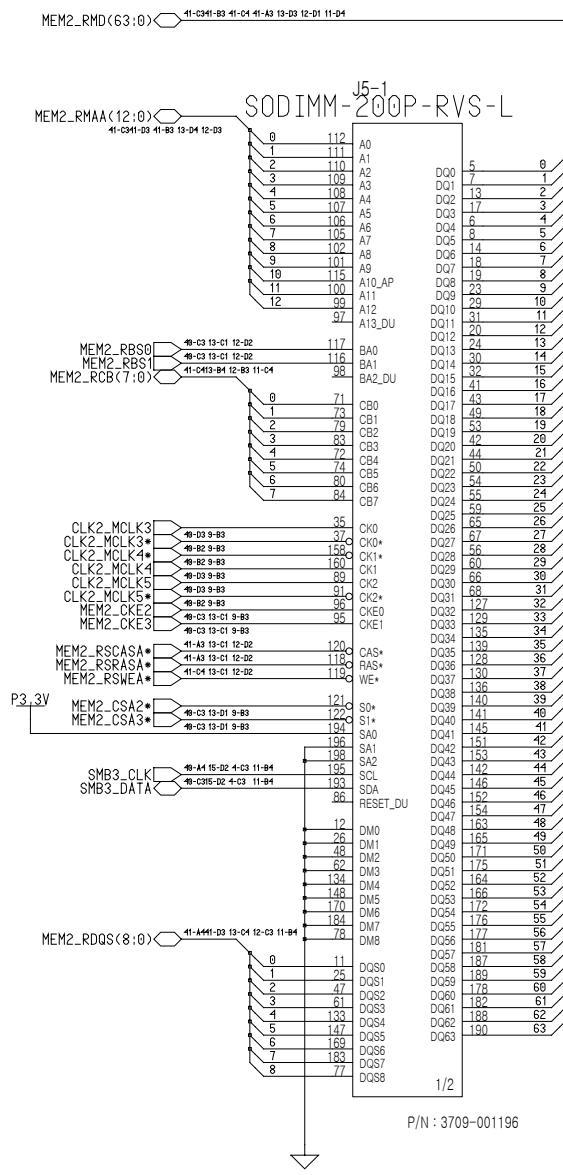
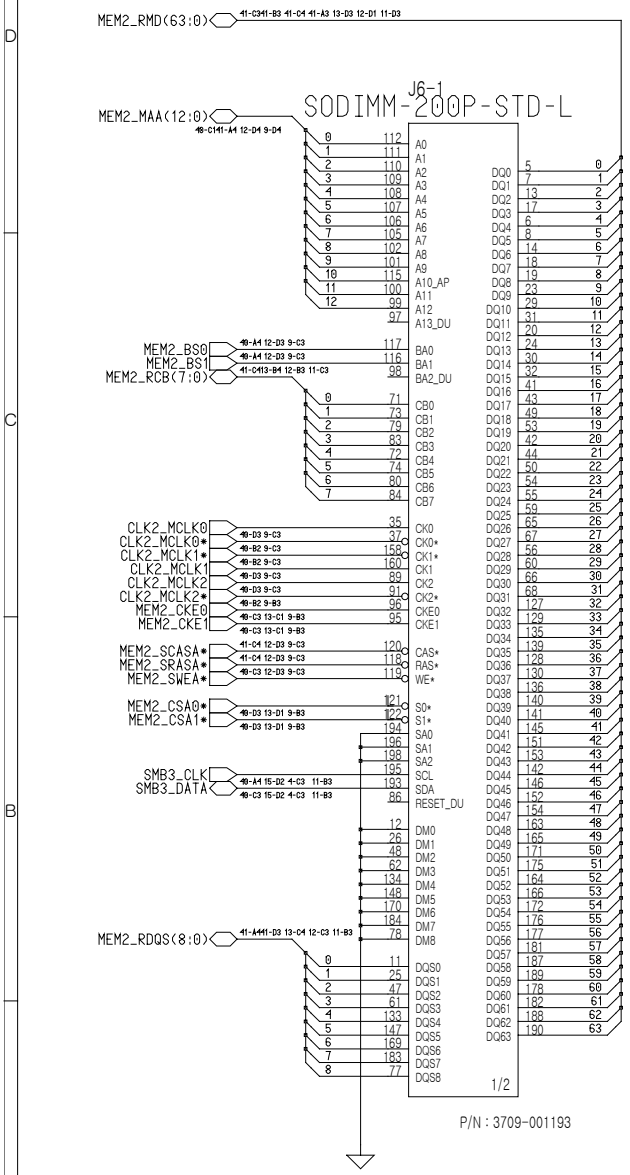
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ST1	ST2	MCH Strap
X	1	DDR
0	X	TEST
1	X	400 MHz

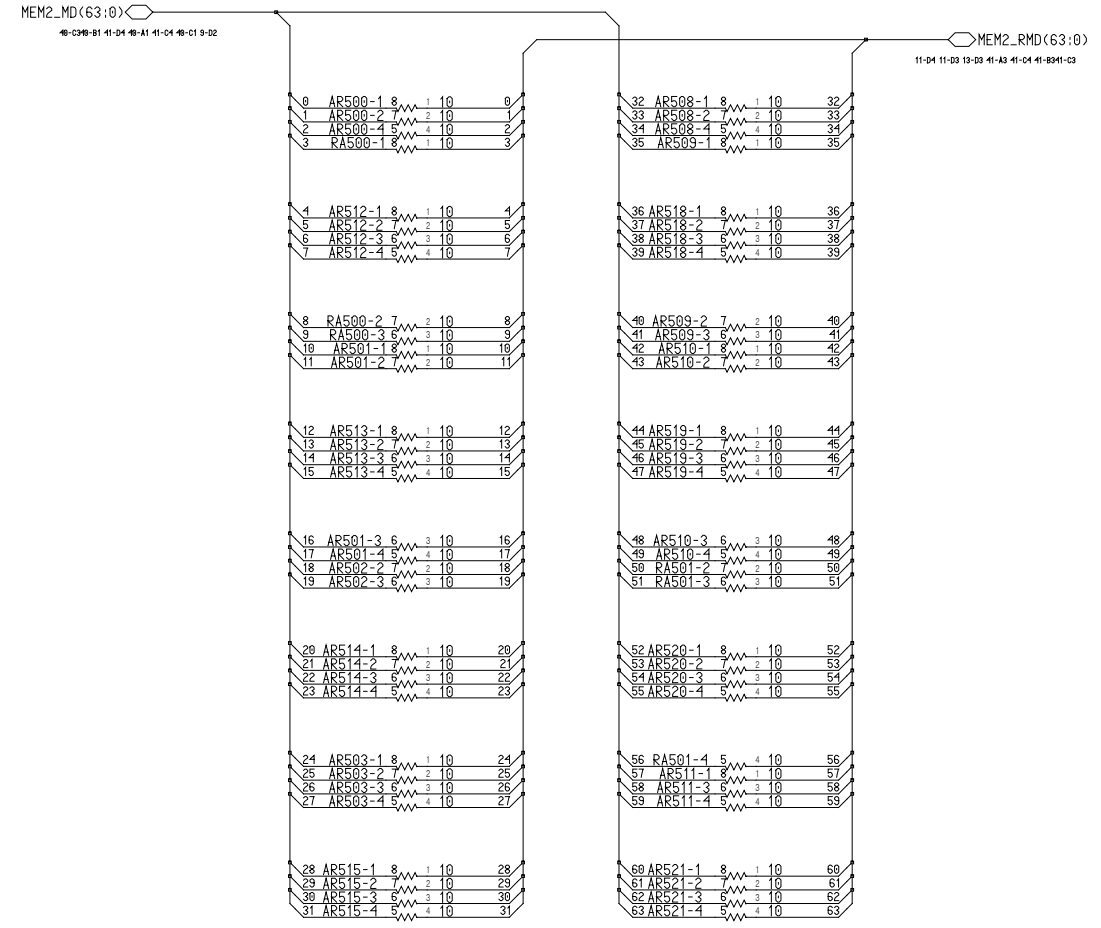
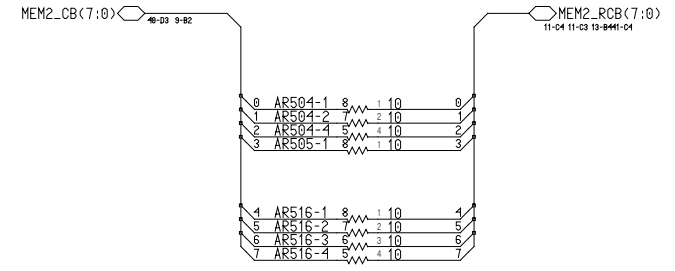
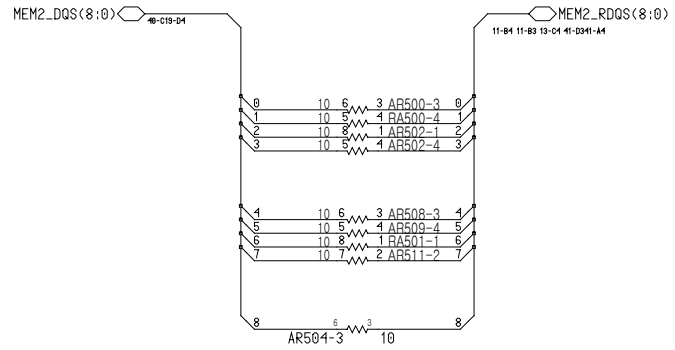
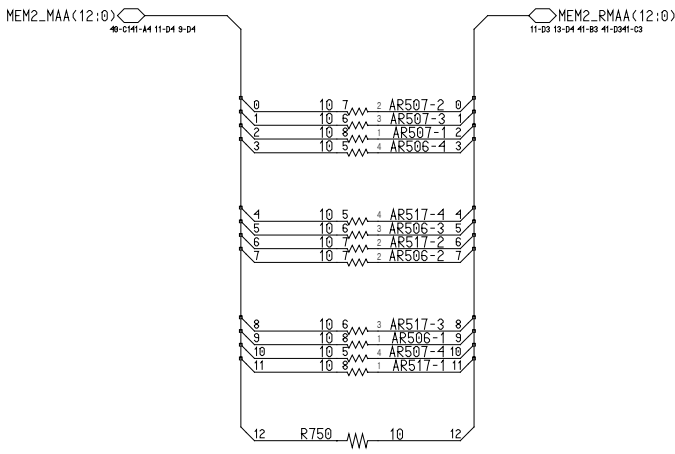
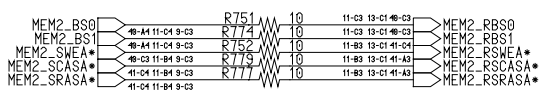
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CHECK		H.S., OH		DEV. STEP	MP						PART NO.	
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MODULE CODE				LAST EDIT		March, 30, 2004 10:19:07 AM			PAGE		10 OF 41	

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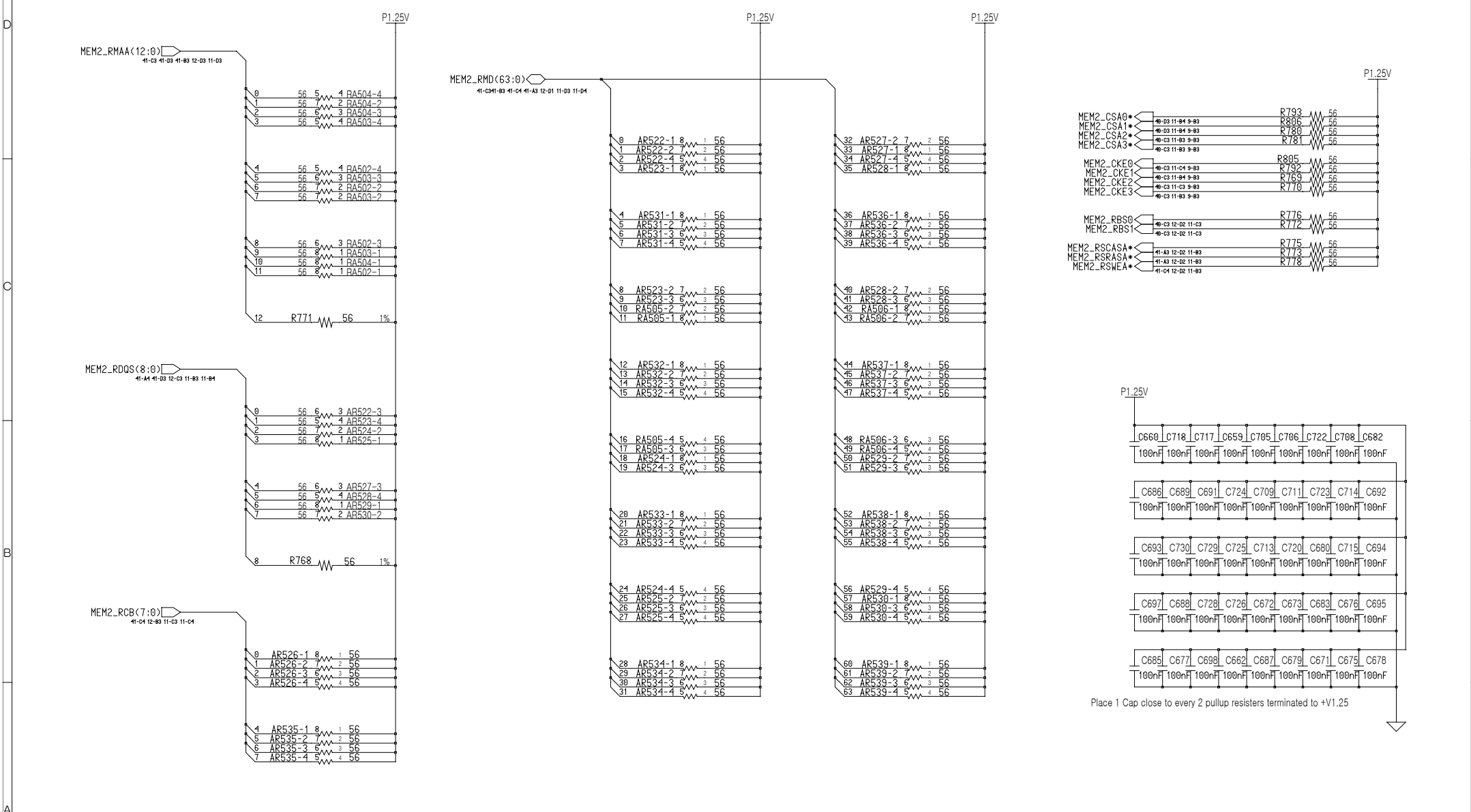
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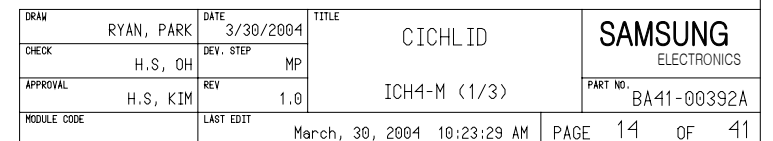
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APPROVAL	H.S, KIM	REV	1.0	DDR S-TERMINATION		PART NO. BA41-00392A
MODULE CODE		LAST EDIT	March, 30, 2004 10:21:51 AM	PAGE	12 OF 41	

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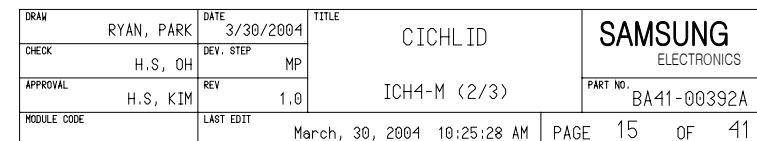
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MODULE CODE		LAST EDIT	March, 30, 2004 10:23:05 AM	PAGE	13	OF 41

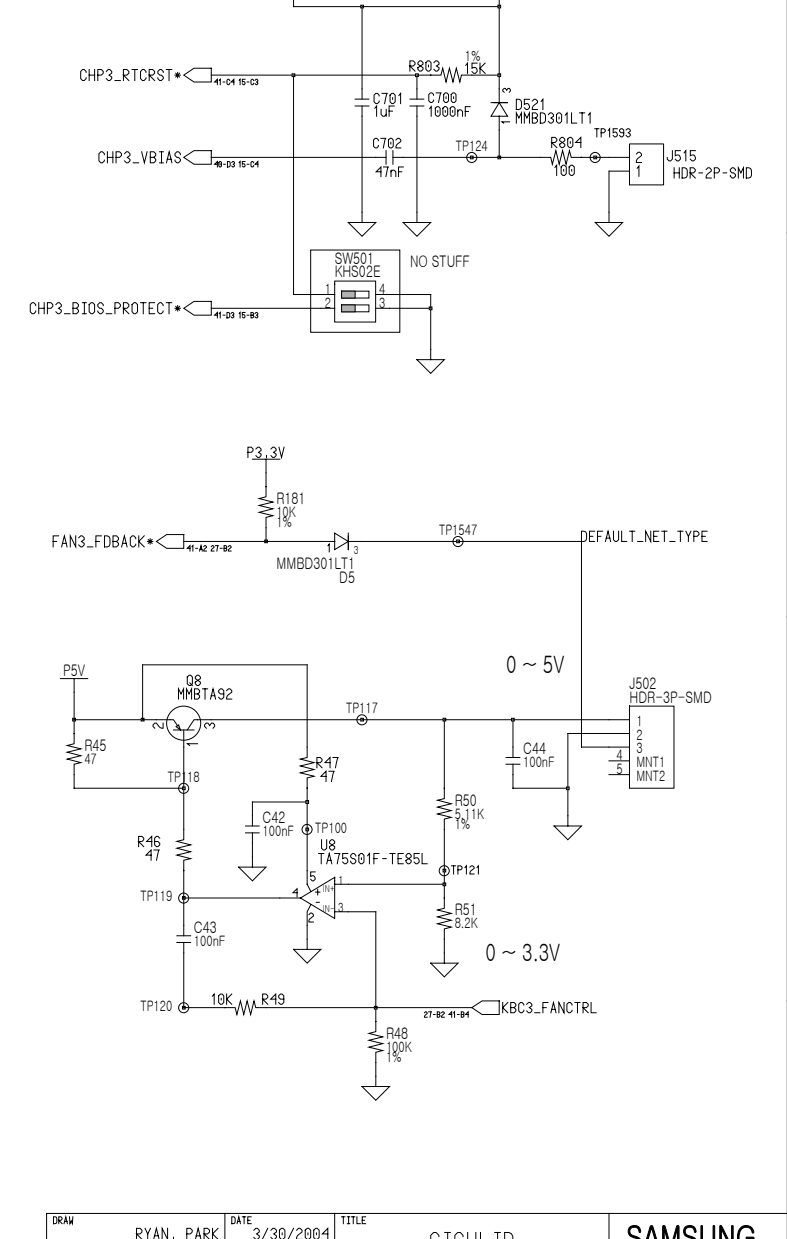






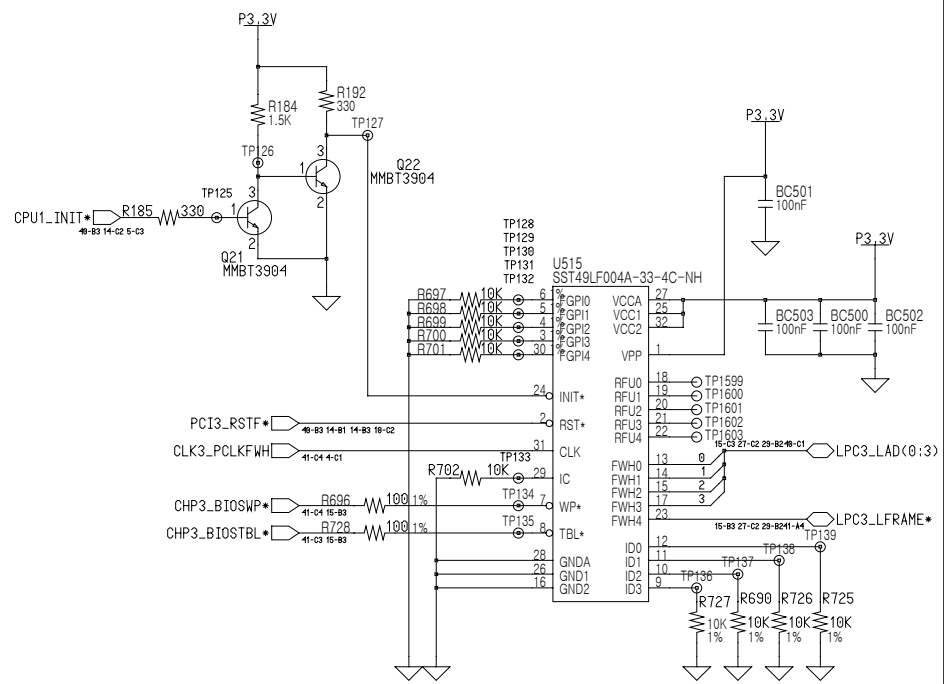
Primary CODEC : AUDIO  
Secondary CODEC : MODEM





DRAW		RYAN, PARK	DATE	3/30/2004	TITLE	CICHLID	SAMSUNG ELECTRONICS		
CHECK	H.S., OH	DEV. STEP	MP						
APPROVAL	H.S., KIM	REV	1.0	ICH4-M (3/3)				PART NO.	BA41-00392A
MODULE CODE		LAST EDIT						March, 30, 2004 10:25:57 AM	PAGE

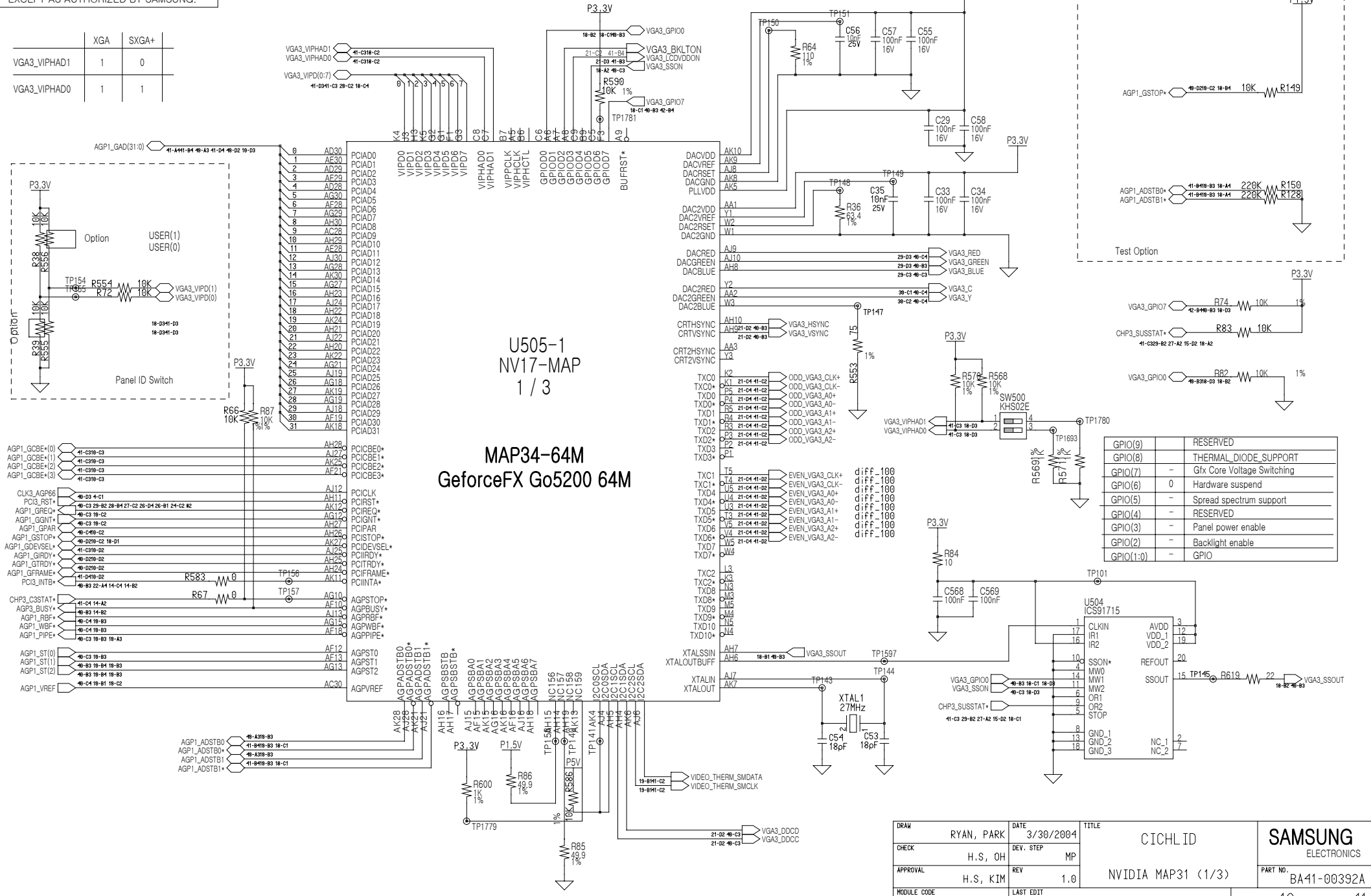


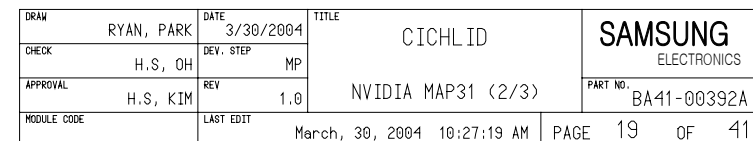


- |    |                                    |    |                                 |
|----|------------------------------------|----|---------------------------------|
| 02 | VERIFY REAL MODE                   | 66 | CONFIGURE ADVANCE CACHE REG.    |
| 03 | DISABLE NMI                        | 6A | DISPLAY EXTERNAL CACHE SIZE     |
| 04 | GET CPU TYPE                       | 6C | DISPLAY SHADOW MESSAGE          |
| 06 | INIT. SYSTEM H/W                   | 6E | DISPLAY NON-DISPOSABLE SEGMENT  |
| 08 | INIT. CHIPSET REG.                 | 70 | DISPLAY ERROR MESSAGE           |
| 09 | SET IN POST FLAG                   | 72 | CHECK FOR CONFIGURATION ERROR   |
| 0A | INIT CPU.REG                       | 74 | TEST REAL-TIME CLOCK            |
| 0B | CPU CACHE ON                       | 76 | CHECK FOR KEYBOARD EERROR       |
| 0C | INIT.CACHE TO POST                 | 7C | SETUP HARDWARE INTERRUPT VECTOR |
| 0E | INIT. I/O VALUE                    | 7E | TEST COPROCESSOR IF PRESENT     |
| 0F | ENABLE THE L-BUS IDE               | 80 | DISABLE ON-BOARD I/O PORT       |
| 10 | INIT. POWER MANAGER                | 82 | DETECT AND INSTALL EXT.RS232C   |
| 11 | LOAD ALTERNATE REG.                | 84 | DETECT AND INSTALL EXT.PARALLEL |
| 13 | PCI BUS MASTER RESET               | 86 | RE-INIT. ON-BOARD I/O PORT      |
| 14 | WITH INITIAL POST VALUE            | 88 | INIT. BIOS DATA ROM             |
| 16 | INIT. KEYBOARD CONTROLLER          | 8A | INIT.EXTENDED BIOS DATA AREA    |
| 18 | CHECK CHECKSUM                     | 8C | INIT. FDD CONTROLLER            |
| 1A | 8254 TIMER INIT.                   | 9A | SHADOW OPTION ROMS              |
| 1C | 8237 DMA CONTROLLER INIT.          | 9C | SETUP POWER MANAGEMENT          |
| 20 | RESET INTERRUPT CONTROLLER         | 9E | ENABLE H/W INTERRUPT            |
| 22 | TEST DRAM REFRESH                  | A0 | SET TIME OF DAY                 |
| 24 | TEST 8742 KEYBOARD CONTROLLER      | A4 | INIT. TYPEMATIC RATE            |
| 26 | SET ES SEGMENT REG. TO 4GB         | A8 | ERASE F2 PROMPT                 |
| 28 | ENABLE A20                         | AA | SCAN FOR F2 KEY STROKE          |
| 32 | AUTO SIZING DRAM                   | AC | ENTER SETUP                     |
| 34 | COMPUTE THE CPU SPEED              | AE | CLEAR IN POST FLAG              |
| 38 | TESET CMOS RAM                     | B0 | CHECK FOR ERRORS                |
| 3A | SHADOW SYSTEM BIOS ROM             | B2 | POST DONE-PREPARE TO BOOT O/S   |
| 3C | AUTO SIZING CACHE                  | B4 | ONE BEEP                        |
| 3D | CONFIGURE ADVANCED CHIPSET REG.    | B6 | CHECK PASSWORD (OPTION)         |
| 42 | LOAD ALTER REG. WITH CMOS VALUE    | B7 | ACPI INIT                       |
| 44 | INIT. INTERRUPT VECTOR             | BA | DMI INIT                        |
| 46 | INIT. BIOS INTERRUPT               | BE | CLEAR SCREEN                    |
| 47 | CHECK ROM COPYRIGHT NOTICE         | C0 | TRY BOOT WITH INT19             |
| 48 | INIT. I20 SUPPORT IF INSTALLED     | D0 | INTERRUPT HANDLER ERROR         |
| 49 | CHECK VIDEO CONFIGURE AGAINST CMOS | D2 | UNKNOWN INTERRUPT ERROR         |
| 4A | INIT. PCI BUS AND DEVICE           | D4 | PENDING INTERRUPT ERROR         |
| 4C | INIT. ALL VIDEO BIOS ROM           | D6 | SHUTDOWN 5                      |
| 50 | SHADOW VIDEO BIOS ROM              | D8 | SHUTDOWN ERROR                  |
| 52 | DISPLAY CPU TYPE AND SPEED         | DA | EXTENDED BLOCK MOVE             |
| 54 | TEST KEYBOARD                      | DC | SHUTDOWN 10                     |
| 56 | SET KEYCLICK IF ENABLED            | 89 | ENABLE NMI                      |
| 58 | ENABLE KEYBOARD                    | 90 | INIT. HDD CONTROLLER            |
| 5A | TEST FOR UNEXPECTED INTERRUPTS     | 91 | INIT. LOCAL BUS HDD CONTROLLER  |
| 5C | DISPLAY " PRESS ..... SETUP"       | 92 | JUMP TO USER PATCH 2            |
| 60 | TEST RAM BETWEEN 512K AND 640K     | 94 | DISABLE A20 ADDRESS LINE        |
| 62 | TEST EXTENDED MEMORY               | 96 | CLEAR HUGE ES SEGMENT REG.      |
| 64 | TEST EXTENDED MEMORY ADDRESS LINE  | 98 | SEARCH FOR OPTION ROMS          |
|    | JUMP TO USER PATCH 1               |    |                                 |

DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHLID	SAMSUNG
CHECK	H.S, OH	DEV. STEP	MP			ELECTRONICS
APPROVAL	H.S, KIM	REV	1.0	FIRMWARE HUB		PART NO.
MODULE CODE		LAST EDIT		March, 30, 2004 10:26:13 AM	PAGE 17	BA41-00392A
					OF 41	

	XGA	SXGA+
VGA3_VIPHAD1	1	0
VGA3_VIPHAD0	1	1



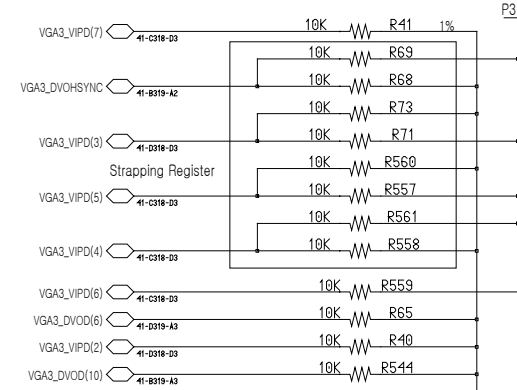
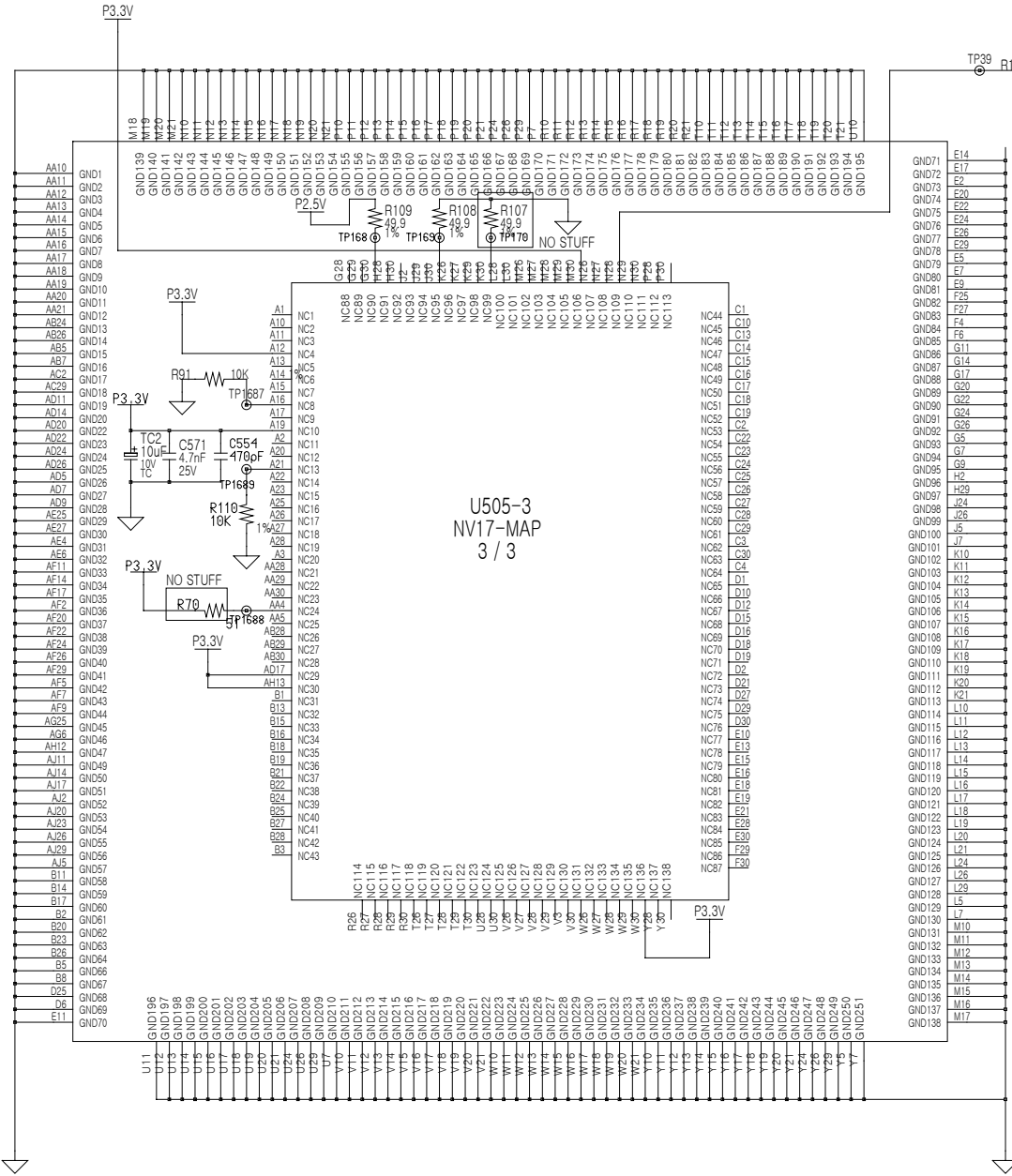


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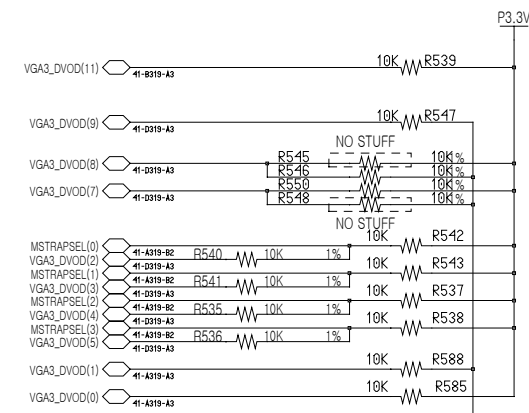
http://laptopblue.vn

Strapping Option

VPID(2):DVOD(10)	xx00	ROM Type ( 00 : Parallel )
DVOD(11)	xxx1	BUS Type ( 1 : AGP mode, 0 : PCI mode )
HSYNC_VIPD	0110	PCI_DEV_ID ( 0110 : NV17-MAP )
VPID(7)	xxx0	AGP Fastwrite ( 0 : Enable, 1 : Disable )
DVOD[9]	xxx0	AGP4X ( 0 : 4X enable, 1 : 4X disable )
DVOD[8:7]	xx01	TV Mode ( 01 : NTSC )
VPID(6):DVOD(6)	xx10	Crystal ( 10 : 27 MHz )
DVOD[5:2]	1101	RAM Cfg ( 1101 : 4Mx32 DDR SDRAM )
DVOD(1)	xxx0	Sub Vendor ( 0 : System BIOS, 1 : Adapter BIOS )
DVOD(0)	xxx1	PCI_AD_Swap ( 1 : Normal, 0 : Reverse )



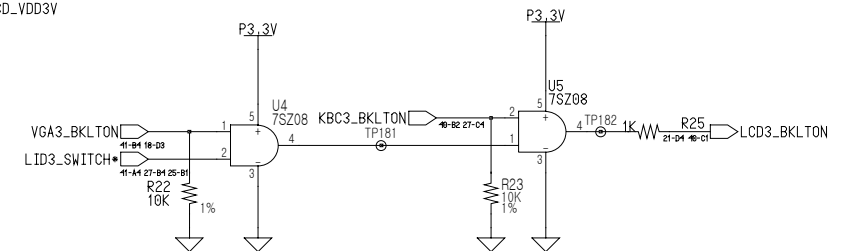
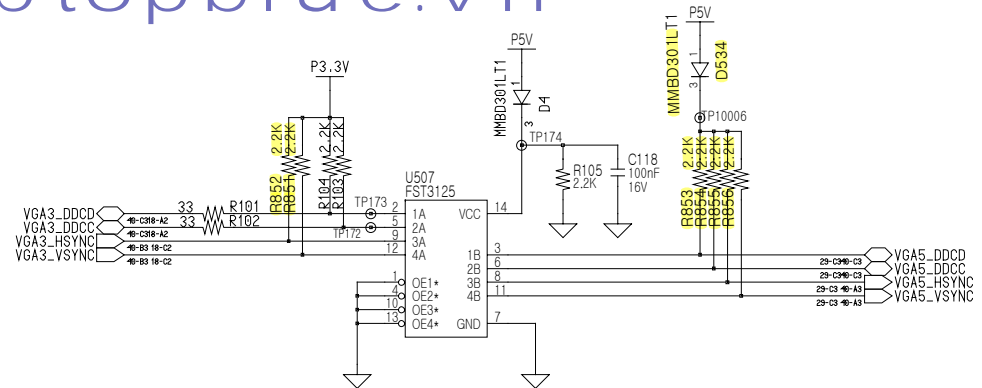
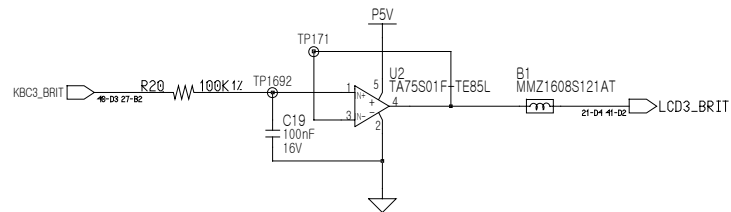
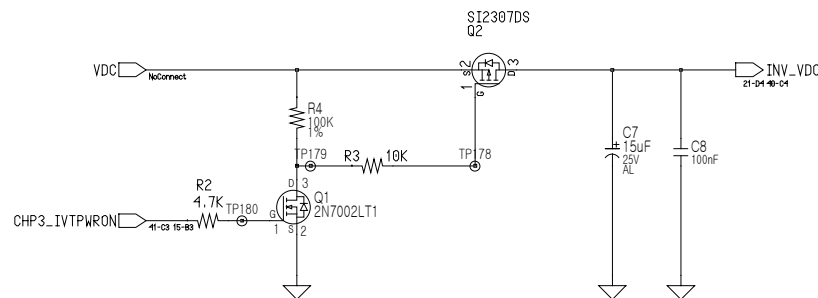
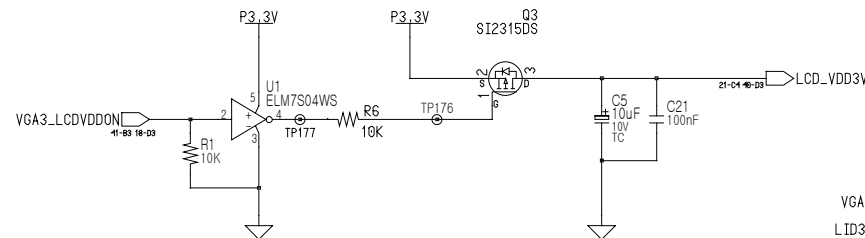
	32MB	64MB	MAP34
VGA3_DVOHSYNC	LOW	HIGH	HIGH
VGA3_VIPD(3)	HIGH	LOW	LOW
VGA3_VIPD(5)	HIGH	LOW	LOW
VGA3_VIPD(4)	LOW	HIGH	LOW



DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHL ID	SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0		NVIDIA MAP31 (3/3)	PART NO.
MODULE CODE		LAST EDIT				BA41-00392A
March, 30, 2004 10:27:42 AM						PAGE 20 OF 41

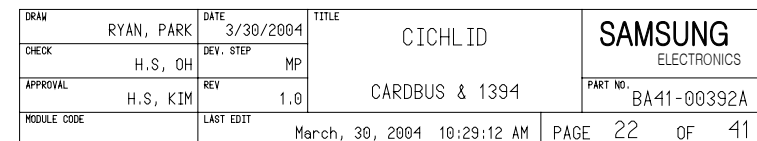
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	XGA	SXGA+
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VGA3_VIPHAD0	1	1

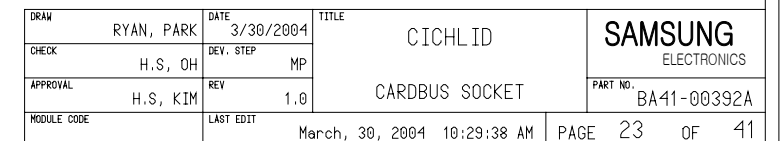


DRAM	KI. IM	DATE	4/7/2003	AQUILA W MAIN LCD_CONNECTOR	SAMSUNG ELECTRONICS
CHECK	KK. BIN	DEV. STEP	DV		
APPROVAL	DW. KIM	REV	1.0		
MODULE CODE	LAST EDIT		April 7, 2003 8:36:31 AM		
				PAGE	21 OF 42

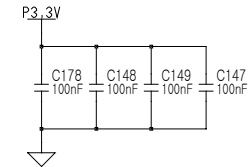
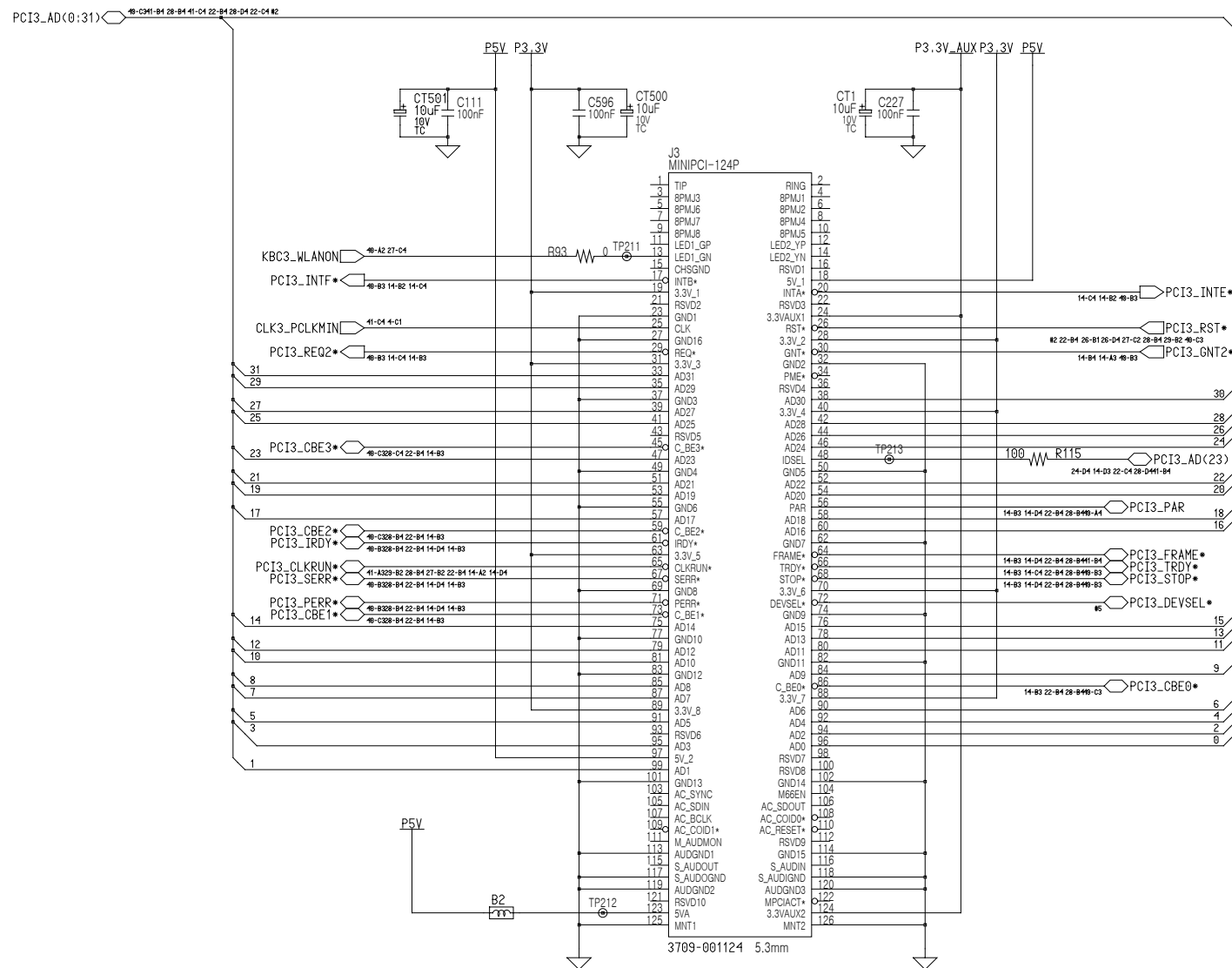
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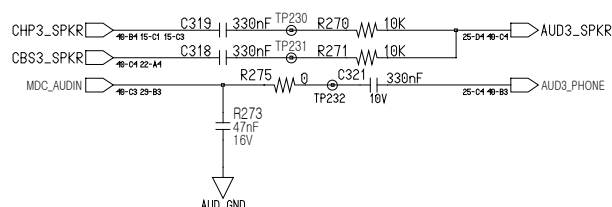
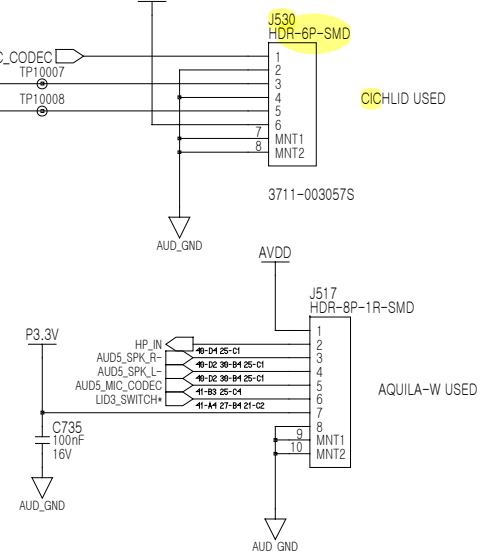
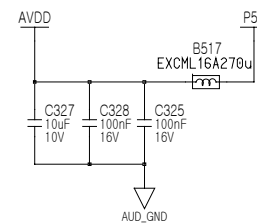
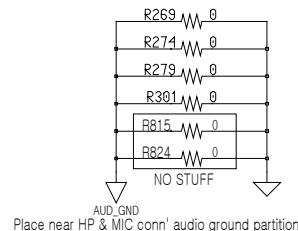
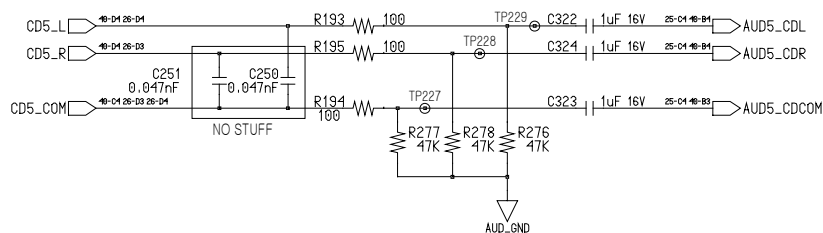
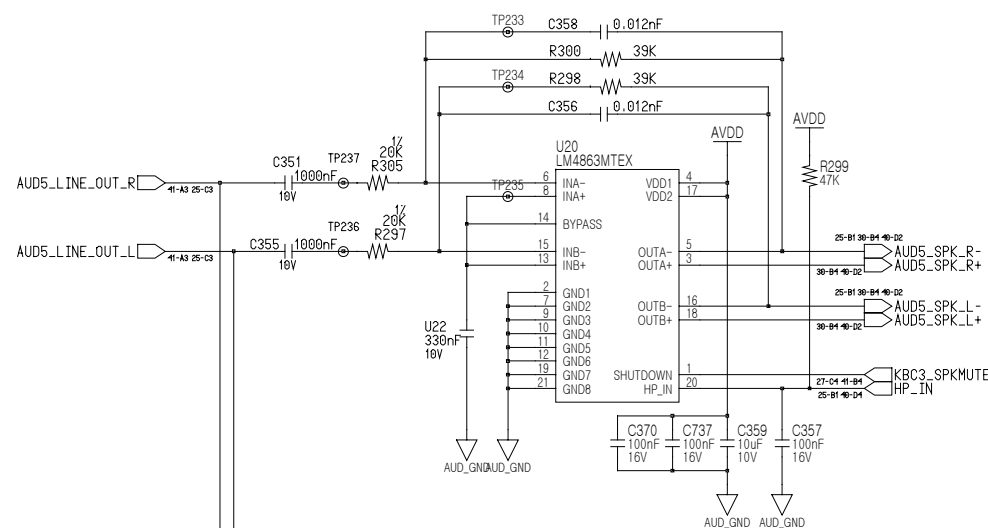
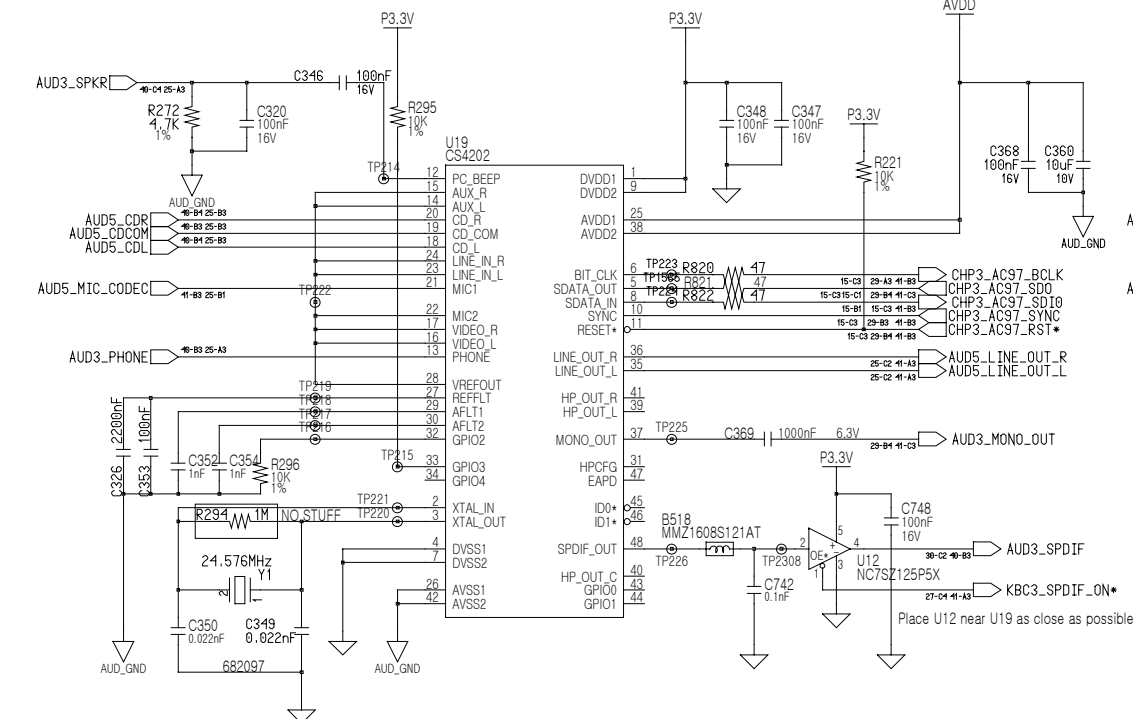
# MINIPCI



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MODULE CODE		LAST EDIT	March, 30, 2004 10:29:54 AM			BA41-00392A
				PAGE	24	OF 41



## Audio AMP



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CHECK	KI. IM	DEV. STEP	DV					
APPROVAL	KK. BIN	KEY	1.0					
MODULE CODE	DW. KIM	LAST EDIT		April 7, 2003 8:36:31 AM				
					PAGE	25	OF	42



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MICOM\_P3V

C605 100nF

C296 100nF

C606 100nF

PSV

K656

10K

10K

K655

KBC3\_RST\*

KBC3\_PWSM\*

41-23 32-04

41-42 27-42 27-01

MICOM\_P3V

R685 470K

R694 10K

C617 1uF

C618 330nF

41

PA0\_F

40

PA1\_F

39

PA2

38

PA3

37

PA4\_F

36

PA5

35

PA6

34

PA7\_F

33

KBC5\_TCLK

40-0389-B3

KBC5\_TDATA

40-A389-B3

120

KBC3\_EXTSMI\*

41-B4 14-B2

119

KBC3\_RUNSCI\*

41-B4 14-B2

118

KBC3\_SCLED\*

40-A2 30-B4

117

KBC3\_NUKLED\*

41-B4 30-B4

116

KBC3\_CAPSLED\*

41-C3 30-B4

115

KBC3\_LBLED\*

40-A3 30-A3

114

KBC3\_PWRGD\*

40-A3 22-B4 15-D4 15-D3

113

KBC3\_PWRON

42-D4 40-A3 37-A4 37-B1 34-C2 32-D2 31-C1 30-D2

94

KBC3\_SPDIF\_ON\*

41-A3 25-B3

93

KBC3\_SPKMUTE

41-B4 25-C1

92

KBC3\_BKLTON

40-B2 21-C1

91

KBC3\_WLANON

41-D2 24-D4

90

BLT3\_BT0N\_LED\*

41-B3 30-D4

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BLT3\_RF0N

40-B3 30-B3

88

87

KBC3\_LANPWRON

66

PD0

65

PD1

64

PD2

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PD3

62

PD4

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PD5

60

PD6

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PD7

41-D4 30-C3

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41-B3 30-C3

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29

4

28

5

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6

26

7

25

PE0\_F

PE1\_F

PE2

PE3

PE4

PE5

PE6

PE7\_F

0

50

1

49

2

48

3

47

4

46

5

45

6

44

7

43

PF0\_F

PF1\_F

PF2

PF3

PF4

PF5

PF6\_F

PF7\_F

8

58

9

57

10

56

11

55

12

54

13

53

14

52

15

51

PG0\_F

PG1\_F

PG2

PG3

PG4

PG5

PG6

PG7\_F

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1P240

144

682081

Y502

10MHz

NC

140

NC

141

X1

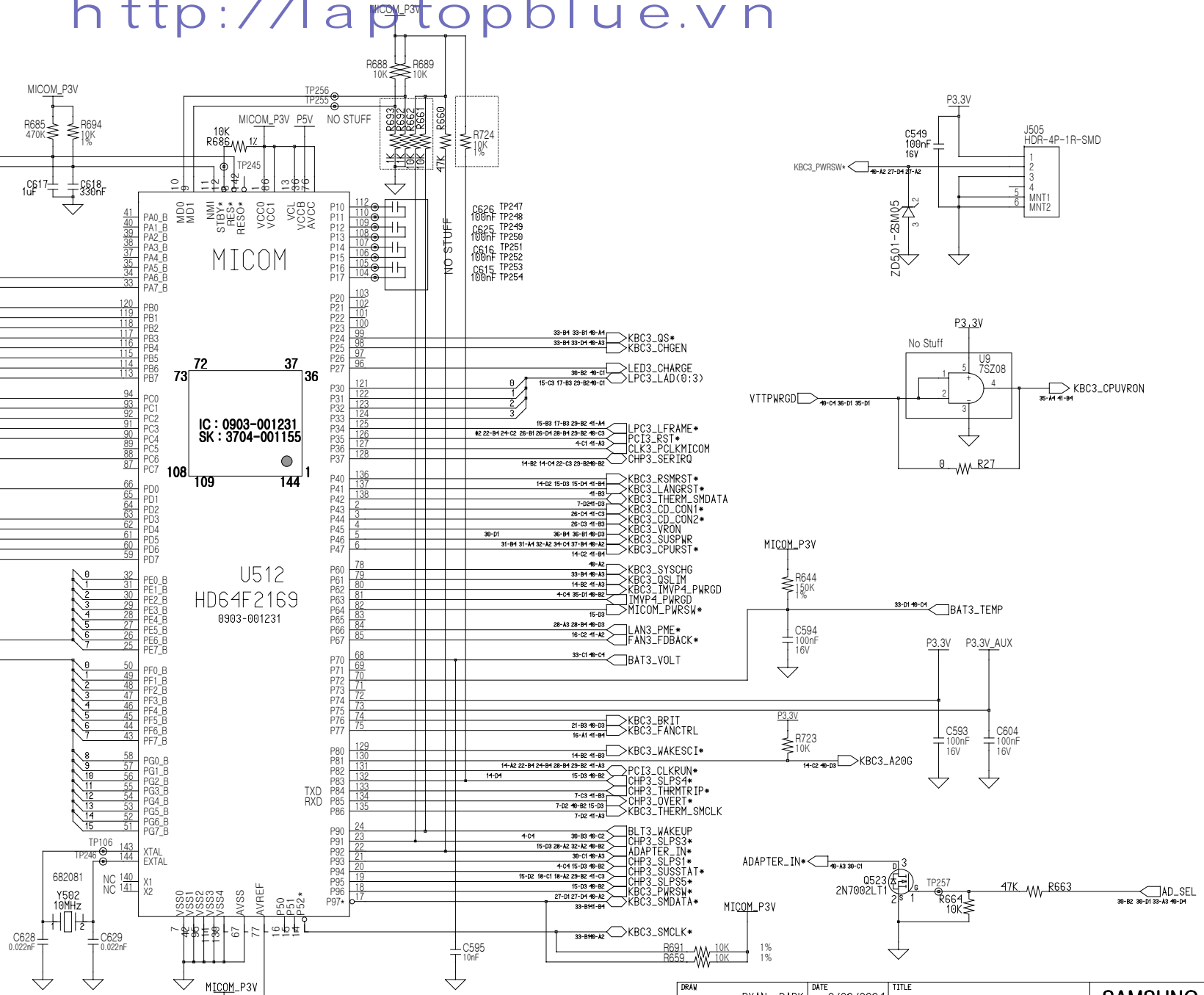
X2

C628 0.022nF

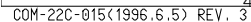
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XTAL

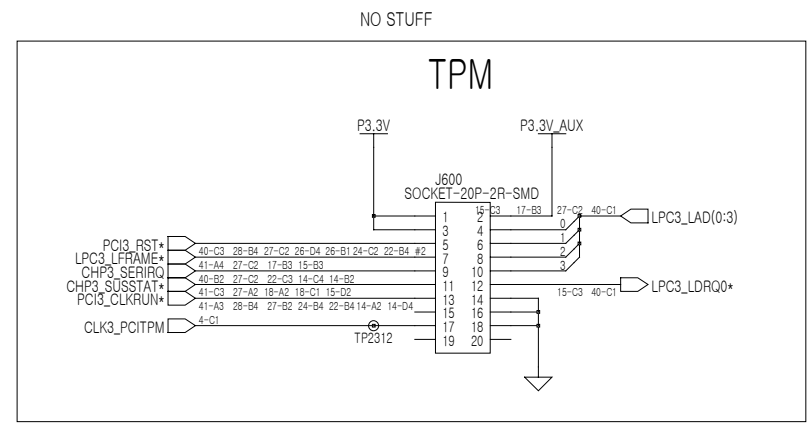
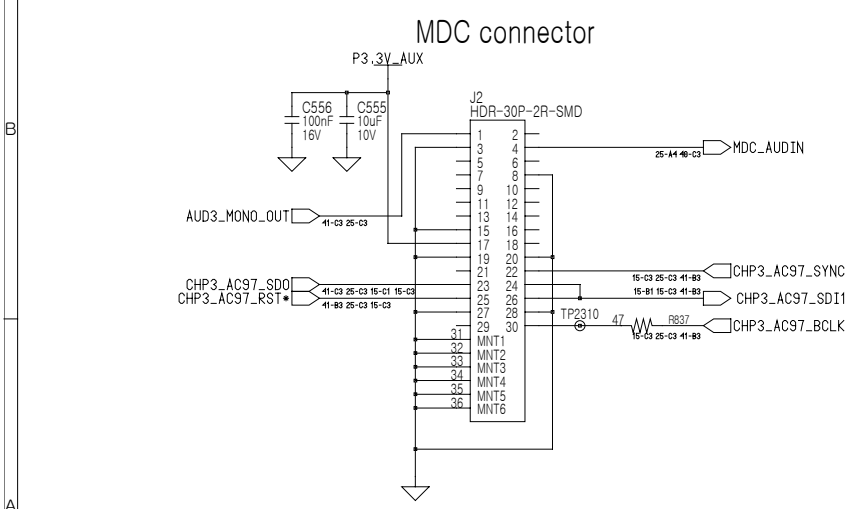
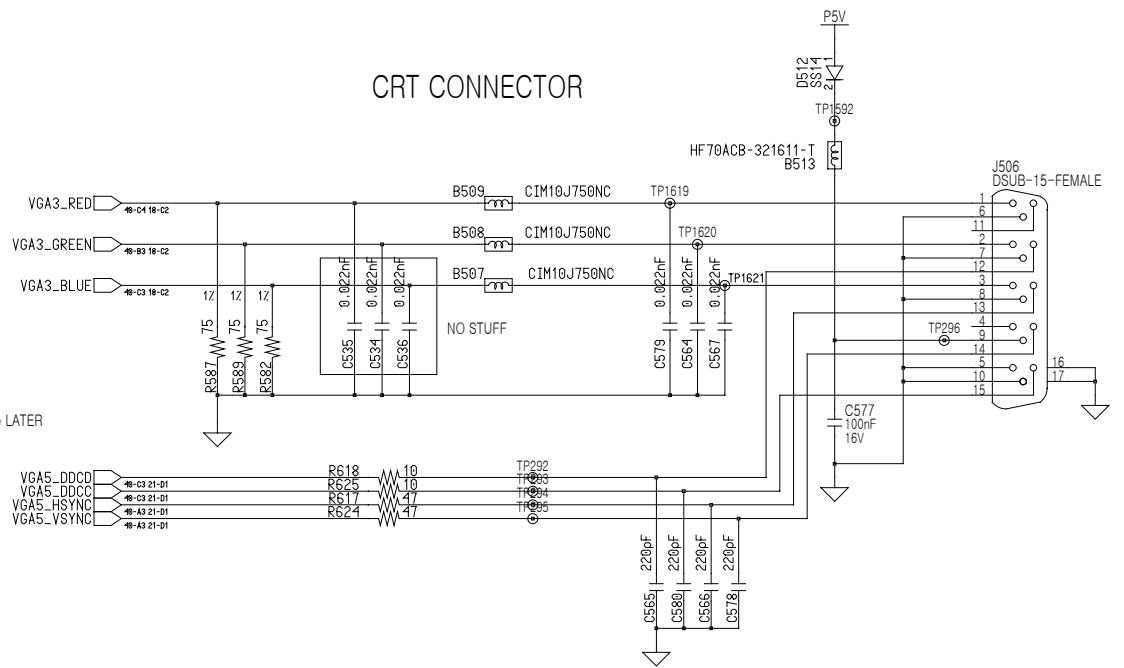
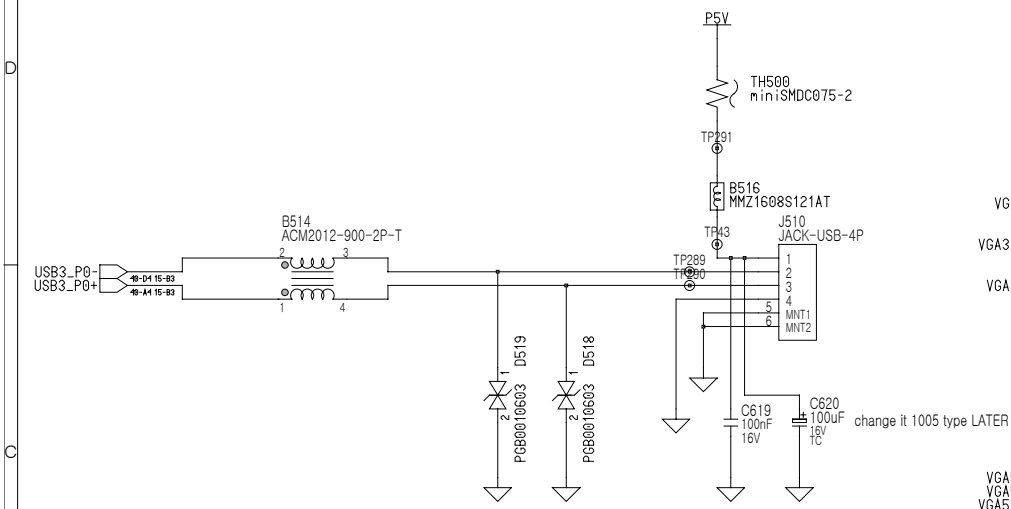


COM-22C-015(1996.6.5) REV. 3



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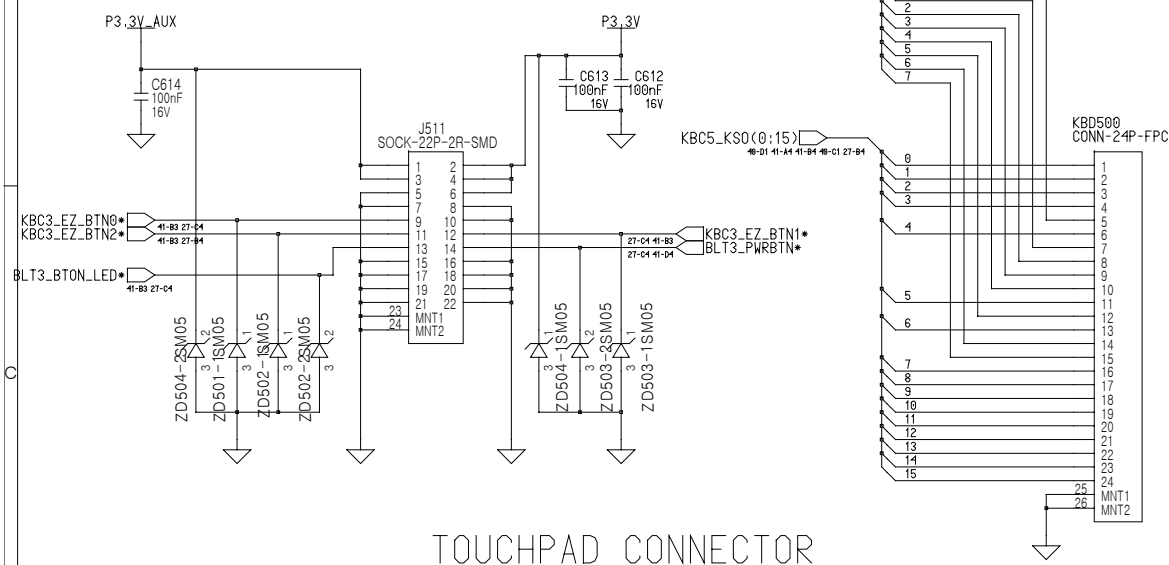
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MODULE CODE		LAST EDIT	March, 30, 2004 10:54:11 AM	PAGE	29	OF 41

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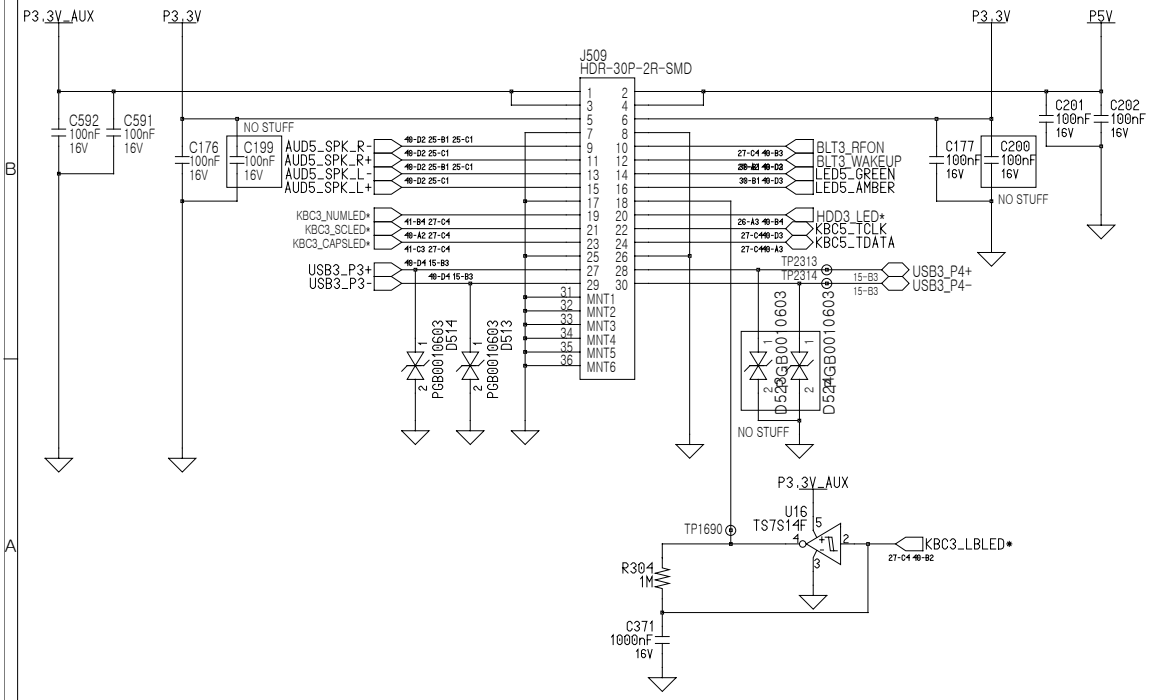
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KEYBOARD

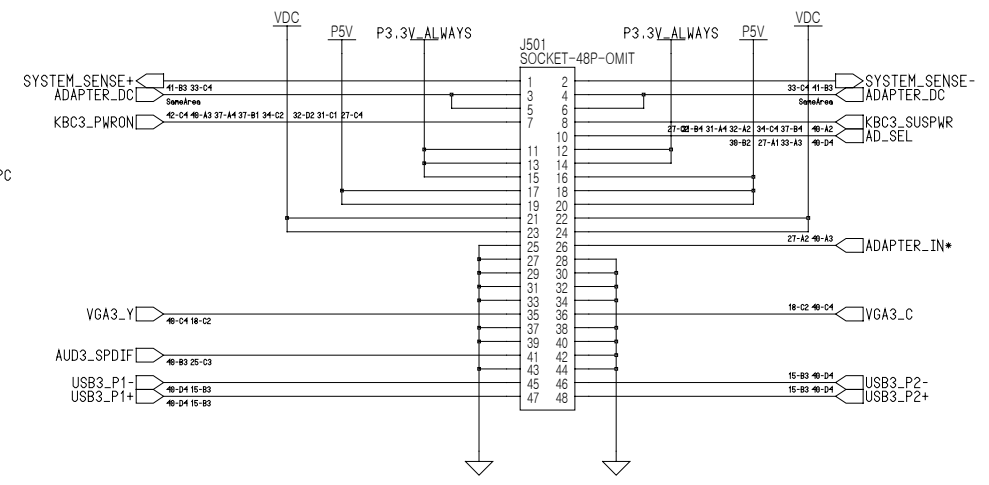
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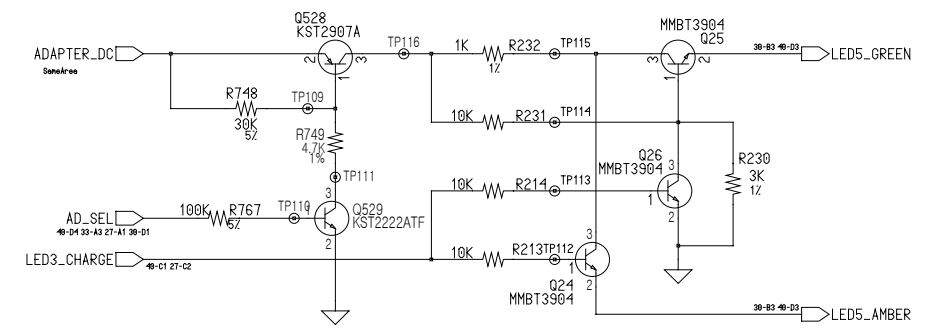
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Main to DC/DC BOARD



ADAPTERIN/CHARGING LED



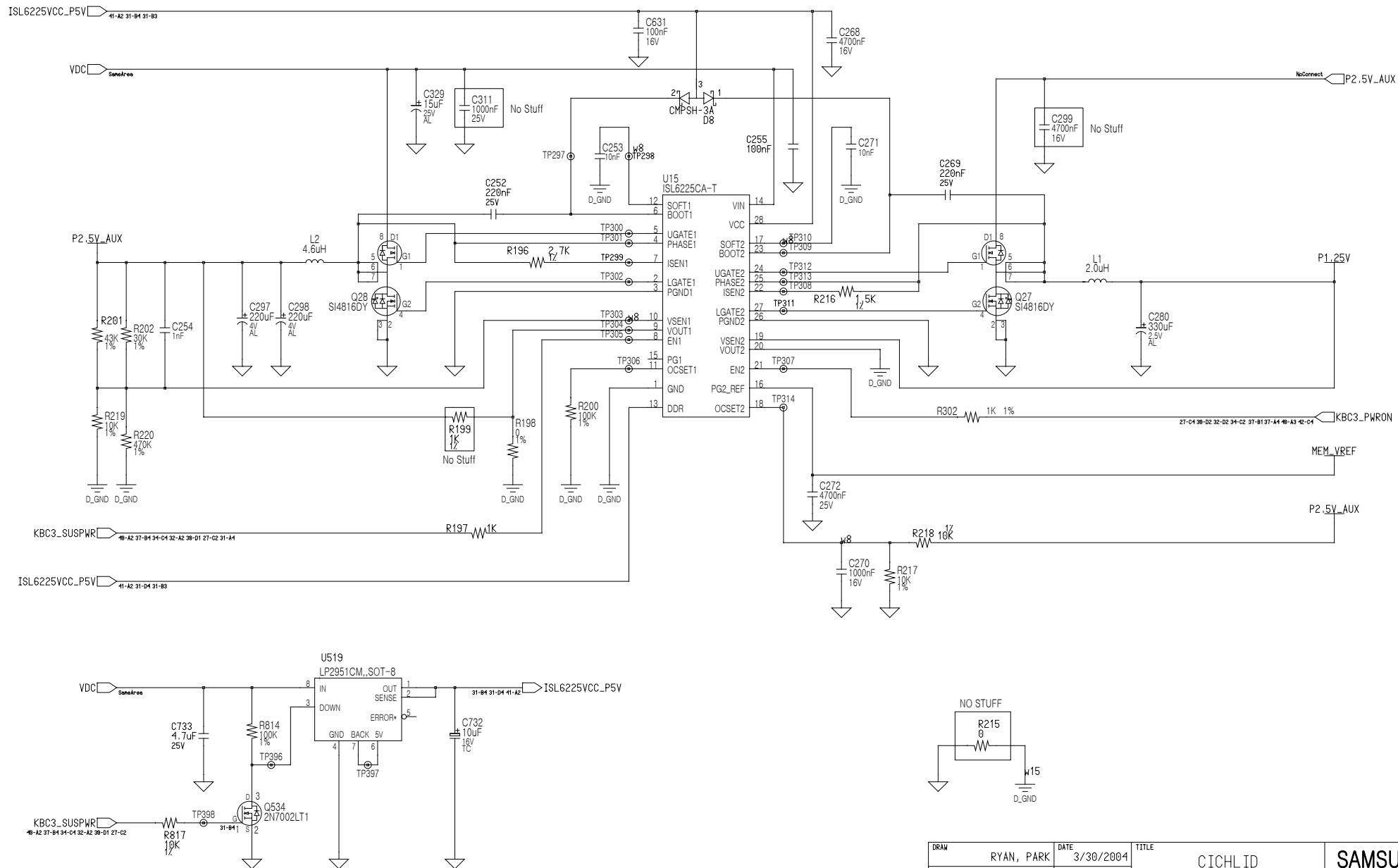
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MODULE CODE		LAST EDIT	March, 30, 2004 10:54:33 AM	PAGE	30	OF 41

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## Main DDR Power

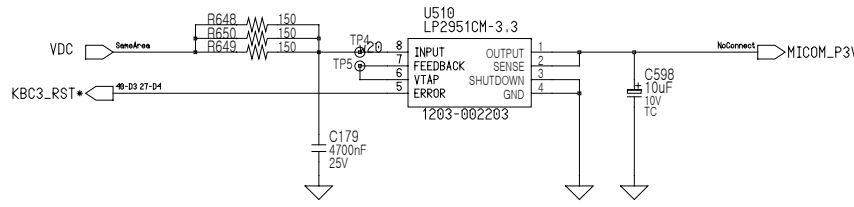


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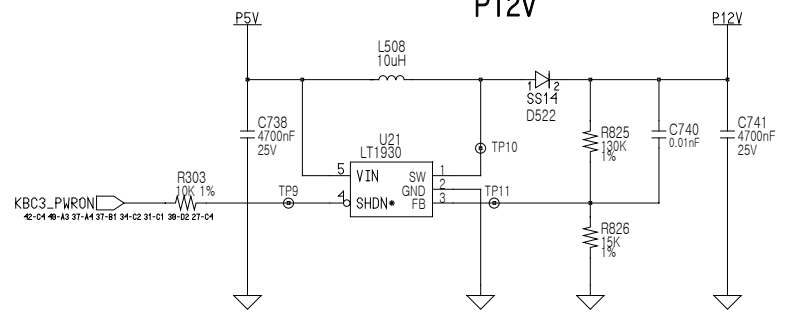
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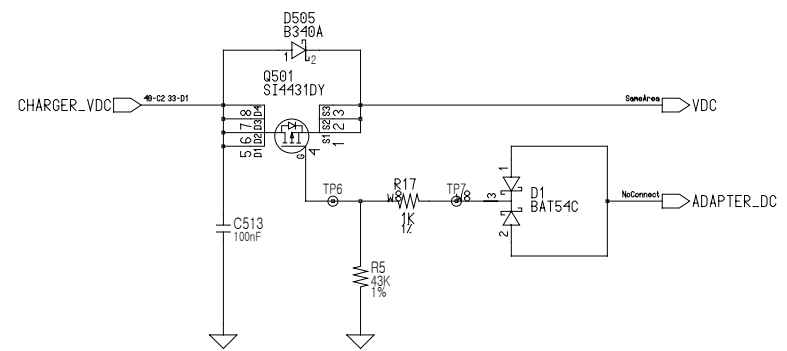
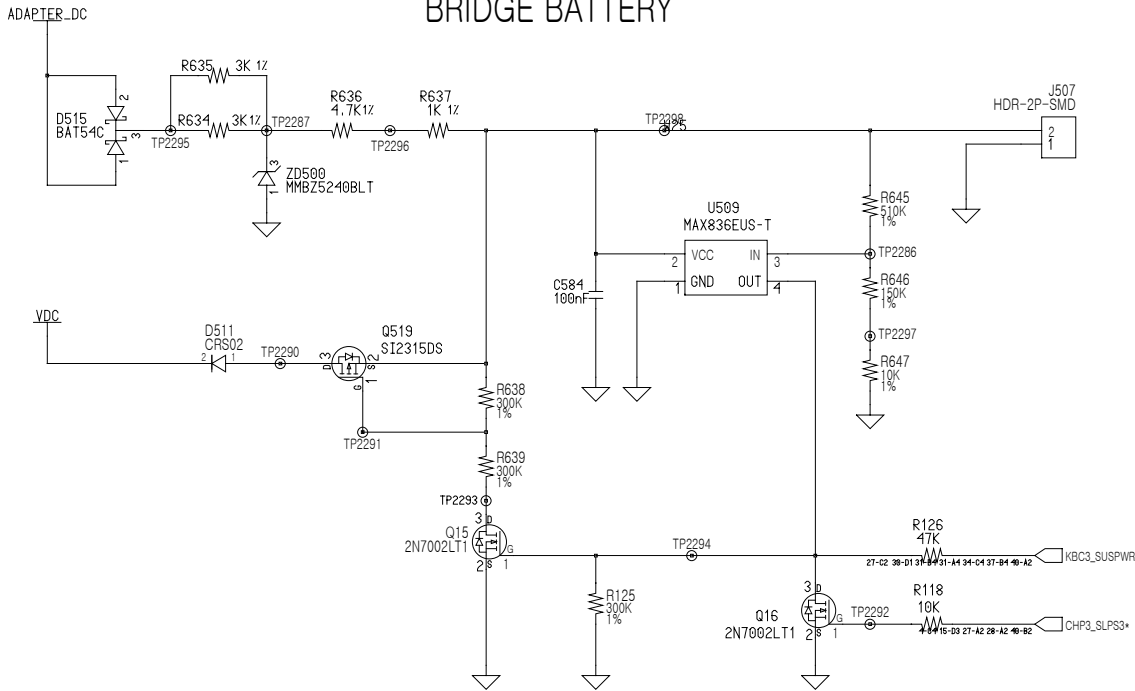
MICOM\_P3V Power



P12V



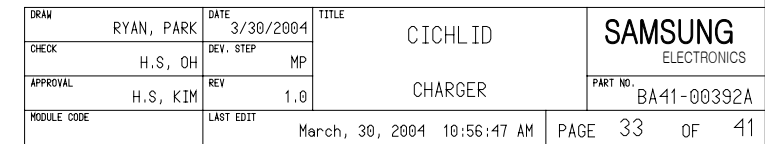
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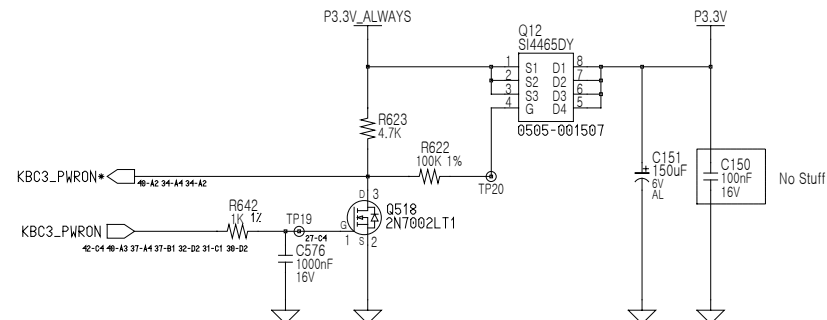
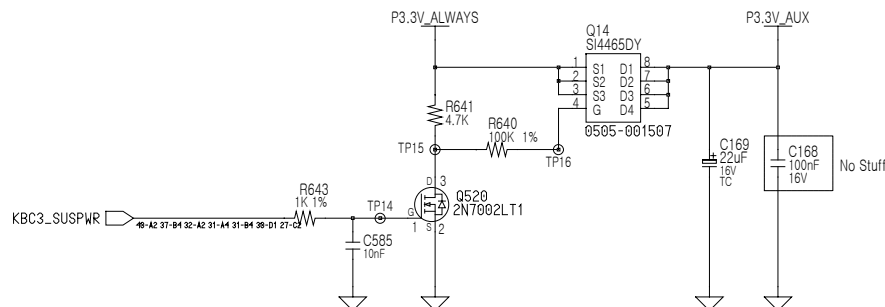
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MODULE CODE		LAST EDIT	March, 30, 2004 10:56:31 AM	PAGE	32	OF 41



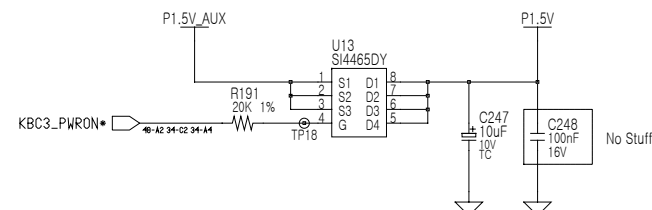
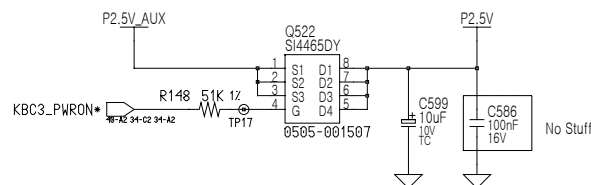
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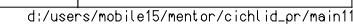


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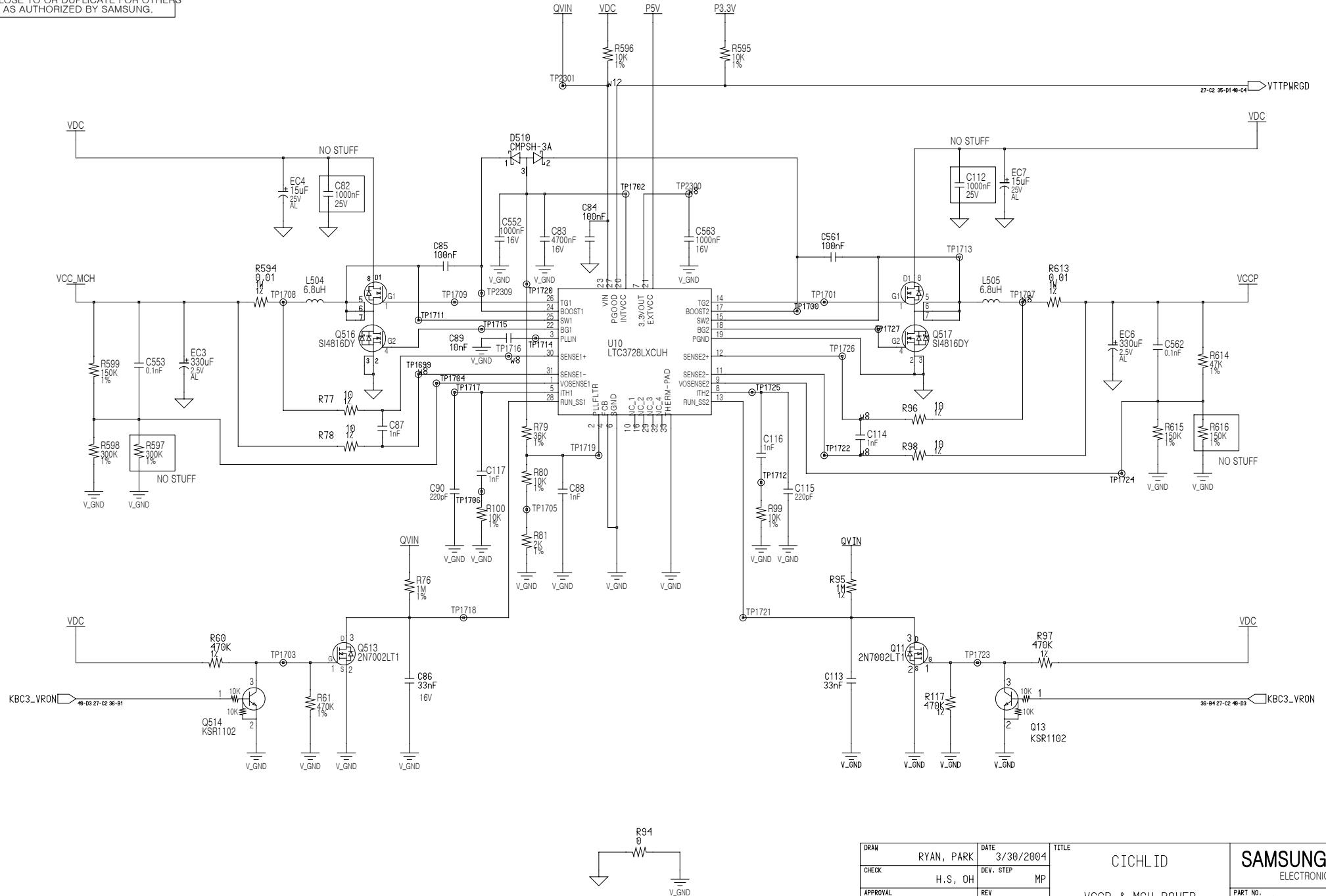



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APPROVAL		H.S., KIM		REV	1.0		P3.3 & P2.5 & P1.5 POWER		PART NO.		BA41-00392A		
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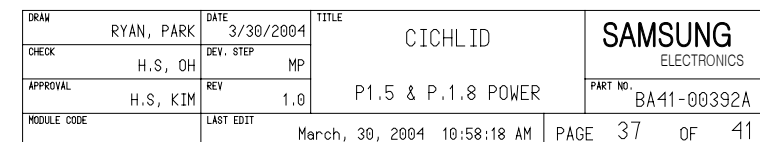


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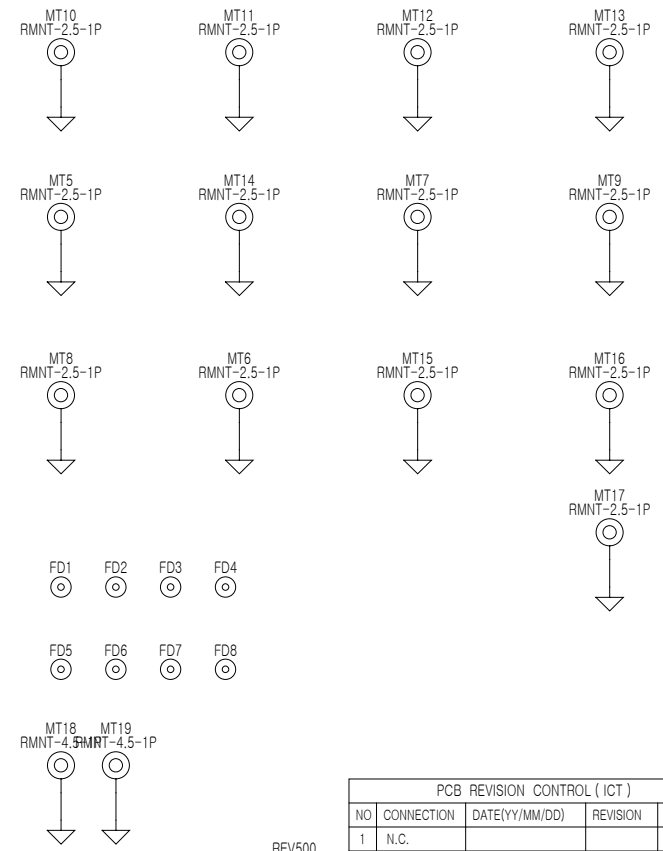
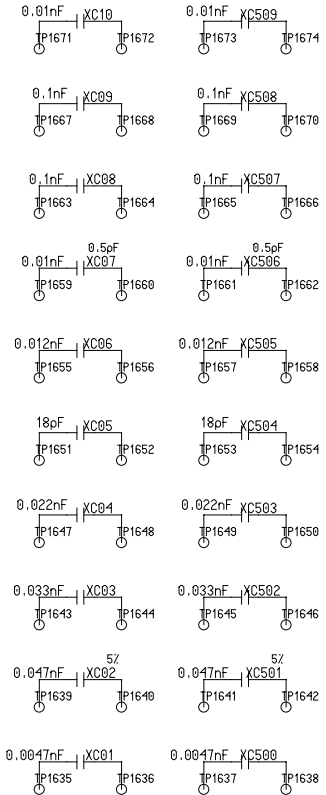
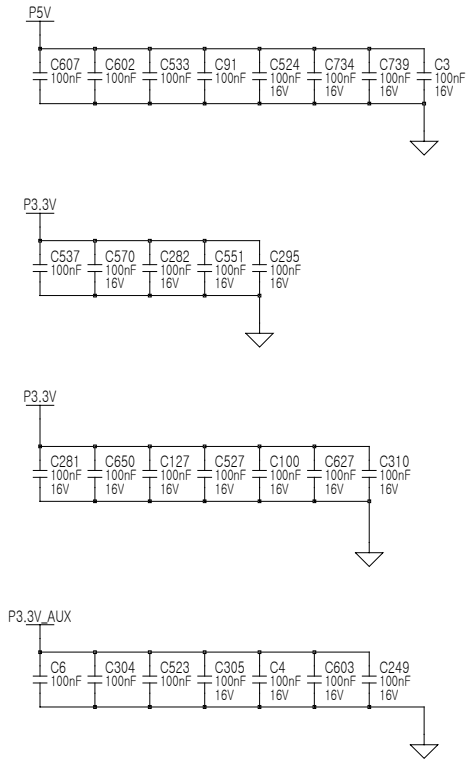
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CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0			
MODULE CODE		LAST EDIT	March, 30, 2004 10:57:47 AM			
				VCCP & MCH POWER	PART NO.	BA41-00392A
				PAGE	36	OF 41

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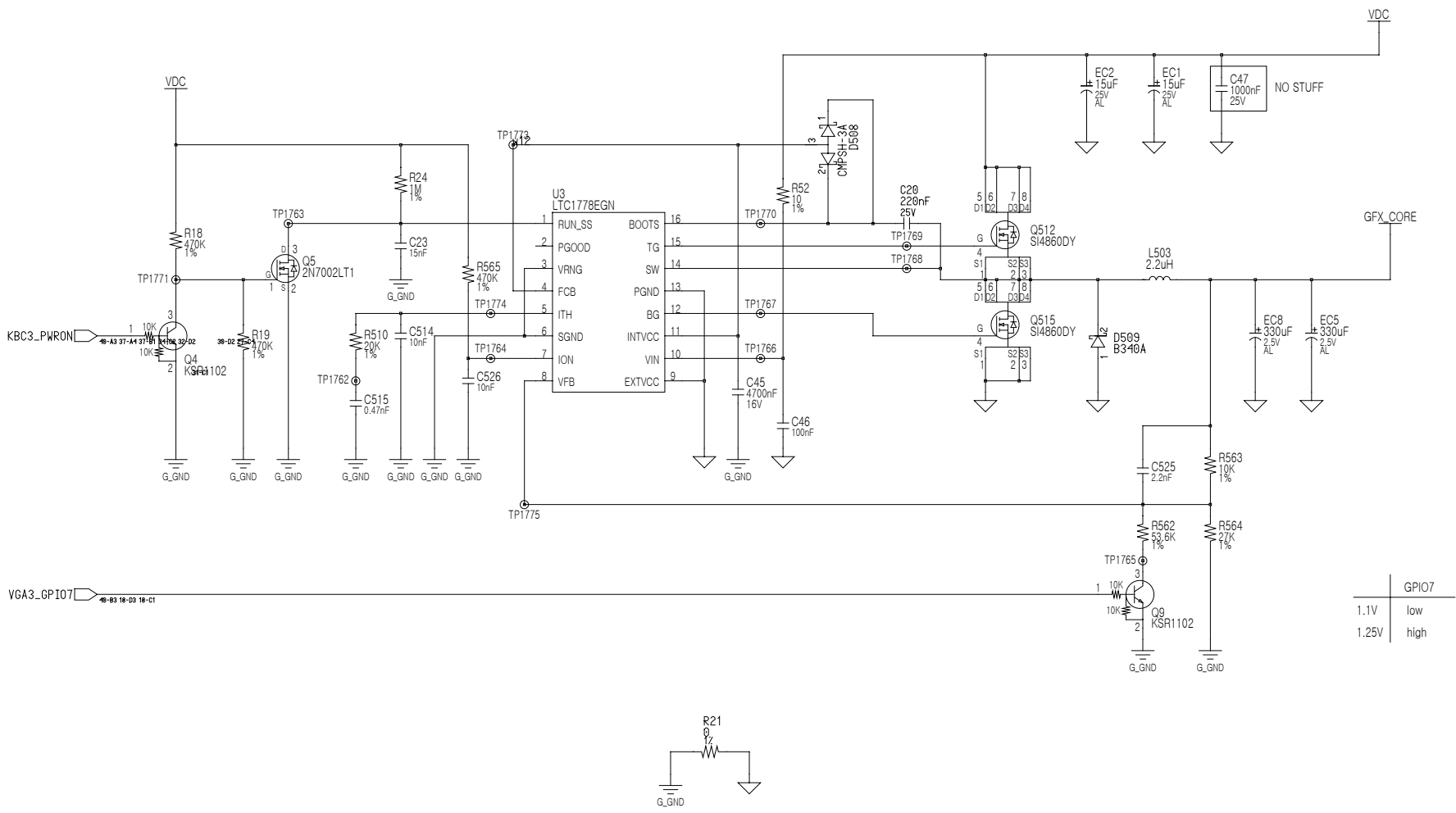


REV500  
1 0  
2 0 03

PCB REVISION CONTROL ( ICT )				
NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHLID	SAMSUNG
CHECK	H.S, OH	DEV. STEP	MP			ELECTRONICS
APPROVAL	H.S, KIM	REV	1.0		MOUNT HOLE & REV.	PART NO. BA41-00392A
MODULE CODE		LAST EDIT	March, 30, 2004 10:58:37 AM	PAGE	38	OF 41

Graphic Core Power



DRAW	RYAN, PARK	DATE	3/30/2004	TITLE		SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0	GRAPHIC POWER		PART NO.
MODULE CODE		LAST EDIT				BA41-00392A
				March, 30, 2004 11:43:13 AM	PAGE 39	OF 41

TP1050OS1+  
TP1051OS1-  
TP1052OS2+  
TP1053OS2-  
  
TP1055OVOS-  
TP1056OCD5\_L  
TP1057OCD5\_R  
TP1058OHP\_IN

TP1062OAD\_SEL  
TP1063OA\_CD1\*  
TP1064OA\_CD2\*  
TP1065OCB3\_B4  
TP1066OCB3\_B8  
TP1067OCB3\_D5  
TP1068OCB3\_J1

TP1074OVGA3\_C  
TP1075OVGA3\_Y  
TP1076OCA3\_VCC  
TP1077OCB3\_VCC  
TP1078OCD5\_COM  
TP1079OCDD5\_A0  
TP1080OCDD5\_A1  
TP1081OCDD5\_A2  
TP1082OHDD5\_A0  
TP1083OHDD5\_A1  
TP1084OHDD5\_A2  
TP1085OINV\_VDC

TP1026OMS\_RFU7  
TP1027OMS\_SCLK

TP1045OAU55\_CDU  
TP1046OAU55\_CDF  
TP1047AOA\_MC\_CDU  
TP1048OCB12\_VPF  
TP1049OCB3\_CCLK  
TP986OCB3\_CPAE  
TP987OCB3\_CVS1  
TP988OCB3\_CVS2  
TP989OCLK0\_ITP  
TP990OCPU1\_NMI  
TP991OCPU1\_TCK  
TP992OCPU1\_TDI  
TP993OCPU1\_TMS  
TP994OCPU1\_STB  
TP995OHUB1\_STE  
TP996OKBC3\_QS4  
TP997OMEM2\_BSG  
TP998OMEM2\_BSG  
TP999OPCT3\_PAR  
TP1000OSMB3\_PLK  
TP1001OUSB3\_C04

TP1002○USB3\_P0-  
TP1003○USB3\_P1+  
TP1004○USB3\_P1-  
TP1005○USB3\_P2+  
TP1006○USB3\_P2-  
TP1007○USB3\_P3+  
TP1008○USB3\_P3-

TP955OVGA3\_RED  
TP956OVTTTPWRGD  
TP957OAGP1\_GPA  
TP958OAGP1\_RBF  
TP959OAGP1\_VRE  
TP960OAGP1\_WBF  
TP961OAUD3\_SPK  
TP962OBAT3\_TEM  
TP963OBAT3\_VOI

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TP966OCB3_BVPP
TP967OCB3_BVPP
TP968OCB3_CCD1
TP969OCB3_CCD2
TP970OCB3_CGN2
TP971OCB3_CINT
TP972OCB3_CREQ
TP973OCB3_CRST
TP974OCBS3_SPK
TP975OCDD5_CS1
TP976OCDD5_CS3
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TP985OCDD5_D(8
TP982OCDD5_D(9
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TP242OCDD5\_IOR  
TP252OCDD5\_IOR  
TP262OCHP3\_PME  
TP272OCHP3\_SPK  
TP282OCLK0\_ITK  
TP292OCPU1\_ADS  
TP302OCPU1\_BNR  
TP312OCPU1\_HIT  
TP322OCPU1\_INT  
TP332OCPU1\_P51  
TP342OCPU1\_R50  
TP352OCPU1\_R51  
TP362OCPU1\_R52  
TP372OCPU1\_SLP  
TP382OCPU1\_SM1  
TP392OCHD3\_LED  
TP402OCHD5\_C18  
TP412OCHD5\_C53  
TP422OCHD5\_C67  
TP432OCHD5\_D1  
TP442OCHD5\_D2  
TP452OCHD5\_D3  
TP462OCHD5\_D4  
TP472OCHD5\_D5  
TP482OCHD5\_D6  
TP492OCHD5\_D7  
TP502OCHD5\_D8  
TP512OCHD5\_D9  
TP522OCHD5\_DRE  
TP532OCHD5\_DRE

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TP890OHDD5_IOW*
TP891OHDD5_LED*
TP892OHUB1_STB*
TP893OKBC3_A20Q
TP894OKBC3_BRIT
TP895OKBC3_RST*
TP896OKBC3_VRON
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TP899OKBC5\_TCLK  
TP900OLAN3\_PME\*

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TP902QLCD_VDD3V
TP903OMDC_AUDIN
TP904OMEM2_CKE0
TP905OMEM2_CKE1
TP906OMEM2_CKE2
TP907OMEM2_CKE3
TP908OMEM2_RBS0
TP909OMEM2_RBS1
TP910OPCI3_RST#
TP911OSMB3_DATA
TP912OUSB3_OC0#
TP913OUSB3_OC1#
TP914OUSB3_OC2#
TP915OUSB3_OC3#
TP916OUSB3_OC4#
TP917OUSB3_OC5#
TP918OVGA3_BLUE
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TP921OVGA3_DDC
TP858OVGA3_DDC
TP859OVGA3_SSON
TP860OVGA5_DDC
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TP862OADAPTER_D
TP863OAGP1_GGNT
TP864OAGP1_GREG
TP865OAGP1_PIPE
TP866OAGP1_ST(0
TP867OAGP1_ST(1
TP868OAGP1_ST(2
TP869OAGP3_BUSY
TP870OAUD3_PHOM
TP871OAUD3_SPD1
TP872OAUD5_CDCC
TP873OBLT3_RFOM
TP874OCB3_AVCC
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TP876OCB3\_BVCC5  
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TP879OCB3\_CAD(C)  
TP880OCB3\_CAD(2)  
TP881OCB3\_CAD(3)  
TP882OCB3\_CAD(4)  
TP883OCB3\_CAD(5)  
TP884OCB3\_CAD(6)  
TP885OCB3\_CAD(7)  
TP886OCB3\_CAD(8)  
TP887OCB3\_CAD(9)  
TP888OCB3\_AUD1  
TP889OCB3\_CCBEB  
TR826OCB3\_CCBEB  
TR827OCB3\_CCBEB  
TR828OCB3\_CCBEB  
TR829OCB3\_CTRDY  
TR830OCB3\_CPERF  
TR831OCB3\_CSERV  
TR832OCB3\_CSTOP  
TR833OCB3\_CTRDY  
TR834OCDD5\_D(10)  
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TR838OCDD5\_D(14)  
TR839OCDD5\_D(15)  
TR840OCDD5\_DACK1  
TR841OCDD5\_IORD1

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TP843OCLK0\_HCLK  
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TP845OCLK0\_HCLK  
TP846OCLK2\_MCLK  
TP847OCLK2\_MCLK  
TP848OCLK2\_MCLK

TP851OCLK2\_MCLK  
TP852OCLK3\_AGPPE  
TP853OCLK3\_ICH1  
TP854OCLK3\_ICH4  
TP855OCLK3\_ICH6  
TP856OCLK3\_MCH0  
TP857OCPU1\_A\*(3)  
TP794OCPU1\_A\*(4)  
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TP797OCPU1\_A\*(7)  
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TP799OCPU1\_A\*(9)  
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TP801OCPU1\_BPM0  
TP802OCPU1\_BPM1  
TP803OCPU1\_BPM2

TP885OCPU1\_DBP1  
TP886OCPU1\_BREQ  
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TP888OCPU1\_D\*(1)  
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TP819OCPU1\_D\*(3)  
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TP812OCPU1\_D\*(5)  
TP813OCPU1\_D\*(6)  
TP814OCPU1\_D\*(7)  
TP815OCPU1\_D\*(8)  
TP816OCPU1\_D\*(9)  
TP817OCPU1\_DBIO  
TP818OCPU1\_DBT1  
TP819OCPU1\_DBT2  
TP820OCPU1\_DBT3  
TP821OCPU1\_DBSY  
TP822OCPU1\_DPWR  
TP823OCPU1\_DRDY  
TP824OCPU1\_FERR  
TP825OCPU1\_HITM  
TP762OCPU1\_INIT

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TP7654CPU1..PREG
TP7660CPU1..TRDY
TP7670CPU1..TRST
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TP7690HDD5..D(1)
TP7710HDD5..D(12)
TP7710HDD5..D(13)
TP7720HDD5..D(14)
TP7730HDD5..D(15)
TP7740HDD5..DACK
TP7750HDD5..TORD
TP7760HUB1..HL(1)
TP7770HUB1..HL(1)
TP7780HUB1..HL(2)
TP7790HUB1..HL(3)
TP7790HUB1..HL(4)
TP7810HUB1..HL(5)
TP7820HUB1..HL(6)
TP7830HUB1..HL(7)
TP7840HUB1..HL(8)
TP7850HUB1..HL(9)
TP7860KBC3..CHGE
TP7870KBC3..PWR0
TP7880KBC3..PWR0
TP7890KBC3..QSL1

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TP792OKBC5\_TDAT  
TP793OLAN3\_DT0E

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TP730OLAN3_EECL
TP731OLED5_AMBE
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TP735OMEM2_CB(2
TP736OMEM2_CB(3
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TP7400MEM2_CB(7)
TP7410MEM2_CSA0
TP7420MEM2_CSA1
TP7430MEM2_CSA2
TP7440MEM2_CSA3
TP7450MEM2_MD(0)
TP7460MEM2_MD(1)
TP7470MEM2_MD(2)
TP7480MEM2_MD(3)
TP7490MEM2_MD(4)
TP7500MEM2_MD(5)
TP7510MEM2_MD(6)
TP7520MEM2_MD(7)
TP7530MEM2_MD(8)
TP7540MEM2_MD(9)
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TP757OPCI3\_AD(0  
TP758OPCI3\_AD(1

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TP700OPC13-AD(7)  
TP701OPC13-AD(8)  
TP702OPC13-AD(9)  
TP703OPC13-CBE0F  
TP704OPC13-CBE1F  
TP705OPC13-CBE2F  
TP706OPC13-CBE3F  
TP707OPC13-GNT0F  
TP708OPC13-GNT1F  
TP709OPC13-GNT2F  
TP710OPC13-GNT3F  
TP711OPC13-GNT4F  
TP712OPC13-INTAF  
TP713OPC13-INTBF  
TP714OPC13-INTCF

TP7160PC13 \_INTIE  
 TP7170PC13 \_INTIF  
 TP7180PC13 \_TRDY  
 TP7190PC13 \_PERR  
 TP7200PC13 \_REQ0  
 TP7210PC13 \_REQ1  
 TP7220PC13 \_REQ2  
 TP7230PC13 \_REQ3  
 TP7240PC13 \_REQ4  
 TP7250PC13 \_RSTF  
 TP7260PC13 \_SERR  
 TP7270PC13 \_STOP  
 TP7280PC13 \_TRDY  
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 TP6660VGA3 \_GP10  
 TP6670VGA3 \_GREEN  
 TP6680VGA3 \_HSYN  
 TP6690VGA3 \_SSOL  
 TP6700VGA3 \_VSYN  
 TP6710VGA5 \_HSYN  
 TP6720VGA5 \_VSYN  
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 TP6740AGP1 \_ADST  
 TP6750AGP1 \_ADST  
 TP6760AGP1 \_GAD0  
 TP6770AGP1 \_GAD0  
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TP688OAGP1\_GTRD  
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TP690OAUD5\_SPK\_  
TP691OAUD5\_SPK\_  
TP692OAUD5\_SPK\_  
TP693OBAT3\_SMCL

TP695OBLT3\_WAKE  
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TP663 CPU3.VID (2)
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TP506OHUB_REF_M
TP507OIMVP4_PWR
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TP511OKBC3\_PWR0  
TP512OKBC3\_PWRS  
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TP533OKBC5\_KSO(

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TP536 OCBC3 (3) KSL  
TP537 OCBC3 (3) CHA  
TP475 OCPC3 (3) LAD  
TP476 OCPC3 (3) LAD  
TP477 OCPC3 (3) LAD  
TP478 OCPC3 (3) LDR  
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TP471 OCPC2 (2) MAA  
TP472 OCPC2 (2) MAA  
TP473 OCPC2 (2) MAA

DRAM	RYAN, PARK	DATE	3/30/2004	TITLE	CICHL ID	SAMSUNG ELECTRONICS
CHECK	H.S., OH	DEV. STEP	MP			
APPROVAL	H.S., KIM	REV	1.0			
MODULE CODE		LAST EDIT	March, 30, 2004	11:53:09 AM	PAGE	40 OF 41



TP15980EM2\_M2\_D(50)  
TP14949EM2\_M2\_D(51)  
TP15890EM2\_M2\_D(52)  
TP15610EM2\_M2\_D(53)  
TP15820EM2\_M2\_D(54)  
TP15830EM2\_M2\_D(55)  
TP15840EM2\_M2\_D(56)  
TP15850EM2\_M2\_D(57)  
TP15860EM2\_M2\_D(58)  
TP15870EM2\_M2\_D(59)  
TP15880EM2\_M2\_D(60)  
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T1253OCHP3_CDRUFEN#
T1254OCHP3_DPSFLVPR
T1255OCHP3_DTPWRN
T1256OCHP3_SUG#(0)
T1257OCPU1_PWRGDGPU

T1264OKBC3_CAPSLED#
T1265OKBC3_CD_CN0#
T1266OKBC3_CD_CN2#
T1267OKBC3_EZ_BTN0#
T1268OKBC3_EZ_BTN1#
T1269OKBC3_EZ_BTN2#
T1270OKBC3_LANGRST#
T1271OKBC3_WAK#(0)
T1272OMCH1_HVSWING1
T1273OMCH1_HVSWING1
T1210EMEM2_RMMA(1)
T1211EMEM2_RMMA(11)
T1212EMEM2_RMMA(12)
T1213OSYSTEM_SENSE#
T1214OSYSTEM_SENSE#
T1215OCHP3_DSGT_RST#(0)
T1216VOGA3_DVOD(11)
T1217VOGA3_DVODXSHN
T1218VOGA3_LCDDVDDN
T1220A0A_ID3_SWITCH#
T1221OBLT3_BTOM_LED#
T1222OCHP3_ACGT_BOLK#
T1223OCHP3_ACGT_RST#
T1224OCHP3_ACGT_SD10
T1225OCHP3_ACGT_SD11
T1226OCHP3_ACGT_SD12
T1227OCHP3_ACGT_SYNC
T1228OCHP3_INTRUDR#
T1229OCHP3_THRMTTRIP#
T1230OCP1_K3_POWMCON
T1231OCPU1_THRMTTRIP#

T1233OKBC3_SPDIF_ON#
T1234OAUD5_LINE_OUT_L
T1235OAUD5_LINE_OUT_R
T1236OCHP3_1394_ROM#

T1238OA0A_AUD5_MIC_CODECC
T1240OCHP3_INVF4_PWRGD
T1240OCHP3_THERM_SWCLK
T1241OA0A_AUD5_LINE_OUT#

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[illegible]TP1380P5V\_CD  
TP1130P5V\_CD  
  
TP1134OPRTC\_BAT  
TP1135OPRTC\_BAT  
  
TP1138OP1\_5V\_AUX  
TP1139OP1\_5V\_AUX  
TP1140OP1\_5V\_AUX  
TP1141OP1\_5V\_AUX  
TP1142OP2\_5V\_AUX  
TP1143OP2\_5V\_AUX  
TP1144OP2\_5V\_AUX  
TP1145OP2\_5V\_AUX  
TP1882OP3\_3V\_AUX  
TP1883OP3\_3V\_AUX  
TP1884OP3\_3V\_AUX  
TP1885OP3\_3V\_AUX  
TP1886OP3\_3V\_ALWAYS  
TP1887OP3\_3V\_ALWAYS  
TP1888OP3\_3V\_ALWAYS  
TP1889OP3\_3V\_ALWAYS  
  
TP1098OVDC  
TP1099OVDC  
TP1099OVDC  
TP1100OVDC  
TP1102OVCCP  
TP1103OVCCP  
TP1104OVCCP  
TP1105OVCCP  
TP1106OVCC\_MCH  
TP1107OVCC\_MCH  
TP1108OVCC\_MCH  
TP1109OVCC\_MCH  
TP1110OVCC\_CORE  
TP1111OVCC\_CORE  
TP1112OVCC\_CORE  
  
TP1166OP5V  
  
TP1576QISL6225VCC\_P5V  
  
TP1561OFAN3\_FDBACK\*  
TP1576QKBC3\_SICEN\*

```

TP2270CEVEN_VGA3_A0+
TP22770CEVEN_VGA3_A1+
TP22780CEVEN_VGA3_A1+
TP22790CEVEN_VGA3_A1+
TP22800CEVEN_VGA3_A2+
TP2280CEVEN_VGA3_A2-
TP2280CEVEN_VGA3_CLK+
TP22830C0D_VGA3_CLK-
TP22840KB3_THERM_ALERT*
TP22850LCD3_BRIT

TP186*00DD_VGA3_A0+
TP186S00DD_VGA3_A0-
TP186100DD_VGA3_A1+
TP186100DD_VGA3_A1-
TP186800DD_VGA3_A2+
TP186900DD_VGA3_A2-
TP181800DD_VGA3_CLK+
TP181100DD_VGA3_CLK-

TP181*00DD180DG
TP18160VIDE0_THERM_SMCLK
TP18160VIDE0_THERM_SMDATA
TP18170A_GND
TP18180A_GND
TP18190A_GND
TP18200A_GND
TP18210_GND
TP18220D_GND
TP18230D_GND
TP18240D_GND
TP18250G_GND
TP18260G_GND
TP18270G_GND
TP18280G_GND
TP18290V_GND
TP17940V_GND
TP17950V_GND

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TP1810VDD18DIG
TP1815OVIDE0_THERM_SMLCK
TP1816OVIDE0_THERM_SMDATA
TP1817OA_GND
TP1818OA_GND
TP1819OA_GND
TP1820OA_GND
TP1821OD_GND
TP1822OD_GND
TP1823OD_GND
TP1824OD_GND
TP1825OG_GND
TP1826OG_GND
TP1827OG_GND
TP17910V_GND
TP17920V_GND
TP17930V_GND
TP17940V_GND
TP17950V_GND
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TP1166OP5V

TP1561OFAN3\_FDBACK\*

TP1676OKBC3\_SICEN\*

DRAM	RYAN, PARK	DATE	3/30/2004	TITLE	CICHLID	SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0			
MODULE CODE	LAST EDIT		March, 30, 2004 11:53:18 AM		PAGE	41 OF 41

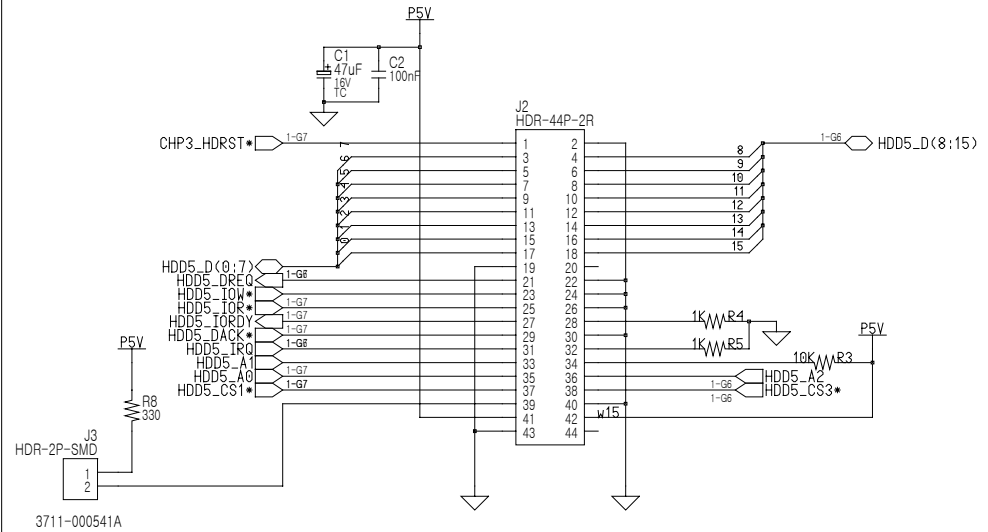
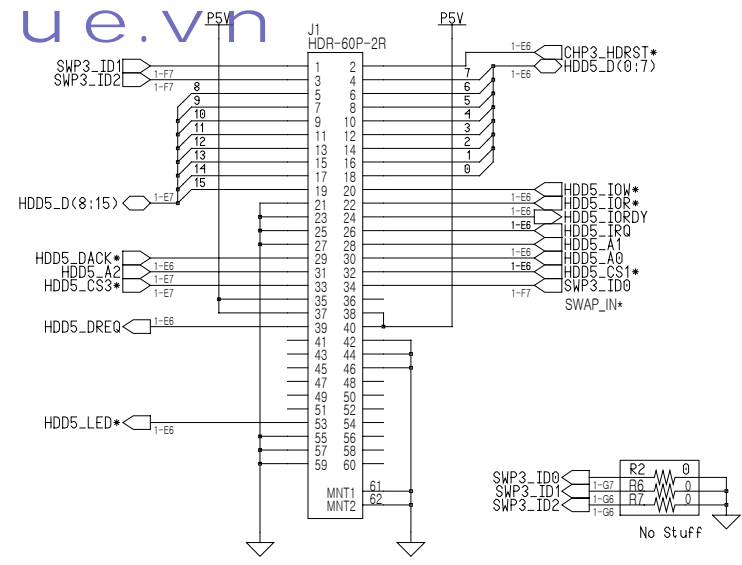
# 2ndHDD-I/F BOARD

CPU : BANIAS  
Chip Set : ODEM+  
Remarks : 2ndHDD

Model Name : CICHOLID  
PBA Name : 2nd HDD Interface  
A'ssy Code : BA59-01330A  
Dev. Step : MP  
Revision : 1.0  
T.R. Date : 2004. 1. 17

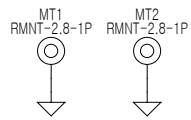
DRAW	CHECK	APPROVAL

Owner : Signature : X



## SWAPBAY ID

Devices  
CD-ROM 0  
2nd HDD 1 (No Connect)



DRAW	RYAN, PARK	DATE	12/11/2003	TITLE	CICHOLID	SAMSUNG ELECTRONICS
CHECK	OH, H.S	DEV. STEP	DV	2ND HDD I/F B'D	2ND HDD I/F B'D	
APPROVAL	LEE, KEVIN	REV	1.0	December, 11, 2003 5:35:29 PM	PAGE 1 OF 1	PART NO. BA41-XXXXXX
MODULE CODE		LAST EDIT				

# CICHLID

CPU : BANIAS/DOTHAN  
Chip Set : ODEM+  
Remarks :

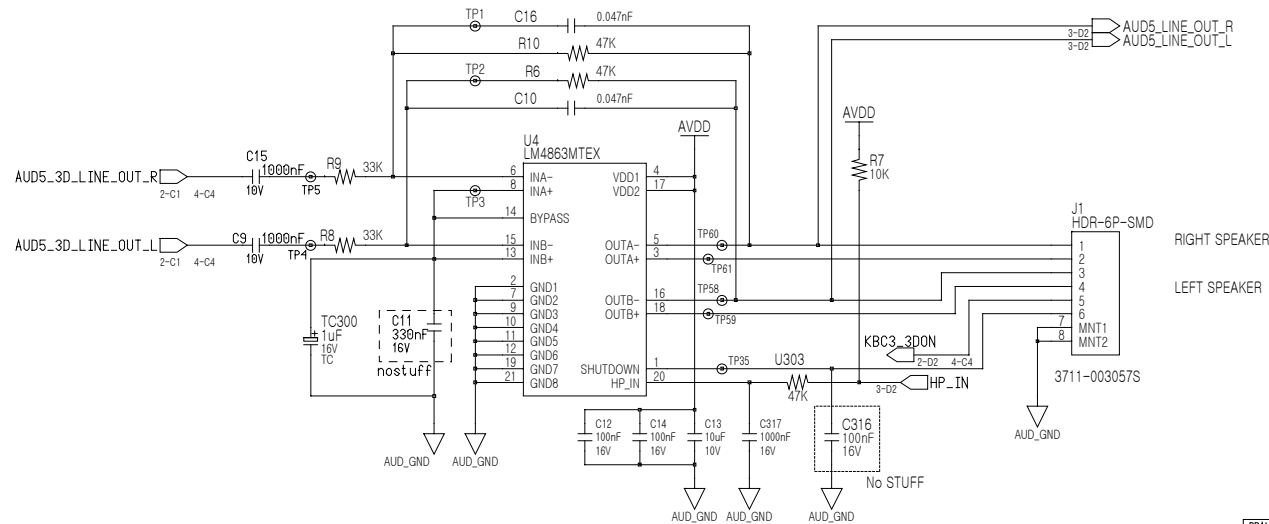
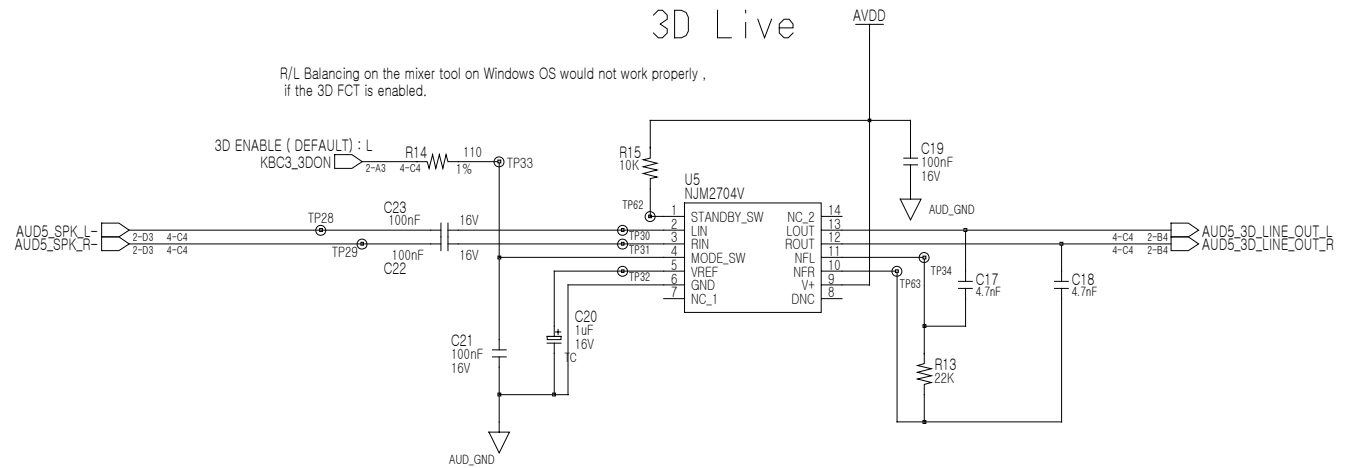
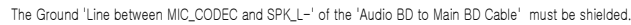
Model Name : AUDIO Board  
PBA Name :  
PCB Code : BA59-01332A  
Dev. Step : MP  
Revision : 1.3  
T.R. Date : 05/07/2004

DRAW	CHECK	APPROVAL

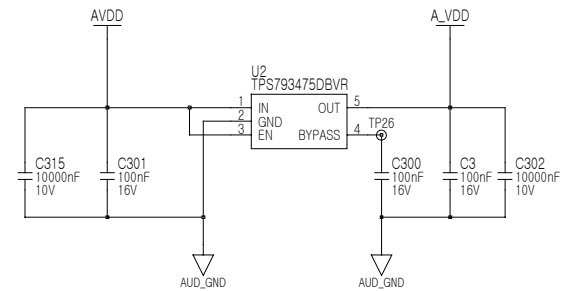
DRAW		PARK, RYAN		DATE	3/22/2004		TITLE	CICHLID AUDIO BOARD	SAMSUNG ELECTRONICS		
CHECK		OH, H.S		DEV. STEP		MP			PART NO.	BA59-01332A	
APPROVAL		LEE, KEVIN		REV		1.1					
MODULE CODE				LAST EDIT				March 22, 2004 7:52:12 PM		PAGE 1 OF 4	


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Enough Thermal Ground Area Should be Guaranteed for spreading intense heat of LM4863.

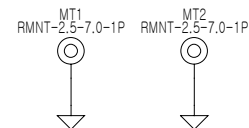
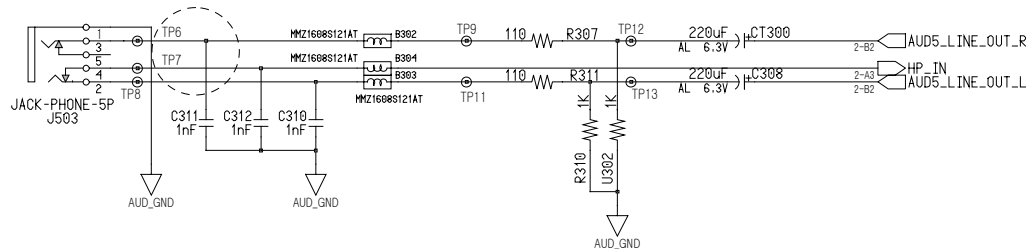


DRAW		DATE		TITLE			
PARK, RYAN		3/22/2004		CICHLID AUDIO BOARD UNDEFINED			
CHECK	OH, H.S	DEV. STEP	MP				
APPROVAL	LEE, KEVIN	REV	1.1				
MODULE CODE		LAST EDIT		March 22, 2004 7:52:12 PM		PAGE	2 OF

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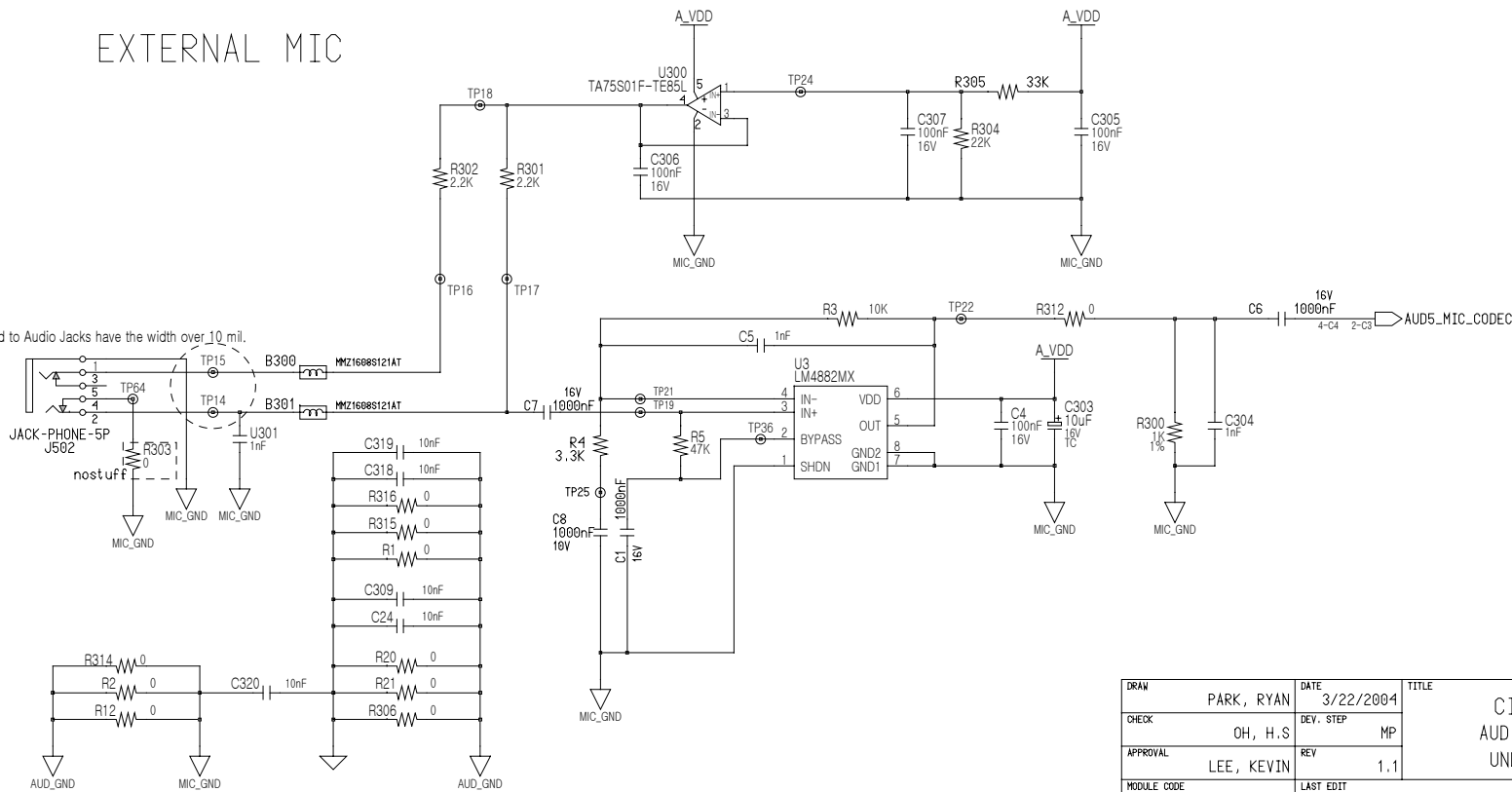
## HEADPHONE

Make sure that the traces led to Audio Jacks have the width over 10 mil.



## EXTERNAL MIC

Make sure that the traces led to Audio Jacks have the width over 10 mil.



DRAW	PARK, RYAN	DATE	3/22/2004	TITLE	CICHLID AUDIO BOARD	SAMSUNG ELECTRONICS
CHECK	OH, H.S	DEV. STEP	MP	REV	1.1	PART NO. BA59-01332A
APPROVAL	LEE, KEVIN	LAST EDIT	March 22, 2004 7:52:12 PM	PAGE	3 OF 4	
MODULE CODE						



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h t t p : / / l a p t o p b l u e . v n

TP37OKBC3\_3D0N  
TP38OAU5\_SPK\_L-  
TP39OAU5\_SPK\_R-  
TP40OAU5\_MIC.CODEC  
  
TP41OAU5\_3D\_LINE\_OUT\_L  
TP42OAU5\_3D\_LINE\_OUT\_R  
  
TP55OAVDD  
TP54OA\_VDD  
  
TP43OAU\_GND  
  
TP51OMIC\_GND

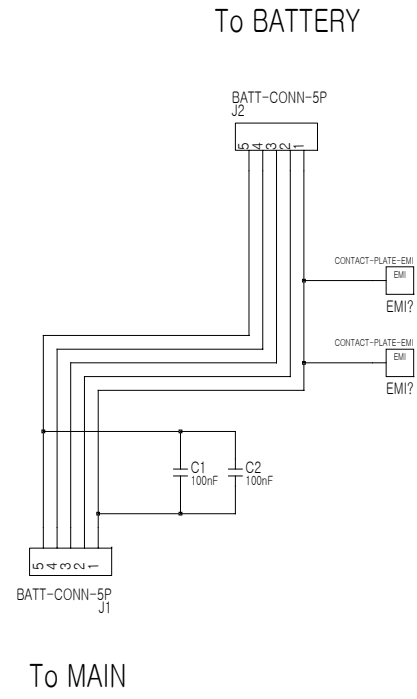
DRAW	PARK, RYAN	DATE	3/22/2004	TITLE CICHLID AUDIO BOARD UNDEFINED		<b>SAMSUNG</b> ELECTRONICS	
CHECK	OH, H.S	DEV. STEP	MP				
APPROVAL	LEE, KEVIN	REV	1.1			PART NO.	BA59-01332A
MODULE CODE	LAST EDIT			March 22, 2004 7:52:12 PM		PAGE	4 OF 4

# CICHLID

CPU : BANIAS / DOTHAN  
Chip Set : ODEM+  
Remarks :

Model Name : BATTERY BR. BOARD  
PBA Name :  
PCB Code : BA59-01331A  
Dev. Step : MP  
Revision : 1.2  
T.R. Date : 2004.04.01

DRAW	CHECK	APPROVAL



- NET LIST NAME
- #1 GND
  - #2 BAT3\_TEMP
  - #3 BAT3\_SMDATA\*
  - #4 BAT3\_SMCLK\*
  - #5 VDC

DRAW	PARK, RYAN	DATE	12/5/2003	TITLE	CICHLID BATTERY BRIDGE BOARD	SAMSUNG ELECTRONICS
CHECK	OH, H.S	DEV. STEP	DV			PART NO. BA41-
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST EDIT	December, 5, 2003 6:00:28 PM	PAGE	1 OF 1	



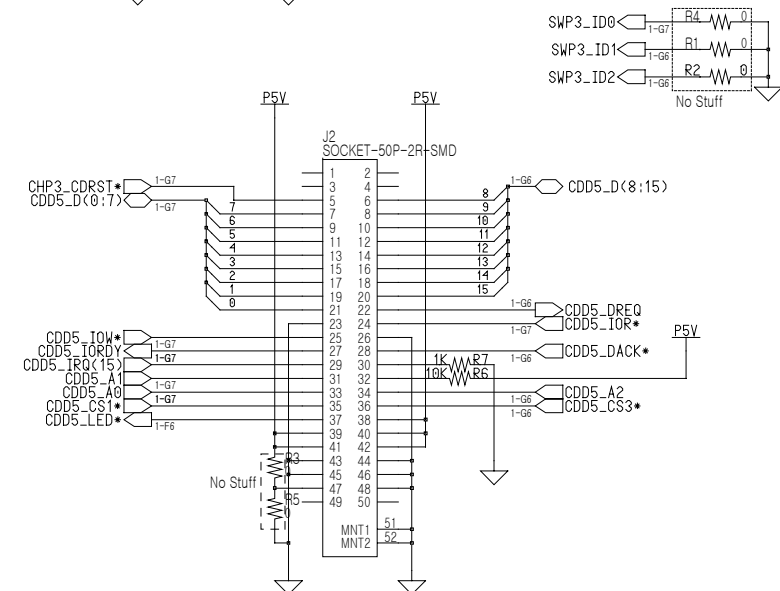
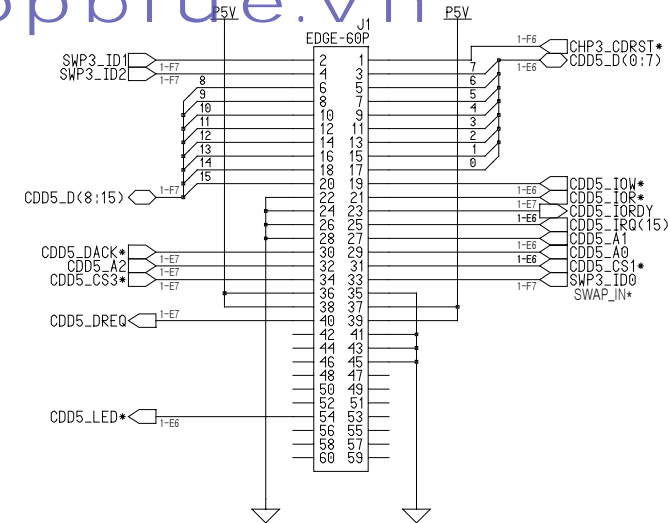
# CD-I/F BOARD

CPU : BANIAS/DOTHAN  
Chip Set : ODEM+  
Remarks : CD/COMBO/DVD-MULTI

Model Name : CICHlid  
PBA Name : CD Interface  
A'ssy Code : BA59-01333A  
Dev. Step : MP  
Revision : 1.1  
T.R. Date : 2004.05.06

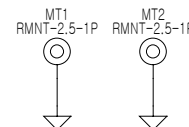
DRAW	CHECK	APPROVAL

Owner : Signature : X



## SWAPBAY ID

Devices	SWAP_IN*
CD-ROM	0
2nd HDD	1



DRAW		PARK, RYAN		DATE	12/4/2003		TITLE		CICHLD		SAMSUNG ELECTRONICS	
CHECK		OH, H.S		DEV. STEP	DV		CD I/F B'D		CD I/F B'D			
APPROVAL		LEE, KEVIN		REV	1.0						PART NO.	BA41-XXXXXX
MODULE CODE				LAST EDIT		December, 4, 2003 2:55:12 PM			PAGE	1	OF	1

# ONTOP BOARD

CPU : BANIAS/DOTHAN  
Chip Set : ODEM+  
Remarks : EASY BUTTON BOARD

Model Name : ONTOP BOARD  
PBA Name :  
PCB Code : BA59-01334A  
Dev. Step : MP  
Revision : 1.0  
T.R. Date : 2004.01.28

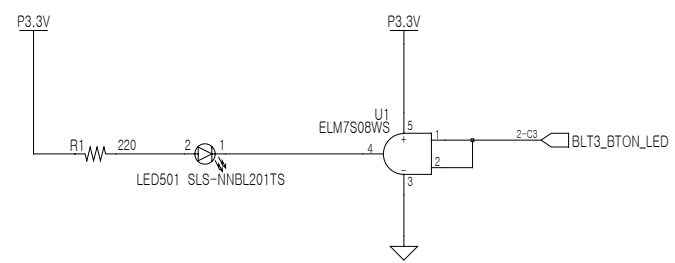
DRAW	CHECK	APPROVAL

DRAW	PARK, RYAN	DATE	12/3/2003	TITLE	CICHLID ONTOP BOARD	SAMSUNG ELECTRONICS
CHECK	OH, H.S	DEV. STEP	DV			
APPROVAL	LEE, KEVIN	REV	1.0			PART NO. BA41-
MODULE CODE	LAST EDIT			January, 28, 2004 2:12:38 PM	PAGE	1 OF 2

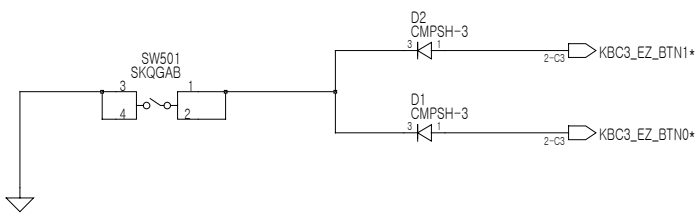
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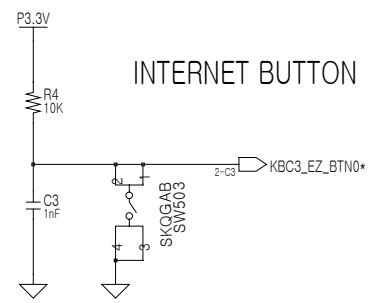
BLUETOOTH BUTTON LED



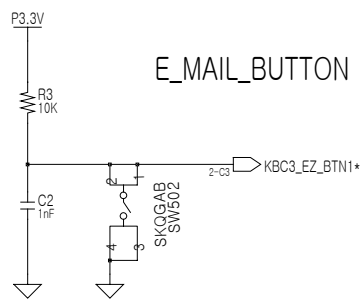
USER BUTTON



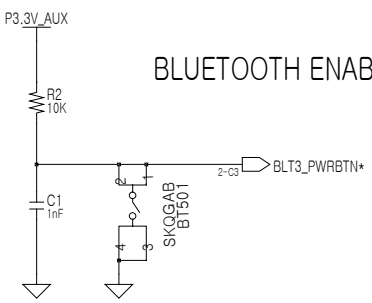
INTERNET BUTTON



E\_MAIL\_BUTTON



BLUETOOTH ENABLE BUTTON



D  
C  
B  
A

D  
C  
B  
A

DRAW	PARK, RYAN	DATE	12/3/2003	TITLE	CICHL ID UNDEF INED ONTOP BOARD	SAMSUNG ELECTRONICS
CHECK	OH, H.S	DEV. STEP	DV			PART NO. BA41-undef ined
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST EDIT	December, 3, 2003 2:13:08 PM	PAGE	2 OF 2	

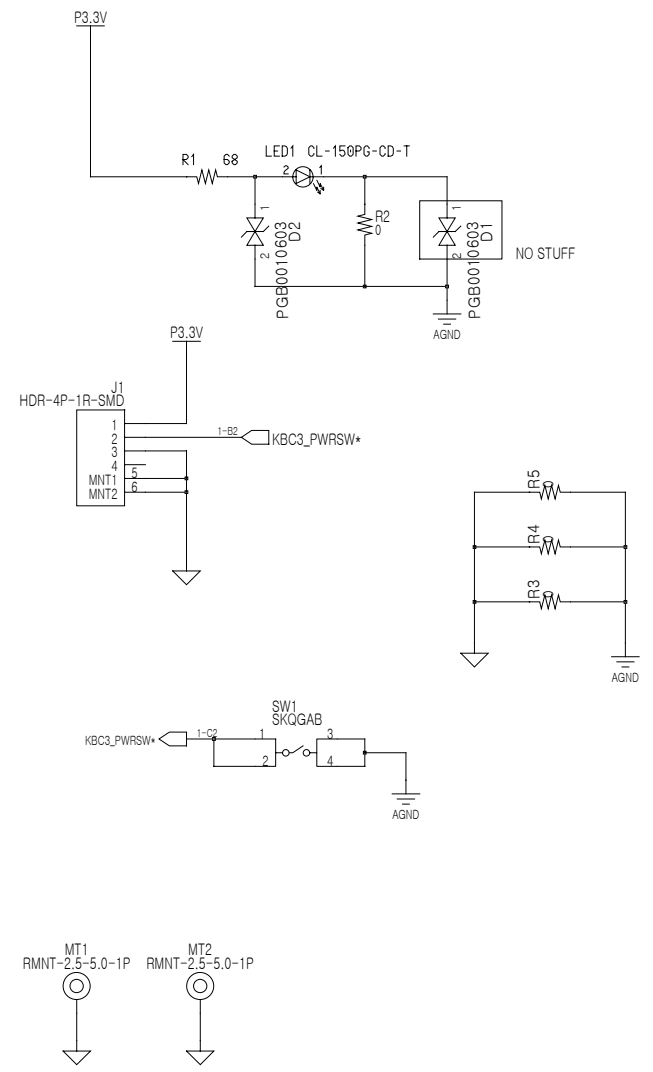


# POWER SW BOARD

CPU : BANIAS/DOTHAN  
Chip Set : ODEM+  
Remarks :

Model Name : Power SW Board  
PBA Name :  
PCB Code : BA59-01336A  
Dev. Step : MP  
Revision : 1.0  
T.R. Date : 2004.01.28

DRAW	CHECK	APPROVAL



DRAW	PARK, RYAN	DATE	12/4/2003	TITLE	CICHLID POWER BOARD	SAMSUNG ELECTRONICS
CHECK	OH, H.S	DEV. STEP	DV			
APPROVAL	LEE, KEVIN	REV	1.0			PART NO. BA41-undef ined
MODULE CODE		LAST EDIT	December, 4, 2003 11:57:34 AM	PAGE	1 OF 1	

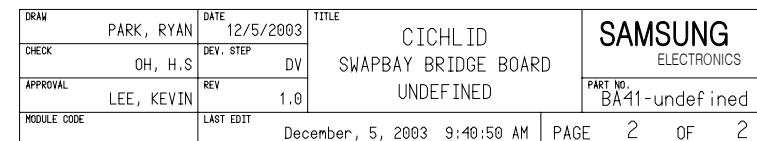
# SWAPBAY BR. BOARD

CPU : BANIAS/DOTHAN  
Chip Set : ODEM+  
Remarks :

Model Name : SWAPBAY BR. BOARD  
PBA Name :  
PCB Code : BA59-01335A  
Dev. Step : MP  
Revision : 1.2  
T.R. Date : 2004.04.01

DRAW	CHECK	APPROVAL

DRAW	PARK, RYAN	DATE	12/5/2003	TITLE	CICHLID SWAPBAY BRIDGE BOARD	SAMSUNG ELECTRONICS
CHECK	OH, H.S	DEV. STEP	DV			PART NO. BA41-
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST EDIT	December, 5, 2003 9:40:29 AM	PAGE	1 OF	2







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- TP19ONS4406
- TP20ONS4407
- TP21ONS4408
- TP22OCDD5\_L
- TP23OCDD5\_R
- TP24ONS4411
- TP25ONS4412
- TP26ONS4413
- TP27ONS4414
- TP28ONS4415
- TP29ONS4416
- TP30ONS4417
- TP31ONS4418
- TP32ONS4419
- TP33OCDD5\_A0
- TP34OCDD5\_A1
- TP35OCDD5\_A2
- TP36OCDD5\_COM
- TP37OSPK\_MUTE
- TP38OCDD5\_CS1\*
- TP39OCDD5\_CS3\*
- TP40OCDD5\_D(0)
- TP41OCDD5\_D(1)
- TP42OCDD5\_D(2)
- TP43OCDD5\_D(3)
- TP44OCDD5\_D(4)
- TP45OCDD5\_D(5)
- TP46OCDD5\_D(6)
- TP47OCDD5\_D(7)
- TP48OCDD5\_D(8)
- TP49OCDD5\_D(9)
- TP50OCDD5\_DREQ
- TP3OCDD5\_IOR\*
- TP4OCDD5\_IOW\*
- TP5ODTV\_USB5+
- TP6ODTV\_USB5-
- TP7OKBC3\_3D0N
- TP8OCDD5\_D(10)
- TP9OCDD5\_D(11)
- TP10OCDD5\_D(12)
- TP11OCDD5\_D(13)
- TP12OCDD5\_D(14)
- TP13OCDD5\_D(15)
- TP14OCDD5\_DACK\*
- TP15OCDD5\_IORDY
- TP16OKBC3\_DTVON
- TP17OCHP3\_CDRST\*
- TP18OCDD5\_IRQ(15)
- TP1OP5V\_CD
- TP2OVDC

# CICHLID

CPU : BANIAS/DOTHAN  
Chip Set : ODEM+  
Remarks :

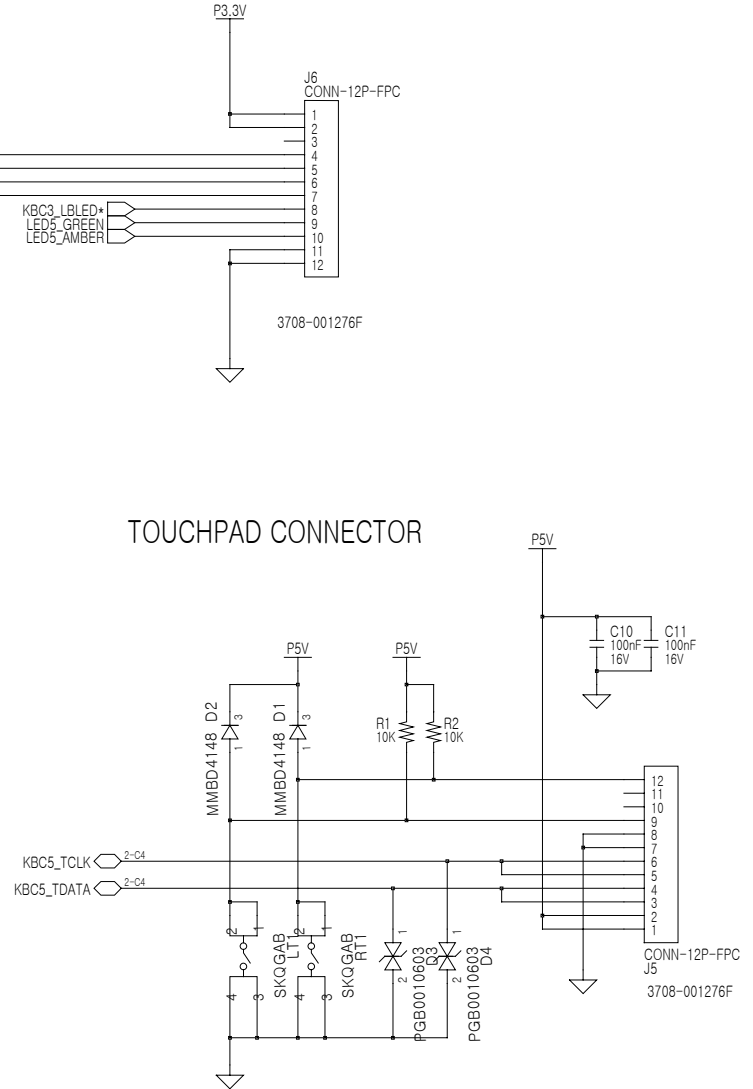
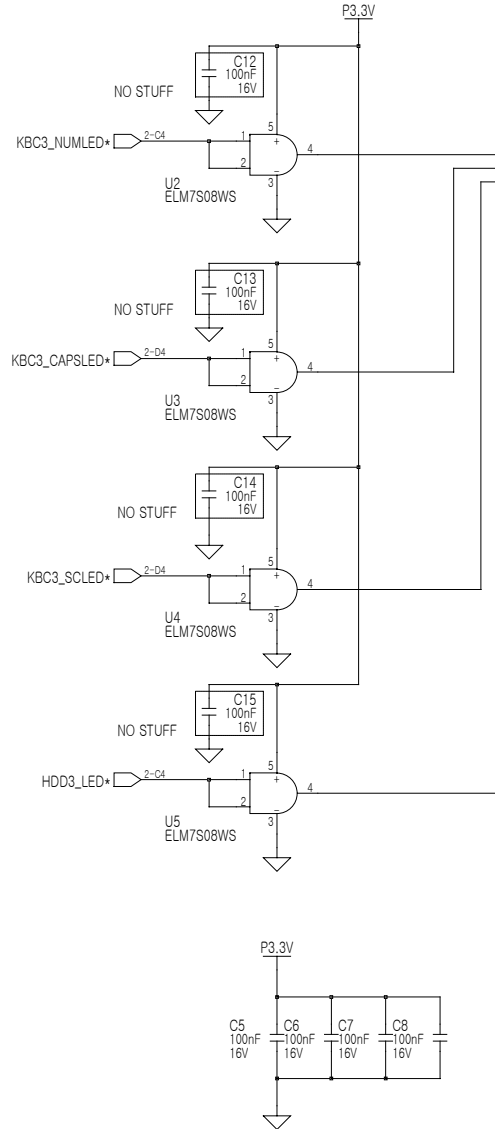
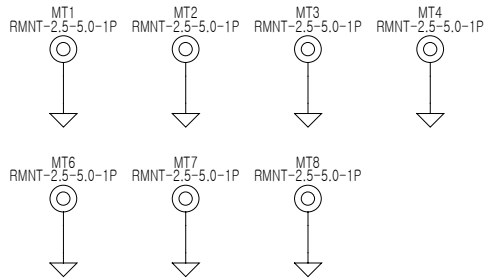
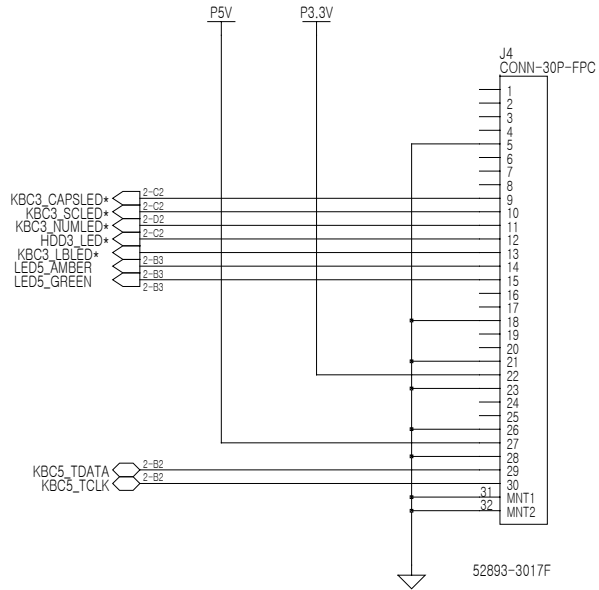
Model Name : TOUCHPAD I/F BOARD  
PBA Name :  
PCB Code : BA59-01329A  
Dev. Step : MP  
Revision : 1.0  
T.R. Date : 2004. 2. 28

DRAW	CHECK	APPROVAL

DRAW	PARK, RYAN	DATE	12/2/2003	TITLE	CICHLID TOUCHPAD I/F BOARD	SAMSUNG ELECTRONICS
CHECK	OH, H.S	DEV. STEP	DV			PART NO.
APPROVAL	LEE, KEVIN	REV	1.0			BA41-
MODULE CODE		LAST EDIT	December, 2, 2003 1:43:54 PM	PAGE	1	OF 2

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DRAW	PARK, RYAN	DATE	12/2/2003	TITLE	CICHLID TOUCHPAD I/F BOARD UNDEFINED	SAMSUNG ELECTRONICS
CHECK	OH, H.S	DEV. STEP	DV			PART NO. BA41-undef ined
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST EDIT	December, 2, 2003 1:44:53 PM	PAGE	2 OF 2	